Building heterogeneous networks of green base stations on TI’s KeyStone II architecture

Heterogeneous networks

Even though mobile data usage has increased exponentially, the Average Revenue Per User (ARPU) has not increased accordingly. One way to improve this situation is to reduce operator costs. In the heterogeneous networks of tomorrow, small cells will increase data rates and capacity while the larger macro cells will ensure extensive coverage. To be successful these heterogeneous networks must be cost effective, allowing operators to maintain or augment profitability while giving them the ability to upgrade their networks easily and efficiently in order to meet escalating data communications demands. Other factors that will affect operator profits will be the deployment of scalable and open platforms to accommodate the evolution of technology in the future and which will allow the effective roll-out of new revenue-generating services.

Another way for operators to achieve cost-effective mobile connectivity would be to upgrade existing radio access technologies to support higher data rates. This might involve redeploying the spectrum to achieve improved spectrum efficiency with the same remote radio head (RRH) and cell site infrastructure. The deployment of LTE/LTE-A networks with its simpler network architecture and greater spectrum efficiency will also benefit operators that are attempting to keep pace with subscriber demand. These changes would require infrastructure hardware that can support multiple 2G/3G/4G radio access standards. In turn, this would ease the migration from one generation of technology to the next.

A homogenous network made up solely of macro cells would be challenged to meet the demands of increased data throughput and extensive coverage. This is why operators are looking to blend small cells, cell edge relays and macro cells to improve overall performance of mobile networks, as shown in Figure 1 on the following page. This blending of cell size in heterogeneous networks will be much easier if operators deploy hardware that easily scales from small to macro cell sizes and which is easy to use and install. Of course, small cells will add more base stations to the network, but they have the potential to improve the overall energy efficiency of the infrastructure. Achieving these goals can be accomplished more effectively when the base station equipment deployed by operators shares a low-power,
high-performance and scalable architecture that capitalizes on hardware and software design re-use across network elements. Taken together, these factors will help operators expand capacity while managing both capital expenses (CAPEX) and operating expenses (OPEX).

Base station equipment based on this notion of an open platform will also form an effective basis for operators to add innovative services which can generate new revenue streams. As such, the equipment must also be based on intelligent and flexible hardware which can be programmed with advanced software development techniques so that the operator’s return on investment in equipment will be maximized. To achieve this, one approach would be to reserve a core (or two) from a multicore system-on-a-chip (SoC) for applications developed by the operator. Another alternative would be to implement an application that enables a flexible multicore programming model on an open platform.

TI’s KeyStone II advanced multicore architecture was created to meet the challenges of heterogeneous networks. As a multicore architecture it enables wireless network solutions for small to macro cell sizes. KeyStone II is the first mobile infrastructure processor that integrates clusters of four ARM® Cortex™-A15 cores while providing high performance at less than half the power consumption of traditional reduced instruction set computing (RISC) cores. This is a critical factor for the green network infrastructure equipment of the future.

Initially, KeyStone II will be implemented in TI’s upcoming 28-nm devices for infrastructure applications. It features robust hardware-based accelerators (AccelerationPacs) for speeding up multi-standard Layer 1 baseband, Layer 2 and 3 network and security, and transport functions. AccelerationPacs operate independently to minimize DSP and ARM core and reduce latencies. The KeyStone II architecture is scalable to the point where the 32 cores it supports can be configured in any combination of cache-coherent ARM A15 clusters (four cores to a cluster) and TMS320C66x DSP cores. In addition, Multicore Navigator in KeyStone II

**Figure 1. Heterogeneous network topology**

**KeyStone II multicore architecture**

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Texas Instruments has been enhanced with 16,000 hardware queues, one million descriptors, and integrated hardware-based intelligence for scheduling and load balancing. An enhanced shared memory controller capable of switching 2.8 terabits per second (Tbps) provides low latency for accessing external memory. The 2.2-Tbps TeraNet switch fabric for non-blocked data movement is also an essential part of KeyStone II. Together these innovations provide all of the multicore capabilities needed for heterogeneous network solutions. Figure 2 above presents a functional diagram of the KeyStone II architecture.

TI’s KeyStone II architecture supports multiple radio standards such as LTE/LTE-A, HSPA+, WCDMA, WiMAX, CMDA and GSM. Moreover, simultaneous dual-mode operations with, for example, LTE and WCDMA executing at the same time, is also supported. The architecture’s Symbol Rate Radio Coprocessors include WCDMA transmit (TAC) and receive chip rate acceleration (RAC). Symbol rate processing for LTE is performed by FFT coprocessors for OFDM processing and frequency domain equalization. The Bit Rate Radio Coprocessors (BCP, TCP3, VCP2) included in KeyStone II are the multi-standard turbo decoder/encoder, rate matcher/dematcher, modulation/demodulation, interleaver/de-interleaver, correlator and Viterbi decoder. These hardware-based accelerators provide the equivalent processing capacity of more than 100 1-GHz DSPs. With this level of processing power, low latency baseband processing is assured while delivering space and cost efficiencies in low-power SoCs. To maximize power amplifier (PA) efficiency, reduce the system’s bill of materials (BOM) cost and lower power consumption, KeyStone II’s Digital Radio AccelerationPac speeds up the execution of the digital up and down converter (DDUC), crest factor reduction (CFR) and digital pre-distortion (DPD).
In addition to radio layer 1 hardware acceleration, AccelerationPacs are also available for layer 2, layer 3 and transport processing. KeyStone II doubled the acceleration of security processing throughput from the previous generation for both air interface ciphering and IPSec. When coupled with the ARM® A15 quad CorePac, KeyStone II enables a complete base station with multiple network RF interfaces on a single chip. KeyStone II deploys standard ARM cores, but they are enhanced with four times the internal interconnect bandwidth, twice the data path (256 bits) and double the clock rate of standard ARM cores.

KeyStone II implements an intelligent chip infrastructure with large on-chip memory, including private L2 memory for each C66x DSP core and shared L2 memory for the clusters of ARM cores. Moreover, up to 6 MB of memory is shared across DSP and ARM cores, while other additional memory is embedded in AccelerationPacs and coprocessors. In total, the on-chip memory of KeyStone II provides the fast access and throughput required by high-performance applications. This on-chip memory delivers extremely low processing latencies, which is essential for providing the improved mobile user experience that wireless operators are seeking.

KeyStone II’s new shared memory controller features 2.8 Tbps of throughput and switching capacity, and it connects directly to external DDR3 memory. This reduces the latencies typically associated with external memory accesses and eliminates the need to move system data traffic over the architecture’s TeraNet central switching fabric. TeraNet is capable of 2.2 Tbps of throughput, which will support non-blocking data flow among all of the cores in the architecture. This means that processing elements can operate near full capacity. Processing cycles will not be wasted since cores will not be idled while they wait for data to process. Multicore Navigator has also been enhanced to support 16,000 hardware queues with eight integrated hardware-based programmable elements for scheduling and load balancing. Advanced multicore programming models can be effectively deployed with the help of Multicore Navigator to achieve maximum multicore efficiency. These enhancements also facilitate the easy software upgrades and rapid service additions that will be required by operators of next-generation heterogeneous mobile networks.

The input/output (I/O) subsystem in KeyStone II features the high-speed 100-gigabits per second (Gbps) Hyperlink interface for interconnecting devices with the KeyStone architecture and allows equipment manufacturers to scale their solutions to fit a particular set of requirements. Hyperlink provides seamless chip-to-chip interconnection without the added complexities of protocol transcoding. Neighboring devices are simply accessed through a fast and efficient extended memory mapping mechanism. In addition, an antenna interface (AIF2) with six links and arranged as a switch enables connections to remote radio heads and also provides the ability to aggregate and distribute antenna traffic based on the requirements of the network topology. This eliminates the need for a costly external antenna-switching mechanism. Four external Ethernet links implemented as a four-port switch function in concert with the Network Coprocessor and ARM subsystem to deliver full-featured network processing capabilities. Integrating these capabilities with KeyStone II devices eliminates the need for power-hungry external network processors and Ethernet switches. This also reduces both the system’s BOM cost and power consumption.
The flexible configuration of DSP cores, ARM® cores, AccelerationPacs and I/O in KeyStone II provides a palette of capabilities from which SoC devices are created. And these devices will, in turn, deliver the performance and reduced cost required by base station equipment manufacturers for small and macro cell base stations, as well as other heterogeneous network elements as shown in Figure 3.

Recently published operational data from China Mobile indicates that only half of the power consumed by a wireless base station is dedicated to Radio Access Network (RAN) equipment. The remaining half is consumed by air conditioning[2]. Since heterogeneous networks will be populated by a large number of small cell base stations, operators will require that these base stations conserve energy.

KeyStone II features low-power ARM® A15 RISC cores, C66x DSP cores and AccelerationPacs, as well as many advanced power management capabilities. For example, each subsystem has its own clock and power domain so that system partitions can be efficiently powered down when they experience idle or low traffic conditions. Each memory subsystem has retention-until-access (RTA) capabilities that dramatically reduce memory power consumption. KeyStone II’s scalable power domains feature TI’s SmartRefl ex™ technology with its Dynamic Voltage and Frequency Scaling (DVSF) capabilities. These enable dynamic voltage scaling to achieve maximum performance at the lowest practical input voltage. Collectively these smart power technologies can reduce a SoC’s power consumption by half and enable new levels of power efficiency in base station design.

Multiple devices based on the KeyStone II architecture can be connected via Hyperlink to form a farm of multicore SoCs for macro base station or cloud RAN purposes. To adapt quickly to different traffic and application conditions and thereby reduce the static and dynamic power dissipation, the multiple devices in a farm configuration can run in different energy-saving modes with varying smart power management techniques. Each device can run in any of the operational power modes, active, standby and hibernate. In the active
mode, a device is in fully operational with all cores, accelerators and I/O in the power-on condition. In standby mode, cores are in the idle mode while most accelerators are in the clock-disabled state. L2, MSMC and DDR3 memory as well as the Ethernet subsystem are active for fast traffic recovery. The typical wake up time from the standby mode is less than 25ms. Running in standby mode can reduce the active power by about 30 percent. In hibernation mode, cores are in the static power-down mode and all IPs are in the power-down or clock-gating mode, only MSMC is active. Since the previous system state can be saved in MSMC for fast recovery, typical wake up time from hibernation mode is less than 100ms. Running in hibernation mode can reduce active power consumption by about 50 percent. Figure 4 illustrates a KeyStone II farm running in different power-saving modes.

Figure 4. KeyStone II farm power saving modes in low traffic condition

**Conclusion**

The KeyStone II architecture offers twice the capacity and performance of its field proven KeyStone predecessor. With new levels of cost-efficiency, this new generation of the KeyStone architecture empowers every network element in the heterogeneous networks that will dominate the wireless industry in the future. Advanced power performance based on TI’s SmartReflex power management technology enables green base stations to contribute to a healthier planet. KeyStone II’s Multicore Navigator provides an advanced multi-core programming paradigm to increase software development efficiency with innovative new techniques for scalability and reusability while maintaining compatibility with popular multicore programming models. With KeyStone II, TI continues its legacy of innovating for base station developers with unprecedented and unmatched performance and functional integration.

**Reference**

[1] Tom Flanagan, “Creating cloud base station with TI’s KeyStone multicore architecture”


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