Introduction

A typical industrial system requires control, application and connectivity capabilities. The control subsystem directly manages motor operation and feedback, the application directs the overall motion, and the connectivity subsystem downloads application, control data and allows the system to be remotely managed.

In general, the core technology that makes up the foundation of each of these subsystems is clearly understood. At the high end, developers continue to innovate new ways to improve overall performance and accuracy. As these technologies mature and the cost to implement them decreases, these solutions that were available for high end applications work their way down the value chain.

The challenge that developers of next-generation systems face today is efficiently implementing incremental innovations to provide better performance with lower latency and greater precision for their target application. To expand market share, they need to deliver better functionality such as new feedback algorithms or novel approaches that improve position accuracy and current sensing at lower costs.

To achieve this, processors offering higher performance and greater integration are required; however, this approach increases development costs and adds system complexities which in turn delay time-to-market and ultimately reduces the competitive advantage of delivering next-generation designs. Implementing new technology must be seamless, simple and value added both to developers and end users.

Designing the Next Generation of Industrial Drive and Control Systems

A New Architecture for Next-Generation Industrial Designs

Many original equipment manufacturers (OEMs) have traditionally relied upon field-programmable gate-array (FPGA) technology to push leading edge performance of critical functions like torque loop management. FPGAs, however, increase system cost and are difficult to program. In addition, FPGAs offer a relatively fixed implementation that lacks scalability across multiple applications without requiring a redesign.

The dual-core C2000™ Delfino™ F2837xD MCU from Texas Instruments (TI) makes it easy to implement various mathematical transforms-and-trig-heavy computations that enable efficient torque loop management in a programmable processor platform. The dual-core Delfino F2837xD is also designed to maximize hardware and software performance for industrial drive and control applications. For example, its fast torque loop calculation can reach sub 3 uS, which is comparable to FPGA implementations.

The F2837xD MCUs extend control loop performance with their fast CPUs further boosted by tightly coupled accelerators. The dual-core MCU is based on TI’s proven C28x CPU. Each CPU core provides 32-bit floating-point processing capabilities at 200 MHz, and dual real-time control accelerators (CLAs) also running at 200 MHz each. Each C28x CPU is augmented by its own Trigonometric Math Unit (TMU) accelerator that provides hardware-based acceleration useful for control-based tasks. These four powerful engines are capable of pounding out the equivalent of 800 MIPS or 1600 MFLOPS of performance enabling consolidation of multi-processor architectures in control loop systems (Figure 1).

![Figure 1 – Before C2000 Delfino F2837xD MCUs, industrial drive systems were complicated and expensive.](image)
For example, in industrial drive applications one CPU (with TMU) + CLA can be used to implement control-side functionality; i.e., the torque loop. The other CPU (with TMU) + CLA can be used to implement the application side of the system; i.e., tracking speed and position, computing trajectories, comparing motion profiles and so on.

This division of the industrial drive system into control and application segments between CPUs provides developers with a clean partitioning to simplify design. Because only control code is running on one of the CPU, it is isolated from application code, thus developers do not need to spend valuable development hours mitigating the potential impact of application code on the responsiveness and latency of real-time tasks (Figure 2).

The Delfino F2837xD MCUs enable developers to migrate high-end functionality down the value chain to mid- and low-range applications. It achieves this through a combination of innovative technologies, including:

- Greater processing capacity at a lower cost than the current solutions
- A streamlined, low-latency architecture that provides higher performance in a deterministic manner
- Advanced hardware-based engines that accelerate common but compute-intensive tasks
- Integration of essential functions into the processor’s architecture to reduce external component count and cost
- Simplified new design migration and reuse of an OEM’s existing code investment

The F2837xD is an MCU powerhouse enabling 800 MIPS of total system performance. This is provided through dual C28x CPUs and dual CLAs. The CPUs also integrate hardware accelerators which enable swift execution of trigonometric based control functions and complex math operations common in encoded communication applications. These hardware accelerators include:

- **Trigonometric Math Unit (TMU)**: TI developed the TMU hardware accelerator to assist the main C28x CPU execute trigonometric functions like SIN, COS, ATAN and 1/X that are commonly used in applications such as robotic motion where hinged joints require linear to angular translation.
These complex functions are computationally intensive and typically require 30 to 90 cycles to complete even when using a CPU with traditional floating-point capabilities.

The TMU can be used as a high octane accelerator to perform floating-point unit calculations in parallel to the CPU. With an average execution time of five cycles per instruction, the speed of math transforms requiring trigonometric calculations can achieve 5X improvement in performance when the TMU is used (Figure 3).

- **Viterbi Complex Unit (VCU II):** This accelerator efficiently processes complex math functions (Figure 4). The VCU accelerates the performance of communications-based algorithms by as much as 10 times and provides headroom, as well as provides headroom for future system growth and higher bit rates, or conversely, enables devices to operate at a lower MHz to reduce system cost and consumption. The VCU II with acceleration is ideal for power line communication (PLC) algorithms in smart grid applications, such as OFDM interleaving and de-interleaving, Viterbi decoding, CRC calculations and more. It increases performance in narrowband PLC standards and supports smart grid advanced meter infrastructure networks (PRIME, G3 and IEEE-P1901.2). The VCU II in industrial drives can better predict motor failures by performing vibrational analysis on motors to increase operational efficiency and reduce downtime.

Along with the TMU and VCU II hardware accelerators, the F2837xD MCUs include dual real-time CLAs which enable intelligent partitioning of critical control tasks in a drives system.

- **Real-time control accelerator (CLA):** The CLAs are standalone, floating-point processors that are tied to the main CPUs. CLAs are dedicated low-latency CPU like architecture with direct access to control peripherals. They are pure mathematical engines that operate independently of the main CPU.

The CLAs can be used in a variety of ways to completely offload intensive signal processing tasks from the CPU (Figure 4). For example, the CLA can serve as part of an analog-to-digital converter’s (ADC’s) front-end and pre-process incoming signals to filter noise and then buffer data in its own random access memory (RAM). In this way, the CPU is involved only when there is an entire block of pre-processed data ready for it to work. Another way to use the CLA is by performing signal analysis on incoming current wave forms, the CLA can then profile a motor’s real-time performance. The profile can
be continuously compared to a “golden signature” based on the type of motor. As the profile begins to deviate from the expected signature, indicating a potential fault, the industrial drive system can alert the operator to take preemptive action before failure occurs. Other tasks the CLA can perform are feedback pre-processing, feed-forward control and special signal analysis or packet processing. These are just a few examples of the many possible features that can be implemented using the CLA.

Although performance is required for industrial drives, overall system design also needs to be simplified. When enhancements increase design complexity, this in turn could increase the development time. For example, determinism is essential for control-based applications. Determinism means how feedback signals are sampled, processed accurately and arrive in time for control loop actuation using the pulse-width modulation (PWM) signals. With the loosely coupled memory architecture of a cache-based processor, determining worst-case responsiveness that accounts for unpredictable cache misses is a difficult calculation to make. Typically, designers must rely on profiling real-time execution of the system to confirm worst-case operation. This means that modifications to system code may require the system to be profiled multiple times to ensure the limits of the system have not been exceeded. This determinism also carries over to the Delfino F2837xD MCU’s peripherals. The latency of the ADCs is known, as is how long the CPU needs to update the PWMs. This greatly simplifies overall system design because there is no need to guess what the worst-case execution path is.

The Delfino F2837xD MCU architecture is built upon its deterministic foundation that allows developers to ensure reliability without increasing design complexity. With its tightly coupled memory architecture, there is no need for a cache, thus eliminating the associated delays that arise from cache misses. All memory transactions to static random-access memory (SRAM), Flash, and peripherals are designed to fit within finite busing structure and cycles, thus providing deterministic throughput. The dual six-channel direct memory access (DMA) peripheral augments an efficient memory management to ensure data is always available when the CPU or the accelerators needs them.

Figure 4—The CLA can increase frequency or number of control loops, offloading the C28x to perform more background control and system tasking.

Low-latency and Deterministic Architecture
To facilitate efficient communication between cores, the Delfino F2837xD uses shared memory where both cores have full read/write access to data. Developers also have access to two message RAMs. Each core has write privileges to one of the message RAMs and read-only privileges to the other. In this way, code on one core cannot accidentally corrupt critical data belonging to the other core. This greatly simplifies messaging, especially for developers new to dual-core design.

There are several error-check functionalities that are spread across the subsystems in Delfino F2837xD MCU architecture. Non-volatile memory and SRAM offer ECC and parity capabilities. Device level diagnostics are collated to generate flags, interrupts and external error signal. System level functional safety are becoming critical in industrial drive systems. These built-in error check mechanisms enable power up and run-time application level diagnostics. This will improve system level integrity for a low cost and help deploy several functional safety topologies.

The hallmark of the Delfino F2837xD devices are the control peripherals. These are the powerful industry-proven PWM timers, 32-bit Enhanced capture units (ECAP) and Quadrature Encoder Pulse (QEP) peripherals. Each of the PWM modules is enhanced to support high resolution capabilities on both A and B channels. These high-resolution channels extend 150ps PWM step resolution to enable high-frequency PWM modulation techniques and advanced control topologies.

Performance is directly impacted by the precision of the PWM control feedback loop. Integrated analog peripherals reduce latency and cost compared to the use of external components. In higher end control applications such as servo drives, high-resolution feedback is required to provide precise phase current measurements for low-torque ripple and precision positioning; however, for some measurements, precise sample rates are more important than higher resolution, such as when making high-speed, low-side shunt current measurements.

To support different accuracy requirements, the Delfino F2837xD MCU architecture offers flexible ADCs that can support two resolution modes: 16-bit resolution at 1.1 MSPS and 12-bit resolution at 3.5 MSPS. The F2837xD features four independently integrated ADCs that provide simultaneous conversions, thereby enabling industrial systems to accurately monitor multiple signals in real time (Figure 5.) For example in a servo drive, designers can monitor the voltages and currents of a three-phase motor while simultaneously software decoding high-frequency feedback from a resolver.

Delfino F2837xD MCU offers three 12-bit buffered digital-to-analog converters (DACs) to provide analog actuation signals and tracking engineering parameters at the system level. Further increasing integration is the availability of eight sigma delta demodulators/filters. Because of the high voltages associated with industrial motor control, isolation is required when measuring feedback signals. Developers can use TI’s AMC120x delta sigma convertor, for example, to convert analog values into a digital bit stream that feeds directly into Delfino F2837xD MCU’s sigma delta interface and is reconstructed by the demodulator. This enables hot-side/high-side current sensing of motor phases, providing the feedback fidelity that is essential in high-performance industrial drives.

Eight windowed comparators are integrated into the Delfino F2837xD MCU architecture, providing “trip points,” and operate independently from the CPU so there is no additional CPU loading. The comparators are
also fast acting and CPU independent to minimize latency with trip signals so the system can react quickly to any abnormal events or over/under limit conditions. The comparator trip events can be configured to help provide a full shut down action in the case of a catastrophic event, making the system more resilient in industrial drive and power systems.

Multiple processing units and accelerators can substantially improve system performance. However, many OEMs are building on existing designs and have made a significant investment in developing a code base with Delfino and other MCUs. TI understands that developers need to be able to exploit architectural enhancements seamlessly with simplified partitioning in the firmware. Use of the TMU, for example, is managed by the C compiler. When a native TMU function is available for use, the compiler will automatically utilize the TMU instead of calling a function from the math library. Thus, existing C28x-CPU-based designs can take immediate advantage of the TMU’s 5X performance boost without any code needing to be rewritten. The TMU can boost the performance of MathLAB/Simulink-based application code as well. This also improves portability of intellectual property (IP) since the same code can be used with TI MCUs with and without a TMU capabilities. The memory subsystem offers a very flexible code protection mechanism to help vendors and developers to exchange valued added IPs.

To accelerate development, TI and its partners offer a wide variety of software libraries, tools, development kits and technical support as part of its extensive development ecosystem. For example, math libraries are available for both the CPU and CLA to assist developers in getting the highest performance from the Delfino F2837xD MCU. TI also provides a wide range of low-level and application-specific libraries to accelerate design of control applications, as well as development boards that provide developers with easy access to all of the Delfino’s F2837xD control-based functionality.
For applications that require communications, the Delfino 37x MCUs provide several serial ports, such as high speed peripheral interface (SPI), which are used for inter-processor connectivity and network connectivity. Other serial ports include USB, CAN, UART and I2C.

For applications that require Ethernet and real-time Ethernet connectivity and protocol, TI’s Sitara™ AM335x processors are available as companion communications processors. The Sitara AM335x devices are built around an ARM® Cortex®-A8 core with differentiated peripherals and certified industrial communication stacks/protocols, such as Profinet, EtherCAT and more. These devices are fully featured to support the ARM ecosystem for extended application processing, if required.

The Delfino F2837xD dual core devices also offer a pin/-software compatible scalable derivative to meet varying performance ranges and cost points. This scalable platform enables designers to leverage existing software and hardware developments and create a portfolio of products ranging from a high end servo drive for factory automation to an AC inverter targeted at industrial pumps.

**Conclusion**

With the Delfino F2837xD MCU, TI has redefined how industrial drives are designed. With its focus on performance, integration, simplicity and transparency, the Delfino F2837xD MCU architecture enables developers to implement proven control systems with next-generation capabilities. Its advanced hardware-based engines and high level of integration provide greater performance at a lower cost and smaller system footprint. Developers can also speed time-to-market by leveraging future single core derivatives which will provide a pin- / software-compatible platform with varying performance ranges. The single-core options allow designers to enjoy many features of the F2837xD platform in a cost-optimized format.

Get started evaluating and developing today with tools from TI using an F28377D Experimenter’s Kit (TMDXDOCK28377D).

This kit has the following features:

- 180pin controlCARD interface
- All key signals routed through the connector interface
- Can be used in existing 100pin controlCARD EVMs via the TMDSADAP180TO100 adapter
- Built-in Isolated xds100v2 JTAG Emulator
- Option for External JTAG emulator
- UART connectivity via USB
- USB host/device
- ADC clamping
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