

# Optimizing Synthetic Aperture Radar design with TI's integrated 66AK2L06 SoC



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## Overview

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High-performance avionics and defense applications, including radar, are sensitive to power consumption constraints that characterize most airborne systems. In an operating environment with finite power budget, setting the optimal balance between processing performance and power consumption is critical for every onboard embedded system. These systems have the industry's longest product life cycle, often measured in decades rather than years making reliability and longevity also key factors in selecting embedded systems.

Applications such as electronic warfare, signal intelligence, countermeasure, military, surveillance and weather radars, military aircraft and generic aviation-control systems all demand high-throughput, high-speed data acquisition and processing. Prior to distributing the data to the end user in real-time, these systems need to be capable of extracting the maximum amount of data from the signals then applying powerful signal processing algorithms on the raw data to improve accuracy and precision. This white paper specifically focuses on radar applications, which use the modern radar technology called "synthetic aperture radar (SAR)". Texas Instruments (TI) 66AK2L06 System-on-Chip (SoC) enables designers of radar applications to deliver game-changing enhancements in system cost, size, weight and power (**SWaP**) with improved performance over their current solutions. Integration of JESD204B interface to the 66AK2L06 SoC not only reduces the complexities of system design, but also reduces the board space requirements for radar applications. The SoC's integration of a programmable digital front end (DFE) enables adaptability and scalability to meet constantly evolving high-speed data acquisition and generation requirements. The developers can take advantage of the Fast Fourier Transform Coprocessor (FFTC) on the SoC to further optimize the latency of SAR algorithms. Together, the enhanced performance, lower power, smaller footprint can reduce the overall system costs by up to 50 percent and board area by 66 percent. Learn more about 66AK2L06 SoC [here](#).

### 1. **SWaP constraints eliminated via new TI SoC**

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**Synthetic aperture radar** has become the premier sensor for aircraft or spacecraft mounted imaging due to its sensitivity, accuracy, independence of weather and atmospheric conditions and subsurface penetration. This complex radar system requires large digital processing capabilities, due to

intensive signal processing. The **SWaP** constraints of the physical environment impose a high level of efficiency on the implementation of digital signal processing (DSP) algorithms. Adaptability is also vital in the implementation as SAR design and data usage requirements are constantly evolving. Higher levels of implementation efficiency and adaptability requirements mean that System-on-Chips (SoCs) combining programmable DSP cores with dedicated accelerators have become the processing platform

of choice. The SoC solution offers unmatched signal processing capacity at very low power levels, supporting avionics and defense (including radar), test and measurement, medical and other industrial applications.

TI's KeyStone™-based multicore devices are at the heart of SWaP efficiency, with their cost-effective performance and low power consumption. Of particular note is the new TI 66AK2L06 SoC, which delivers breakthrough performance and SWaP efficiency to the designers of avionics and defense systems. Based on TI's new KeyStone II multicore architecture, the 66AK2L06 SoC integrates a mix of processing elements including TI fixed- and floating-point TMS320C66x DSP cores, fastest ARM® Cortex®-A15 cores and advanced accelerators. The 66AK2L06 SoC is equipped with high-speed **JESD204B** interface for **direct connectivity** to TI's high-speed analog-to-digital converters (ADC), digital-to-analog (DAC) converters and analog front ends (AFE). Integration of a software-programmable DFE for digital conversion and digital filtering eliminates the need for what would otherwise be a set of discrete components (as per current competing solutions), further reducing power and board space, yielding the best power per watt in a small footprint.

## 2. No more sacrificing performance to gain floating-point accuracy with DSP cores and KeyStone II architecture

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The use of multiple **DSP cores** is a key technique which facilitates increasingly sophisticated signal-processing algorithms to advance the vanguard of waveform-intensive applications, such as avionics, radar, sonar, test and measurement and

beamforming. Multicore capabilities, combined with an expanding array of **AccelerationPacs** and development tools for multicore DSPs, enable high performance at exceptionally low power in compact form factors. Avionics and defense applications need multicore DSPs to meet the advancing requirements of these mission-critical applications including higher processing throughput, finer resolution,

*Of particular note is the new TI 66AK2L06 SoC, which delivers breakthrough performance and SWaP efficiency to the designers of avionics and defense systems.*

increased accuracy and the integration of advanced interfaces. Many of these functions rely on floating-point math to achieve the required precision. TI's KeyStone II architecture offers significant flexibility to the designer by providing floating- or fixed-point execution within a single device on an instruction-by-instruction basis. Significantly, the floating-point operations execute at clock rates up to 1.2 GHz for this architecture; these rates were previously reserved for fixed-point devices only. Designers no longer have to sacrifice performance to gain floating-point accuracy or complicate designs with separate fixed- and floating-point processors<sup>[1]</sup>.

The key objective behind the KeyStone II platform is to provide connectivity, abundant throughput and on-chip resources so that the processing cores will be able to reach their optimum processing performance without constraints<sup>[2]</sup>. Referred to as multicore "entitlement," this empowering of the processing cores is achieved by the architecture's capability in providing non-blocking access to all processing cores, peripherals, coprocessors and input/output (I/O) channels. Key aspects of the KeyStone II architecture are its Multicore Navigator, TeraNet and Multicore Shared Memory Controller, leading to a highly flexible and scalable solution for **JESD-attach** applications.

### 66AK2L06 key features:

- Two ARM Cortex-A15 RISC cores @ 1.2GHz with 8400 DMIPS; These ARM cores provide high-performance RISC processing at ultra-low power consumption levels to handle control and housekeeping functionalities
- Four TMS320C66x DSP cores @ 1.2GHz with fixed- and floating-point processing providing 76 GFLOPs and 153 GMACS
- Integrated DFE technology (programmable filtering, IQ imbalance correction, up sampling / down sampling, etc.) offloads a lot of heavy signal processing
- Advanced integrated network coprocessor offloads IP routing and IP termination from ARM/DSP cores, allowing greater system differentiation and efficient support of encryption and security.
- **FFTC** improves latency for **FFT/inverse FFT** (IFFT) execution up to 8K-points with better performance than the fixed-point DSP core implementation
- Integral Multicore Shared Memory Controller (MSMC) with 2MBytes of memory shared by the cores and the accelerators
- Multicore Navigator offers operation of single-core simplicity to multicore SoC software design
- Ethernet switch with 4x 1GbE ports
- Two one-lane PCIe Gen2 interfaces supporting up to 5 GBaud
- Highly integrated SoC reduces bill of material (BOM) costs, system size and power consumption
- High-speed JESD204B chip-to-chip interface optimizes board layout (fewer lanes, fewer pins) and reduces power consumption supporting up to four lanes (Max SerDes speed of 7.37 Gbps line rate) interface to multiple ADCs/DACs/AFEs

## 3. High-performance I/O and AccelerationPacs contribute to SWaP improvements

### JESD204B

In addition to greater integration at the silicon level, the 66AK2L06 SoC enables a smaller BOM, reducing board production costs. This is due to the simplified circuit board design and layout through the use of a JESD204B serial communication link interface. JESD204B provides a high-throughput, low-pin-count serial link between data converters (ADC/DAC), on-board logic devices such as field programmable gate arrays (FPGA), DSPs, SoCs and application specific integrated circuits (ASIC).

By embedding the clock in the data stream and including certain embedded algorithms to optimize the sampling of data bits, JESD204B simplifies routing between devices because significantly fewer lanes are needed on the board. By comparison, to

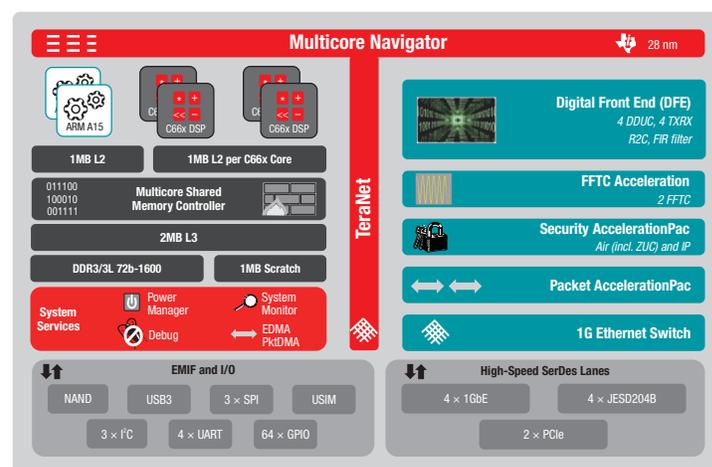


Figure 1: 66AK2L06 SoC block diagram

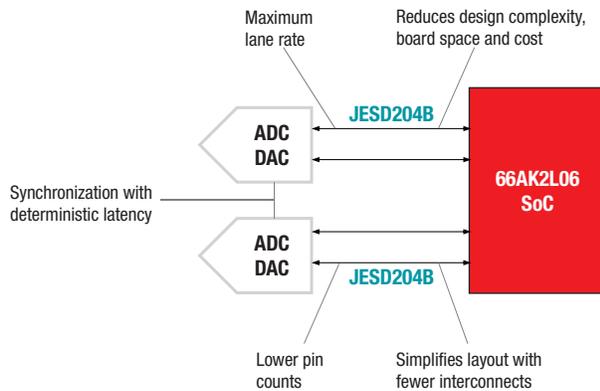


Figure 2: JESD interface benefits

achieve the same throughput as JESD204B, the more prominent SerDes interfaces, such as PCI Express (PCIe) would require more lanes on the board. Fewer board lanes mean that the number of I/O channels on devices are also reduced, resulting in lower pin counts and allowing smaller package sizes. In addition to simplifying the system design, JESD204B shortens circuit board bring-up by reducing the setup and hold times that are

usually performed across the many more lanes typically employed by other SerDes interfaces such as PCIe and low-voltage differential signaling (LVDS). JESD204B is a flexible and scalable serial link interface that can accommodate a wide range of data transfer speeds and configurations, such as multiple ADCs or DACs on one JESD differential pair.

## Digital front end (DFE)

By integrating the DFE, the 66AK2L06 SoC combines all the high-throughput digital processing into one optimized software-programmable processing unit that includes control, baseband and DFE. As a result, the SoC is able to perform a variety of functions on-chip, from fundamental signal-processing including channelization/decimation and re-sampling, to exponential complex multiplications, filtering and FFT/iFFT, which are essential to synthetic radar processing algorithms. Designers of radar systems can now benefit from

### Key DFE features:

**Channelization and data-converter interface functions** – these are mandatory signal-processing functions to be performed with most types of applications:

- Carrier filtering to comply with standardized spectral emission masks
- Tuning and channel aggregation and distribution
- JESD204B SerDes interfaces to TI high-speed ADCs and DACs
- The Baseband (BB) block provides:
  - Programmable complex gain per channel for transmit data
  - Programmable circular clipper for transmit data
  - Programmable back-end automatic gain control (BeAGC) for receive data
- Programmable power measurement options for both TX and RX channels
- Supports up to 24 RX channels and 24 TX channels
- Provides loopback functionality
- The digital down up conversion (DDUC) provides:
  - Multi-channel up/down conversion
  - Flexible input/output sample rates
  - Programmable resampling options
  - Programmable FIR to meet spectral mask requirements
  - Gain, phase and fractional delay adjustment per channel

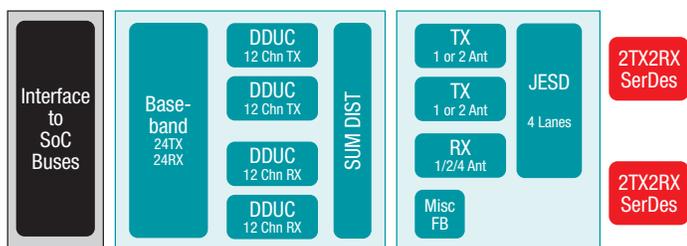


Figure 3: DFE block diagram

the on-chip digital up/down conversion, filtering and the efficient high-speed connectivity to the latest high-speed ADC/DACs<sup>[3]</sup>. See Figure 3.

## FFTC

The FFTC module is accessible across all four C66x cores on the 66AK2L06 SoC. This module can be used to accelerate the FFT and iFFT computations that are required in various applications hence freeing up DSP core cycles for other processing.

The FFTC provides the following features<sup>[6]</sup>.

- iFFT and FFT processing for the following sizes:
  - $2^a \times 3^b$  for  $2 \leq a \leq 13$ ,  $0 \leq b \leq 1$  – maximum size 8192
  - $12 \times 2^a \times 3^b \times 5^c$  for sizes between 12 and 1296
- 16 bits I / 16 bits Q input and output
- Throughput varies slightly depending on the FFT size. Example of an FFT of 4096 points, it can be processed by a single FFTC at a throughput of 525 Msps for a 1.2-GHz device.
- SNR ranging from 84 to 100dB depending of the FFT size
- Dynamic and programmable scaling modes
- Dynamic scaling mode returns block exponent
- Support for “FFT shift” (switch left/right halves)
- Support for cyclic prefix (addition and removal)
- Ping/Pong input, output buffers
- Input data scaling with shift

- Output data scaling
- Zero padding

## 4. Optimizing SAR applications with the 66AK2L06 SoC

### SAR requirements

SAR is a form of radar which is used to create images of an object, such as a landscape. Typically a SAR system is mounted on a moving platform such as an aircraft or spacecraft, operating by transmitting a succession of microwave pulses; the echo of each pulse reflected back to the radar is then collected by a receiver and recorded. A SAR system uses the distance travelled by the SAR antenna over a target region to “synthesize” a larger antenna aperture (“size” of antenna), providing finer spatial resolution than possible with conventional beam-scanning radars. Signal processing of the recorded radar echoes then combines the recordings from the multiple antenna locations to create the image.

As radar wavelengths are much longer than those of visible or infrared light, a SAR can “see” through cloud, smoke haze, humidity and darkness. Depending upon choice of frequency, it is possible to produce images that penetrate through foliage to map the topology of the land below, or penetrate below the earth’s surface or through shallow water<sup>[6]</sup>. Alternatively, when the illuminating sensor is stationary and the target region is moving, the radar system is called inverse SAR (iSAR).

SAR data is acquired in time domain and is transformed in frequency domain and range Doppler domain where matched filters can be applied. While there are several approaches for

SAR processing, each with its advantages and disadvantages, the range Doppler algorithm (RDA) is a one-dimensional Fourier transform. Another similar approach to RDA, however relying on frequency modulated chirp-encoded signals, is called the chirp scaling algorithm (CSA). A third approach is a two-dimensional Fourier transform algorithm known as the wave equation (WE) algorithm. This two-dimensional WE algorithm processes the range and azimuth data simultaneously whereas the range Doppler processing algorithm implements range compression processing followed by azimuth compression processing. The most commonly employed algorithm in SAR processing systems is the RDA, which is the approach of focus for this paper.

## Range Doppler algorithm (RDA) description

The RDA provides good accuracy of result for low squint cases. Its main steps are:

1. Transform to range domain (range FFT)
2. Range compression
3. Transform to time domain (inverse FFT)
4. Transform to range Doppler domain (azimuth FFT)

5. Range Cell Migration Correction (RCMC)
6. Azimuth compression (Azimuth filtering)
7. Image reconstruction

Range and azimuth compression are both correlation processing, realized as two one-dimensional matched filter operations. The first matched filtering operates on the single pulse radar returns and the second matched filtering operation operates on the Doppler signal<sup>[7]</sup>. Figure 4 shows the basic concept of the SAR processing based on the range Doppler processing algorithm as studied in the paper **“Synthetic Aperture Radar on Low Power Multi-Core Digital Signal Processor”** implemented on the C66x DSP cores.

## Range compression

Data is captured and loaded into the 66AK2L06 SoC using its JESD204B RX interface.

Let  $S_0(\tau, \eta)$  be the received data where:

- $\eta = \frac{k}{f_a}$  is the “azimuth time” (slow time between pulses), with  $f_a$  being the azimuth sampling rate;
- $\tau = \frac{m}{f_r}$  is the “range time” (fast time within a pulse) with  $f_r$  being the range sampling rate;

The data is stored in the internal shared memory (MSMC) until a trigger is sent to the 66AK2L06

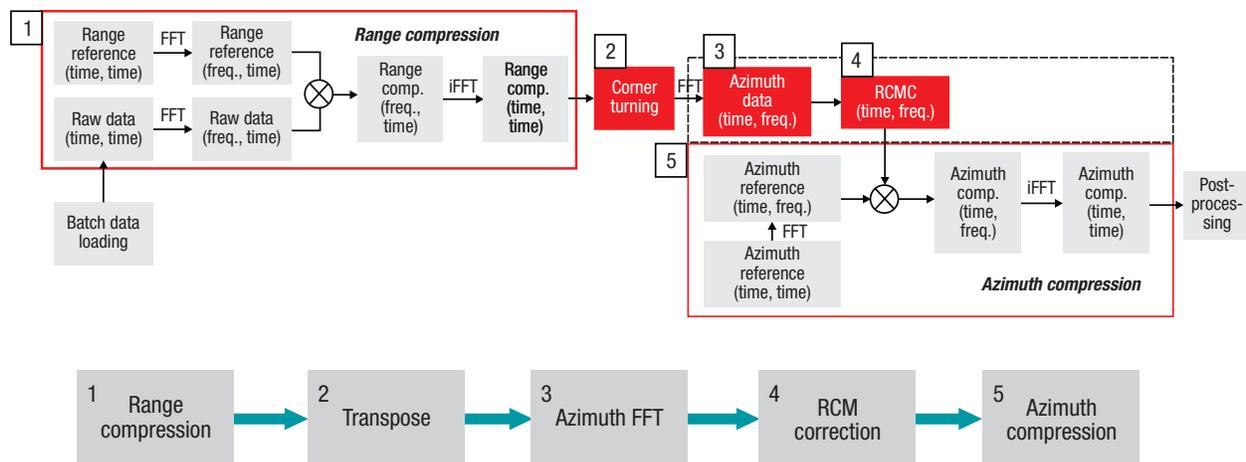


Figure 4: RDA and modularization

platform, to signal the end of a single-pulse capture. Once a complete pulse series is received, range compression processing is triggered.

Range compression is done to compress the received pulse along the range direction to concentrate the main energy into a narrower duration. It is performed with a fast convolution between the raw data and a reference signal in the frequency (range) – time (azimuth) domain. Therefore, **FFT** along the range direction is first performed, followed by matched filter multiplication and range **iFFT**. Match filtering is implemented as **complex multiplications** in the frequency domain.

Range compression is using the following steps on the 66AK2L06 platform:

1. A “range” FFT is performed along the range direction (“rows”) to convert the data. Depending on the expected resolution, it is executed either on
  - A C66x core (floating-point operation – takes ~28  $\mu$ s to process a 4Kpoint FFT)
  - Or on an FFTC accelerator (block floating-point operation – takes ~8  $\mu$ s to process a 4Kpoint FFT)

Resulting data are  $S_r(f_\tau, \eta)$  vectors with  $f_\tau$  being the range frequency.

2. A range-matched filter is applied using C66x DSP cores:

$$H_r(f_\tau) = \exp\left(-\frac{j\pi f_\tau^2}{K_r}\right) \text{ (see [11])}$$

$$S_{mc}(f_\tau, \eta) = S_r(f_\tau, \eta) \cdot H_{az}(f_\tau)$$

3. A “range” iFFT is performed to convert the data in the time domain, resulting data are  $S_2(\tau, \eta)$  vectors.

## Transpose

Also known as corner turning, the transpose function is used to rearrange the compressed data such that it can be read in azimuth line order for processing along the azimuth direction. The range compressed data stored in memory are grouped into blocks, preferably squared size since because memory accesses achieve higher efficiency when the row size of the loading/writing data is no less than the number of rows. To efficiently load/write the data between the external memory and internal memory (L2), the enhanced direct memory access (EDMA3)<sup>[9]</sup> on the 66AK2L06 SoC can be applied to service data transfer. EDMA3 is a unique design of TI’s KeyStone architecture featuring a fully orthogonal transfer on three dimensions with synchronization on two dimensions, flexible transfer definitions, multiple DMA channels and memory protection support.

## Range cell migration correction (RCMC)

Range cell migration is caused by the range variations due to the platform movement (following a hyperbolic trend). The range cell migration correction is to then rearrange the data in the memory to straighten the trajectory such that azimuth compression can be conducted along each parallel azimuth line. RCMC can be achieved by a range interpolation operation based on an interpolation kernel, such as sinc function or spline. In this implementation<sup>[8]</sup> on TI’s TMS320C6678 multicore DSP, the 16-set 8-tap sinc filter is adopted as the interpolation filter. The coefficients of the 16 sets of filters are stored as a constant number. The index of which filter should be selected is determined by the fractional part. The same filter is used for each range cell. The TMS320C66x

DSP's unique double-float load, write and arithmetic instructions are utilized to improve the interpolation computation efficiency.

RCMC is using the following steps on the 66AK2L06 platform:

- An “azimuth” FFT is performed along the azimuth direction (“column”) to convert the data to range Doppler domain, either on DSP or FFTC.
- Resulting data are  $S_a(\tau, f_\eta)$  vectors with  $f_\eta$  being the azimuth frequency.
- A “sinc” is applied to the signal (principle of stationary phase) after estimation of the Doppler frequency  $f_D$

$$S_{RCMC}(\tau, f_\eta) = \alpha S_a(\tau, f_\eta) \cdot \text{sinc}(\beta\tau - \gamma(f_\eta^2 - f_D^2) - \delta).$$

## Azimuth compression

The azimuth compression step compresses the spread energy in the trajectory to a single cell in the azimuth direction. This procedure is similar to range compression except that the azimuth reference function is range dependent. In other words, the azimuth reference function at each range line is different, which leads to a more complicated procedure compared to the range compression. Similar to RCMC, azimuth compression is also performed in range Doppler domain. The final image is obtained by transforming the azimuth compressed signal back to the time domain, followed by some post-processing steps.

1. An azimuth matched filter is applied using C66x DSP cores on the 66AK2L06 platform:

$$H_{az}(f_\eta) = \exp\left(-\frac{j\pi f_\eta^2}{K_a}\right) \text{ (see [11])}$$

$$S_a(\tau, f_\eta) = S_{RCMC}(\tau, f_\eta) \cdot H_{az}(f_\eta)$$

2. A “range” iFFT is performed to convert the data in the time domain, resulting data are  $S_3(\tau, \eta)$  vectors.

## Multicore deployment of range Doppler algorithm on 66AK2L06 SoC

The parallel implementation of the range Doppler algorithm using the four C66x DSP cores in the 66AK2L06 SoC can be achieved by allowing each core to process a different portion of the data. The algorithm presents a high level of parallelism which can be used to efficiently deploy the processing tasks over different cores using **openMP**<sup>[10]</sup> to achieve load balancing as well as minimize the processing latency.

Leveraging the hardware accelerators on the 66AK2L06 SoC provides multiple benefits ranging from freeing up cycles on the DSP cores for extra processing functions to reducing the total application latency. The DFE can offload multiple types of processing before handling the SAR algorithm. The received signal out of the ADC is a real signal and can be conditioned before the first stage of SAR processing. In streaming mode at up to 368MSPS, the DFE can convert the real signal into complex signal using its R2C module at 18-bit precision in and out. Using the programmable filters, the DFE can perform complex FIR filtering, with up to 79 coefficients.

For the SAR algorithm itself, many FFTs and iFFTs are needed as part of the range/azimuth compressions. These functions could be offloaded to the two FFTC accelerators on the 66AK2L06 SoC. In <sup>[8]</sup>, it was reported that the latency for executing the SAR algorithm to process a 4K×4K image on a single DSP core would take 1404 ms of which it is assumed that 50 percent of this latency is due to FFT/iFFT processing. The throughput of the FFTC when processing 4K-points is 525MSPS, which leads to a processing latency of ~8 μs. The azimuth FFT in <sup>[8]</sup> consists of 4096 FFT of size 4K-points taking 18 percent of the total latency (252

ms) when executed on the DSP core with a floating-point code. The same azimuth FFT would take around 16 ms as a projected latency in case the two FFTCs in the 66AK2L06 SoC are used. Considering the effect of the accesses to the external memory, the use of the two FFTCs could lead to at least a 5x improvement in the FFT/iFFT processing latency in this SAR algorithm implementation experiment. This brings the total latency down by 40 percent from 1404 ms to 842 ms. This reduction in latency would free up significant cycle resources to address other algorithmic enhancements and thus improve the performance of the final SAR image reconstruction.

The two other SAR processing approaches, CSA and WE, are also signal processing driven algorithms where a lot of FFT/iFFT operations, filtering, scaling and complex multiplications are needed highlighting that the 66AK2L06 SoC is an excellent platform to handle the deployment and execution of such algorithms.

## 5. Three times faster development

SAR systems and purpose-designed software exploitation tools have been developed for a vast range of military and non-military applications. These include detection, monitoring, mapping and

measuring phenomena on land, sea, ice and in the atmosphere of our planet and other planets.

Modern radar designs are incorporating signal processing functions at the front end (exciter/receiver) of the radar system. This may include waveform generation, filtering, matrix-inverse/transpose operations, FFT/iFFT and signal correlation.

There are also math functions in radar systems, which include exponential complex multiplications, and other algorithmic math operations. Many designers have implemented these functions in C-based processors (in fixed-point and/or floating-point operations). These types of designs can take advantage of the small form factor and quad fixed- and floating-point C66x DSP cores provided in the 66AK2L06 SoC to meet systems requirements while reducing latency and improving the power dissipation of the system.

Based on TI's high-throughput KeyStone II architecture, the new 66AK2L06 SoC is a scalable low-power solution with an integrated DFE and high-speed JESD204B interface, to meet the more stringent system cost and SWaP requirements of the avionics and defense (including radar) applications. This integrated system solution can cut

***This integrated system solution can cut the development time from weeks to days and from days to hours.***

the development time from weeks to days and from days to hours. Developers can take advantage of TI Designs which focus on pre-validating the 66AK2L06 SoC with multiple ADCs, DACs and AFEs. All of this results in faster time

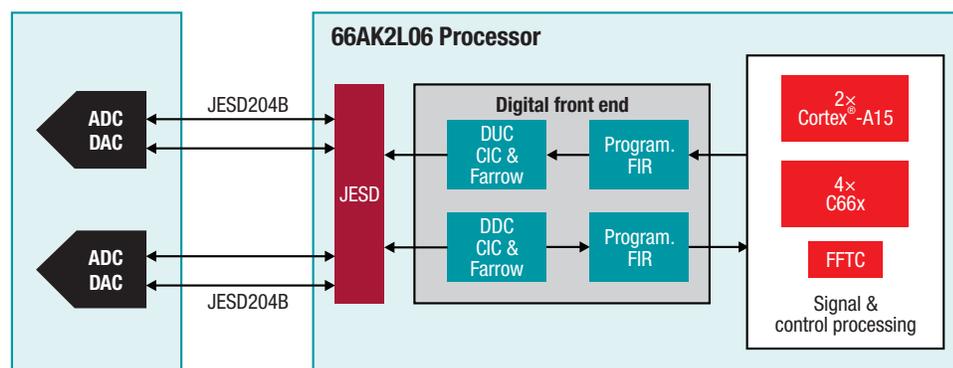


Figure 5: System-optimized alternative FPGAs

to market and developers can develop up to three times faster than other solutions available today. Learn more about 66AK2L06 SoC [here](#).

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