

Reliability advantages of TI flip-chip BGA packaging



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Flip-chip ball grid array (FCBGA) packaging technology is a cost-effective alternative to traditional wire-bond packages and has been available for use in production devices since the late 1990s.

From bottom to top, the package's key components are the BGA, interfacing with the system printed circuit board (PCB); the package substrate, consisting of input/output interconnect routing, power and ground layers; and the die bump interface, which includes bump metal, under-bump metallization and under-fill.

A key advantage of flip-chip packages over wire-bond BGA packages is that the die bumps (effectively, the die/package interface) can be located near the chip sub-system location on the die (digital logic, analog and memory blocks), thus optimizing power and signal integrity. Flip-chip packages avoid the manufacturing complexity and potential quality/reliability risks of high-density, multi-row wire bonding. Texas Instruments (TI) employs the flip-chip class of package technologies to deliver high performance, quality and reliability at a competitive cost.

The mmWave radar sensors use tin-silver (SnAg) (lead [Pb]-free) solder bumps, a mature technology that has been in high-volume production for years in applications, including automotive, telecom such as servers or wireless base stations, industrial automation and consumer electronics. Many years of development led to improved quality and reliability of the SnAg solder-bump (die/package) interface.

The essential features of a die bump interface are the substrate surface (usually a solder mask), substrate pad, bump metal, under-bump metallization on the die, under-fill and the die overcoat to form the stress buffer layer. Optimized die-attach flux and cleanup processes ensure robust connection of the bumped die to the substrate and removal of any residual flux before under-fill dispensing and curing. If present, residual flux may interfere with the wetting of the under-fill to the die and substrate surfaces.

The purpose of under-fill is to form a stress buffer between the die and package, which have a coefficient of thermal expansion mismatch, and to minimize the risk of bump cracks in the presence of thermomechanical stresses resulting from system board assembly/surface-mount technology processes, or later in the field, such as temperature cycling in actual application use.

All of the features I mentioned form a robust, reliable interface layer designed to last at least 100,000 power on hours (POH) with operating temperatures up to 105°C, as well as more limited time frames (20,000 POH) up to 125°C.

Package-to-PCB under-fill

Some customers choose to apply under-fill between the integrated circuit (IC) FCBGA package and their PCB. Applying under-fill improves the robustness and reliability of the BGA solder joint against temperature cycle fatigue, impact resistance, vibration resistance, etc. TI neither requires nor specifically recommends the use of board-level under-fill. This is a decision made solely by designers and/or their contracted manufacturer with respect to the specific needs and goals of the deployed application.

TI performs board-level reliability temperature cycling (T/C) testing, which I'll discuss later, without under-fill between the IC package and the PCB. If you determine that TI board-level reliability test results meet or exceed application needs without package-to-PCB under-fill, you can realize a significant cost savings.

Corrosion and other issues in high-temperature and high-humidity environments

Wire-bond technologies can suffer from corrosion-related risks, particularly in the presence of halogens such as chlorine (Cl), leading to premature failure of either die ball bonds or stitch bonds. In contrast, corrosion mechanisms are rarely a problem in FCBGA packages. While copper (Cu) interconnect metallization can extrude along a dielectric crack in the package substrate in the presence of high temperature, humidity and bias, this extrusion can occur on any laminate substrate common to most BGA technologies, not just FCBGA. These defects, though rare, are detectable under qualification testing such as temperature humidity and bias (THB), biased highly accelerated stress test (BHAST) or unbiased HAST (UHAST), and thus can be addressed with corrective and preventive actions before production begins.

Another issue on high-Sn leaded devices is "Sn whiskers," crystalline structures that form and expand due to diffusion. It can happen to package leads plated with matte Sn. Although the solder die bumps on FCBGA packages, particularly Pb-free/SnAg, are high in Sn content, they generally do not have problems with Sn whiskers, which is a key advantage.

Component-level reliability (qualification) testing

TI performs a rigorous suite of component-level reliability tests as part of the production qualification process before releasing a product to production. TI also executes the same test environments later as ongoing reliability monitors of process robustness and stability.

Component level in this context means that the device under test (DUT) is not soldered to a test board but is either inserted into a test socket or unenclosed (free-standing) in the test chamber, depending on the test. Component-level testing is synonymous with first-level reliability testing. TI also performs board-level testing, also known as second-level reliability testing.

If products are dual or multipurpose, with automotive, industrial or broad market applications, TI generally applies the more strenuous sampling and test conditions between the Automotive Electronics Council (AEC)-Q100 standard or prevailing American National Standards Institute (ANSI)/Institute for Printed Circuits (IPC)/Joint Electron Device Engineering Council (JEDEC) standards.

The component-level reliability tests that evaluate the influence of package design, materials and manufacturing are:

- High-temperature operation life (HTOL) testing, which evaluates thermomechanical stress influence on the die (such as inducement and growth of cracks, typically in the dielectrics), as well as ionic species introduced during the packaging manufacturing process that may influence circuit performance if diffused into the die.
- High-temperature bake/storage life (HTSL) testing, which evaluates diffusion-related mechanisms, including void formation. In TI's experience, this test very rarely results in failures on solder-bump FCBGA packages.
- T/C, which is the thermal cycling of DUTs from cold to hot temperatures (in the case of TI FCBGA packages, usually -40°C to 125°C) to test for thermomechanical-stress-induced failure mechanisms such as cracks, extrusions or interfacial delamination (such as under-fill from die or package substrate).
- Biased HAST or THB testing, which evaluates concurrently elevated temperature and percent of relative humidity (%RH) in the presence of static electrical bias. TI uses either "85/85" (85°C, 85%RH, Vddmax bias) or 110°C BHAST (also 85%RH, Vddmax bias). This test is important for the detection of corrosion and filament/extrusion (normally metallic) failure mechanisms.
- UHAST testing, which is normally performed at 110°C / 1.2 Atmosphere (ATM) for FCBGA packages. Like THB and BHAST, UHAST typically accelerates corrosion and metallic filament/extrusion mechanisms. Since it is unbiased, there is no power dissipation (Joule heat generation) impacting a change in moisture concentration

beyond the ambient condition. Unlike THB/BHAST, it is an un-socketed test with no boards and is thus less logistically complex to execute.

- Charged device model (CDM) electrostatic discharge (ESD) testing. The choice of packaging dimensions and materials affects the capacitance of the package, which in turn affects the charge buildup and discharge current during this type of testing. Other factors being equal, larger packages should have higher peak currents and lower voltage ratings than smaller packages.

Board-level reliability (qualification) testing

TI performs board-level reliability T/C testing as part of product qualification for FCBGA packages on special daisy-chain vehicles, with die and substrates designed for equipment that monitors resistance on daisy-chain "nets." These nets are metal lines and vias that traverse through the package substrate, through the die bumps, into the die, and back through the bumps to the substrate and BGAs. Daisy-chain devices use the same package outline and bump/package manufacturing flow as functional devices, with a die that is approximately the same dimensions.

Daisy-chained die/packages are intended to represent functional die/packages in terms of bump and package material, bump design rules, assembly materials and manufacturing processes, and BGA layout. The boards are standardized to fit the test chamber and are typically 62mil to 93mil thick, with six to eight metal layers and FR4 material. Variations in all of these parameters may occur depending on the end application, such as Rogers material for radio-frequency applications.

In some rare special-purpose cases, TI performs other board-level reliability tests, such as impact, shock and vibration. These are not standard tests for catalog device product qualification and are only performed at TI's discretion. In some cases, you may wish to perform your own board-level environmental reliability testing (power cycling, T/C, vibration, shock), which should always be the best gauge of performance for your application.

Once TI completes its board-level reliability testing, it constructs a “Weibull plot.” This is a lifetime reliability model associated with the failure of the weakest link in a system; in this case, a BGA. The two-parameter Weibull plot, technically of the cumulative distribution function (CDF), also known as unreliability, predicts what fraction of the population will fail based on time duration, cycles, drops, etc. (the independent variable). **Equation 1** gives the CDF (total fraction failed), shown as a function of time:

$$F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^\beta}$$

where the two parameters are η (scale or characteristic life) and β (slope).

Figure 1 demonstrates an example Weibull model with an arbitrary data set. The acceleration factor ([AF], stress to application) in this particular instance is based on the Norris-Landzberg equation, which is itself based on maximum temperature, cycling frequency and minimum/maximum temperature range. The details of the Norris-Landzberg equation are beyond the scope of this paper. Nevertheless, TI can provide assistance as needed to those who wish to model TI board-level reliability results to application conditions.

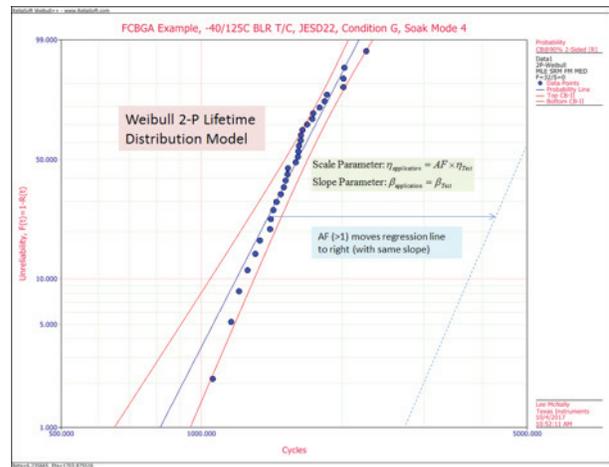


Figure 1. An example Weibull model/plot of board-level reliability T/C data demonstrating the effect of AF.

Conclusion

Solder-bump FCBGA is a cost-effective and reliable package technology, enabling high-performance processing that traditional wire-bond technologies are unlikely to achieve. As of 2017, flip-chip design, material selection, manufacturing and quality/reliability have all benefited from decades of development, production experience and process optimization, both on the die bump and package. Flip chip is an excellent choice for reliability and may be a good fit for use in a wide array of application environments, including automotive and industrial, when hermetically sealed packaging is not required.

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