Sitara™ AM6x processors for protection relays

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The worldwide electric power infrastructure is an interconnection of power generation, transmission and distribution systems commonly known as the power grid.

In order to improve the overall reliability, utilization and efficiency; communication and additional sensors are being added making the power grid smarter referred commonly as smart grid.

A substation is a key component of the smart grid infrastructure, located along power transmission and distribution including low-voltage feeders serving residences and businesses. Substations transform voltage levels for transmission and perform important functions such as feeder switching, protection of load switches and breakers and continuous monitoring of assets to increase utilization, efficiency and reduce downtime.

One of the key end equipment used in grid is the multifunction protection relay. A multifunction protection relay implements protect and control functionalities and can be configured to protect generators, transmission lines, motors, BUSBAR, or other grid equipment's.

Multifunction Protection relays are used in the smart grid to:

- Detect abnormal power system behavior of the grid, provide alerts and take required actions.
- Sample the analog inputs and Compute electrical parameters of the equipment they are connected to and take actions based on the functionality configured, including providing trip signal to the circuit breakers for protection.
- Improve efficiency and reliability of power systems including power generation, transmission, and distribution.
- Send status updates to centralized monitoring system through a redundant communication infrastructure such as High-Availability Seamless Redundancy (HSR)/Parallel Redundancy Protocol (PRP) as per international Electrotechnical Commission (IEC) 61850 and IEC 62439 standards requirement.

The protection relay consists of ac analog module. Multiple voltage and current inputs are connected to the analog input module, scales the inputs to the ADC range and converts the analog inputs to digital values using high precision ADCs. The processor module acquires sampled digital values from the analog input module and process the sample data including digital filtering, computing electrical parameters, implementing protection algorithms and communicating the parameters to central network.

This white paper focuses on the processor module in a protection relay.

The processor module in protection relays typically performs functions of acquiring samples, processing and communication the data as shown in **Figure 1** and additionally provides capability for HMI and diagnostics.

The processor module acquires digital data from the analog-to-digital converter (ADC) using serial/parallel interface and presents the data for signal processing which performs digital filtering for smoothening the input signal and remove abnormalities.

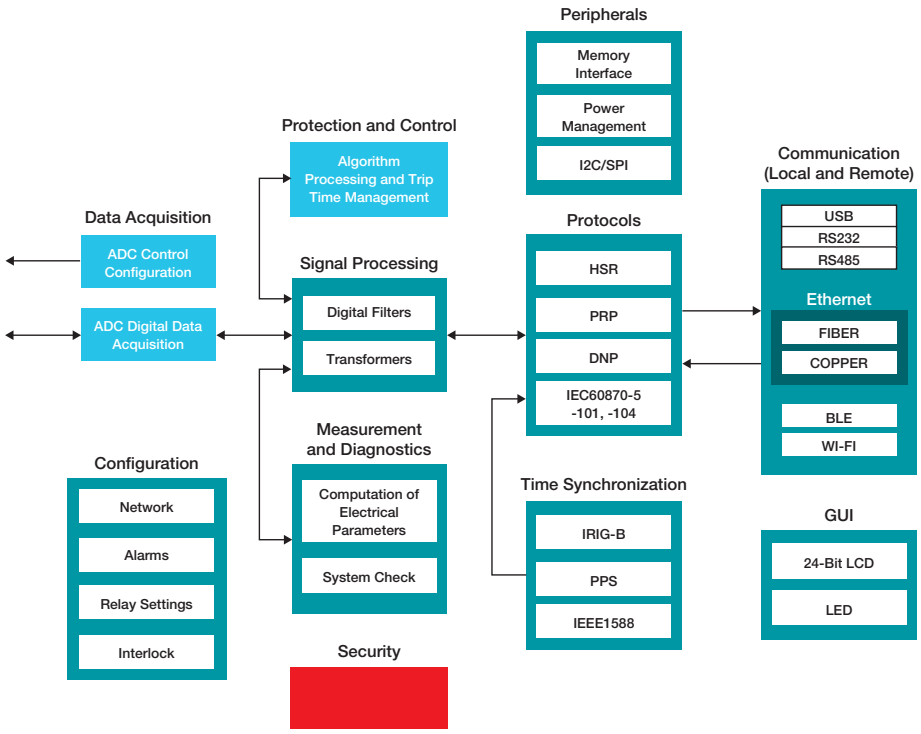

***Figure 1**. Typical data flow within the processor module in a protection relay.*

The filtered data is then moved for processing protection algorithm, which involves processing of application-specific algorithms to determine whether monitored parameters are in range, and to analyze data for end-equipment-specific protection requirements like overload, differential, reverse power and provide trip signal to circuit breakers with predefined timing following standard trip curves. The filtered data is also used to compute electrical parameters used for measurement and diagnostics. A communication unit implements different communication interfaces and the required protocols including redundant protocols like HSR/PRP, reports events and status to higher layers like SCADA supervisory control and data-acquisition systems. A graphic LCD presents the status of the parameters and the equipment being protected in a graphical form for quick analysis.

Challenges addressed by processor module in protection relays

As the traditional grid gives way to smart grid and as the deployments of smart grid increase, the processor module has these challenges to address:

- Interfacing with multiple external ADCs with different interfaces and protocols.
- Processing of acquired ADC data to achieve highest AC performance.
- Performing advanced digital signal processing (DSP), transforms and data-management functions using multi-core subsystems.
- Supporting redundant industrial Ethernet protocols such as HSR/PRP.
- Presenting intuitive and rich human machine interface (HMI).
- Supporting high reliability, long power-on hours (POH) and full error-correction code (ECC).
- Supporting advanced security functions and functional safety.
- Extensive peripheral set to connect with multiple serial and parallel interfaces.

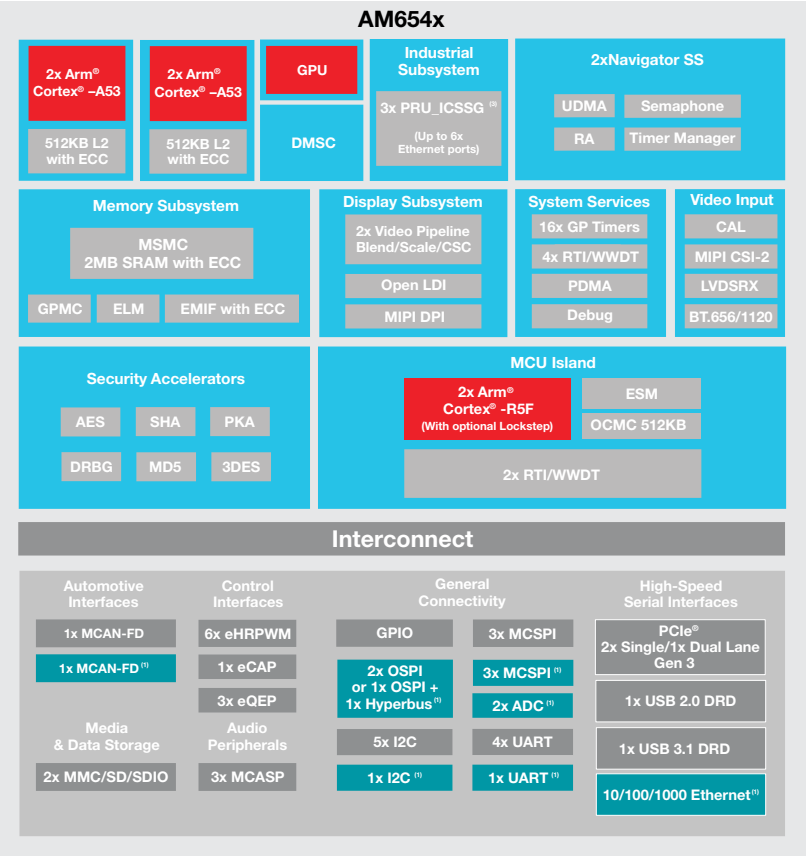

Figure 2. *AM654x processor block diagram.*

Sitara AM6x devices for multifunction protection relay processor module application

The processor module may require multiple processing subsystems to meet different processing needs and challenges. Combining functions into fewer or a single device can reduce system cost and complexity.

Texas Instruments (TI) Sitara™ AM6x processors are single-chip solutions designed to suit well in the processor modules in protection relays. **Figure 2** is the block diagram of AM654x processor, a device in the family of the AM6x processor.

Let's match the challenges listed above to features of the AM6x processor.

Acquiring high-speed and high-performance data from an external ADC with different interfaces and protocols. One of the key challenge for a processor module is the ability to connect to multiple external ADCs simultaneously, with different interface options including Serial Peripheral Interface (SPI) and changing timing requirements based on the input frequency for implementing coherent sampling. To further complicate the situation, many ADC manufacturers have created ADC interface that requires custom timings to acquire data from the processor.

The TI AM6x processor solves the challenge of interfacing multiple ADC with programmable real-time unit subsystem and industrial communication subsystem (PRU-ICSS) peripheral, which can attach

to external ADCs directly and save bill-of-materials (BOM) cost. The PRU-ICSS improves signal-chain performance and adjusts the time base for the ADC interface to achieve coherent sampling, thereby reducing spectral leakages.

Performing multicore processing for advanced DSP and data-management functions. To meet the high-performance processing requirements including advanced signal processing and management functions, the AM6x device family combines up to four Arm® Cortex®-A53 cores with NEON extension, and a dual Arm Cortex-R5F microcontroller (MCU) subsystem. The Cortex-A53 cores are arranged in dual-core clusters with shared L2 memory to create two high-performance processing channels. The Cortex-R5F cores with integrated tightly coupled memories (TCM) can be used for ADC sample data filtering and DSP functions, whereas the Cortex-A53 cores provide ample performance for protection-relay management and Ethernet communication functions.

Supporting Ethernet protocols including redundant industrial protocols such as HSR/PRP. The need for high reliability and predictability in Ethernet networks for substation automation is the motivation for the IEC 62439 standard, with the goal to create a low-cost, easy-to-maintain and interoperable communication network infrastructure with built-in redundancy. IEC 62439-3 Clauses 4 and 5 define High-availability Seamless Redundancy (HSR) and Parallel Redundant Protocol (PRP).

The AM6x processor leverages PRU-ICSS technology to support HSR/PRP. The implementation consists of PRU-ICSS firmware, drivers (Linux®/real-time operating system [RTOS]), application and Simple Network Management Protocol support. PRU-ICSS firmware handles link redundancy, whereas the host (Cortex-A53) runs drivers and application code.

Additional asynchronous or synchronous communication interfaces can be implemented using UART/SPI ports or the PRU-ICSS can be used to add additional universal asynchronous receiver transmitter ports or SPI ports. The PRU-ICSS cores can also be used for custom general-purpose input/output manipulations and deep packet inspections.

Presenting an intuitive and rich HMI. Multifunction protection relays are integrated with Graphical LCD with intuitive HMI for displaying waveforms, trends, electrical parameters, configuration and status. A rich HMI helps reduce training costs, simplifies analysis and also minimizes chances of misconfiguration. The AM6x processor has an integrated LCD controller as well as a 3D graphic accelerator to enable the creation of rich HMI features.

Increased reliability and diagnostics by supporting high reliability, long POH and full ECC. Protection relays require high reliability and extended lifetimes and are often operate in extreme environments. AM6x processors are built to meet these requirements. The extensive ECC coverage on memories and the design strategy to limit failures in time in logic drive some of the lowest total soft error rates available for a complex system on chip.

The AM6x processor has an industrial temperature rating with junction temperatures (Tj) ranging from -40°C to 105°C. At a maximum Tj of 105°C, the AM6x processor has an estimated operational lifetime of 100,000 POH, with all Cortex-A53 cores operating at 1.0 GHz and the rest of the device operating at maximum frequencies.

Another common requirement for industrial applications is to operational device lifetimes of greater than 100,000 POH. For applications that can cope with a lower Tj of 95°C, the AM6x processor offers an estimated lifetime up to 200,000 POH.

The AM6x processor includes extensive hardware diagnostics that operate continuously. Some examples include the lockstep Cortex-R5F architecture, memory management units, firewalls, single- and double-error detection and parity for memories and interconnect, power-supply diagnostics, temperature sensors, and reset diagnostics. The AM6x safety manual details the diagnostic features.

Supporting advanced security functions and functional safety. Functional safety is a new emerging requirement in protection relays, as it is often the last line of defense to protect the grid infrastructure. Functional safety gives system designers more confidence in the ability of systems to diagnose component failures quickly and act to prevent damage. TI designed functional safety enablers and full ECC requirements into the AM6x processor.

AM6x processors can be used in industrial control applications with target levels as high as IEC 61508 safety integrity level (SIL) 3. TI provides a SafeTI™ design package to assist in meeting functional safety requirements for systems that integrate AM6x processors while managing both systematic and random failures. As standards require, TI follows independently certified hardware and software development processes with requirements tracking, documentation and validation.

A TI-provided software compliance package and compiler qualification kit manage systematic failures. For random failures, TI provides a configurable AM6x failure modes effects and diagnostics analysis tool to detail failure modes and metrics from the device design and diagnostic coverage. The SafeTI package also provides a safety analysis report, which is the certification summary from a third-party assessment of the AM6x processor as a safety element out of context.

Concerns about grid infrastructure attacks are at an all-time high. Security threats are always present and, with the rapid proliferation of the Internet of Things in the smart grid, those threats can come from anywhere, even inconspicuous and low-cost end-node devices. The question is not whether a system will be attacked but when. Security is just as much about risk management as it is about protection. Given that the protection relay may come under attack, it is imperative that system designers prioritize security.

Software and hardware security features must work together for a more secure layer of protection than either solution working independently. Of course, the strength of a security architecture will depend on its foundation. Four aspects of the foundational layer are essential: a secure boot process, debugging security, hardware-based device keys/ID and cryptographic acceleration.

AM6x processors enable security features like secure boot, debugging security, keys/ID, cryptographic acceleration, trust execution environment (TEE), secure storage, network security, software intellectual property (IP) protection, initial secure programming, secure firmware and software.

Processing module BOM

A reduced BOM is always a priority for a processor module. One way to reduce BOM costs is to use fewer devices, which helps save components and associated printed circuit board (PCB) costs. Fewer components means simpler designs and less PCB routing issues.

The AM6x processor integrates the PRU-ICSS, which can eliminate the need for field-programmable gate arrays (FPGAs) to connect to external ADCs.

The same PRU-ICSS peripheral can be used to implement redundant protocols like HSR/PRP.

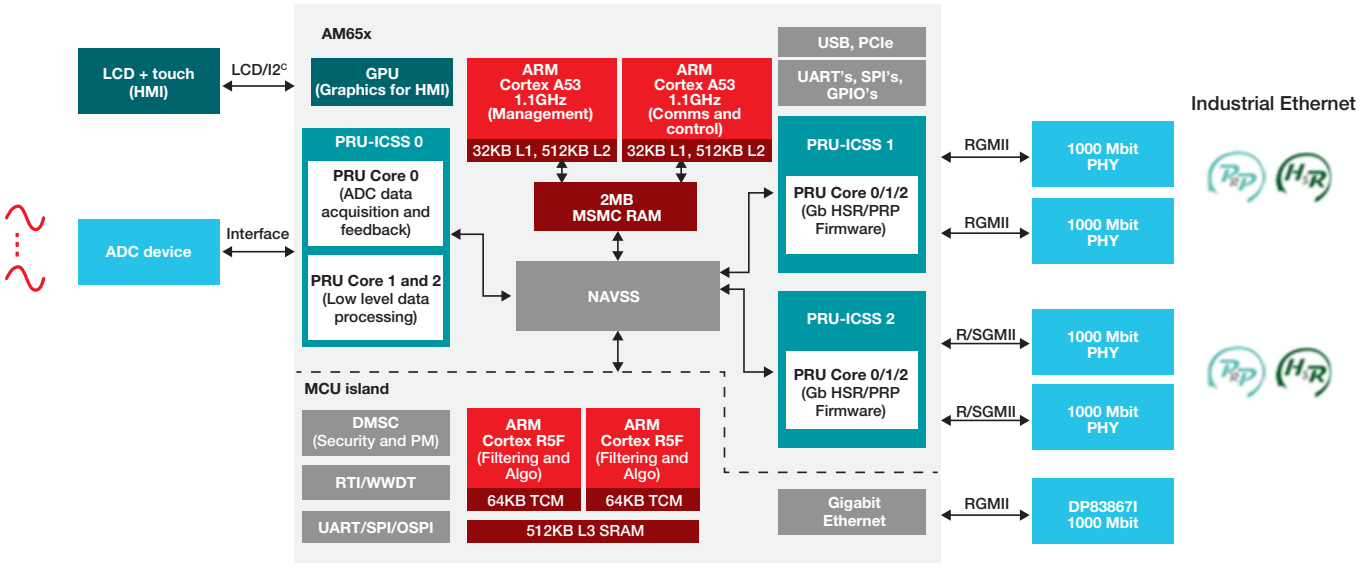

***Figure 3**. System block diagram for AM6x processor-based protection relays.*

With an integrated LCD controller and 3D graphics accelerator, coupled with a high-performance multicore architecture, AM6x processors are a good fit for a processor module.

Processor module example using the AM6x

Figure 3 is an example of a multifunction protection relay based on the AM6x processor. External ADCs attach directly to the PRU-ICSS using an interface signal that can mimic SPI or multi-SPI. The PRU-ICSS carries out ADC configuration and data acquisition under PRU-ICSS firmware control; this firmware is customizable based on the external ADC selected.

AM6x processors include three instances of the PRU-ICSS subsystem. With one used for ADC interface, that leaves two PRU-ICSS subsystems for HSR/PRP processing. Each PRU-ICSS support two Ethernet ports, hence total of four Ethernet ports.

The AM6x PRU-ICSS's three RISC cores, running at 250 MHz, enable the application of low-level processing like zero-cross detection and finite impulse response filtering. Filtered data is transferred via extensive inter-process communication using hardware direct memory access engines to the Cortex-R5F subsystem memory.

AM6x processors include dual Arm Cortex-R5F MCUs running at 400 MHz that can carry out real-time functions such as filtering, normalization and processing end-equipment-specific algorithms. Each Cortex-R5F core has a 64 KB TCM for fast access to data. End-equipment-specific actions and processing can occur in this subsystem because the Cortex-R5F is a real-time processing core with deterministic capabilities.

AM6x processors also have quad Arm Cortex-A53 processor cores that can perform general application management and run communication protocol stacks. Each core can run at a maximum speed of 1.1 GHz, thereby giving ample computational power for complex stacks and management protocols.

Conclusion

The AM6x processor provides a single-chip solution for processor module in multifunction protection relay with the ability to directly interface to external ADCs, implement multiple communication interfaces and protocols. The ability to offer customizable interfaces and protocols using the PRU-ICSS can eliminate the need for an FPGA to handle interfacing with ADC.

AM6x processors have the potential to support gigabit HSR/PRP by using the PRU-ICSS. The AM6x processor has three instances of PRU-ICSS that can be used for ADC attach or two-port HSR/PRP per instance.

The AM6x processor's integrated LCD controller and 3D graphics accelerator fit the current trend in protection relays toward richer HMI features to provide on-device status and configuration, along with on-device training videos for operators. The AM6x processor provides ample connectivity options including multiple UART, SPI, I^2C, McASP, USB and Peripheral Component Interconnect Express (PCIe) to enable the direct attachment of peripherals without external extender devices.

The AM6x processors reliability and functional safety features include full ECC across all memories in the device, with extensive hardware diagnostics included in the on-chip memory, peripherals and interconnect. The processor as a whole includes features intended to help design systems that can achieve levels up to SIL 3 of IEC 61508.

AM6x processors enable security features like secure boot, debugging security, keys/ID, cryptographic acceleration, TEE, secure storage, network security, software IP protection, initial secure programming, secure firmware and software to defend protection relays from malicious attacks.

Additional resources

- TI provides reference designs for common ADCs like the ADS8688, including Flexible Interface (PRU-ICSS) Reference Design for Simultaneous, Coherent DAQ Using Multiple ADCs.
- Read the application report, "HSR/PRP Solutions on Sitara Processors for Grid Substation Communication."
- Watch the PRU-ICSS Training Series.

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