

AWR1642 mmWave sensor: 76–81-GHz radar-on-chip for short-range radar applications



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Introduction

The use of radar technology has grown tremendously in recent years. In the automotive context, the primary radar applications can be broadly grouped into corner radars and front radars. Corner radars (rear and front) are typically short-range radar sensors that handle the requirements of blind-spot detection (BSD), lane-change assist (LCA) and front/rear cross-traffic alert (F/RCTA), while front radars are typically mid- and long-range radars responsible for autonomous emergency braking (AEB) and adaptive cruise control (ACC).

Traditionally, corner radars were based on 24-GHz technology. However, there is a shift in the industry toward the 77-GHz frequency band due to emerging regulatory requirements, as well as the larger bandwidth availability, smaller sensor size and performance advantages.

This white paper introduces the [AWR1642](#) device as a highly integrated 76–81-GHz radar-on-chip solution for short-range radars. The device comprises the entire millimeter wave (mmWave) radio-frequency (RF) and analog baseband signal chain for two transmitters (TX) and four receivers (RX), as well as two customer-programmable processor cores in the form of a C674x digital signal processor (DSP) and an ARM[®] Cortex[®]-R4F microcontroller (MCU). In the next few sections, we will present the high-level architecture and features of the AWR1642 device and show sample illustrations of chip configurations for typical use cases.

AWR1642 high-level architecture

The AWR1642 device is a highly integrated single-chip 77-GHz radar-on-chip device that includes two transmit and four receive chains, a 600-MHz user-programmable C674x DSP and a 200-MHz user-programmable ARM Cortex-R4F processor. The device supports wide RF bandwidth, covering both the 76–77-GHz and 77–81-GHz bands. As **Figure 1** on the following page shows, the device comprises four main subsystems: the RF/analog subsystem, the radio processor subsystem, the DSP subsystem and the master subsystem.

The RF/analog subsystem includes the RF and analog circuitry: the synthesizer, power amplifiers (PAs), low-noise amplifiers (LNAs), mixers, intermediate frequency (IF) chains and analog-to-digital converters (ADCs). This subsystem also includes crystal oscillators, temperature sensors, voltage monitors and a general-purpose ADC.

The AWR1642 device uses a complex baseband architecture and provides in-phase (I-channel) and quadrature (Q-channel) outputs. A separate white paper titled “[Using a complex-baseband architecture in FMCW radar systems](#)” describes the advantages of a complex-baseband architecture.

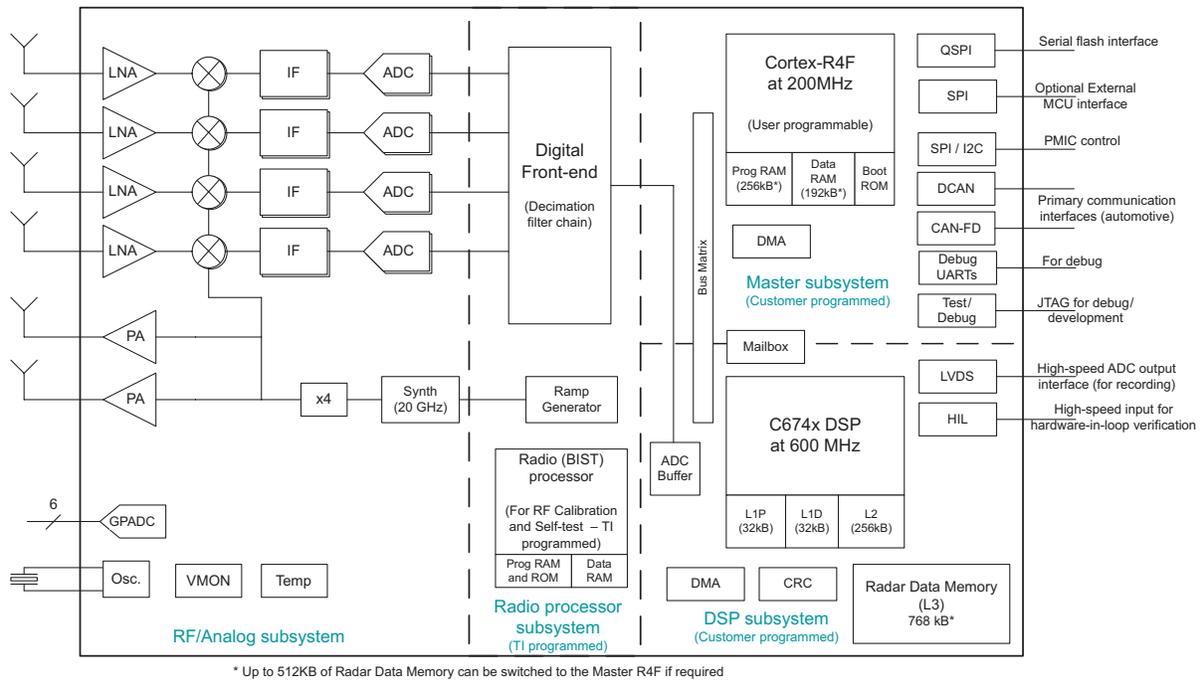


Figure 1. AWR1642 high-level architecture.

The radio processor subsystem (also known as the built-in self-test [BIST] subsystem) includes the digital front-end, the ramp generator and an internal processor for controlling and configuring low-level RF/analog and ramp generator registers based on well-defined application programming interface (API) messages from the master or DSP subsystem. (Note: this radio processor is TI-programmed and takes care of RF calibration needs and BIST/monitoring functions; the processor is not available directly for customer use.) The digital front end takes care of filtering and decimating the raw sigma-delta ADC output and provides the final ADC data samples at a programmable sampling rate.

The DSP subsystem includes a TI C674x DSP clocked at 600 MHz for radar signal processing—typically the processing of raw ADC data until object detection. This DSP is customer-programmable, and enables full flexibility when using proprietary algorithms.

The master subsystem includes ARM’s automotive-grade Cortex-R4F processor clocked at 200 MHz,

which is customer-programmable. This processor controls the overall operation of the device, handles the communication interfaces, and typically implements higher-layer algorithms such as object classification and tracking. This processor can run Automotive Open System Architecture (AUTOSAR) if required.

The AWR1642 mmWave sensor can function as an autonomous radar-on-chip sensor for short-range radar (SRF) applications. The device includes a Quad Serial Peripheral Interface (QSPI), which can download customer code directly from a serial Flash. A Controller Area Network-Flexible Data Rate (CAN-FD) interface and an additional (classic) CAN interface are included so that the sensor can communicate directly with the vehicle CAN bus or with other sensors on a private CAN bus. An SPI/Inter-Integrated Circuit (I²C) interface is available for power-management integrated circuit (PMIC) control when using the AWR1642 device as an autonomous sensor.

Memory partition

The total memory available on the AWR1642 mmWave sensor is 1.5 MB. This is partitioned between the R4F program RAM, R4F data RAM, DSP L1 and L2 memory and radar data memory (L3 memory). **Table 1** lists some example memory configurations.

- The L2 memory in the DSP subsystem is 256 KB and typically used for instruction and immediate data for the DSP application.
 - The DSP subsystem also includes 32 KB each of L1 program and data RAMs, which are configurable as cache, either in full or partially.
- The R4F has dedicated memory of 448 KB, which is partitioned between the R4F's tightly coupled memory interfaces—viz., TCMA (256 KB) and TCMB (192 KB).
 - Although the complete 448-KB memory is unified and useable for instruction or data, typical applications use TCMA as instruction memory and TCMB as data memory.
- The remaining 768 KB is L3 memory, which is available as radar data cube memory. It is also possible to share up to 512 KB of L3 memory for the R4F in 128-KB increments.

Option	R4F RAM	DSP L2 RAM	Radar data memory
1	448 KB	256 KB	768 KB
2	576 KB	256 KB	640 KB
3	704 KB	256 KB	512 KB

Table 1. Example memory configurations.

The DSP advantage

One of the key advantages of the AWR1642 device is its built-in C674x DSP. Frequency-modulated continuous-wave (FMCW) radar technology has evolved significantly in the past several years and continues to do so. Automotive manufacturers are adding more applications as radar plays a larger

role in modern vehicles, both for driver comfort and safety. These emerging applications also make radar performance requirements tighter in terms of spatial resolution, velocity resolution and object detection and classification.

The availability of a fully programmable DSP in the AWR1642 device enables you to implement proprietary algorithms and build innovative solutions to address difficult challenges with respect to radar performance. Research advancements continue around algorithms to improve performance in several critical areas, such as:

- **Interference mitigation:** As more vehicles deploy radar technology, the problem of interference between radars becomes important. In this context, an active area of research and signal-processing algorithm development is in innovative algorithms for detecting and mitigating interference.
- **Improved detection algorithms:** Due to new emerging applications for radar, including the ultimate vision of fully automated driving, there is a need for improved algorithms related to object detection, ground clutter removal and minimizing false detections to ensure robustness.
- **High-resolution angle estimation:** One of the key challenges associated with radar sensors is the limited angular resolution natively available. Several advanced angle-estimation algorithms beyond traditional beamforming are possible to improve angular resolution, including Multiple Signal Classification (MUSIC) and Estimation of Signal Parameters via Rotational Invariance Technique (ESPIRIT).
- **Clustering and object-classification algorithms:** This is another active area of research and algorithm development, especially in the context of object classification using

a high-resolution radar-point cloud and the identification of pedestrians using techniques such as micro-Doppler.

For these needs, the built-in DSP enables high performance and fully programmable signal-processing capability. **Table 2** provides some benchmark data for the performance of the DSP in a few typical radar signal-processing routines.

Option	Operation	Clock cycles (C674x DSP)	Execution time (at 600 MHz)
1	128-pt fast Fourier transform (FFT) (16-bit)	516	0.86 μ s
2	256-pt FFT (16-bit)	932	1.55 μ s
3	512-pt FFT (16-bit)	2,168	3.61 μ s
4	Windowing (length N vector)	$0.595N + 70$	0.37 μ s (for N = 256)
5	Log magnitude (16-bit)	$1.8N + 75$	0.893 μ s (for N = 256)
6	Constant false-alarm rate-cell averaging (CFAR-CA) (for N cells)	$3N + 161$	1.55 μ s (for N = 256)

Table 2. Benchmark data for common radar signal-processing routines.

Security

AWR1642 mmWave sensor provides a secure boot mechanism. Secure boot, a type of security enabler, provides the mechanism to help keep the code/ algorithms in an encrypted form and help protect it from unauthorized access. Also, it helps avoid the implantation of rogue code on to a device, thus protecting the device from running an altered code/functionality.

To speed up the coding and decoding process which is computation intensive, the AWR1642 mmWave sensor is equipped with hardware-based accelerator security features which can also be used by the application code for additional security implementation:

- Advanced Encryption Standard (AES).
- Secure Hash Accelerator (SHA2).

- True Random Number Generator (TRNG).
- Public Key Accelerator (PKA).

Further, the AWR1642 sensor provides a secure debugging mechanism, making debugging hassle-free while helping protect the device from various threats.

Safety

The AWR1642 sensor is part of TI's SafeTI™ design package to assist developers to achieve International Organization for Standardization (ISO) 26262 Automotive Safety Integrity Level (ASIL) B in their applications.

The AWR1642 sensor follows a concept called Safe Island, which involves a balance between the application of hardware diagnostics and software diagnostics to help manage functional safety. A core set of elements are tested thoroughly at power up and monitored closely to help provide correct software execution. This core set of elements includes the power supply, clocks, resets, and the R4F processor, interconnect and associated program and data memory to assist with the execution of software, enabling software-based diagnostics on other device elements such as peripherals.

The device includes advanced built-in circuits for on-chip monitoring of the RF and analog front-end, both online during functional chirp periods and offline during inter-chirp and inter-frame idle periods. The dedicated radio processor (delayed lock step) core running TI's firmware helps ease application development and completely offloads the DSP and MCU processor million instructions per second (MIPS) from any kind of radar front-end monitoring. The AWR1642 sensor supports these front-end diagnostic features:

- Synthesizer chirp-frequency monitor.
- TX output-power monitor.

- RF loopback-based noise figure, gain imbalance and phase-imbalance monitor.
- RX saturation monitor.
- IF loopback-based IF amplifier (IFA) filter-attenuation monitor.
- Ball-break monitor.
- Temperature sensors.

Other key diagnostic features include logic BIST for central processing unit (CPU) cores, memory BIST for all memories, windowed watchdogs for each processor, end-to-end error-correcting codes, memory protection units, clock and supply monitors, glitch filtering on resets, and an error-signaling module. These features help enable developers more easily and quickly achieve ASIL-B functional safety for their end applications and designs.

Safety-critical development requires the management of both systematic and random faults. TI has created a unique development process for safety-critical semiconductors, tailoring the functional safety life cycles of ISO 26262:2011 to best match the needs of a safety element out of context (SEooC). This development process has been certified by an independent third-party auditor TÜV SÜD.

AWR1642 use case

The AWR1642 is a radar-on-chip for short-range radar applications in the automotive market. Let's take a multimode usage example with a range of 80 m for short-range radar (SRR) and a range of 20 m for ultra-short-range radar (USRR); see

Table 3.

The example in **Table 3** uses 512 KB of radar data cube memory and achieves an 80-m range with eight virtual antennas (two TX, four RX). Other variations are possible to achieve different system-performance metrics.

Multimode usage example

	Short-range radar (SRR)	Ultra-short-range radar (USRR)
Maximum unambiguous range	80 m	20 m
Sweep bandwidth	425 MHz	1,725 MHz
Range resolution	35 cm ← Normal resolution	8.7 cm ← Higher resolution
Ramp slope	8.3 MHz/μs	33.75 MHz/μs
Chirp duration	51 μs valid (+7.5 μs inter-chirp)	51.1 μs valid (+7.4 μs inter-chirp)
Number of chirps	128 (TX1 + TX2, TX1 – TX2 alternating)	128
Maximum unambiguous relative velocity	±30 kph*	±30 kph
Maximum beat frequency	4.5 MHz	4.5 MHz
ADC sampling rate (I, Q)	5 MSPS (complex)	5 MSPS (complex)
Frame time	128 × 58.5 μs = 7.5 ms	128 × 58.5 μs = 7.5 ms
Range FFT size	256 (complex)	256 (complex)
Radar data memory	256 × 128 × 4 RX × 4 Bytes = 512 KB	256 × 128 × 4 RX × 4 Bytes = 512 KB

*The actual maximum velocity can be higher using velocity ambiguity-resolution techniques.

Table 3. Example chirp configuration for a multimode SRR example.

Figure 2 on the following page depicts radar images with the 80-m chirp configuration for a simulated case of two-point objects at 25 m and 40 m, respectively. The left side of **Figure 2** depicts the range and relative speed of the objects, while the right side shows range and angle.

Compared to 24 GHz, the use of 76–81 GHz for these applications enables high-range resolution (up to 4 cm range resolution is possible) and higher-velocity resolution (which is important for parking-assist applications), and also results in a smaller form factor for the antennas, which is a significant advantage.

The R4F processor has 704 KB of available memory for higher-layer algorithms, such as clustering and tracking, as well as control and host interface functions (including AUTOSAR, which is typically required for stand-alone sensor implementations).

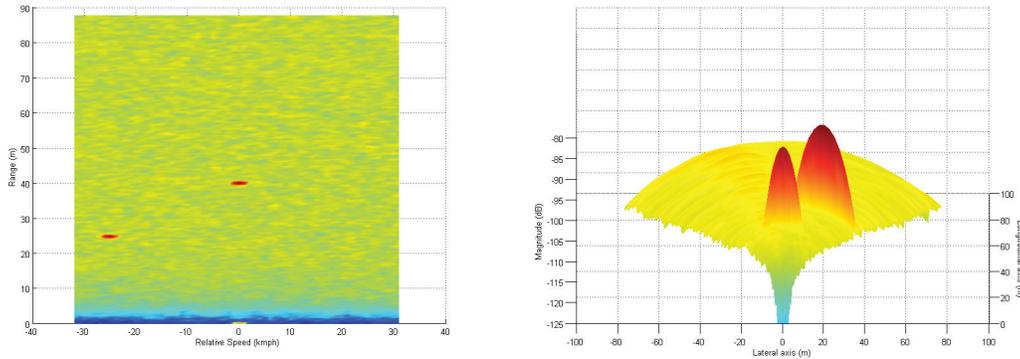


Figure 2. Radar 2-D FFT images for a simulated case of two-point objects.

Developers can also consider implementing higher-layer algorithms like clustering and tracking in the DSP.

Figure 3 illustrates the use of the AWR1642 device as a satellite sensor mounted at four corners of a vehicle, feeding raw-detected objects to a radar fusion box. In this topology, the four corner radars perform 1-D, 2-D FFT, detection and angle-estimation processing, and send raw detected objects over the CAN-FD interface to the central radar fusion box. The availability of the second CAN interface also enables the sensor to simultaneously communicate with the other sensors over a private CAN bus.

Summary

Developers now have the ability to design with a sensor that offers them a high level of integration and precision that enhances short-range automotive radar applications. The benefits of the [AWR1642](#) mmWave sensor are endless.

- For improved performance, the AWR1642 sensor offers wider RF bandwidth of 76–81 GHz, highly linear chirps, faster ramps up to 100 MHz/μs and on-chip BIST functionality
- For ease-of-use and safety monitoring, the AWR1642 sensor includes on-chip BIST processor functionality
- With DSP integration, the AWR1642 sensor enables innovative algorithms to handle emerging challenges with interference and robust detection of objects

AWR1642 sensor provides the relevant features and supporting infrastructure which can help customers to achieve their system goals both from cost and performance perspective.

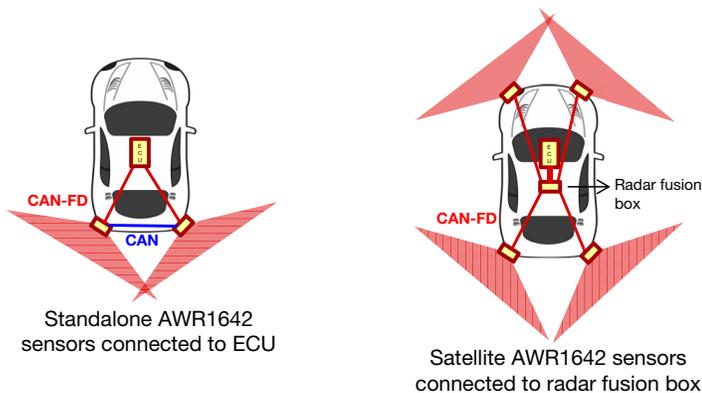


Figure 3. Corner radar system topologies using AWR1642 mmWave sensor

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