FAB NOTES :

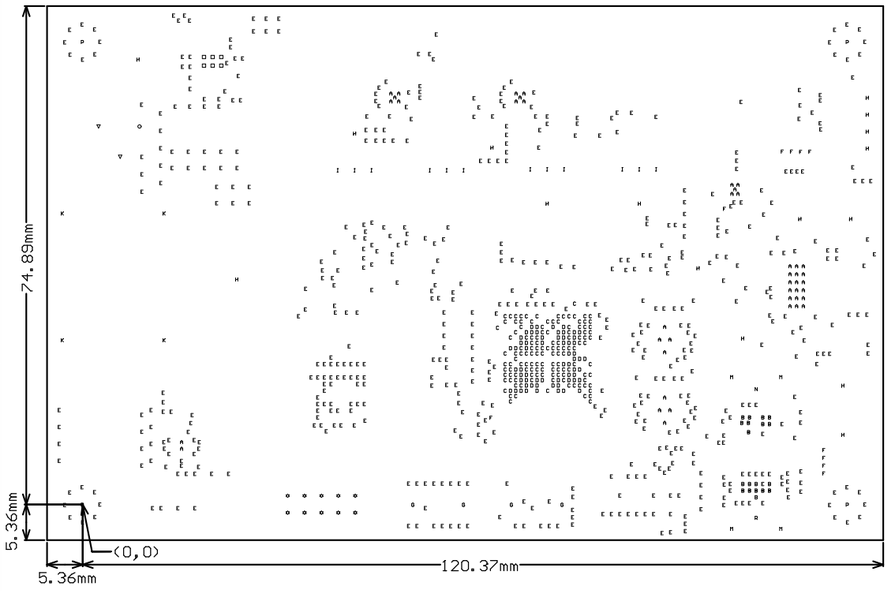
1. BOARD DIMENSION : 125.73MM X 80.25MM.
2. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED VIA TENTING/COVERING REQUIREMENTS.
3. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS OTHERWISE SOLDER MASK IS OPENED IN GERBER.
4. TRACES WITH 6.5MIL TO BE 50 OHMS +/-10% SINGLE ENDED ON TOP LAYER, SIGNAL1, SIGNAL2 & BOTTOM LAYER (L1,L3,L6 & L8).
5. 8.02MIL VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001 ON TOP SIDE ONLY AND +0.000/-0.003 ON BOTTOM SIDE. MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.
6. 8.01MIL VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001 ON BOTTOM SIDE ONLY AND +0.000/-0.003 ON TOP SIDE. MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

LAYER STACK-UP :

	Layer	Name	Material	Thickness	Constant	Board Layer Stack
		Top Overlay				
4		Top Solder	Solder Resist	0.80mil	3.5	
	1	Top Layer		2.80mil		
		Dielectric 1	FR-4 High Tg	4.00mil	4.1	
	2	GND1	CF-004	1.40mil		
4		Dielectric 2	FR-4 High Tg	8.00mil	4.1	
	3	SIGNAL1	CF-004	1.40mil		
		Dielectric 3	FR-4 High Tg	8.00mil	4.1	
	4	POWER1	CF-004	1.40mil		
		Dielectric 4	FR-4 High Tg	6.40mil	4.8	
	5	POWER2	CF-004	1.40mil		
4		Dielectric 5	FR-4 High Tg	8.00mil	4.1	
	6	SIGNAL2	CF-004	1.40mil		
		Dielectric 6	FR-4 High Tg	8.00mil	4.1	
	7	GND2	CF-004	1.40mil		
4		Dielectric 7	FR-4 High Tg	4.00mil	4.1	
	8	Bottom Layer		2.80mil		
		Bottom Solder	Solder Resist	0.80mil	3.5	
		Bottom Overlay				

NOTE : THIS IS AN IMPEDANCE CONTROLLED BOARD.

1. ALL CORE AND PREPREG THICKNESSES ARE UP TO FAB SHOP TO SELECT.
2. EXTERNAL LAYER CU THICKNESSES ARE FINISHED THICKNESS AFTER PLATING.



DRILL TABLE:

	Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Length	Routed Path Length	Hole Tolerance (Mils)
	A	43	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	-	-	+0.00/-7.874
	C	126	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	-	-	+0.00/-8.00
6	D	61	8.01mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	-	-	+0.00/-8.01
5	B	19	8.02mil (0.204mm)	PTH	Round	Top Layer - Bottom Layer	-	-	+0.00/-8.02
	E	601	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	-	-	+0.00/-10.00
	□	6	12.99mil (0.330mm)	PTH	Round	Top Layer - Bottom Layer	-	-	
	F	10	17.72mil (0.450mm)	PTH	Round	Top Layer - Bottom Layer	-	-	+/-3.00
	G	4	29.92mil (0.760mm)	NPTH	Round	Top Layer - Bottom Layer	-	-	+/-2.00
	▽	2	29.92mil (0.760mm)	PTH	Rectangle	Top Layer - Bottom Layer	120.08mil (3.050mm)	120.08mil (3.050mm)	
	H	16	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	-	-	+/-3.00
	I	12	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	-	-	+/-3.00
	O	1	40.16mil (1.020mm)	PTH	Rectangle	Top Layer - Bottom Layer	140.16mil (3.560mm)	140.16mil (3.560mm)	
	✡	10	44.88mil (1.140mm)	PTH	Round	Top Layer - Bottom Layer	-	-	
	K	4	70.87mil (1.800mm)	PTH	Round	Top Layer - Bottom Layer	-	-	+/-3.00
	M	4	92.52mil (2.350mm)	NPTH	Round	Top Layer - Bottom Layer	-	-	+/-2.00
	R	1	94.49mil (2.400mm)	NPTH	Round	Top Layer - Bottom Layer	-	-	+/-2.00
	N	1	94.49mil (2.400mm)	NPTH	Slot	Top Layer - Bottom Layer	116.14mil (2.950mm)	21.65mil (0.550mm)	+/-2.00
	P	4	125.98mil (3.200mm)	PTH	Round	Top Layer - Bottom Layer	-	-	+/-3.00
		925 Total							

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 5 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER _____
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER _____
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☐ MATTE ☒ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: DLP2021AM263Q1EVM
DESIGNED FOR: Public Release
FILE NAME: DLP096A.PcbDoc

ENGINEER: A. Whitehead	LAYOUT BY: SVT
SCALE: 1.12	ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: DLP096	REV: A	SVN REV: Not in version control
LAYER NAME = FAB	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 9/12/2023 11:35:07 AM	TEXAS INSTRUMENTS	

WO# : 309481 - 9479-D