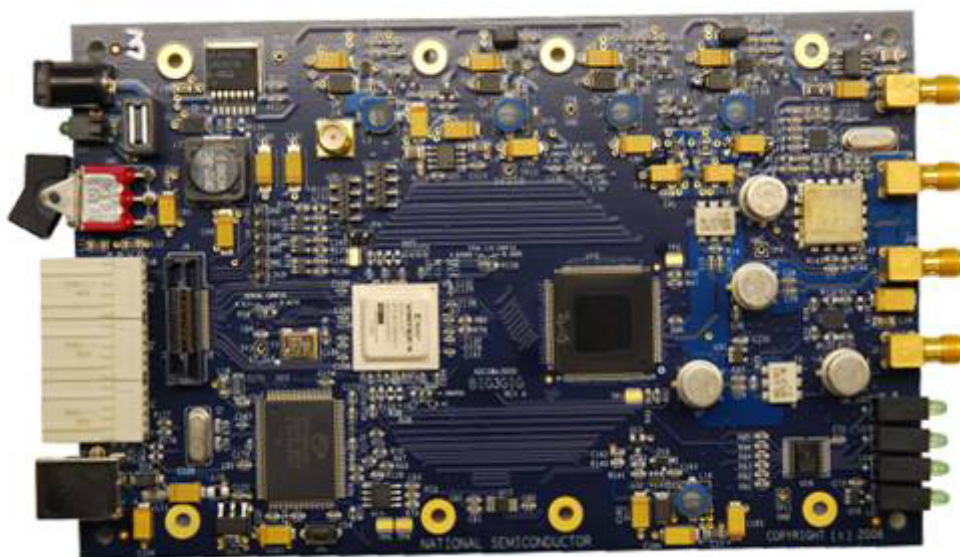


Reference Board User's Guide

**ADC08x3000RB: 8-Bit, 3.0 GSPS, 1.8W A/D Converter with Xilinx
Virtex 4 (XC4VLX15) FPGA**



ADC08x3000RB REFERENCE BOARD USER'S GUIDE – TABLE OF CONTENTS

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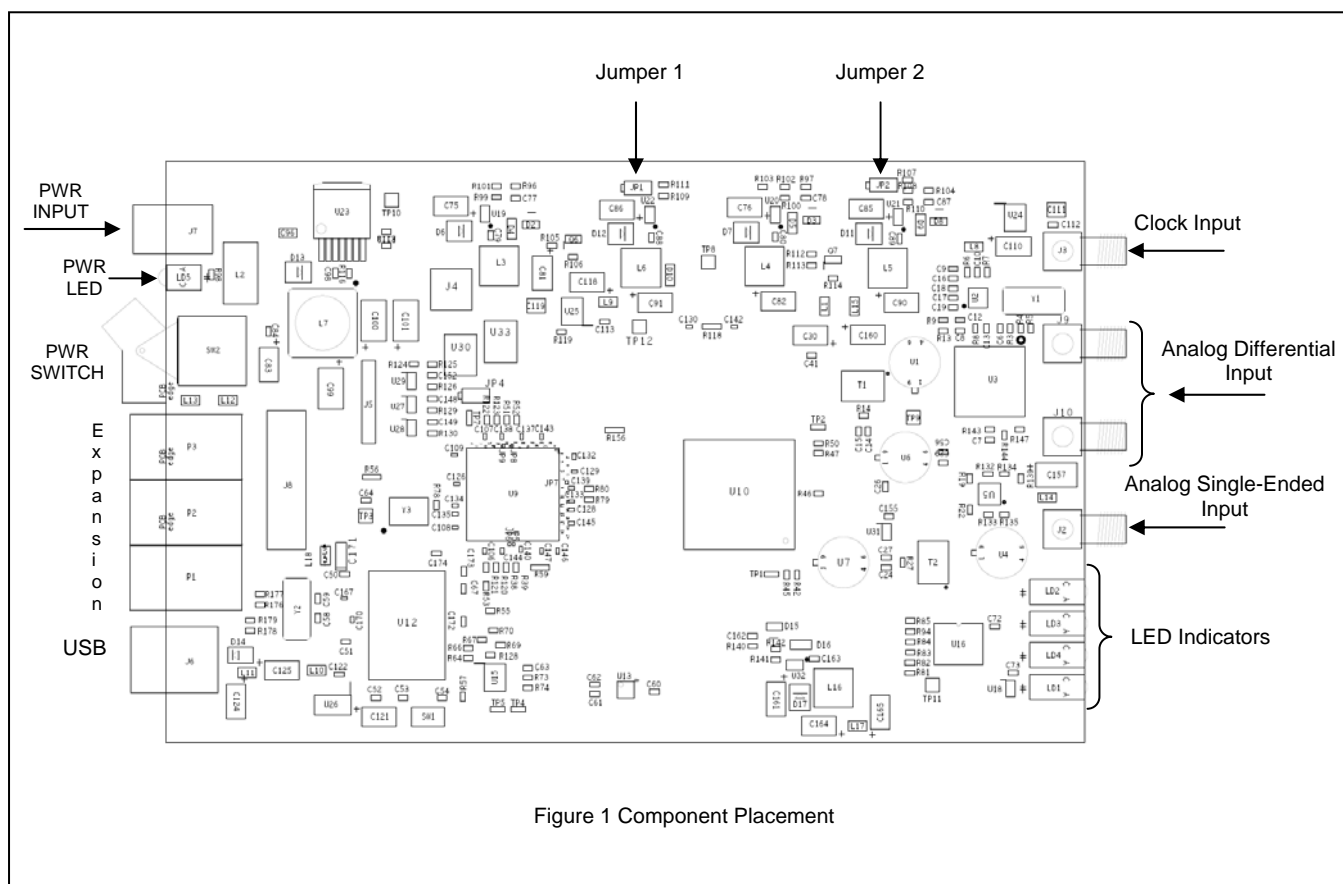
1.0 Introduction

The ADC08x3000RB Board is designed to allow quick evaluation and design development of National Semiconductor's ADC083000 and ADC08B3000 8-bit Analog-to-Digital Converters. These devices are specified for 3.0 GSPS operation. This development board is designed to function with National Semiconductor's WaveVision Software, for fast evaluation. It requires only 3 connections to get started: a Power Supply, a USB Interface to PC and an analog Signal Source. A 1.5GHz Clock generator is provided on board and the system also allows for an external clock to be used if alternative sample rates are required.

The ADC connects to a Xilinx Virtex4 FPGA which stores up to 4K of data from each channel before transferring it through the USB interface to the PC.

2.0 Board Assembly

The ADC08x3000RB Evaluation Board comes as a plain board with rubber standoffs and requires no assisted cooling due to its low power consumption. The ADC083000 and ADC08B3000 devices are configured entirely through software and also allow changes to easily be made to the FPGA configuration to enable system development.



3.0 Quick Start

Refer to Figure 1 for locations of the power connection, signal input and USB port.

IMPORTANT NOTE:

Install the Wavevision 4.3.01.5 Beta ADC08x3000 Software before connecting this product to the PC. See Appendix B – Installing Wavevision. NOTE: If other versions of Wavevision software have previously been installed, they need to be uninstalled prior to installing this version and the “National Semiconductor” folder in the C:\Program Files directory must be deleted. Never install more than one version of WaveVision onto a PC at a time.

For quick start operation:

1. Ensure jumpers 1 and 2 are installed.
2. Connect the 12V DC power source (included with the development board) to the power input (8-12V DC).
3. Push the Power Switch to the ON position and check that the Green LED between the switch and the power connector illuminates.
4. Connect the USB cable (included) from the USB port to a PC. If this is the first time the board has been connected, Windows may install the drivers for this product at this time.
5. Obtain a stable analog source capable of supplying the desired frequencies at up to 8 dBm. Using a band pass filter, connect this source signal to either the single ended input (J2) or the differential inputs (J9 & J10). The exact level needed from the generator will depend upon the insertion loss of the filter used.
6. Start the Wavevision Software
7. Once loaded, the “Firmware Download” Progress bar should be displayed. See Appendix B for more information.
8. Upon Firmware Download completion, the control panel for the board should automatically be displayed on the PC and the CLK LED on the front panel should be on and blinking at a 50% duty cycle indicating the ADC has locked onto the clock signal. Refer to section 10.1 for LED identification.
8. **For the ADC083000:** Set the signal source for the analog input to 8 dBm at the desired frequency. Observe that the Out of Range, (OVR) LED is illuminated. If this LED is not on, increase the input signal source until it

is. Now, reduce the signal source level until the OVR LED just turns off.

From the Wavevision window pull-down menu select **Acquire** and then **Samples**. to activate the overrange sampling circuit. Adjust the input source level after each data capture until the LED just shuts off.

10. From the Wavevision window pull-down menu select **Acquire** and then **Samples**. The system will then capture the input waveform and display the results in the time domain.

11. For FFT Analysis click the FFT Tab.

4.0 Functional Description

The ADC08x3000RB Reference Board schematic is shown in Section 7.0.

4.1 Input circuitry

The analog input signal to be digitized should be applied to the “Analog Single-Ended Input” or the “Analog Differential Input” SMA connectors. These inputs are intended to accept low-noise analog signals. To accurately evaluate the dynamic performance of this converter, the input analog signals will have to be passed through a high-quality bandpass filter with at least 10-bit equivalent noise and distortion characteristics.

This reference board as delivered is set up to handle either a single-ended or a differential analog input. The single-ended input is converted to differential signals on board via a transformer connected as a balun and provides the single-ended to differential conversion for the ADC. The differential PCB traces to the ADC input pins have a characteristic differential impedance of 100 Ohms.

When the DC-coupled input path is selected, a 50Ω DC impedance to ground must exist at the input (signal generator must be DC coupled and only a lowpass filter should be used). Should an AC-coupled signal generator or a bandpass filter be required, the AC-coupled input path should be used. However, should the customer desire to use an AC-coupled source or a bandpass filter with the DC-input path selected, a 49.9Ω resistor should be populated to the device location R24 to ensure the 50Ω DC impedance requirement is met.

No scope or other test equipment should be connected anywhere in the signal path while gathering data.

4.2 ADC reference

The ADC083000 and ADC08B3000 have an internal reference that can not be adjusted. However, the Full-Scale (differential) Range may adjusted with the Software Control Panel Refer to Section 9.0 for more information

4.3 ADC clock

The ADC clock is supplied on board and is fixed at 1.5GHz. An external clock signal may be applied to the ADC through the SMA Connector labeled in Figure 1 as "Clock Input". The balun-transformer (T1) converts the single ended clock source to a differential signal to drive the ADC clock pins. **When using the internal clock, be sure to physically isolate the external clock signal (either gate the signal generator off or remove the external clock cable).**

Note that it is very important that the ADC clock should be as free of jitter as possible or the apparent SNR of the ADC device will be compromised.

When switching from an external reference clock to the internal reference clock, or from an internal clock to an external clock, be sure to press the "Test Communication" button in the Capture Settings window.

4.4 Digital Data Output

The digital output data from the ADC is connected to a Xilinx Virtex 4 FPGA. Up to 4K Bytes of data per channel can be stored and then uploaded over the USB interface to the Wavevision software. The FPGA logic usage is low allowing further code to be written and tested for product development.

4.5 Power Requirements

The power supply requirement for the ADC08x3000RB Reference Board is 12V at 800mA.

Most of the regulators on board are switching regulators for increased power efficiency.

The board typically draws around 500mA but it is always good practice to have extra power reserve in the power supply over the typical power requirements.

A Universal 100-240V AC input to 12V DC Brick Power Supply is included with the development board.

4.6 Power Supply Connections

Power to this board is supplied through the power connector. It is advised that only the supplied PSU is used with this board.

The ADC supply voltage has been set to 1.9V, ± 50 mV using on board regulators.

5.0 Obtaining Best Results

Obtaining the best results with any ADC requires both good circuit techniques and a good PC board layout. For layout information for this product please contact you nearest National Semiconductor representative.

5.1 Clock Jitter

When any circuitry is added after a signal source, some jitter is almost always added to that signal. Jitter in a clock signal, depending upon how bad it is, can degrade dynamic performance. We can see the effects of jitter in the frequency domain (FFT) as "leakage" or "spreading" around the input frequency, as seen in Figure 2a. Compare this with the more desirable plot of Figure 2b. Note that all dynamic performance parameters (shown to the right of the FFT) are improved by eliminating clock jitter.

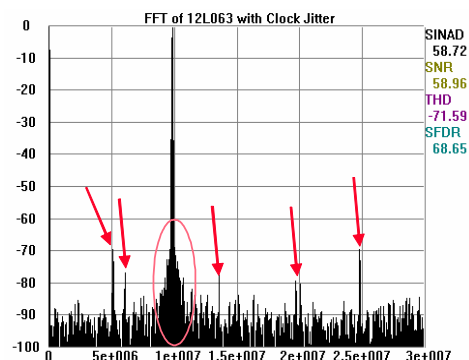


Figure 2a. Jitter causes a spreading around the input signal, as well as undesirable signal spurs.

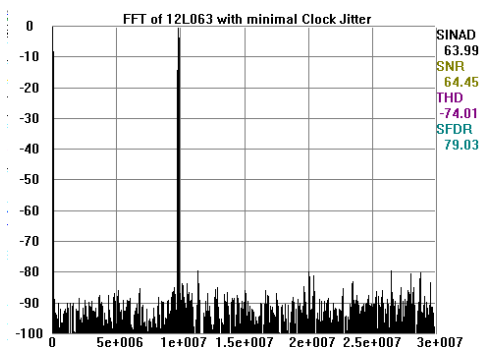
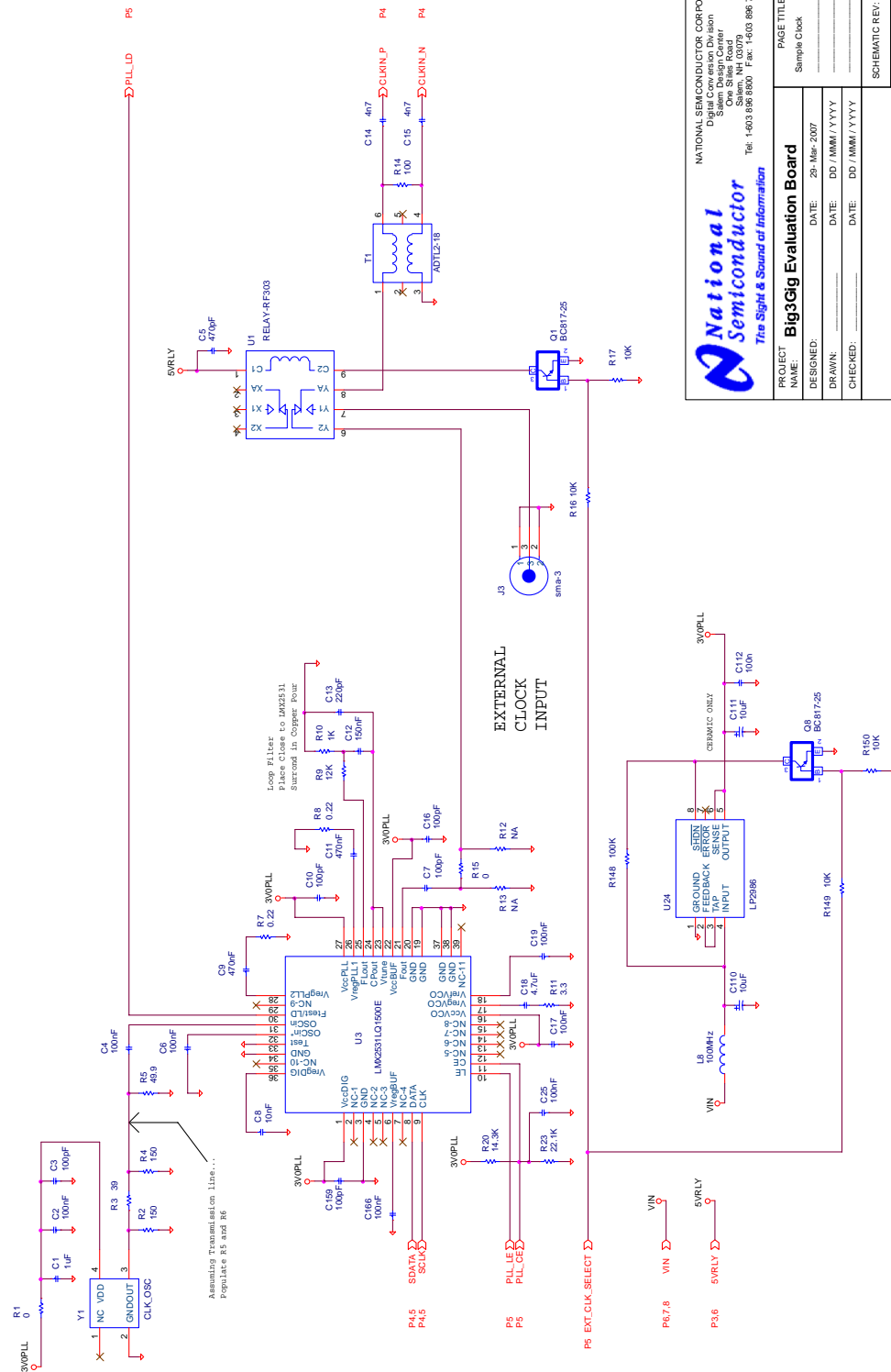



Figure 2b. Eliminating or minimizing clock jitter results in a more desirable FFT that is more representative of how the ADC actually performs.

6.0 Reference Board Specifications

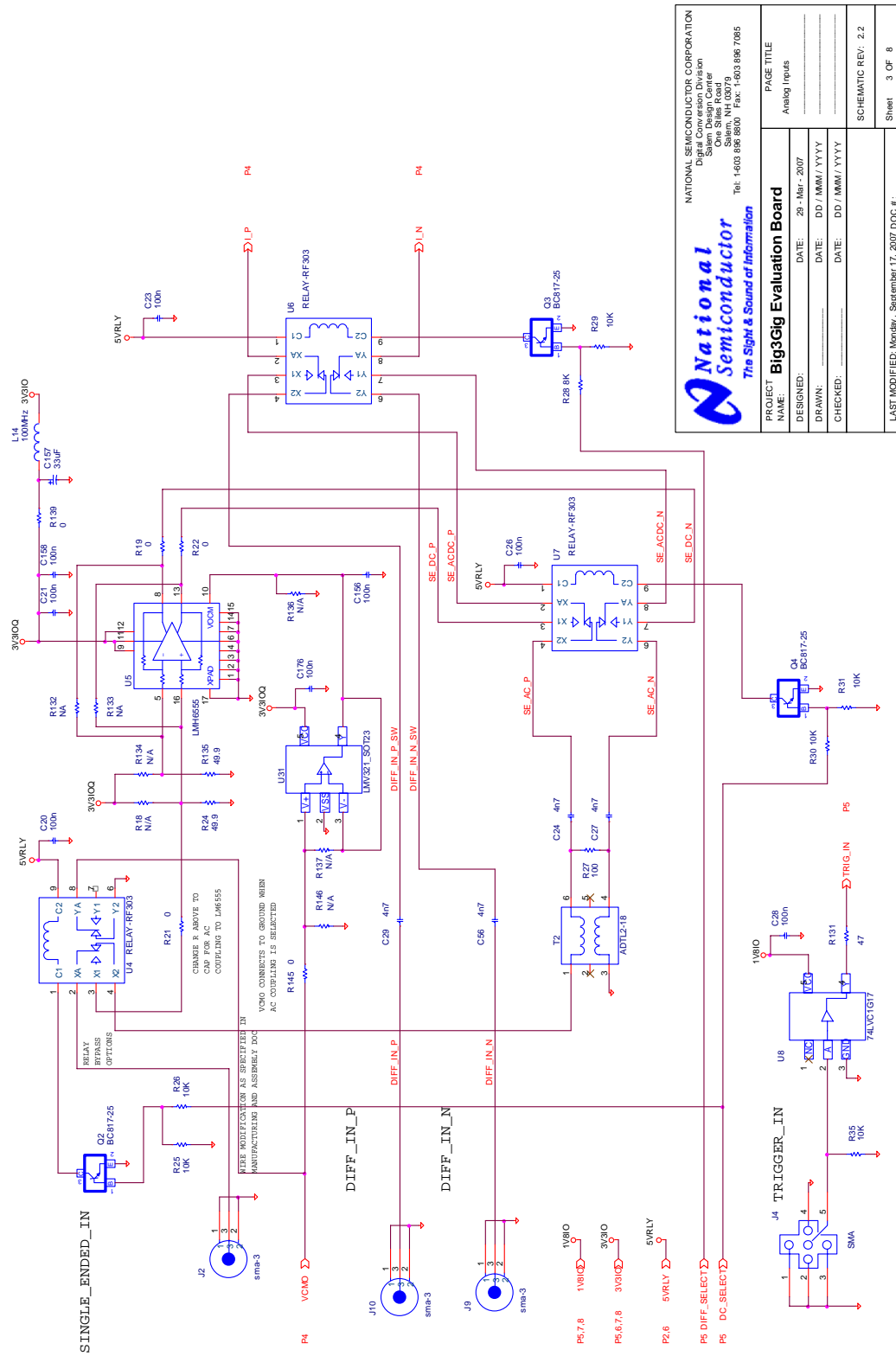
Board Size:	168mm x 100mm
Power Requirements:	+12V, 800mA
Clock Frequency Range :	800 MHz to 1.5 GHz
Analog Input Range (AC Coupled)	30MHz to 1800MHz
Nominal Analog Input Voltage:	600 mV P-P to 800 mV P-P
Impedance:	50 Ohms

7.0 Schematic Drawing ADC08x3000RB – Onboard Clock (VCO + PLL)

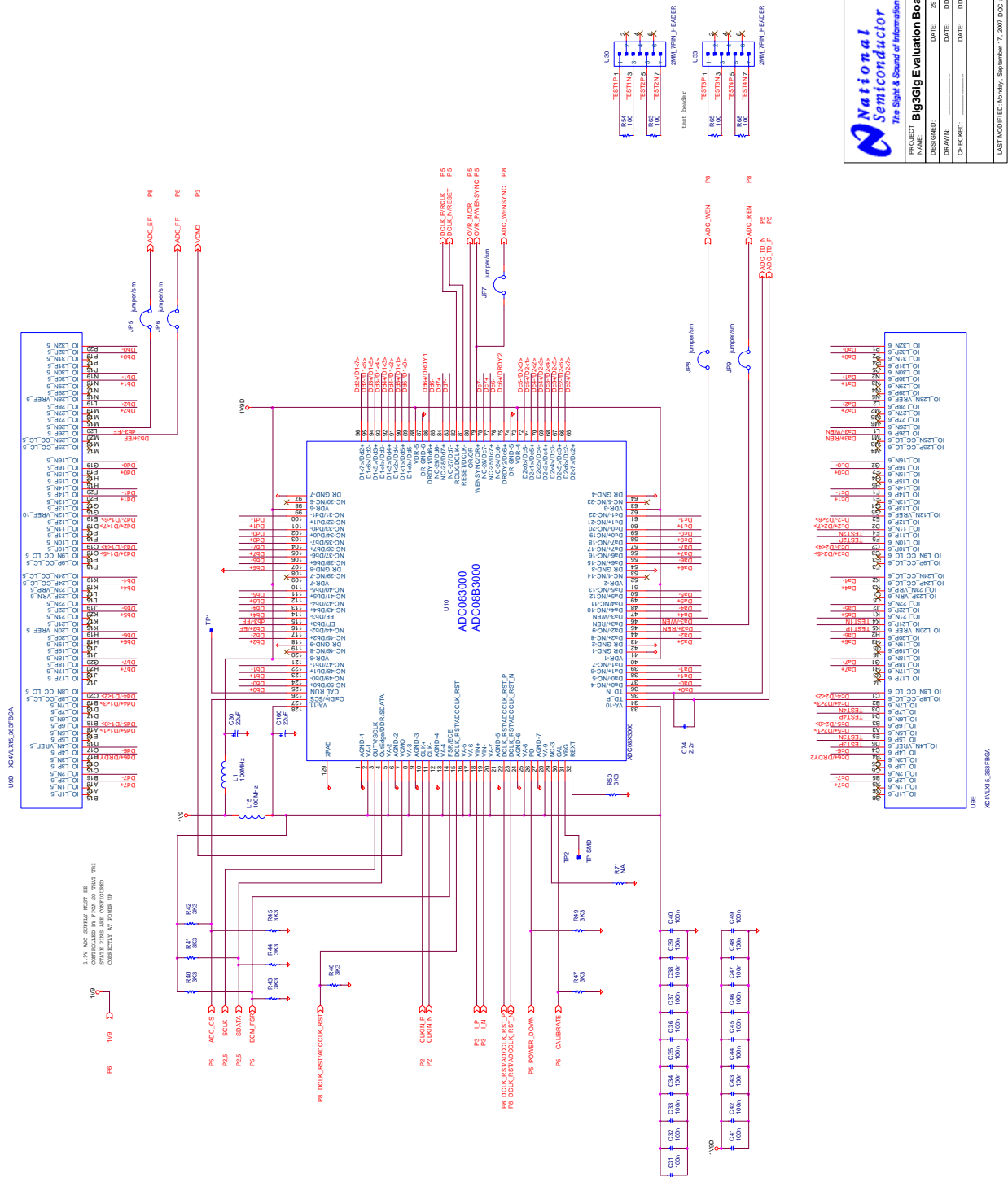


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	PROJECT NAME: Big3Gig Evaluation Board	PAGE TITLE Sample Clock		
		DESIGNED: 29-Mar-2007 DATE: _____ DRAWN: _____ DATE: DD / MM / YYYY CHECKED: _____ DATE: DD / MM / YYYY	SCHEMATIC REV: 2.2 Sheet OF 8	
LAST MODIFIED: Friday, September 21, 2007 DOC # :				

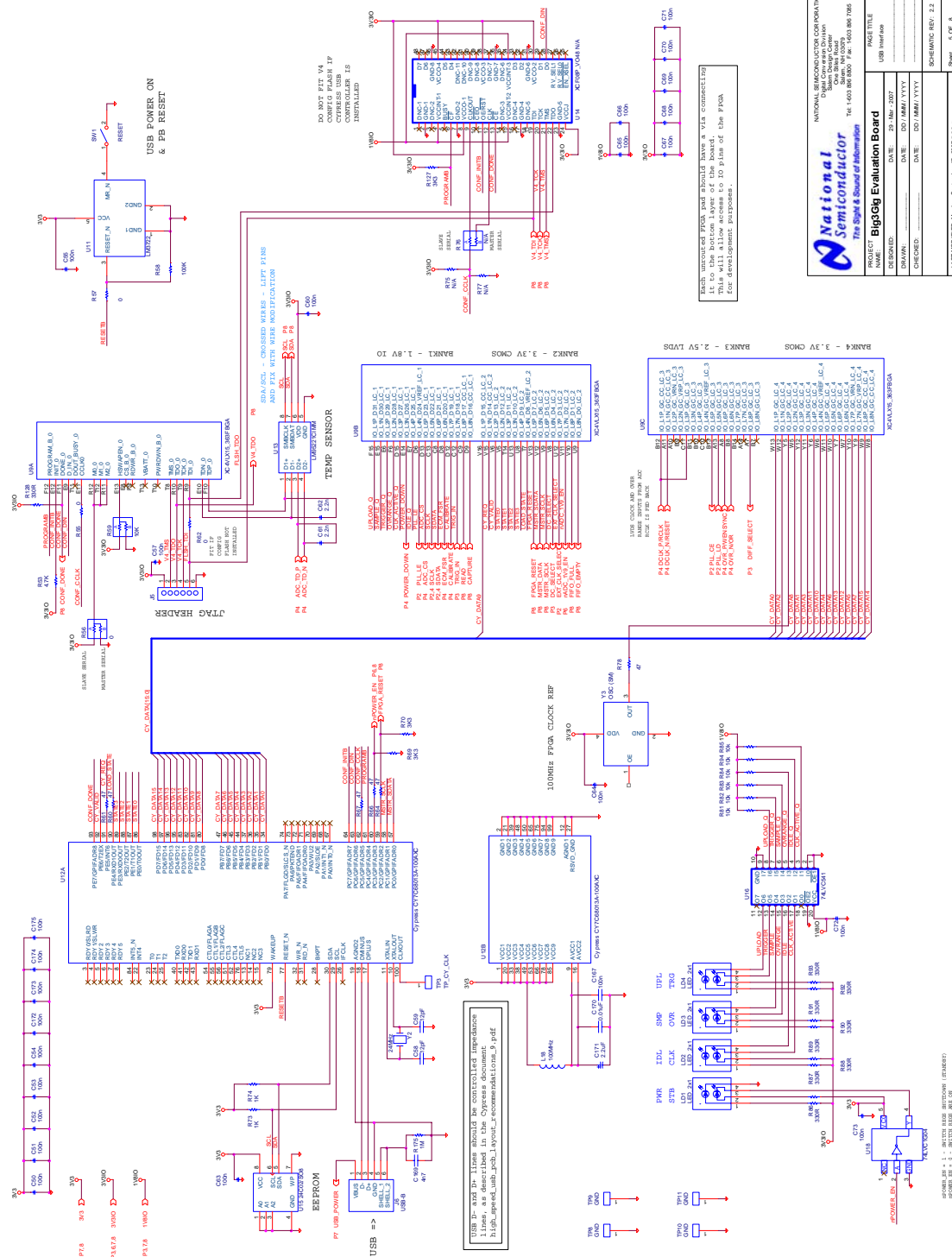
7.1 Schematic Drawing ADC08x3000RB – Analog Inputs



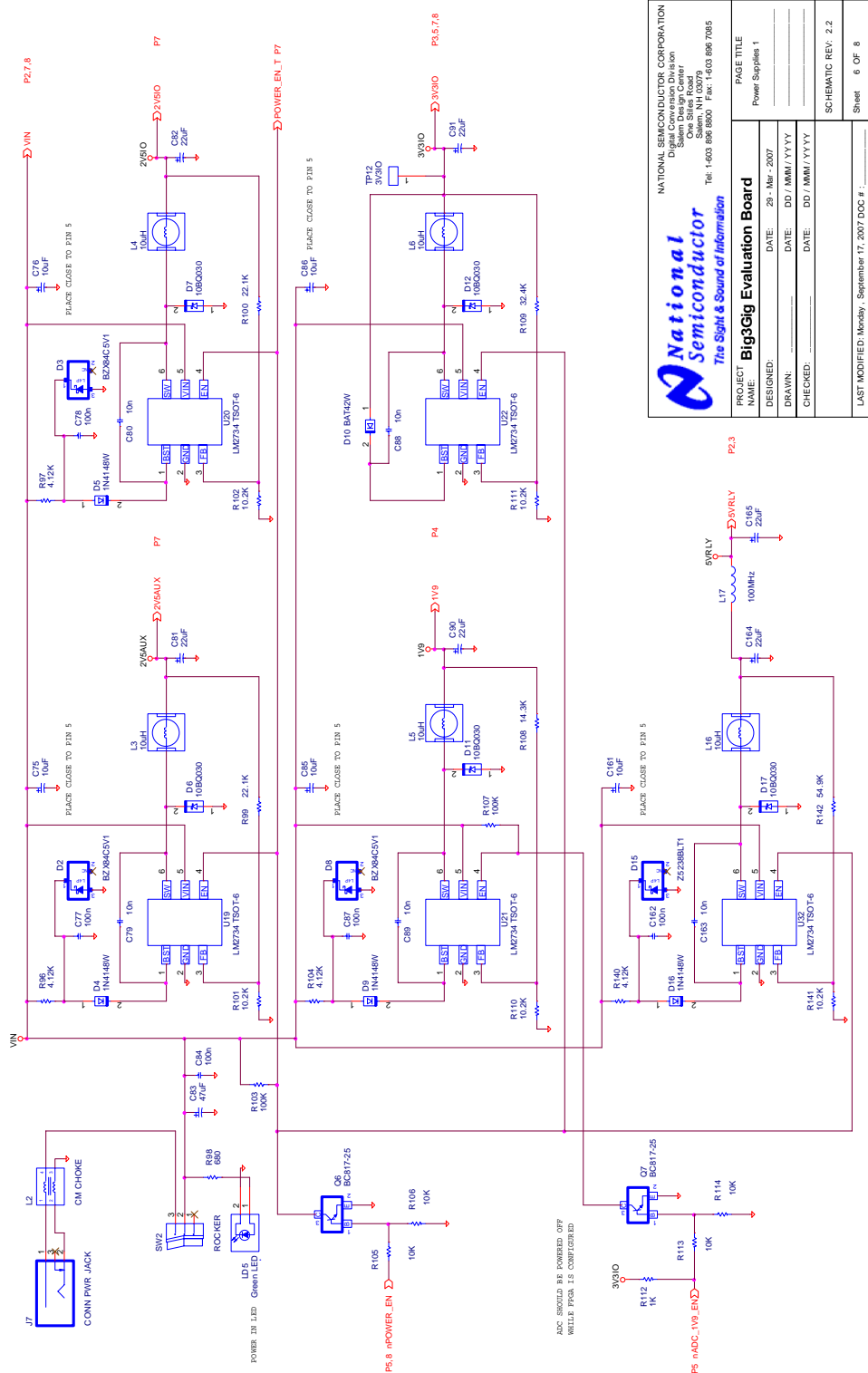
7.2 Schematic Drawing ADC08x3000RB – ADC connected to Virtex4 FPGA




7.3 Schematic Drawing ADC08x3000RB – USB Interface

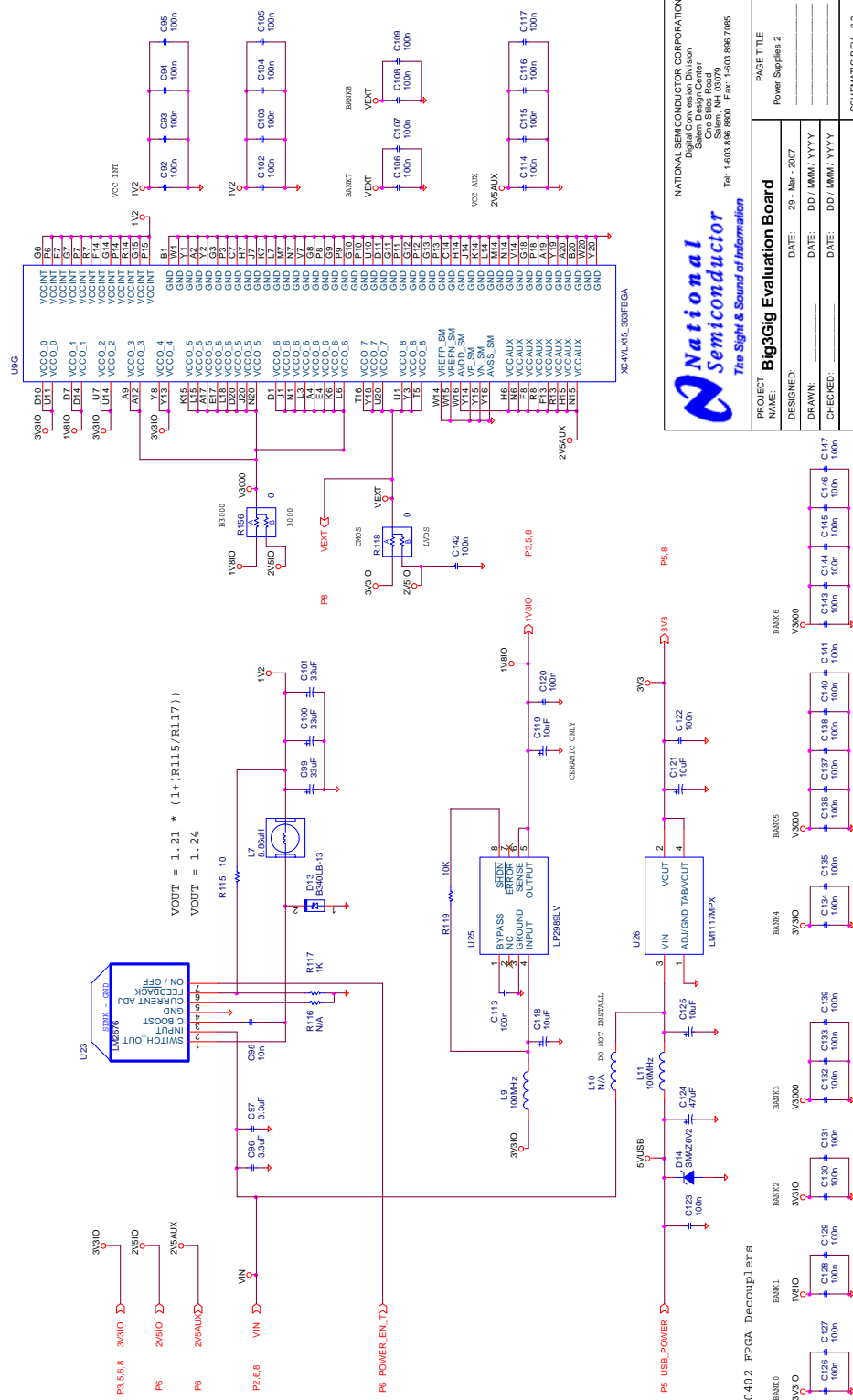


7.4 Schematic Drawing ADC08x3000RB – Power Supplies 1

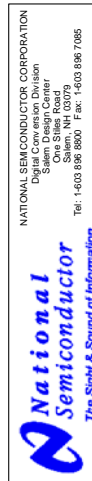


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	CHECKED: DATE: DD / MM / YYYY		SCHEMATIC REV: 2.2	
LAST MODIFIED: Monday, September 17, 2007 10:00 a.m.				Sheet 6 OF 8

7.5 Schematic Drawing ADC08x3000RB – Power Supplies 2

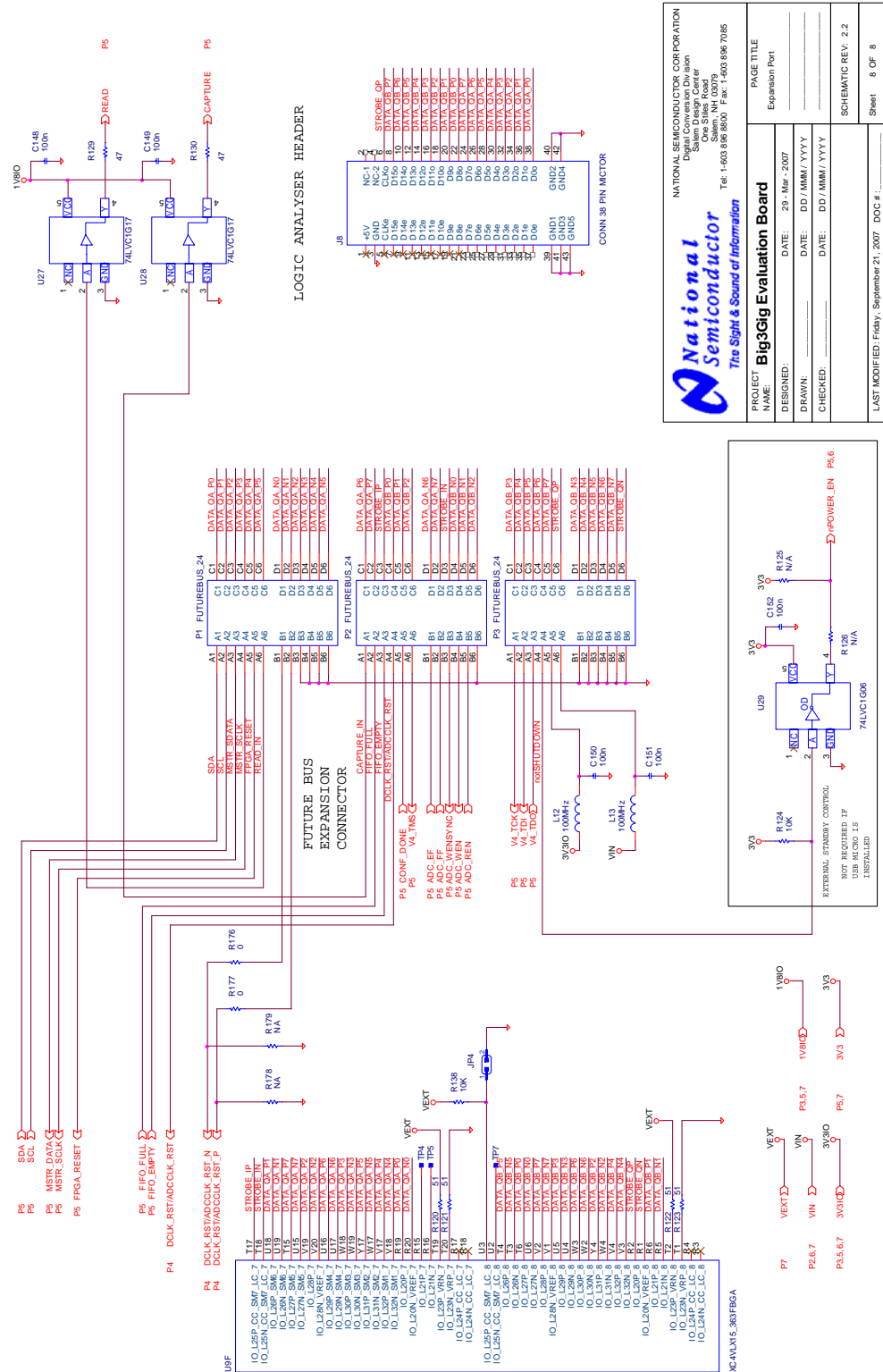


0402 FPGA Decouplers



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LAST MODIFIED: Monday, September 17, 2007 DDC #: _____			SCHWATIC REV: 2.2
			Sheet OF 8

7.6 Schematic Drawing ADC08x3000RB – Expansion Header Interface



8.0 Bill of Materials (Page 1 of 2)

NATIONAL SEMICONDUCTOR						
		Total QTY for Board Build	ADC08X3000 R2.2 BUILD			
Item	Qty		Part Reference	Value	Description	Manufacturer Part Number
SMT Capacitors						
1	1		C1	1uF	Capacitor, SMT 0603, MLC, X5R, 10%, 16V	Panasonic ECJ-1VB1C105K
2	72		C2,C4,C8,C17,C19,C20,C21, C23,C26,C28,C31,C32, C33,C34,C35,C36,C37,C38, C39,C40,C41,C42,C43,C44, C46,C48,C47,C48,C49,C50, C51,C52,C53,C54,C55,C57, C60,C63,C64,C65,C66,C67, C68,C69,C70,C71,C72,C73, C77,C78,C84,C87,C112, C113,C120,C122,C123,C148, C149,C150,C151,C162,C166, C168,C162,C166,C172,C173, C174,C175,C176	100n	Capacitor, SMT 0603, MLC, X7R, 10%, 16V	Panasonic ECJ-1VB1C104K
3	4		C3,C10,C16,C159	100pF	Capacitor, SMT 0603, MLC, NPO, 5%, 50V	Panasonic ECJ-1VC1H101J
4	1		C5	470pF	Capacitor, SMT 0603, MLC, NPO, 5%, 50V	Panasonic ECJ-1VC1H471J
5	1		C7	100pF	Capacitor, SMT 0402, MLC, X7R, 5%, 50V	Panasonic ECJ-0EC1H101J
6	7		C8,C79,C80,C88,C89,C96, C163	10n	Capacitor, SMT 0603, MLC, X7R, 10%, 16V	Panasonic ECJ-1VB1C103K
7	2		C9,C11	0.47uF	Capacitor, SMT 0603, MLC, X7R, 10%, 16V	Kemet C0603C474K4RACTU
8	1		C12	0.15uF	Capacitor, SMT 0603, MLC, X7R, 10%, 16V	MuRata GRM188R71C154KA01D
9	1		C13	220pF	Capacitor, SMT 0603, MLC, NPO, 5%, 50V	Panasonic ECJ-1VC1H221J
10	6		C14,C15,C24,C27,C29,C56	4n7	Capacitor, SMT 0402, MLC, X7R, 10%, 25V	Panasonic ECJ-0EB1E472K
11	1		C18	4.7uF	Capacitor, SMT 0603, MLC, NPO, 5%, 50V	Panasonic ECJ-1VC1H101J
12	8		C30,C81,C82,C90,C91,C160, C164,C165	22uF	CAP 22UF 16V TANTALUM TEL SMD	EPCOS Inc B45197A3226K309
13	2		C58,C59	12pF	CAP CERAMIC 12PF 50V 0603 SMD	Panasonic ECJ-1VC1H120J
14	3		C61,C62,C74	2.2n	Capacitor, SMT 0603, MLC, X7R, 10%, 50V	Panasonic ECJ-1VB1H222K
15	9		C75,C76,C85,C86,C110, C118,C121,C125,C161	10uF	CAP 10UF 20V TANTALUM TEL SMD	Kemet T491C106K020AT
16	2		C83,C124	47uF	CAP 47UF 20V TANTALUM TEL SMD	AVX TAJC476K020R
17	39		C92,C93,C94,C95,C102, C103,C104,C106,C108,C107, C108,C109,C114,C115,C116, C117,C126,C127,C128,C129, C130,C131,C132,C133,C134, C135,C136,C137,C138,C139, C140,C141,C142,C143,C144, C145,C146,C147,C167	100n	Capacitor, SMT 0402, MLC, X5R, 10%, 10V	Panasonic ECJ-0EB1A104K
18	2		C96,C97	3.3uF	Capacitor, SMT 1206, MLC, X5R, 10%, 25V	Kemet C1206C335K3PACTU
19	4		C99,C100,C101,C157	33uF	CAP 33UF 16V TANTALUM TEL SMD, 10%	Kemet T491C336K016AT
20	2		C111,C119	10uF	CAP 10UF 20V CERAMIC TEL SMD	Kemet C1210C106K4PACTU
21	1		C169	4n7	Capacitor, SMT 0603, MLC, X7R, 10%, 50V	Panasonic ECJ-1VB1H472K
22	1		C170	0.01uF	CAP CERAMIC 0.01uF 0402 SMD	Kemet C0402C103J3RACTU
23	1		C171	2.2uF	CAP 2.2UF SMD Size 3216	Kemet T491A225K010AT
Diodes						
24	3		D2,D3,D8	BZX84C5V1	DIODE ZENER 5.1V 350MW SOT-2	Diodes Inc BZX84C5V1-7-F
25	4		D4,D5,D9,D16	1N4148W	DIODE SWITCH 75V 400MW SOD-123	Diodes Inc 1N4148W-7-F
26	5		D6,D7,D11,D12,D17	10BQ030	DIODE SCHOTTKY 30V 1A DO-214AA	International Rectifier 10BQ030PBF
27	1		D10	BAT42W	DIODE SCHOTTKY 30V 200MW SOD-123	Diodes Inc BAT42W-7-F
28	1		D13	B340LB-13	RECTIFIER SCHOTTKY 40V 3A SMB	Diodes Inc B340LB-13-F
29	1		D14	SMAZ6V2	DIODE ZENER SMD 6.2V 1W SMA	DIODES INC. SMAZ6V2-13-F
30	1		D16	Z6238BLT1	DIODE ZENER 8.7V 225MW SOT-23	ON Semiconductor MMBZ6238BLT1G
Connectors						
31	1		P4	JUMPER 2X1	HEADER 2X1 0.1" SP MALE STR	Sullins PBC36SAAN
32	4		J2,J3,J9,J10	SMA-3	CONN JACK SMA 50 OHMS EDGE MOUNT	Emerson 142-0761-841
33	1		J4	SMA	CONN SMA RECEPTLE STRAIGHT PCB GO	Amphenol 901-144-3RFX
34	1		J6	CONN 6 PIN SINGLE ROW	HEADER 6X1 0.1" SP MALE STR	Sullins PBC36SAAN
35	1		J6	USB-B	USB Connector Type B, Single Through Hole	Mill-Max 897-43-004-90-000000
36	1		J7	CONN PWR JACK	CONN PWR JACK 2.5X5.5MM HIGH CUR	CUI Inc PJ-102BH
37	1		J8	CONN 38 PIN MICTOR	MICTOR VERTICAL RECEPT. 38 POS	AMP/Tyco Electronics 5787054-1
38	3		P1,P2,P3	FUTUREBUS_24	CONN RCEPT RTANG 2MM 24POS 30AU	AMP/Tyco Electronics 5536511-1
Ferrites						
39	10		L1,L8,L9,L11,L12,L13,L14, L15,L17,L18	100MHz	FERRITE CHIP 120 OHM 3000MA 1206	Murata BLM31PG121SN1L
40	1		L2	CM CHOKE	CHOKE COMMON MODE 170 OHMS PCB	Steward CM2545X171B-10
41	5		L3,L4,L5,L6,L16	10uH	INDUCTOR SHIELD PWR 10UH 7032	TDK SLF7032T-100M1R4-2-PR
42	1		L7	8.86uH	INDUCTOR SHIELD PWR 8.2UH SMD	Coiltronics DR127-8R2-R

8.1 Bill of Materials (Page 2 of 2)

Item	Qty	Part Reference	Value	Description	Manufacturer	Manufacturer Part Number
Resistors						
43	12	R1,R19,R21,R22,R55,R57, R62,R137,R139,R145,R176,R177	0	RES 0 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEY0R00V
44	2	R2,R4	150	RES 150 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ151V
45	1	R3	39	RES 39 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ390V
46	2	R5,R135	49.9	RES 49.9 OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF49R9V
47	2	R7,R8	0.22	RES 0.22 OHM 1/8W 1% 0603 SMD	Susumu Co Ltd	RP1608S-R22-F
48	1	R9	12K	RES 12K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ272V
49	5	R10,R73,R74,R112,R117	1K	RES 1K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ102V
50	1	R11	3.3	RES 3.3 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ3R3V
51	2	R14,R27	100	RES 100 OHM 1/16W 5% 0402 SMD	Panasonic	ERJ-2GEJ101X
52	1	R15	0	RES 0 OHM 1/16W 5% 0402 SMD	Panasonic	ERJ-2GE0R00X
53	23	R16,R17,R25,R26,R29,R30, R31,R35,R61,R62,R63,R64, R85,R94,R105,R106,R113, R114,R119,R124,R136,R149, R150	10K	RES 10K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ103V
54A	1	R20	4.42K	RES 4.42K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF4421V
54	1	R108	14.3K	RES 14.3K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1432V
55	3	R23,R99,R100	22.1K	RES 22.1K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1212V
56	1	R28	8K	RES 8.06K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF8061V
57	13	R40,R41,R42,R43,R44,R45, R46,R47,R49,R50,R69,R70, R127	3K3	RES 3.3K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ332V
58	1	R53	4.7K	RES 4.7K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ472V
59	4	R54,R63,R65,R68	100	RES 100 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ101V
60	4	R56,R103,R107,R148	100K	RES 100K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ104V
61	9	R60,R61,R64,R66,R67,R78, R129,R130,R131	47	RES 47 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ470V
62	9	R66,R67,R68,R69,R90,R91, R92,R93,R128	330R	RES 330 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ331V
63	4	R66,R97,R104,R140	4.12K	RES 4.12K OHM 1/10W 0.1% 0603 SMD	Susumu Co Ltd	RR0816P-4121-B-T5-60H
64	1	R68	680	RES 680 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ681V
65	5	R101,R102,R110,R111,R141	10.2K	RES 10.2K OHM 1/10W 0.5% 0603 SMD	Susumu Co Ltd	RR0816P-1022-D-02C
66	1	R109	32.4K	RES 32.4K OHM 1/10W 0.5% 0603 SMD	Susumu Co Ltd	RR0816P-3242-D-50C
67	1	R115	10	RES 10 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ100V
68	4	R120,R121,R122,R123	51	RES 51 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ510V
69	1	R142	54.9K	RES 54.9K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3EKF5492V
70	1	R175	1M	RES 1.0M OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ105V
71	4	U1,U4,U6,U7	RELAY-RF303	RF RELAY DPDT	Teledyne	RF303-6
IC's						
72	1	U3	LMX2531LQ1500E	1.5GHz Centre Frequency PLL, 3V		
73	1	U5	LMH6555			LMH6555/NOPB
74	3	U8,U27,U28	74LVC1G17	IC SCHMITT-TRIG BUFF SOT-23-5	TI	SN74LVC1G17DBVR
75	1	U9	XC4VLX15_363FBGA	VIRTEX 4 363 pin FPGA	Xilinx	XC4VLX15-10SF6363C
76	1	U10	ADC08x3000	ADC08x3000 128 PIN Exposed Pad TOFP	NSC	ADC08x3000-C1YB/NOPB
77	1	U11	LM3722	5-pin uP reset ckt, sot23-5 pkg, LM3722EM5-3.08	NSC	LM3722EM5-3.08/NOPB
78	1	U12	Cypress CY7C68013A-100AXC			CY7C68013A-100AXC
79	1	U13	LM95221CIMM	LM95221 Dual Remote Diode Digital Temperature Sensor	NSC	LM95221CIMM/NOPB
80	1	U15	24C02/SO8	EEPROM 2 WIRE 2Kbit (256 x 8) 8 Pin SOIC	ATMEL	AT24C02BN-10SU-1.8
81	1	U16	74LVC641	IC OCT BUFF/DRVR TRI-ST 20-SSOP	Texas Instruments	SN74LVC641ADBR
82	1	U18	74LVC1G04	IC SINGLE INVERTER-GATE SOT-23-5	Texas Instruments	SN74LVC1G04DBVR
83	5	U19,U20,U21,U22,U32	LM2734 TSOT-6	IC PWM STP-DWN REG 1A SOT23-6	NSC	LM2734YMKCT-ND/NOPB
84	1	U23	LM2676	IC REG SIMPLE SWITCHER TO-263-7	NSC	LM2676S-ADJ-ND/NOPB
85	1	U24	LP2986	IC REGULATOR MICROFWR LDO 8-SOIC	NSC	LP2986IM-3.0-ND/NOPB
86	1	U25	LP2989LV	IC REGULATOR MICROFWR LDO 8-SOIC	NSC	LP2989IM-1.8-ND/NOPB
87	1	U26	LM1117MPX	IC REG 3.3V 800MA LDO SOT-223	National Semiconductor	LM1117MPX-3.3CT-ND/NOPE
88	1	U29	74LVC1G06	IC INVERTER BUFF/DRVR SOT-23-5	TI	SN74LVC1G06DBVR
89	2	U30,U33	2MM_7PIN_HEADER		Samtec	FTR-107-03-G-S
Misc						
91	4	LD1,LD2,LD3,LD4	LED_2x1	LED 3MM 2-HIGH GREEN/GREEN PCMNT	Lumex	SSF-LXH2103GGDI4
92	1	LD5	GREEN LED	LED 3MM RA FAULT-IND GRN PC MNT	Lumex	SSF-LXH103GD
93	7	Q1,Q2,Q3,Q4,Q6,Q7,Q8	BC817-25	TRANS NPN GP 500MA 45V SOT23	ON Semiconductor	BC817-25L1TG
94	1	SW1	RESET	SWITCH TACT MOM 130Gf H=6MM	ITT INDUSTRIES	PT5635SL60
95	1	SW2	ROCKER	SWITCH ROCKER SPDT HORZ ACT RA	ITT Industries/C&K Div	7101J1AQE2
96	2	T1,T2	ADTL2-18	RF TRANSFORMER SMT 6 PINS upto 1.8GHz	Mini Circuits	ADTL2-18+
97	1	Y1	60MHz	CCHD-950 SERIES, CMOS ULTRA LOW PHASE NOIS	Crystek	CCHD-950-25-60
				or	Pietronics	SM7744HV-60.0M
				or	Vectron	VCC1-F3A-60M000
98	1	Y2	24MHz	CRYSTAL 24.000MHZ	ECS Inc.	ECS-240-12-5PX-TR
99	1	Y3	OSC (SM)	OSCILLATOR 100.0000 MHZ SMT	Pietronics	SM7745DSV-100.00 M
100	1	POWER SUPPLY		External Plug-in Power Supply Output Voltage:12.0V	XP Power	AED70US12
101		ALTERNATIVE POWER SUPPLY		External Plug-in Power Supply Output Voltage:12.0V	ELPAC	FW3012-760F
DO NOT SOLDER THE FOLLOWING TO BOARD						
102	1	U31	LM321_SOT23	LM321 Low Power Single Op-Amp	National	LM321MF/NOPB
103	2	L10	N/A	FERRITE CHIP 120 OHM 3000MA 1206	Murata	BLM31PG121SN1L
104	14	R12,R13	NA	RES 0 OHM 1/16W 5% 0402 SMD	Panasonic	ERJ-2GE0R00X
		R18,R71,R75,R77,R116, R125,R126,R132,R133,R134, R136,R146,R175,R179	NA	RES 0 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEY0R00V
105	1	R76	NA	RES 0 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEY0R00V
106	4	R56,R59,R118,R156	0	RES 0 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEY0R00V
107	1	U14	XCFO8P_VO48 N/A	Xilinx Configuration Flash ROM (8Mb) JTAG	Xilinx	XCFO8P VO48 C
108	5	JP5,JP6,JP7,JP8,JP9	jumper/5m	bridge jumper		
109	1	R24	NA	RES 49.9 OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF49R9V

9.0 Using the Wavevision software with the ADC08x3000RB

IMPORTANT NOTE: Before connecting this board to the PC, please install the Wavevision Software from the CDROM included with the development kit. (See Appendix B)

Connecting the Development Board before installation may result in the board being registered as an unknown USB device. If this happens you will need to uninstall the device using the Windows Device Manager before installing the Wavevision Software.

NOTE: If other versions of Wavevision software have previously been installed, they need to be uninstalled prior to installing this version and the “National Semiconductor” folder in the C:\Program Files directory must be deleted. Never install more than one version of WaveVision onto a PC at a time.

9.1 Getting Started

This development board is designed to connect over a USB interface to a PC running the Wavevision Software.

Ensure the board is connected to the 12V power supply (included in the package) and that the switch on the rear panel is pushed to the “ON” position. The Green LED near the power switch should be illuminated if on.

Connect the USB cable between the PC which has Wavevision software installed and the ADC08x3000RB board.

If this is the first time the board has been connected to the PC, Drivers may be required to be installed (automatic) by the Operating System. Follow the on screen instructions and use the recommended settings.

Start the Wavevision software (Start -> All Programs -> Wavevision -> Wavevision 4)

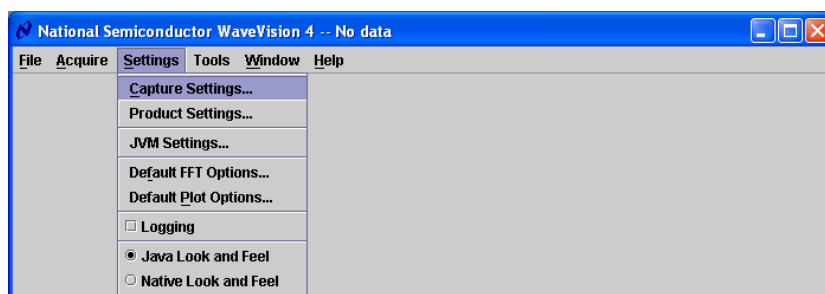
The software may take several seconds to initialize, but should display a welcome screen similar to the following.



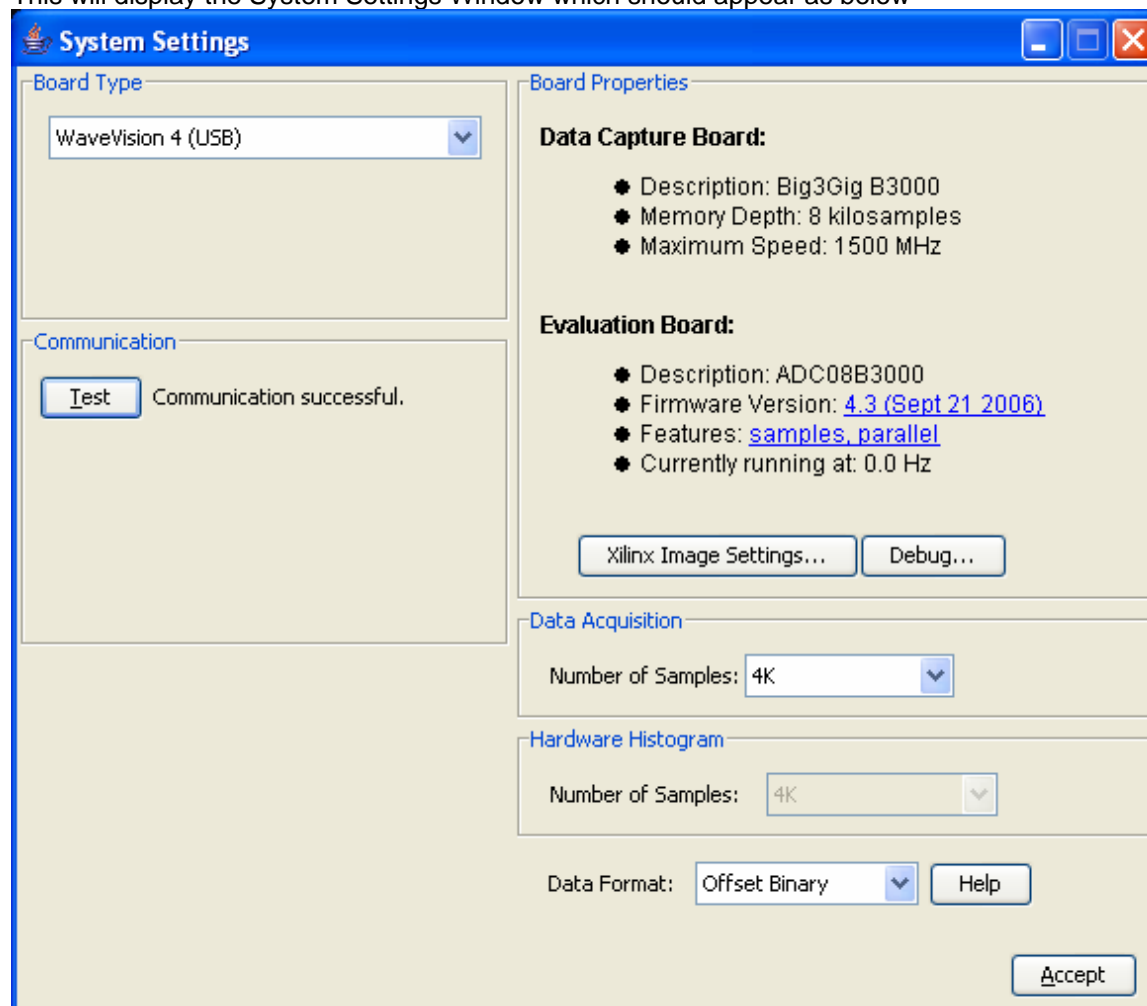
If the board is connected correctly the following popup box should appear to indicate that the board has been recognized and the firmware for the FPGA is being downloaded over the USB interface



If the "Downloading firmware" box does not appear automatically, click on the "Settings" pulldown menu and then click Capture Settings as shown below.



This will display the System Settings Window which should appear as below



If the board has not been detected click the “Test” button under the Communication heading and the development board should be found. If the communications fail, check that the USB drivers are installed correctly, then disconnect and re-connect the USB cable. Finally restart the Wavevision software See Appendix B for more information.

9.2 Control Panel

Once the FPGA Firmware download has completed one of the development board Control Panels will automatically be displayed as shown below.

The screenshot shows the ADC083000 Control Panel. The top status bar displays 'FPGA Temp 47.125 DegC' and 'ADC Temp 65.000 DegC'. The 'Control' tab on the left includes settings for Hardware/Serial (Hardware Pin Control), OutV (Low Amplitude), OutEdge (Rising Edge), DDR (Enable Dual Data Rate), FSR (600mv Full Scale), Standby (Active), PD (Disable Shutdown), DC_Coup (AC Coupling), Ext Clock (Internal Clock), and Diff In (Differential Data). The 'Registers' section on the right shows Addr 1: Configuration Register (DRE, RTD, DCS, DCP, nDE, OV, OE), Addr 2: Offset Register (0.00 mV), Addr 3: Full Scale Voltage Adjust Register (700 mV), Addr D: Extended Clock Phase Adjust Fine Register, Addr E: Extended Clock Phase Adjust Coarse Register (0.00 ps), and Addr F: Test Pattern Register (TP). Buttons for 'Reset FPGA', 'Calibrate ADC', and 'Reset Registers' are at the bottom.

The following section describes the Function of the pull-down selection tabs in the left hand side of the ADC08x3000RB product Control Panel

Temp Sensor

Displayed below the Channel Selection tab is the die temperature of both the FPGA and the ADC.

Hardware/Serial Control

Hardware Pin Control – The ADC is controlled by the logic states on the dedicated control pins. The logic on these pins is determined by the setting of **OUTV**, **OUTEDGE**, **DDR**, **FSR** and **RCLK** below.

Serial Register Program – The ADCs registers are accessed through the Extended Control Mode. In this mode the hardware pin control is disabled and the programmable registers are available for fine tuning.

NOTE: The Following Pull-down Tabs are available only when Hardware Pin Control is selected.

Out V

Low Amplitude – LVDS output voltage amplitude is set to 510mV pk-pk.

High Amplitude – LVDS output voltage amplitude is set to 710mV pk-pk.

OutEdge

Falling Edge – Data outputs are changed on the falling edge of DCLK+ (Single Data rate mode only).

Rising Edge – Data outputs are changed on the rising edge of DCLK+ (Single Data rate mode only).

DDR

Disable Dual Data Rate – DDR Mode is disabled (data output follows OutEdge Setting).

Enable Dual Data Rate – Data is output with rising and falling edge of DCLK (**Default for 1.5GHz clock**).

FSR

600mV Full Scale – Sets the full scale range to 600mV pk-pk.

800mV Full Scale – Sets the full scale range to 800mV pk-pk.

NOTE: The Following Pull-down Tabs are available regardless of Hardware/Serial Control setting.

RCLK

0 – TBD **2** – TBD

1 – TBD **4** – TBD

Standby

Disable Standby – Enable all on-board power regulators.

Enable Standby – Board is put into standby mode – All power is shutdown except USB power.

PD

Disable Shutdown – The ADC is powered up and Active.

Enable Shutdown – The ADC is put into low power mode. Register Settings are retained.

DC_Coup

AC Coupling – The single-ended analog input is AC coupled to the ADCs input

DC Coupling – The single-ended analog input is DC coupled to the ADCs input (not available on AC only model)

Ext Clock

Internal Clock – The ADC is clocked using the on-board 1.5GHz clock

External Clock – The ADC is clocked from an External clock source connected to the “CLOCK” input.

Diff In

Differential Data – The ADC is connected to the differential analog inputs.

Single Ended Data – The ADC is connected to the single-ended analog input.

Reset FPGA

This button resets the FPGA, and also returns all the pulldown tabs to their default values.

Calibrate ADC

This button issues an on-command calibration to the ADC by toggling the ADCs calibrate pin.

9.3 Serial Control Mode

When the Hardware/Serial Control tab is selected as “Serial Register Program”, the control panel display will be changed to the following view.

The screenshot shows the ADC083000 control panel. The title bar reads "ADC083000". The interface is divided into two main sections: "Control" on the left and "Registers" on the right.

Control Section:

- Hardware/Serial: **Serial Register Program** (selected in a dropdown menu)
- OutV: **Low Amplitude** (dropdown)
- OutEdge: **Rising Edge** (dropdown)
- DDR: **Enable Dual Data Rate** (dropdown)
- FSR: **600mv Full Scale** (dropdown)
- Standby: **Active** (dropdown)
- PD: **Disable Shutdown** (dropdown)
- DC_Coup: **AC Coupling** (dropdown)
- Ext Clock: **Internal Clock** (dropdown)
- Diff In: **Differential Data** (dropdown)
- Buttons: **Reset FPGA** and **Calibrate ADC**

Registers Section:

- Addr 1: Configuration Register**

1	0	0	1	0	0	1	0	1
DRE	RTD	DCS	DCP	nDE	OV	OE		
- Addr 2: Offset Register**

0	0	0	0	0	0	0	0	0
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit09	Bit08	Sign

0.00 mV
- Addr 3: Full Scale Voltage Adjust Register**

1	0	0	0	0	0	0	0	0
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit09	Bit08	Bit07

700 mV
- Addr D: Extended Clock Phase Adjust Fine Register**

0	0	0	0	0	0	0	0	0
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit09	Bit08	Bit07
- Addr E: Extended Clock Phase Adjust Coarse Register**

0	0	0	0	0	1	1	1	1
ENA	CAM3	CAM2	CAM1	CAM0				

0.00 ps
- Addr F: Test Pattern Register**

1	1	1	1	0	1	1	1	1
				TP				

Reset Registers

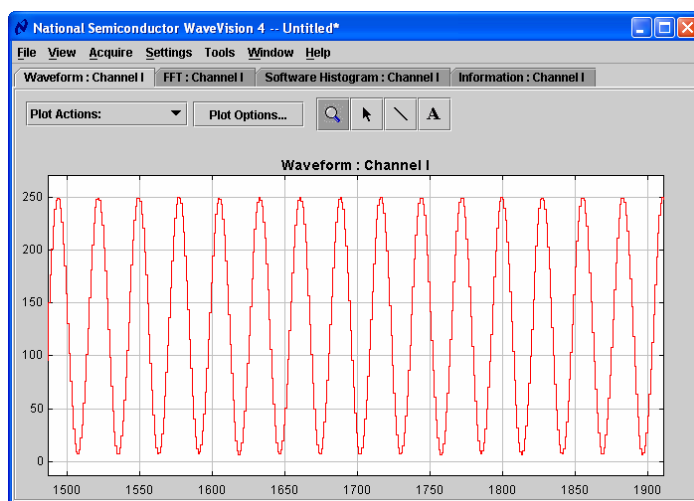
In this mode the register settings can be changed simply by clicking on the bits. Doing so will toggle the bit value and any linear values such as Full Scale Range or Offset will automatically be updated.

The “Reset Registers” button at the bottom of the Control Panel will reset and write all the values to the power-on default settings.

Please refer to the ADC083000/ADC08B3000 datasheets for a full description of the ADCs internal registers.

9.4 Capturing Waveforms

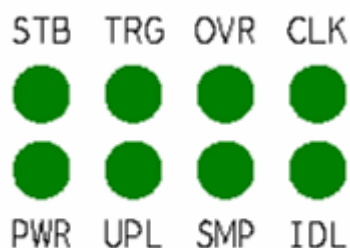
When the ADC has been configured as required, the selected input(s) can be sampled by clicking the “Acquire” pull-down menu and selecting “Samples”. Alternatively press F1 then the Escape key.



10.0 Appendix A - Hardware Information

10.1 LED functions

The function of the LEDs on the board is as follows



STB – STANDBY, illuminates when the board is in standby mode.

TRG – TRIGGER EVENT, illuminates when the Trigger Input makes low to high transition

OVR – ADC OVER RANGE, illuminates when the data input exceeds the full scale range of the ADC

- ADC083000: The LED will dynamically follow the change in the input magnitude
- ADC08B3000: The LED will latch the last magnitude from the last capture buffer write. It will only change state during a capture buffer write.

CLK – SAMPLE CLOCK INPUT

- ADC083000: The LED will flash with 50% duty cycle if the ADC is receiving a good clock input.
- ADC08B3000: The LED will stay illuminated if the sample frequency was input by the user.

PWR – POWER, illuminates when the external 12V is connected and the system is not in Standby.

UPL – UPLOAD, illuminates when the FPGA is uploading sample data to the PC

SMP – SAMPLE, illuminates when the FPGA is sampling data and storing to the FIFO buffers

IDL – IDLE, illuminates when the system is IDLE.

10.2 Expansion Header

A 72 pin Future Bus Expansion Header is provided on the rear panel to allow easy connection to a third party microprocessor board to allow for the reading and analysis of the data captured by the FPGA.

The signals connector to this expansion bus will be as follows

PIN	DESCRIPTION	PIN	DESCRIPTION
P1-A1	I2C - SDA	P1-B1	ADC DCLK RESET N
P1-A2	I2C - SCL	P1-B2	ADC DCLK RESET P
P1-A3	SSP - SERIAL DATA	P1-B3	GROUND
P1-A4	SSP - SERIAL CLOCK	P1-B4	GROUND
P1-A5	FPGA RESET	P1-B5	GROUND
P1-A6	READ FIFO	P1-B6	GROUND
P2-A1	WRITE FIFO	P2-B1	ADC EMPTY FLAG
P2-A2	FIFO FULL	P2-B2	ADC FULL FLAG
P2-A3	FIFO EMPTY	P2-B3	ADC WRITE SYNC
P2-A4	ADC DCLK RESET	P2-B4	ADC WRITE ENABLE
P2-A5	FPGA CONF DONE	P2-B5	ADC READ ENABLE
P2-A6	FPGA JTAG – TMS	P2-B6	GROUND
P3-A1	FPGA JTAG - TCK	P3-B1	GROUND
P3-A2	FPGA JTAG – TDI	P3-B2	GROUND
P3-A3	FPGA JTAG – TDO	P3-B3	GROUND
P3-A4	notSHUTDOWN	P3-B4	GROUND
P3-A5	3.3V SUPPLY	P3-B5	GROUND
P3-A6	12V SUPPLY	P3-B6	GROUND
P1-C1	DATA BUS A P0 (LVDS or CMOS)	P1-D1	DATA BUS A N0 (LVDS or CMOS)
P1-C2	DATA BUS A P1 (LVDS or CMOS)	P1-D2	DATA BUS A N1 (LVDS or CMOS)
P1-C3	DATA BUS A P2 (LVDS or CMOS)	P1-D3	DATA BUS A N2 (LVDS or CMOS)
P1-C4	DATA BUS A P3 (LVDS or CMOS)	P1-D4	DATA BUS A N3 (LVDS or CMOS)
P1-C5	DATA BUS A P4 (LVDS or CMOS)	P1-D5	DATA BUS A N4 (LVDS or CMOS)
P1-C6	DATA BUS A P5 (LVDS or CMOS)	P1-D6	DATA BUS A N5 (LVDS or CMOS)
P2-C1	DATA BUS A P6 (LVDS or CMOS)	P2-D1	DATA BUS A N6 (LVDS or CMOS)
P2-C2	DATA BUS A P7 (LVDS or CMOS)	P2-D2	DATA BUS A N7 (LVDS or CMOS)
P2-C3	INPUT STROBE P	P2-D3	INPUT STROBE N
P2-C4	DATA BUS B P0 (LVDS or CMOS)	P2-D4	DATA BUS B N0 (LVDS or CMOS)
P2-C5	DATA BUS B P1 (LVDS or CMOS)	P2-D5	DATA BUS B N1 (LVDS or CMOS)
P2-C6	DATA BUS B P2 (LVDS or CMOS)	P2-D6	DATA BUS B N2 (LVDS or CMOS)
P3-C1	DATA BUS B P3 (LVDS or CMOS)	P3-D1	DATA BUS B N3 (LVDS or CMOS)
P3-C2	DATA BUS B P4 (LVDS or CMOS)	P3-D2	DATA BUS B N4 (LVDS or CMOS)
P3-C3	DATA BUS B P5 (LVDS or CMOS)	P3-D3	DATA BUS B N5 (LVDS or CMOS)
P3-C4	DATA BUS B P6 (LVDS or CMOS)	P3-D4	DATA BUS B N6 (LVDS or CMOS)
P3-C5	DATA BUS B P7 (LVDS or CMOS)	P3-D5	DATA BUS B N7 (LVDS or CMOS)
P3-C6	OUTPUT STROBE P	P3-D6	OUTPUT STROBE N

The Data busses on this header can be configured as follows

- Two 8 bit busses with LVDS differential signaling, plus two LVDS strobes
- Four 8 bit busses with LVCMOS (3.3V IO) signaling plus four CMOS strobes

All control signals on pins (P1-A1 to P3-A6) and (P2-B1 to P2-B5) will be at LVCMOS 3.3V levels. P1-B1 and P1-B2 are LVDS differential signaling.

11.0 Appendix B - Installing and running the Wavevision 4 software

11.1 Install the WaveVision Software.

- Insert the WaveVision CD-ROM into your computer's CD-ROM drive.
- The WaveVision software requires a Java™ Runtime Environment or Java™ Development Kit, version 1.4 or higher, from Sun Microsystems, Inc. For detailed information on WaveVision's use of Java technology, please see below. If your computer does not have this software, the WaveVision installer will instruct you on how to install it.
- Locate and run the **WaveVision 4 Setup.exe** program on the CD-ROM. Follow the on-screen instructions to finish the install.

11.2 Java™ Technology

The WaveVision software uses Sun Microsystems® Java technology. The underlying Java software must be installed on your computer in order for the WaveVision software to run. The software can run on top of either the Java Runtime Environment (JRE) or the Java Development Kit (JDK), version 1.4 or higher. A suitable copy of the JRE is included on your WaveVision CD-ROM.

The WaveVision installer will first look for an existing copy of the JRE or JDK on your computer. If neither is found, the installer will instruct you to first install a JRE. To do this, run the **J2RE*.exe** installer program off the CD-ROM. Follow the on-screen instructions to finish the install.

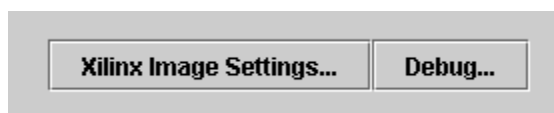
After a suitable JRE or JDK is installed, run the WaveVision installer again. The installer will detect the Java software and configure the WaveVision software to use it.

Java technology can allow software to run on different platforms. However, the WaveVision software contains Windows specific hardware interface code and therefore is only currently supported under Windows.

11.3 Automatic Device Detection & Configuration

The WaveVision system provides automatic hardware detection and configuration for the device under test. The FPGA is re-programmed on the fly by the host PC when the Development board is turned on.

Normally, the configuration process is totally transparent to the user, and requires no intervention. However, this process can be overridden if required by specifying a new Xilinx configuration image by clicking the Xilinx Image Settings button within the Capture Setting window (Settings -> Capture Settings).



11.4 Windows Driver

The WaveVision software communicates with the WaveVision hardware through the Windows device driver software. If you are unable to connect to the Wavevision board after installing the software, do the following to uninstall and reinstall the driver. Go to the Windows Control Panel and select System. If you are using Windows 2000/XP select the Hardware tab. Then click on Device Manager and go down to the Universal Serial Bus controllers. With the WaveVision board connected, you will see it (or an unknown device) listed. Right click on it and uninstall the driver. Then unplug and plug in the board again to reinstall the driver.

12.0 Appendix C - Using WaveVision Plots

The WaveVision software provides several tools to help you interact with plots. A toolbar appears above each plot, similar to Figure 4.

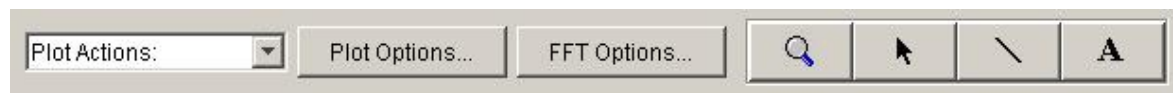


Figure 4: WaveVision Plot Tools

Seen from left to right, the following tools are available:

Plot Actions menu: This menu contains commands that pertain to this particular plot. You may export the plot data to a file, print the plot, save it as a graphic, or change the plot's colors.

Plot Options: This button opens a dialog box with options that pertain to this particular plot. You may turn off labels, annotations, or other elements in this dialog. The WaveVision software maintains default options for new plots. You may edit the default options by choosing **Default Plot Options** from the **Settings** menu.

FFT Options: The toolbar shown in Figure 4 is from an FFT plot, and thus contains a button to edit the options for the FFT calculation. Depending upon the type of plot, various options may be present on the toolbar. Please consult the appropriate section below for more information about these options.

Magnifying glass tool: This tool allows you to zoom in and out to see fine details in the plot. Click and drag a box from upper-left to lower-right to zoom in on a particular region of your plot. Click and drag a box from lower-right to upper-left to zoom out. **With the magnifying glass tool selected, click the right mouse button to return to a normal, 100% view.**

Arrow Tool: The arrow tool is used to select, move, and edit annotations. To edit an annotation, double click it with the arrow tool. To delete an annotation, select it with the arrow tool and press the **Delete** key on your keyboard.

Line Annotation Tool: To draw lines on the plot, select this tool. Drag to draw new lines. To add arrowheads or fix the endpoints of the line, double-click it with the arrow tool.

Text Annotation Tool: To draw labels on the plot, select this tool and click at the desired location in the plot. To edit the justification, location, or text of an annotation, double-click it with the arrow tool.

The Waveform Plot

The Waveform plot shows you the raw samples collected from the hardware. This plot is mainly used to verify the integrity of collected data – the waveform is the best view in which to diagnose a distorted signal, an irregular clock, a low-amplitude signal, and many other common ADC system problems.

The Waveform plot also quickly shows you how much of the ADC's dynamic range your signal occupies.

The FFT Plot

The WaveVision software automatically computes a Fast Fourier Transform (FFT) of the sample set, and displays the results in an FFT plot. The FFT plot is, in many respects, the heart of the software. The FFT shows you the frequency content of your input signal. It marks the fundamental frequency, and a selectable number of harmonics. It also labels their order and frequencies. It shows the power in the fundamental and harmonics. Try hovering your mouse cursor over a harmonic to get information about it.

The FFT can be used to diagnose common ADC problems such as input spectral impurity, clock phase noise, and clock jitter. The FFT plot also shows several statistics on the quality and purity of the collected

samples, such as SNR, SINAD, THD, SFDR, and ENOB. These statistics are to be interpreted with the following definitions (which are repeated in every National Semiconductor ADC datasheet):

Signal to Noise Ratio (SNR) is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

Signal to Noise Plus Distortion (S/N+D or SINAD) Is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all of the other spectral components below half the clock frequency, including harmonics but excluding DC.

Total Harmonic Distortion (THD) is the ratio, expressed in dBc, of the RMS total of the first five harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$\text{THD} = 20 \log \sqrt{\frac{f_2^2 + \dots + f_N^2}{f_1^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_N are the RMS power in the first N harmonic frequencies.

Spurious-Free Dynamic Range (SFDR) is the difference, expressed in dB, between the RMS values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

Effective Number of Bits (ENOB, or Effective Bits) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as $(\text{SINAD} - 1.76) / 6.02$ and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FFT Options

FFT plots can be configured in many different ways. Clicking the “FFT Options” button at the top of the plot will display a dialog showing the options for that particular plot. The software also maintains default options for new FFT plots, which are editable. You can edit the default FFT options by choosing **Default FFT Options** from the **Settings** menu. The options are:

Windowing: You may choose from one of five different window functions. The window function is applied to the samples before computing the FFT to compensate for the fact that the sample set may not be an integral number of wavelengths of the input signal. In general, Flat-Top will give the best results, but you may find it easier to compare data with other systems when the windowing functions are the same.

dB Scale: You may select to represent power on the FFT in dBc (decibels relative to carrier), in which 0 dB is taken to be the fundamental (carrier) power, or dBFS (decibels relative to full-scale), in which 0 dB is taken to be the power contained in a signal which uses the entire dynamic range of the ADC.

Harmonics: You may select the number of harmonics recognized (and labeled) by the software. You may also select the number of FFT bins excluded around harmonics in, for example, SNR calculations. The exclusion region around each harmonic will be shown in a different color than the rest of the data points.

IMD Calculations: The WaveVision software is capable of performing Intermodulation Distortion calculations. When two fundamental frequencies within 3 dBFS are present in the waveform, The software will normally perform IMD calculations. You may inhibit this behavior by deselecting the “Allow IMD calculation” checkbox. When IMD calculation is enabled, you may also select whether the software will include only 2nd order or both 2nd and 3rd order terms.

Histogram Plots

Histogram plots are created by counting the number of times each ADC output code appears in a dataset. Histograms may be computed by software. A software histogram is computed from a dataset which is normally 128k samples or smaller. The resulting histogram will show discontinuities between comparators, gain or offset errors, and other common ADC system problems.

The Histogram plot also displays the number of codes that were never counted (missing codes), followed by the first ten such missing codes.

Information Viewer

The information viewer is not a plot, but it displays a variety of useful information about the dataset, such as the sampling rate, and any warnings generated by the software. You may also store comments about the dataset here, to be saved in a WaveVision file.

Data Import and Export

The WaveVision software provides a variety of means to share data with others, in both textual and graphical formats.

The most flexible way to import data into the software is from a tab-delimited ASCII text file. The contents can be either a sample set or a histogram, provided with or without time information. The simplest example of this would be a file with a single column of samples. You can open tab-delimited text files by choosing **Open** from the **File** menu; you can interleave data from multiple columns and/or files. You can choose **ReOpen** to reopen the same file later with the same settings (for example when you update the file with new data),

There are a variety of ways to export data from the software:

- Save the file as a normal WV4 (*.wv4) file. WV4 files are ASCII, tab-delimited text files. Samples are stored one per line in a single column. You can open a WV4 file directly in a spreadsheet program.
- Save the file as a TXT (*.txt) file. You will produce a one- or two-column tab-delimited ASCII text file of samples or histogram information, without the header information that is contained in a WV4 file.
- You can export the contents of an individual plot by choosing **Export Data...** from the plot's **Plot Actions** menu. The format of the data is always tab-delimited ASCII text.
- You can export a plot as either a GIF (*.gif) or Encapsulated Postscript (*.eps) graphic by choosing **Export Plot as Graphic** from the plot's **Plot Actions** menu. GIF files are suitable for the web or for emails. Encapsulated Postscript files are high-resolution scalable files suitable for direct publication.

13.0 Appendix D – Developing Application Specific FPGA code

National Semiconductor offers the FPGA source code as a starting point for the development of application specific FPGA Code. However, National cannot support modified FPGA code. Any difficulties, errors or 'bugs' that result due to modifications to the original source code are the sole responsibility of the end user.

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