

# BIG3GIG EVALUATION BOARD

ADC083000RB, ADC08B3000RB

## MANUFACTURING KIT / REFERENCE DESIGN

National Semiconductor 3 GHz, 8-bit ADC + XILINX Virtex 4

### SPECIAL NOTES

The information contained herein might not reflect the exact configuration of the board provided.

National Semiconductor reserves the right to make changes to this product.

ALL parts labeled "NA" are NOT ASSEMBLED.


This schematic revision 2.3 is component value changes to hardware REV 2.2.

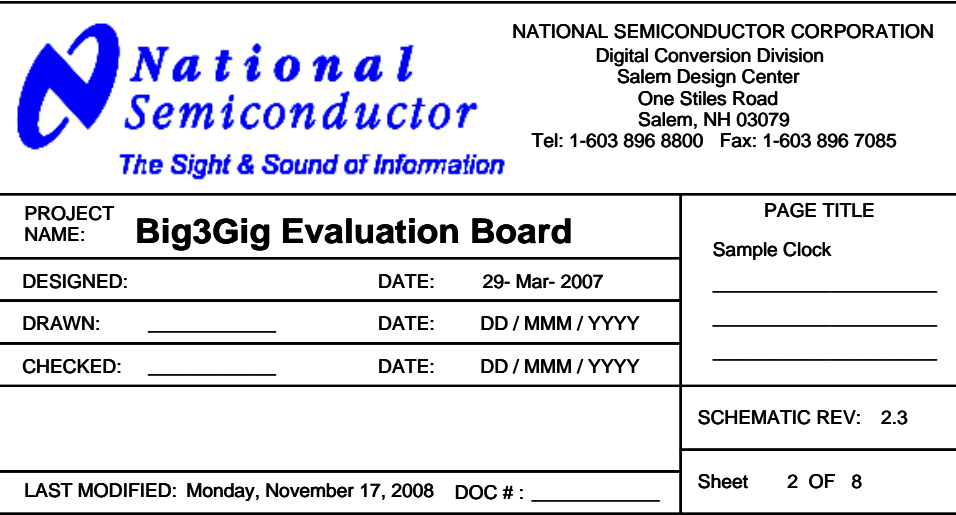
Print Instructions:

- To create a readable printout, we recommend the use A3 or 11x17" paper size.
- When printing from this PDF file, make sure to check the "Shrink to fit" box.

### SYSTEM CONFIGURATION

Module	Configuration	Description
FRONT END	1 channel DIFF. / SINGLE ENDED	AC AND DC COUPLING OF SIGNAL PATH
CLOCK SOURCE	SINGLE ENDED	LMX2531LQ1500E
FPGA		XC4VLX15-10SFG363C - 363 PIN BGA
USB I/F		CY7C68013A EZ USB

		NATIONAL SEMICONDUCTOR CORPORATION Digital Conversion Division Salem Design Center One Stiles Road Salem, NH 03079 Tel: 1-603 896 8800 Fax: 1-603 896 7085	
PROJECT NAME: <b>Big3Gig Evaluation Board</b>			
DESIGNED:	DATE: 29 Mar 2007	LAYOUT JOB#: _____	
DRAWN: _____	DATE: DD / MMM / YYYY	LAYOUT REV: _____	
CHECKED: _____	DATE: DD / MMM / YYYY	ASSEMBLY REV: _____	
		SCHEMATIC REV: 2.4	
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Signal source should have a 50-Ohm RESISTANCE to ground. If it has an AC IMPEDANCE, a 50-Ohm terminator should be used at J2 when using the DC coupled mode to avoid excessive signal offset.

SINGLE\_ENDED\_IN

P4 VCMO  
VCMO is grounded through relay U4 when AC coupling is selected.

J10 DIFF\_IN\_P  
sma-3

J9 DIFF\_IN\_N  
sma-3

P5,7,8 1V8IO

P5,6,7,8 3V3IO

P2,6 5VRLY

P5 DIFF\_SELECT

P5 DC\_SELECT

TRIGGER INPUT HAS NO FUNCTIONALITY AS BOARD IS PROVIDED.

J4 TRIGGER\_IN

SMA

U8

74LVC1G17

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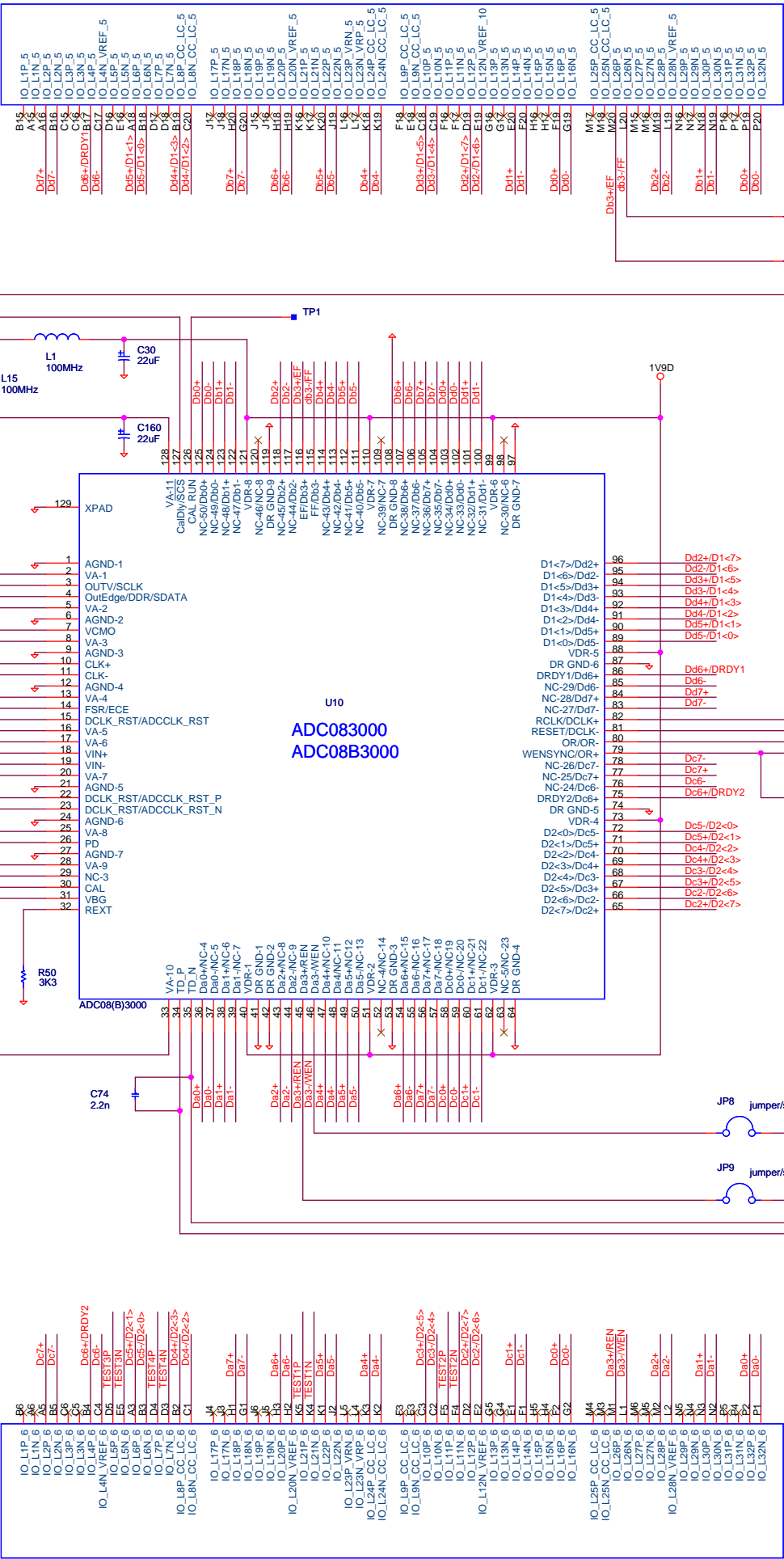
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U9D XC4VLX15\_363FBGA

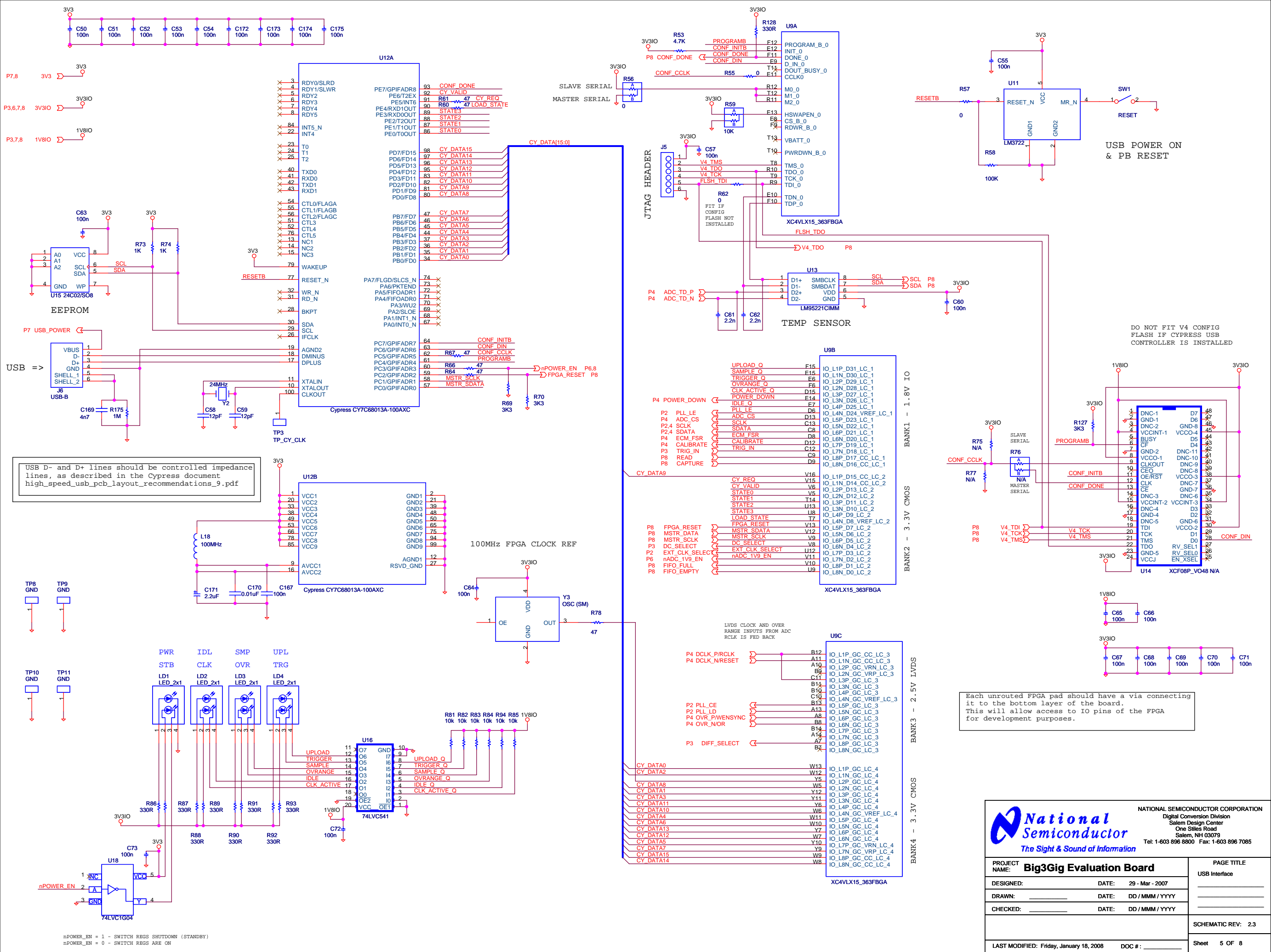


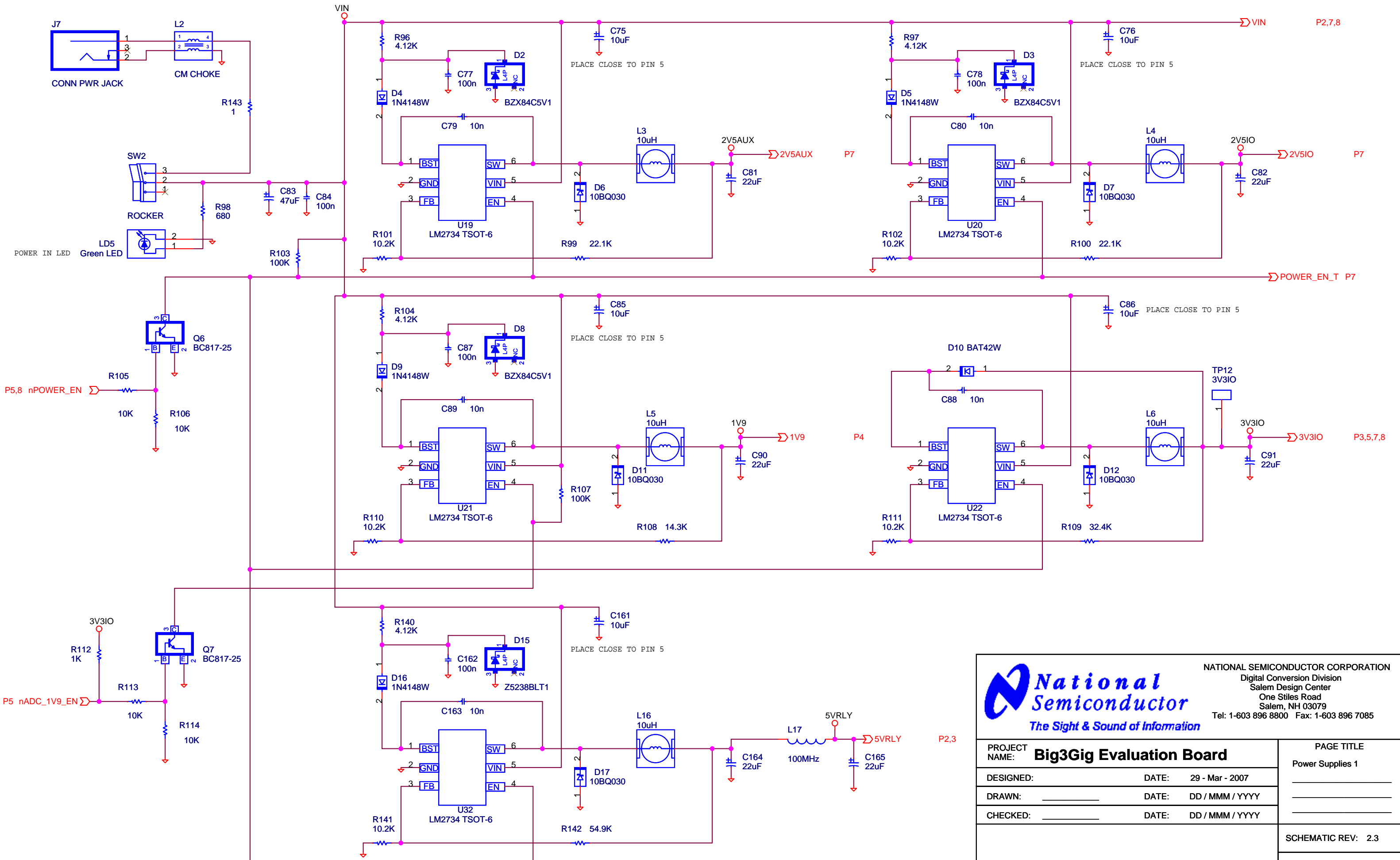



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PROJECT NAME: <b>Big3Gig Evaluation Board</b>		PAGE TITLE ADC08x3000 + Virtex 4
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