SWITCHING POWER SUPPLY DESIGN:
PWM CURRENT MODE DUAL SYNCHRONOUS BUCK CONVERTER:
LM5642

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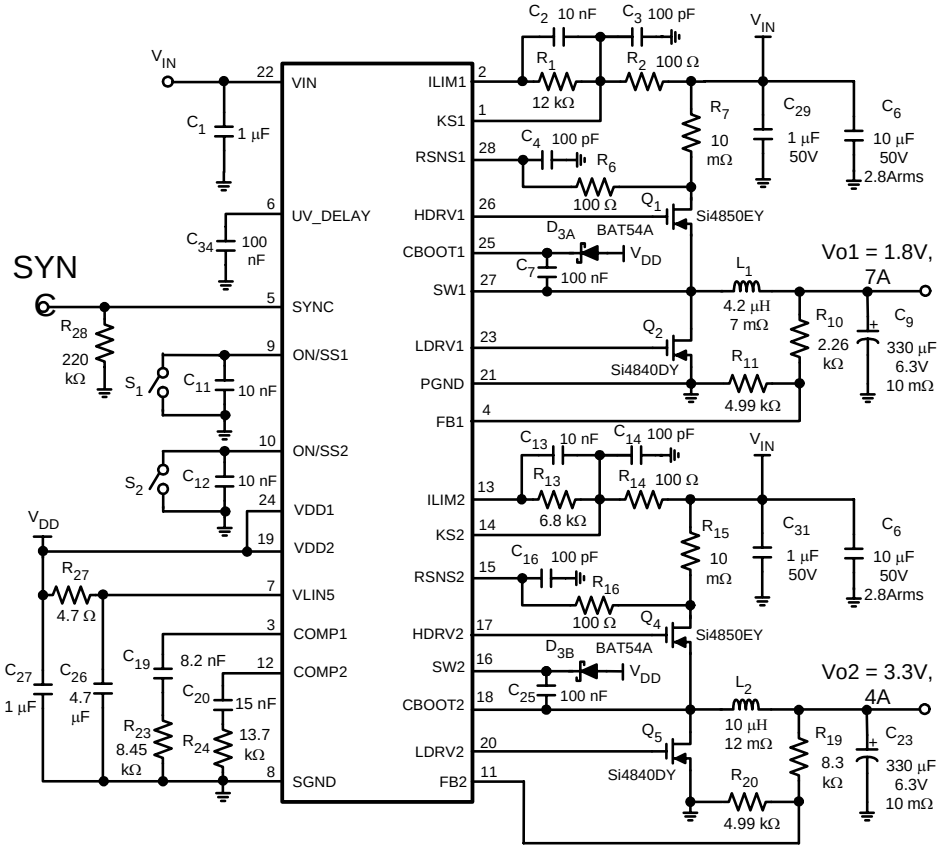


Notes:

Write down the power supply requirements in the following boxes : $X_{xx} :=$

Get the results from the following boxes: $Rsults_{xx} :=$

This Mathcad file helps with the calculation of the external components of a typical dual synchronous buck converter with the LM5642 controller:

1) Power supply specifications:

Input voltage:

- Minimum input voltage: $Vi_{min} := 10 \cdot volt$

- Maximum input voltage: $Vi_{max} := 30 \cdot volt$

- Nominal input voltage: $Vi_{nom} := 24 \cdot volt$

Output:

- Nominal output voltage, maximum output ripple, minimum output current, maximum output current

$Vo1 := 1.8 \cdot volt$ $Vrp1 := 100 \cdot mV$ $Io1_{min} := 0.200 \cdot amp$ $Io1_{max} := 7 \cdot amp$

$Vo2 := 3.3 \cdot volt$ $Vrp2 := 200 \cdot mV$ $Io2_{min} := 0.200 \cdot amp$ $Io2_{max} := 4 \cdot amp$

$Po_{min} := Vo1 \cdot Io1_{min} + Vo2 \cdot Io2_{min}$ $Po_{min} = 1.02\,watt$

$Po_{max} := Vo1 \cdot Io1_{max} + Vo2 \cdot Io2_{max}$ $Po_{max} = 25.8\,watt$

- Switching Frequency: $fsw := 200 \cdot kHz$

$T := \frac{1}{fsw}$ $T = 5\,\mu sec$

The switching frequency can be synchronised to an external clock between 150kHz and 250kHz

2) Maximum and minimum duty cycle : Dmax and Dmin

$D1_{max} := \frac{Vo1}{Vi_{min}}$ $D2_{max} := \frac{Vo2}{Vi_{min}}$

Maximum duty cycle

$D1_{max} = 0.18$ $D2_{max} = 0.33$

$D1_{min} := \frac{Vo1}{Vi_{max}}$ $D2_{min} := \frac{Vo2}{Vi_{max}}$

Minimum duty cycle

$D1_{min} = 0.06$ $D2_{min} = 0.11$

$D1_{nom} := \frac{Vo1}{Vi_{nom}}$ $D2_{nom} := \frac{Vo2}{Vi_{nom}}$

Nominal duty cycle

$D1_{nom} = 0.075$ $D2_{nom} = 0.137$

$Ton1_{min} := D1_{min} \cdot T$ $Ton1_{min} = 0.3\,\mu sec$

Minimum ON time

$Ton2_{min} := D2_{min} \cdot T$ $Ton2_{min} = 0.55\,\mu sec$

To insure the output regulation the maximum duty cycle has to be lower than **0.96**, and the minimum on-time greater than **166nsec**.

3) Select output filter: L/C Inductors and output capacitors

Output capacitors and output inductors are usually selected in order to meet voltage transient requirements during worst case load transients, maximum AC ripple current, and output ripple

voltage. The selection of the best optimised L-C filter is usually achieved with few design iterations, as compromises are made between the cost/size of inductors and capacitors that meet the output requirements.

-Allowed transient voltage excursion: ΔVcs

$\delta\% := 7\%$ (Maximum output voltage regulation window)

$\lambda\% := 1.5\%$ (Output voltage initial accuracy)

$\Delta Vcs1 := (\delta\% - \lambda\%) \cdot Vo1 - \frac{Vrp1}{2}$ $\Delta Vcs1 = 0.049V$

$\Delta Vcs2 := (\delta\% - \lambda\%) \cdot Vo2 - \frac{Vrp2}{2}$ $\Delta Vcs2 = 0.082V$

-Maximum load current change during load transient: ΔIcs

$\Delta Ics1 := Io1_{max} - Io1_{min}$ $\Delta Ics1 = 6.8A$

$\Delta Ics2 := Io2_{max} - Io2_{min}$ $\Delta Ics2 = 3.8A$

-Maximum total ESR capacitor value: ESRmax

Assumes that the rise and fall times of a load transient are faster then the response speed of the control loop.

$ESR1_{max} := \frac{\Delta Vcs1}{\Delta Ics1}$ $ESR1_{max} = 7.206 \times 10^{-3} \Omega$

$ESR2_{max} := \frac{\Delta Vcs2}{\Delta Ics2}$ $ESR2_{max} = 0.021\Omega$

Select output capacitors that have ESR value < than ESRmax:

$ESR1 := 0.005\Omega$ $ESR2 := 0.010\Omega$

-Minimum inductor selection:

$L1_{min} := (Vi_{nom} - Vo1) \cdot T \cdot D1_{nom} \cdot \frac{ESR1}{Vrp1}$ $L1_{min} = 0.416\mu H$

$L2_{min} := (Vi_{nom} - Vo2) \cdot T \cdot D2_{nom} \cdot \frac{ESR2}{Vrp2}$ $L2_{min} = 0.712\mu H$

L(min) is the minimum inductance needed to meet the output ripple specification.The actual inductor value selected is a compromise between cost, size, maximum inductor losses and maximum AC ripple current allowed on the inductor:
AC core losses. and AC winding losses are directly proportional to the current ramp on the inductor, and the switching frequency. In high current applications, a good compromise is achieved with a maximum ripple current between 30-50% of the nominal output current.

- Desired secondary ripple current: $\Delta Is\% := 40 \cdot \%$

$L1_b := \frac{Vi_{nom} - Vo1}{\Delta Is\% \cdot Io1_{max}} \cdot T \cdot D1_{nom}$ $L1_b = 2.973\mu H$

$L2_b := \frac{Vi_{nom} - Vo2}{\Delta Is\% \cdot Io2_{max}} \cdot T \cdot D2_{nom}$ $L2_b = 8.895\mu H$

Select Inductor value >= Lmin and Lb

L1 selected----> $L1_{us} := 4.2 \cdot \mu H$ $RL1 := 0.004\Omega$

L2 selected ----> $L2_{us} := 10 \cdot \mu H$ $RL2 := 0.004 \Omega$

-Minimum output capacitance value: Comin

The minimum capacitance of the output capacitors bank needed to meet voltage transient requirements during worst case load transients is:

$$Co1_{min} := \frac{L1_{us} \cdot \left[\Delta Vcs1 - \sqrt{\left[\Delta Vcs1^2 - \left(\Delta Ics1 \cdot ESR1 \right)^2 \right]} \right]}{Vo1 \cdot ESR1^2} \qquad Co1_{min} = 1.28 \times 10^3 \, \mu F$$

$$Co2_{min} := \frac{L2_{us} \cdot \left[\Delta Vcs2 - \sqrt{\left[\Delta Vcs2^2 - \left(\Delta Ics2 \cdot ESR2 \right)^2 \right]} \right]}{Vo2 \cdot ESR2^2} \qquad Co2_{min} = 284.882 \mu F$$

C1 selected----> $C1_{us} := 330 \cdot 2 \cdot \mu F$ $ESR1 = 5 \times 10^{-3} \, \Omega$

C2 selected ----> $C2_{us} := 330 \cdot \mu F$ $ESR2 = 0.01 \Omega$

4) AC, peak inductor currents:

- Ramp amplitude: AC inductor current:

$$\Delta Io1 := \frac{\left(Vi_{nom} - Vo1 \right) \cdot D1_{nom} \cdot T}{L1_{us}} \qquad \Delta Io1 = 1.982 amp$$

$$\Delta Io2 := \frac{\left(Vi_{nom} - Vo2 \right) \cdot D2_{nom} \cdot T}{L2_{us}} \qquad \Delta Io2 = 1.423 amp$$

- Peak current:

$$Io1_{peak} := Io1_{max} + \frac{\Delta Io1}{2} \qquad Io1_{peak} = 7.991 A$$

$$Io2_{peak} := Io2_{max} + \frac{\Delta Io2}{2} \qquad Io2_{peak} = 4.712 A$$

The buck converter will operate in continuous mode, and it will move in to discontinuous mode when the output load currents fall below Io(disc)

$$Io1_{disc} := \frac{Vi_{nom} - Vo1}{2 \cdot Vi_{nom}} \cdot \frac{Vo1}{L1_{us} \cdot fsw} \qquad Io1_{disc} = 0.991 A$$

$$Io2_{disc} := \frac{Vi_{nom} - Vo2}{2 \cdot Vi_{nom}} \cdot \frac{Vo2}{L2_{us} \cdot fsw} \qquad Io2_{disc} = 0.712 A$$

- Output capacitor bank rms current:

$$ICo1_{rms} := \frac{\left(1 - D1_{nom} \right) \cdot Vo1}{\sqrt{12} \cdot L1_{us} \cdot fsw} \qquad ICo1_{rms} = 0.572 A$$

$$ICo2_{rms} := \frac{\left(1 - D2_{nom} \right) \cdot Vo2}{\sqrt{12} \cdot L2_{us} \cdot fsw} \qquad ICo2_{rms} = 0.411 A$$

Select capacitors with maximum RMS current >>> $ICo1_{rms}$ and $ICo2_{rms}$

5) Select input capacitors:

$D1_{max} = 0.18$ $D2_{max} = 0.33$

If there is not overlap between the two channels, (Dmax<50%), the input capacitor RMS ripple current is:

$A1 := Io1_{max}^{2} \cdot D1_{nom} \cdot (1 - D1_{nom})$ $A2 := Io2_{max}^{2} \cdot D2_{nom} \cdot (1 - D2_{nom})$

$A3 := 2 \cdot Io2_{max} \cdot D2_{nom} \cdot Io1_{max} \cdot D1_{nom}$

$ICia_{rms} := \sqrt{A1 + A2 - A3}$ $ICia_{rms} = 2.172A$

If there is overlap between the two channels, (Dmax>50%), the input capacitor RMS ripple current is:

$B1 := \left[Io1_{max} \cdot (1 - D1_{nom}) + Io2_{max} \cdot (1 - D2_{nom}) \right]^{2} \cdot (D1_{nom} + D2_{nom} - 1)$

$B2 := \left[Io1_{max} \cdot (1 - D1_{nom}) - Io2_{max} \cdot D2_{nom} \right]^{2} \cdot (1 - D2_{nom})$

$B3 := \left[Io2_{max} \cdot (1 - D2_{nom}) - Io1_{max} \cdot D1_{nom} \right]^{2} \cdot (1 - D1_{nom})$

$ICib_{rms} := \sqrt{B1 + B2 + B3}$ $ICib_{rms} = 6.275iA$

The Input capacitors should meet the minimum requirements of voltage and ripple current rating.

6) External switching MOSFETs: power losses, efficiency

- Internal Driver Specifications:

$Vdr := 5 \cdot volt$ $Rdr_{on} := 4\Omega$ $Rdr_{off} := 2 \cdot \Omega$

The goal in selecting a MOSFET is to minimise junction temperature rise by minimising the power loss while being cost effective. Besides maximum voltage rating, and maximum current rating, the other three important parameters of a MOSFET are Rds(on), gate threshold voltage, and gate capacitance.
The switching MOSFET has three types of losses which are, conduction loss, switching loss, and gate charge losses.
-**Conduction losses** are: I^2*R losses, therefore the total resistance between the source and drain during the on state, Rds(on) has to be as low as possible.
- **The switching loss equation is**: Switching-time*Vds*I*frequency. The switching time, rise time and fall time are a function of: a) The gate to drain Miller-charge of the MOSFET, Qgd, b) The internal resistance of the driver and c) The Threshold Voltage, Vgs(th) which is the minimum gate voltage which enables the current through the drain and source of the MOSFET.
-Gate charge losses are caused by charging up the gate capacitance and then dumping the charge to ground every cycle. The gate charge losses are equal to: frequency • Qg(tot) • Vdr
Unfortunately, the lowest on resistance devices tend to have higher gate capacitance.
Because this loss is frequency dependent, in very high current supplies with very large FETs, with large gate capacitance, a more optimal design may result from reducing the operating frequency.
Switching losses are also affected by gate capacitance. If the gate driver has to charge a larger capacitance, then the time the MOSFET spends in the linear region increases and the losses increase. The general rule is the faster the rise time, the lower the switching loss. Unfortunately this causes high frequency noise.

High Side MOSFET losses: Q1, Q4

Mosfets: Si4850EY Syliconix

$Rds1_{on} := 0.031 \cdot ohm$ $Rds4_{on} := 0.031 \cdot ohm$

(Total resistance between the source and drain during the on state)

$Coss1 := 70 \cdot pF$ $Coss4 := 70 \cdot pF$ (Output capacitance)

$Qg1_{tot} := 19 \cdot n \cdot coul$ $Qg4_{tot} := 19 \cdot n \cdot coul$ (Total gate charge)

$Qgd1 := 5.3 \cdot n \cdot coul$ $Qgd4 := 5.3 \cdot n \cdot coul$ (Gate drain Miller charge)

$Qgs1 := 3.4 \cdot n \cdot coul$ $Qgs4 := 3.4 \cdot n \cdot coul$ (Gate to source charge)

$Vgs1_{th} := 3 \cdot volt$ $Vgs4_{th} := 3 \cdot volt$ (Threshold voltage)

- Conduction losses: Pcond

$Pcond1 := Rds1_{on} \cdot Io1_{max}^{2} \cdot D1_{max}$ $Pcond1 = 0.273\,watt$

$Pcond4 := Rds4_{on} \cdot Io2_{max}^{2} \cdot D2_{max}$ $Pcond4 = 0.164\,watt$

- Switching losses: Psw(max): V*I/2*freq*(Tswon+Tswoff)

$Idriver1_{LH} := \frac{Vdr - Vgs1_{th}}{Rdr_{on}}$ $Idriver4_{LH} := \frac{Vdr - Vgs4_{th}}{Rdr_{on}}$ $Idriver1_{LH} = 0.5\,amp$

$Idriver1_{HL} := \frac{Vdr - Vgs1_{th}}{Rdr_{off}}$ $Idriver4_{HL} := \frac{Vdr - Vgs4_{th}}{Rdr_{off}}$ $Idriver1_{HL} = 1\,amp$

$Qg1_{sw} := Qgd1 + \frac{Qgs1}{2}$ $Qg4_{sw} := Qgd4 + \frac{Qgs4}{2}$ $Qg1_{sw} = 7\,C\,n$

$tsw1_{LH} := \frac{Qg1_{sw}}{Idriver1_{LH}}$ $tsw4_{LH} := \frac{Qg4_{sw}}{Idriver4_{LH}}$ $tsw1_{LH} = 14\,s\,n$

$tsw1_{HL} := \frac{Qg1_{sw}}{Idriver1_{HL}}$ $tsw4_{HL} := \frac{Qg4_{sw}}{Idriver4_{HL}}$ $tsw1_{HL} = 7\,s\,n$

$t1_{sw} := Qgd1 \cdot \frac{Rdr_{on}}{Vdr - Vgs1_{th}}$ $t4_{sw} := Qgd4 \cdot \frac{Rdr_{on}}{Vdr - Vgs4_{th}}$ $t1_{sw} = 10.6\,s\,n$

$Psw1_{max} := \frac{Vi_{hom} \cdot Io1_{max}}{2} \cdot fsw \cdot \left(tsw1_{LH} + tsw1_{HL}\right) + \frac{Coss1 \cdot Vi_{hom}^{2} \cdot fsw}{2}$ $Psw1_{max} = 0.357\,watt$

$Psw4_{max} := \frac{Vi_{hom} \cdot Io2_{max}}{2} \cdot fsw \cdot \left(tsw4_{LH} + tsw4_{HL}\right) + \frac{Coss4 \cdot Vi_{hom}^{2} \cdot fsw}{2}$ $Psw4_{max} = 0.206\,watt$

- Gate charge losses: Pgate

Average current required to drive the gate capacitor of the MOSFET:

$Igate1_{awg} := fsw \cdot Qg1_{tot}$ $Igate4_{awg} := fsw \cdot Qg4_{tot}$ $Igate1_{awg} = 3.8 \times 10^{-3}\,amp$

$Pgate1 := Igate1_{awg} \cdot Vd$ $Pgate4 := Igate4_{awg} \cdot Vd$ $Pgate1 = 0.019\,watt$

-Total Q1 & Q4 losses: Ptot(max)

$Pmosfet1_{tot} := Pcond1 + Psw1_{max} + Pgate1$ $Pmosfet1_{tot} = 0.649\,watt$

$Pmosfet4_{tot} := Pcond4 + Psw4_{max} + Pgate4$ $Pmosfet4_{tot} = 0.388\,watt$

-Maximum junction temperature and heat sink requirement:

Maximum junction temperature desired: $Tj_{max} := 175\,Celsius$

Maximum ambient temperature: $Ta_{max} := 70\,Celsius$

-Thermal resistance junction to ambient temperature:

$$\theta ja1 := \frac{Tj_{max} - Ta_{max}}{Pmosfet1_{tot}} \qquad \theta ja1 = 161.725 \frac{1}{watt} Celsius$$

$$\theta ja4 := \frac{Tj_{max} - Ta_{max}}{Pmosfet4_{tot}} \qquad \theta ja4 = 270.401 \frac{1}{watt} Celsius$$

Low Side MOSFET losses: Q2, Q5

The Low side losses are mainly the conduction losses of the MOSFET, plus the losses from the external diode (during the time that both MOSFETs are off)

MOSFET: Si4840DY Siliconix $Rds2_{on} := 0.012 \cdot ohm$ $Rds5_{on} := 0.012 \cdot ohm$

(Total resistance between the source and drain during the on state)

$Coss2 := 50 \cdot pF$ $Coss5 := 50 \cdot pF$ (Output capacitance)

$Qg2_{tot} := 28 \cdot n \cdot coul$ $Qg5_{tot} := 28 \cdot n \cdot coul$ (Total gate charge)

$Qgd2 := 7.5 \cdot n \cdot coul$ $Qgd5 := 7.5 \cdot n \cdot coul$ (Gate drain Miller charge)

$Qgs2 := 6 \cdot n \cdot coul$ $Qgs5 := 6 \cdot n \cdot coul$ (Gate to source charge)

$Vgs2_{th} := 3 \cdot volt$ $Vgs5_{th} := 3 \cdot volt$ (Threshold voltage)

- Conduction losses: Pcond

$Pcond2 := Rds2_{on} \cdot Io1_{max}^2 \cdot (1 - D1_{max})$ $Pcond2 = 0.482\,watt$

$Pcond5 := Rds5_{on} \cdot Io2_{max}^2 \cdot (1 - D2_{max})$ $Pcond5 = 0.129\,watt$

Switching losses are like before but Vin is just the voltage drop on the diode:

$t_{deadtime} := 30n \cdot sec$

Voltage drop on the diode: $Vf_{diode} := 0.6V$ (Or internal MOSFET body diode)

$Pdiode2 := t_{deadtime} \cdot fsw \cdot Vf_{diode} \cdot Io1_{ma}$ $Pdiode2 = 0.025W$

$Pdiode5 := t_{deadtime} \cdot fsw \cdot Vf_{diode} \cdot Io2_{ma}$ $Pdiode5 = 0.014W$

$Pmosfet2_{tot} := Pcond2 + Pdiode2$ $Pmosfet2_{tot} = 0.507watt$

$Pmosfet5_{tot} := Pcond5 + Pdiode5$ $Pmosfet5_{tot} = 0.143watt$

- Total MOSFET losses:

$Pmosfet_{tot} := Pmosfet1_{tot} + Pmosfet2_{tot} + Pmosfet4_{tot} + Pmosfet5_{tot}$ $Pmosfet_{tot} = 1.688W$

-Maximum efficiency:

$$\eta := \frac{Po_{max}}{Po_{max} + Pmosfet_{tot} + 0.002amp \cdot Vi_{max} + RL1 \cdot Io1_{max}^{2} + RL2 \cdot Io2_{max}^{2}}$$ $\eta = 0.928$

7) Current limit, current sensing:

In order to keep the current sense amplifier in the linear operation REGION, the maximum voltage drop voltage across the current sense resistor Rsns, or across the high side MOSFET is 200mV. The minimum should be 50mV. Therefore the Rsns resistor has to be < of:

$$Rsns1_{max} := \frac{200mV}{Io1_{peak}}$$ $Rsns1_{max} = 0.025\Omega$

$$Rsns2_{max} := \frac{200mV}{Io2_{peak}}$$ $Rsns2_{max} = 0.042\Omega$

-Select the current sense resistors, for each channel:

$Rsns1_{used} := 0.010\Omega$ $Rsns2_{used} := 0.010\Omega$

$Rsns1_{used} \cdot Io1_{peak} = 0.08V$

Rlimit set the maximum peak current limit:

$$Rlimit1 := \frac{Io1_{peak} \cdot Rsns1_{used}}{10\mu A}$$ $Rlimit1 = 7.991K\Omega$

$$Rlimit2 := \frac{Io2_{peak} \cdot Rsns2_{used}}{10\mu A}$$ $Rlimit2 = 4.712K\Omega$

- Select $Rlimit1_{us}$, $Rlimit2_{us}$ resistors >> than $Rlimit$

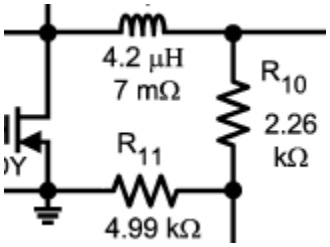
$Rlimit1_{us} := 12K\Omega$ $Rlimit2_{us} := 6.8K\Omega$

Maximum peak current limit:

$$\frac{Rlimit1_{us} \cdot 10\mu A}{Rsns1_{used}} = 12A$$

Has to be > than $Io1_{peak} = 7.991A$

$$\frac{Rlimit2_{us} \cdot 10\mu A}{Rsns2_{used}} = 6.8A$$



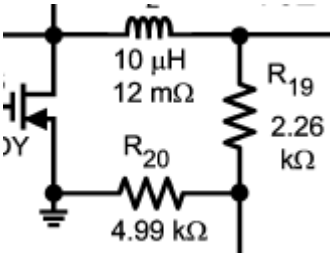
Has to be > than

$Io2_{peak} = 4.712A$

8) Output voltage setting:

$Vref_{fb} := 1.2364 volt$ $Ifb_{max} := 0.2 \cdot \mu A$

$R11_{max} := \frac{0.3\% \cdot Vo1}{Ifb_{max}}$ $R11_{max} = 27K\Omega$ ---> $R11_{us} := 4.99K\Omega$

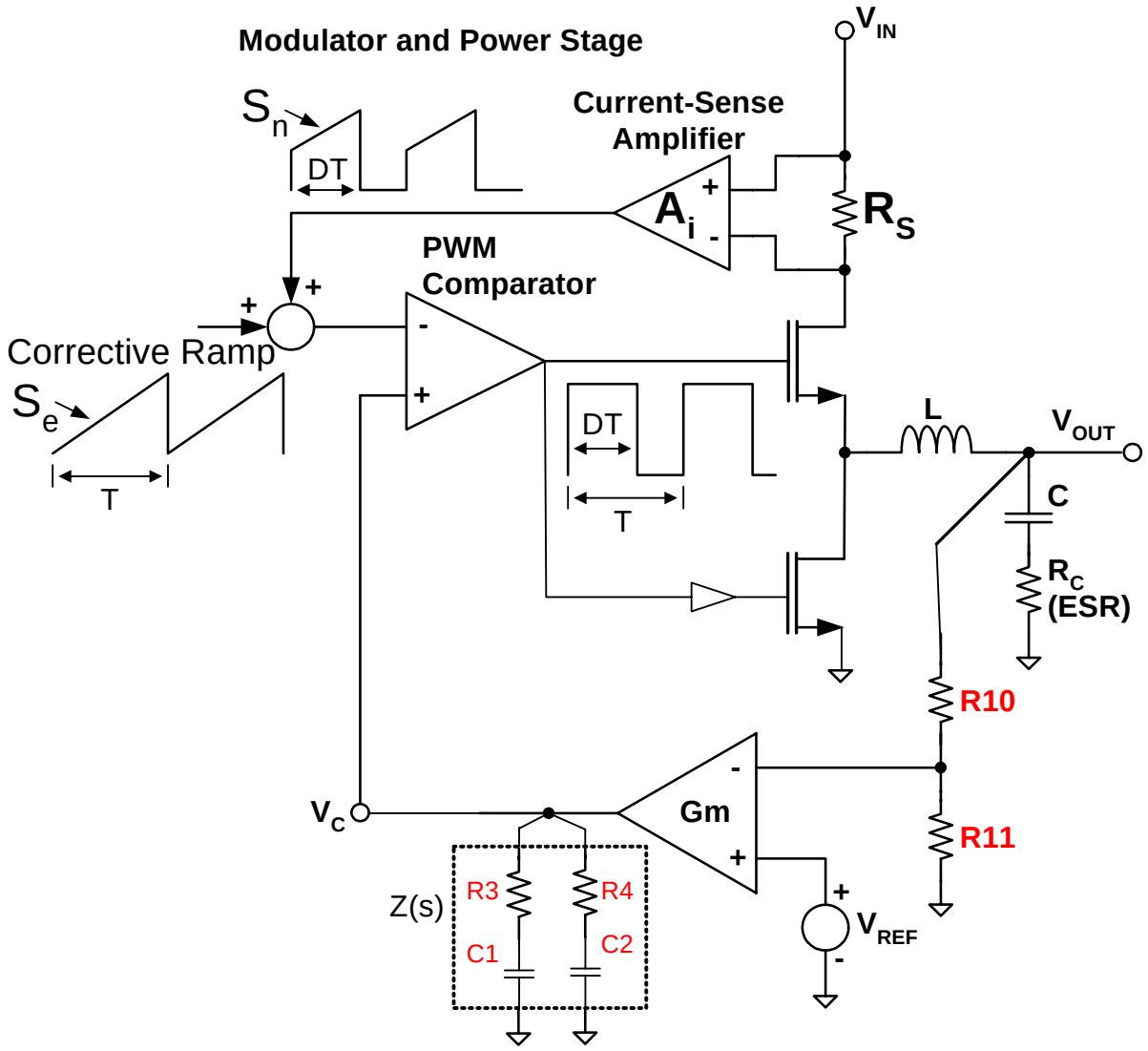


$R20_{max} := \frac{0.3\% \cdot Vo2}{Ifb_{max}}$ $R20_{max} = 49.5K\Omega$---> $R20_{us} := 4.99K\Omega$

$R10 := \frac{R11_{us} \cdot (Vo1 - Vref_{fb})}{Vref_{fb}}$ $R10 = 2.275K\Omega$

$R19 := \frac{R20_{us} \cdot (Vo2 - Vref_{fb})}{Vref_{fb}}$ $R19 = 8.329K\Omega$

9) Compensation network:(only for channel 1)



The model of the transfer function, the selection of the proper compensation network, and the final closed loop bode plots are explained only for the first output.
The simplified model below gives very simple reliable results without going deeply into details with complex analysis:

$i := 1..2000$ $\quad f_i := 100^{\frac{(i-200)}{500}}$ $\quad w_i := f_i \cdot \frac{1}{s}$ $\quad s_i := 2\pi \cdot j \cdot w_i$

$D1_{off} := 1 - D1_{nom}$

- Gain current sense amplifier:

$\rho := 5$

- Sensed current waveform into the PWM controller is: Sn1

$$Sn1 := \frac{D1_{off} \cdot Vi_{nom}}{L1_{us}} \cdot Rsns1_{used} \cdot \rho \qquad Sn1 = 2.643 \times 10^5 \frac{volt}{sec}$$

-Peak to peak internal compensation ramp: $Vm := 0.25V$

- Correction ramp slope: Se

$Se := Vm \cdot fsw$ $\quad Se = 5 \times 10^4 \frac{volt}{sec}$

- The compensation ramp factor: mc1

$mc1 := 1 + \frac{Se}{Sn1}$ $\quad mc1 = 1.189$

mc1 has to be > than $\frac{1}{2 \cdot D1_{off}} = 0.541$

- Output equivalent resistance: (at minimum and maximum load)

$Rout1_{max} := \frac{Vo1}{Io1_{max}}$ $\quad Rout1_{max} = 0.257\Omega$

$Rout1_{min} := \frac{Vo1}{Io1_{min}}$

- DC Gain: M

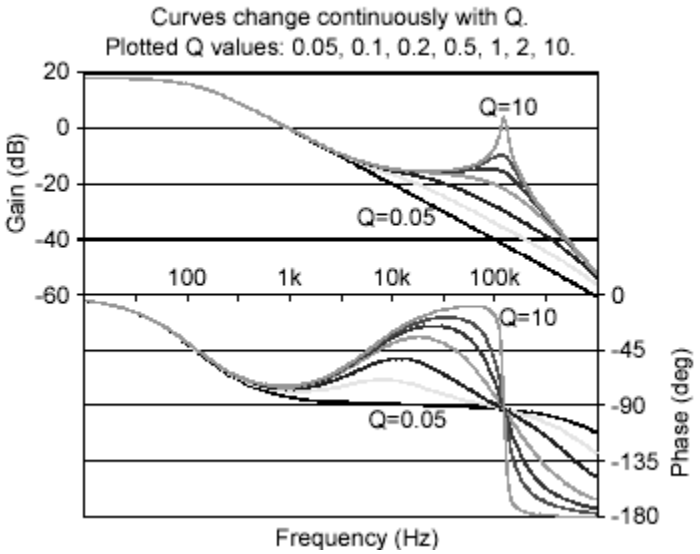
$M1_{max} := \frac{Rout1_{max}}{Rsns1_{used} \cdot \rho} \cdot \frac{1}{1 + \frac{Rout1_{max}}{L1_{us} \cdot fsw} \cdot (D1_{off} \cdot mc1 - 0.5)}$ $\quad M1_{max} = 4.345$

$M1_{min} := \frac{Rout1_{min}}{Rsns1_{used} \cdot \rho} \cdot \frac{1}{1 + \frac{Rout1_{min}}{L1_{us} \cdot fsw} \cdot (D1_{off} \cdot mc1 - 0.5)}$ $\quad M1_{min} = 24.231$

- Q factor: damping factor

$Q1 := \frac{1}{\pi \cdot (D1_{off} \cdot mc1 - 0.5)}$ $\quad Q1 = 0.531$

The control output transfer function has three poles and one zero. Two poles are either complex conjugated that are located at half the switching frequency, or are separate real poles.When Q is < 0.5 the two poles are real poles.
Negative Q means an unstable system because the control output transfer function will have a right half plane pole. Q is a function of duty cycle and the deepness of the ramp compensation (mc). The larger the duty cycle, the higher the Q value.



-First low frequency pole:(LC filter) (The pole change with load)

$$fp1_{max} := \frac{1}{2\cdot\pi\cdot C1_{us}\cdot Rout1_{max}} + \frac{1}{2\cdot\pi\cdot L1_{us}\cdot C1_{us}\cdot fsw}\cdot\left(D1_{off}\cdot mc1 - 0.5\right) \qquad fp1_{max} = 1.11KHz$$

$$fp1_{min} := \frac{1}{2\cdot\pi\cdot C1_{us}\cdot Rout1_{min}} + \frac{1}{2\cdot\pi\cdot L1_{us}\cdot C1_{us}\cdot fsw}\cdot\left(D1_{off}\cdot mc1 - 0.5\right) \qquad fp1_{min} = 0.199KHz$$

-Single zero:(Cout*ESR)

$$fz1 := \frac{1}{2\pi C1_{us}\cdot ESR1} \qquad fz1 = 48.229KHz$$

- Double poles, at half the switching frequency

$$fn := \frac{fsw}{2} \qquad fn = 100KHz$$

$$Fh1_i := \frac{1}{1 + \frac{s_i}{2\cdot\pi\cdot fn\cdot Q1} + \frac{(s_i)^2}{(2\cdot\pi\cdot fn)^2}}$$

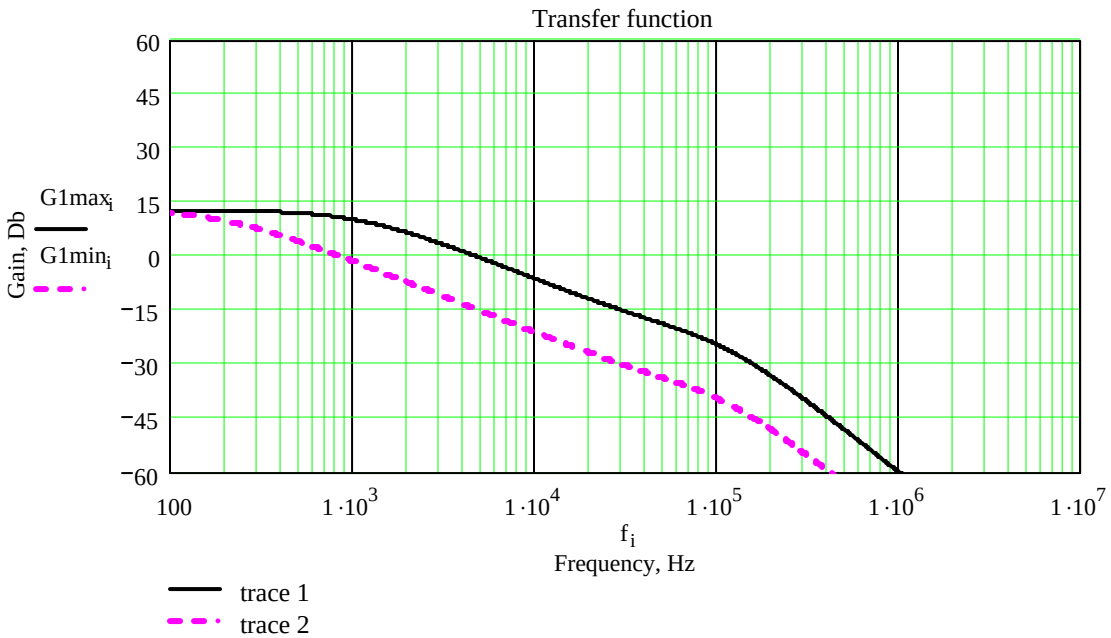
$$Fpmin_i := \frac{1 + \frac{s_i}{2\cdot\pi\cdot fz1}}{1 + \frac{s_i}{2\cdot\pi\cdot fp1_{min}}}$$

$$Fpmax_i := \frac{1 + \frac{s_i}{2\cdot\pi\cdot fz1}}{1 + \frac{s_i}{2\cdot\pi\cdot fp1_{max}}}$$

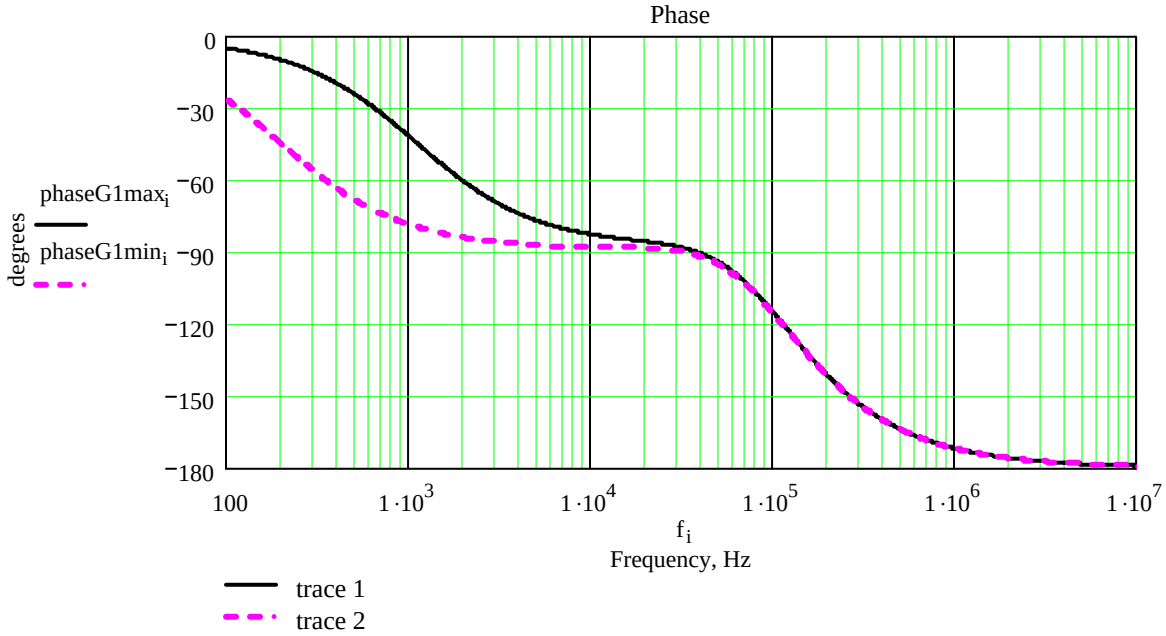
- The transfer function of the control loop:

$$Gs1max_i := M1_{max}\cdot Fpmax_i\cdot Fh1_i \qquad G1max_i := 20\cdot\log\left(\left|Gs1max_i\right|\right)$$

$$Gs1min_i := M1_{max}\cdot Fpmin_i\cdot Fh1_i \qquad G1min_i := 20\cdot\log\left(\left|Gs1min_i\right|\right)$$



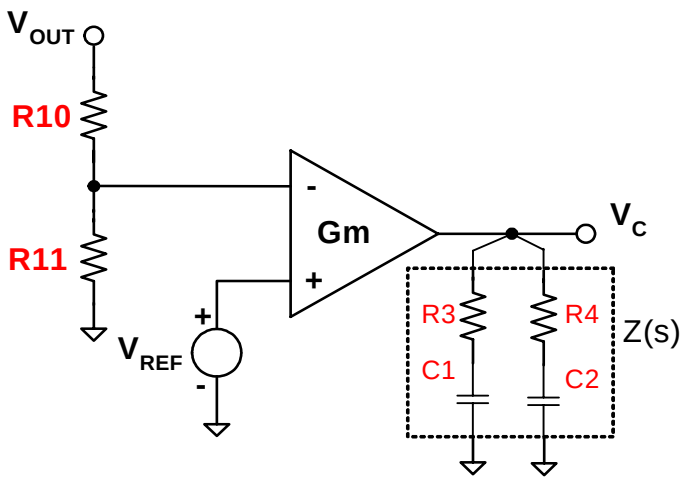
$$phaseG1min_i := arg\left(Gs1min_i\right)\cdot\frac{180}{\pi} \qquad phaseG1max_i := arg\left(Gs1max_i\right)\cdot\frac{180}{\pi}$$



- Proposed loop compensation design: basic rules

- Good to have a loop gain slope of -20dB/decade
- The crossover frequency should not exceed one fifth of the switching frequency:

Crossover frequency should be < $\frac{fsw}{5} = 40\,KHz$



1) Place a pole in the compensation at zero frequency, in order to increase the DC gain and therefore have higher DC regulation accuracy.
2) Place the first zero at first control loop pole: Zero1comp=fp1
3) Place the second pole at fz1: Pole2comp= fz1
4) Place the second zero at fp (half the switching frequency): Zero2comp=fp
-Transconductance error amplifier:

$g_m := 670 \cdot 10^{-6} \text{mho}$

- Desired loop transfer function crossover frequency: $fcc := 20\text{KHz}$

It can be optimised at maximum load, or minimum load

- Gain of the compensation:

$K := \frac{fcc}{M1_{max} \cdot fp1_{max}}$ $K = 4.147$

$R3 := \frac{K}{g_m} \cdot \frac{R10 + R11_{us}}{R11_{us}}$ $R3 = 9.011\text{K}\Omega$

$C1 := \frac{1}{2\pi \cdot fp1_{max} \cdot R3}$ $C1 = 15.912\text{nF}$

$C2 := \frac{1}{2\pi \cdot fz1 \cdot R3}$ $C2 = 0.366\text{nF}$

$R4 := \frac{1}{2\pi \cdot \frac{fsw}{2} \cdot C2}$ $R4 = 4.346\text{K}\Omega$

$Kcomp := g_m \cdot \frac{R11_{us}}{R10 + R11_{us}}$

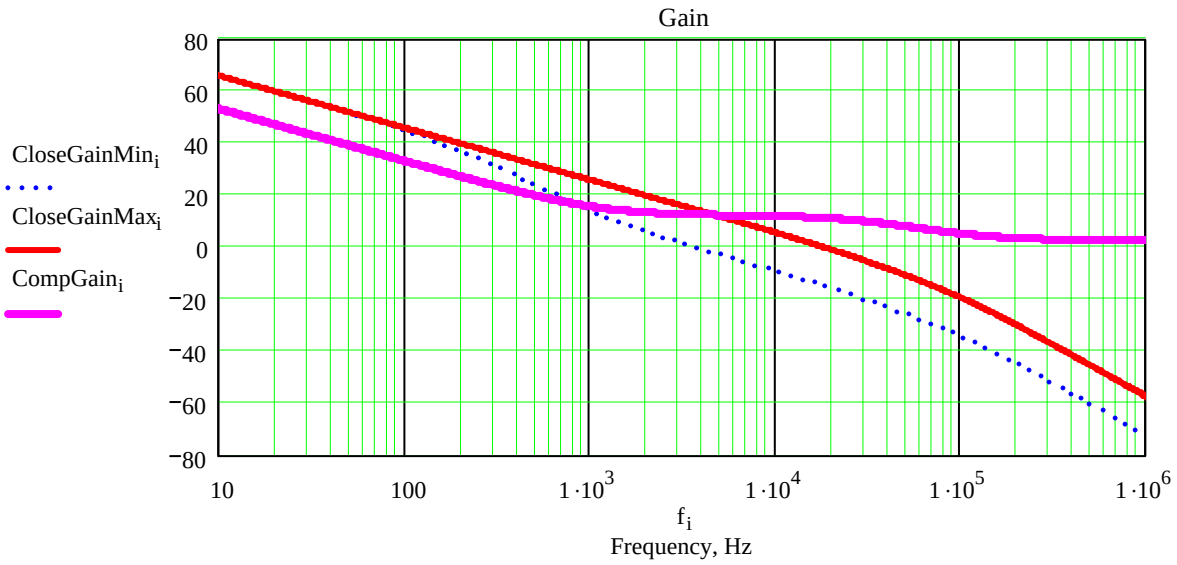
- Compensation DC gain:

$Z1_i := R3 + \frac{1}{C1 \cdot s_i}$ $Z2_i := R4 + \frac{1}{C2 \cdot s_i}$

$CompGain_i := 20\log\left[\left| Kcomp \cdot \frac{(Z1_i) \cdot (Z2_i)}{(Z1_i + Z2_i)} \right|\right]$

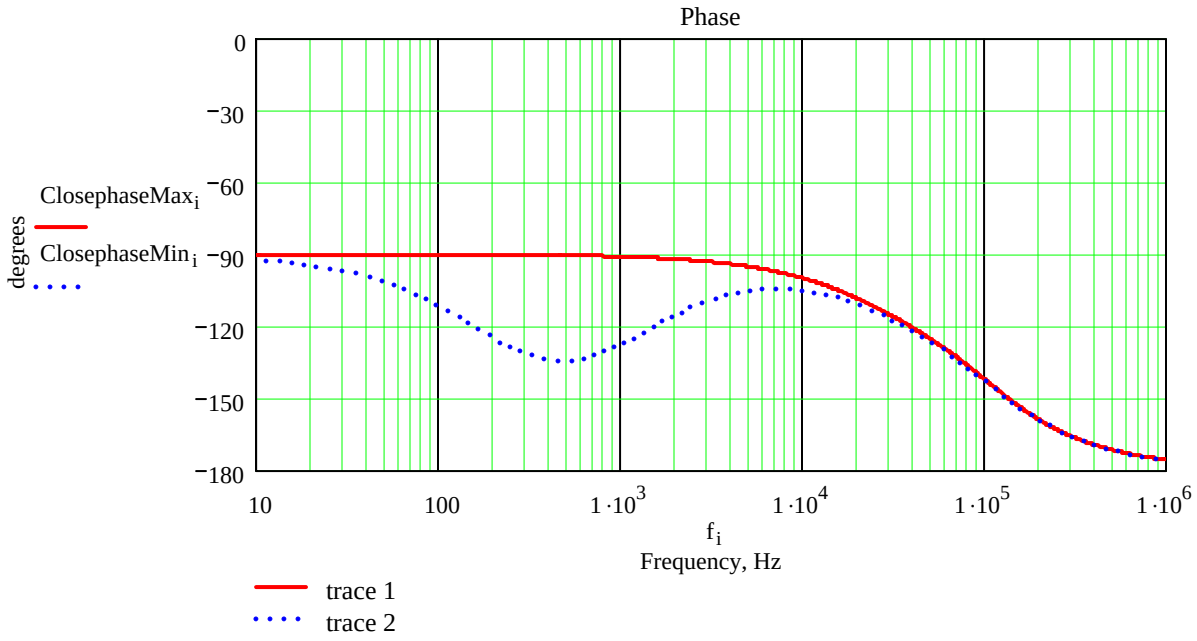
$CloseGainMin_i := 20\log\left[\left| Gs1min_i \cdot Kcomp \cdot \frac{(Z1_i) \cdot (Z2_i)}{(Z1_i + Z2_i)} \right|\right]$

$$CloseGainMax_i := 20\log\left[\left|Gs1max_i \cdot Kcomp \cdot \frac{(Z1_i)\cdot(Z2_i)}{(Z1_i + Z2_i)}\right|\right]$$



$$ClosephaseMax_i := \arg\left[Gs1max_i \cdot Kcomp \cdot \frac{(Z1_i)\cdot(Z2_i)}{(Z1_i + Z2_i)}\right] \cdot \frac{180}{\pi}$$

$$ClosephaseMin_i := \arg\left[Gs1min_i \cdot Kcomp \cdot \frac{(Z1_i)\cdot(Z2_i)}{(Z1_i + Z2_i)}\right] \cdot \frac{180}{\pi}$$



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3. C. Richardson, National Semiconductor, AN-1292 LM5642 Evaluation Board
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