ADC16DX370 IBIS Model Example Report

10/15/2013

IBIS Model

The IBIS model was generated by the TI modeling group from simulated results based on the IC design database. The model is called ‘adc16dx370.ibis’ and applies to the ADC16DX370 and LM97937. The verification here demonstrates the functional use of the models in Agilent ADS and verifies expected results.

CLKIN

CLKIN is a differential input with internal 100ohm termination. The model is a differential input model but IBIS does not natively model differentially oriented elements, so the internal termination can be instantiated with an additional 100 ohm resistor or with the ‘100_ohm’ Series model defined in the model file. Figure 1 shows an example test bench in Agilent ADS with the differential IBIS_DI model and the IBIS_S_I model which models the termination. The testbench drives a 100ohm matched, 400Vpp waveform into the CLKIN input and is verified in Figure 2.

Note that the IBIS model does model the 500mV input common-mode but the AC coupled circuit has a very long convergence time. Simulation time to steady-state operation can be greatly reduced with the use of initial condition at the CLKIN pins and small AC coupling cap values. Common-mode convergence is demonstrated in Figure 3.

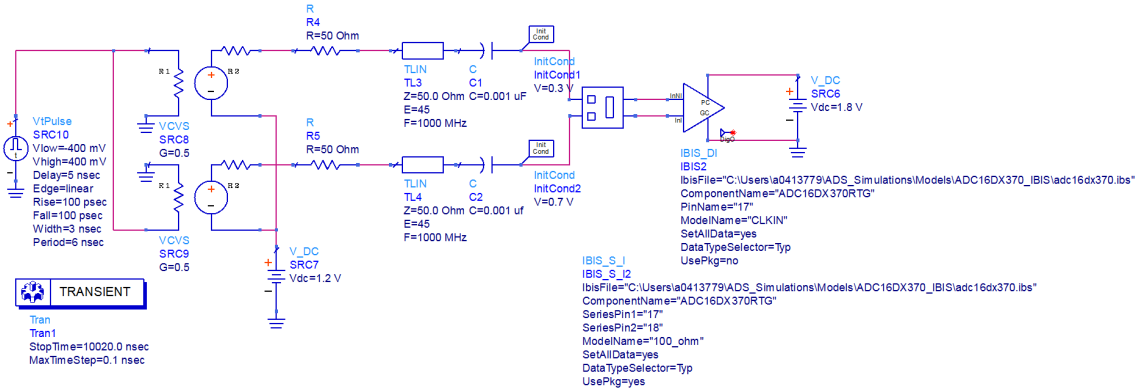


Figure 1: CLKIN IBIS Model Test Bench

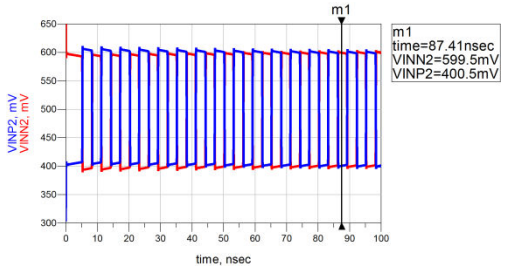


Figure 2: Simulated waveforms at CLKIN+ (VIP2) and CLKIN- (VIN2) inputs

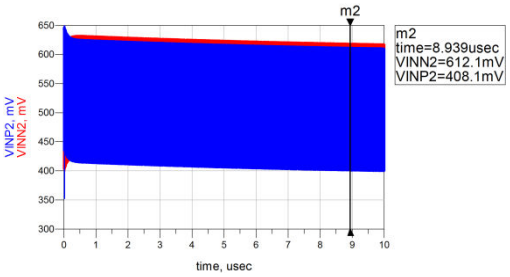


Figure 3: Common-mode convergence with non-ideal initial conditions

SYSREF

The SYSREF model is similar to the CLKIN model aside from the internal termination. The SYSREF input has a 2000 ohm internal differential termination that can be implemented with an external 2000 differential resistor or using the '2000_ohm' model in the IBIS file. The verification testbench is shown in Figure 4. Unlike the CLKIN testbench, the SYSREF interface requires a 100 ohm differential external termination on the source side of the AC coupling capacitors.

The steady-state waveform at the SYSREF input is shown in Figure 5 and the common-mode convergence is shown in Figure 6. The common-mode converges to ~460mV.

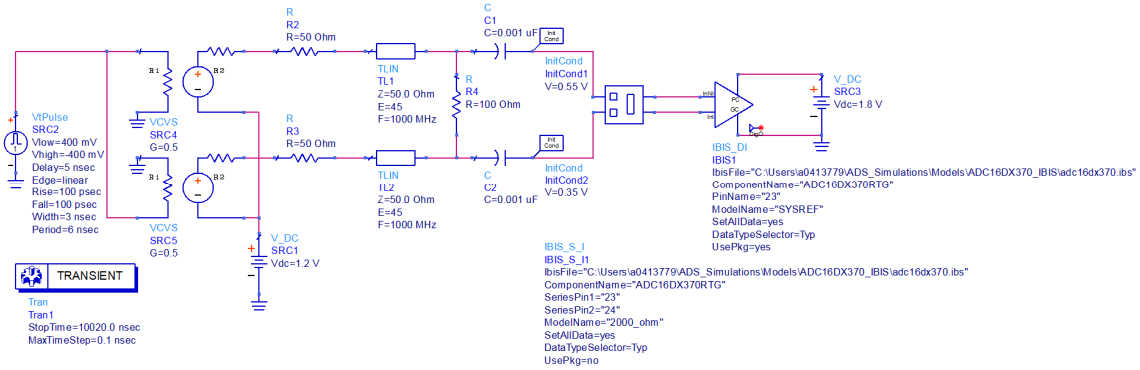


Figure 4: SYSREF IBIS Model Test Bench

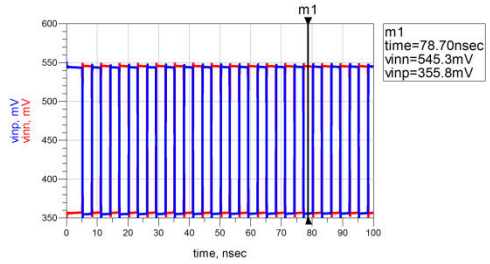


Figure 5: Simulated steady-state waveform at SYSREF+ (blue) and SYSREF- (red) inputs

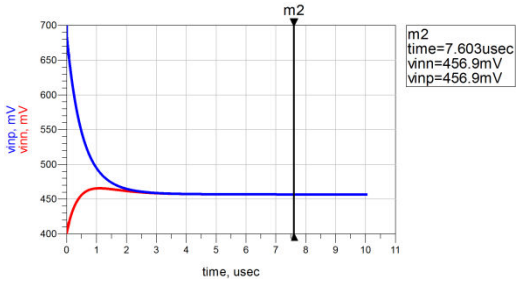


Figure 6: SYSREF common-mode convergence to

SYNC

The SYNC model also requires the external '100_ohm' termination model or an external 100 ohm resistance. The testbench is shown in Figure 7 and is DC couple from the source to load. Figure 8 verifies the waveform at the SYNCb+/- input for a standard LVDS signal with 1.2V common-mode and Figure 9 (a) and (b) demonstrates the compatibility at 0.6V and 1.8V common-mode.

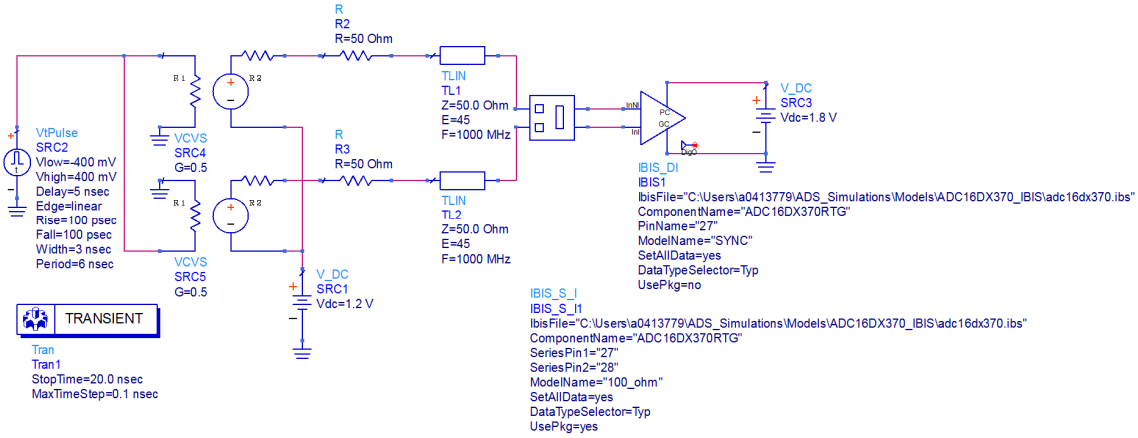


Figure 7: SYNCb IBIS Model Test Bench

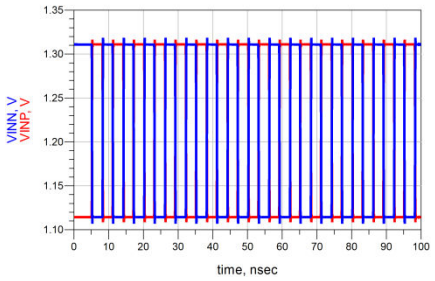
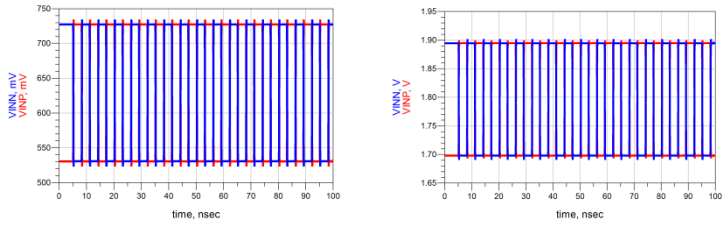


Figure 8: Simulated steady-state waveform at SYNCb+ (blue) and SYNCb- (red) inputs with 1.2V driving common-mode



(a) (b)

Figure 9: Simulated steady-state waveform with (a) 0.6V and (b) 1.8V driving common-mode

SDI, SCLK, CSb

The SPI input models are all collectively modeled under one name, SDI. The input model is demonstrated in the testbench of Figure 10 with 8ohm source, 22ohm series damping resistor, transmission line and an extra external loading capacitance. Figure 11 show the waveform result of a 1.8V CMOS logic signal incident at the SDI input and Figure 12 shows a close-in look at the rising-edge for different values of added capacitance at the load.

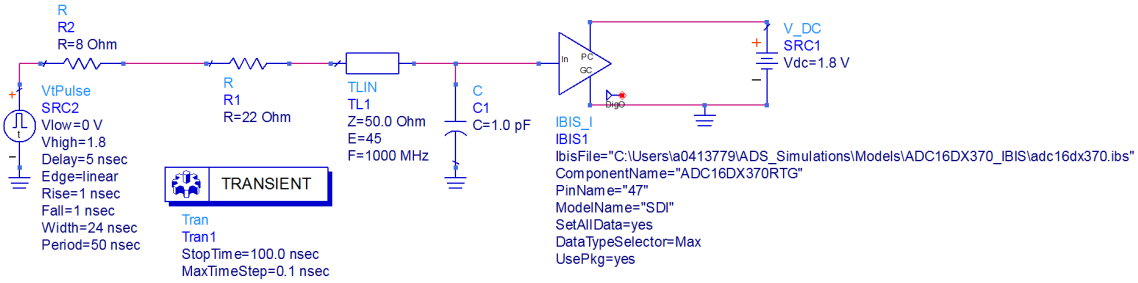


Figure 10: SDI IBIS model testbench

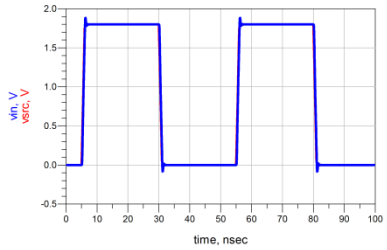


Figure 11: 1.8V CMOS waveform at the SDI input

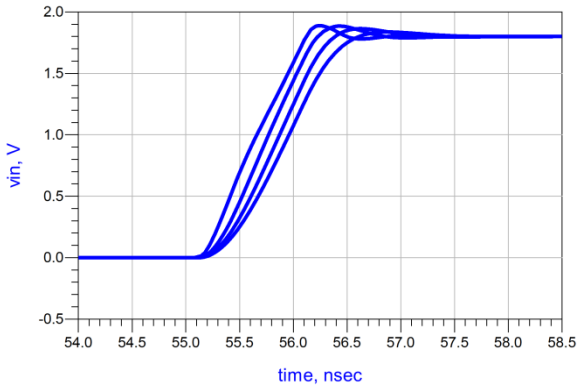


Figure 12: Waveform at SDI input for 1p, 4p, 7p, and 10pF additional capacitance at the load

SDO

The SDO model is a basic output model. The ADC16DX370 family supports an SDO output at multiple logic levels, but this model only accommodates the 1.8V logic output. The testbench of Figure 13 demonstrates the output driving a 22 ohm damping resistor, transmission line and capacitive load.

Figure 14 demonstrates the 1.8V logic waveform at the source and Figure 15 shows the rising edge at the source and load for different capacitive loading. Note that the dip in the waveform around the transition point at the source is caused by the transmission line, not the SDO model.

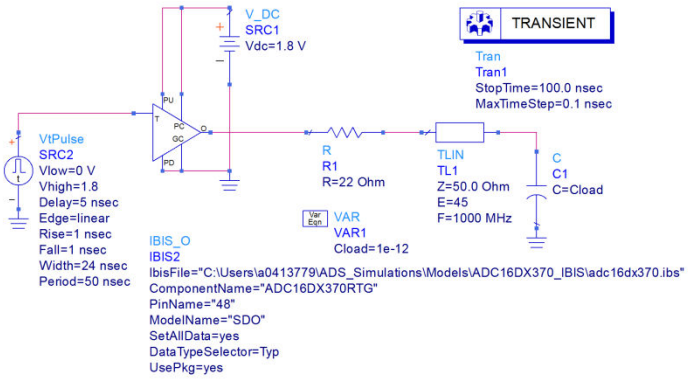


Figure 13: SDO IBIS model test bench

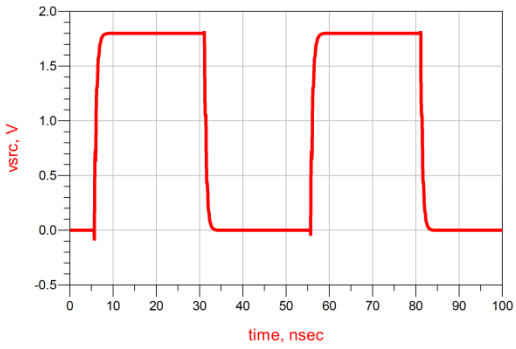
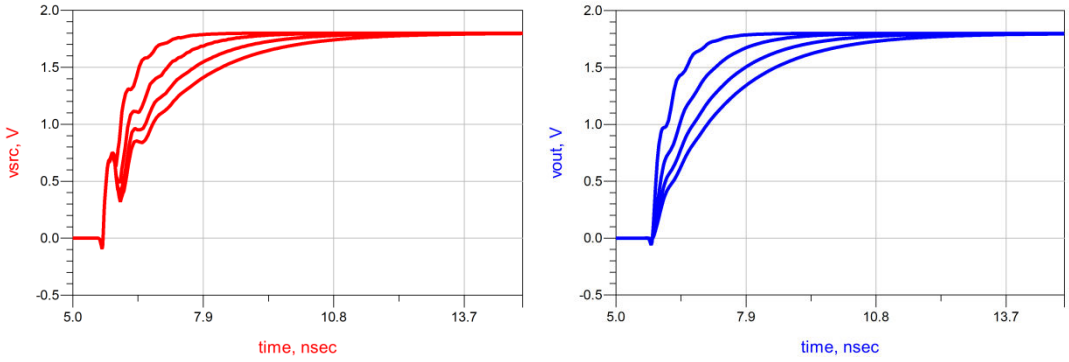


Figure 14: SDO output waveform at the source



(a) (b)

Figure 15: SDO output waveform at the (a) source and (b) load for 1p, 4p, 7p, and 10pF loading

SDIO

The SDIO model is used to represent the OVRA/TRIGRDY and OVRB/TRIGGER pins of the LM97937 and OVRA and OVRB pins of the ADC16DX370. The OVRA, OVRB, TRIGRDY signals are all outputs but the TRIGGER signal is an input to the LM97937, therefore the architecture of these pins are I/Os. The testbench implementation is shown in

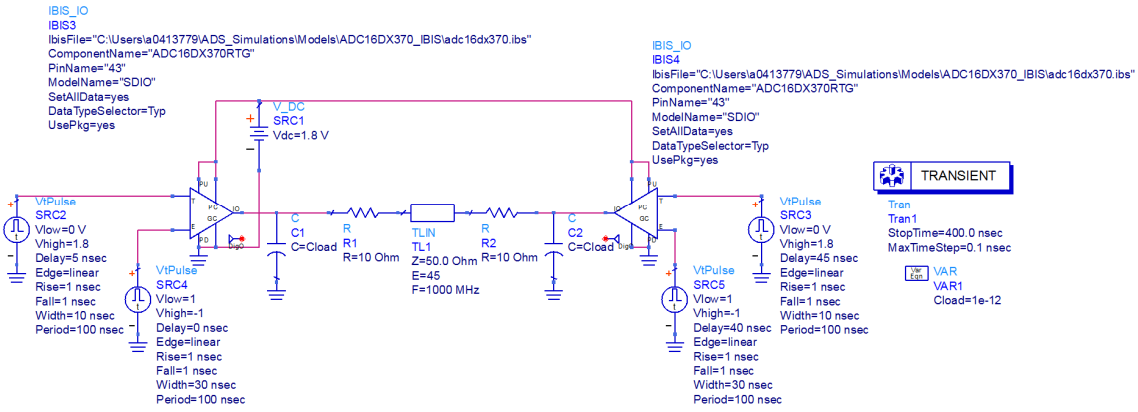


Figure 16: SDO IBIS model test bench

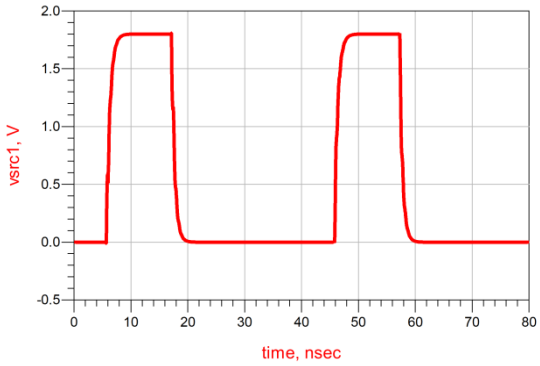
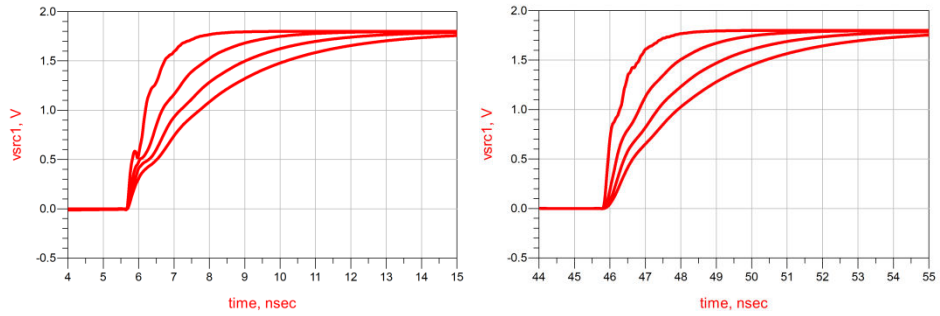


Figure 17: SDIO output waveform at the source where the first pulse is the response from the near driver and the second pulse is the response from the far driver



(a) (b)

Figure 18: SDIO output waveform at the (a) source and (b) load for 1p, 4p, 7p, and 10pF loading (at both source and load)