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Dynamic Limitations of Switched Mode Power Supplies

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By Bernd Geck, Power Design Services PDS

Updated by Josh Mandelcorn for Tech Day October 24, 2017

TI Training - Summary

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For several reasons power supplies are limited in dynamic behavior; this short presentation explains those physical reasons in depth.

Analyzing the physics in time domain and frequency domain will extend the knowledge of the audience in control theory.

One non-linear effect will be presented followed by 4 effects which limit maximum allowed speed (or Bandwidth) of overall control. Quantitating the phase shift effect of each of these 4 effects will allow evaluation of systems where more than one of these effects are active.

Agenda

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1) Power Stage - limited dynamics due to current slope of main choke

2) Pulse Width Modulator PWM – Nyquist criteria by Sample & Hold

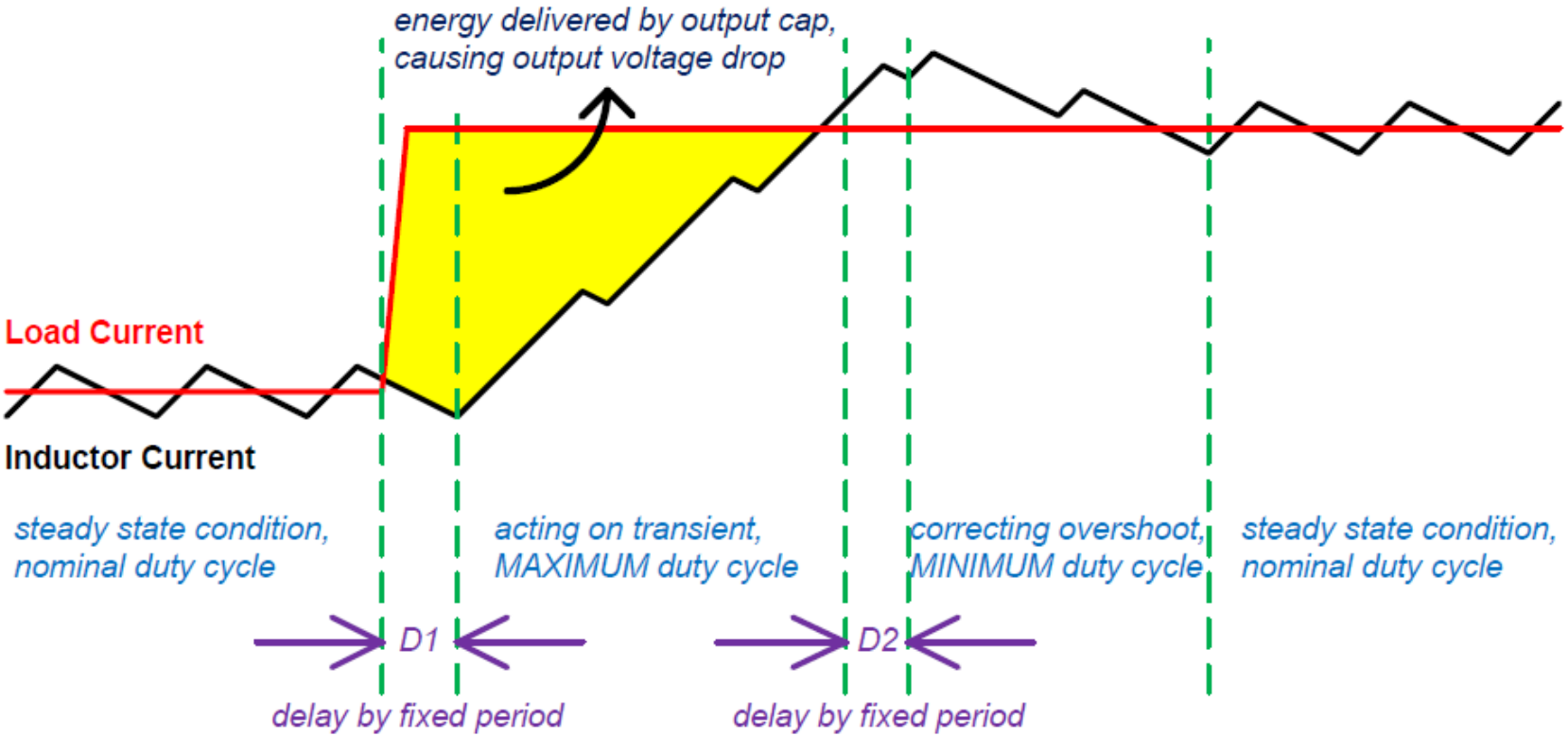
3) Error Amplifier – integrating transfer function

4) Opto-coupler – integrating transfer function

5) CCM Flyback Topologies – the Right Half Plane Zero RHPZ
Calculating the RHPZ

6) Summing up multiple effects – overall phase lag at desired crossover

1) Inductance limits current slope



1) Inductance limits current slope

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Just see Inductance Law: $-U_L = L \times di/dt$

So applying a certain voltage across an inductor will result in a rising current,

BUT: This slope is limited by inductance itself !

- **The inductor current is not able to follow fast load transients**
- **Output capacitor will be discharged causing an output voltage drop**
- **A smaller inductance might be beneficial for dynamic needs**

REMEMBER: for general purpose a ripple current 20% to 30% of DC load; for Point of Load's (POLs) supplying processor cores up to 40% is viable

Current slew rate in Low V POL outputs

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- With large load dumps only the low Vout is available to slew down inductor current
- Turning off synchronous FET during large load dumps helps somewhat
- Often target load is more tolerant of brief overshoots (heating) than brief undershoots (loss of sanity)
- In multi-phase allowing multiple phases to be on at same time helps with undershoot
- Max negative slew rate of converter current: (Vout + Vd)*Number of phases/L of each output inductor
- Vd being diode drop of synchronous rectifier FET if low side is turned off during load dump and near zero if low side FETs are on

Effects that limit control loop bandwidth

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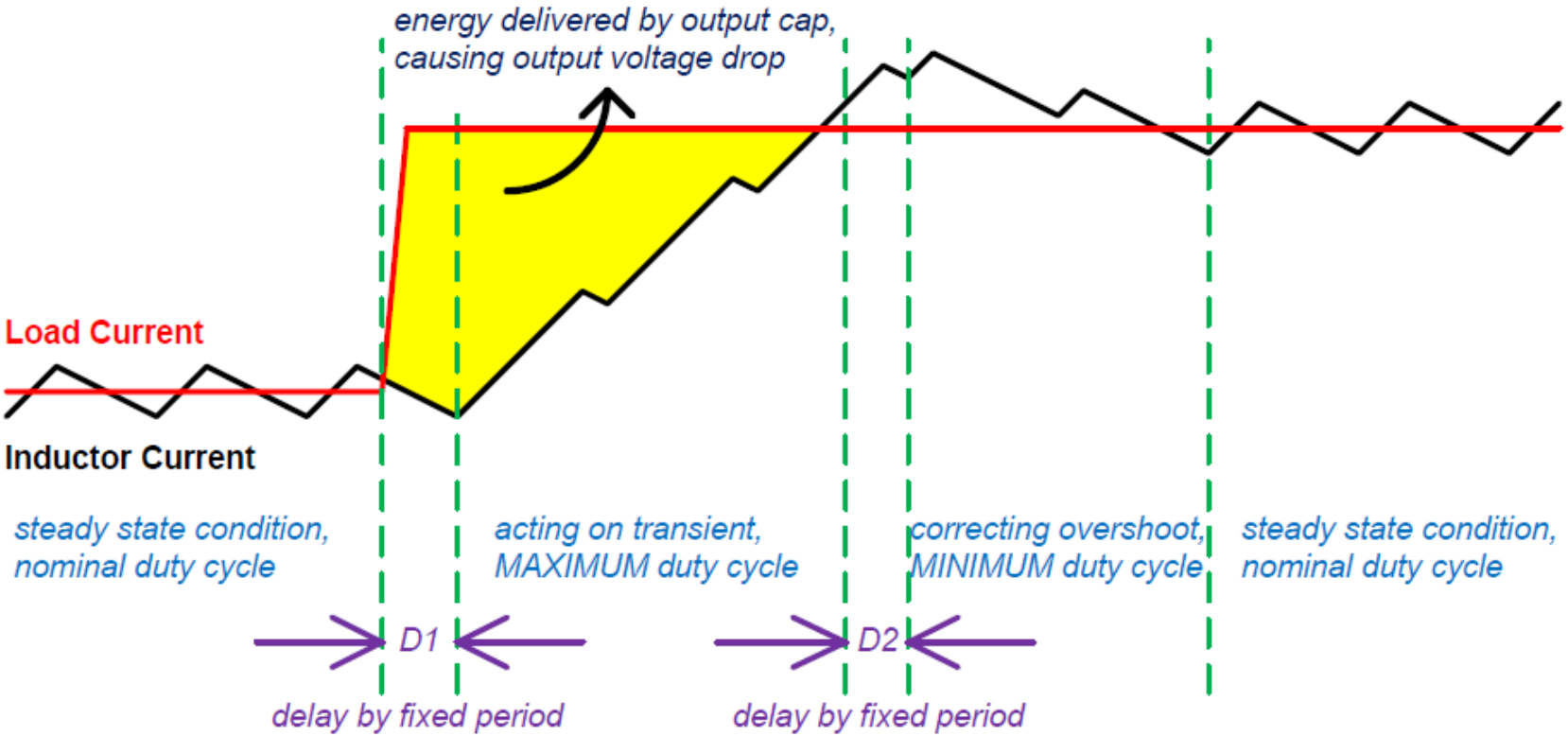
- Above inductor limitation is non-linear effect and regardless of loop control speed
- Effects to follow will limit maximum speed of control loop
- Loop speed expressed in terms of frequency that overall control loop gain reaches unity or zero dB gain
- Common stability target is at least 45 degrees phase margin at that frequency
- Phase budget for these effects – a little as 20 degrees for Voltage mode with ceramic output caps (-180 degrees for dual L-C pole, +67 degrees for type 3 compensation vs. 45 degrees margin target)
- Also needed for good stability is for gain to continue to drop such at gain is at least ~10dB when phase margin reaches zero (overall -180 degrees phase shift)

2) Pulse Width Modulator Delays Response



PWM creates delay that limits Loop Bandwidth

- Trailing edge modulation is most common scheme
- Especially in small signal case, any change is delayed until next turn off decision point
- Even in large signal, after turn off no change can occur until next cycle
- In small signal average delay will be ½ switching cycle
- Control transfer function of a pure delay is a phase lag of 360 degrees times frequency times delay

Pulse Width Modulator (PWM) limits Loop Bandwidth

- feedback divider transfers reference level to needed output level
- error amplifier provides gain – and loop compensation (poles & zeros)
- error voltage gets compared with saw tooth voltage
- the final result is a pulse width modulated signal to drive the power FET

- When decision made the error voltage is effectively SAMPLED into pulse width AND HELD until the next cycle's decision point – better resolution needs higher switching frequency!

Remember: ***for general purpose loop bandwidth a decade below switching frequency is safe, set Fco to 1/10 of Fsw***

Phase margin effect of PWM delay

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- From control loop standpoint PWM creates an average delay of ½ switching period
- Phase lag effect is 360 degrees times delay divided by frequency or 180 degrees times Fcrossover/Fswitching
- With above rule of crossover frequency being 1/10th switching frequency delay reduces phase margin by 18 degrees
- This is about the maximum loss of phase margin allowed in voltage mode controllers with all ceramic output caps
- With either low ESR output caps or current mode control and more inherent phase margin crossover at 1/5th switching frequency may be feasible
- In multi-phase with analog control PWM delay gets divided by number of phases

Error Amplifier Bandwidth limits Dynamics

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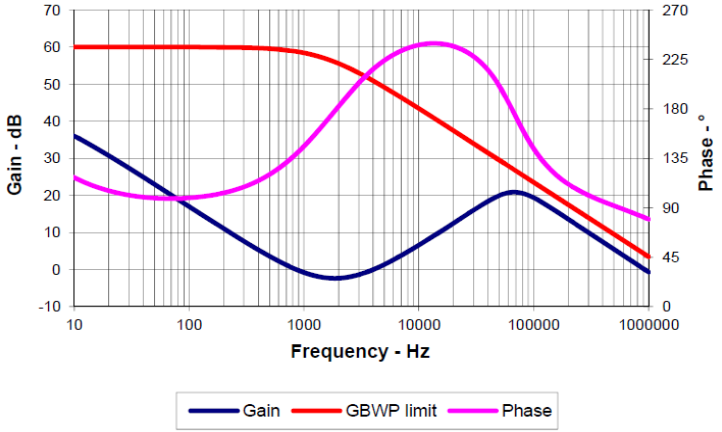
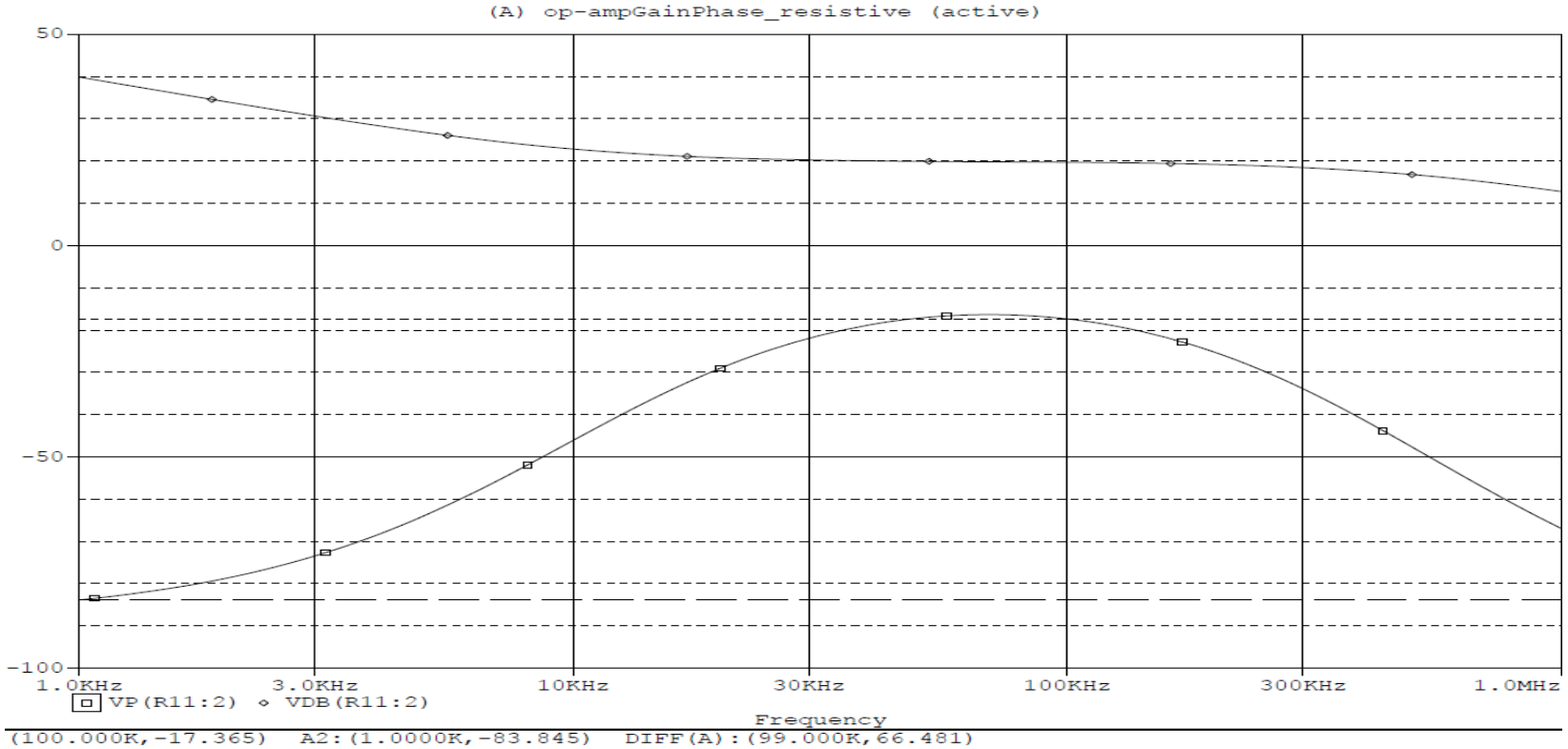
Limitation: the error amplifier itself is just an operational amplifier, physically limited by open loop gain and gain bandwidth product – results in integrating behavior:



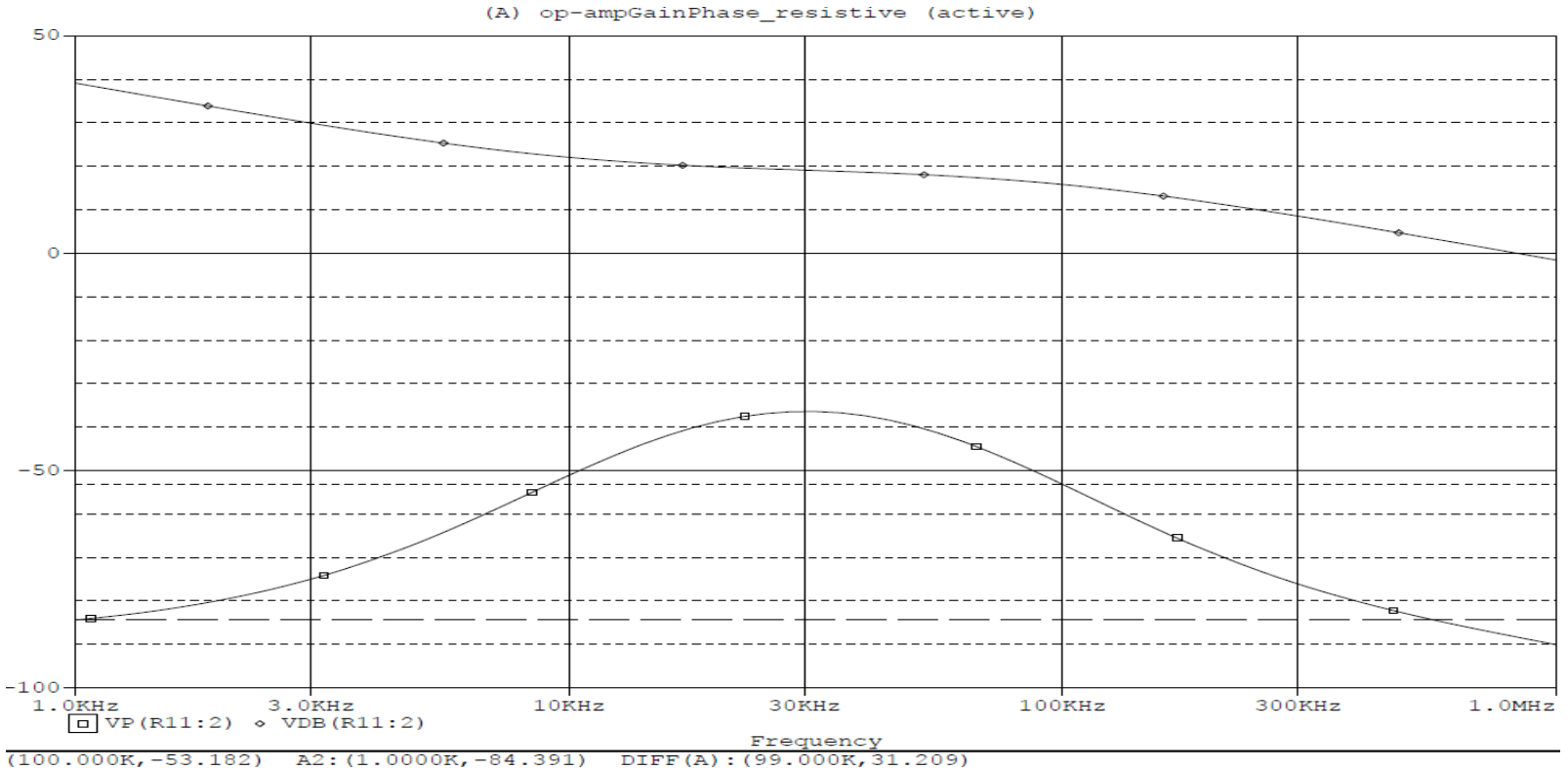
the **gain** applied to the error amplifier must stay below **Gain Bandwidth Product**

Remember: a rule of thumb is that gain bandwidth product of op-amp should be >10x crossover frequency times gain needed at crossover

GBW at 10MHz – Target gain of 10 @100kHz



GBW at 1MHz – Target gain of 10 @100kHz

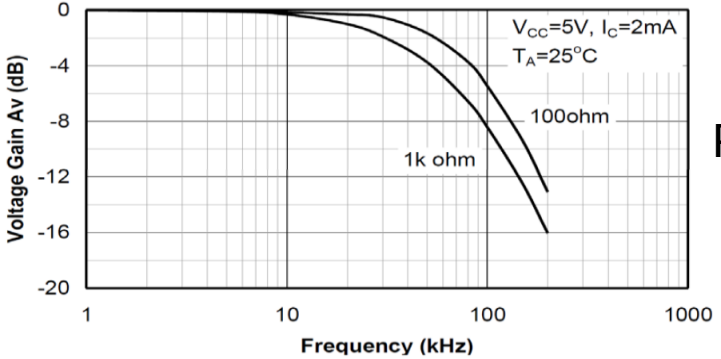


Phase lag due to Gain Bandwidth GBW of Op-amp

- For op-amp with input impedance resistive at frequency of interest
- A good approximation of added lag due to op-amp Gain Bandwidth product
- 57.3 degrees times (needed op-amp gain at frequency of interest plus one) divided by GBW of op-amp
- For input impedance capacitive at this frequency of interest added lag is about ½ to ¾ above formula
- This based upon PSPICE op-amp simulations
- Frequency of Interest is generally overall loop crossover frequency

Opto Coupler limits Dynamics at Isolated SMPS

The opto coupler, closing the loop in between error amplifier on secondary side and controller on primary side, has an integrator transfer function, too.
Frequency response of LTV-10xx-G.cut off -3dB around 70kHz



Phase lag = ArcTan(Frequency/pole frequency

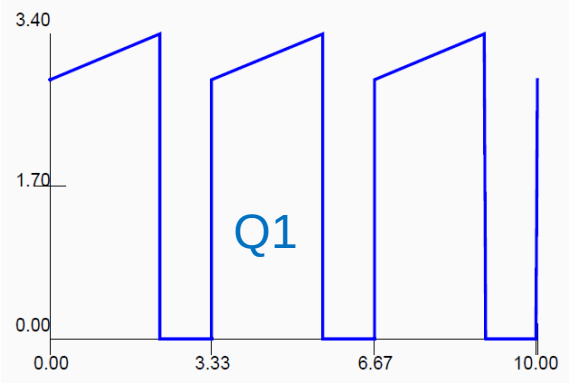
Options for Improvement: - high performance opto coupler (cost !) or - digital isolator (cost !)
- or controller at secondary side (needs secondary auxiliary voltage and isolated gate drive to primary)

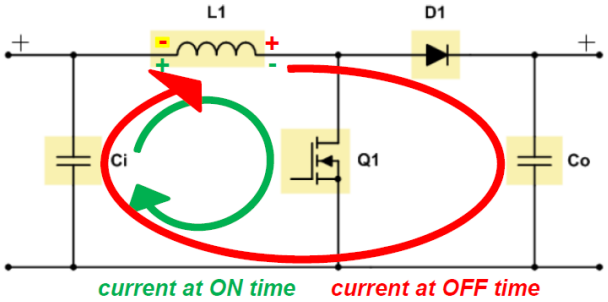
The Right Half Plane Zero RHPZ

All topologies transferring energy to the output as switch is OPEN like boost – flyback – SEPIC - Cuk and working in CCM are affected by RHPZ !

Boost power stage example:

ON time =
energizing the inductor





just valid for steady state,

? what about transient ?

OFF time =
powering the output

The RHPZ in Time Domain

In case of load transient = output demands more power

1. the inductor needs to be energized even more, so INCREASING the ON time first, means
2. at a fixed period DECREASING the OFF time, so delivering LESS energy to the output, means

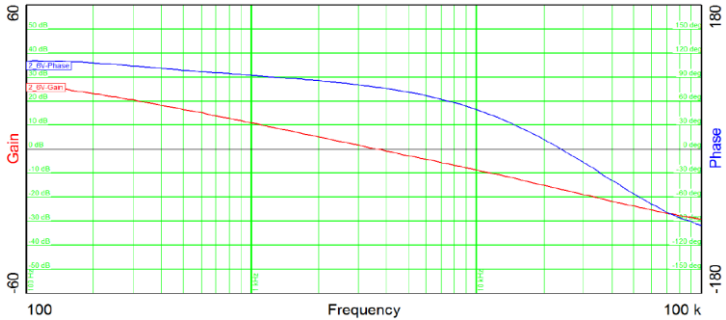
at the very first moment exactly the opposite behavior that is needed by load

This interaction of duty cycle, the transient phenomenon needs to be damped; **duty cycle slew rate needs to be slower than inductor slew rate** (see topic 1).

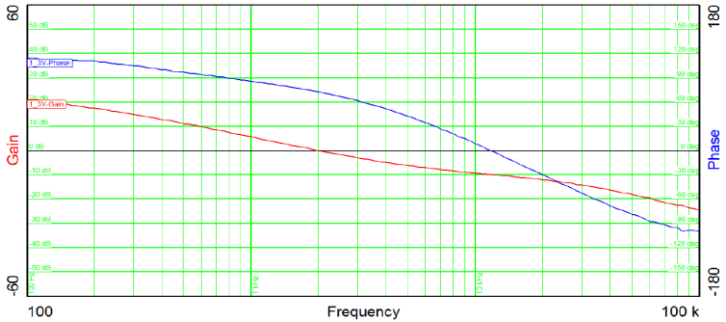
Remember: the RHPZ itself could NOT be compensated

The RHPZ in Frequency Domain

The RHPZ is a function of inductance, duty cycle and load; in frequency domain a zero at the right half plane results in increase of gain and **DECREASE** of phase. If RHPZ is close to cross over area the design will be unstable – see true hardware:



PMP30149, tiny 10W CCM SEPIC, loop at 6Vin, duty cycle 49%, **RHPZ 88kHz** no impact to crossover area 3.6kHz (phase margin 77degrees, gain margin -17dB)



Loop at 3Vin, duty cycle 66%, **RHPZ 22kHz** here gain increases and phase drops ! Bandwidth reduced to 2kHz, but still less PM 73degrees, GM-12dB Above crossover gain increased and phase reduced

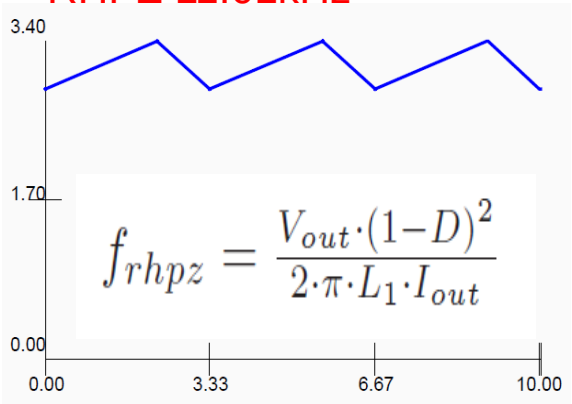
The RHPZ in Discontinuous Conduction Mode

Analyzing the inductor current of prior boost example (5Vin/15Vout/300kHz/22uH)

The RHPZ still exists in BM and CCM – but due to- high load resistance in boundary mode BM and even higher load resistance and small duty cycle in DCM the typical crossover area will not be affected by RHPZ

CCM, load 1A, d=68%

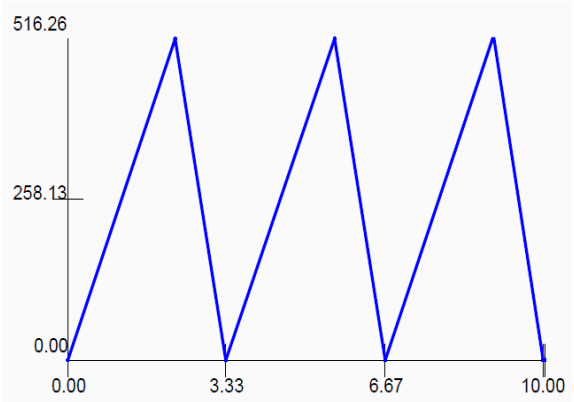
RHPZ 11.01kHz



$$f_{rhpz} = \frac{V_{out} \cdot (1-D)^2}{2 \cdot \pi \cdot L_1 \cdot I_{out}}$$

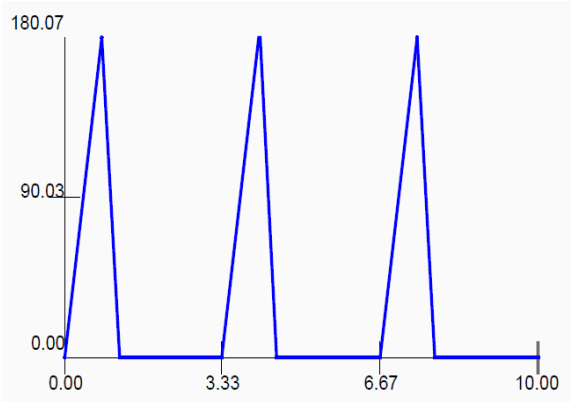
BM, load 82mA d=68%

RHPZ 134kHz



DCM, 10mA, d=24%

RHPZ 6.3MHz



The RHPZ - Summary

- **At Forward topologies RHPZ does not exist; reacting on load transients an increase of duty cycle directly results in increase of output power.**
- **In DCM the RHPZ is out of crossover area not affecting the loop, an easy explanation in time domain: Any change in inductor current needed is completed each cycle.**
- **IN CCM the RHPZ could not be fully compensated, gain increase needs to be cancelled with pole at same frequency which doubles phase lag.**
- **For fairly low power and need of best dynamics operate the design in DCM; ensure, that the design stays in DCM under all circumstances.**

Remember: for safe operation of boost and flyback working in CCM set crossover frequency to below 1/6th to 1/3rd of RHPZ

RHPZ mitigation with Pole at same frequency

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- Adding Pole at same frequency as RHPZ will cancel the gain increase with frequency
- However, this Zero – Pole combination will add phase lag with increasing frequency, similar to a pure delay
- Phase lag will be ArcTan of (frequency / RHPZ frequency) plus ArcTan of (frequency / Added pole frequency)
- Limiting crossover to 1/6th this RHPZ frequency will limit this to 19 degrees similar to 1/10th switching frequency rule above
- For current mode or damped output capacitance cases, crossover limited to 1/3rd RHPZ will limit added phase lag to 37 degrees (similar to 1/5th switching frequency)

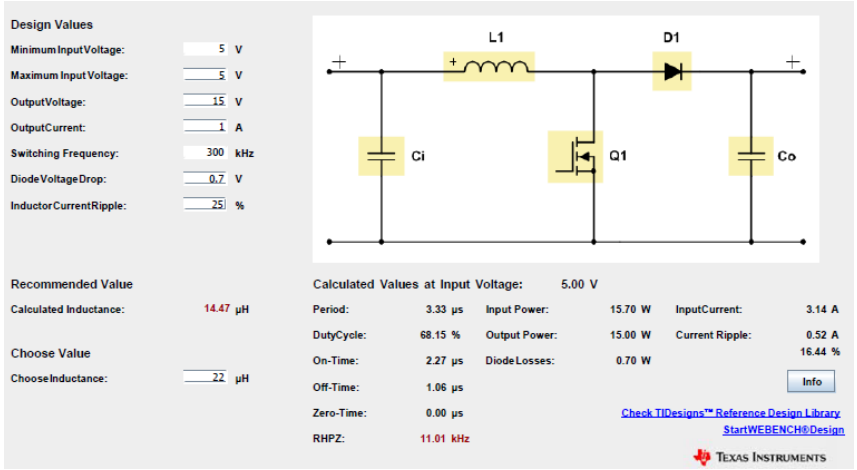
RHPZ mitigation continued – other options….

- Worst case (lowest frequency) RHPZ will need to be used – for Boost that will be minimum Vin and maximum load
- For opto-isolated feedback the pole of the opto can be used for this purpose of insuring gain does not rise with frequency
- Likewise the GBW limitation “pole” of the error-amp can also serve this purpose
- On the other hand, the delay due to PWM is not a gain roll off and cannot cancel increasing gain of the RHPZ

Calculating the RHPZ

JAVA based design tool “**TI POWER STAGE DESIGNER**” by PDS Europe calculates RHPZ

http://www.ti.com/tool/powerstage-designer



“**TI Power Topologies Handbook**” by PDS Europe contains all equations regarding topologies – and RHPZ…
Power Stage Designer, the Handbook, the Quick Reference Guide, also at: http://www.ti.com/tool/powerstage-designer

Calculating the RHPZ - handcrafted

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Boost Converter:

$$f_{rhpz} = \frac{V_{out} \cdot (1-D)^2}{2 \cdot \pi \cdot L_1 \cdot I_{out}}$$

Inverting Buck Boost:

$$f_{rhpz} = \frac{V_{out} \cdot (1-D)^2}{2 \cdot \pi \cdot D \cdot L_1 \cdot I_{out}}$$

SEPIC:

$$f_{rhpz} = \frac{V_{out} \cdot (1-D)^2}{2 \cdot \pi \cdot D^2 \cdot L_1 \cdot I_{out}}$$

Cuk:

$$f_{rhpz} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{1-D}{L_1 \cdot C_{ccap}}}$$

Flyback:

$$f_{rhpz} = \frac{V_{out} \cdot (1-D)^2}{2 \cdot \pi \cdot D \cdot L_{sec} \cdot I_{out}}$$

Multiple bandwidth limits Interactions

- In applications where more than one of the above 4 effects are applicable the total phase lag that they contribute at the desired crossover frequency must be looked at
- This is the sum of the phase lag of the RHPZ, opto-coupler “pole”, bandwidth limitation of error-amp and delay of PWM
- Again phase lag for each pole or RHPZ is Arctan(Fcrossover/[Fpole or Frhpz])
- For voltage mode with all ceramic output caps this phase lag needs to be held to 20 degrees
- For current mode, or voltage mode with low esr output caps a 40 degrees of lag target is applicable

TI Design - EXAMPLE

Automotive i.MX6 Quad Core Processor Power Reference Design

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Description

The TIDA-00804 reference design is a low-cost discrete power solution for the i.MX6Q quad core application processor. All the DCDC regulators operate at frequencies above the AM radio broadcast band to avoid interference with the radio and to provide a small solution size due to smaller filter components. The first stage DC-DC converter can support a voltage input range of 6V to 42V, allowing the design to support start-stop operation as well as load dump. The second stage DC-DC converters provide all the necessary power rails to power the i.MX6Q. No power sequencer is necessary for this design. The PWB is a 4 layer board with 2 oz. copper to provide good power dissipation at 85 C ambient.

Visit: ti.com/tidesigns

Part number:
TIDA-00804

Features

Wide input voltage range: off battery 6V to 42V power supply to support start-stop system and load dump
The DC-DC regulators all operate above 1.8 MHz to avoid AM band interference
Very small form factor: 75mm x 58mm circuit board dimensions
No power sequencer necessary
Less than 5% ripple on all power rails

Thank you