TECH DAYS
Texas Instruments

Optimizing EMI and Mitigating Noise in Automotive DC/DC Converters

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Training Summary

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Optimizing EMI and Mitigating Noise in Automotive DC/DC Converters

High-frequency conducted and radiated emissions from power converters occur based on the transient voltage (dv/dt) and transient current (di/dt) generated during hard switching. Such electromagnetic interference (EMI) is an increasingly vexing issue in the design and qualification cycle, especially given the increased switching speed of power MOSFETs. This training provides an understanding of EMI from both theoretical and practical standpoints. Three sections are provided as follows:

1. **EMI overview and fundamentals**
2. **EMI noise sources and mitigation**
3. **EMI management with practical circuit examples**

What you'll learn:
Understand, avoid and solve power supply EMI issues.

- Understand EMI standards, measurements, differential & common-mode emissions
- Identify the role of power stage parasitics in EMI generation
- Learn about e-field coupling mechanisms
- Look at filtering and mitigation, leveraging IC and system-level "features"
- Review practical circuit examples – PCB layout recommendations, EMI plots

Audience: Analog, Power, DC/DC converter, Buck controller

Specific TI Designs & Parts:

- Part #'s: LM5145, LM53635-Q1
- TID #'s: TIDA-00987

Detailed agenda

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1. **EMI overview and fundamentals**
   - EMI noise coupling paths (DM & CM)
   - EMI standards: EN55022 class B (industrial), CISPR 25 class 5 (automotive)
   - EMI measurement setup & LISN schematic
   - EMI filtering, DM & CM equivalent circuits, CM noise propagation paths
2. **EMI noise sources and mitigation**
   - “Hot” loops, parasitic inductance, magnetic fields
   - SW node harmonics & voltage ringing, electric fields
   - Circuit and layout techniques for EMI mitigation
3. **EMI management in DC/DC converters**
   - Component placement, GND plane management, PCB stack-up strategies, etc.
   - Practical circuit examples, EMI performance-optimized PCB layouts, EMI results
     - **LM5145**: V_{IN} = 6V to 100V, V_{OUT} = 5V, I_{OUT} = 20A [PCB layout, input caps, inductor selection]
     - **LM53635-Q1**: V_{IN} = 3.5V to 42V, V_{OUT} = 5V, I_{OUT} = 3.5A [HotRod package, PCB layout]

Acronym definitions

- **CISPR** - COMITÉ INTERNATIONAL SPÉCIAL DES PERTURBATIONS RADIOÉLECTRIQUES (INTERNATIONAL SPECIAL COMMITTEE ON RADIO INTERFERENCE)
- **LISN** Line Impedance Stabilization Network
- **AN** Artificial Network
- AMN Artificial Mains Network
- EUT Equipment Under Test
- **DM** Differential Mode
- **CM** Common Mode
- CE Conducted Emissions
- RE Radiated Emissions
- RBW Resolution Bandwidth (of EMI receiver / spectrum analyzer)
- FFT Fast Fourier Transform
- dBµV → 0dBµV = 1µV, 20dBµA = 10µA
- PE (Protective Earth) or GW (Green Wire) = Earth Ground

EMI Overview and Fundamentals

EMI challenges

EMI challenges in power supply design

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1. EMI is a challenge for nearly all electronic systems, especially for **automotive** devices

2. **EMI source → coupling path → receptor**
   – Conducted path through cabling
   – Radiated EMI path through air

3. ***Conducted EMI*** : **CISPR 22** covers frequencies from **150kHz to 30MHz** (higher with **CISPR 25** automotive spec… up to **108MHz**)

4. ***Radiated EMI*** : **CISPR 22** covers frequencies from **30MHz to 1GHz** (higher with **CISPR 25** automotive spec… up to **2.5GHz**)

5. Leverage IC and system-level features:
   - Low inductance IC package / pinout
   - Careful PCB layout
   - Spread spectrum / slew-rate control
   - EMI filtering

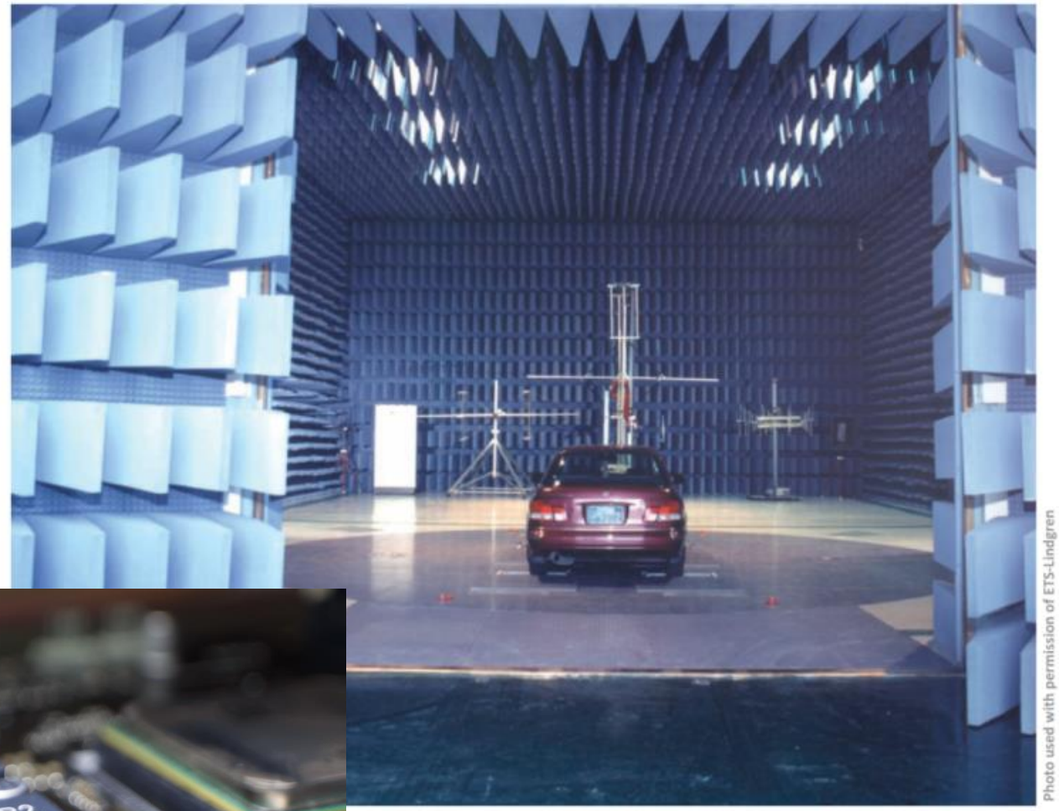
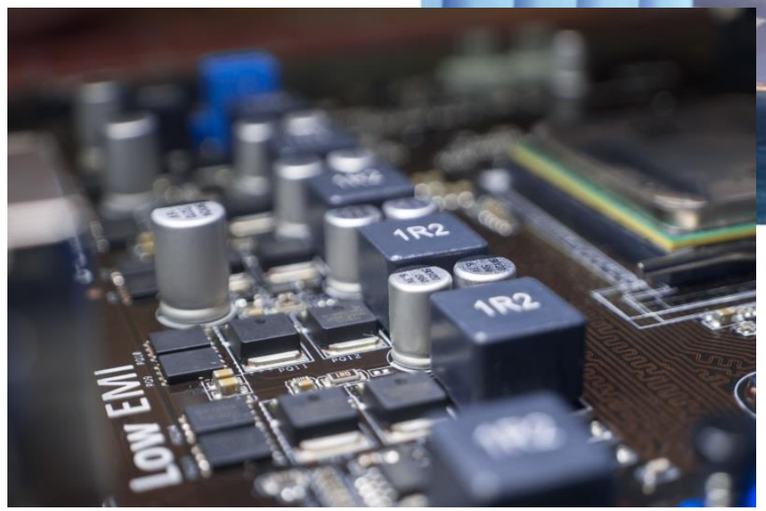
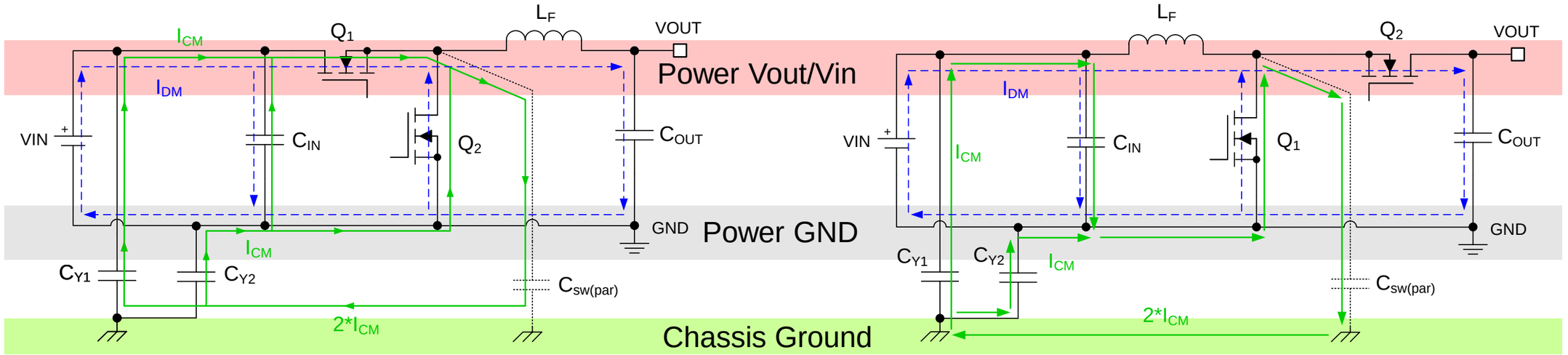


Photo used with permission of ETS-Lindgren



DM and CM conducted noise paths: buck & boost

1. **Differential-mode (DM)** AC noise current flows in power wires (forward and return path, opposite direction)
2. **Common-mode (CM)** AC noise current flows in both power wires (same direction), returning via chassis Ground



Differential-mode noise is like:

The measured input or output ripple of a DC/DC converter.

Vin or Vout noise against GND that can be filtered with caps, ferrite bead and low frequency PI-Filter.

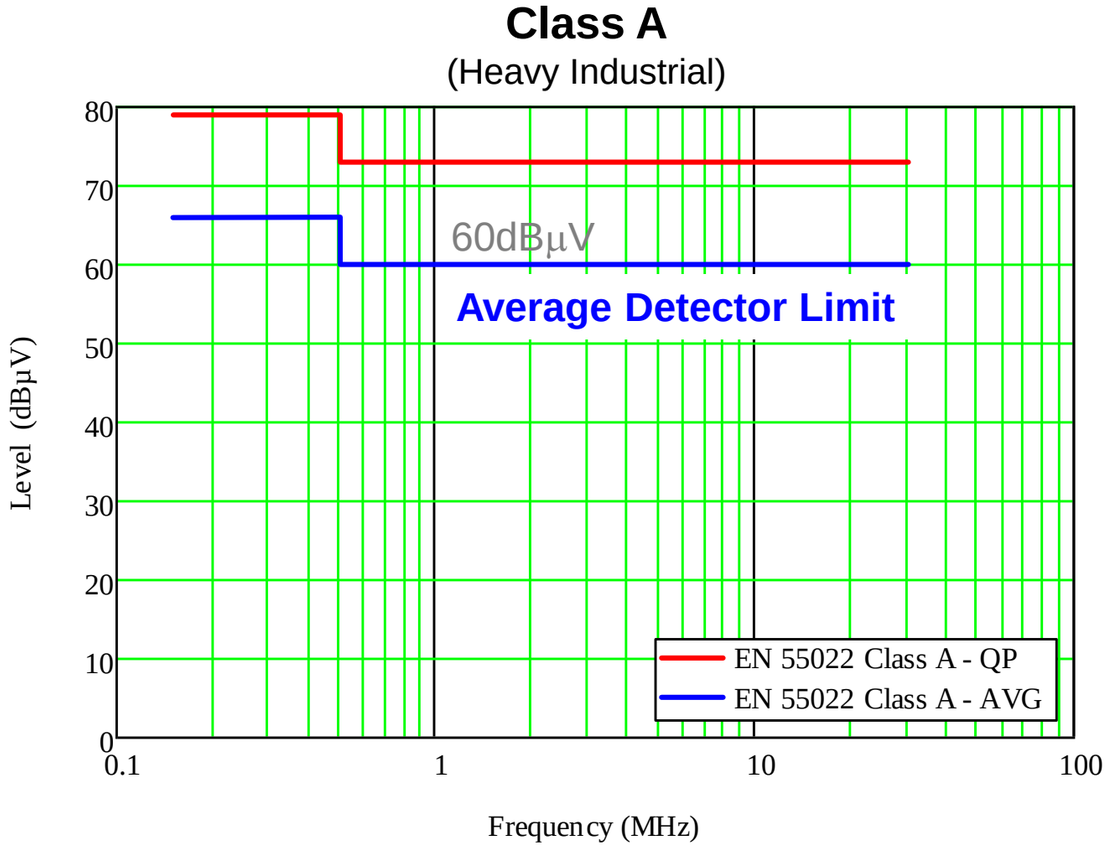
Common-mode noise is like:

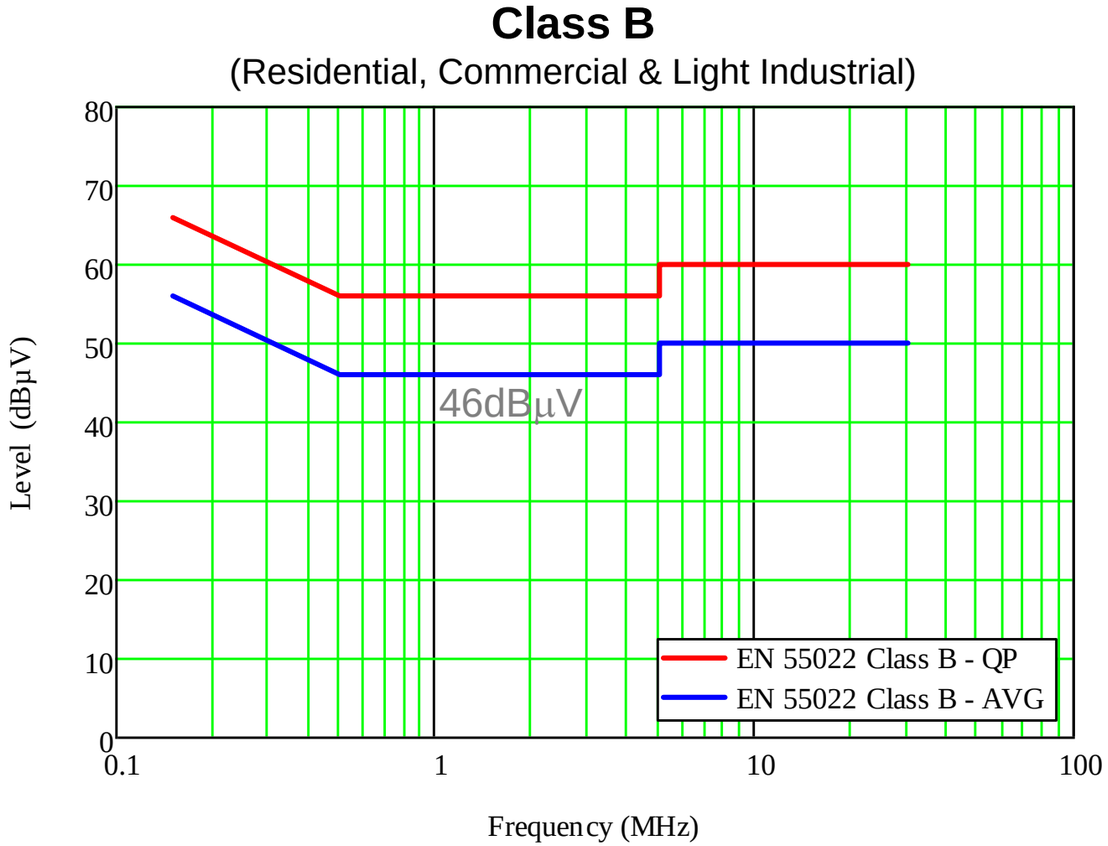
The noise signal on both power wires with same phase.

Can be filtered with Common Mode Choke.

EN55022 limit lines – conducted emissions

Class A and Class B limits, quasi-peak & average, 150kHz–30MHz



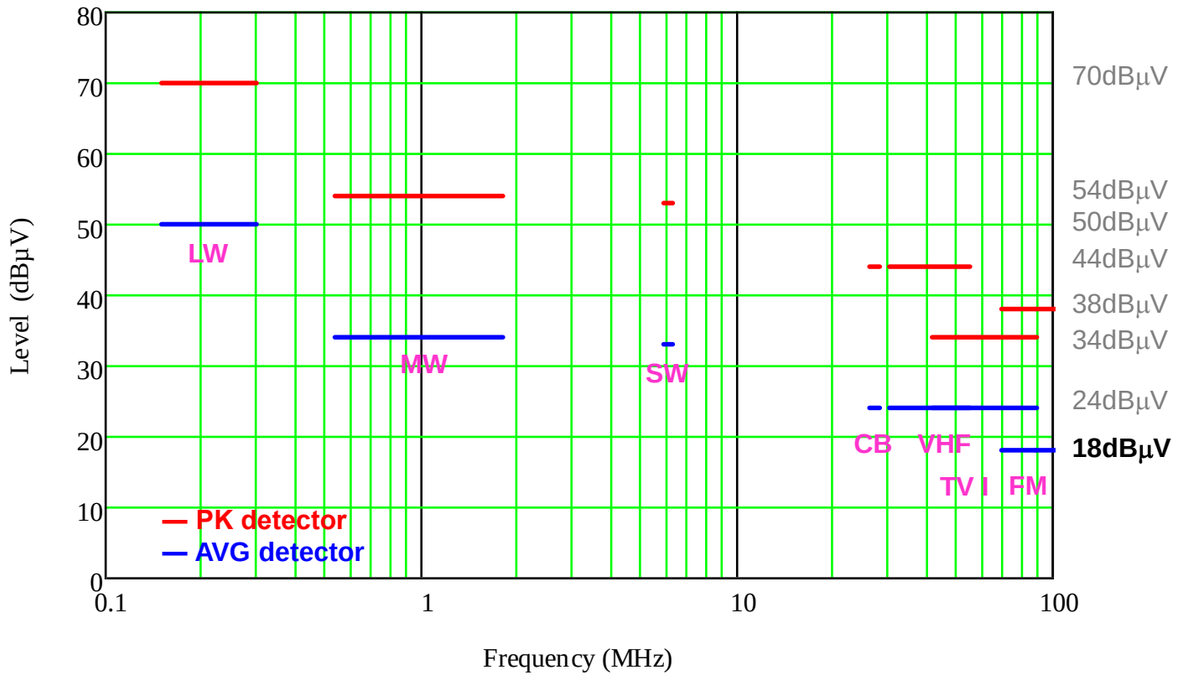


[1] EN55022, 2010, “Information technology equipment– Radio disturbance characteristics– Limits and methods of measurement”

CISPR 25 limits – conducted emissions

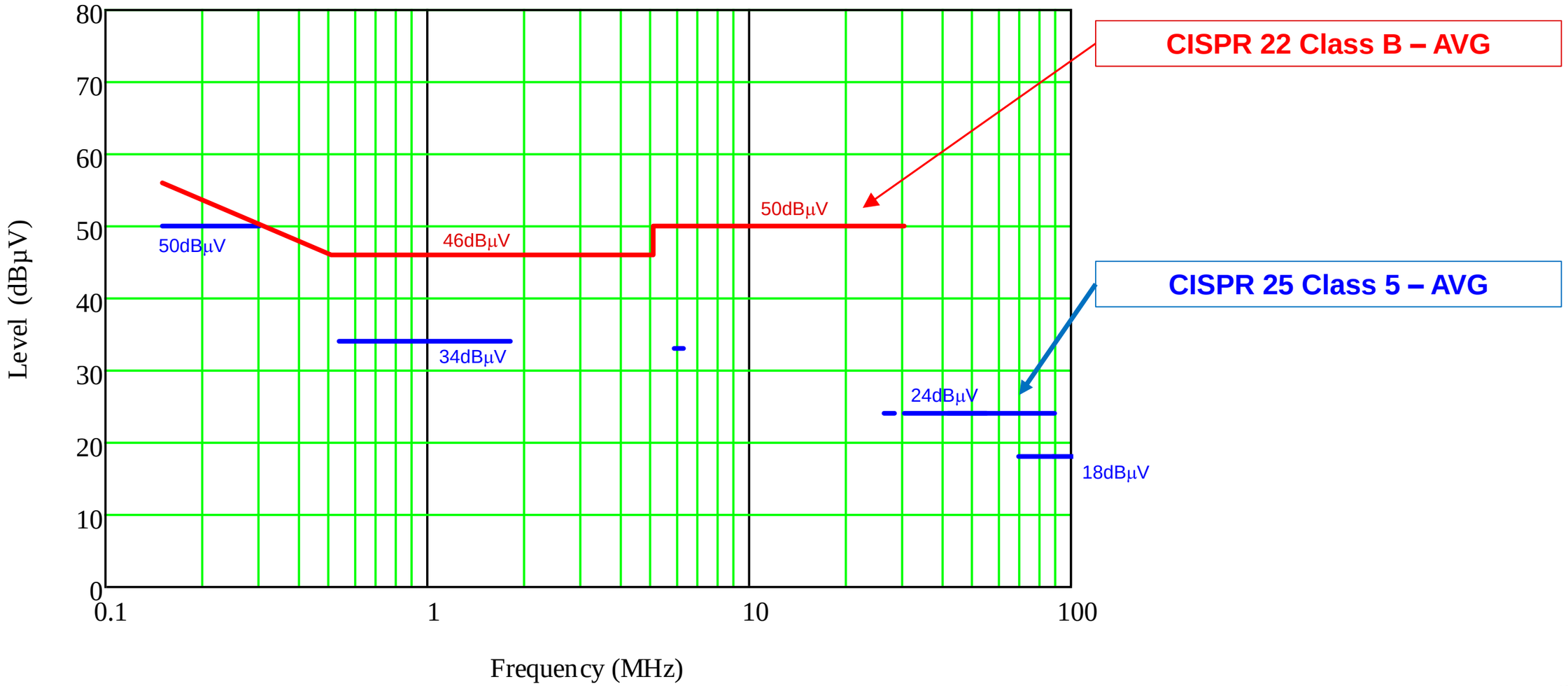
150kHz–108MHz in seven bands for LW, MW, SW, FM, TV-I, CB, VHF

Class 5 limit lines for Peak and Average detectors

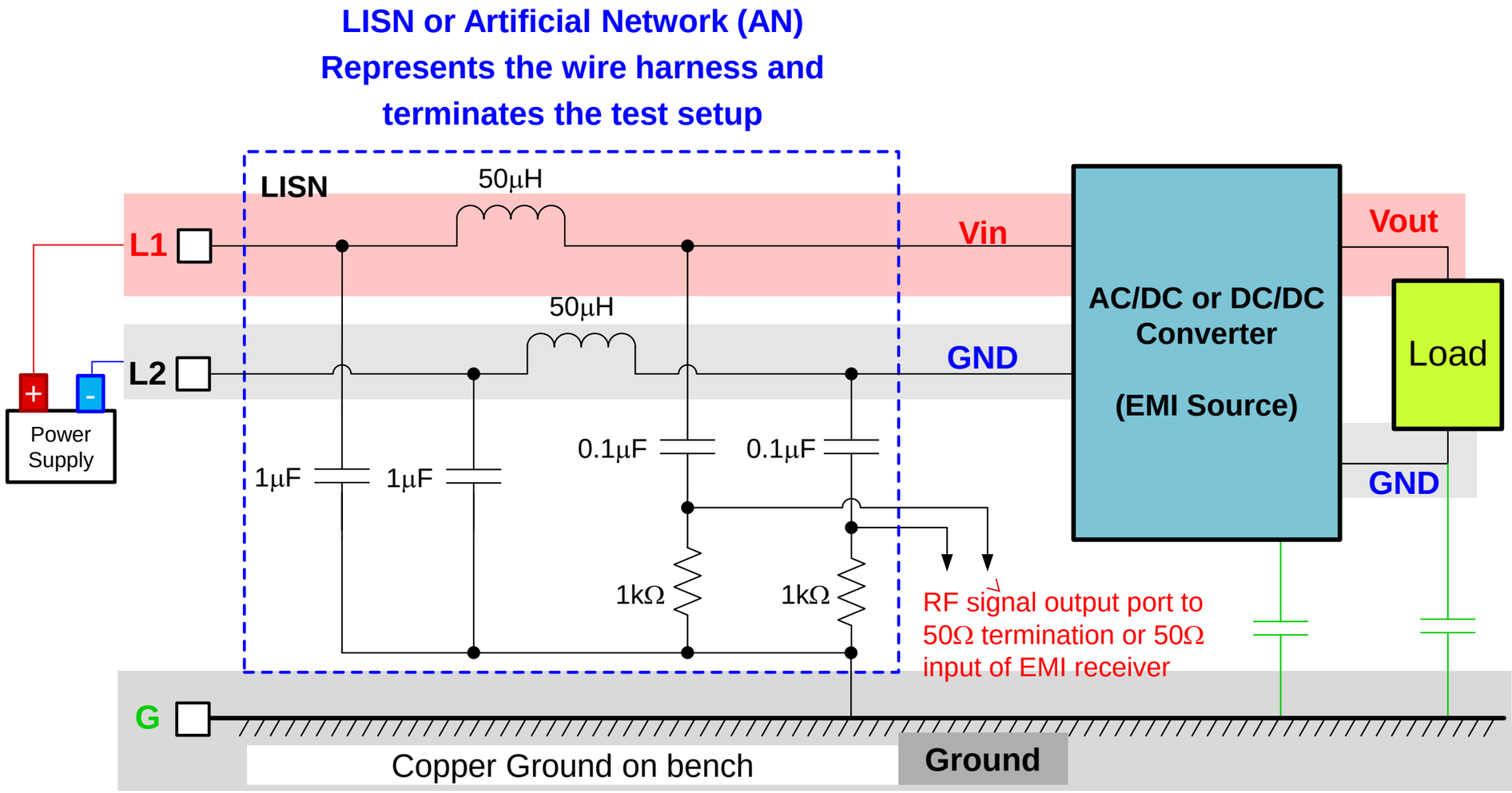


	Band	Frequency (MHz)	PK (dBµV)	QP (dBµV)	AVG (dBµV)
Broadcast	LW	0.15–0.3	70	57	50
	MW	0.53–1.8	54	41	34
	SW	5.9–6.2	53	40	33
	FM	76–108	38	25	18
	TV Band I	41–88	34	–	24
Mobile Services	CB	26–28	44	31	24
	VHF	30–54 68–87	44 38	31 25	24 18

CISPR 22 class B versus CISPR 25 class 5 conducted EMI average limits



Measuring conducted emissions with LISN



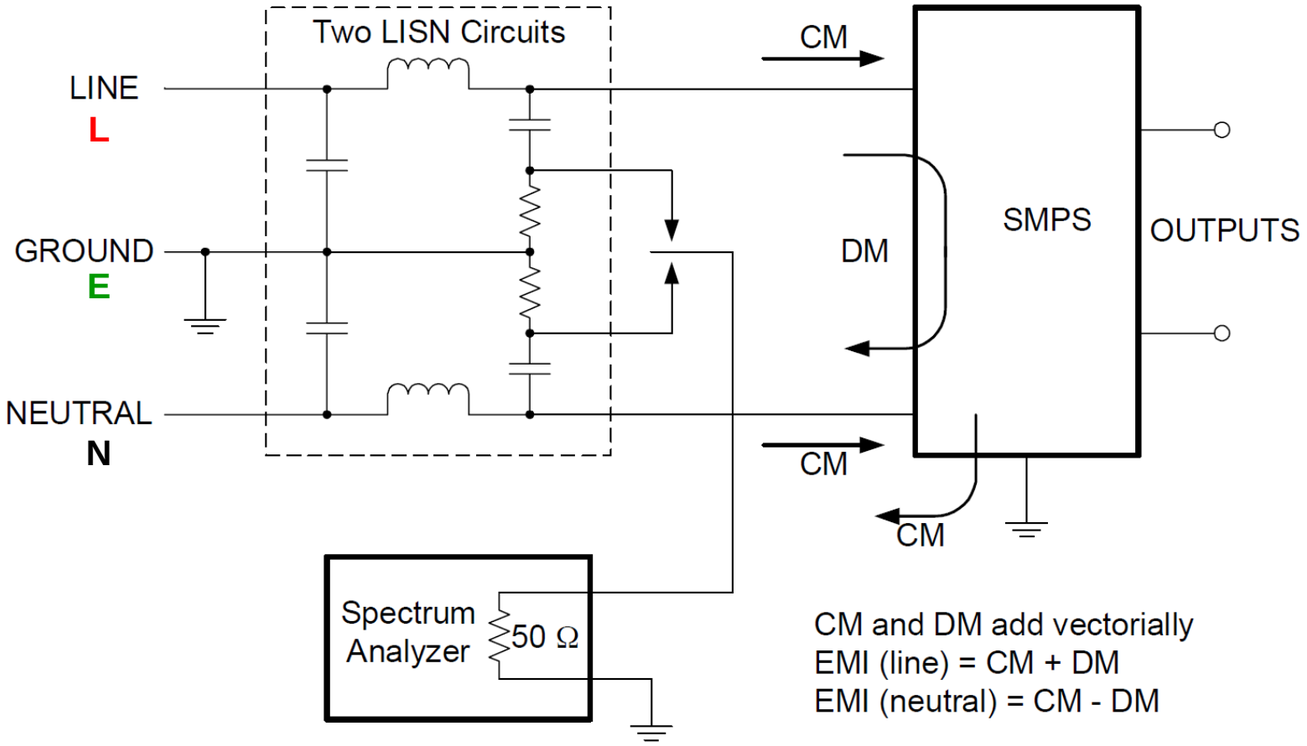
Spectrum Analyzer measures the noise from:

1. **Vin** to **Ground**
2. **GND** to **Ground**

EMI noise currents are very low amplitude

QUESTION:

The **EN55022 Class A** AVG conducted emission limit is **60dBµV** at 10MHz **(Class B is 50dBµV)**. Assuming 50Ω impedance, what is the current level at the conducted emission limit in: (a)µA, (b) dBµA



ANSWER:

$$V_P = V_N = 60\ \text{dB}\mu\text{V} = 10^{-6}\,10^{3}\ \text{V} = 1\ \text{mV}$$

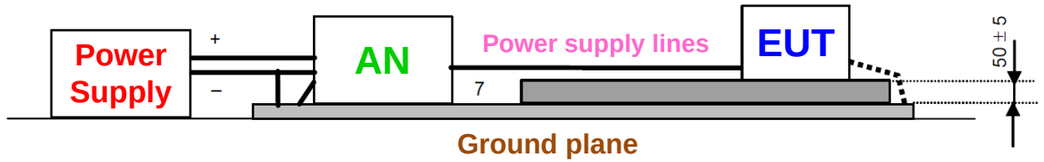
$$V_P = I_P R_L \qquad V_N = I_N R_L \qquad R_L = 50\ \Omega$$

$$I_P = I_N = \frac{1\ \text{mV}}{50\ \Omega} = 20\ \mu\text{A}$$

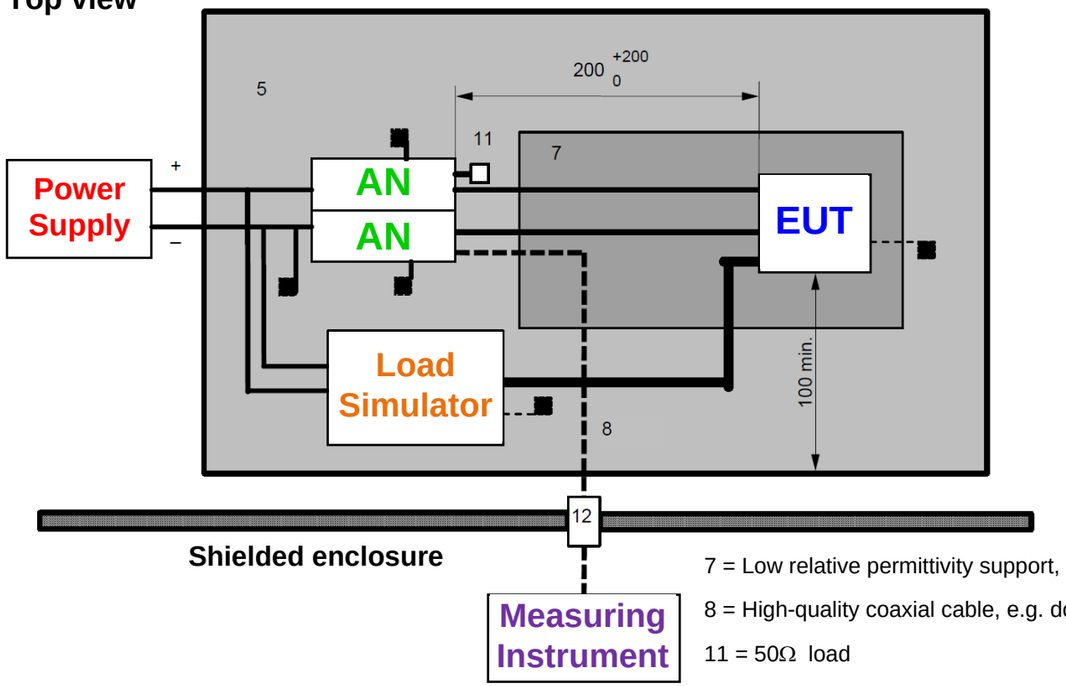
$$I_{P,\text{dB}\mu\text{A}} = I_{N,\text{dB}\mu\text{A}} = 20\log_{10}\left[\frac{20\times10^{-6}}{10^{-6}}\right] = 26.02\ \text{dB}\mu\text{A}$$

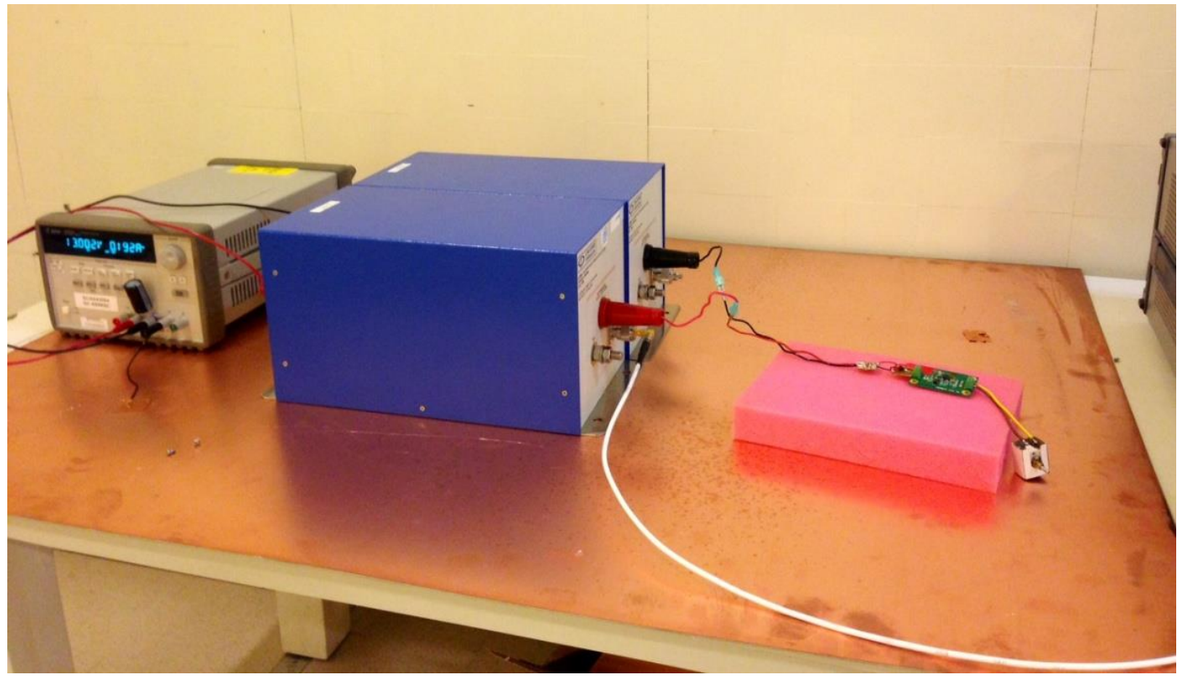
CISPR 25 conducted EMI test setup

Side view



Top view





7 = Low relative permittivity support, $\varepsilon_R < 1.4$

8 = High-quality coaxial cable, e.g. double-shielded 50Ω

11 = 50Ω load

12 = Bulkhead connector

CISPR 25 conducted EMI setup general overview

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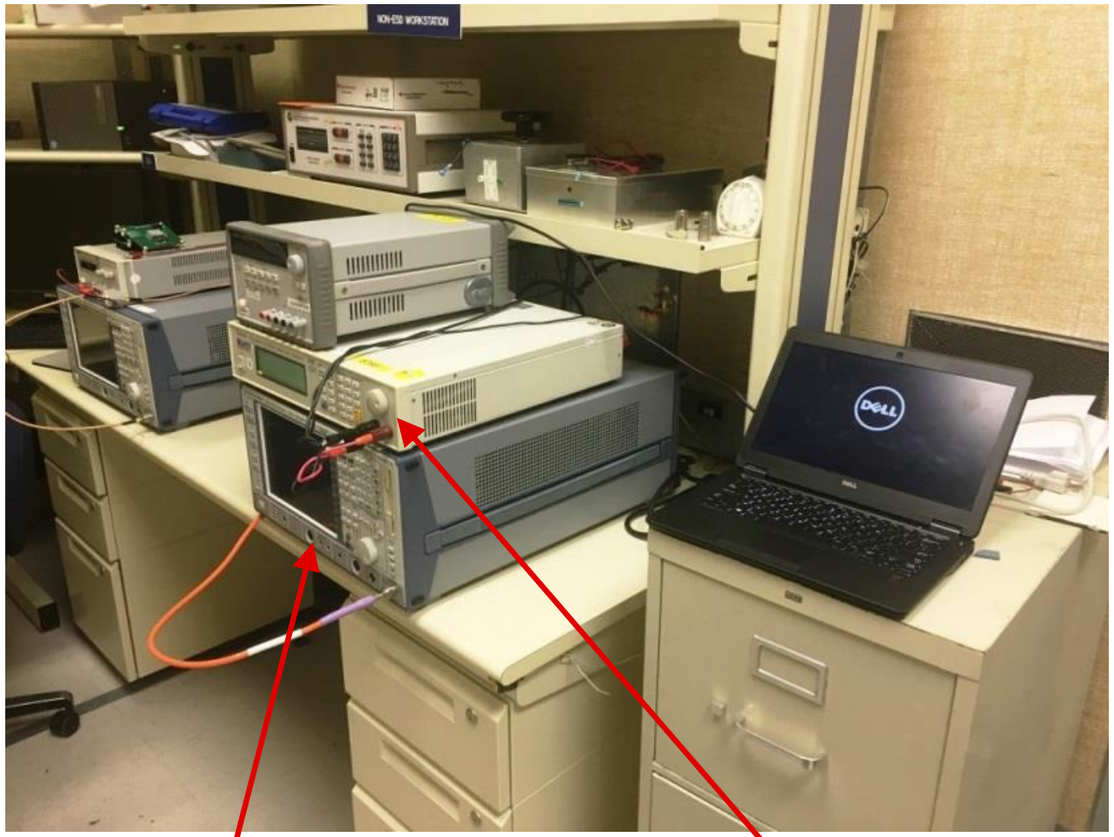
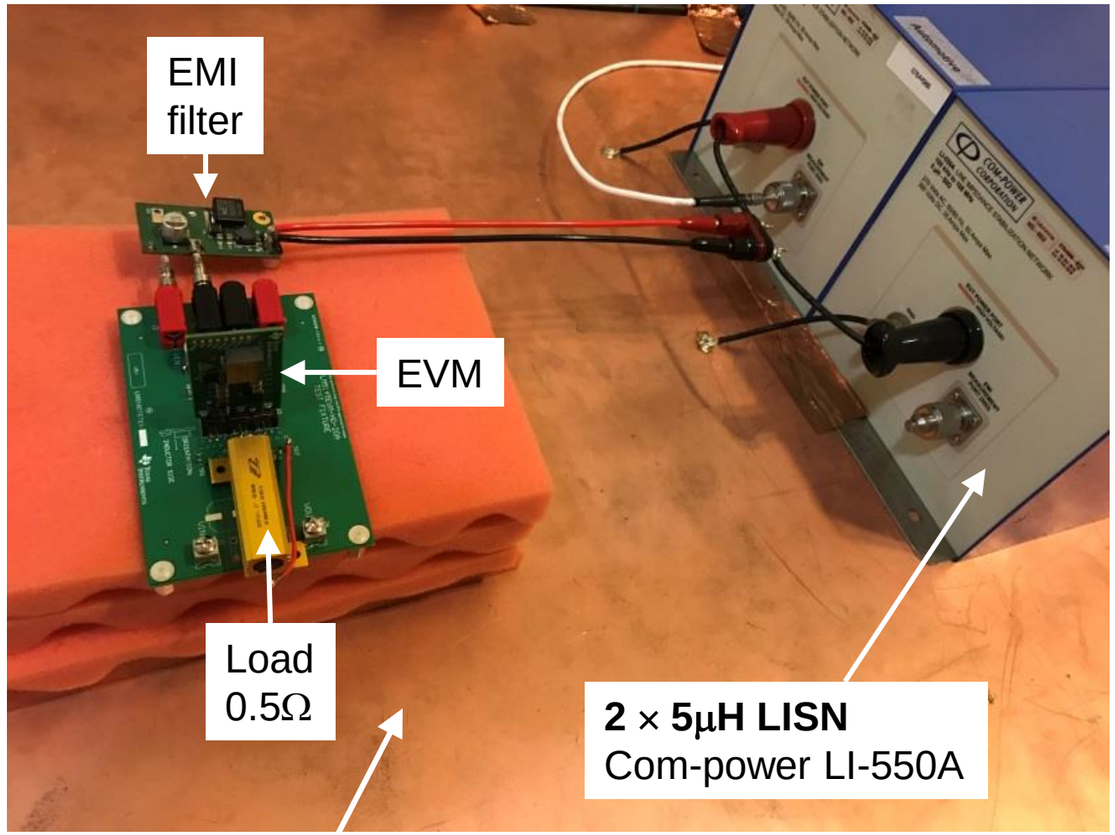
Outside screen room



Spectrum analyzer Power supply, V_{IN} = 13.5V

Inside EMI chamber

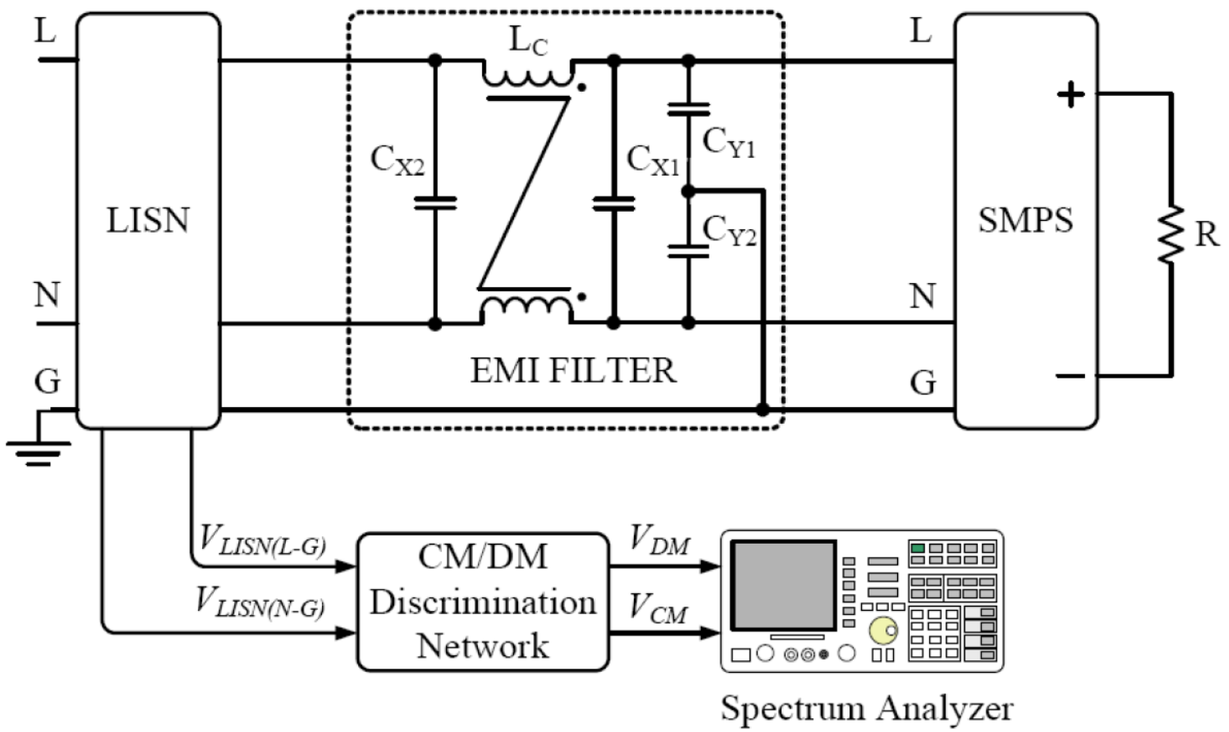


Copper **Ground plane**

Measure conducted emissions (DM & CM) with LISN

Separation of **DM/CM Conducted Emissions**:

1. Diagnosis of power supply conducted EMI
   - **Troubleshoot** source of emissions
   - Distinguish carefully
2. EMI filter design
   - Check if one component (DM or CM) is **dominant**, e.g. in a particular frequency range
   - Directly measure the required DM & CM **attenuation**
   - Minimize filter component count & size for **optimized design**
3. Use DM and CM equivalent circuits
   - Design DM and CM filter stages separately

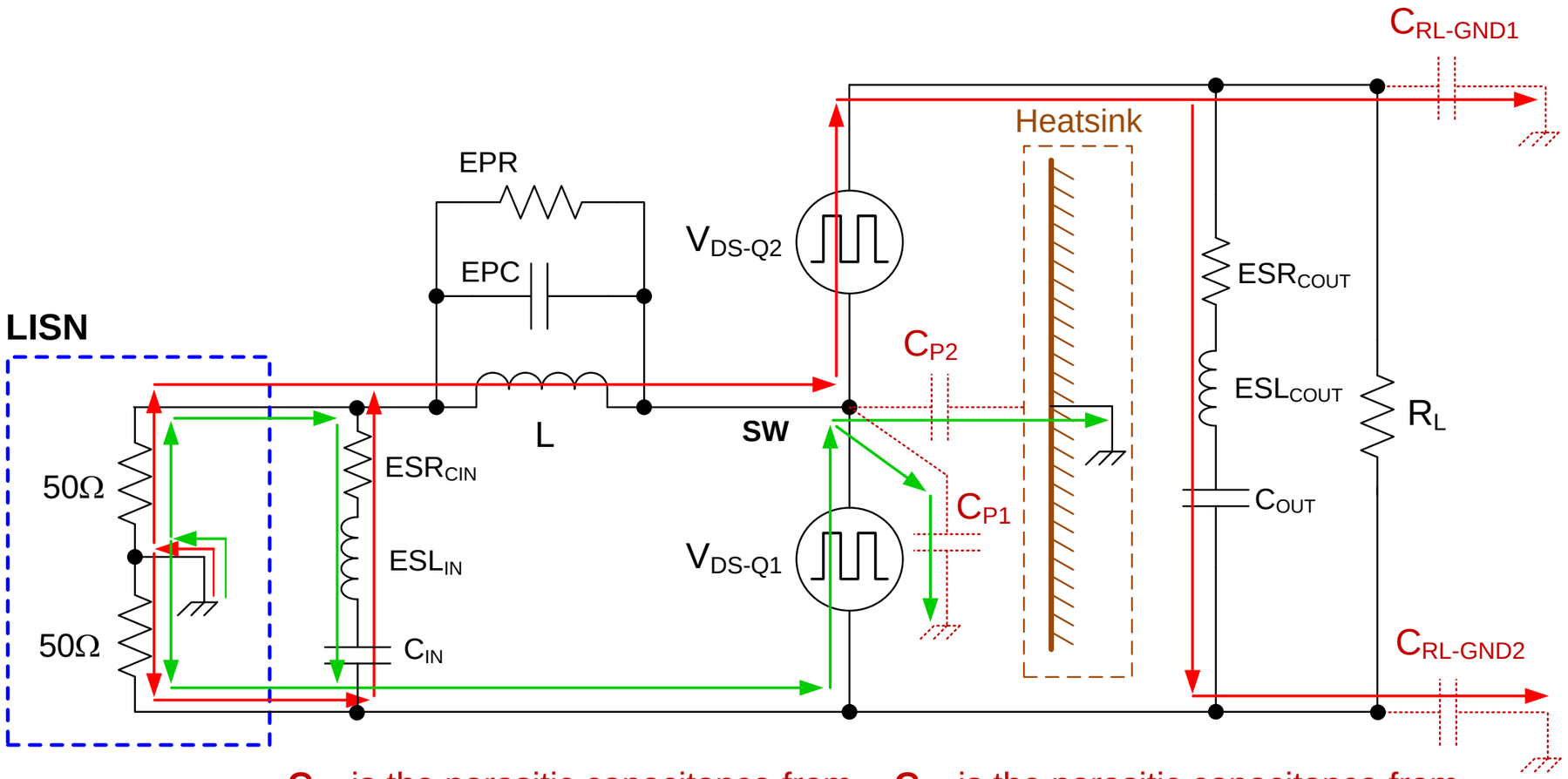


** Need to measure both LISN outputs simultaneously to retain phase information of vectorial quantities **

[3] Kostov et al, “The input impedance of common-mode and differential-mode noise separators,” IEEE Transactions on Industry Applications, May 2015, pp. 2352-2360, http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=6954393

[4] Mainali et al, “Conducted EMI mitigation techniques for switch-mode power converters: a survey,” IEEE Transactions on Power Electronics, Sept 2010, pp. 2344-2356, http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5444974

Automotive sync boost converter CM noise curent



C_{RL-GND} is the parasitic capacitance from Load to chassis GROUND

e.g. long load lines, downstream DC/DC, motor drive systems, metal-clad load resistors

C_{P1} is the parasitic capacitance from SW to chassis GROUND

C_{P2} is the parasitic capacitance from SW to grounded heatsink (large area)

[5] D. Han et al., "A case study on common mode electromagnetic interference characteristics of GaN HEMT and Si MOSFET power converters for EV/HEVs," IEEE Transactions on Transportation Electrification, March 2017, pp. 168-179, http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7707424

EMI Sources
Circuit & Layout Techniques to Reduce EMI & Voltage Stress

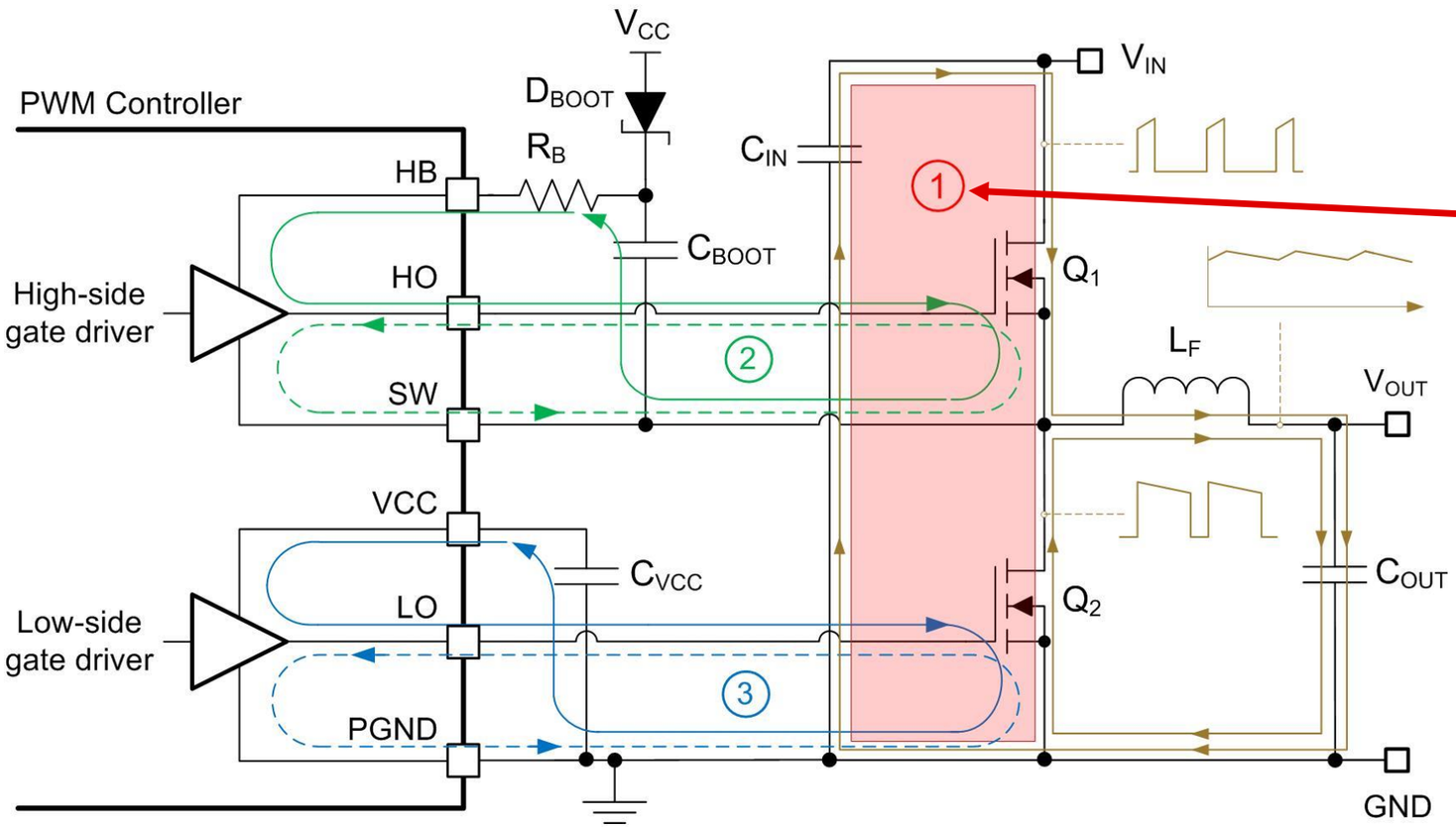
Critical switching loops, component parasitic

Minimizing inductive parasitic

EMI sources & related frequency ranges / relevant harmonics

Equivalent circuits for SW node ringing

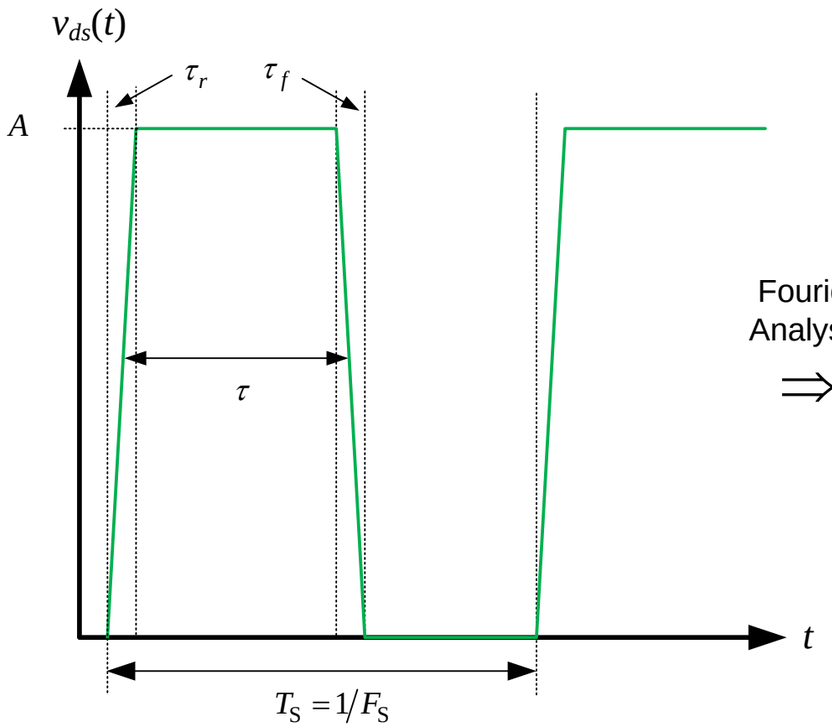
Identify critical loops with high di/dt currents



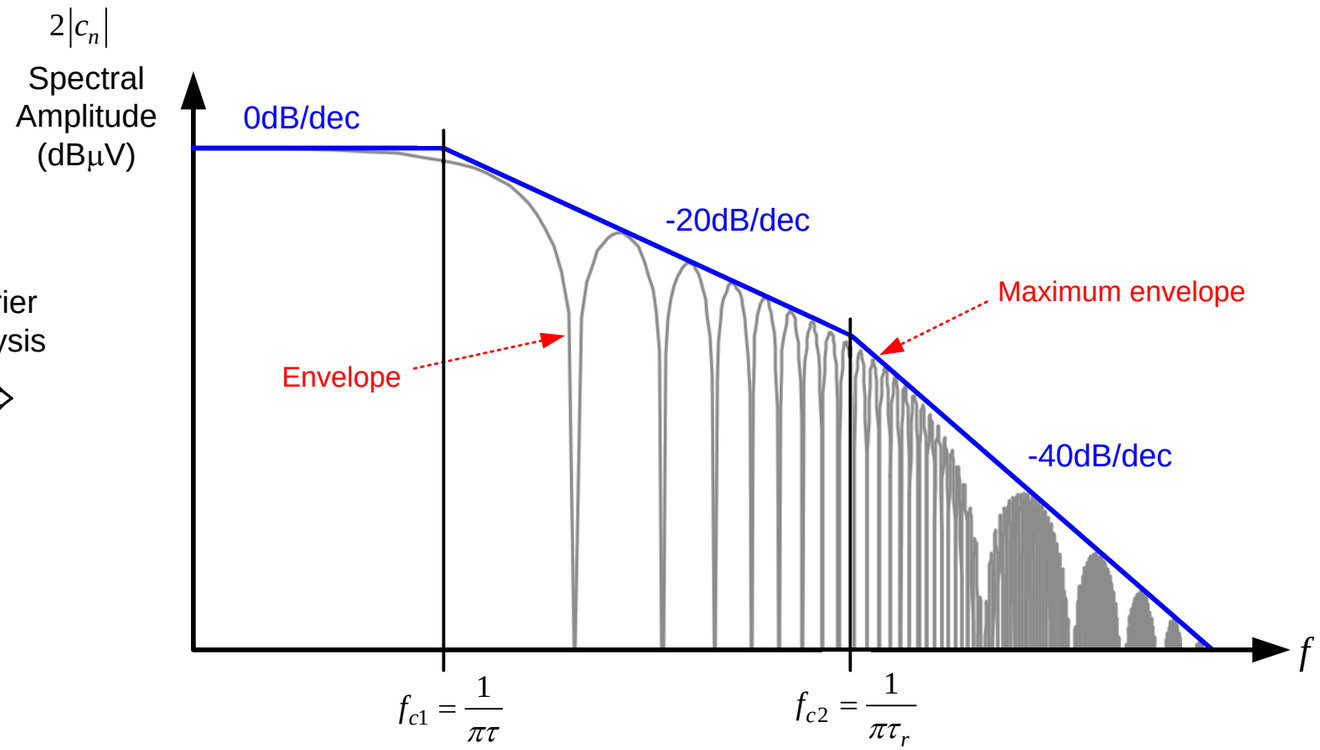
High frequency "power loop"
…critical path area reduction

In translating a converter schematic to a board layout, it's essential to pinpoint the high slew-rate current (**high di/dt**) **loops** to recognize the layout-induced **parasitic or stray inductances** that cause excessive **noise, overshoot, ringing and ground bounce.**

SW node voltage waveform & spectral envelope



Fourier Analysis ⇒

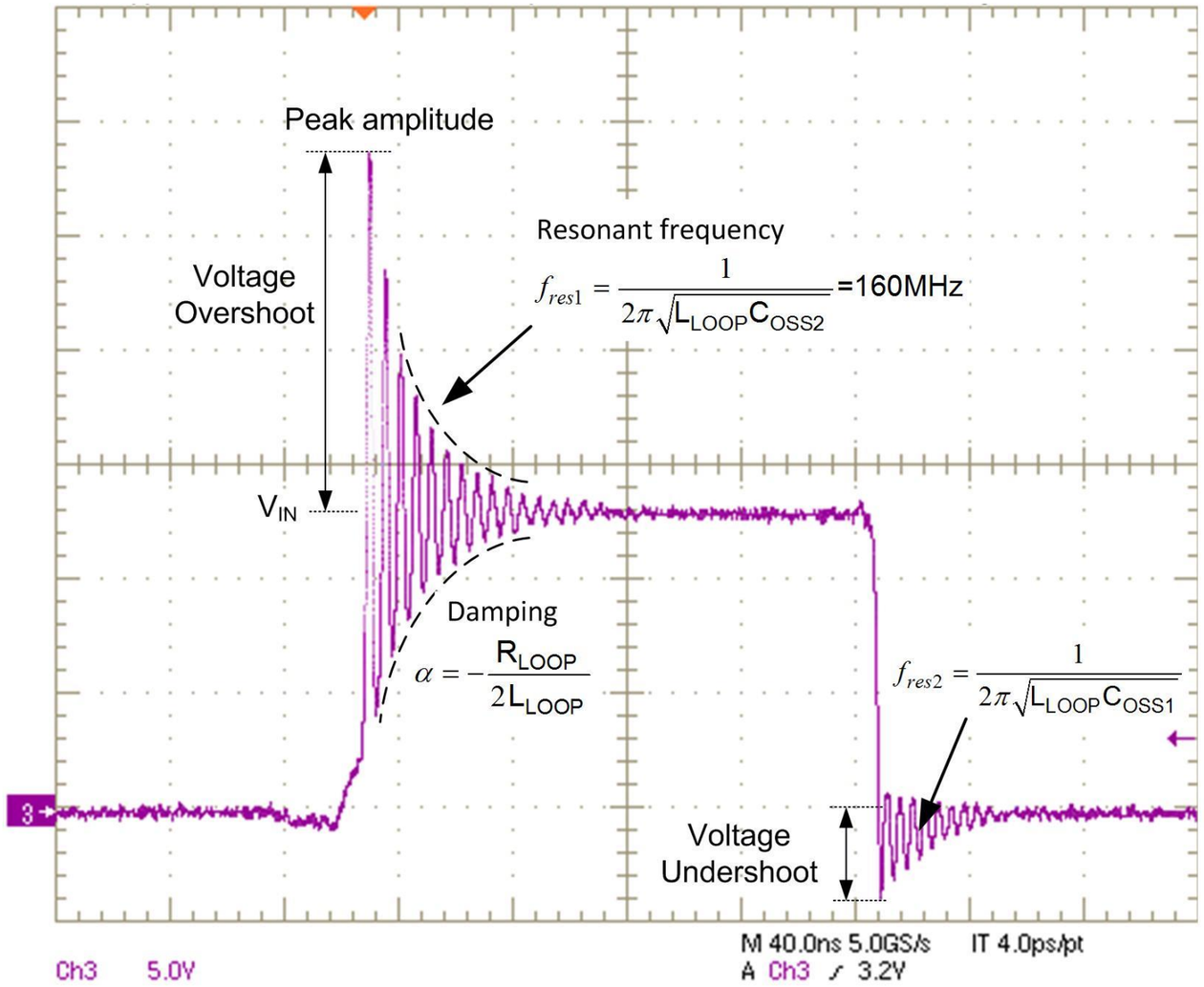


τ = pulse width (measured at half-maximum)
T_S = pulse period
D = duty cycle = τ / T_S
τ_r = rise time; τ_f = fall time of edge transition

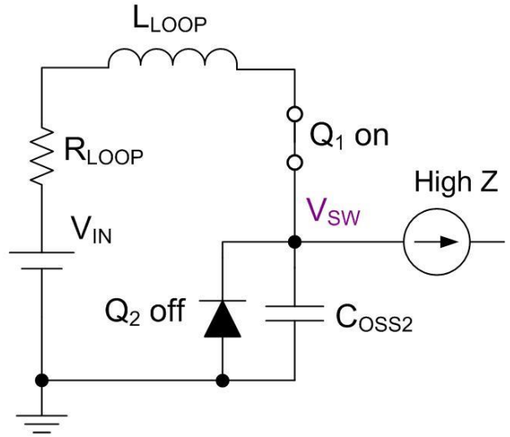
$$|c_n| = A\frac{\tau}{T_S}\left|\text{sinc}\left(n\omega_o\frac{\tau}{2}\right)\right|\left|\text{sinc}\left(n\omega_o\frac{\tau_r}{2}\right)\right|$$

[8] N. Oswald et al., “Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation,” IEEE Transactions on Industry Applications, Sept 2014, pp. 2154-2165, http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5953506

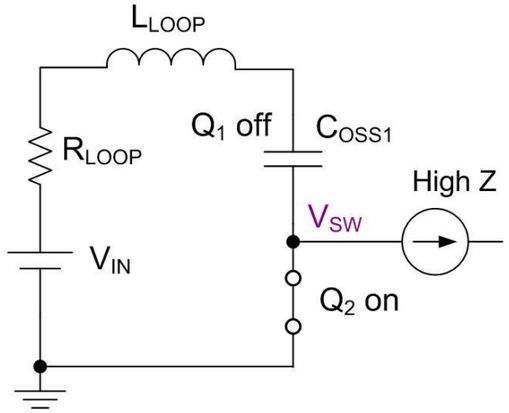
Equivalent RLC circuits for SW node ringing – buck



Equivalent RLC circuit after Q_1 turns **ON**



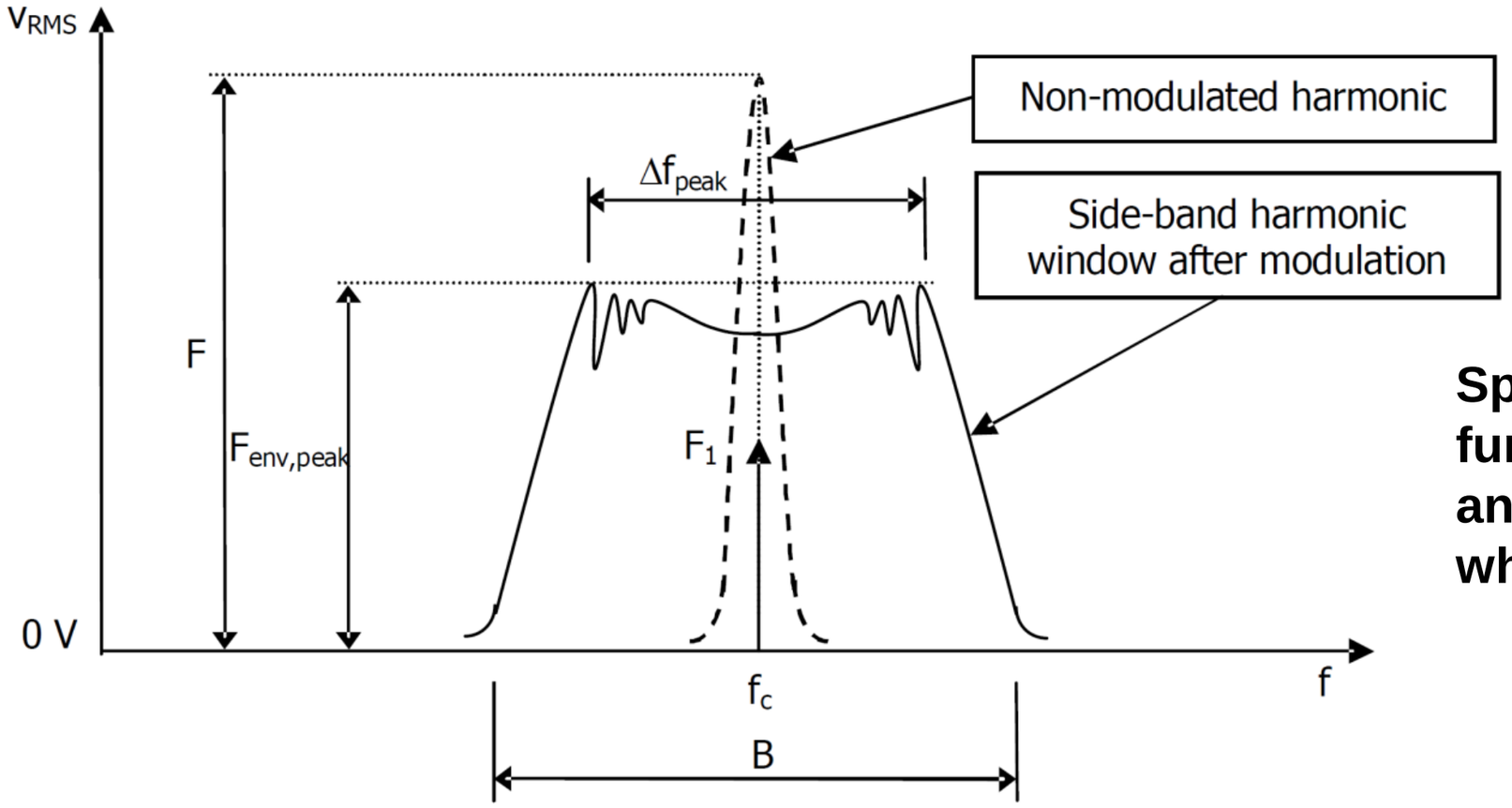
Equivalent RLC circuit after Q_1 turns **OFF**



Spread spectrum / dithering – what is it?

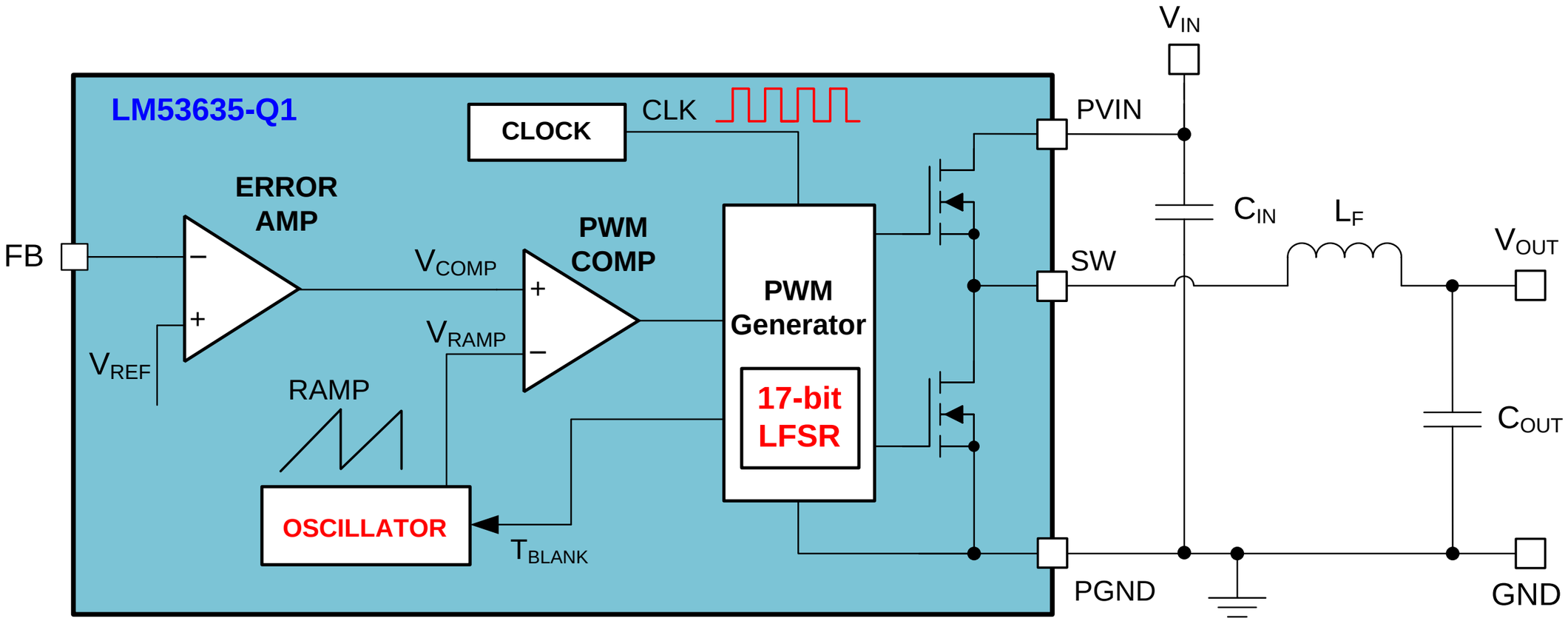
Spread spectrum is a technique to reduce EMI by dithering the switching frequency

e.g. LM53635-Q1, ΔF_{SW} = ±3%; LM5175-Q1, ΔF_{SW} = ±5%; LM5141-Q1, ΔF_{SW} = ±5%



Spread spectrum reduces the fundamental signal energy and the overall peak value while widening the spectrum

Spread spectrum implementation



17-bit **linear feedback shift register (LFSR)** generates 2^{17} random codes, passed to the oscillator

Oscillator generates **pseudo-random** current depending on code from LFSR

Overspread in switching frequency, $\Delta F_{SW} = \pm 3\%$

Mitigating EMI by PCB layout

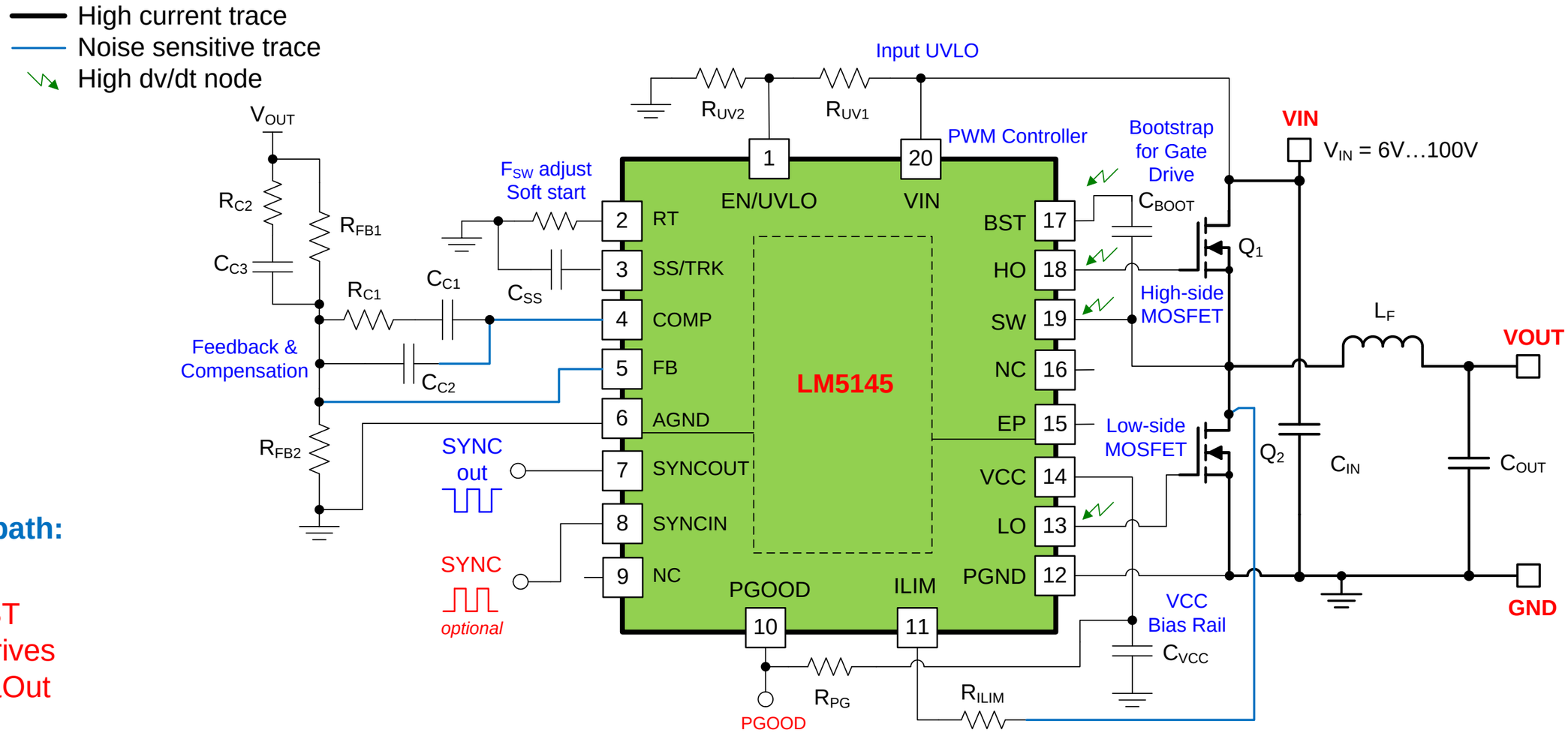
Power stage layout	
1	Component selection and floor-planning of the MOSFETs, decoupling capacitors, and shunt resistor should target absolute smallest area and circumference of “hot” loops.
2	Reduce power loop parasitic inductance, including partial inductances from the MOSFET packages, decoupling capacitor, shunt resistor, and PCB interconnections, as it leads to voltage overshoot, ground bounce, ringing, EMI, and power loss.
3	With a power loop configured for horizontal current flow, add a close (6 mil spacing) GND plane on the layer immediately underneath to act as a shield layer for H-field self-cancellation and reduced parasitic inductance.
4	Connect multiple decoupling capacitors in parallel to reduce ESR and ESL, optimize placement for flux cancelation.
5	SW node copper area is a tradeoff between managing dv/dt-related noise and providing acceptable heatsinking for the low-side MOSFET. Large planes with high AC voltage become transmit and receive antenna structures for radiated EMI. Use shielding techniques around the SW node to minimize electric field coupling.
6	Route tightly-coupled MOSFET gate and source (return) traces on inner layers that are shielded by GND planes above and below; use via stitching for 3-D Faraday shielding effect.
7	Locate SW node snubber network and anti-parallel Schottky diode for deadtime conduction extremely close to the synchronous FET.
8	Separate the inductor terminals’ copper pours to avoid increasing the inductor’s equivalent parallel capacitance (EPC), decreasing its self-resonant frequency (SRF).

EMI Mitigation in DC/DC Converters

LM5145: Communications systems
LM53635-Q1: Automotive

“Local” EMI control (PCB layout) is less cost than EMI filtering

LM5145 Buck – Identify high dV/dt path

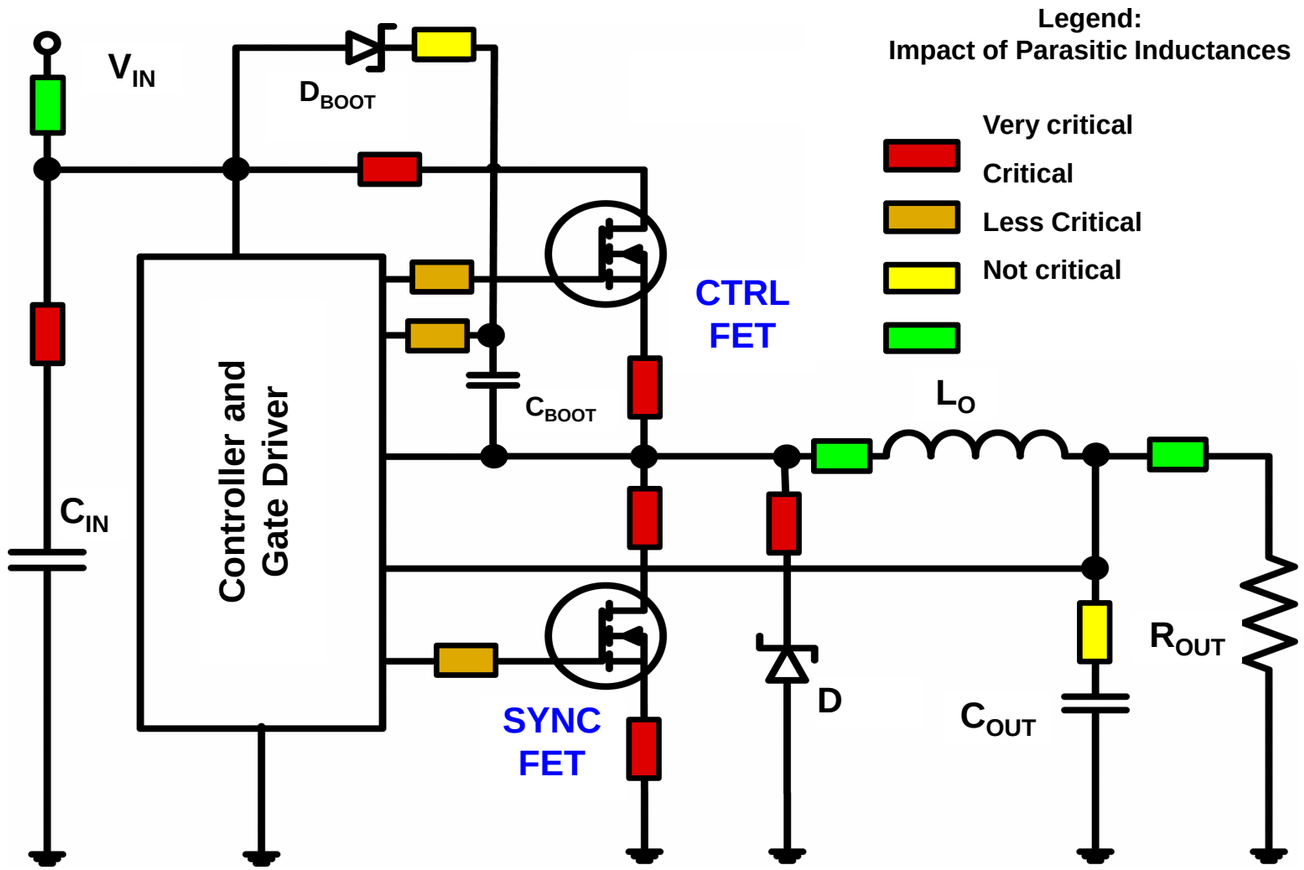


High dV/dt path:

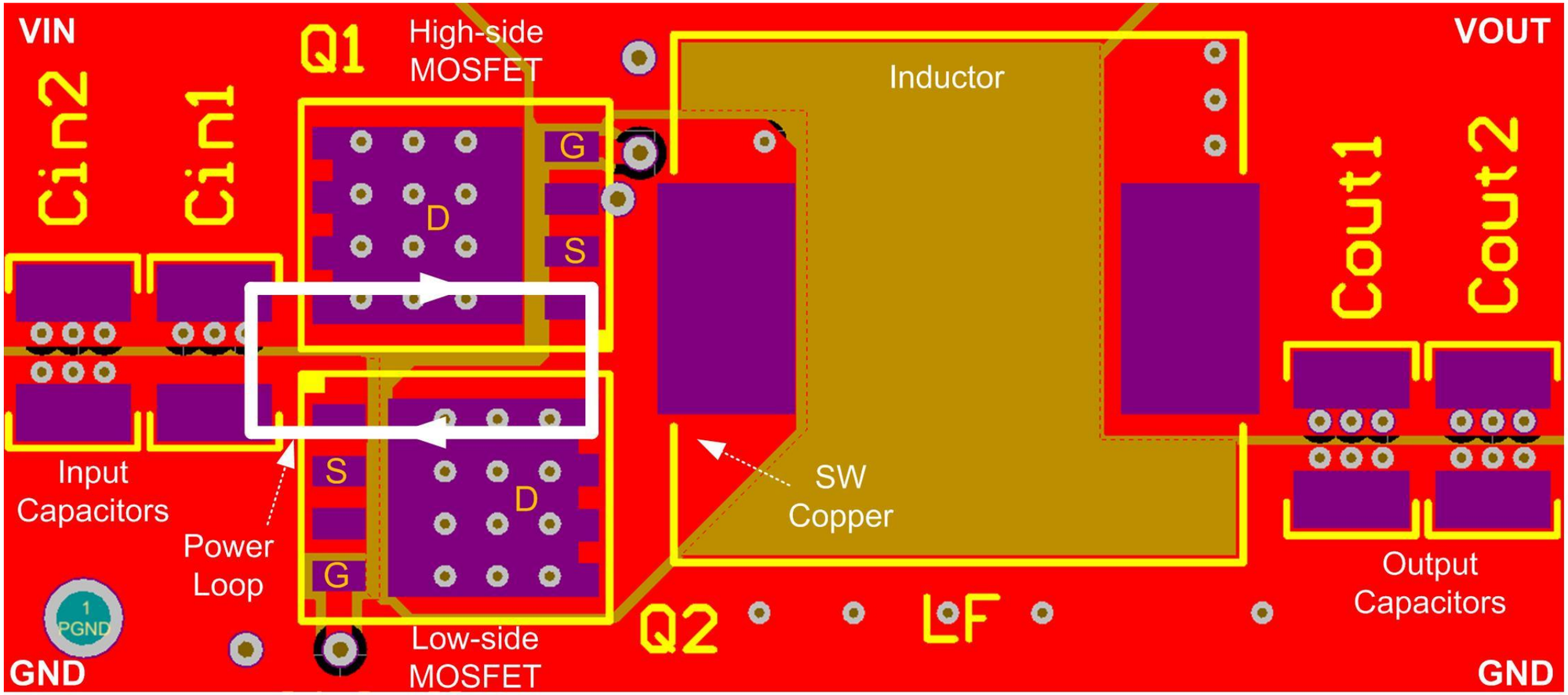
1. Switch
2. Cboot, BST
3. HO, LO drives
4. SYNC In&Out

Review critical parasitic inductances

In translating a converter schematic to a board layout, one essential step is to identify the high slew-rate current loops and recognize the layout-induced parasitic or stray inductances that cause excessive noise, overshoot, ringing and ground bounce.



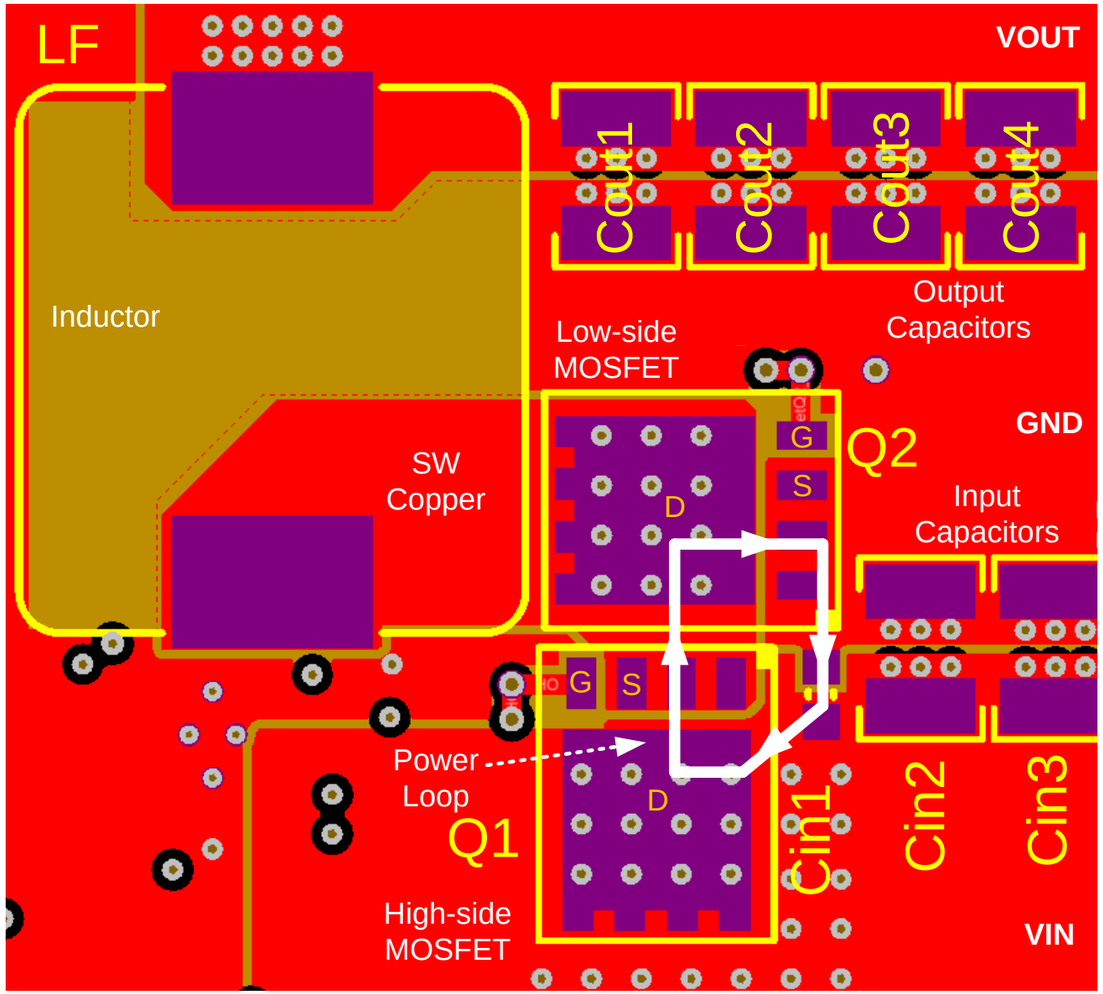
PCB layout LM5145 sync buck controller

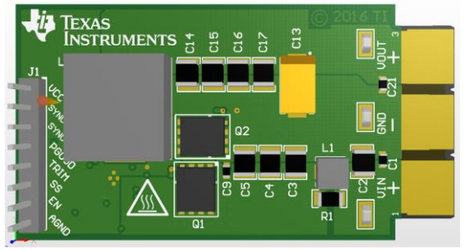


Legend

- Top Layer Copper
- Layer 2 GND Plane
- Top Solder

PCB layout LM5145 sync buck controller





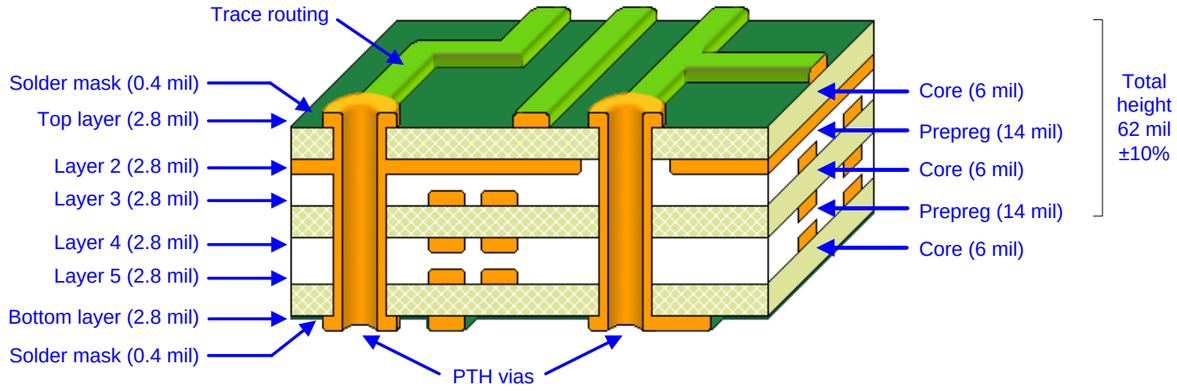
Layout modification

Rotate high-side MOSFET Q1 90°

Add **0603 input cap**, Cin1

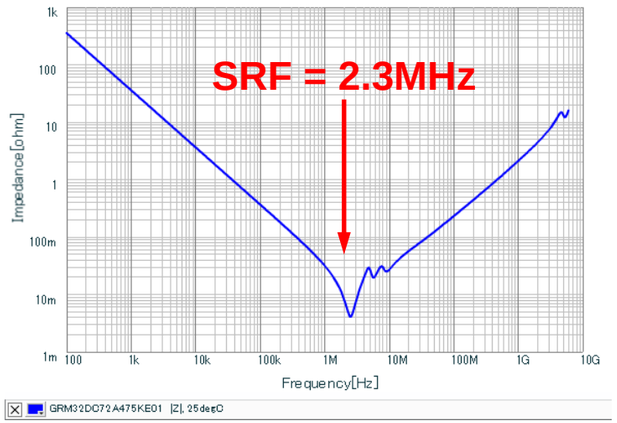
- ✓ 10nF, 100V, 0603, X7R
- ✓ 77MHz SRF (Self-Resonant Frequency)
- ✓ Smaller high-frequency power loop area

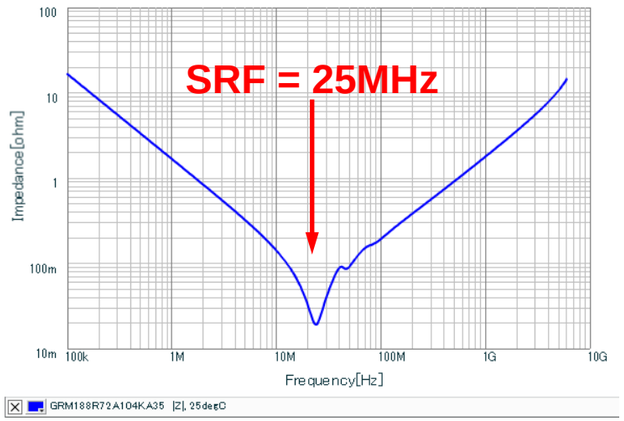
Specify PCB stack-up with **6-mil spacing** top layer to L2 GND plane

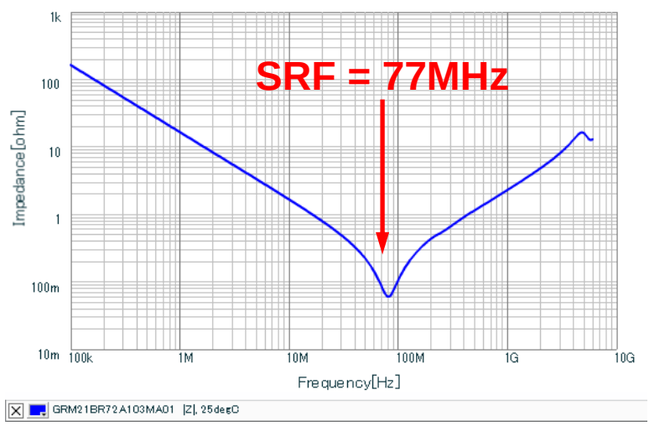


Legend Top Layer Copper | Layer 2 GND Plane | Top Solder

Input caps – 4.7µF 1210 and 10nF 0603 in parallel







4.7µF, 100V, X7S, 1210

SRF = 2.3MHz (Z_C = 4mΩ)

ESL = 0.4nH

Z_C = 237mΩ @ 100MHz

0.1µF, 100V, X7R, 0603

SRF = 25MHz (Z_C = 20mΩ)

ESL = 0.35nH

Z_C = 195mΩ @ 100MHz

10nF, 100V, X7R, 0603

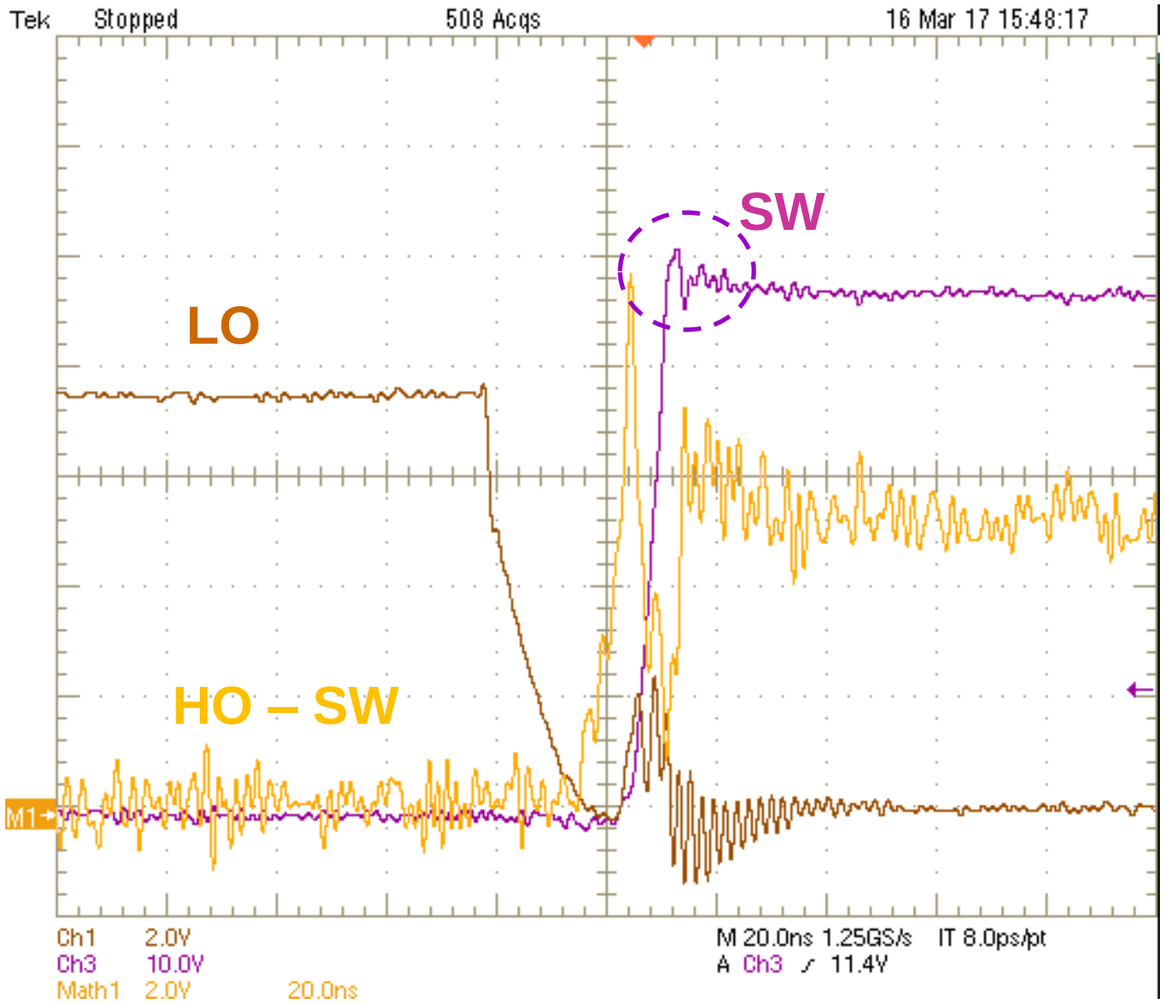
SRF = 77MHz (Z_C = 60mΩ)

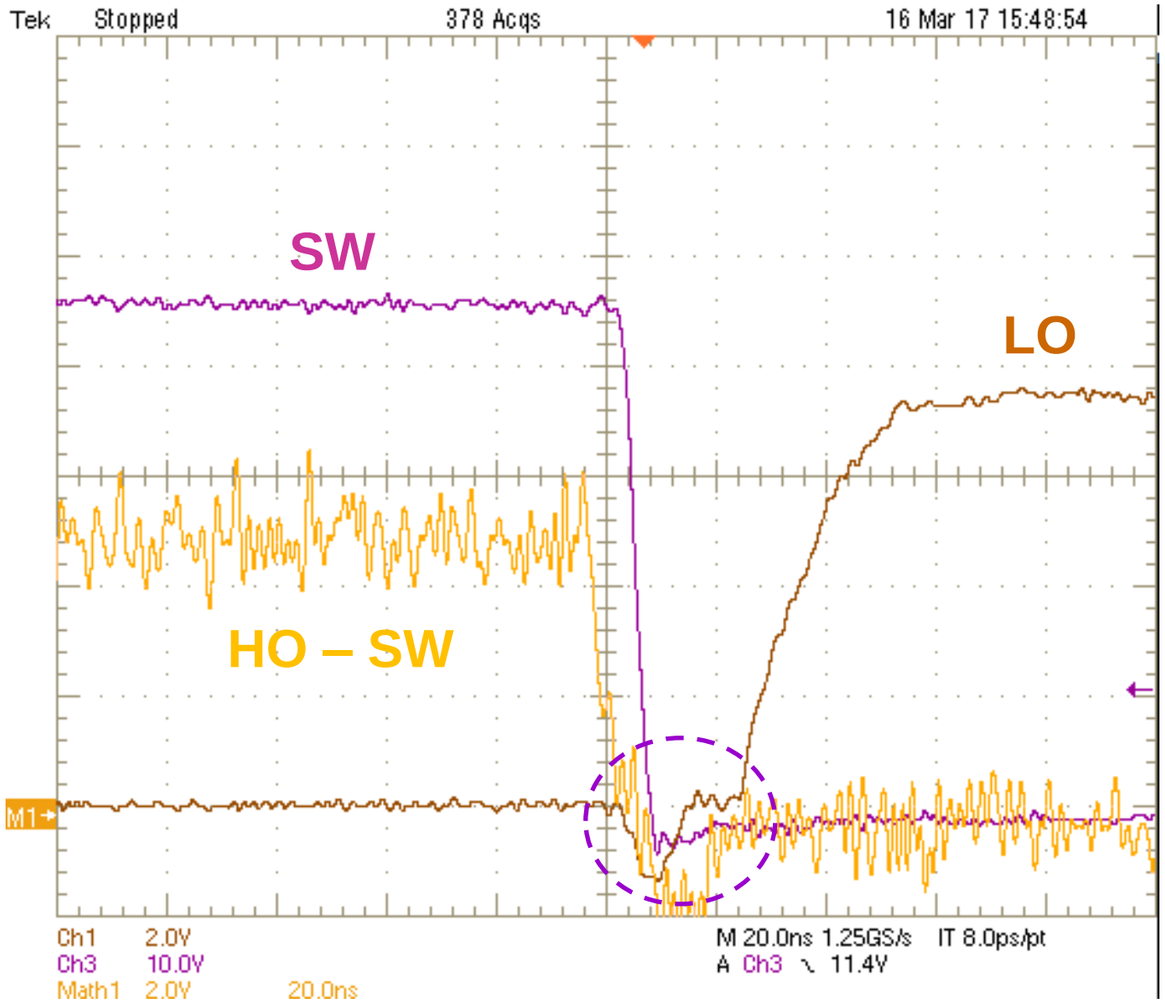
ESL = 0.33nH

Z_C = 110mΩ @ 100MHz

[9] Murata Simsurfing tool, http://ds.murata.co.jp/software/simsurfing/en-us/index.html

SW node waveforms, VIN = 48V, VOUT = 5V, IOUT = 10A





Inductors with improved e-field signature

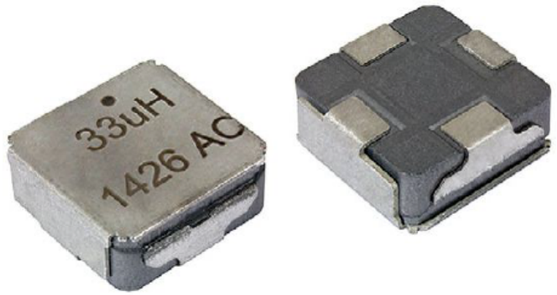
VISHAY

www.vishay.com

IHLE-4040DD-5A

Vishay Dale

Low Profile, High Current Inductors with e-field Shield



Manufactured under one or more of the following:
US Patents; 6,198,375/6,204,744/6,449,829/6,460,244.
Several foreign patents, and other patents pending.

FEATURES

- High temperature, up to 155 °C
- Integrated E-Shield for maximum EMI reduction (1)
- Excellent DC/DC energy storage up to 1 MHz to 2 MHz. Filter inductor applications up the SRF (see Standard Electrical Specifications table).
- Integrated e-field shield eliminates need for separate shielding
- 20 dB e-field reduction at 1 cm
  - Measured vertically from top center of device
- Lowest DCR/µH, in this package size
- Handles high transient current spikes without saturation
- Coplanarity of the 4 terminals ≤ 100 µm
- AEC-Q200 qualified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

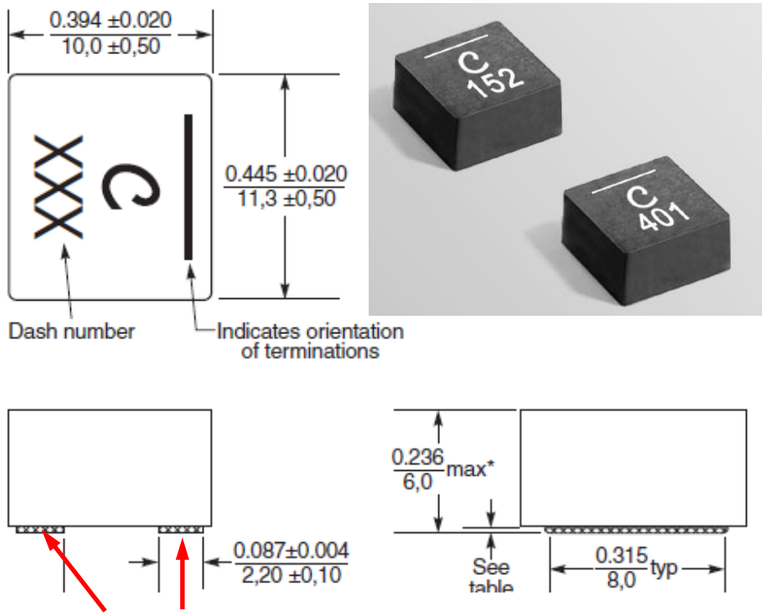
RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

Note

(1) Maximum e-field reduction is realized with the IHLE shield is connected to ground.

Shielded Power Inductors – XAL1060



No vertical sidewall terminals (exposed metal) minimizes e-field coupling

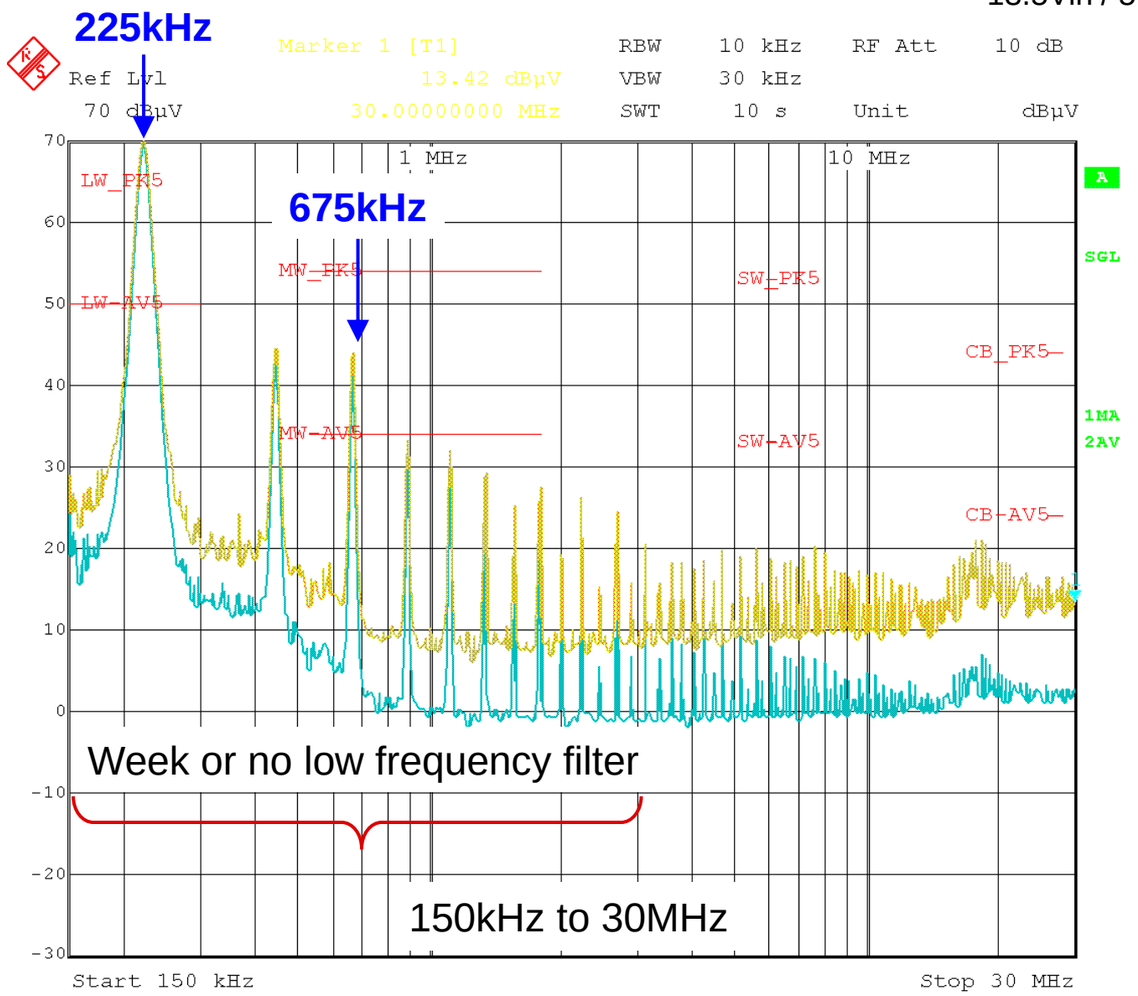
PCB layout guidelines for buck controller
Designing for lowest EMI

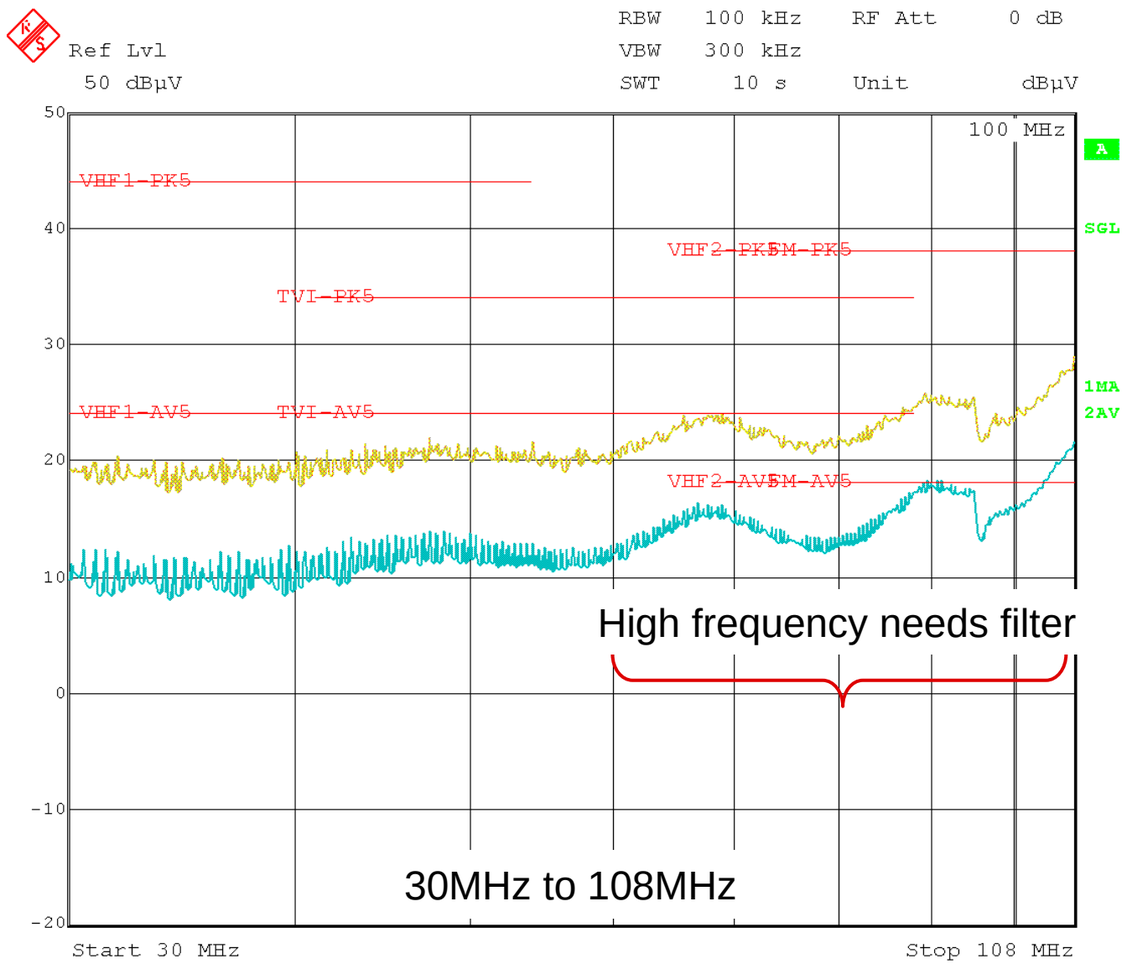
TECH DAYS
Texas Instruments

1. **Input & output caps**
   - Bypass VIN to GND with multiple low-ESR ceramic caps of X7R dielectric
   - Place C_{IN} as close as possible to the MOSFETs VIN and GND connections
   - Minimize the **loop area** formed by C_{IN} terminals and the MOSFETs
   - Ground return paths for both C_{IN} & C_{OUT} should consist of localized top-side planes that connect to the GND plane
2. **Inductor**
   - Locate the inductor close to the MOSFETs (SW node) and connect **dotted terminal** to SW
   - Minimize the area of the SW trace/polygon to reduce **e-field coupling**
   - Use GND plane shielding around SW with “3D” via stitching
3. **Ground plane**
   - Use **full 2-oz copper ground plane on layer 2** immediately (**6 mils**) under the power stage
   - Provides H-field cancellation & noise shielding, reduced “loop” inductance, better thermals
4. **Gate drives**
   - Route high-side gate drive traces as diff pair (HO and SW together)
   - Route gate drive traces short and direct, preferably on **inner PCB layer for shielding**

LM5145 EVM – Conducted EMI without EMI filter

13.5Vin / 5Vout @ 10A



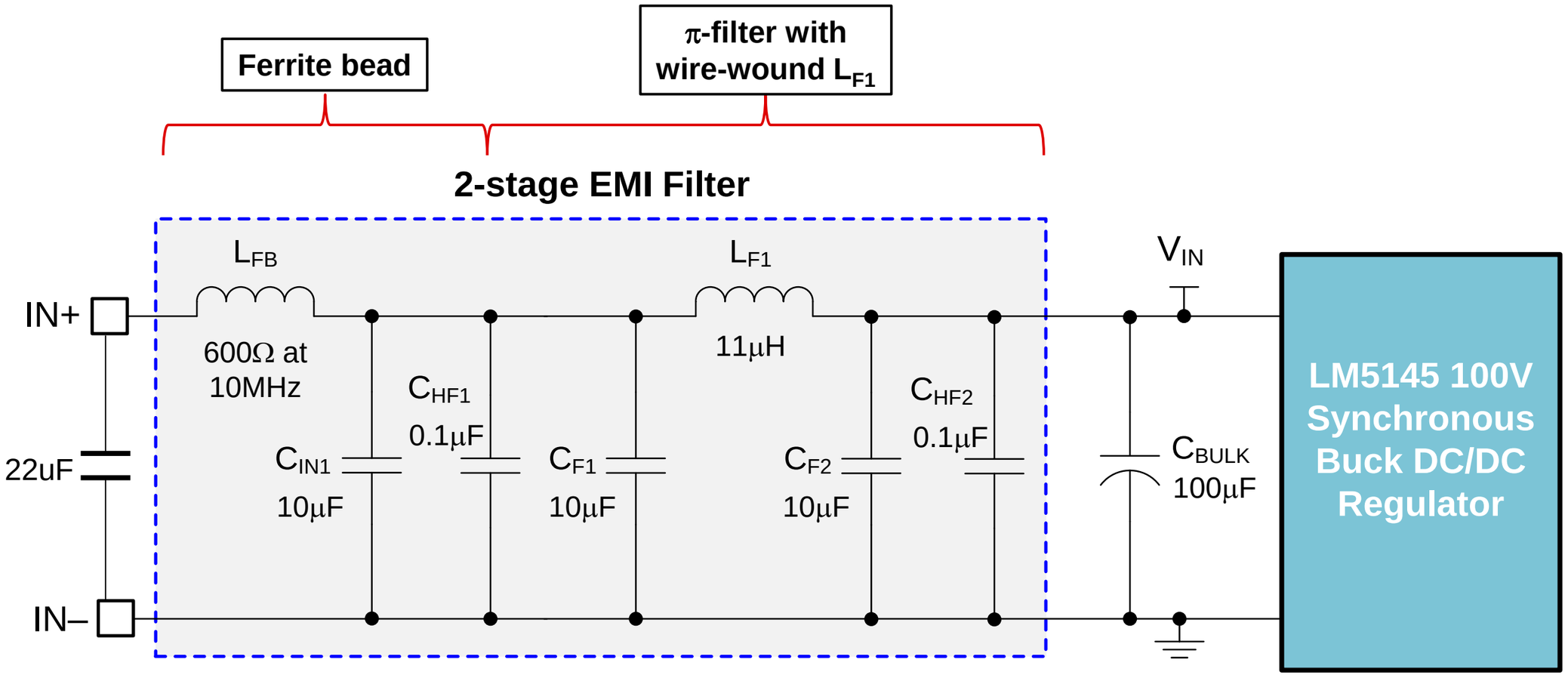


Yellow: Peak detection result

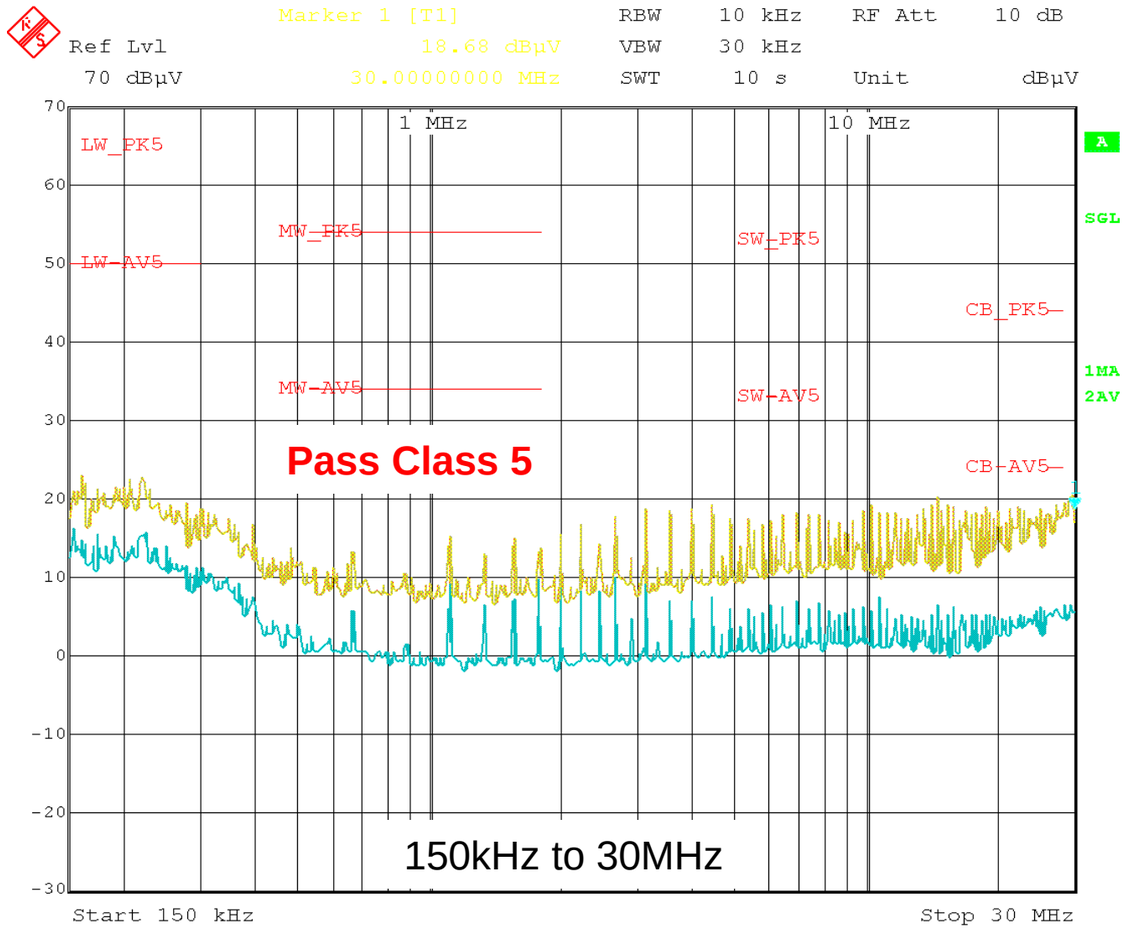
Blue: Average detection result

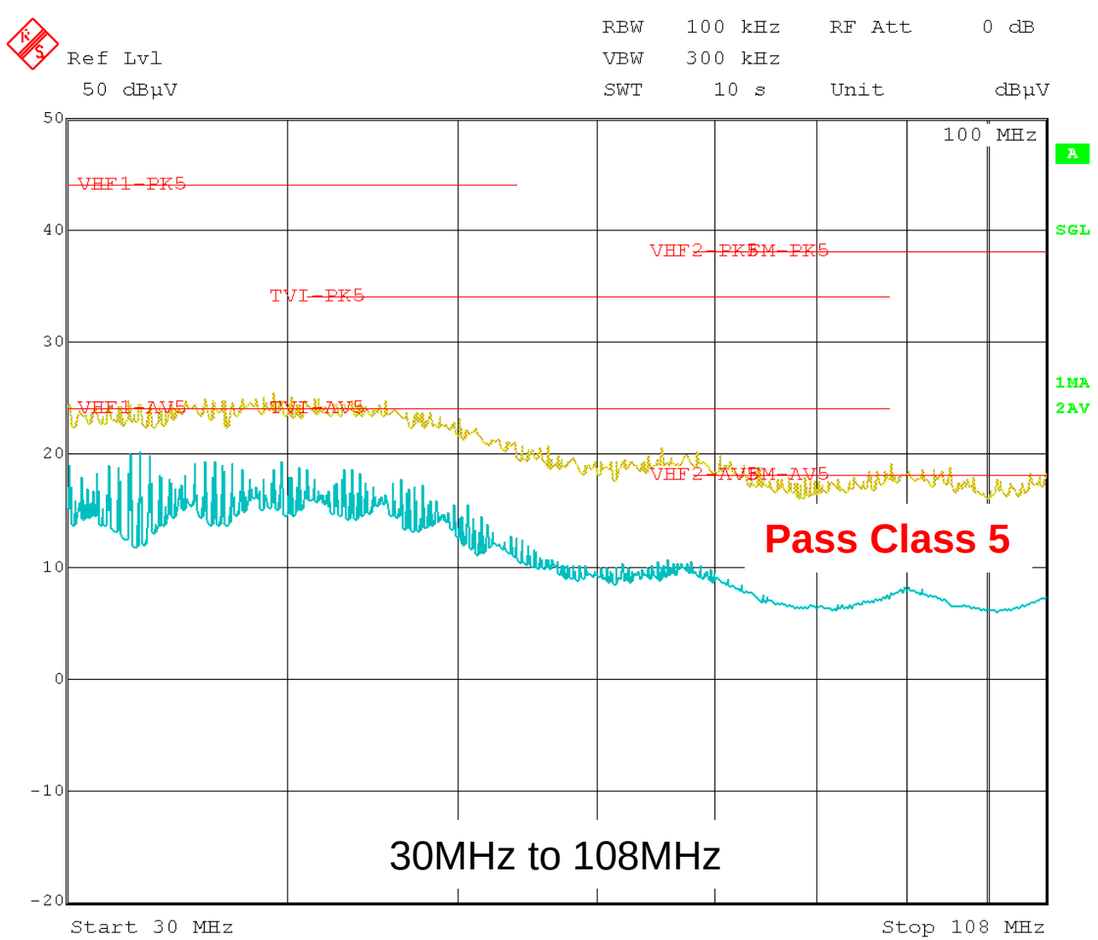
Red Lines: Class 5 Limits

EMI filter schematic



LM5145 EVM – Conducted EMI with 2-stage EMI filter



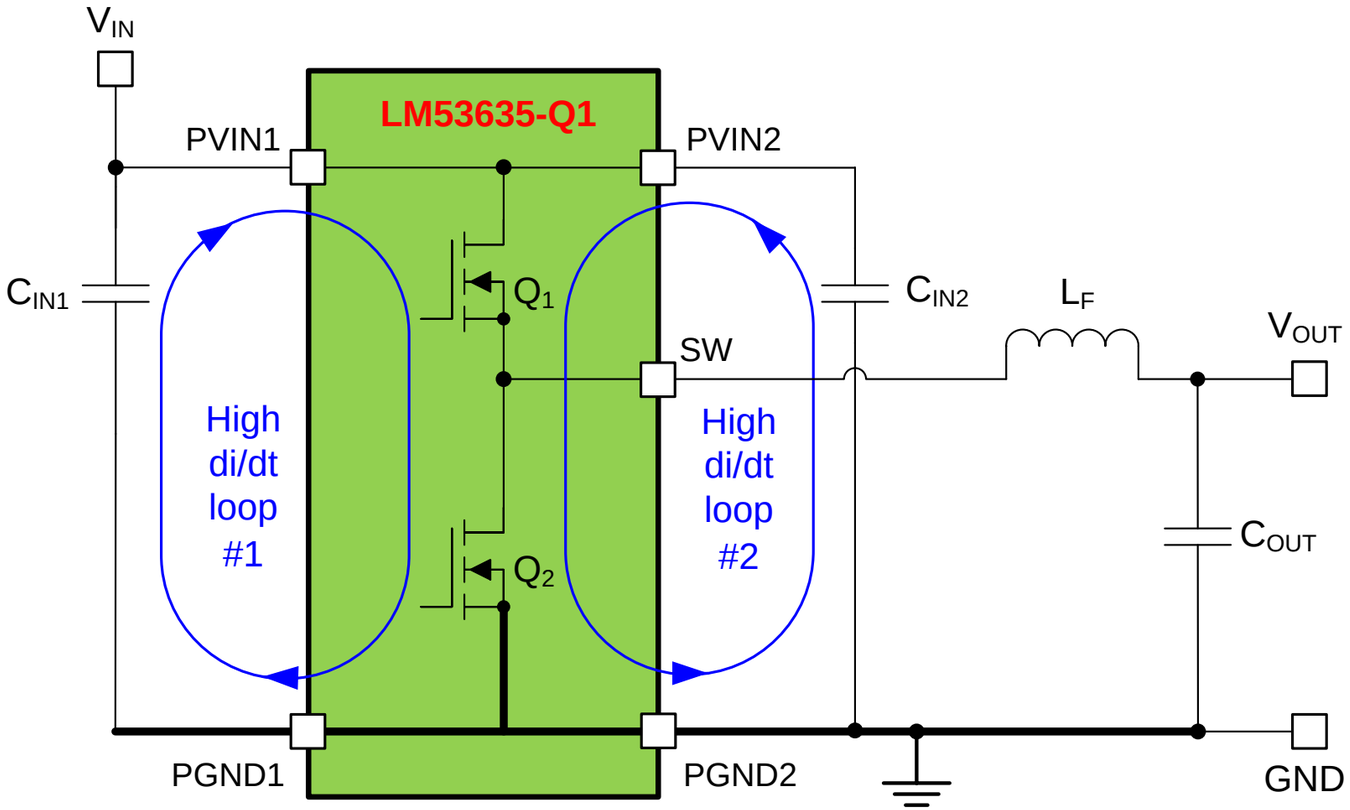


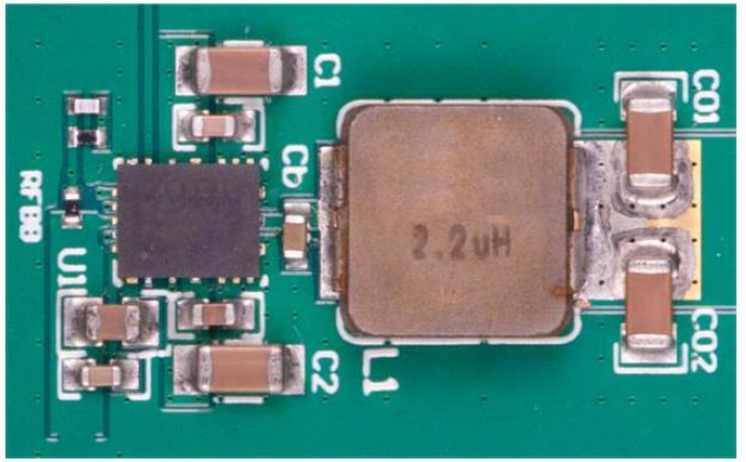
Yellow: Peak detection result
Blue: Average detection result

Red Lines: Class 5 Limits

LM53635-Q1 36V 3.5A automotive buck converter

HotRod package, 2.1MHz (above AM band), spread spectrum, optimized layout

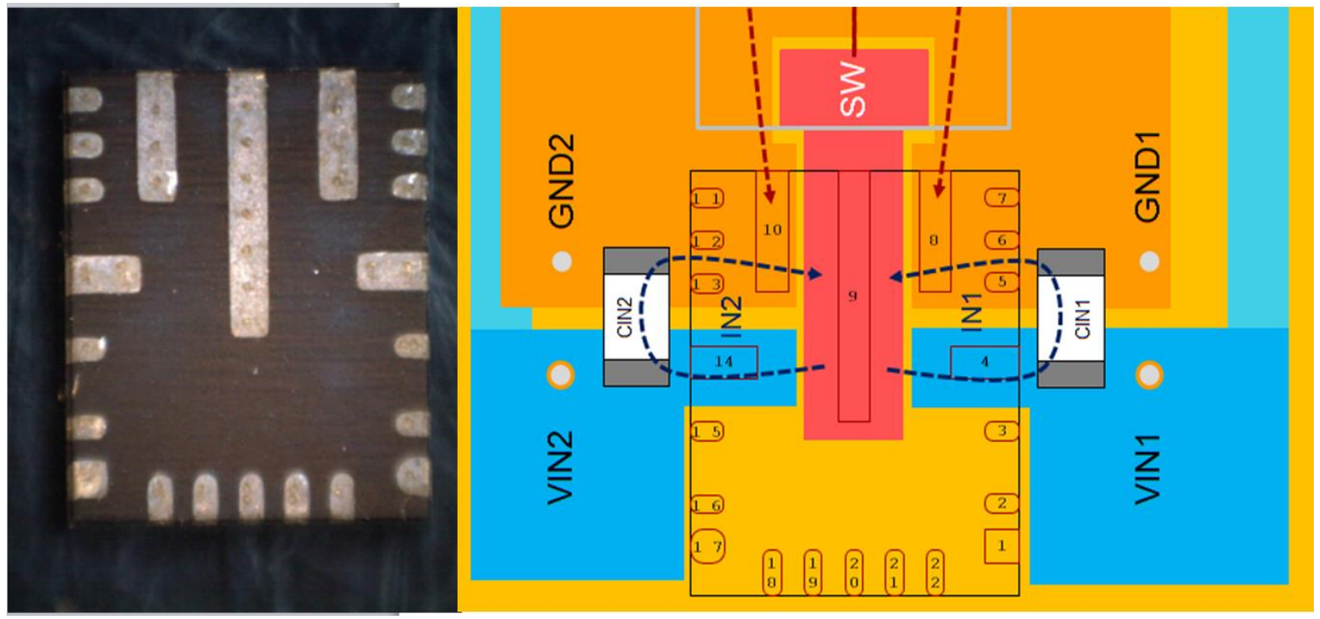


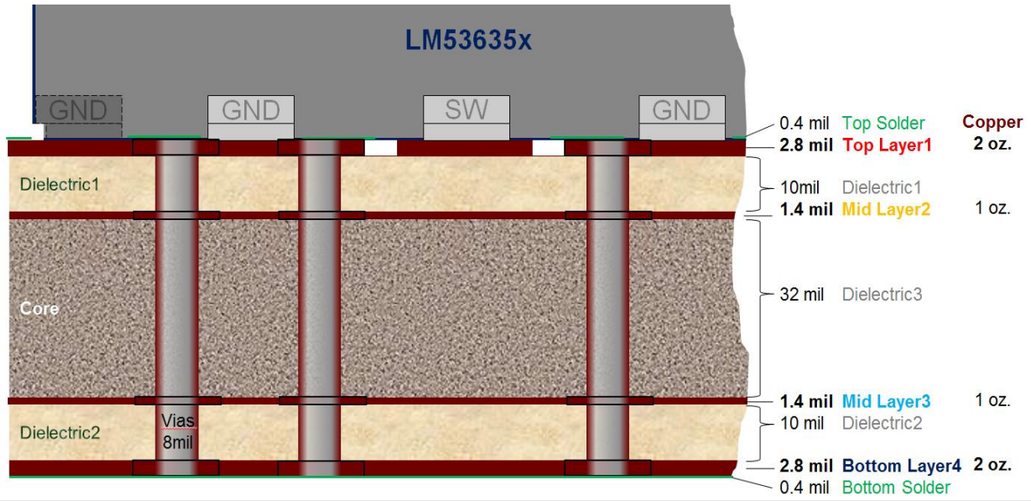


1. **Two input bypass caps**, **forming two current loops**
2. Small area, single layer SW node PCB layout
3. Integrated **spread spectrum**
4. R_{BOOT} adjustable SW node rise time

[9] TIDA-00987 “CISPR 25 Class 5 USB Type-C Reference Design with USB3.0 Data Support,” www.ti.com/tool/tida-00987

LM53635-Q1 low parasitic inductance package

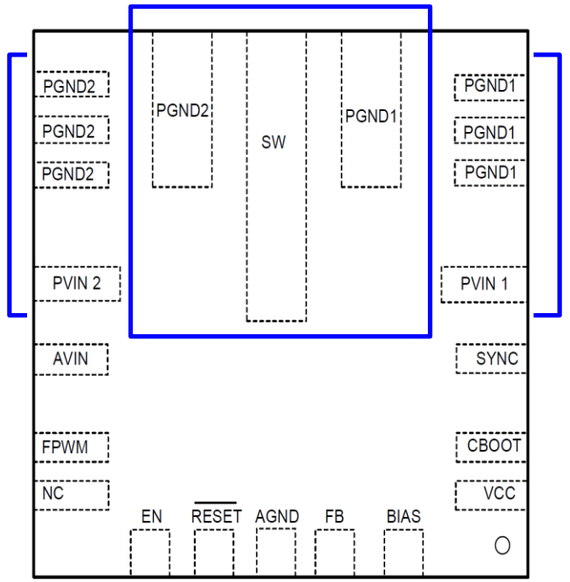




Package is 4mm × 5mm **VQFN-22** with flip-chip-on-lead (FCOL) **HotRod** technology and **wettable flank** pins

CIN1 and CIN2 creating 2 input loops.

PVIN2, PGND2 pins



PVIN1, PGND1 pins

LM53635-Q1 optimized PCB floorplan guidelines

Input Caps

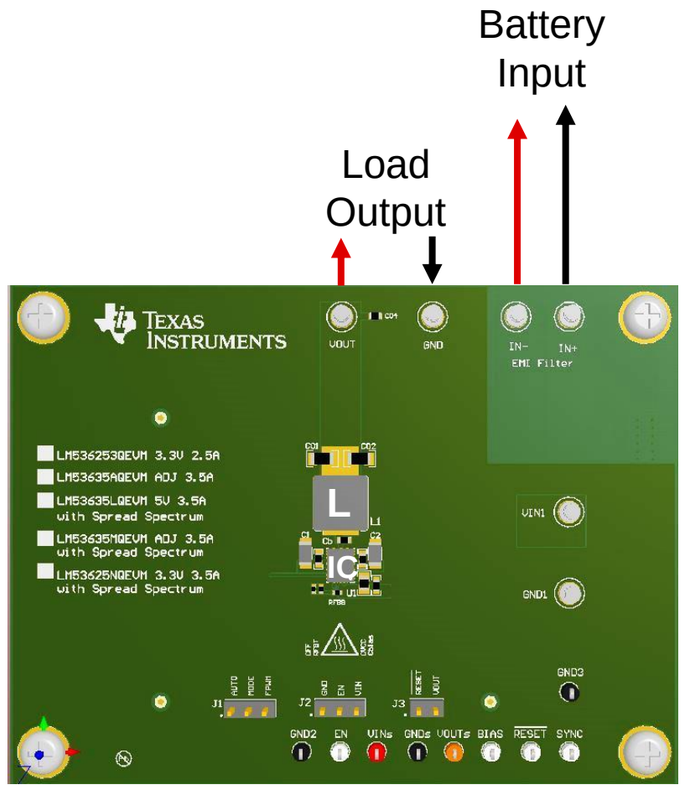
1. Input caps placed on **both sides of IC** to create two parallel paths for input ripple current (half current, flux cancellation, minimized parasitic L)

EMI Mitigation Guidelines

1. IC and switch-node are placed on PCB **top/center** most far away from EMI table **GND** plane
2. Battery input and load output wires are on same side on PCB to minimize EMI emission from power wires
3. EMI Filter area is moved **away from IC** and to the **bottom layer side** to prevent coupling from SW into “clean input”
4. All connector posts are placed away from SW to prevent **coupling** into any other external wire that could act as an antenna.
5. Bottom layer is a **closed GND** plane with minimal switching or ripple noise traces, **facing/coupling to EMI table GND plane**

Thermal Guidelines

1. Hottest components – IC and inductor L – are placed in PCB center and on **top layer** for best heat distribution and dissipation
2. Top & bottom layers have **maximized filled copper** coverage area for large area and 2oz copper to transfer heat away from source



References

[1] “Understanding noise-spreading techniques and their effects in switch-mode power applications,” SEM1800 topic 2, 2008, TI app note, http://www.ti.com/download/trng/docs/seminar/Topic_2_Rice_Gehrke_Segal.pdf (paper)

http://focus.ti.com.cn/cn/download/shared/panasia/sem908009_2_Rice_Segal_slides_V5.pdf (slides)

[2] “Understanding and optimizing electromagnetic compatibility in switchmode power supplies,” SEM1500 topic 2, 2002, TI app note, https://www.ti.com/lit/slup202

[3] “Conducted EMI mitigation techniques for switch-mode power converters: a survey,” IEEE TPE, Sept 2010, pp. 2344–2356, http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=5444974

[4] N. Oswald et al., “Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation,” IEEE Transactions on Industry Applications, Sept 2014, pp. 2154-2165, http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5953506

[5] Shuo Wang, “Common mode noise reduction for boost converters using general balance technique,” IEEE Transactions on Power Electronics, July 2007, pp. 1410-1416, http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4267785

[6] D. Han et al., “A case study on common mode electromagnetic interference characteristics of GaN HEMT and Si MOSFET power converters for EV/HEVs,” IEEE Transactions on Transportation Electrification, March 2017, pp. 168-179, http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7707424

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Valuing wide V_{IN}, low EMI synchronous buck circuits for cost driven, demanding applications	White paper	http://www.ti.com/lit/wp/slyy104/slyy104.pdf
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