Driving the SAR

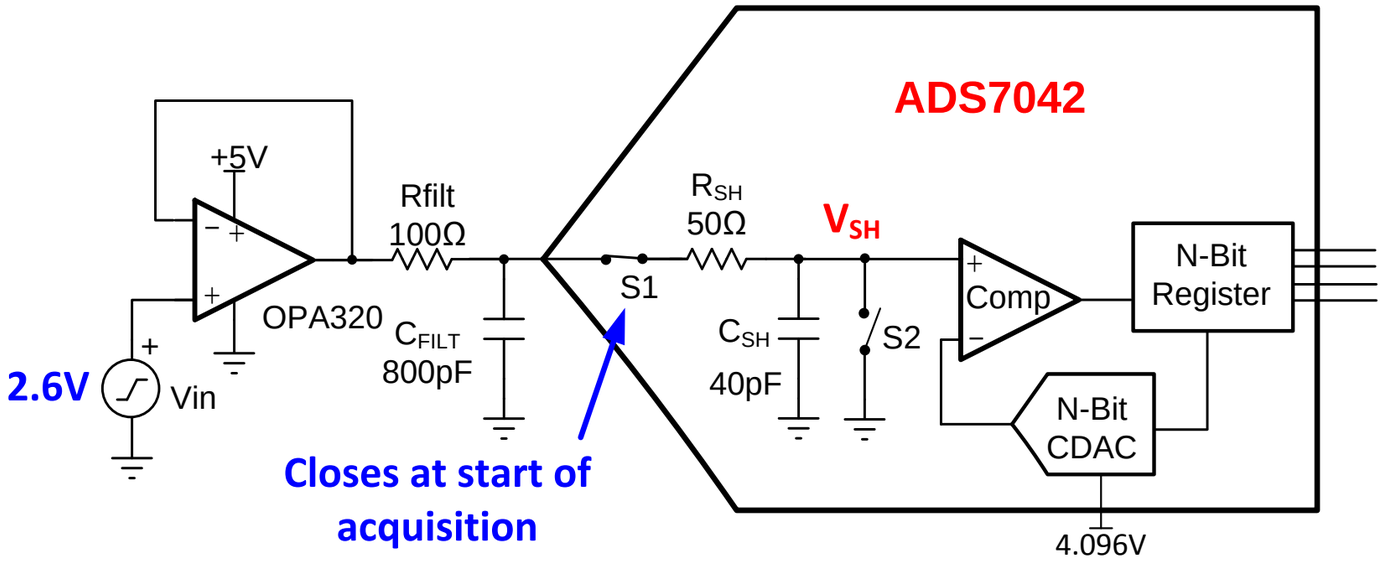
Summit 2017

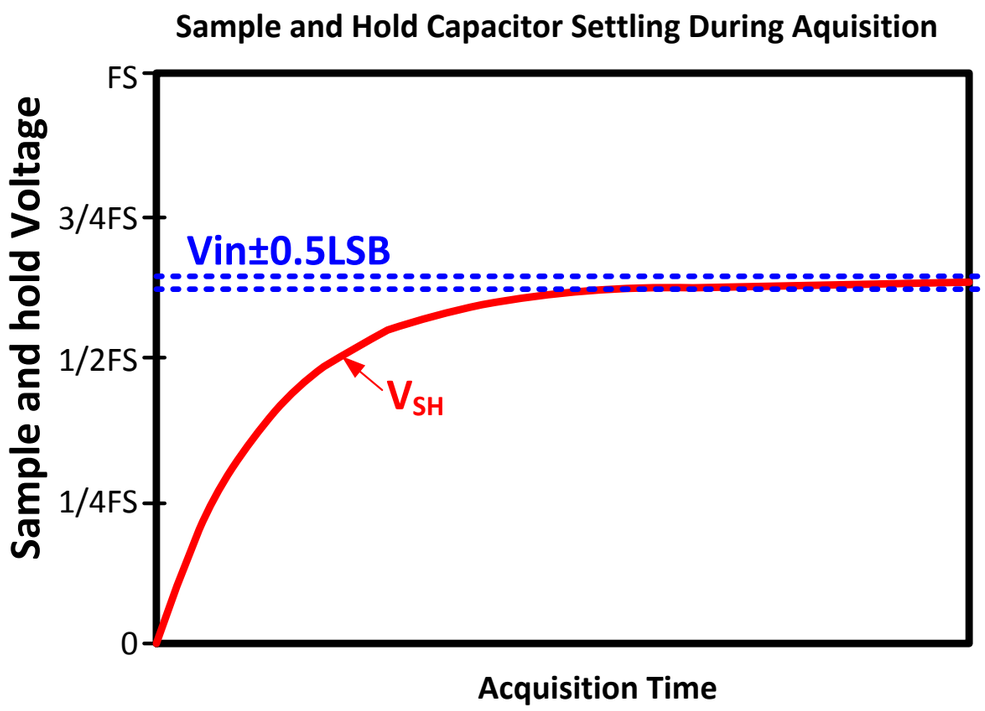
By Tim Green, Art Kay, Luis Chioye, and Dale Li

Agenda

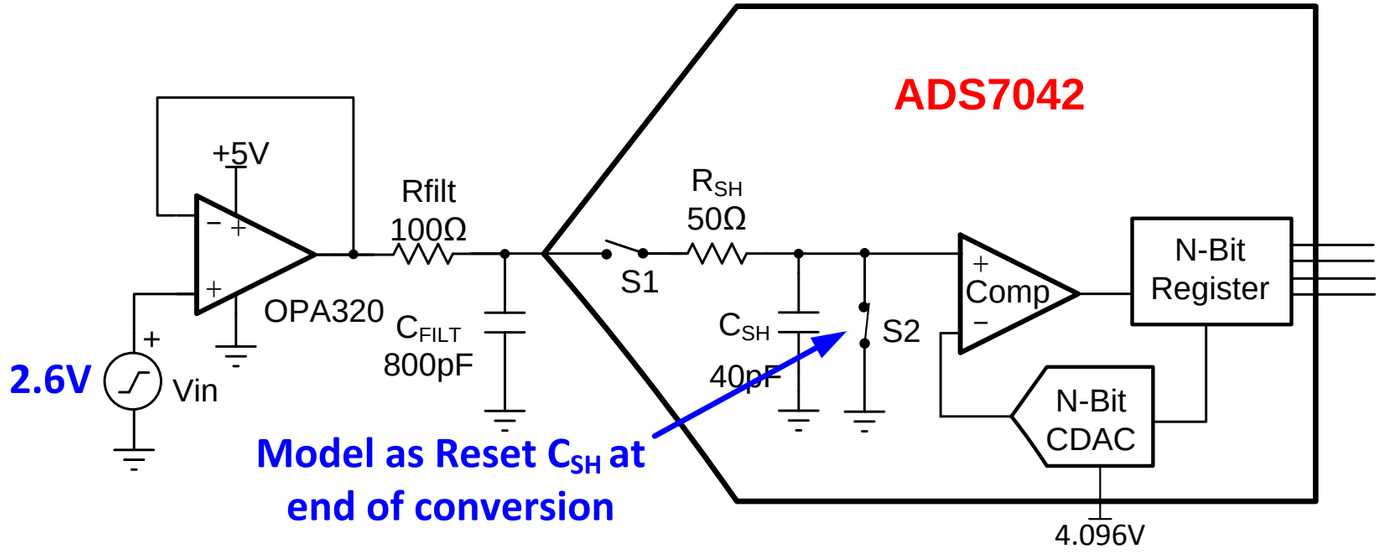
1. SAR Operation Overview
2. Select the data converter
3. Use the Calculator to find amplifier and RC filter
4. Find the Op Amp
5. Verify the Op Amp Model
6. Building the SAR Model
7. Refine the Rfilt and Cfilt values
8. Final simulations
9. Measured Results
10. SAR Drive Calculator Algorithm

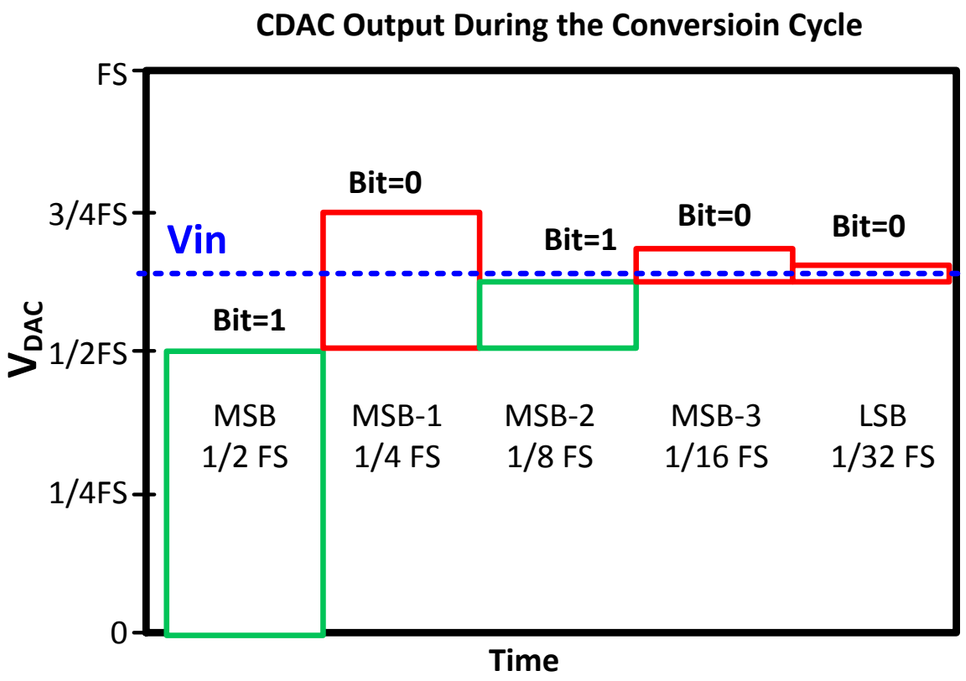
Acquisition phase





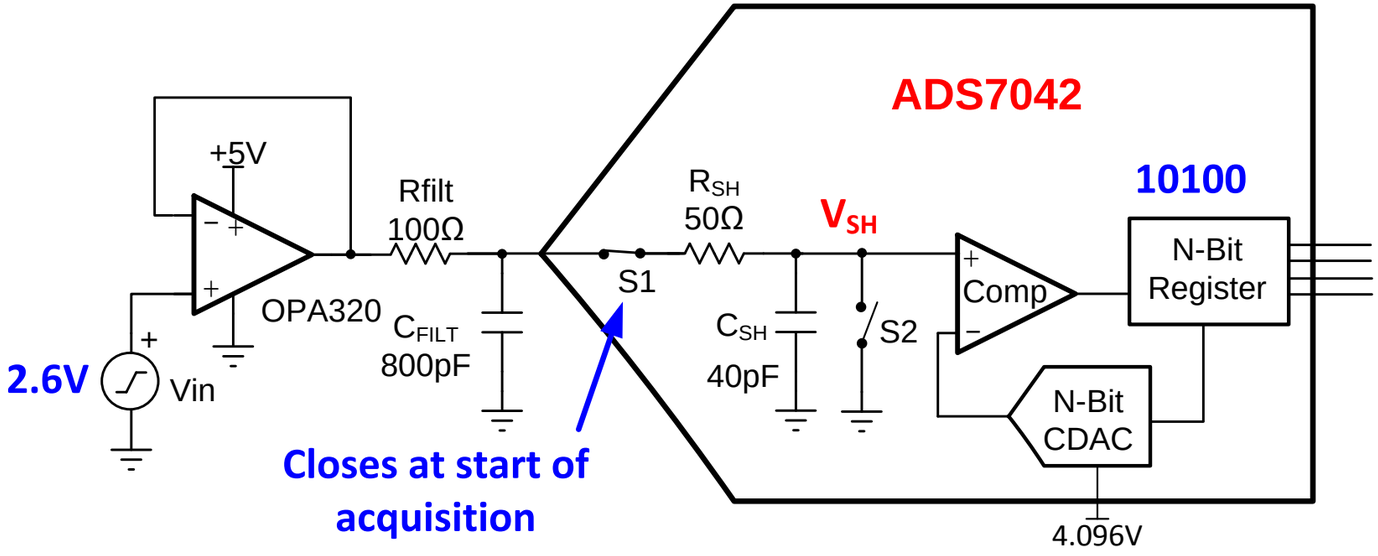
Conversion Phase

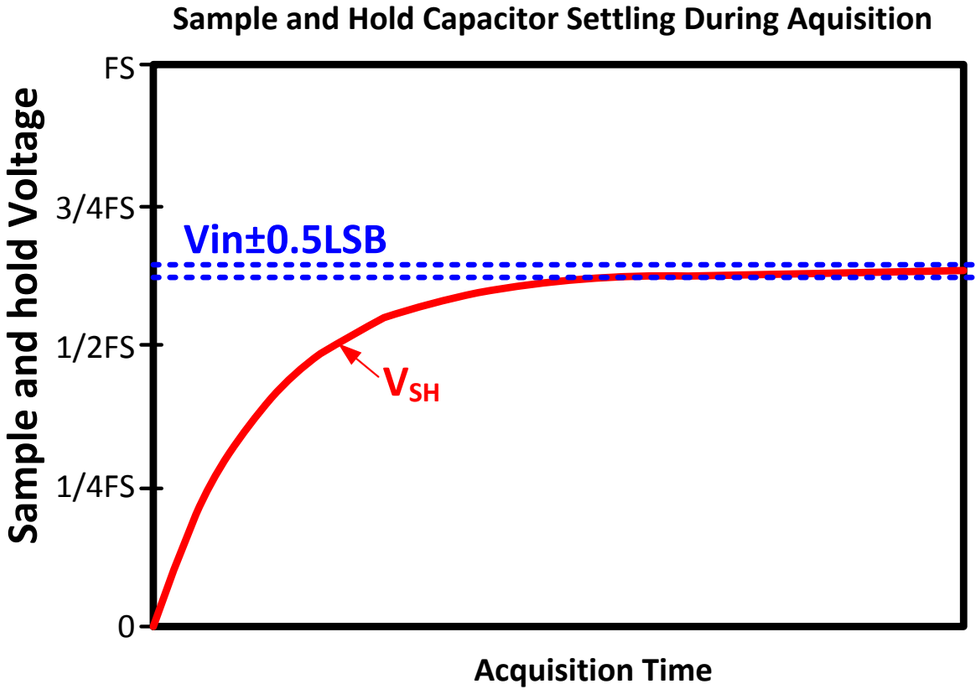




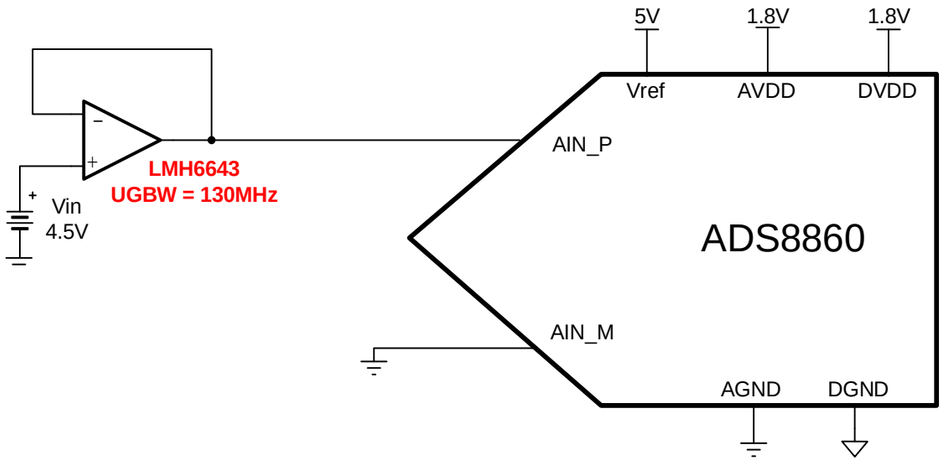
Overall Objective

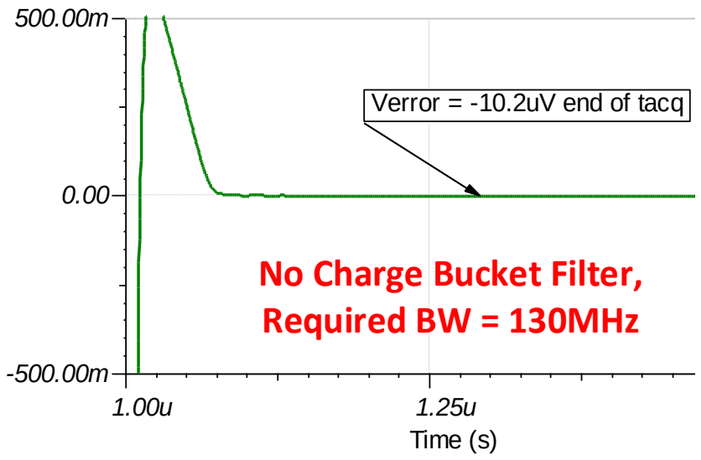
- Find Rfilt and Cfilt charge bucket filter that will optimize settling
- Find amplifier with bandwidth sufficient for settling
- Achieve final settling of 0.5LSB or better at end of tacq

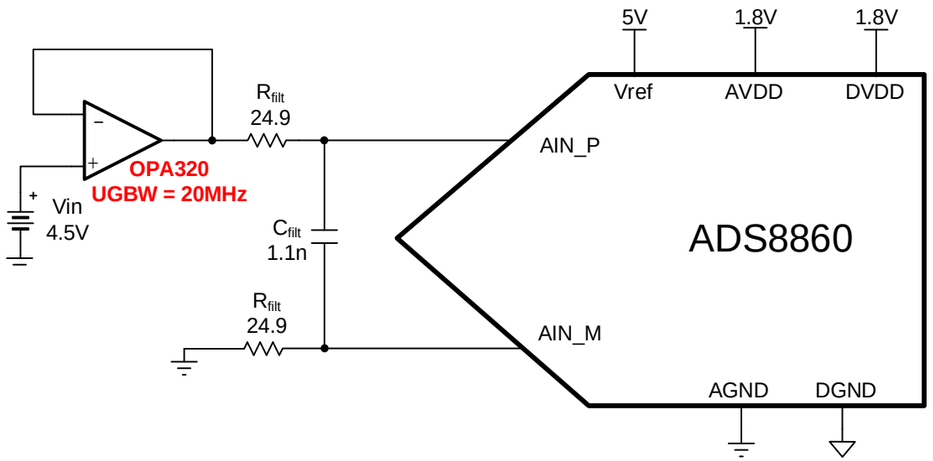


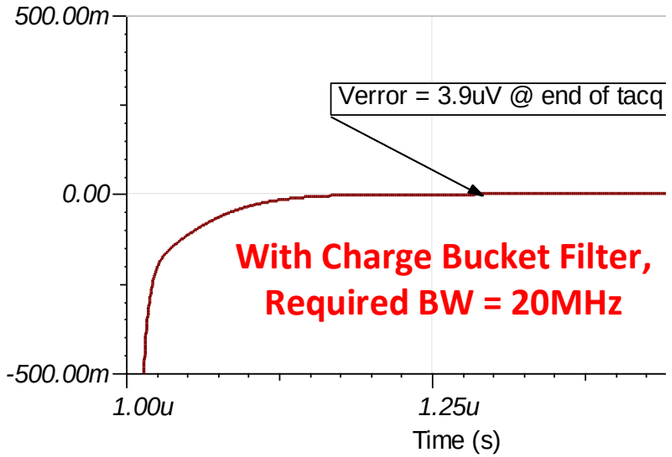


Is the charge bucket filter required?









Advantage of low BW Amp

- Lower Iq
- Better Vos, Ib
- Lower cost
- Less sensitive to stability issues

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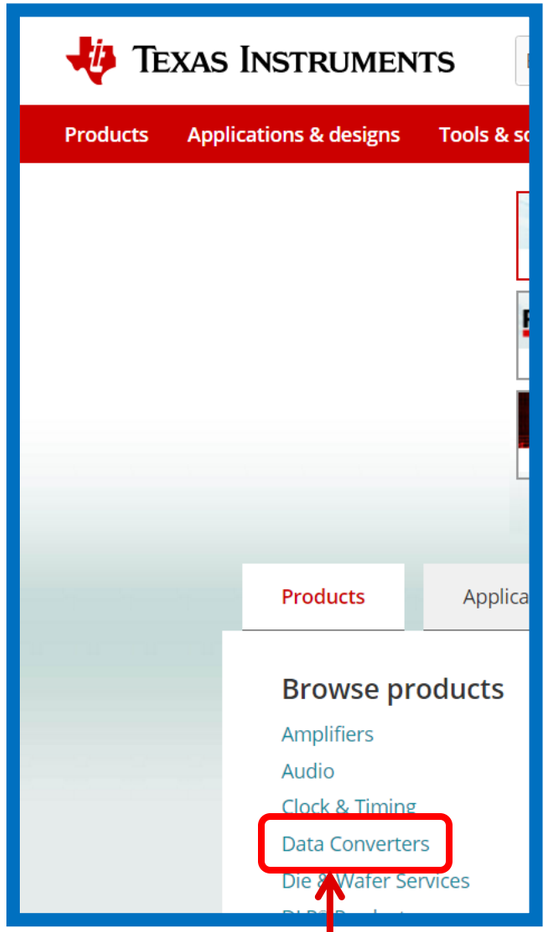
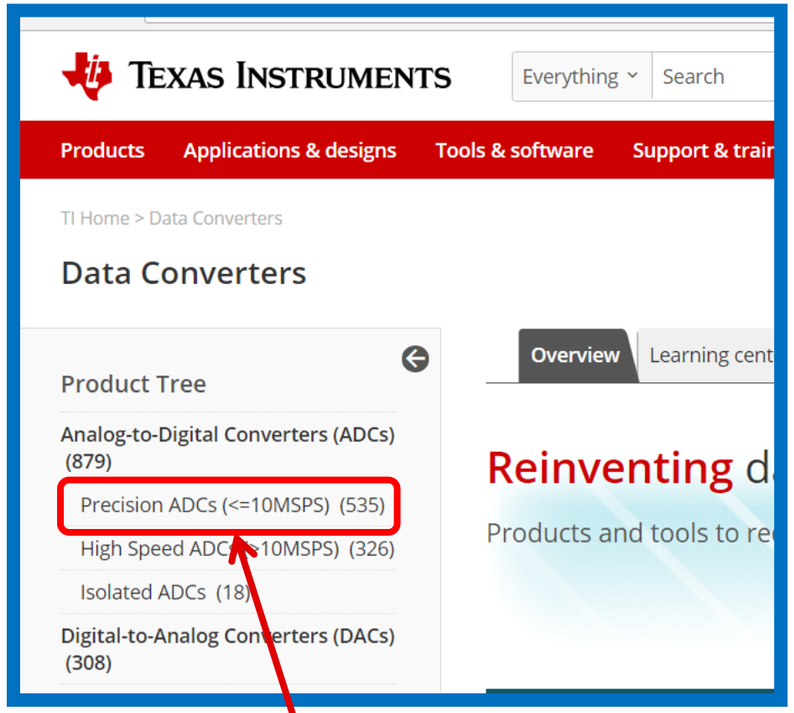
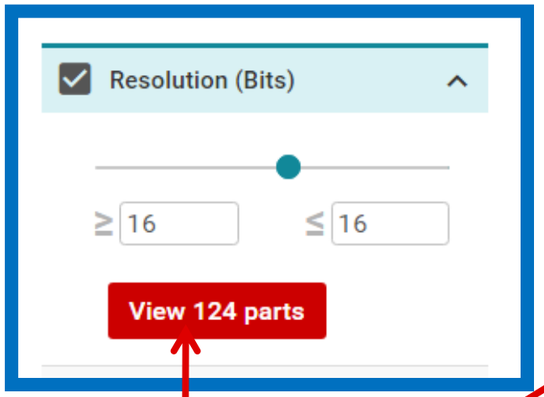
Find the data converter

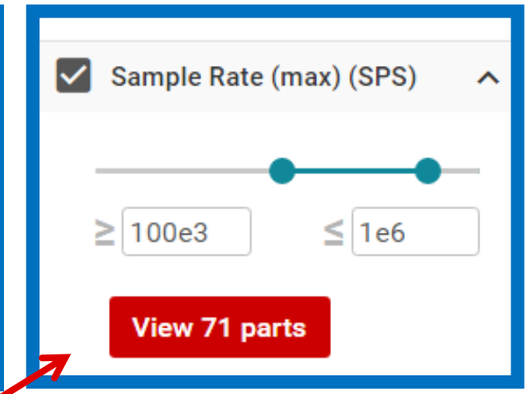


Select Data Converters



Select “Precision ADC”
535 different choices!





Continue to refine selection

Design Goal:
#Bits = 16
100kSPS < Sample Rate <1MSPS
Single Ended Input
5V input range
SPI interface

Find the data converter

 # Input Channels

≥ 1 ≤ 1

View 42 parts

Input Range (Max) (V)

≥ 0.0195 ≤ 5

View 17 parts

Interface

- [ ] I2C
- [ ] Microwire (Serial I/O)
- [ ] Parallel
- [ ] QSPI
- [x] SPI
- [ ] Serial

View 11 parts

Input Type

OR

- [ ] Differential
- [ ] Pseudo-Differential
- [x] Single-Ended

View 4 parts

Continue to refine selection

4 matching parts out of 535 total parts

Compare	Part Number (Filter by part number)	Resolution (Bits)	Sample Rate (max) (SPS)	# Input Channels	Multi-Channel Configuration	Input Range (Min) (V)	Input Range (Max) (V)	Interface	Integrated Features	Analog Voltage AVDD (Min) (V)	Analog Voltage AVDD (Max) (V)	Architecture	Rating	Operating Temperature Range (C)	Package Group
☐	ADS8866 - 16-Bit, 100-kSPS, Serial Interface, microPower, Miniature, Single-Ended Input, SAR Analog-to-Digital	16	100kSPS	1	N/A	0	5	SPI	Daisy-Chainable, Oscillator	2.7	3.6	SAR	Catalog	-40 to 85	VSSOP, VSON
☐	ADS8864 - 16-Bit, 400-kSPS, Serial Interface, microPower, Miniature, Single-Ended Input, SAR ADC	16	400kSPS	1	N/A	0	5	SPI	Daisy-Chainable, Oscillator	2.7	3.6	SAR	Catalog	-40 to 85	VSON, VSSOP
☐	ADS8862 - 16-Bit, 680-kSPS, Serial Interface, uPower, Miniature, Single-Ended, Differential Input SAR ADC	16	680kSPS	1	N/A	0	5	SPI	Daisy-Chainable, Oscillator	2.7	3.6	SAR	Catalog	-40 to 85	VSON, VSSOP
☐	ADS8860 - 16 bit 1 MSPS, Serial, Pseudo-Differential Input, Micro Power, Miniature, SAR ADC	16	1MSPS	1	N/A	0	5	SPI	Daisy-Chainable, Oscillator	2.7	3.6	SAR	Catalog	-40 to 85	VSON, VSSOP

ADS8860
Choose the data converter with the highest sample rate from this group

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Information needed from the data sheet

Full Scale Range (FSR)	The range of voltage that is applied to the converter for valid conversions. Typically this is Vref or a multiple of Vref.
Resolution	The number of bits used to represent the digital equivalent of the equivalent analog signal. In this example we use a 16 bit converter that has 2^{16} or 65536 codes.
$\mathbf{C_{sh}}$	Sample and Hold capacitance. Sometimes called Cin. Typically between 10pF and 100pF.
$\mathbf{R_{sh}}$	On-resistance for sample and hold switch. Typically between 10 ohms and 100 ohms. Normally, this information is in the data sheet equivalent circuit.
$\mathbf{t_{acq}}$	Acquisition time. This is duration that the sample and hold switch is closed. A longer acquisition time makes it easer to settle. The data sheet provides a minimum acquisition time that corresponds to the maximum throughput (samples / second).

Example: Full Scale Range, Resolution, C_{sh}, R_{sh}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input span (1)	AINP – AINN	0		V_{REF}	V
	Operating input range (1)	AINP	–0.1		V_{REF} + 0.1	V
		AINN	–0.1		+ 0.1	V
C_I	Input capacitance	AINP and AINN terminal to GND		59		pF
	Input leakage current	During acquisition for dc input		5		nA
SYSTEM PERFORMANCE						
	Resolution			16		Bits

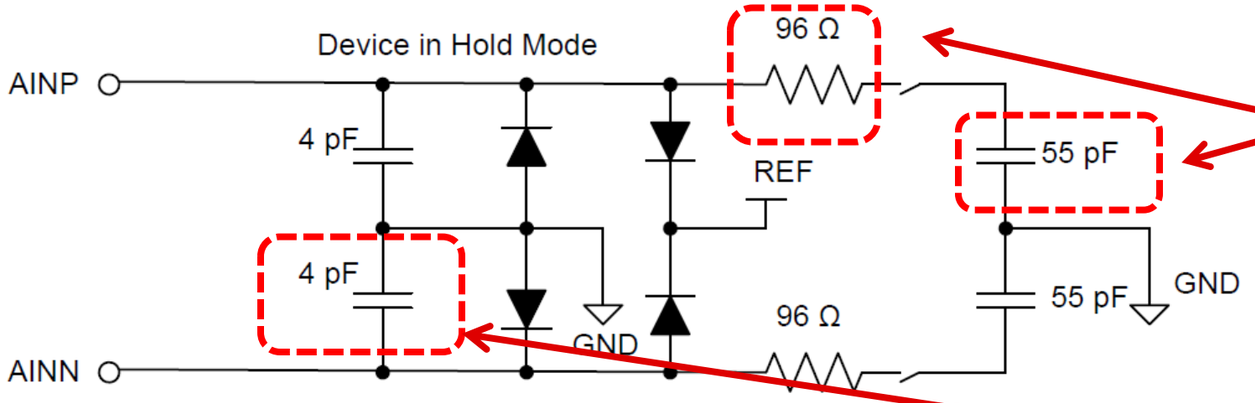


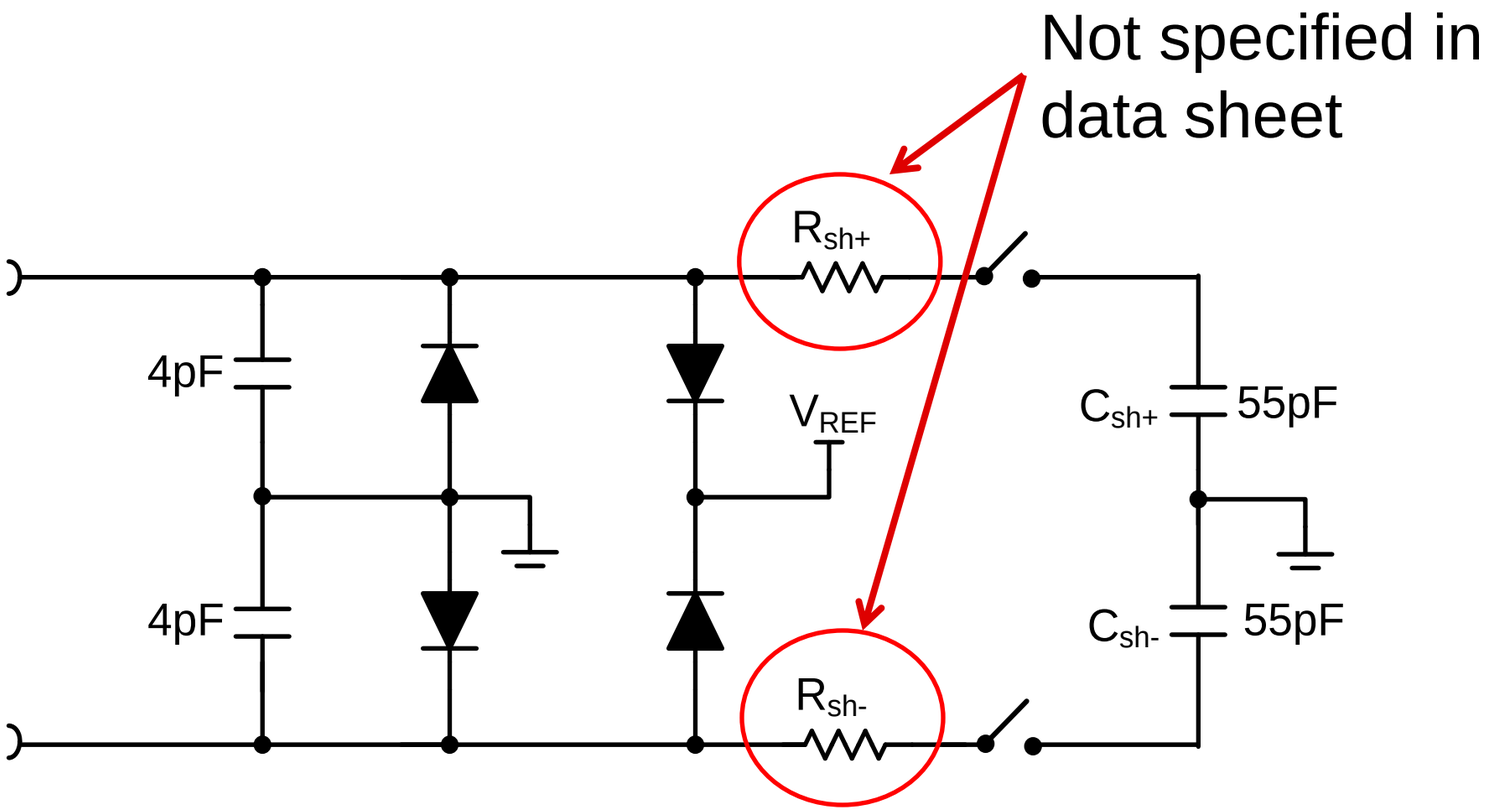
Figure 45. Input Sampling Stage Equivalent Circuit

C_{sh} and R_{sh} can usually be found in the equivalent circuit.

Full Scale Range and resolution

Note: C_I from the table
C_I = 55pF+4pF

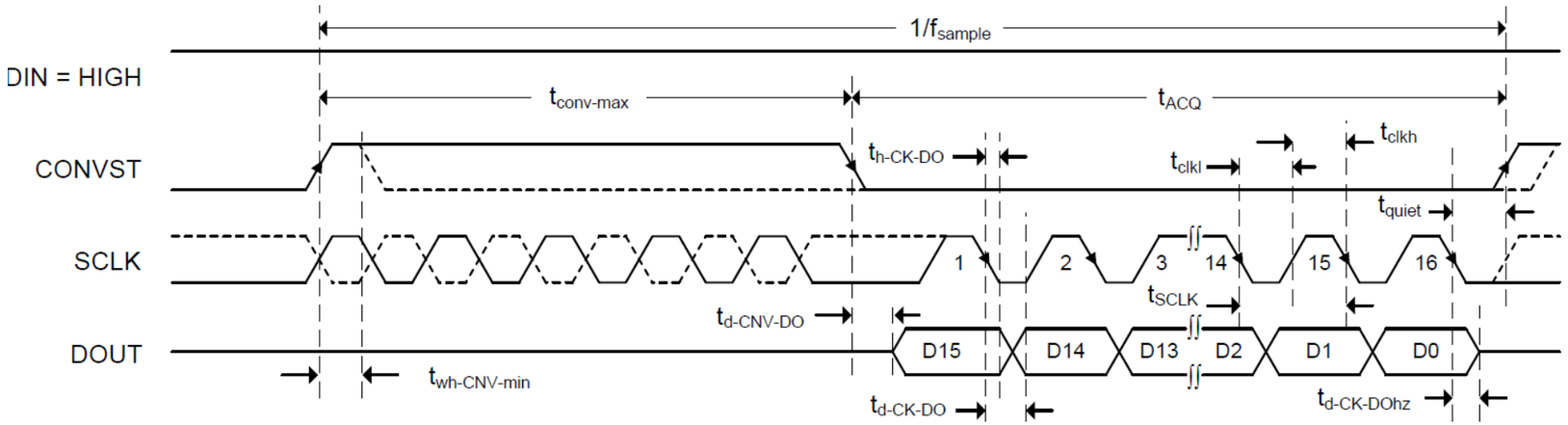
If the data sheet doesn't provide R_{sh}



$$R_{sh} \approx \frac{t_{acq_min}}{100 \cdot C_{sh}}$$

$$R_{sh} \approx \frac{290ns}{100 \cdot 55pF} = 53\Omega$$

For our example: acquisition time



Conversion time set by internal clock. The maximum time for conversion is 710ns.

PARAMETER		MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time	290			ns
t_{conv}	Conversion time	500		710	ns

We are running at maximum throughput (1MHz)

$1/f_{sample} = t_{conv\text{-}max} + t_{acq\text{-}min} = 710ns + 290ns = 1\mu s$, or $f_{sample} = 1MHz$

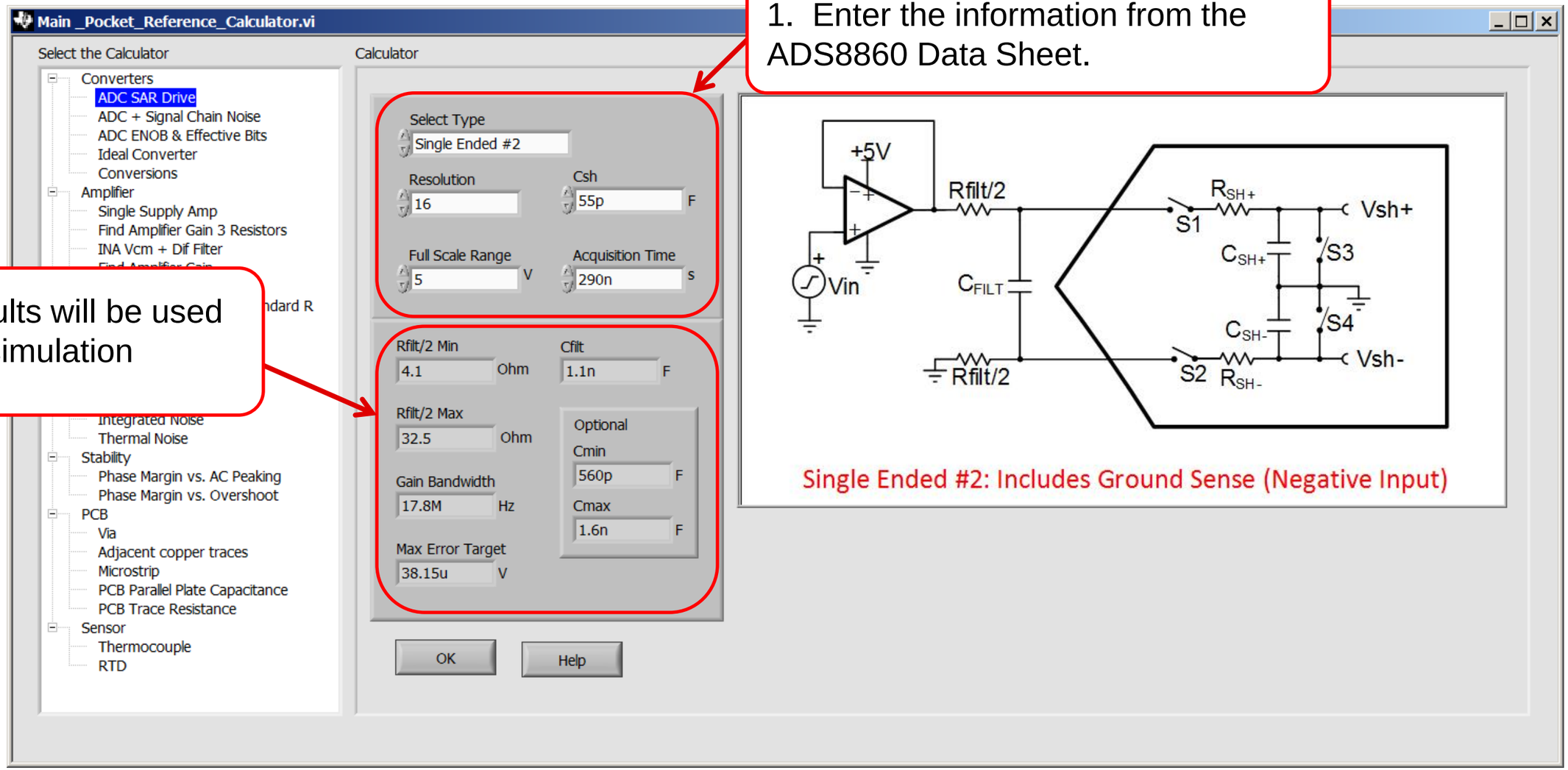
For cases where you aren't running at maximum throughput (e.g. 500kHz)

$t_{acq} = 1/f_{sample} – t_{conv\text{-}max} = (1/500kHz) – 710ns = 1290ns$

Run the “ADC SAR Drive” tool: ADS8860 Example

1. Enter the information from the ADS8860 Data Sheet.

2. Results will be used in the simulation



http://www.ti.com/tool/analog-engineer-calc

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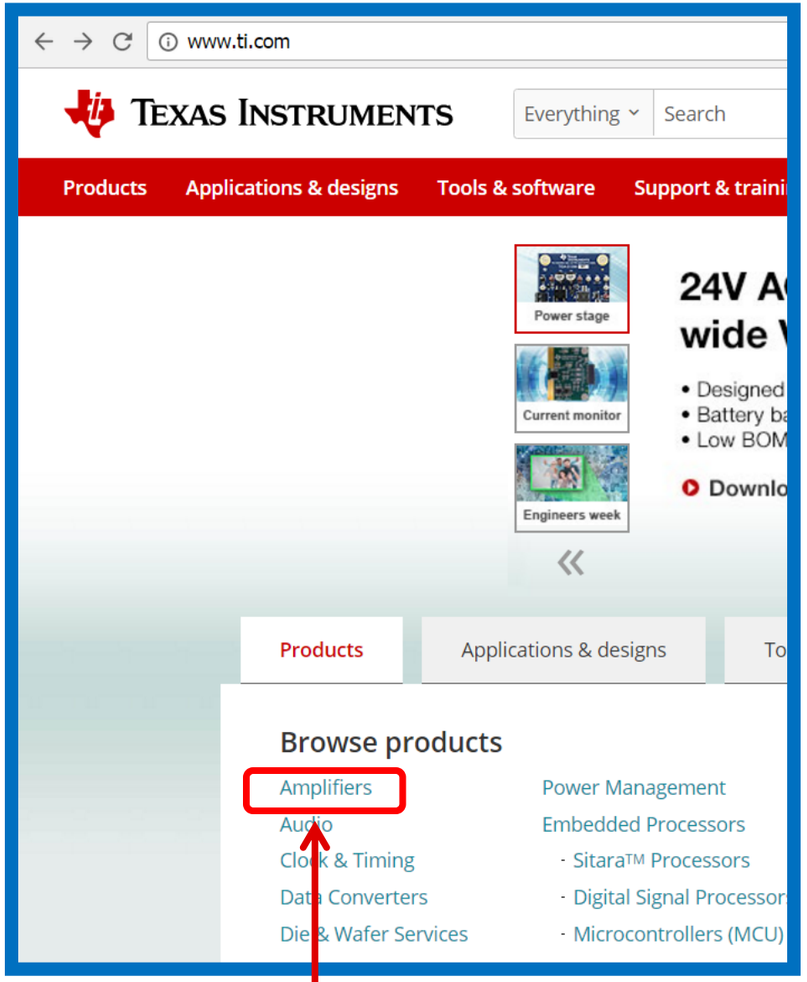
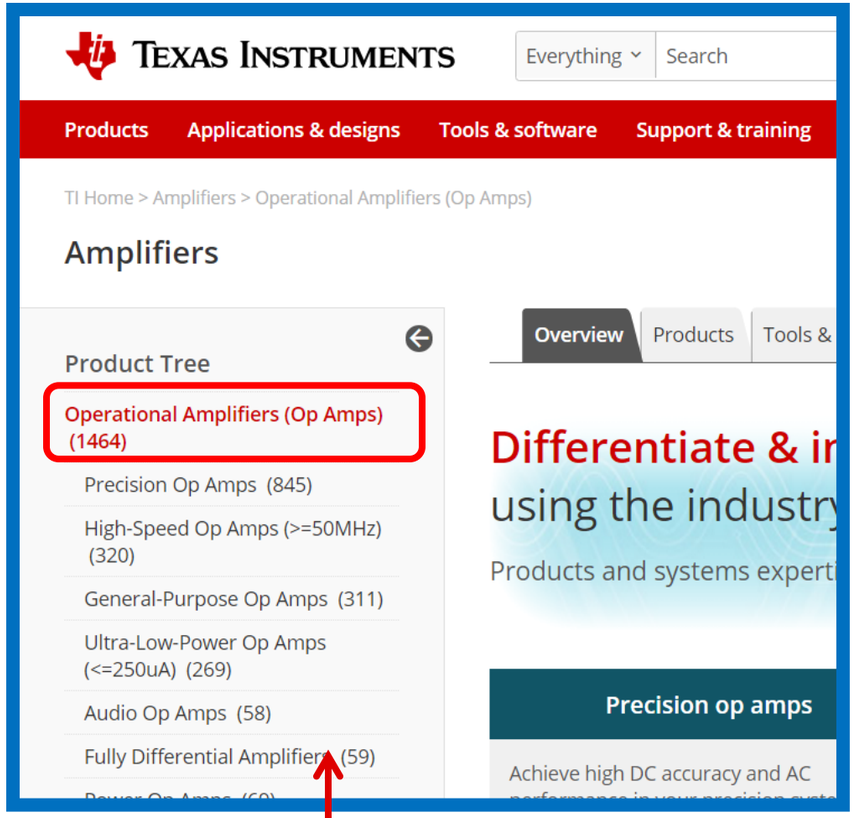
Find the Op Amp

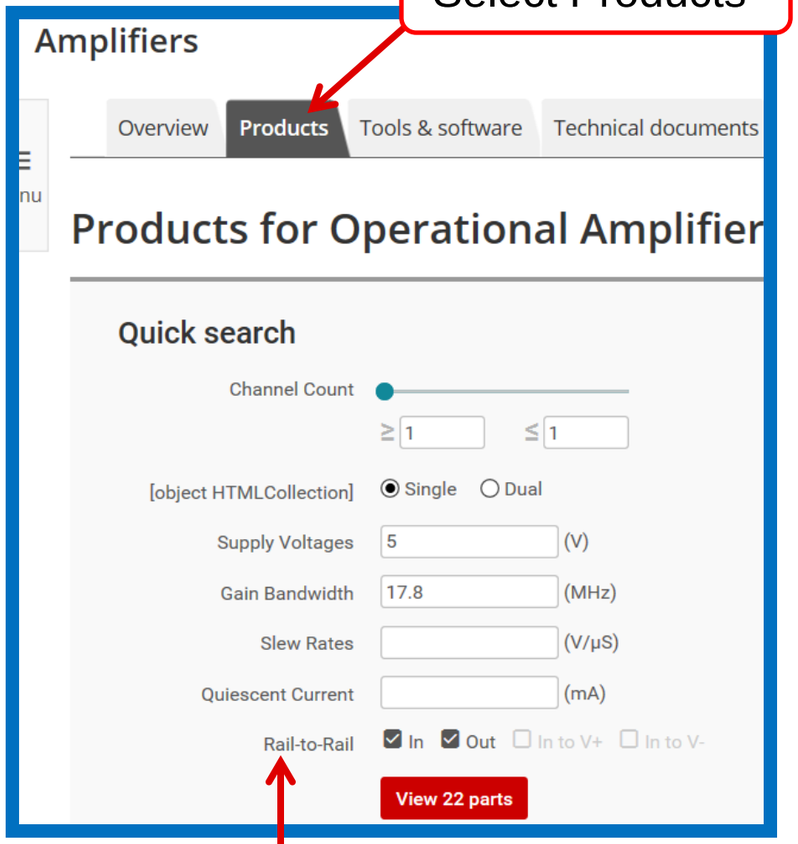


Select Amplifiers



Select
Operational Amplifiers (Op Amps)
1464 different choices!

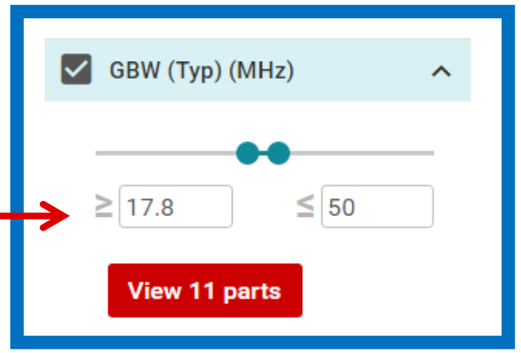
Select Products

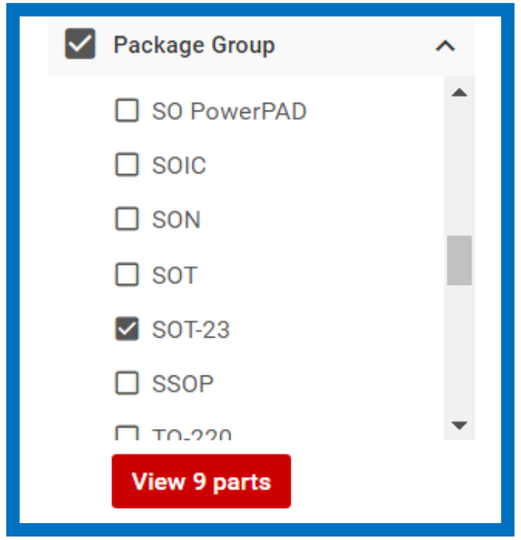


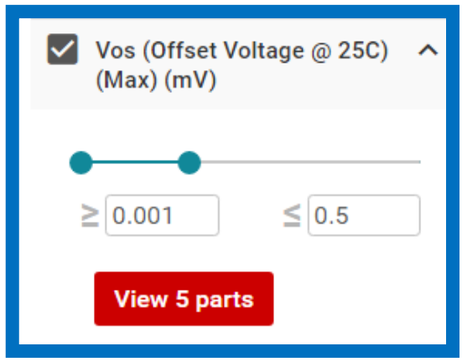
Channel Count = 1
Supply Voltage = 5V
Gain Bandwidth = 17.8MHz
22 devices left!

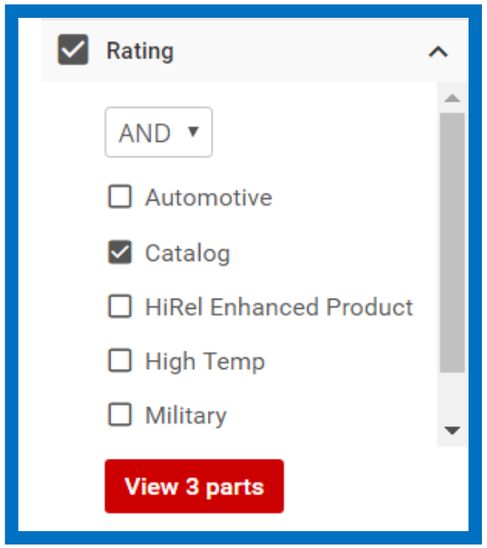
Set filters to find the best device

Use the filters to narrow options









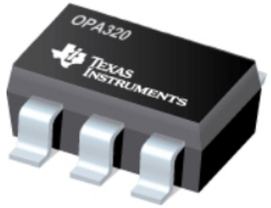
OPA320 Best offset

3 matching parts out of 1464 total parts

Email Download to Excel

Compare	Part Number (Filter by part number)	Number of Channels (#)	Total Supply Voltage (Min) (+5V=5, +/-5V=10)	Total Supply Voltage (Max) (+5V=5, +/-5V=10)	GBW (Typ) (MHz)	Rail-to-Rail	Slew Rate (Typ) (V/us)	Vos (Offset Voltage @ 25C) (Max) (mV)	Iq per channel (Typ) (mA)	Rating	Operating Temperature Range (C)	Package Group	Approx. Price (US$)
☐	OPA320 - Precision, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier	1	1.8	5.5	20	In, Out	10	0.15	1.5	Catalog	-40 to 125	SOT-23	0.80 | 1ku
☐	OPA365 - 2.2V, 50MHz, Low-Noise, Single-Supply Rail-to-Rail Operational Amplifier	1	2.2	5.5	50	In, Out	25	0.2	4.6	Catalog	-40 to 125	SOIC, SOT-23	0.65 | 1ku
☐	LMP7731 - 2.9 nV/sqrt(Hz) Low Noise, Precision , RRIO Amplifier	1	1.8	5.5	22	In, Out	2.4	0.5	2.2	Catalog	-40 to 125	SOIC, SOT-23	0.63 | 1ku

Get the latest model from the web



TI Home > Semiconductors > Amplifiers > Operational Amplifiers (Op Amps) > Precision Op Amps >

OPA320 (ACTIVE)

Precision, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier

OPAx320x Precision, 20-MHz, 0.9-pA, Low-Noise, RRIO, CMOS Operational Amplifie
F)

OPA320, OPA320S, OPA2320, OPA2320S EMI Immunity Performance

Description & parametrics | Online datasheet | Technical documents | **Tools & software** | Order Now | Compare | Quality &

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Models (6)

Title	Category	Type	Size (KB)	Date	Views
OPA320S PSpice Model (Rev. A)	PSpice Model	ZIP	4 KB	29 Aug 2013	117 views
OPA320S TINA-TI Reference Design (Rev. A)	TINA-TI Reference Design	TSC	1203 KB	29 Aug 2013	64 views
OPA320S TINA-TI Spice Model (Rev. A)	TINA-TI Spice Model	ZIP	8 KB	29 Aug 2013	50 views
OPAy320 Family PSpice Model (Rev. C)	PSpice Model	ZIP	3 KB	28 Jul 2014	132 views
OPAy320 Family TINA-TI Reference Design (Rev. C)	TINA-TI Reference Design	TSC	255 KB	29 Jul 2014	90 views
OPAy320 Family TINA-TI Spice Model (Rev. C)	TINA-TI Spice Model	ZIP	8 KB	29 Jul 2014	125 views

Do you want to open or save **sbom439c.tsc** from **ti.com**? Open | Save | Cancel

1. The TINA model is located under tools and software.

2. Select the “reference design”. This will be a fully wired example schematic.

3. Press open and TINA SPICE will directly open the schematic.

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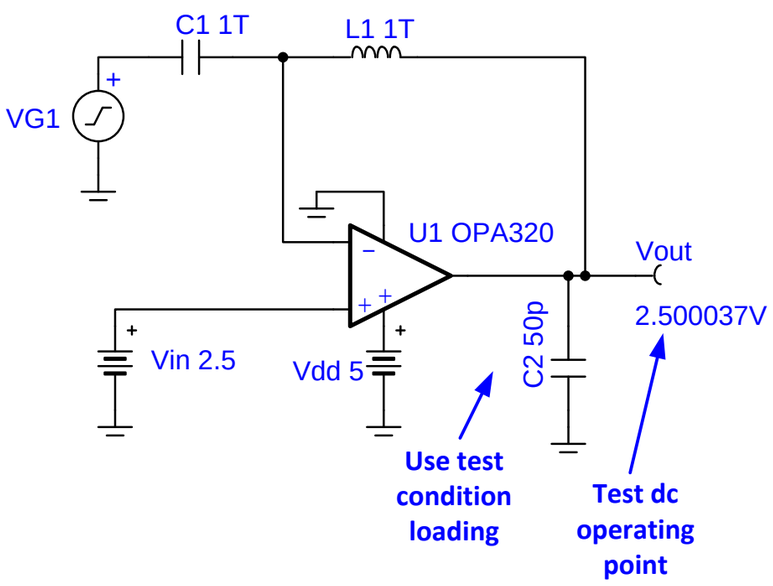
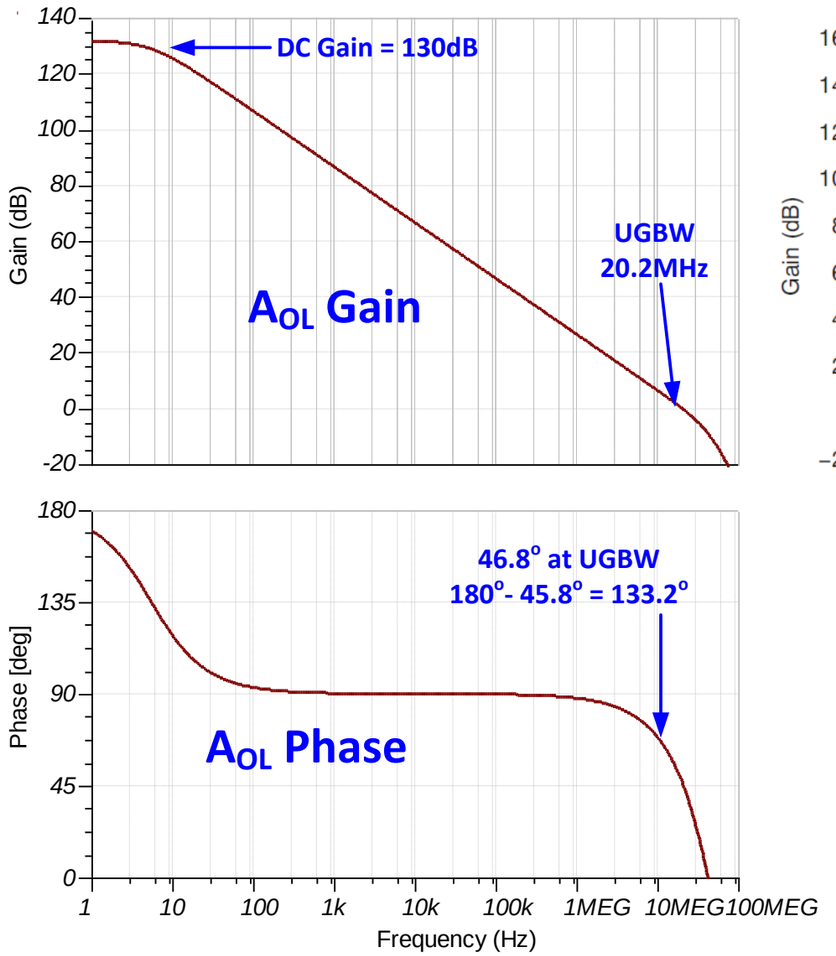
Op Amp Model: Open Loop Gain

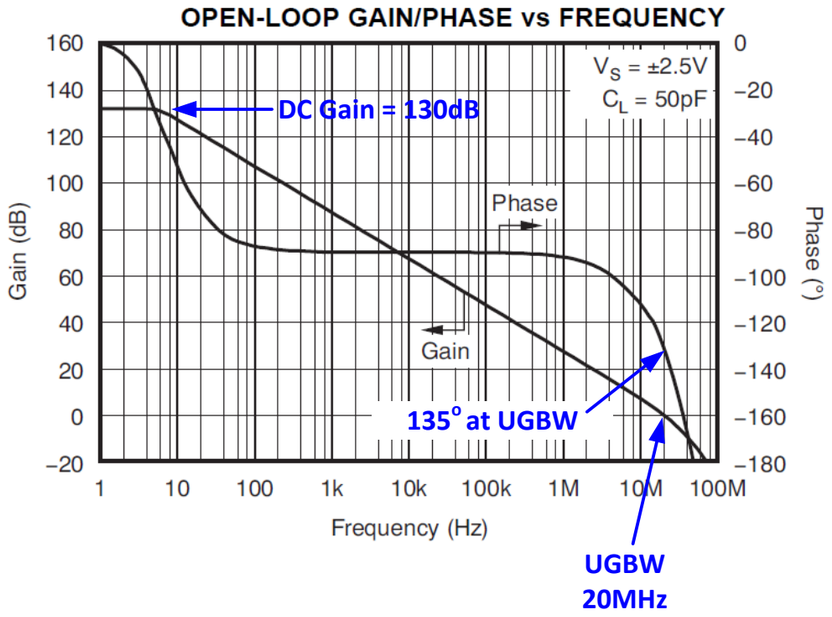
Test Circuit for Aol



Simulated results



Data Sheet Specification



1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for A_{OL} curve

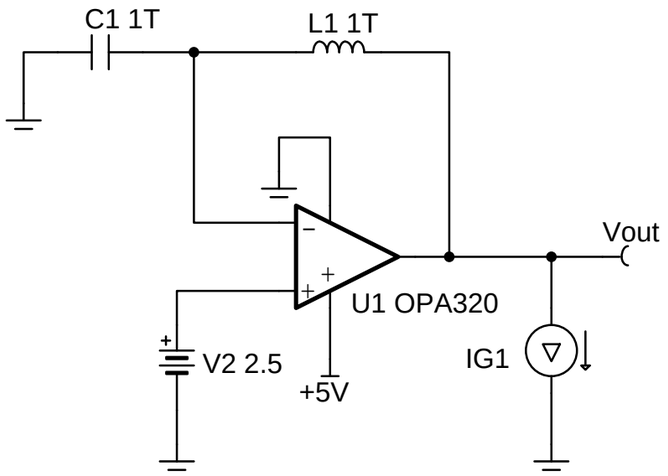
A_{OL} = Vout

Compare key points on simulation results to data sheet curve.

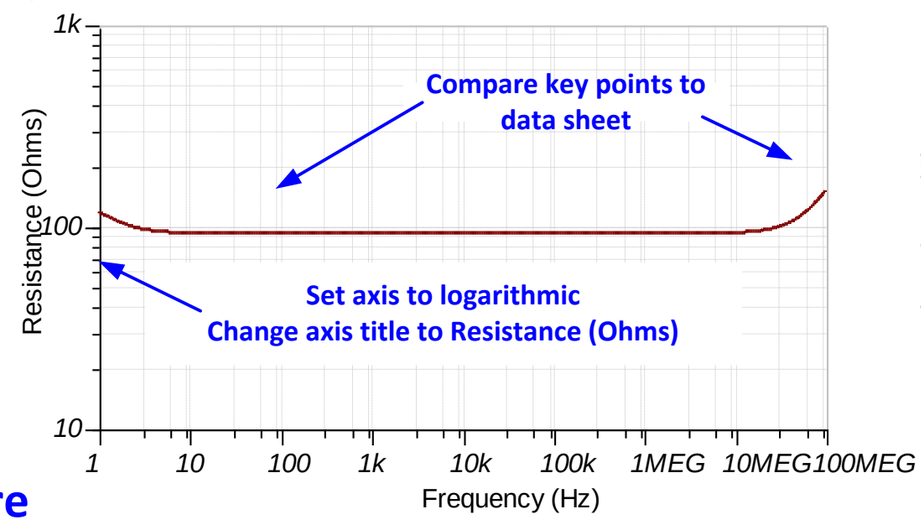
Aol opa320_TG.TSC

Op Amp Model: Open Loop Output Impedance

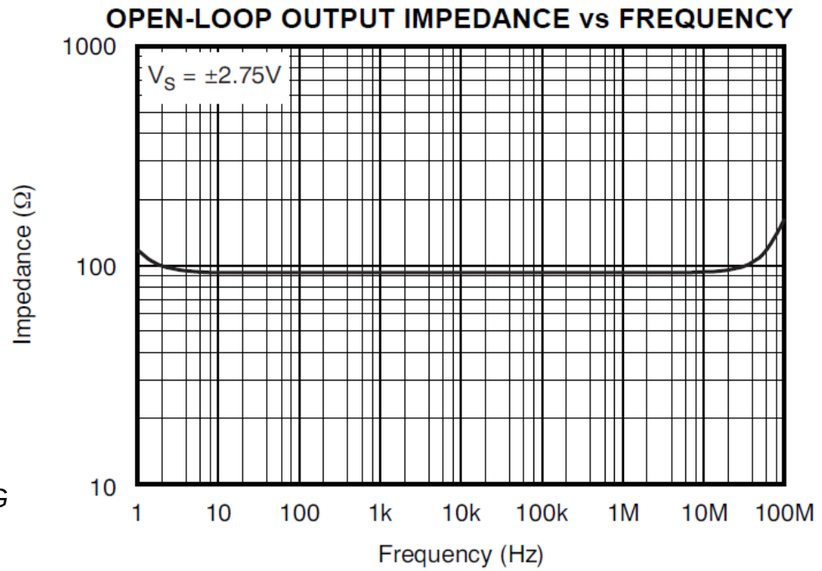
Test Circuit for Aol



Simulated results



Data Sheet Specification



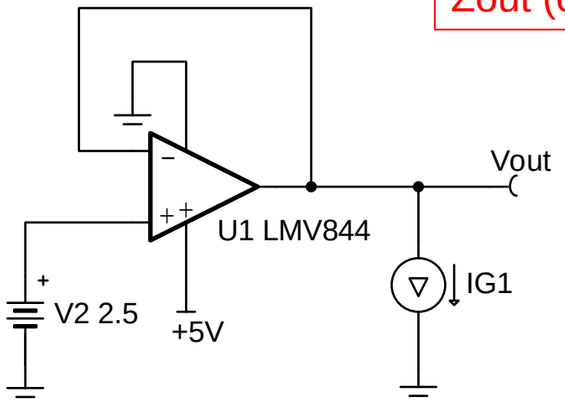
1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for Z_o curve.

Zo(dB) = Vout(dB)
Zo(ohms) = Vout(Logarithmic)

Zo opa320_TG.TSC

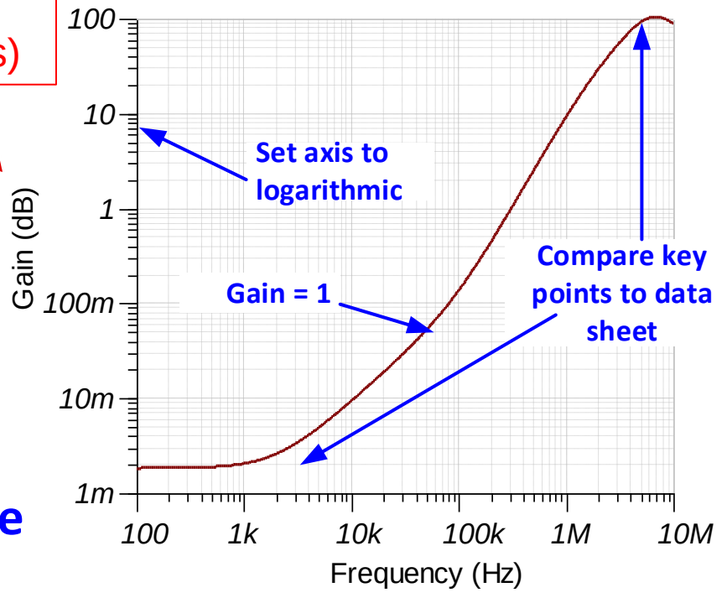
Op Amp Model: Closed loop output impedance

Test Circuit for Zout



Should Be:
Zout (ohms)

Simulated results



Data Sheet Specification

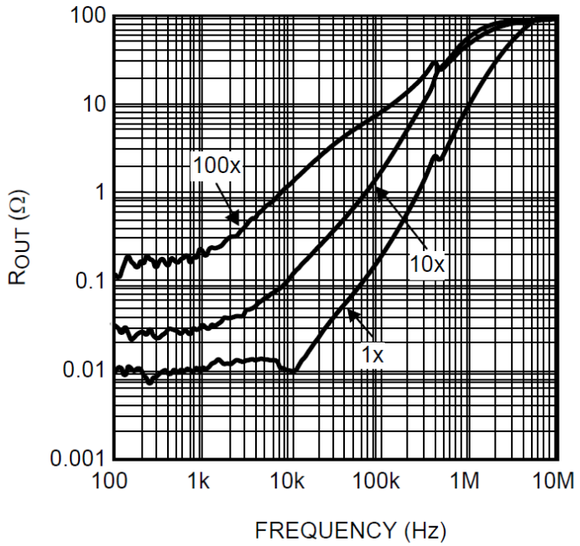


Figure 33. Closed-Loop Output Impedance vs Frequency

1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for Z_{out} curve.

Zout(dB) = Vout(dB)
Zout(ohms) = Vout(Logarithmic)

LMV844Zout_TG.TSC

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Equivalent Circuit: Translate to TINA

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input span(1)	AINP – AINN	0		V_{REF}	V
	Operating input range(1)	AINP	–0.1		V_{REF} + 0.1	V
		AINN	–0.1		+ 0.1	V
C_I	Input capacitance	AINP and AINN terminal to GND		59		pF
	Input leakage current	During acquisition for dc input		5		nA

59pF = 55pF + 4pF

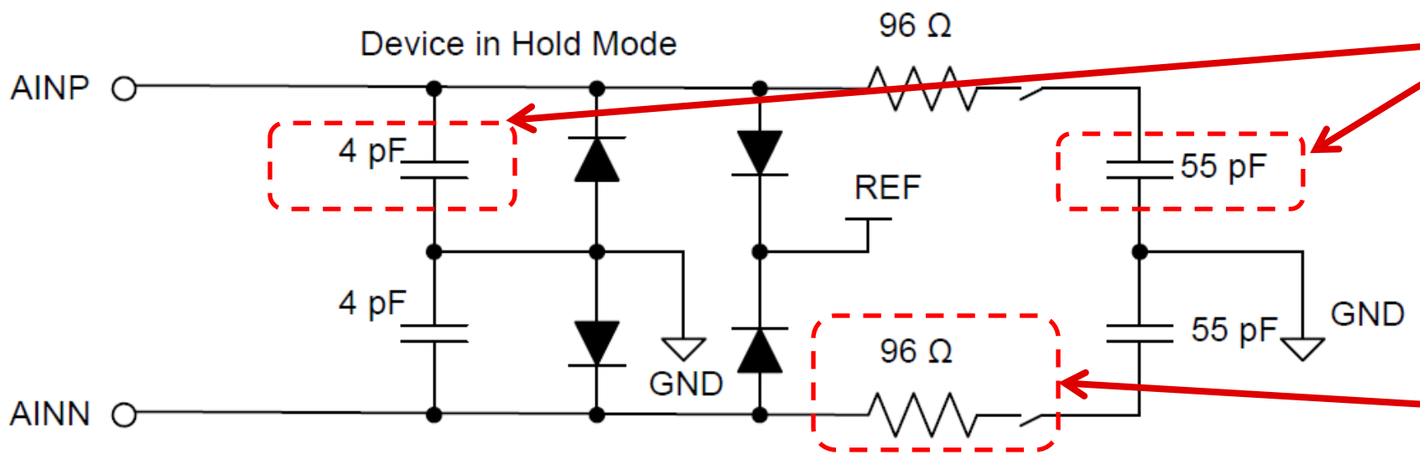


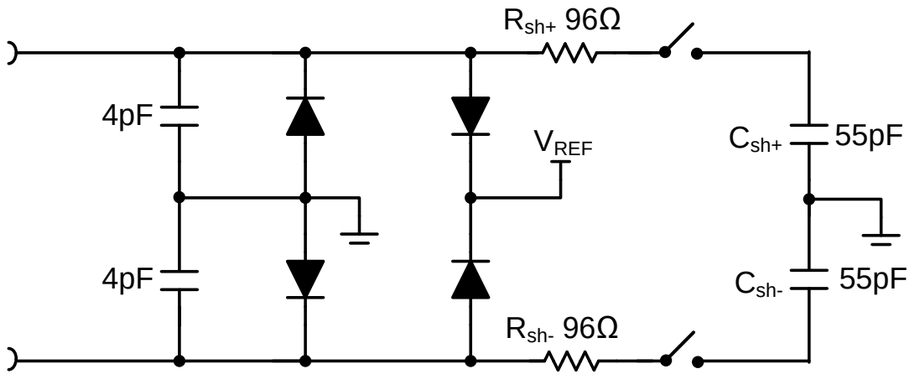
Figure 45. Input Sampling Stage Equivalent Circuit

$$R_{sh} \approx \frac{t_{acq_min}}{100 \cdot C_{sh}}$$

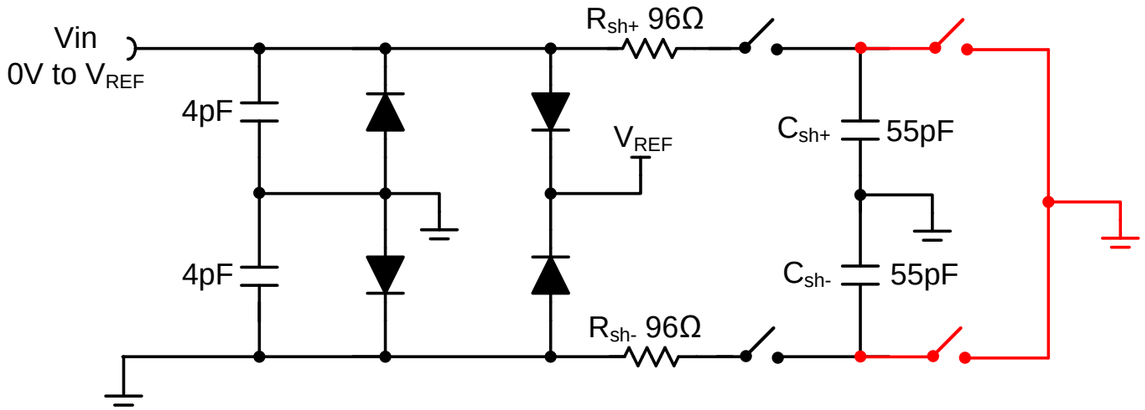
$$R_{sh} \approx \frac{290ns}{100 \cdot 55pF} = 53\Omega$$

Simplifying the input model

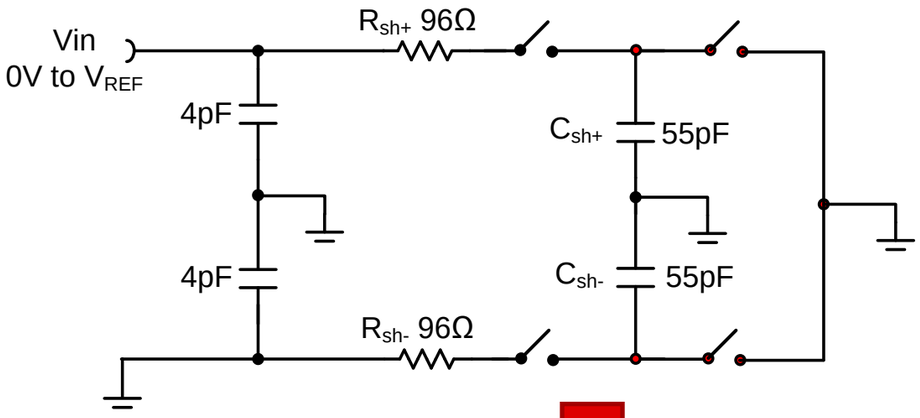
1) Input Circuit from the data sheet



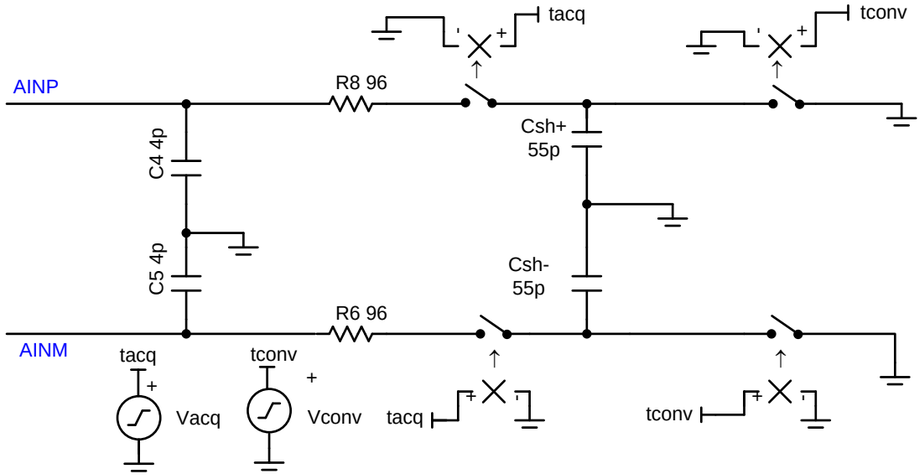
2) Add the sample and hold reset circuit



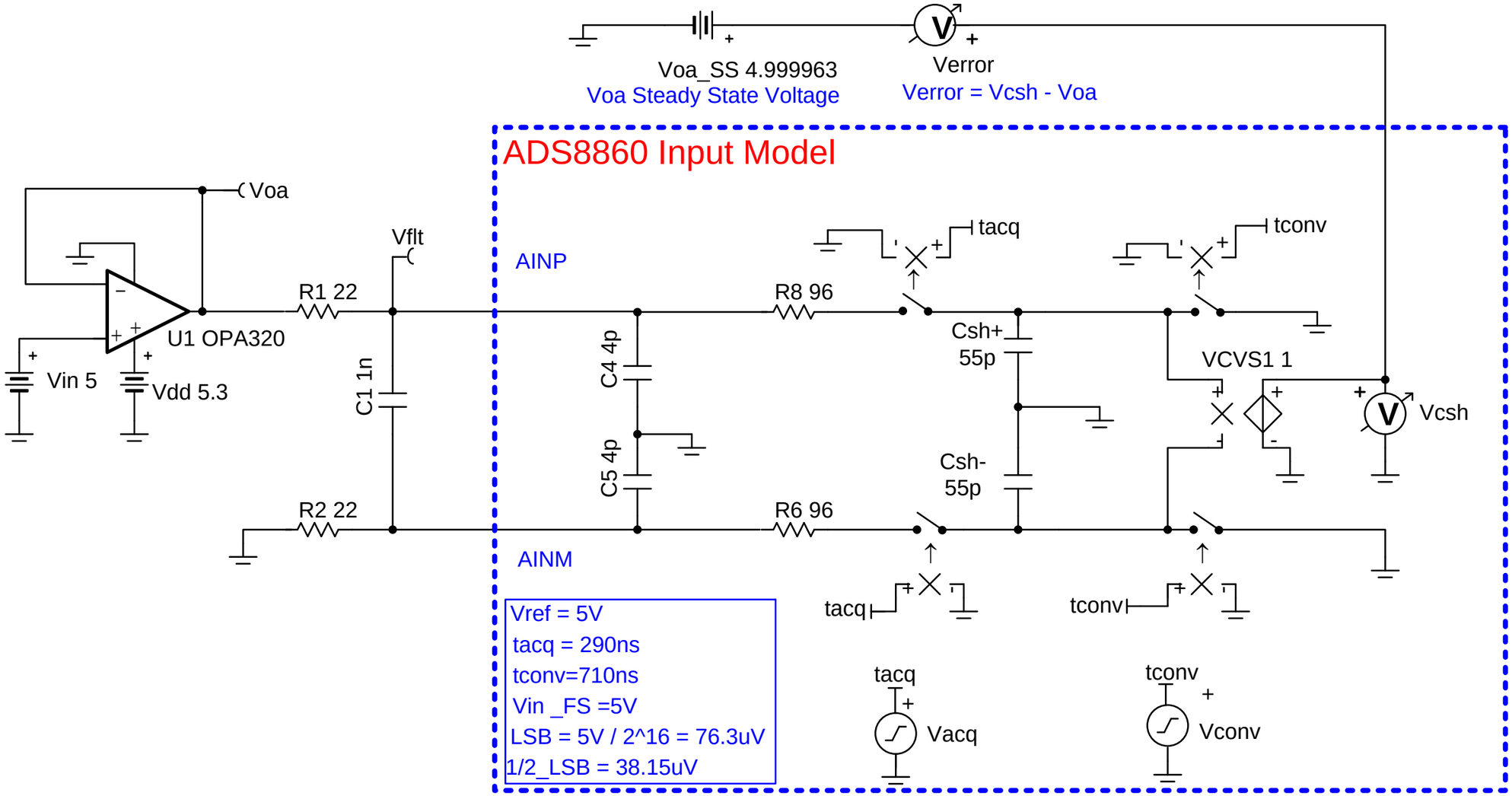
3) Diodes are reverse bias



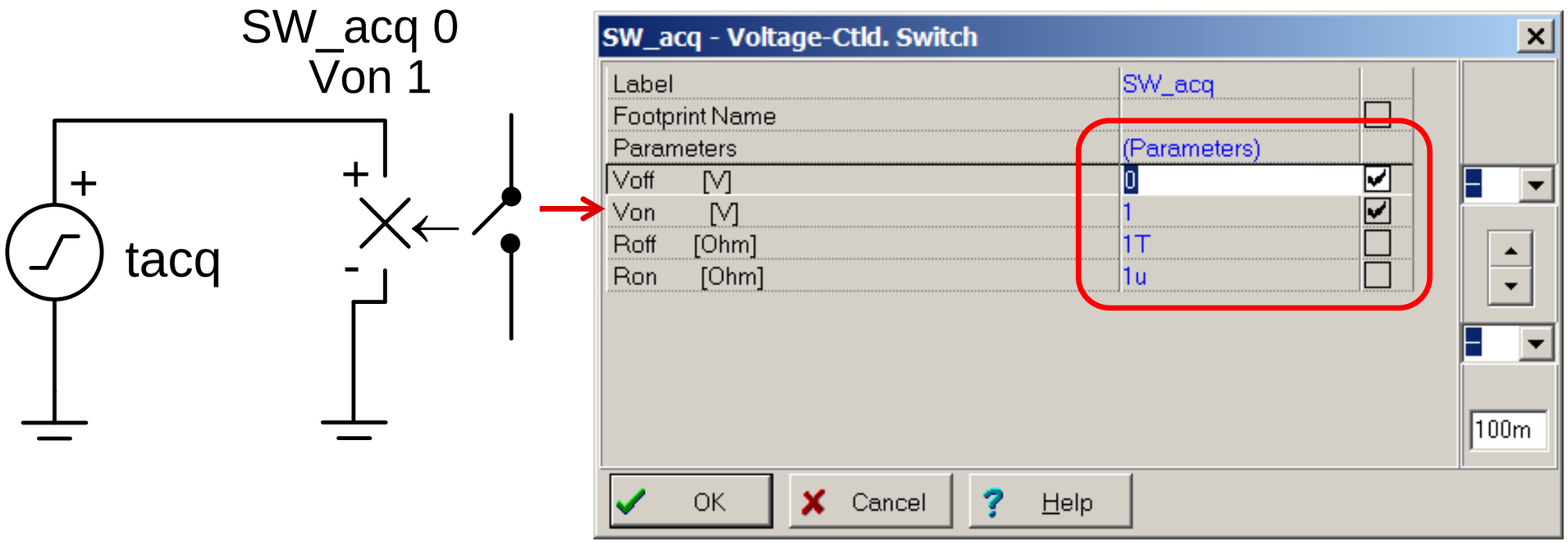
4) TINA Spice Model



TINA SPICE Equivalent Model



Configure the voltage controlled switch

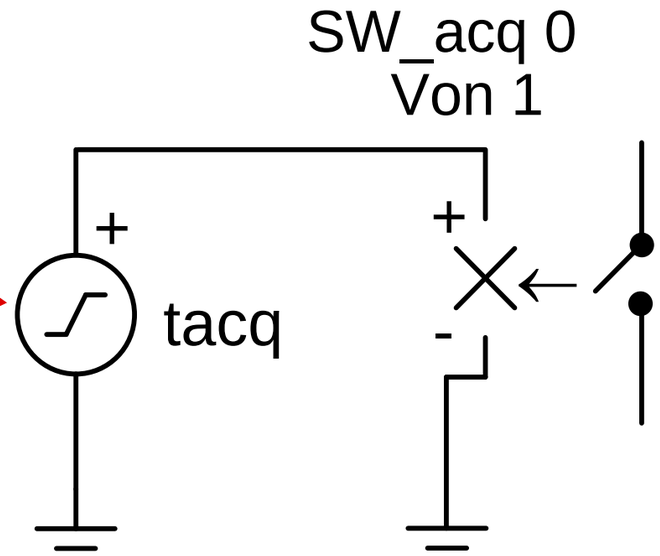


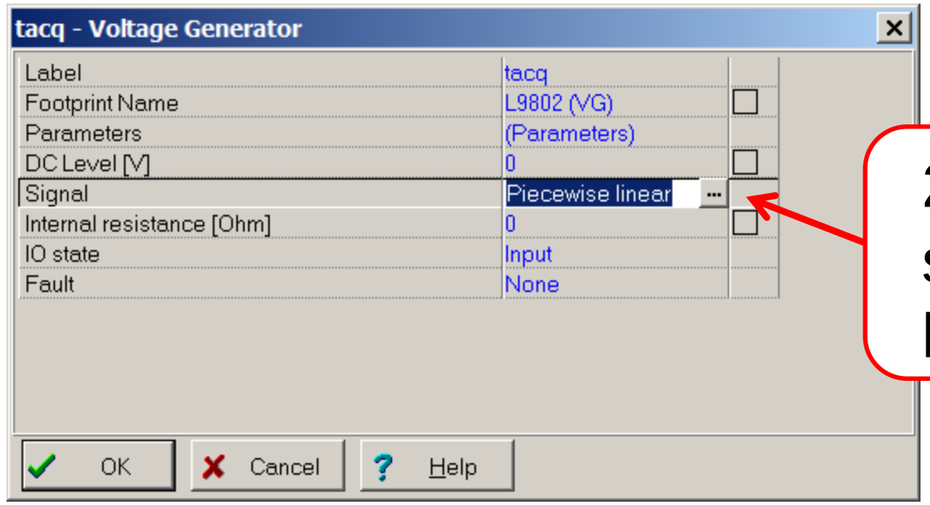
Set all parameters as shown.

Default Roff=1GΩ and Ron=0Ω will impact accuracy.

Configure the signal source to control the switch

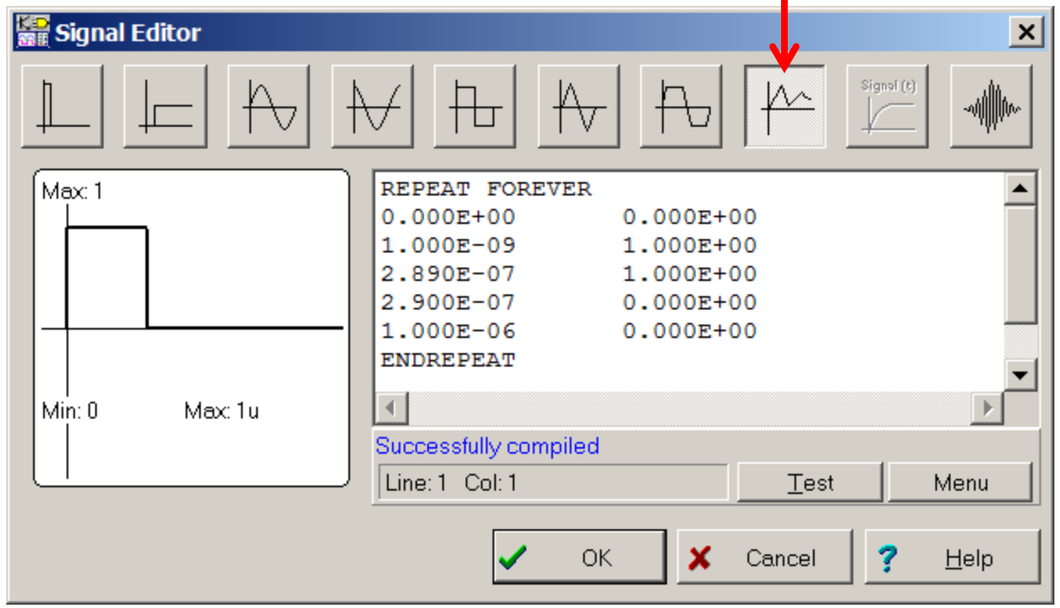
1. Click on source to select and edit switch control signal



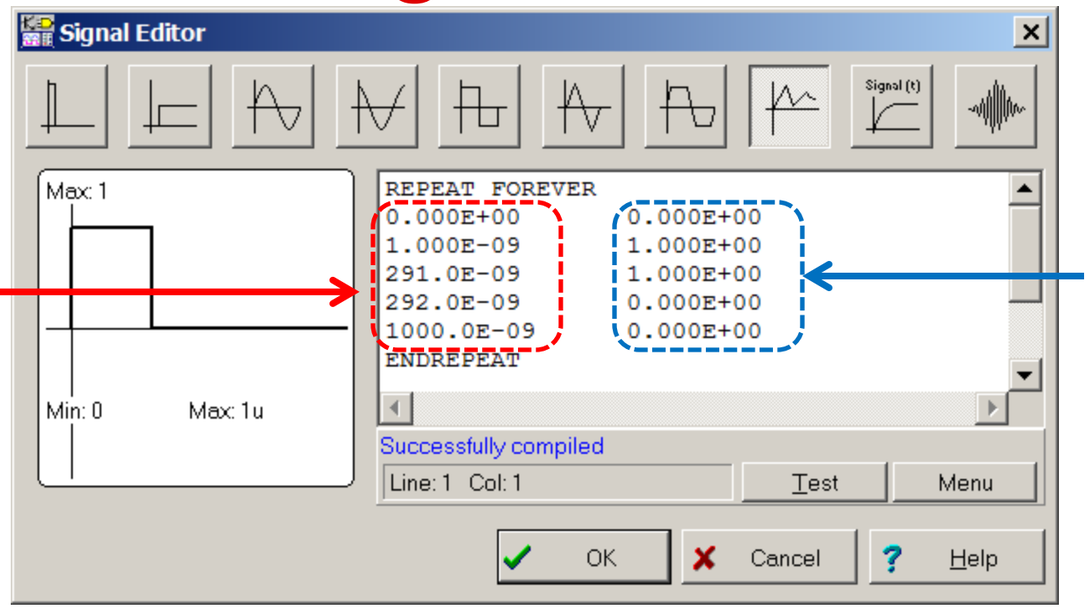


2. Under signal, click here to edit.

3. Select "Piecewise linear"

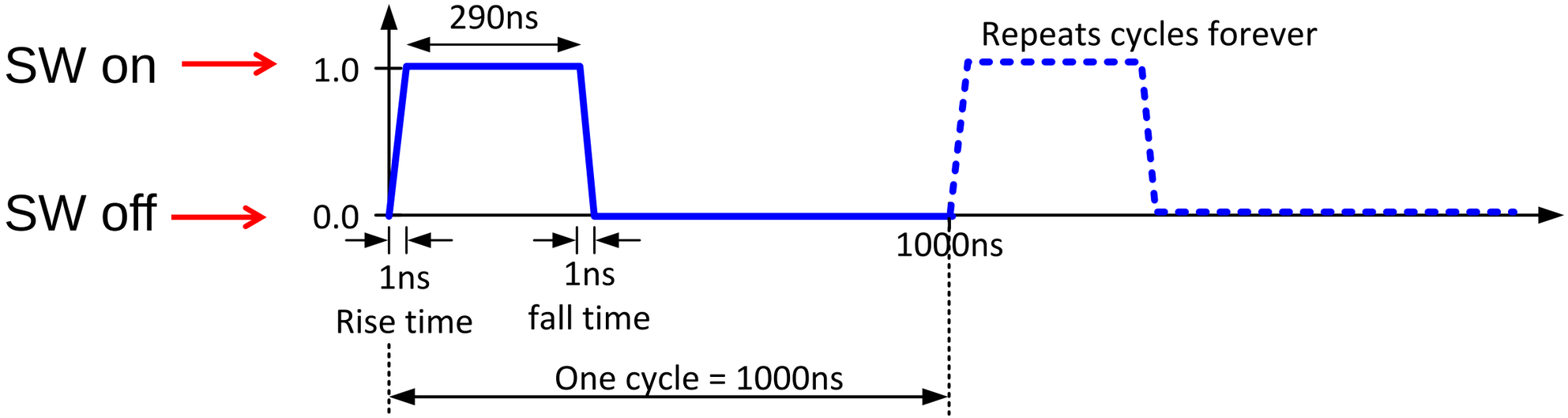


Configure the signal source to control the switch

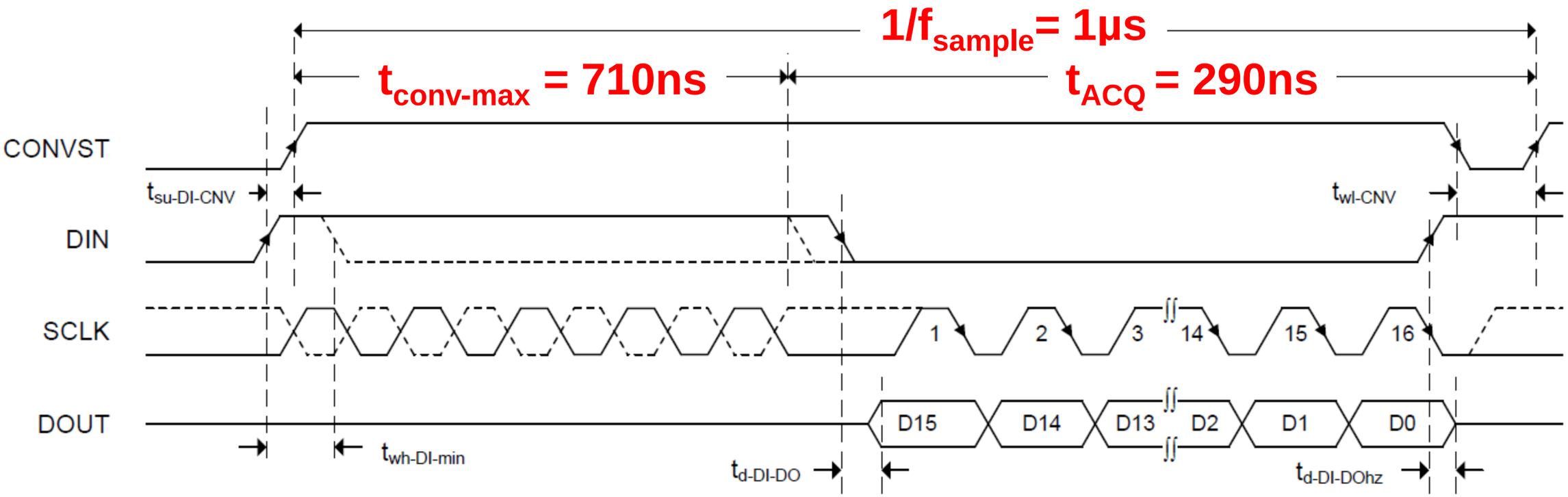


Time

Voltage levels
On: V ≥ 1V
Off: V ≤ 0V



Timing diagram



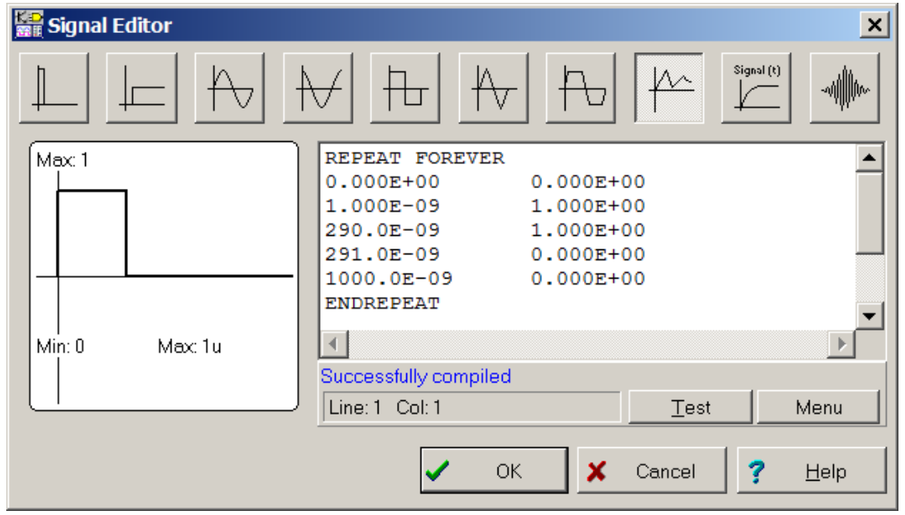
Parameter		MIN	TYP	MAX	UNIT
t_{acq}	Acquisition time	290			ns
t_{conv}	Conversion time	500		710	ns

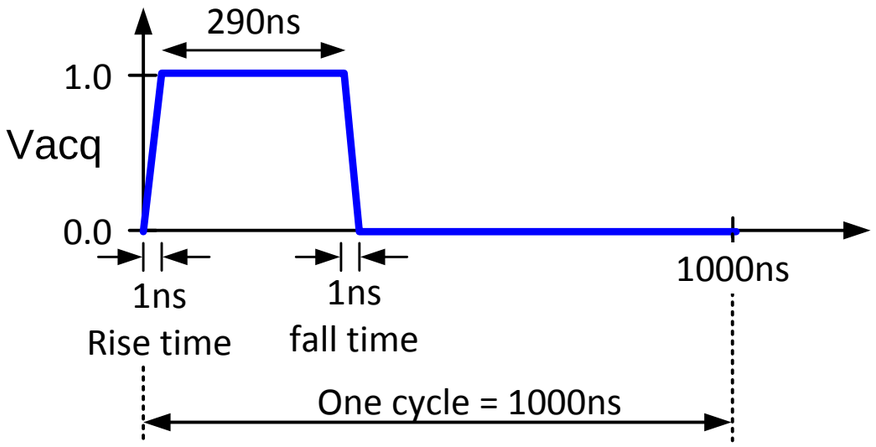
$1/f_{sample} = 290ns + 710ns$

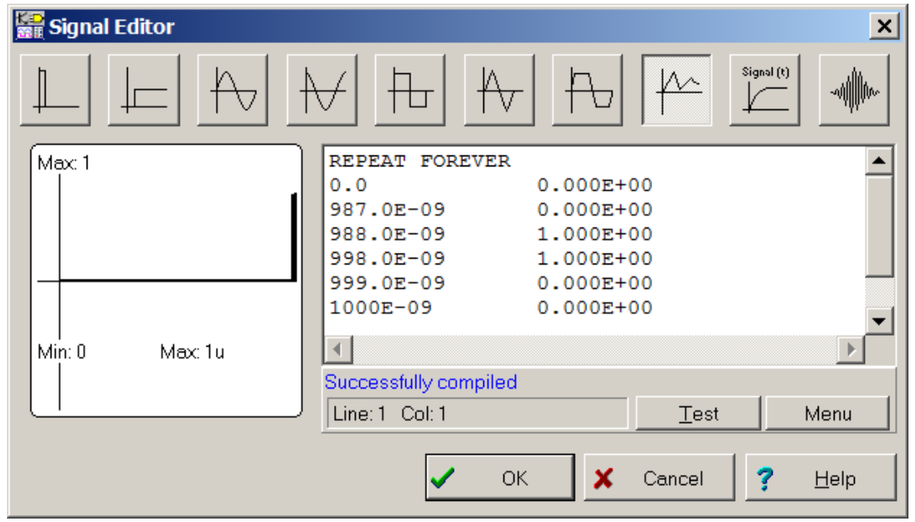
$1/f_{sample} = 1\mu s$

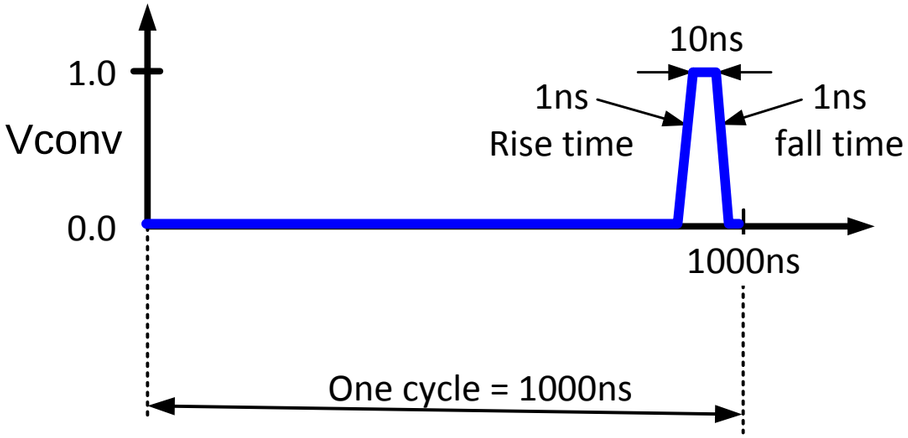
$f_{sample} = 1MHz$

Example simulation: simulator settings

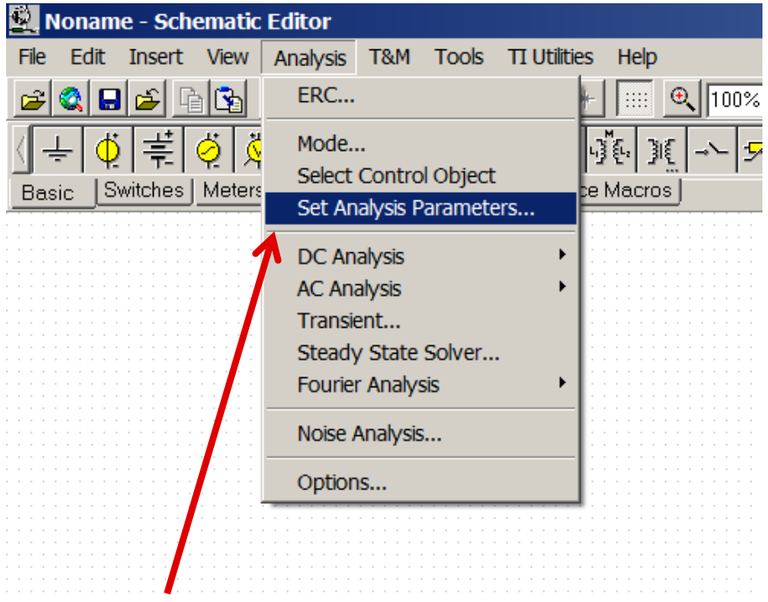




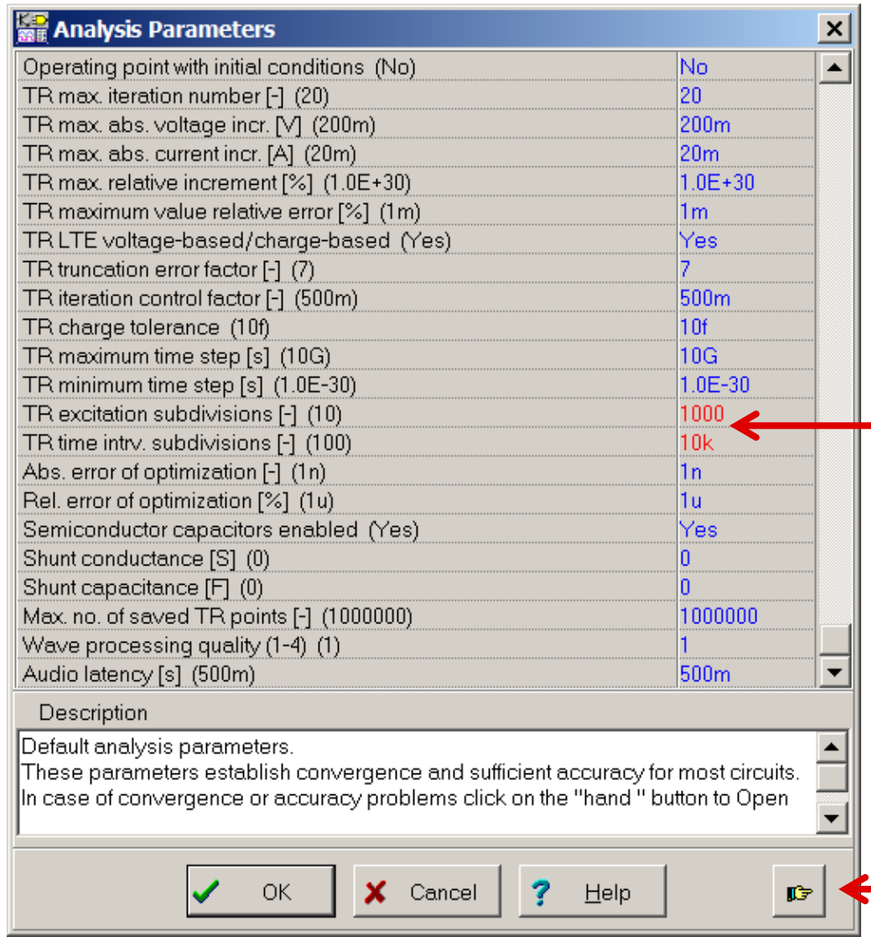




Optimizing Simulation Results



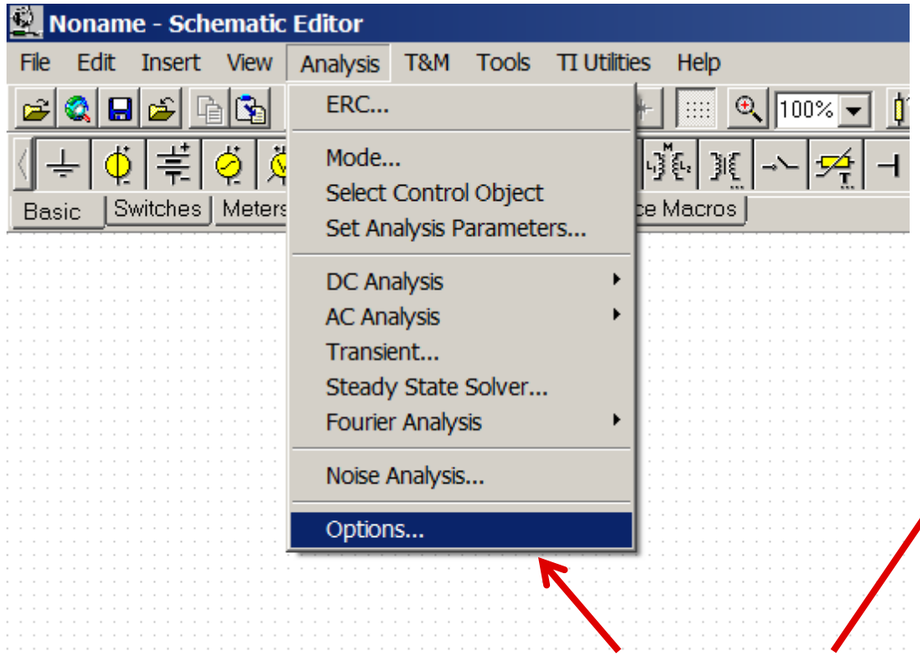
"Set Analysis Parameters" adjusts how the simulator math engine operates.

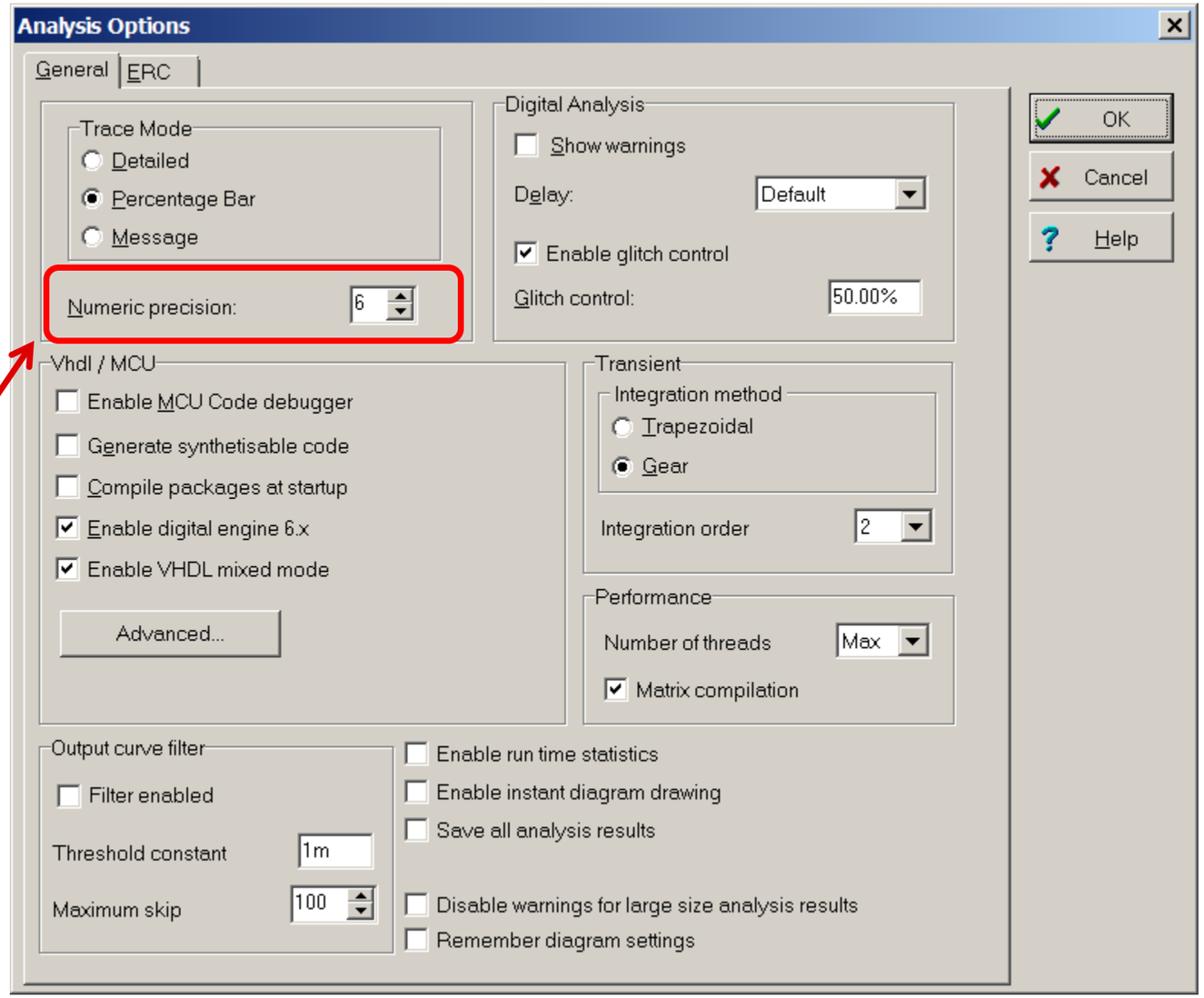


TR excitation subdivisions = 1000
TR time intrv. subdivisions = 10k
This increases the number of points vs time so that transient behaviors aren't obscured.

Press this button to expand the list.

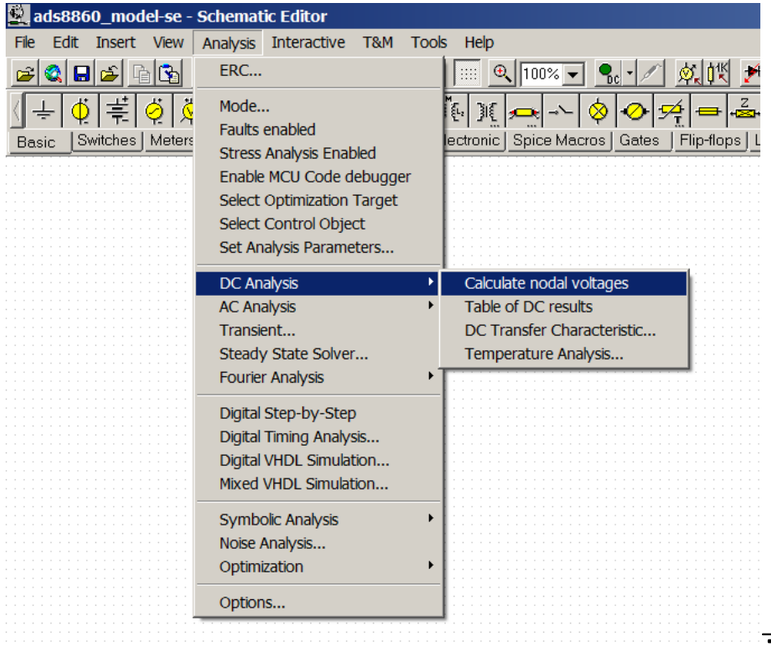
Optimizing Simulation Results



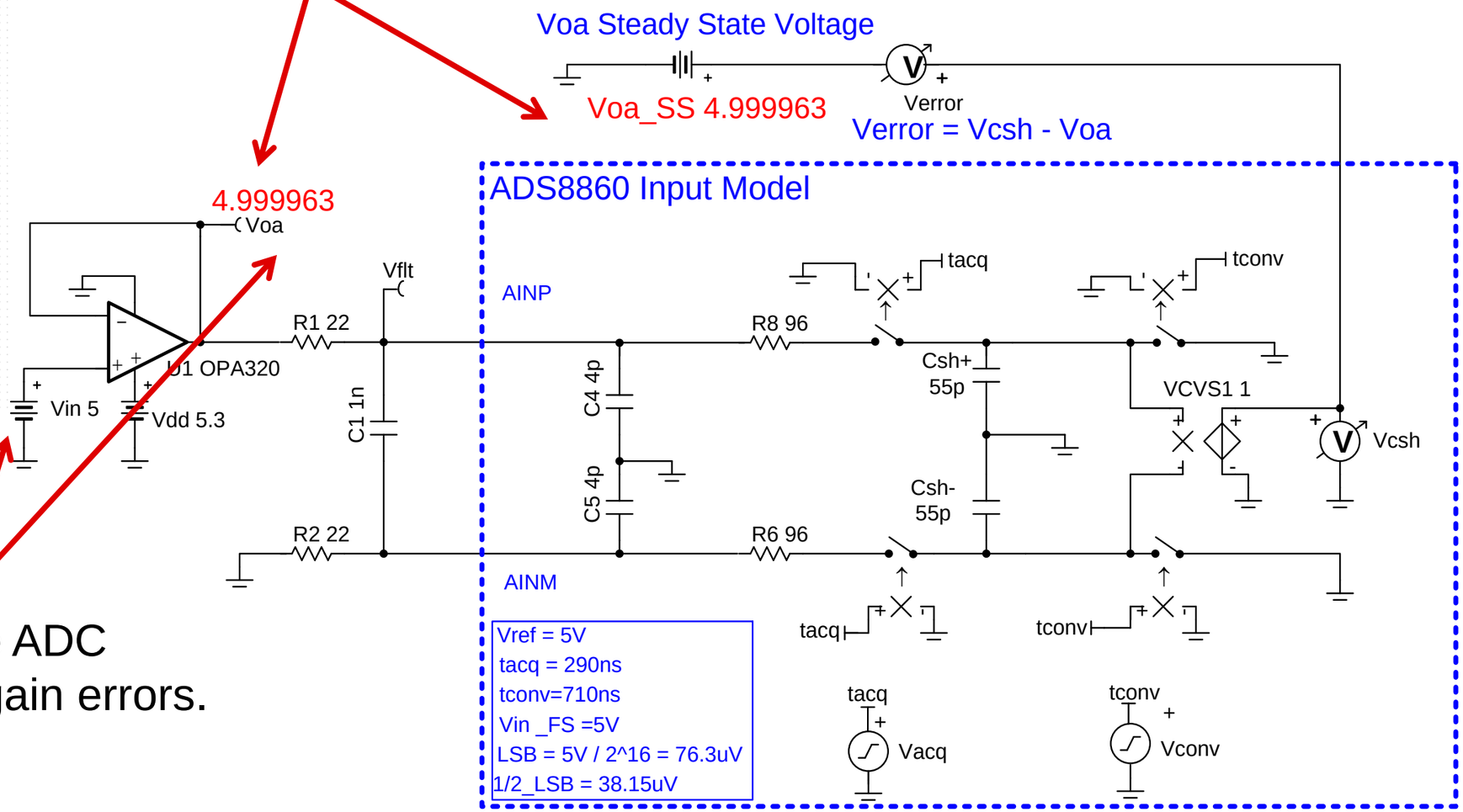


Set the “numeric precision” to 6 digits. This will allow us to see dc operating points to six digits. The importance of this is highlighted on the next slide.

Steady State Simulation Results

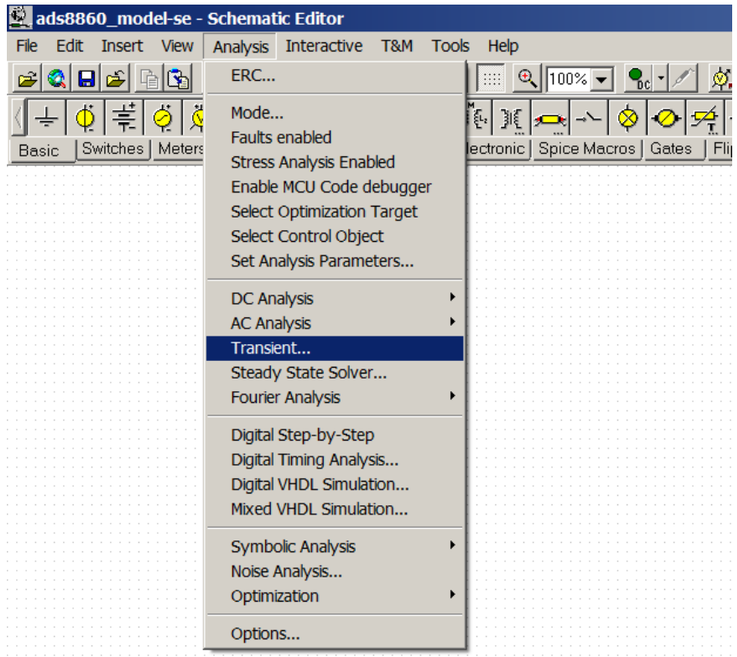


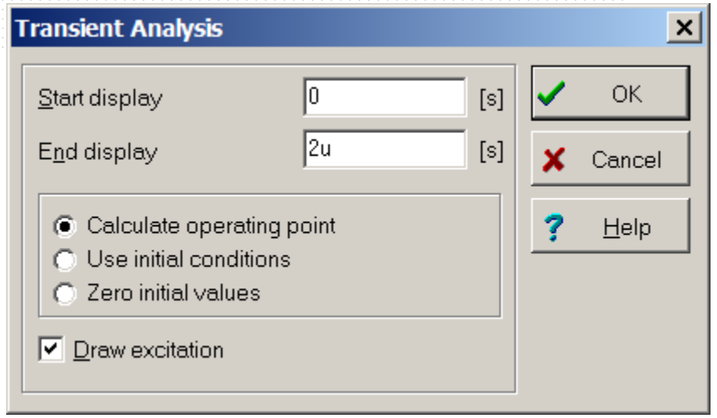
Set the output source to match the steady state ADC input.

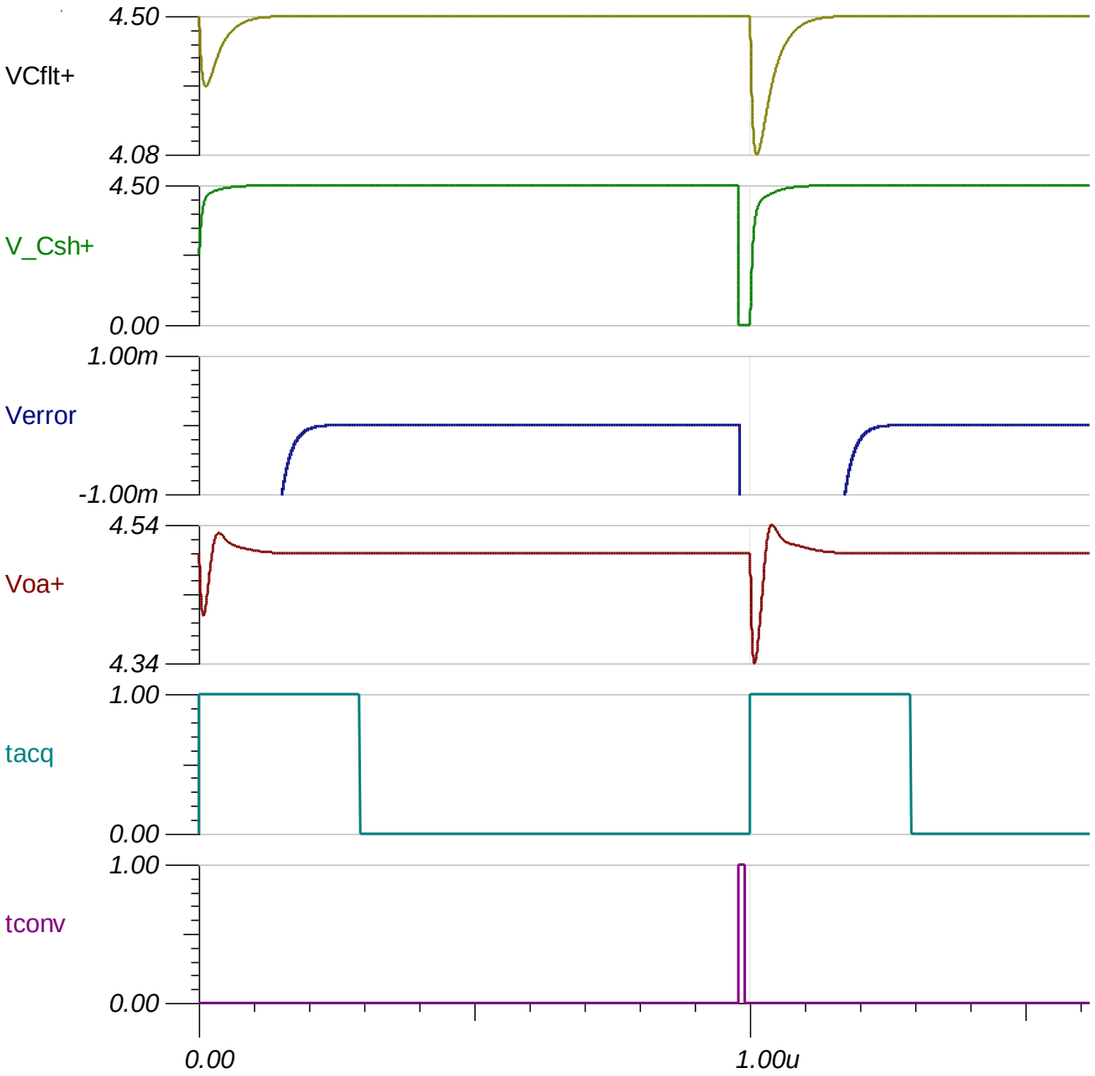


The steady state input to the ADC includes amplifier offset an gain errors.

Example simulation: simulator results







Input to ADC across Charge bucket filter

Internal ADC sample and hold capacitor

Error in ADC settling sampled signal

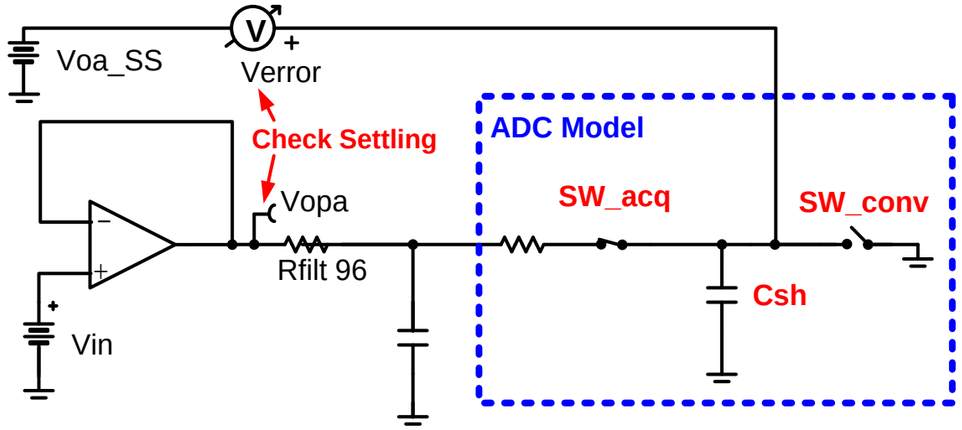
Op amp output

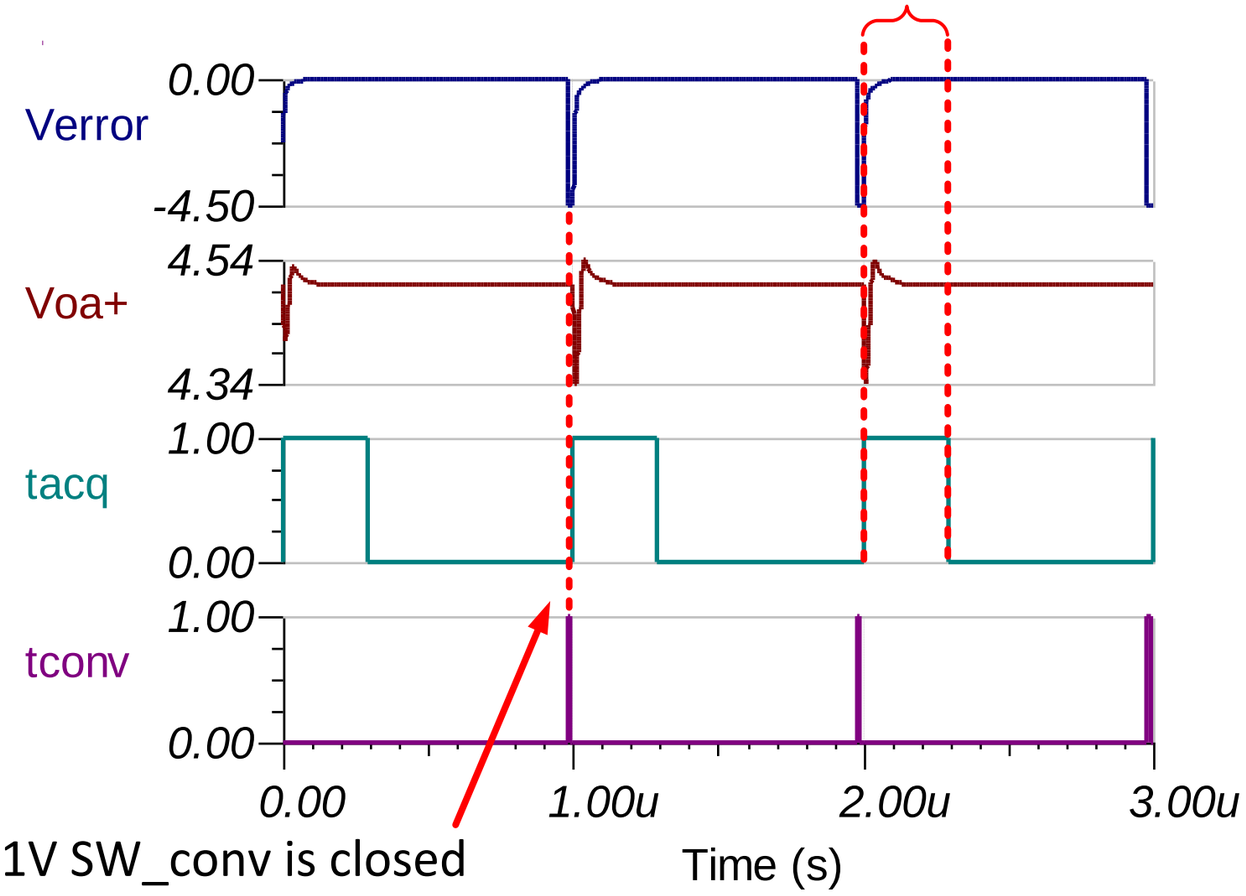
Acquisition switch control

Conversion switch control

Key Result: Error Signal

When tacq = 1V SW_acq is closed
Verror and Vopa must settle in this window





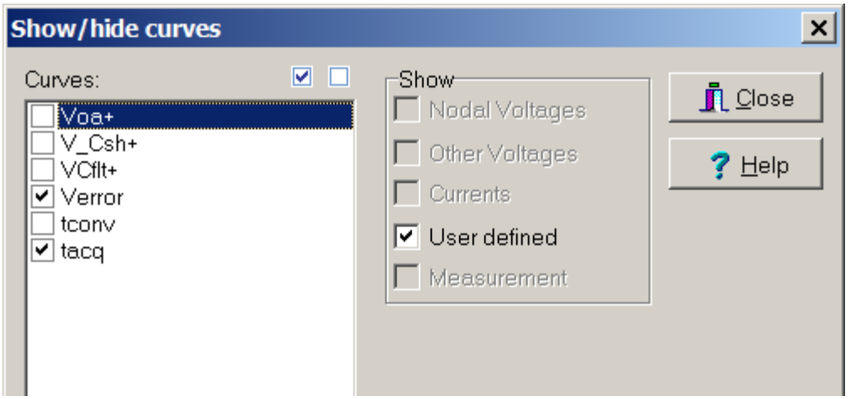
When tconv = 1V SW_conv is closed
This resets the internal S &H Capacitor Csh

Zoom in on Error Signal

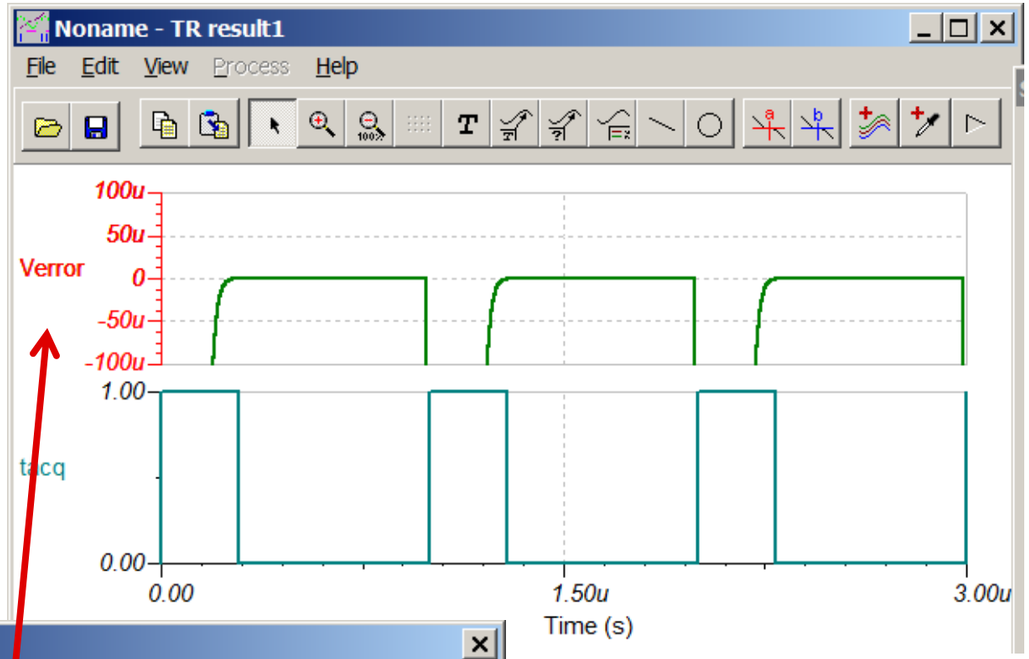
$N = 16$ — Number of bits

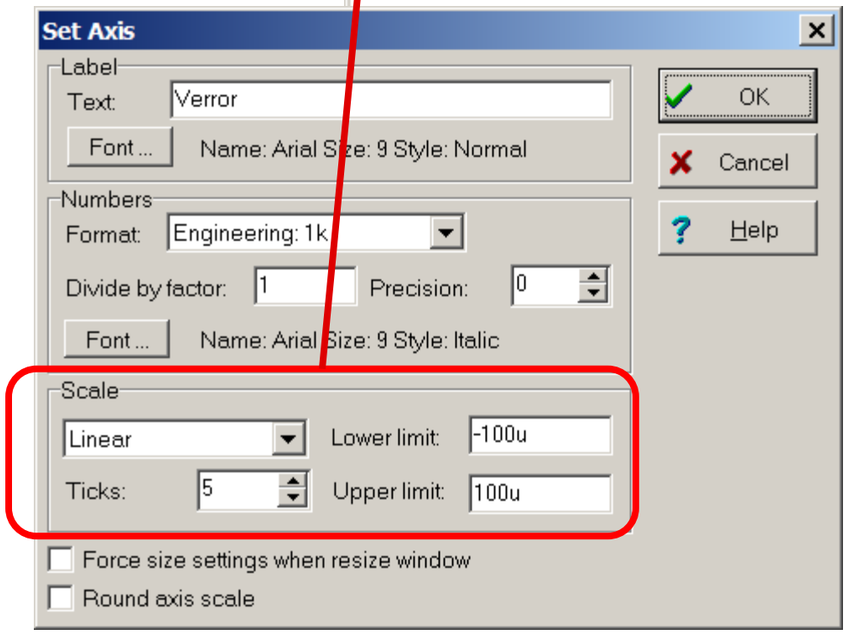
$$\mathrm{LSB} = \frac{FSR}{2^N} = \frac{5.0V}{2^{16}} = 76.3\mu V$$ — Resolution

$0.5 \cdot \mathrm{LSB} = 38.1\mu V$ — Target Error



Use “view>show / hide curves” to focus on most important curves.





Click on axis and adjust the scale relative to LSB resolution.

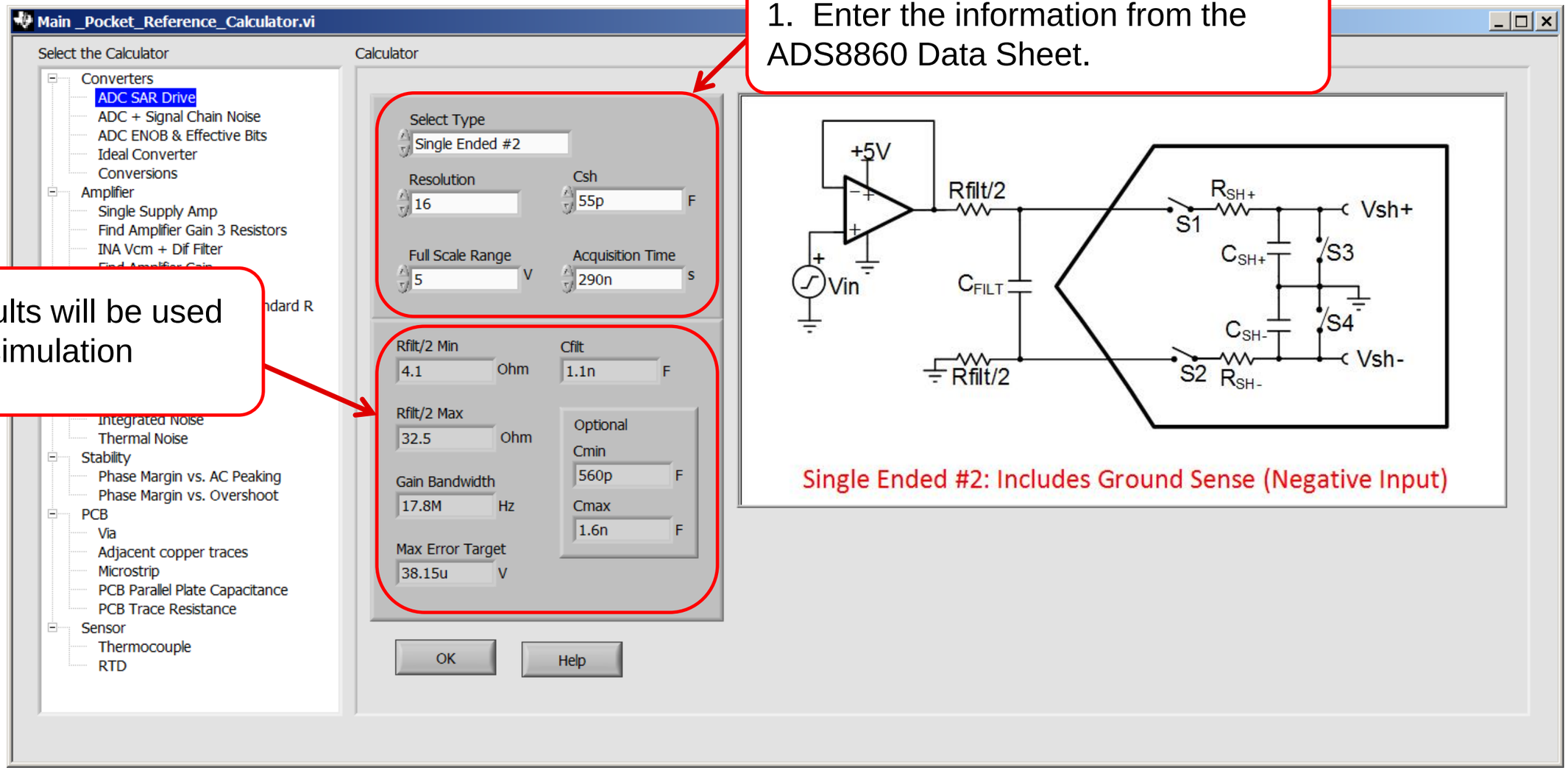
Agenda

1. SAR Operation Overview
2. Select the data converter
3. Use the Calculator to find amplifier and RC filter
4. Find the Op Amp
5. Verify the Op Amp Model
6. Building the SAR Model
7. Refine the Rfilt and Cfilt values
8. Final simulations
9. Measured Results
10. SAR Drive Calculator Algorithm

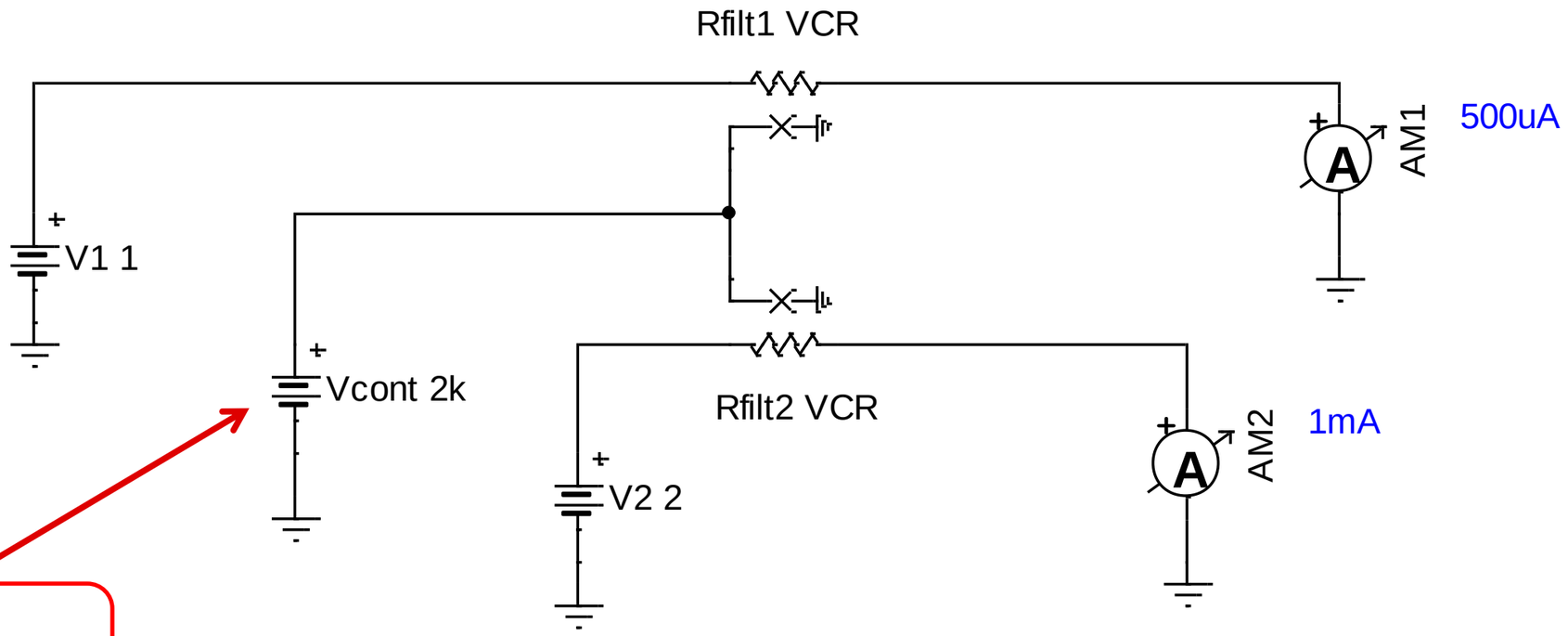
Remember: ADS8860 example calculator results

1. Enter the information from the ADS8860 Data Sheet.

2. Results will be used in the simulation



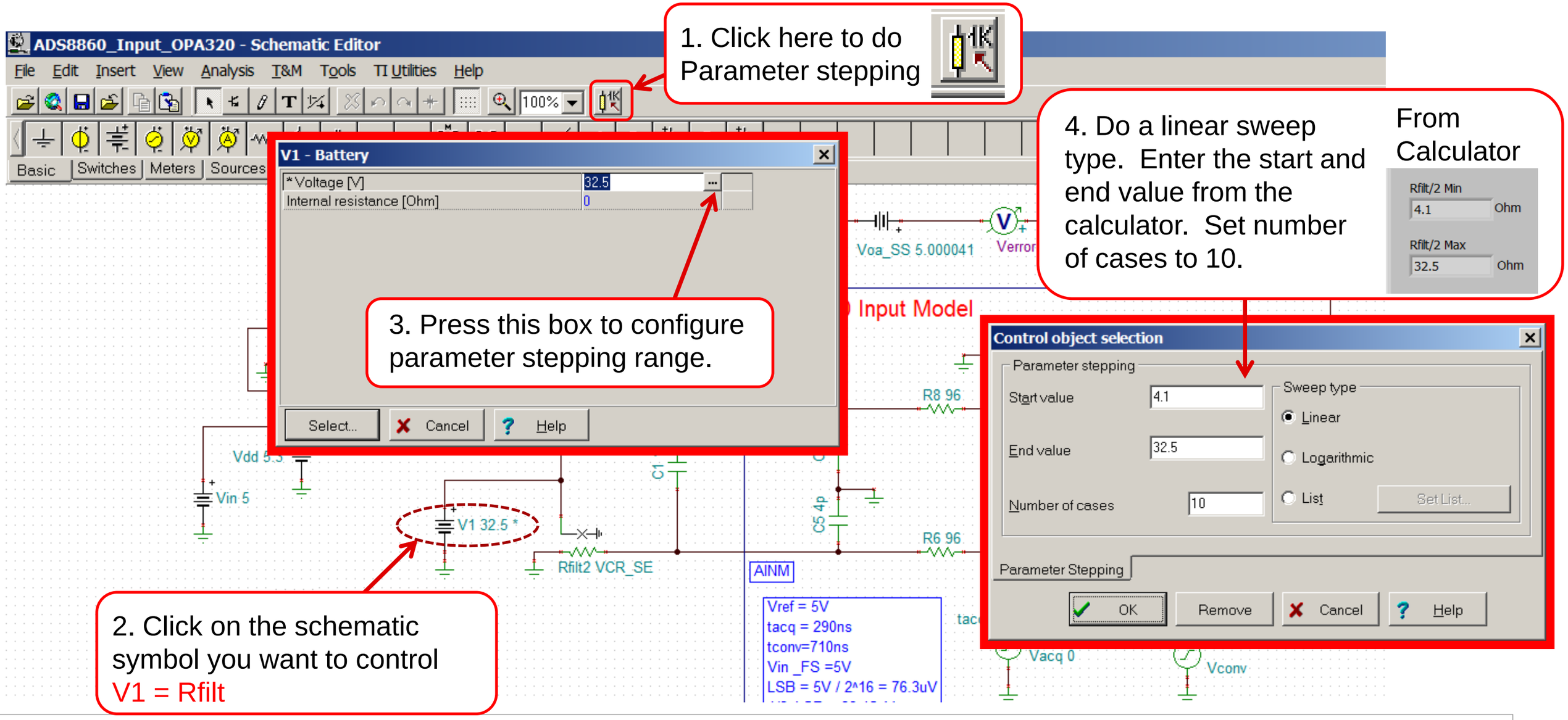
Trick: Voltage controlled resistor



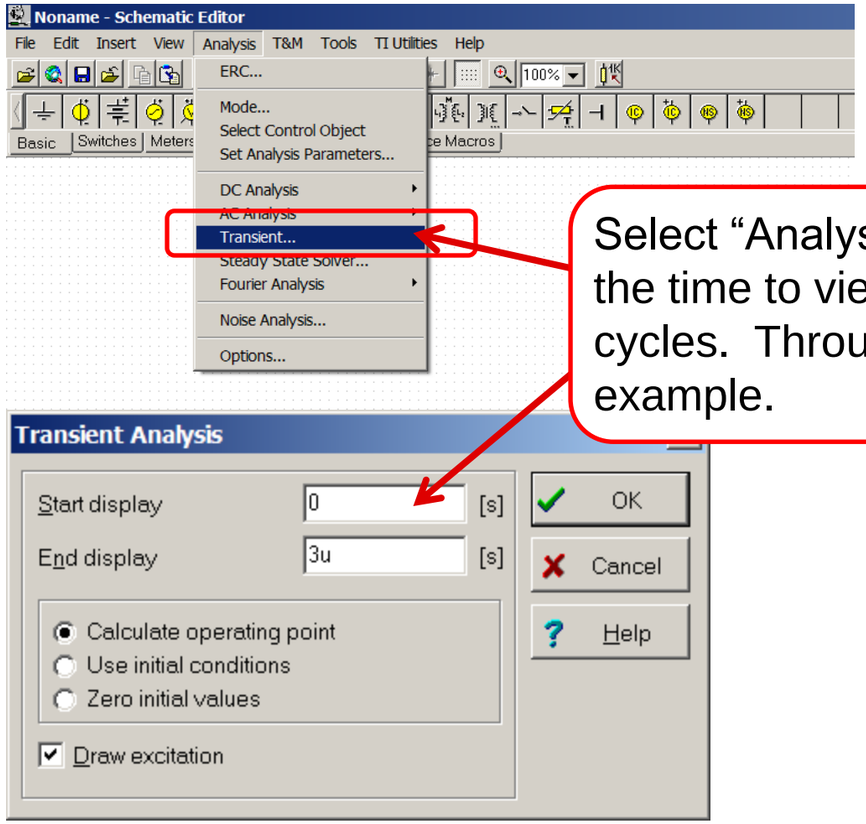
The resistance for both resistors is equal to Vcont.

VCR_Test.TSC

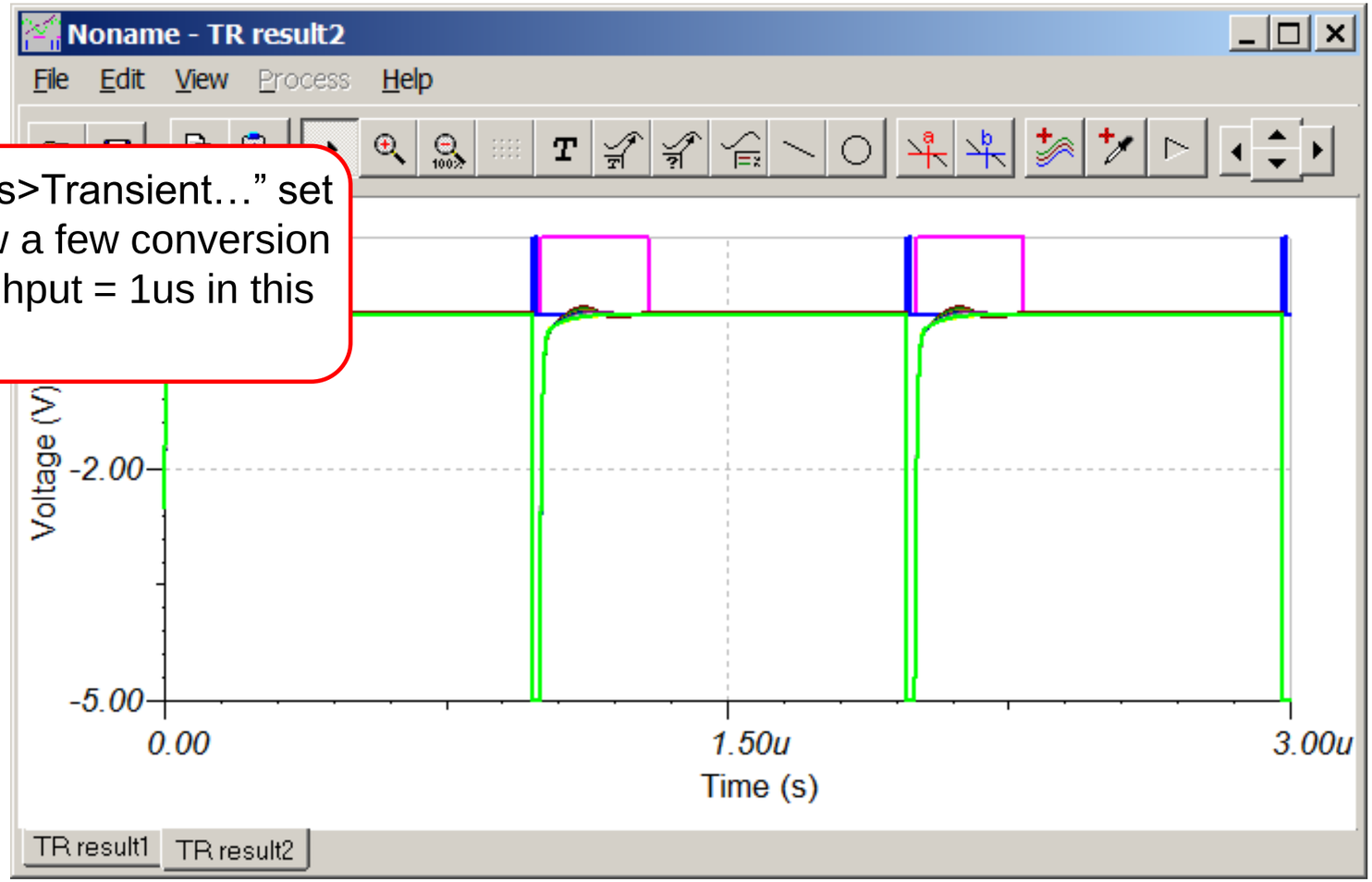
Use Parameter Stepping on Rfilt



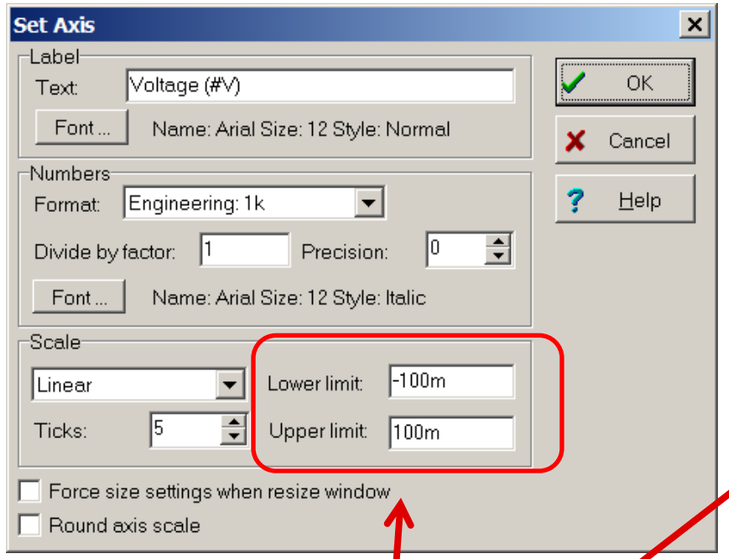
Run a Transient analysis

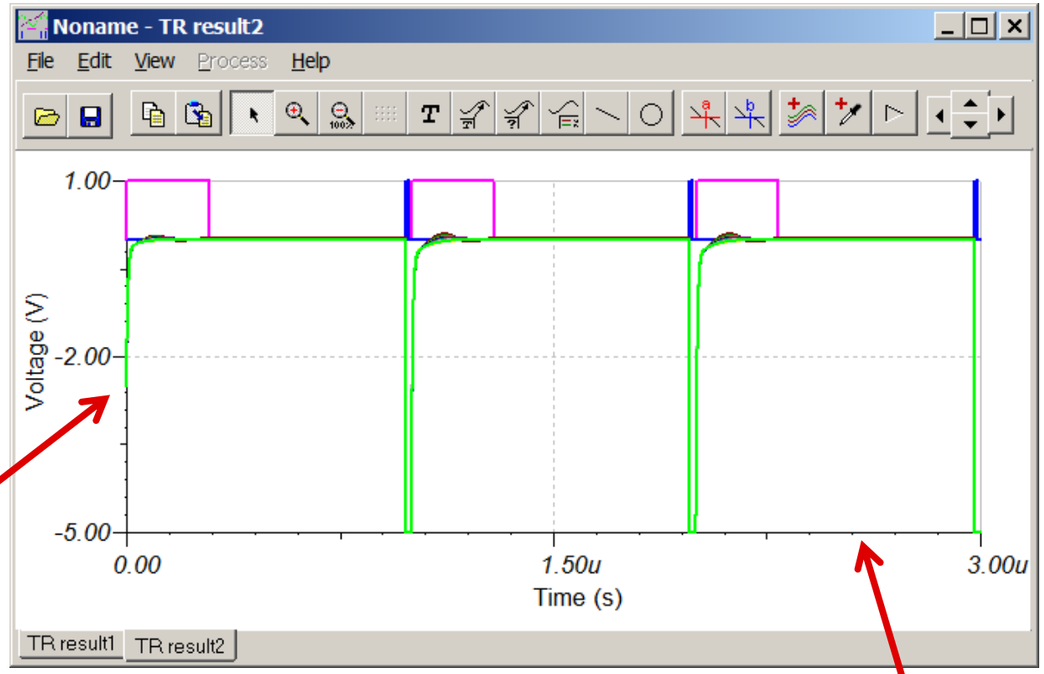


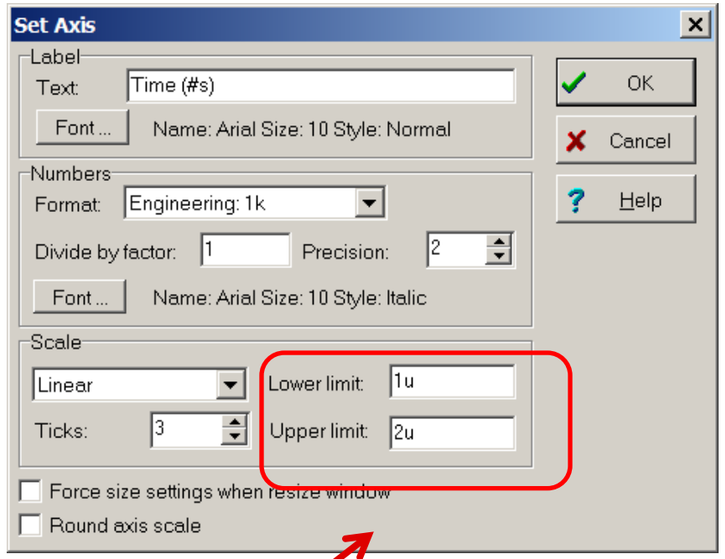
Select “Analysis>Transient…” set the time to view a few conversion cycles. Throughput = 1us in this example.



Adjust the X and Y axis





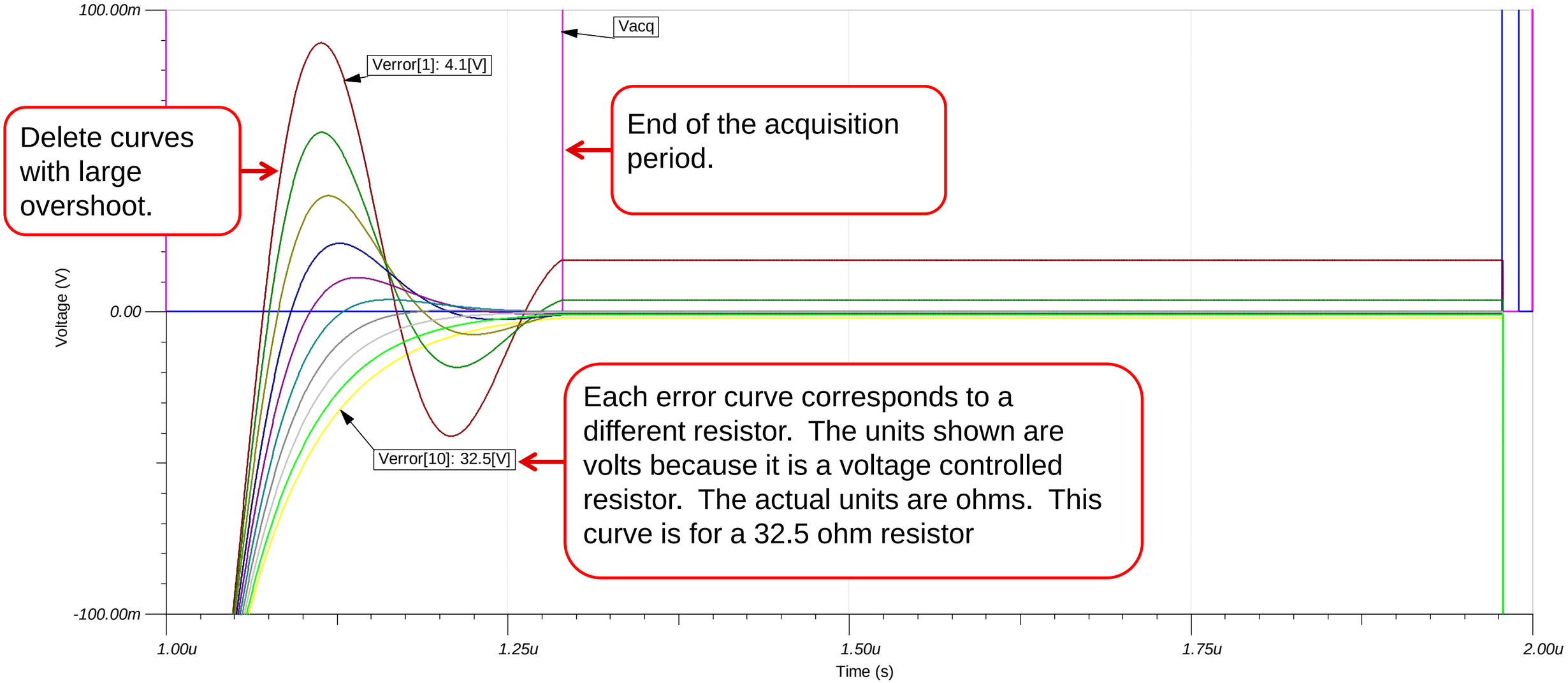


Click on axis and change the vertical range to ±100mV

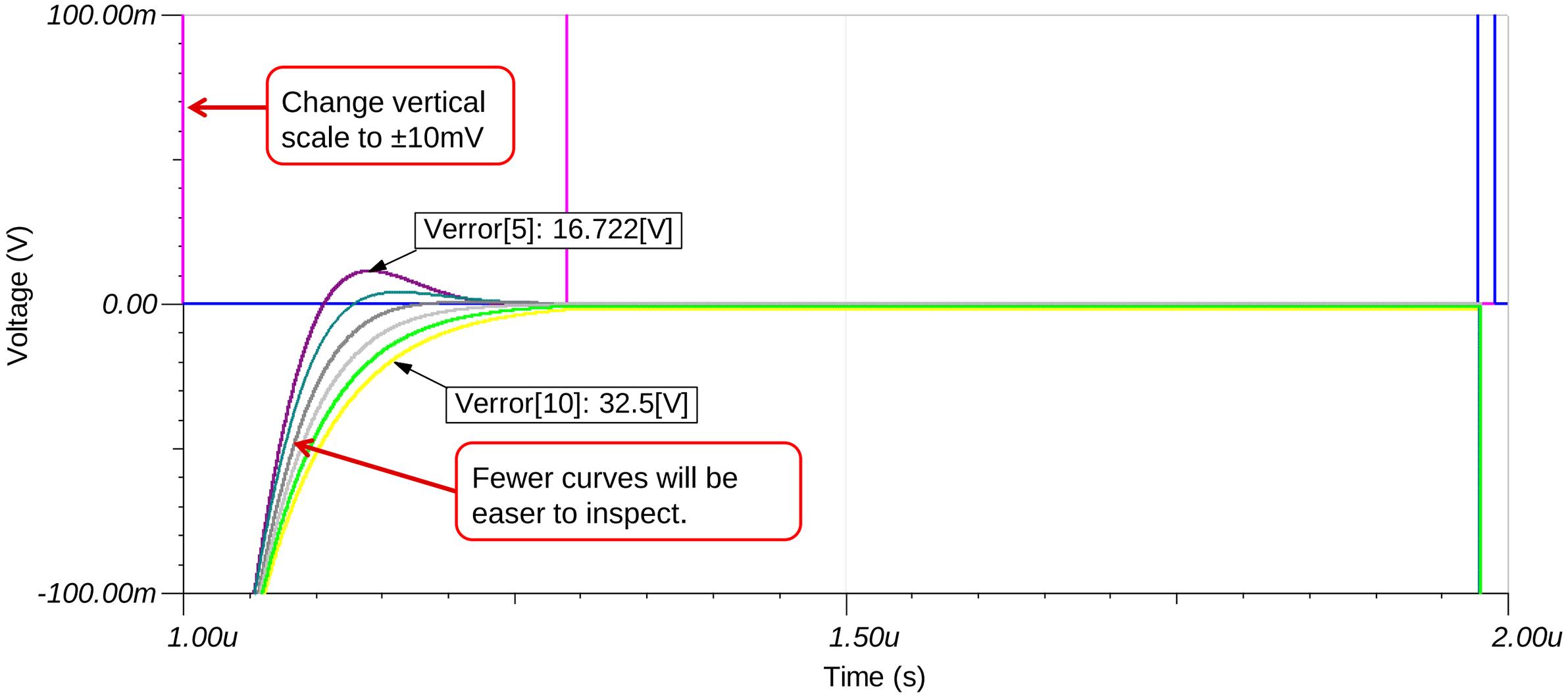
Click on axis and change the horizontal range to show 1 acquisition cycle.
Always ignore first cycle!

ADS8860_Input_OPA320 - 1st.TSC

Error for R = 4.1 ohms…32.5 ohms

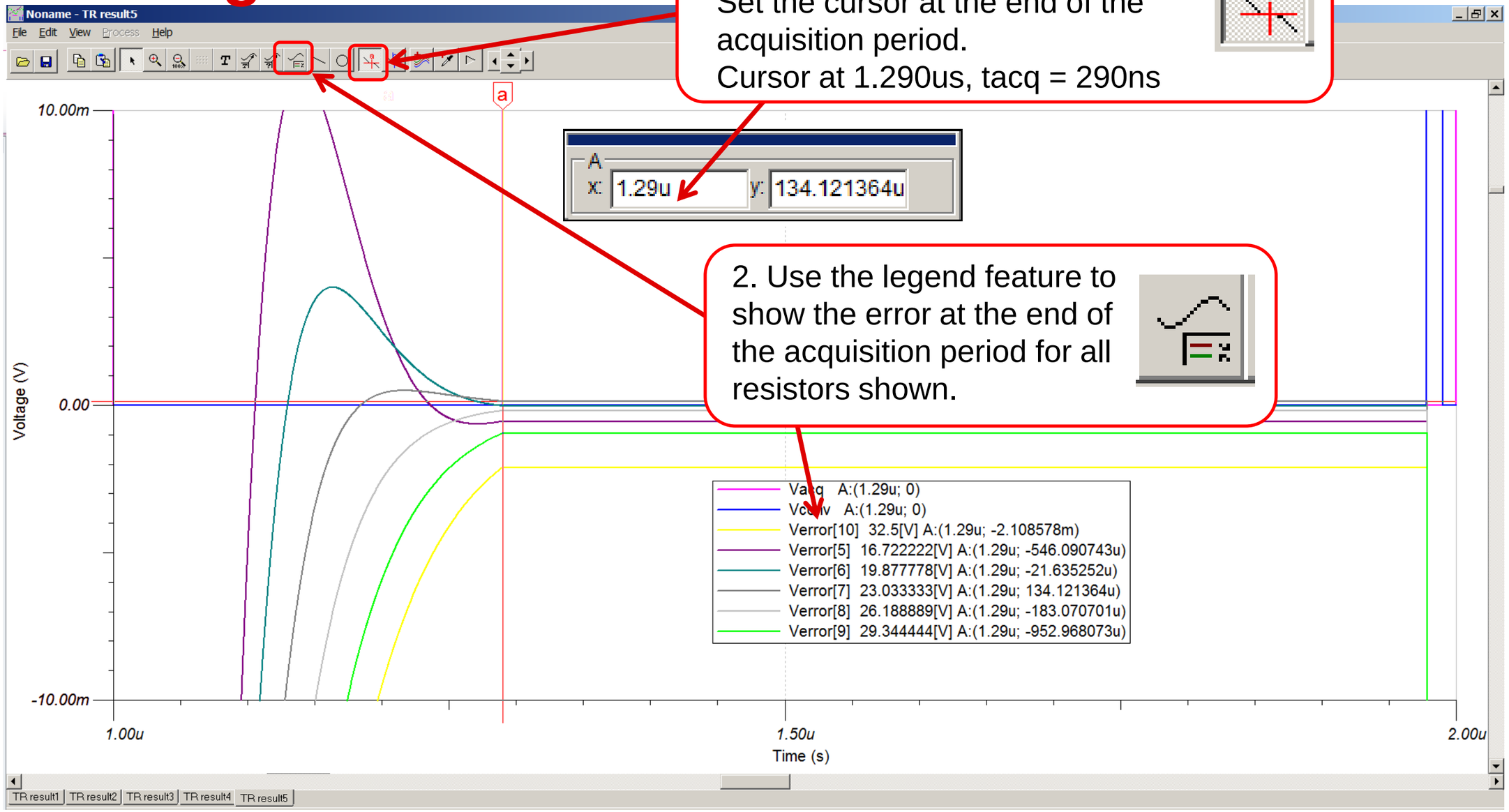


Large overshoot curves deleted



Add a legend

1. Click here to set the cursor. Set the cursor at the end of the acquisition period. Cursor at 1.290us, tacq = 290ns

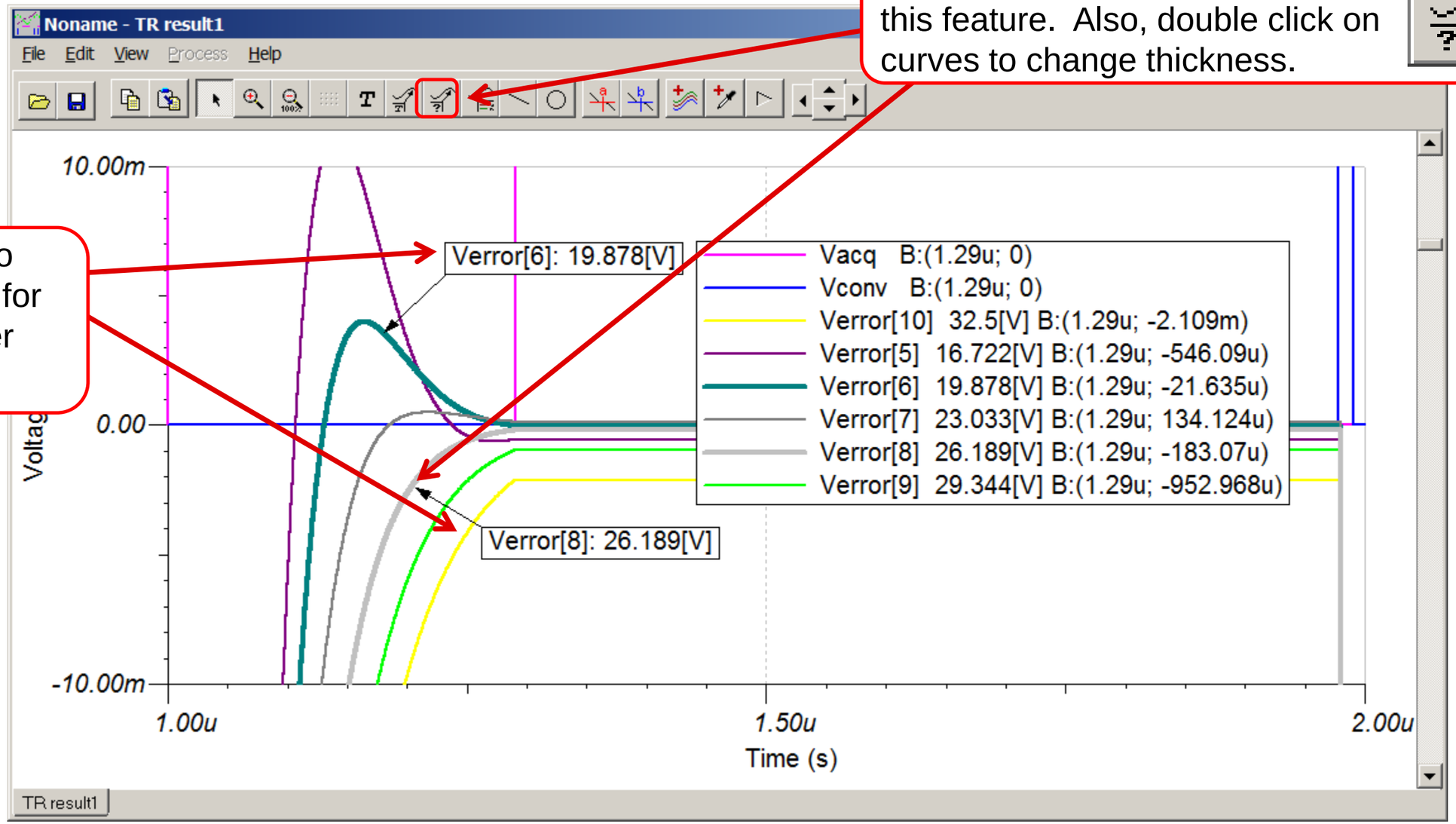


2. Use the legend feature to show the error at the end of the acquisition period for all resistors shown.

Select the best three curves

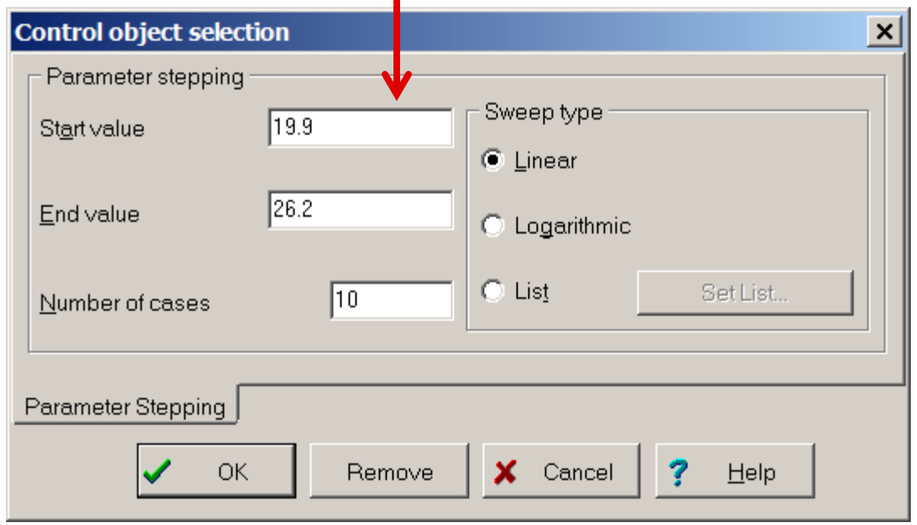
Add labels to the key curves using this feature. Also, double click on curves to change thickness.

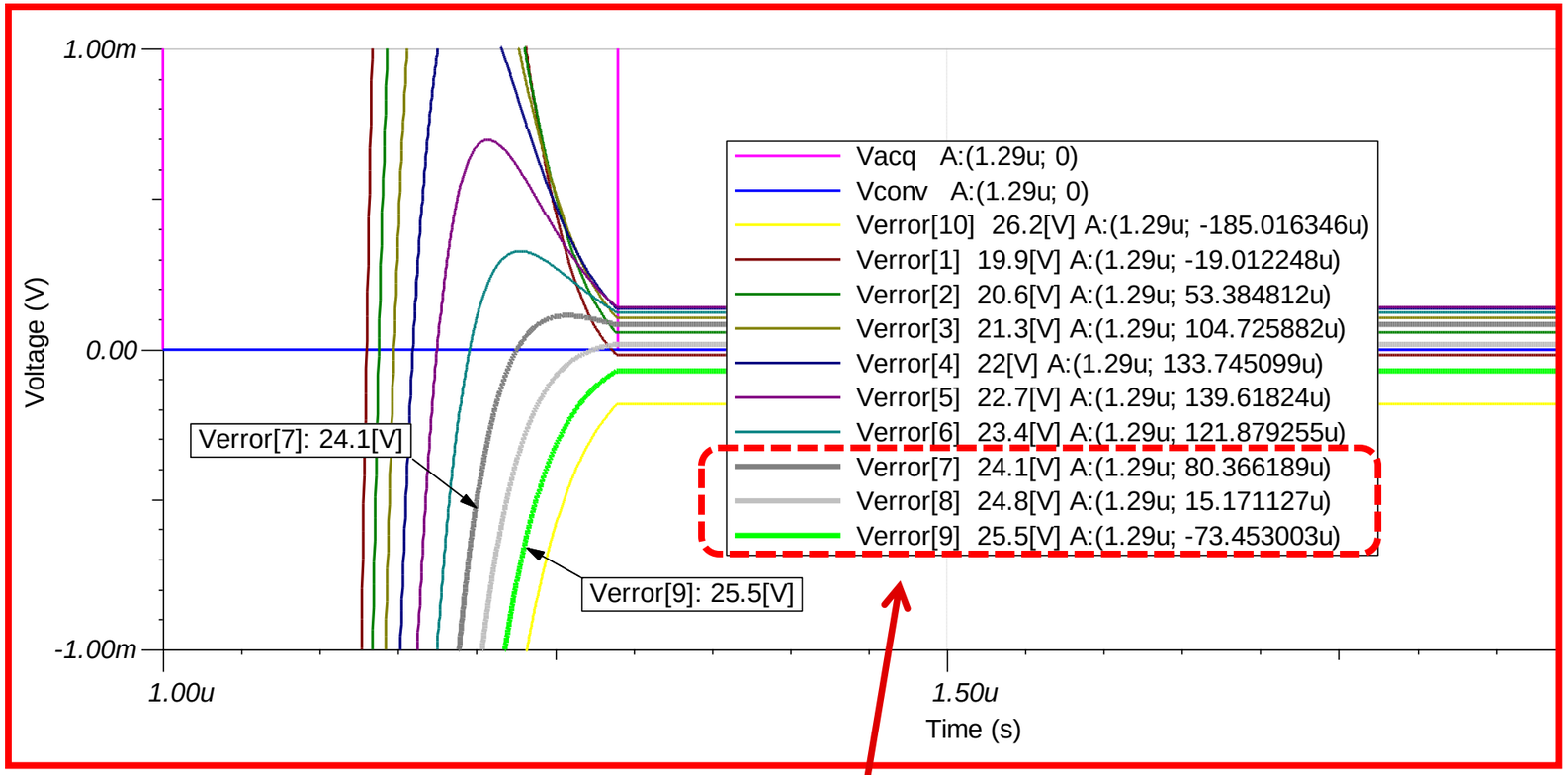
We will use **19.9** to **26.2** as the range for the next parameter step simulation



Second Run: further refinement in Rflt value

1. Enter a new range for the Rfilt range based on last simulation (i.e. **19.9** and **26.2**)



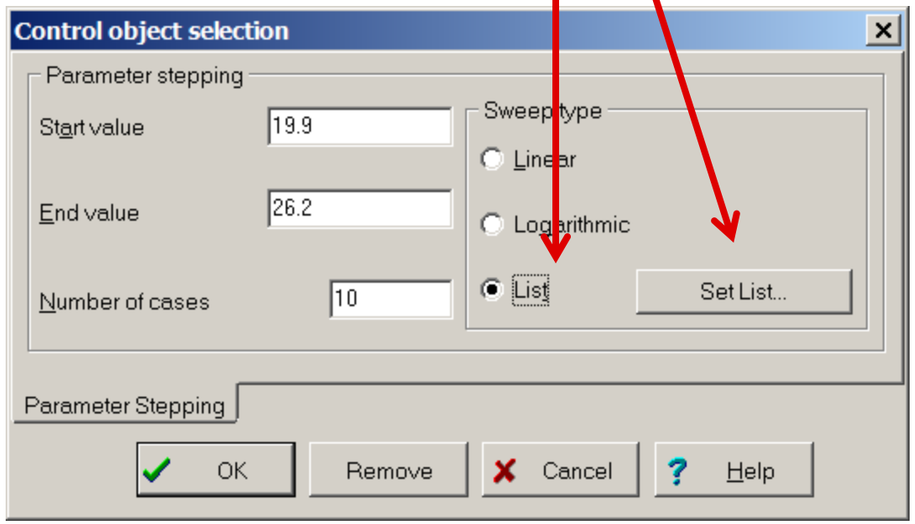


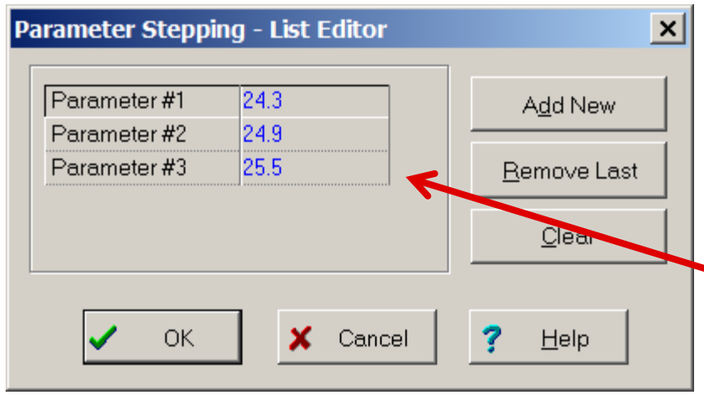
2. Find the three best curves to set the range for the next simulation. Typically the three curves will be overdamped, underdamped and critically dampened. Notice the polarity of the error switches. We will use **24.1** to **25.5** for next simulation.

ADS8860_Input_OPA320 - 2nd.TSC

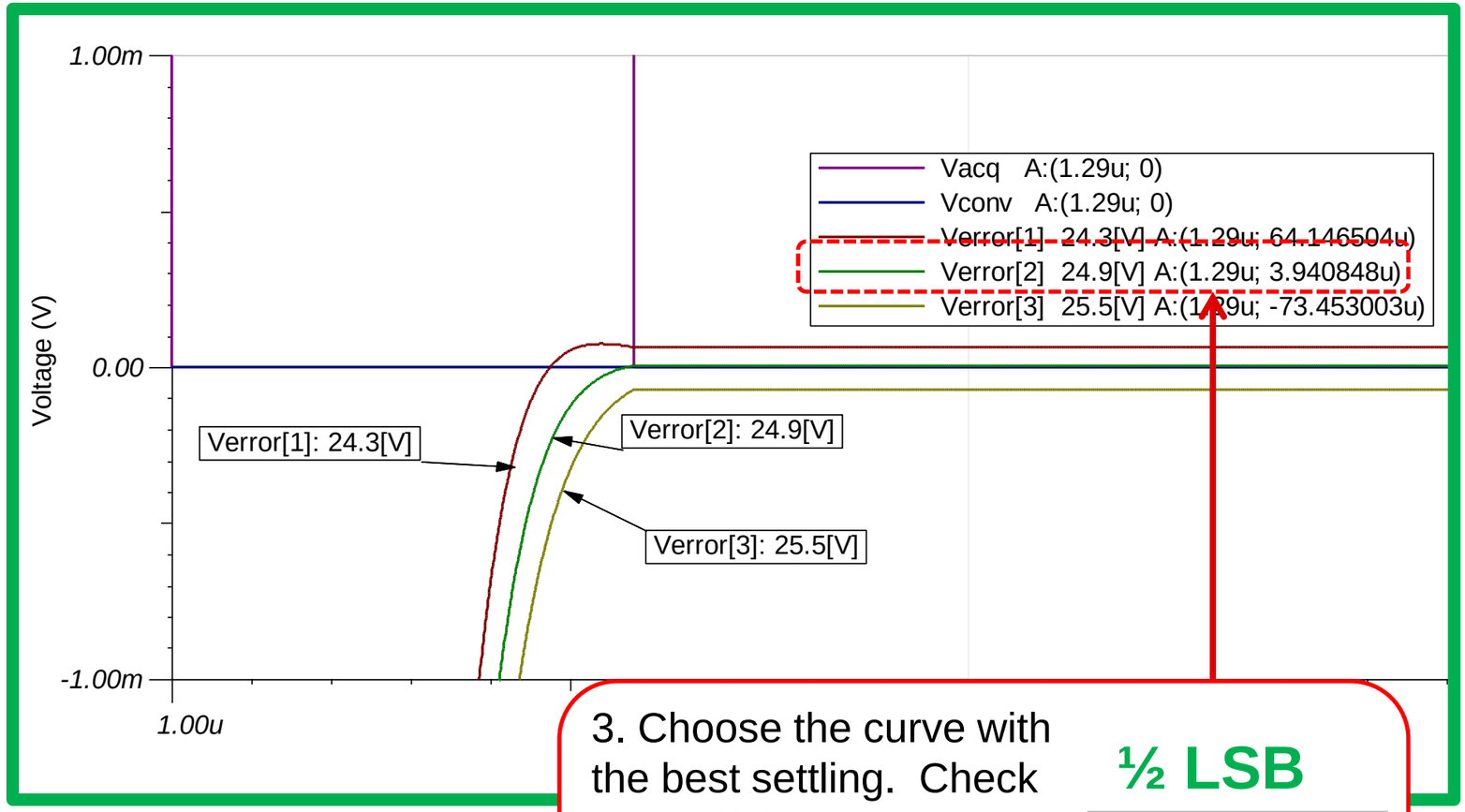
Final Run: Use Standard Values

1. Use the “List” sweep type



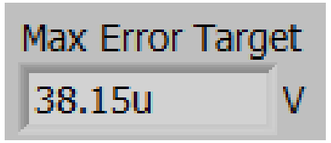


2. Enter standard resistor values using the results of the previous sweep (i.e. **24.1** to **25.5**)

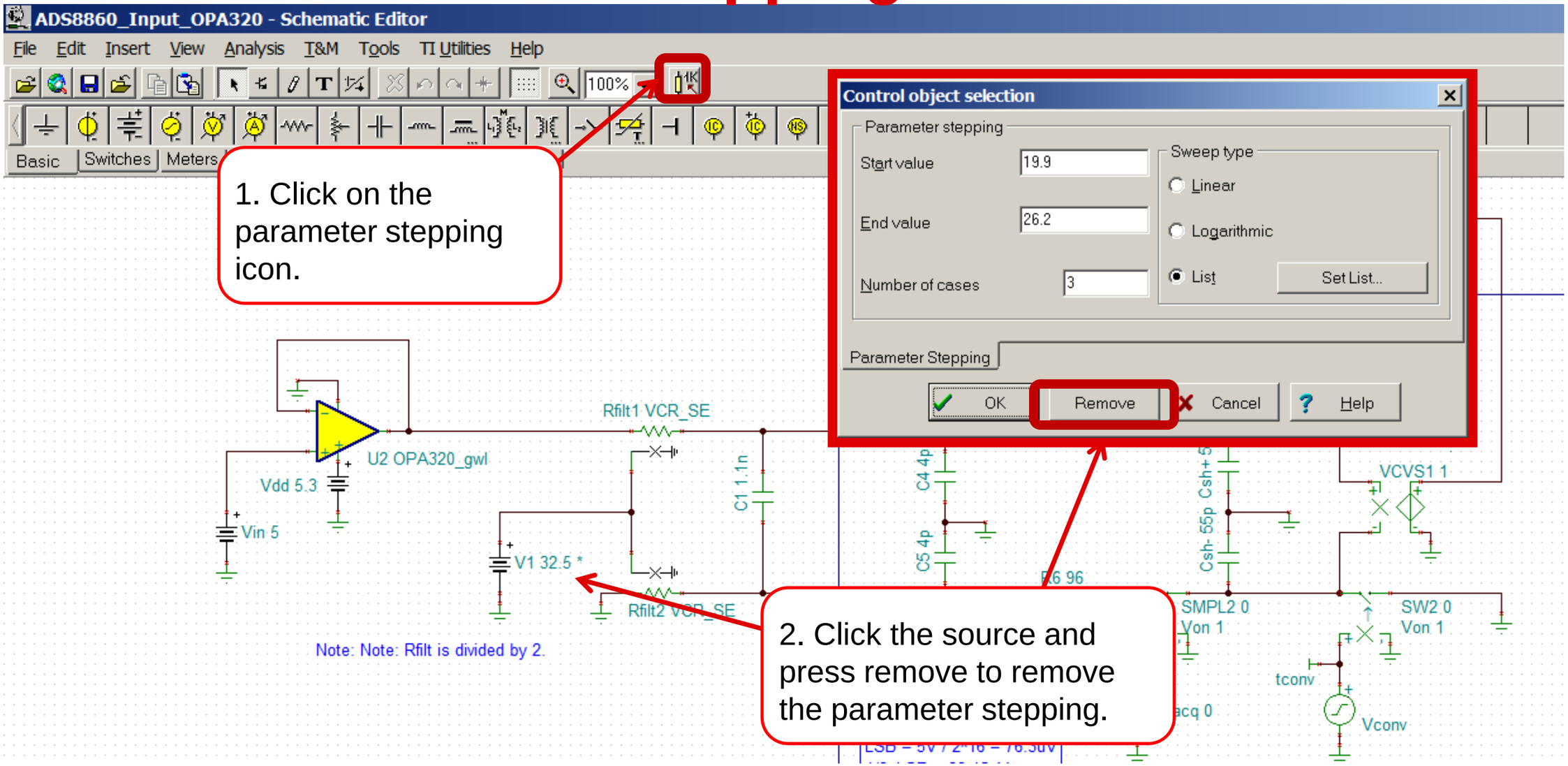


3. Choose the curve with the best settling. Check to see if the error target from the calculator is met.
Yes! 3.9uV << 38.15uV
For R_{filt} = 24.9 Ω

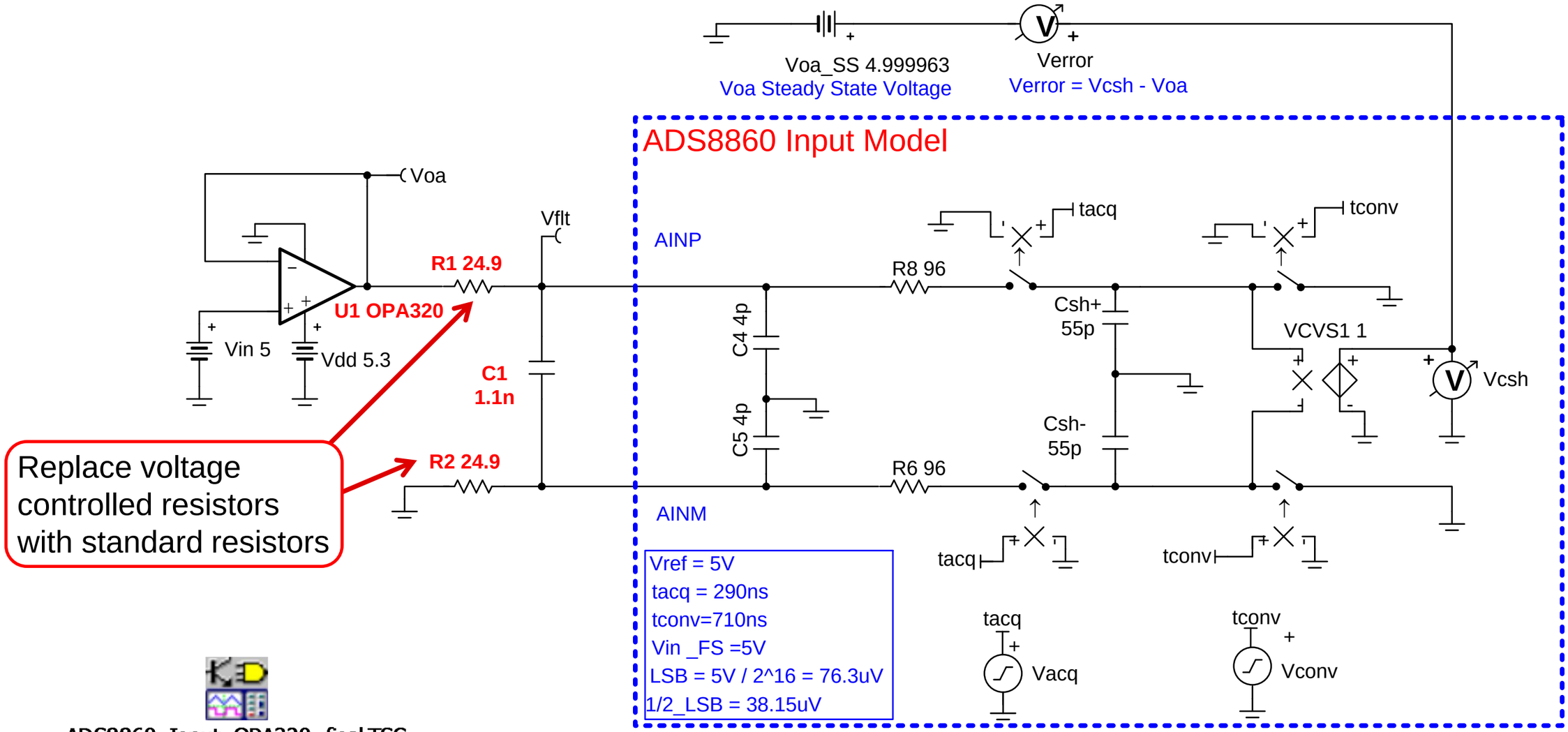
½ LSB



Turn off Parameter Stepping



Final Circuit

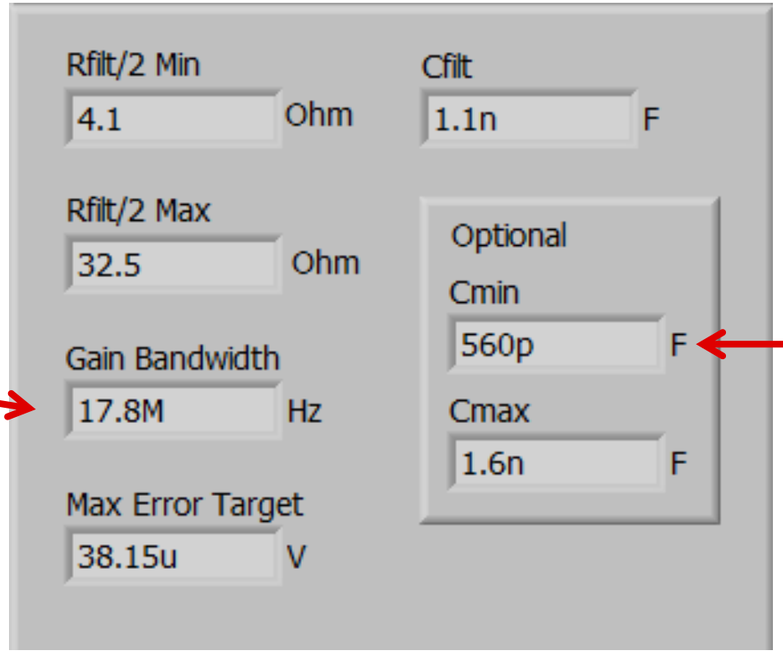


Replace voltage controlled resistors with standard resistors

ADS8860_Input_OPA320 -final.TSC

What if we didn't meet the error target?

2. If no RC combination works, try an amplifier with wider bandwidth.



1. Try reiterating on Rfilt using Cmin. If Cmin doesn't work try Cmax.

Note 1: Typically step 1 and 2 will not be required.
Note 2: Output impedance can also impact settling. Ideally open loop output impedance is low (R < 100Ω) and flat.

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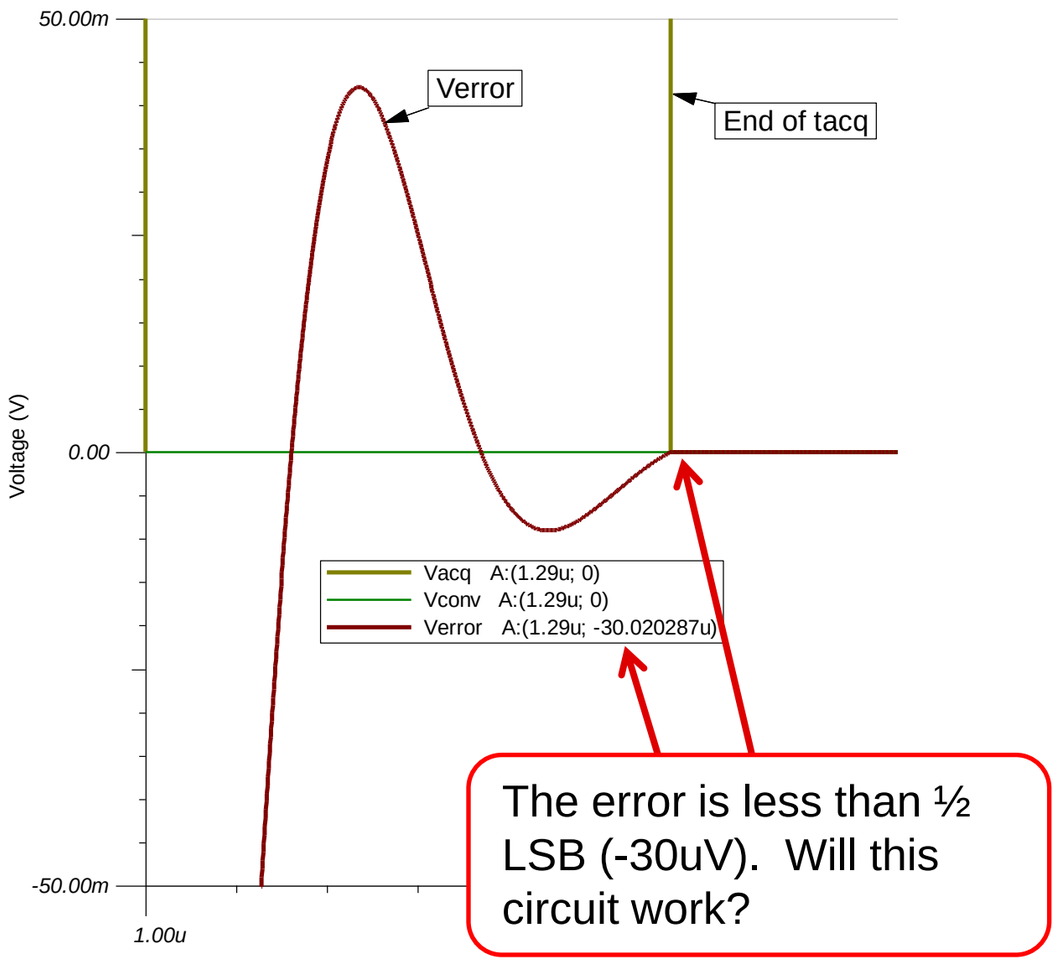
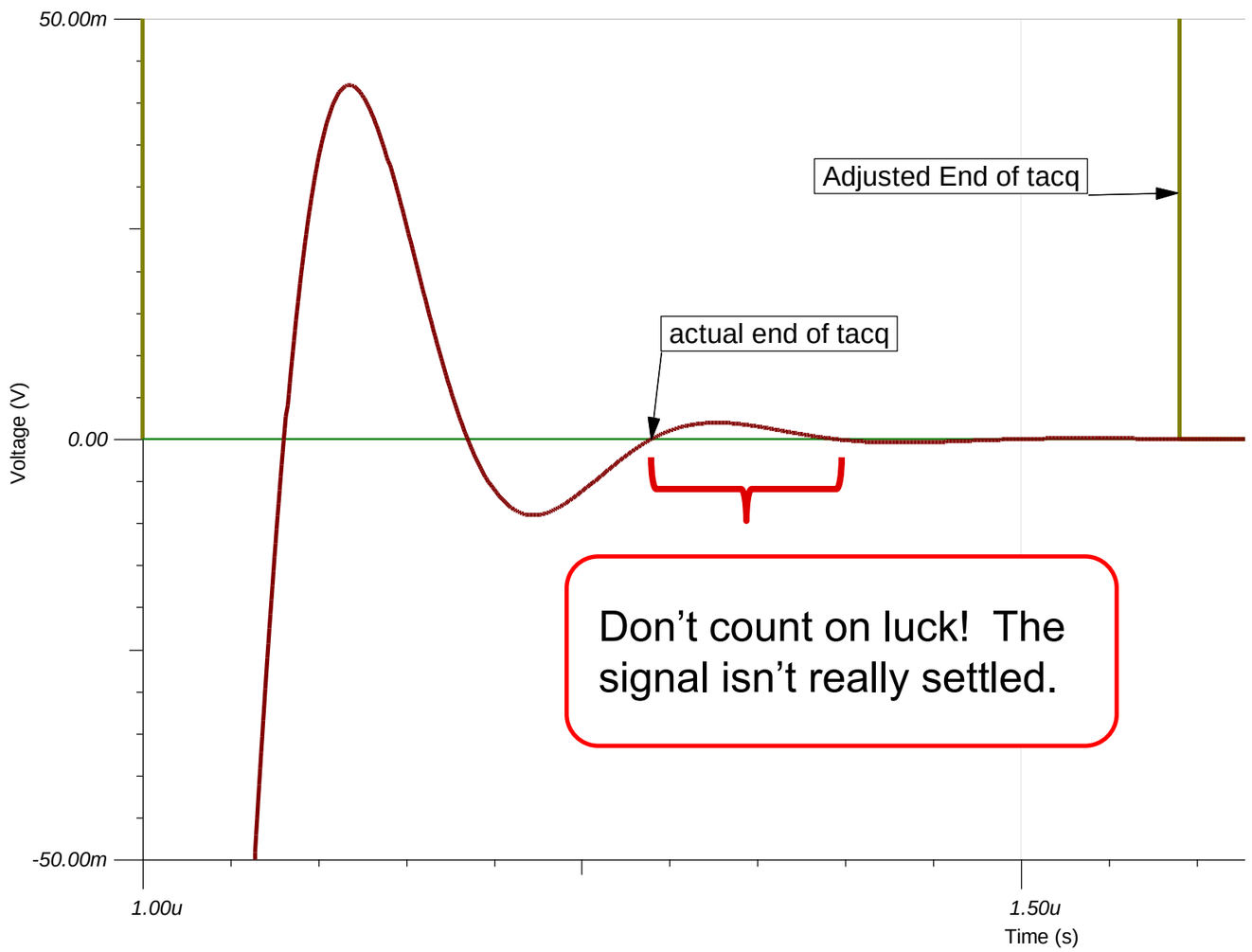
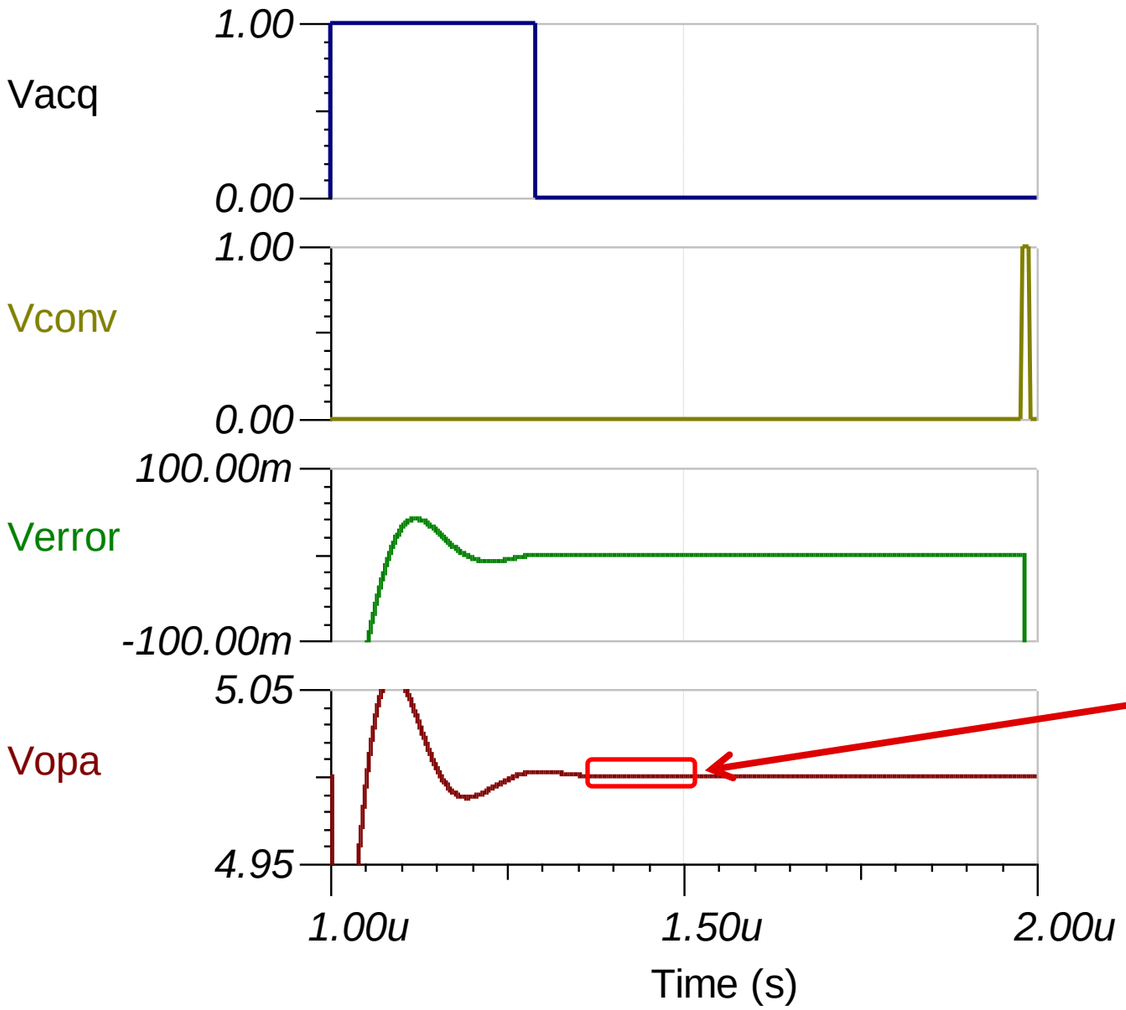
Expand the acquisition time to check settling





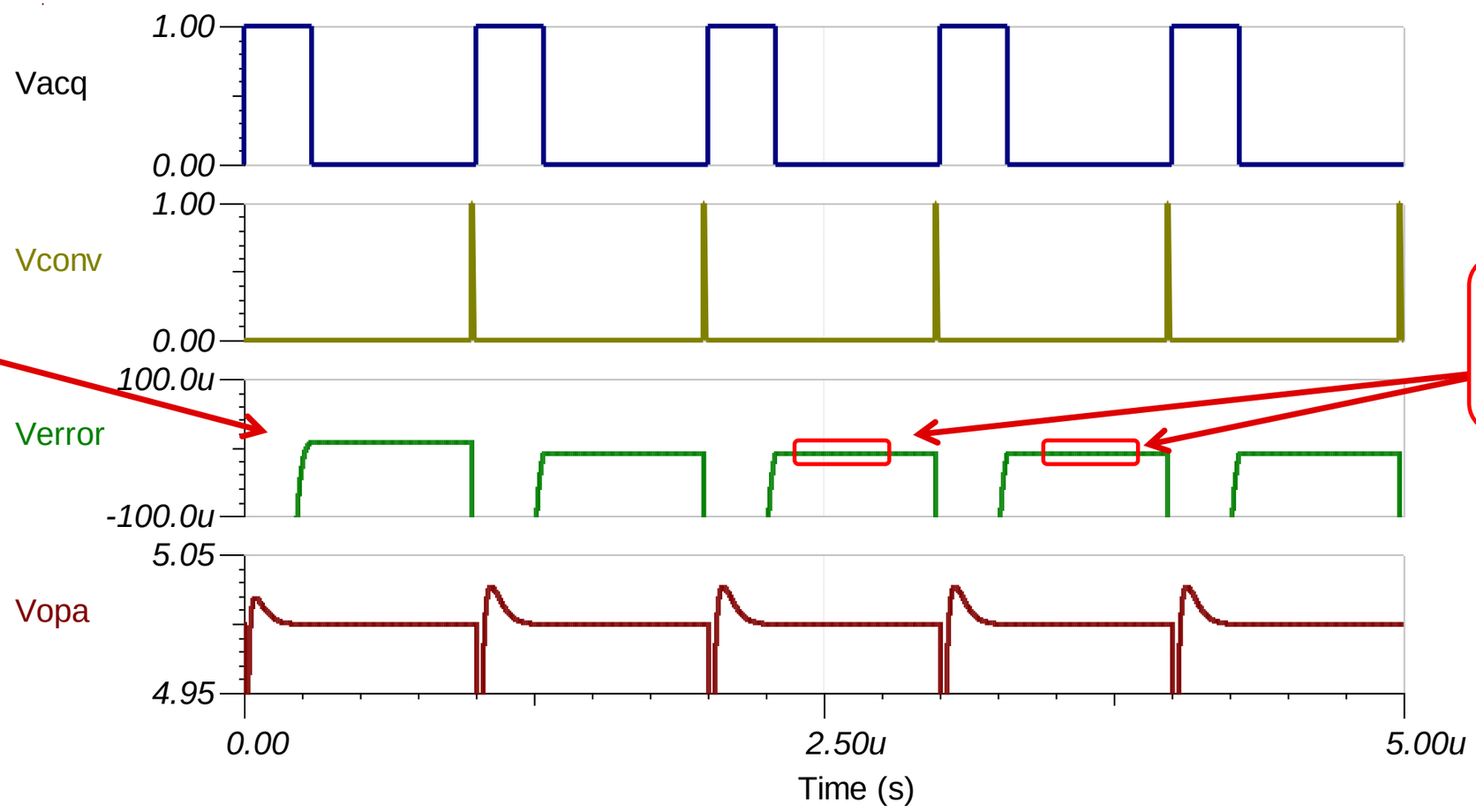
t_{acq} change in simulation only to test for marginal design. Not adjusted in real circuit.

Look at Op Amp Settling



Amplifier settled to ½ LSB or better after tacq ends.

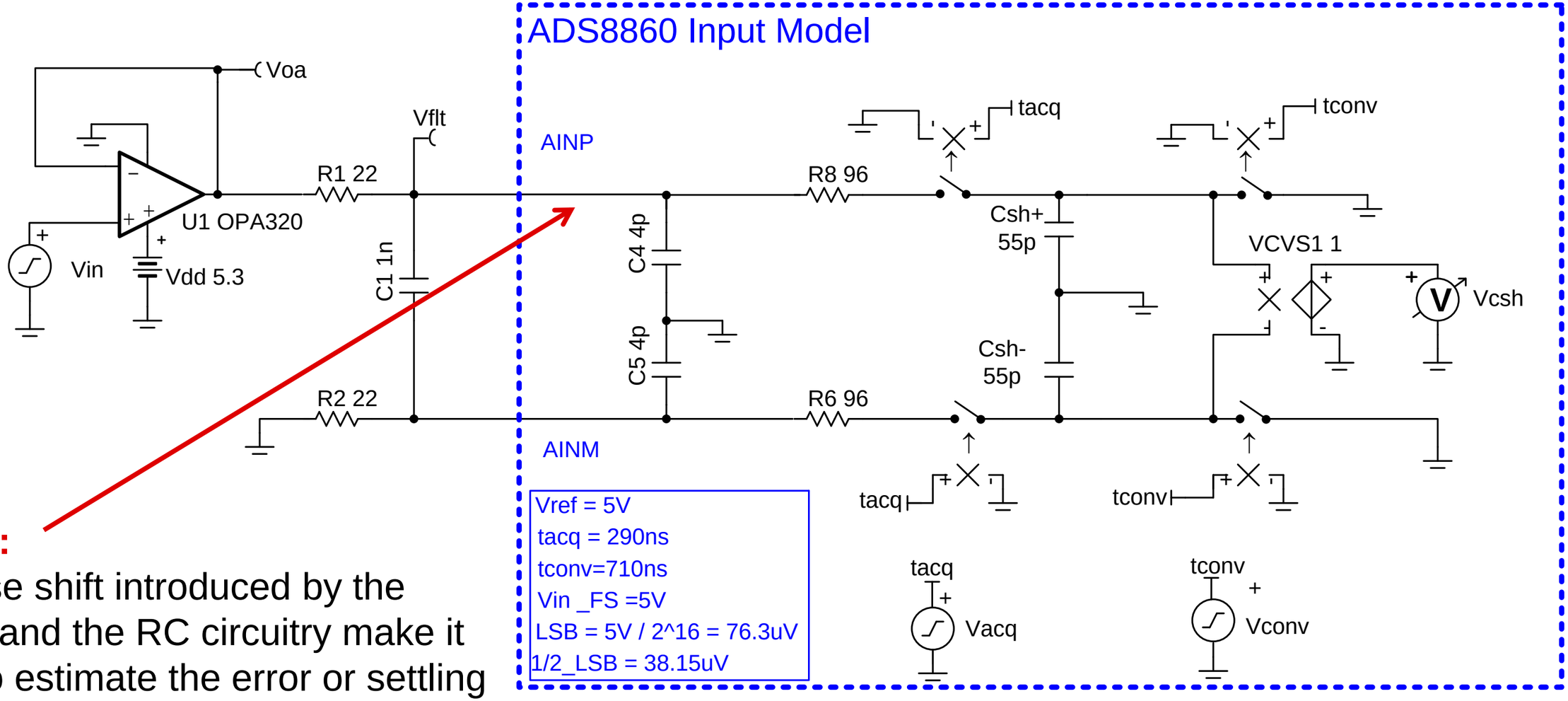
Check settling for multiple cycles



Always discard the first cycle.

Make sure that settling is consistent from cycle to cycle.

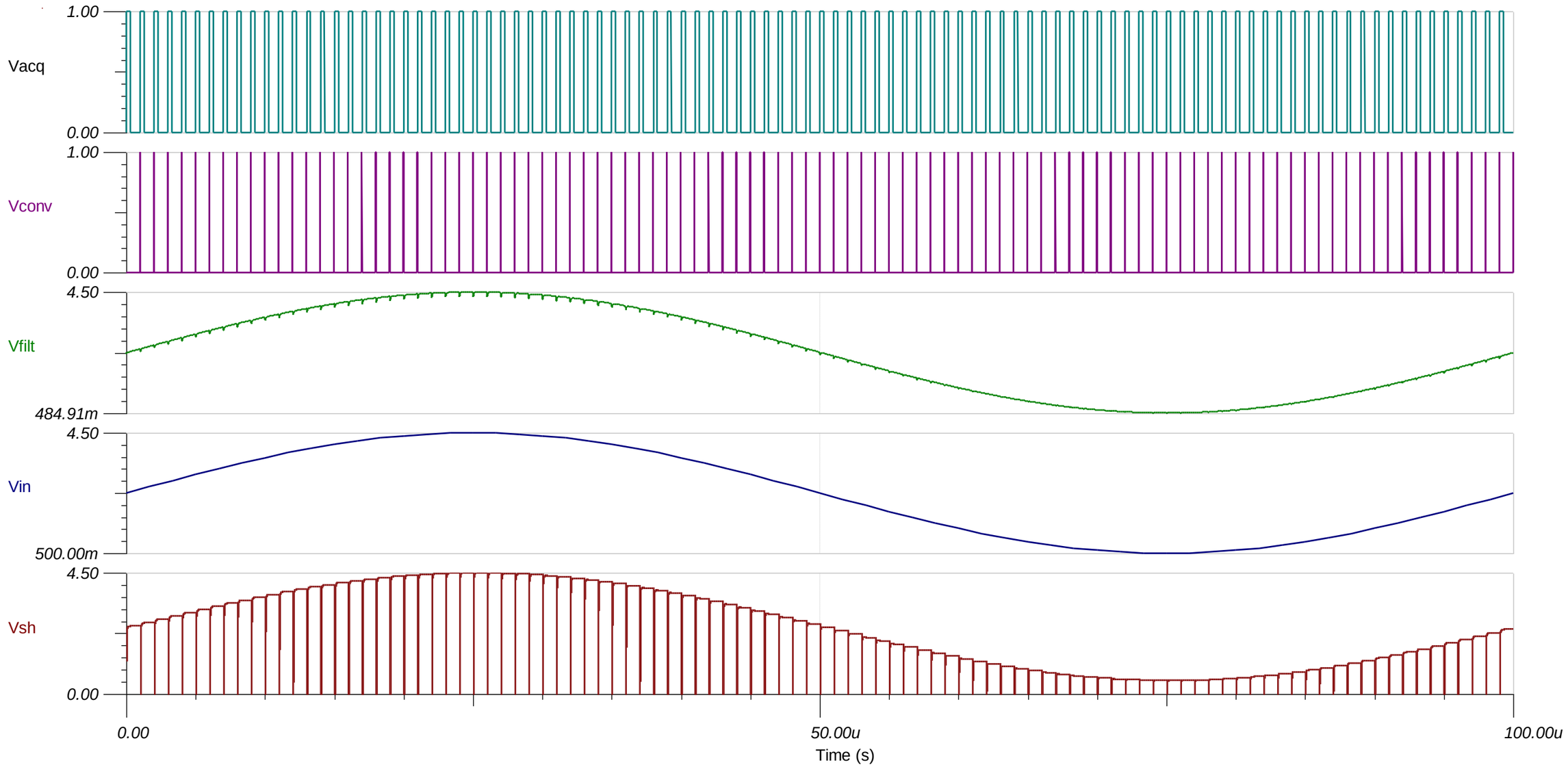
AC Input Signal Simulation Example



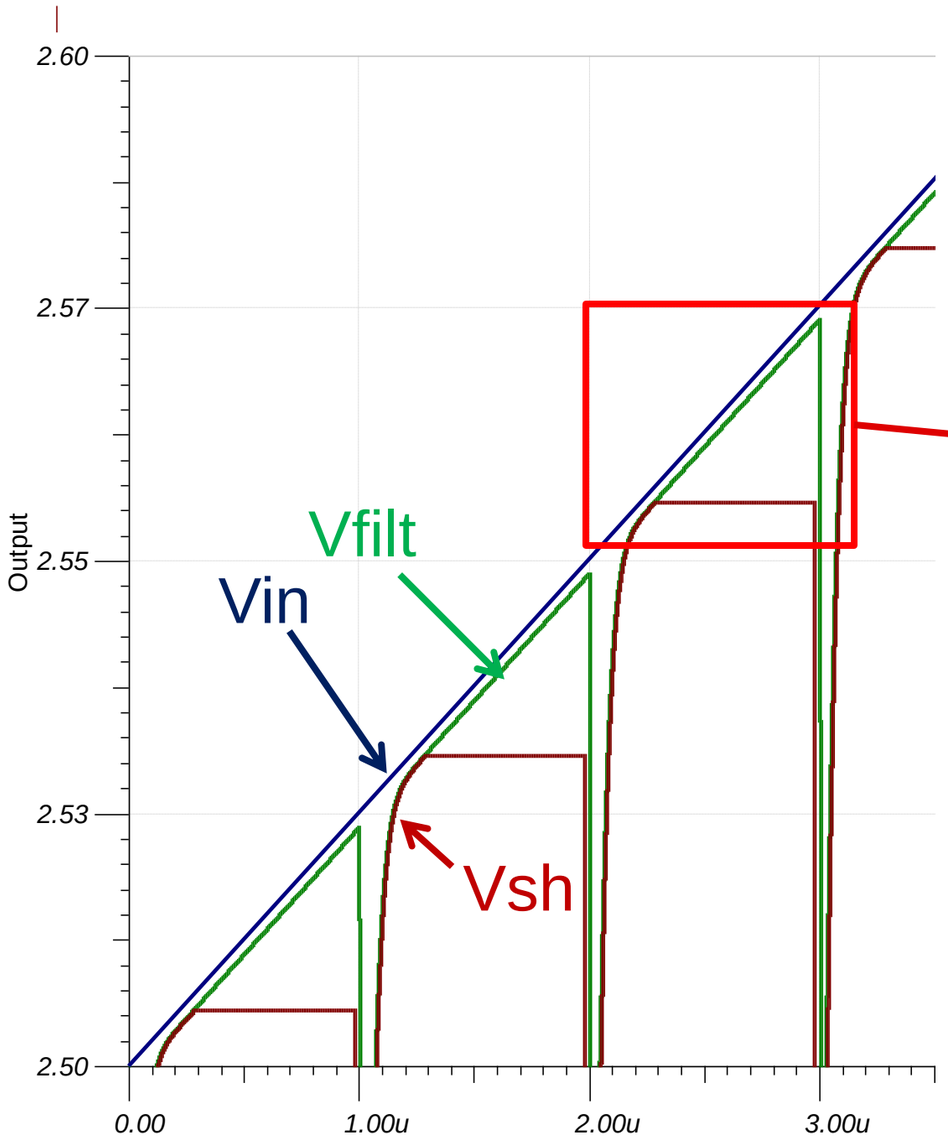
PROBLEM:

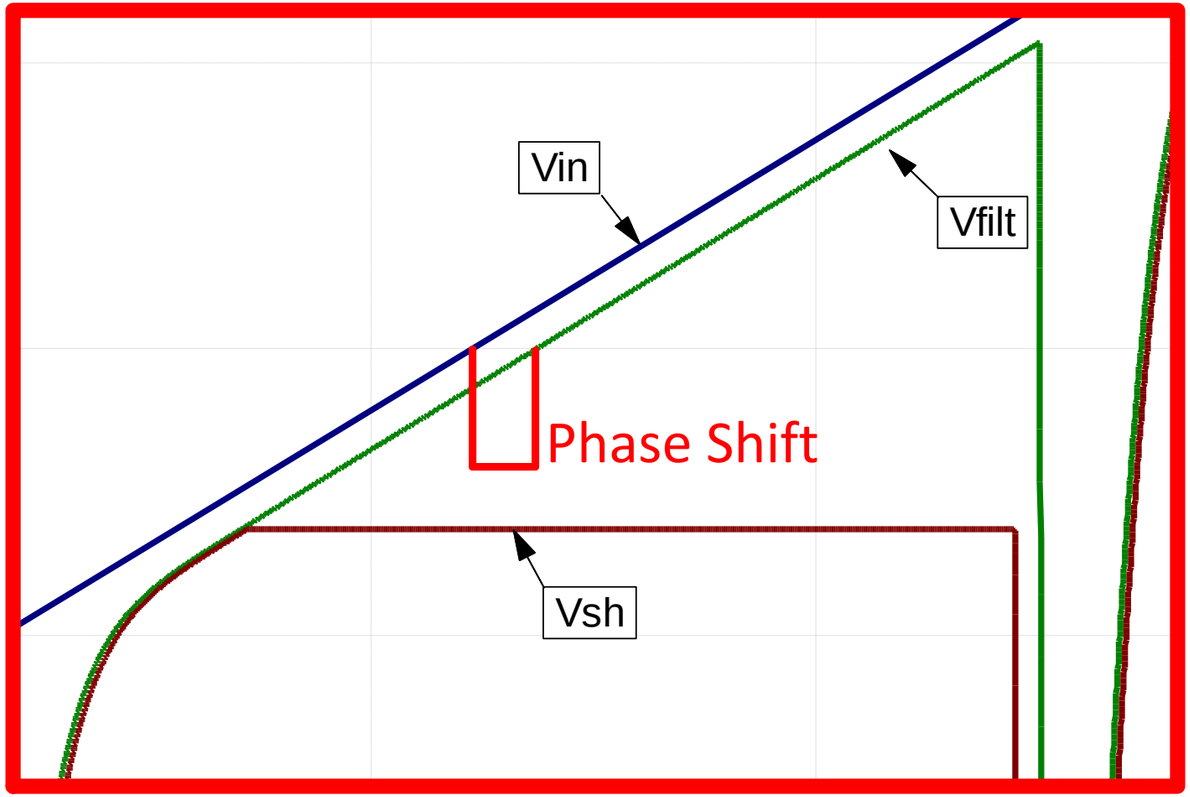
- The phase shift introduced by the amplifier and the RC circuitry make it difficult to estimate the error or settling signal

Results for an AC Simulation: What about error



AC Input Signal Simulation Example

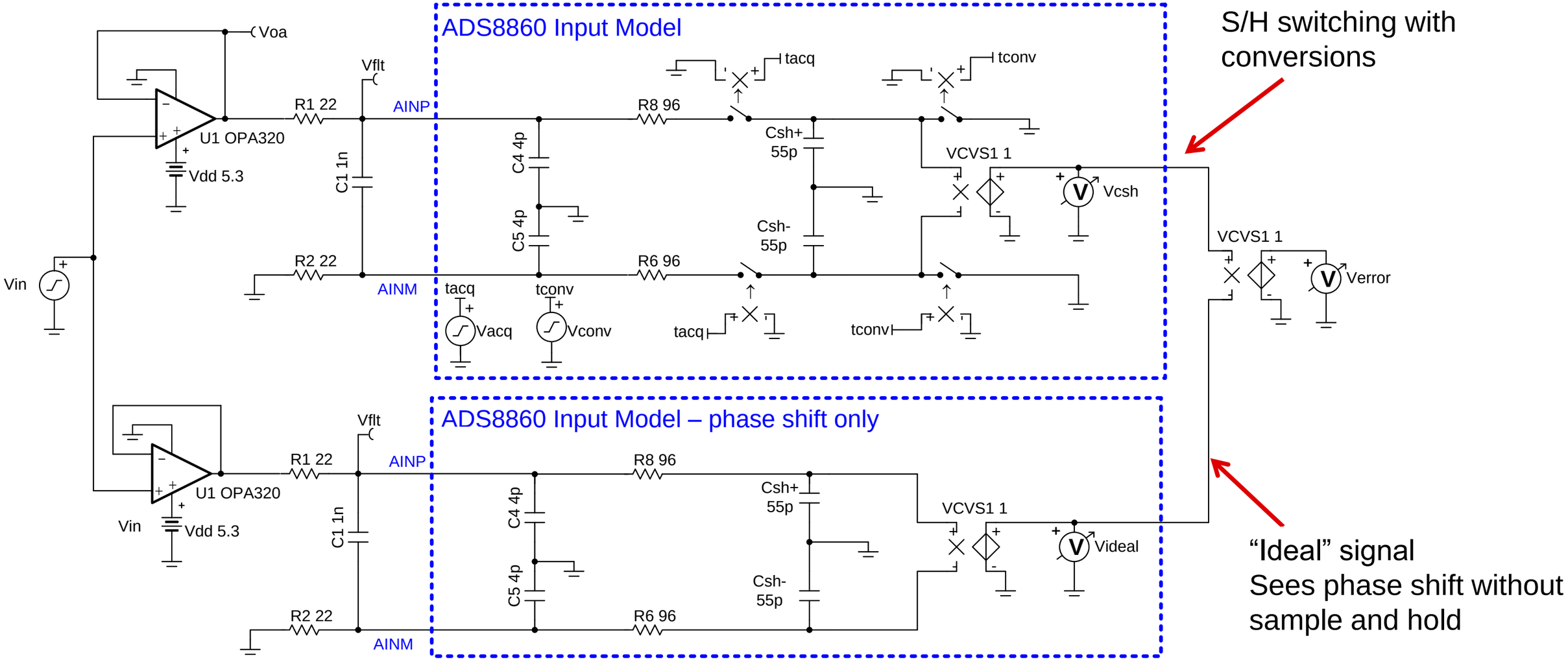




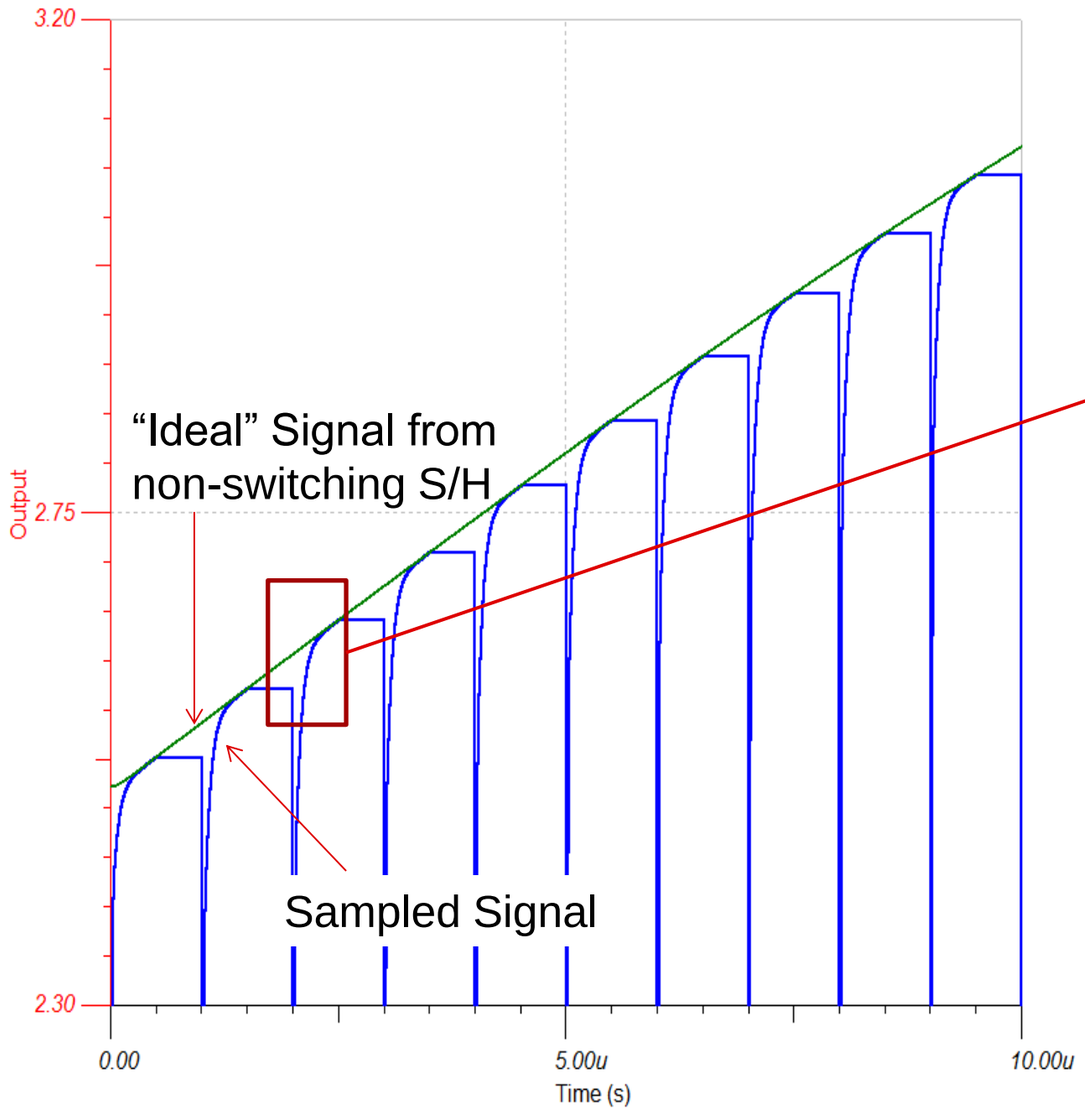
PROBLEM:

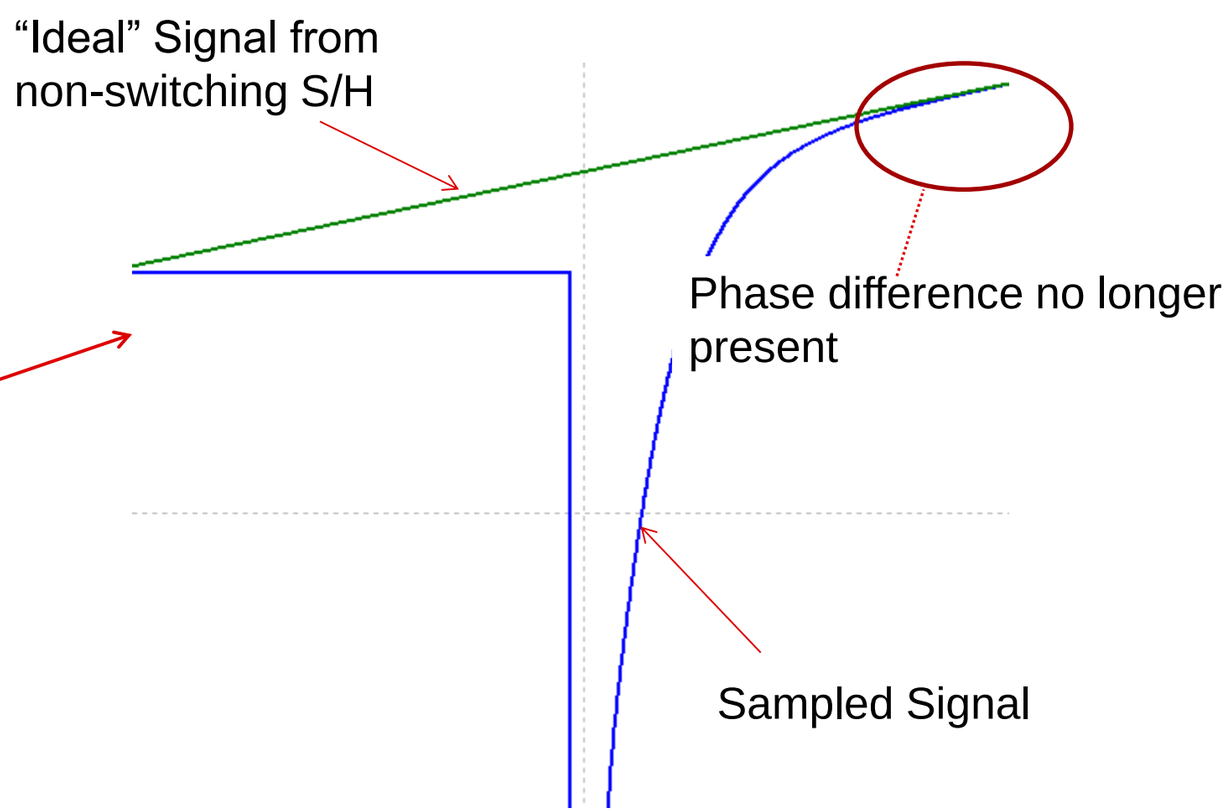
- The phase shift introduced by the amplifier and the RC circuits make it difficult to estimate the settling error in the sample and hold

AC Input Simulation Example



AC Input Signal Simulation Example





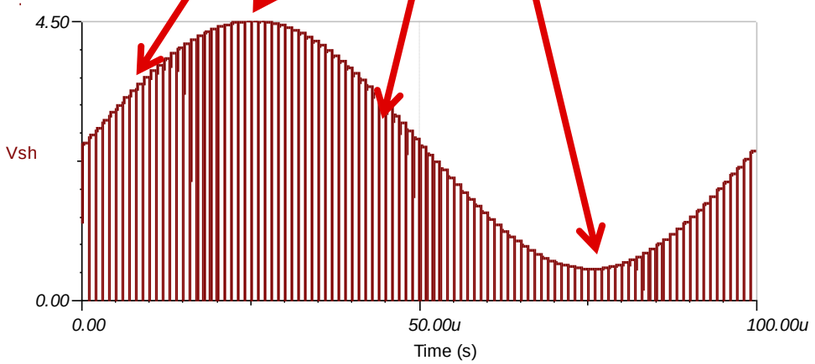
Solution:

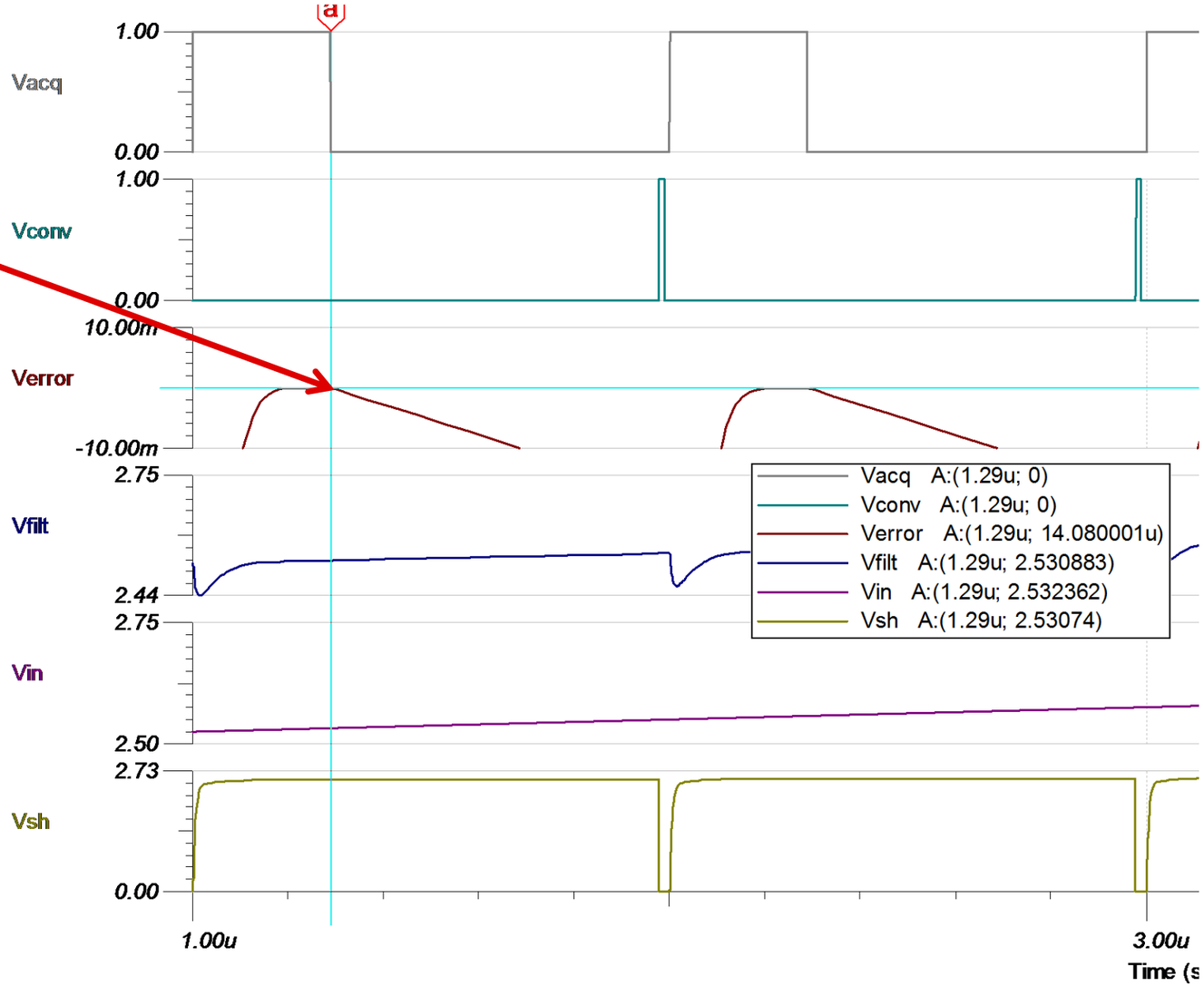
- The "Ideal" Signal generated from non-switching S/H has same phase as the Sampled Signal; allowing the calculation of settling errors

Check the error for AC simulations

Place the cursor at the end of an acquisition cycle. Generate a legend. The error should be less than ½ LSB.

Check the error at multiple locations





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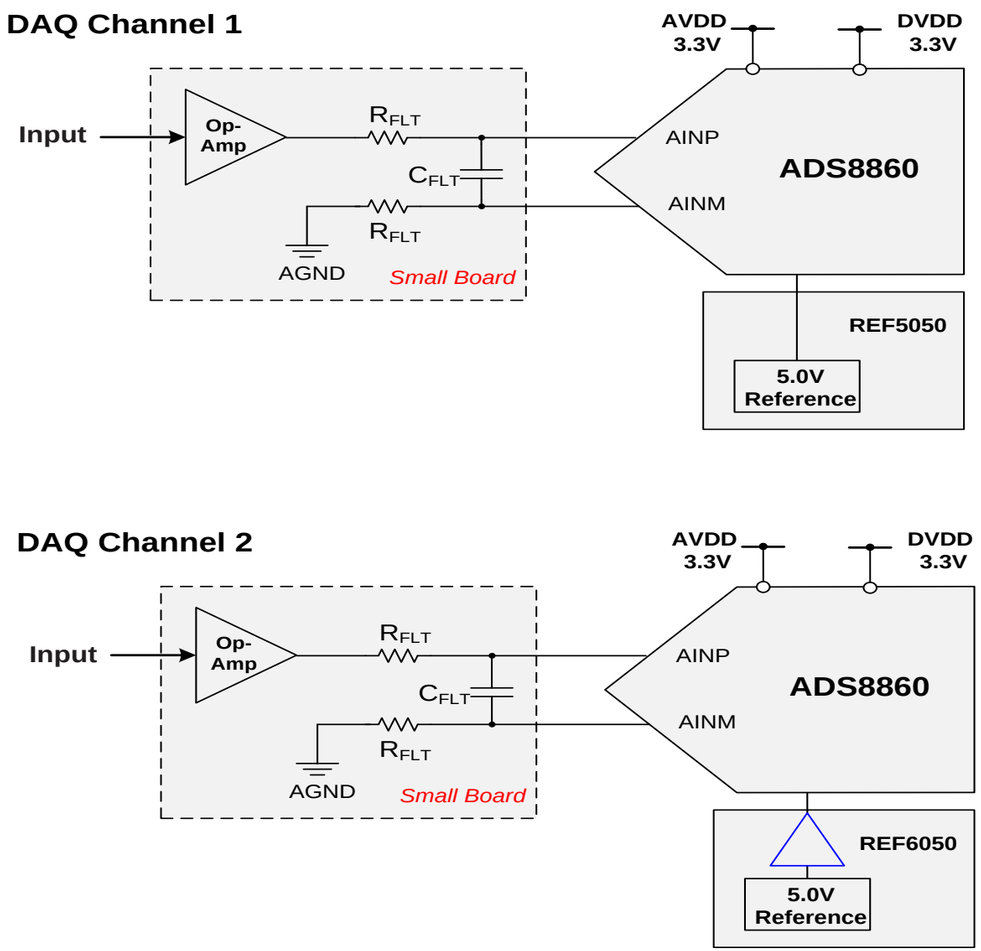
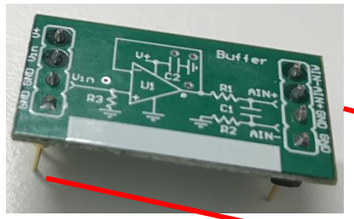
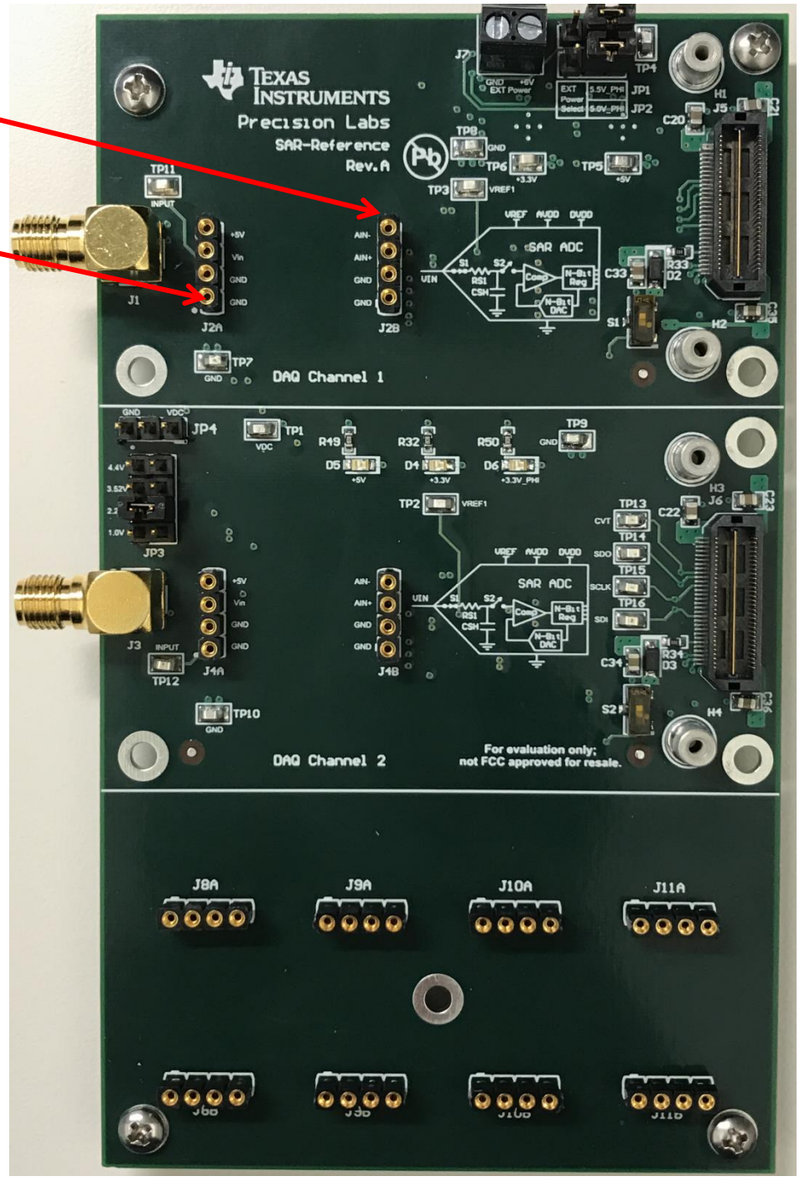
Hardware Kit







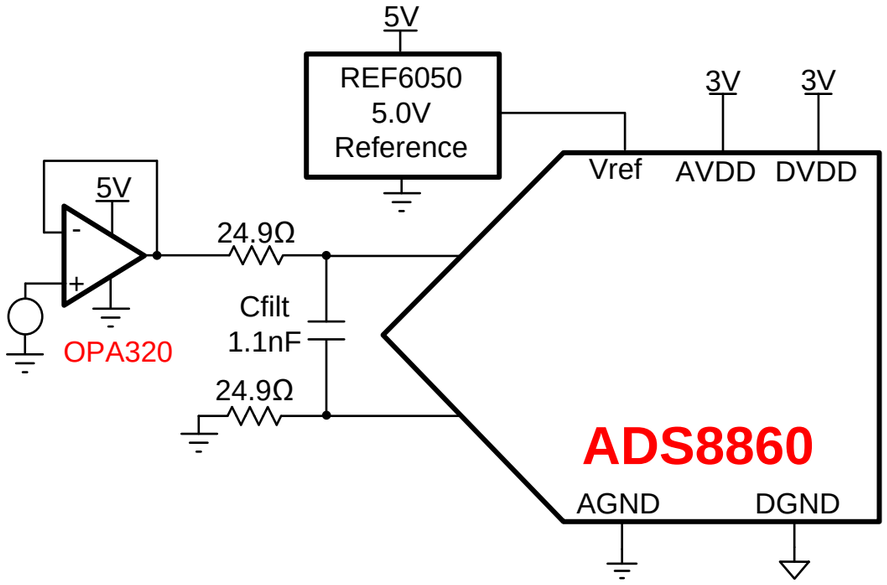
ADS8860: 16-Bit, 1-MSPS, SAR Analog-to-Digital Converter.

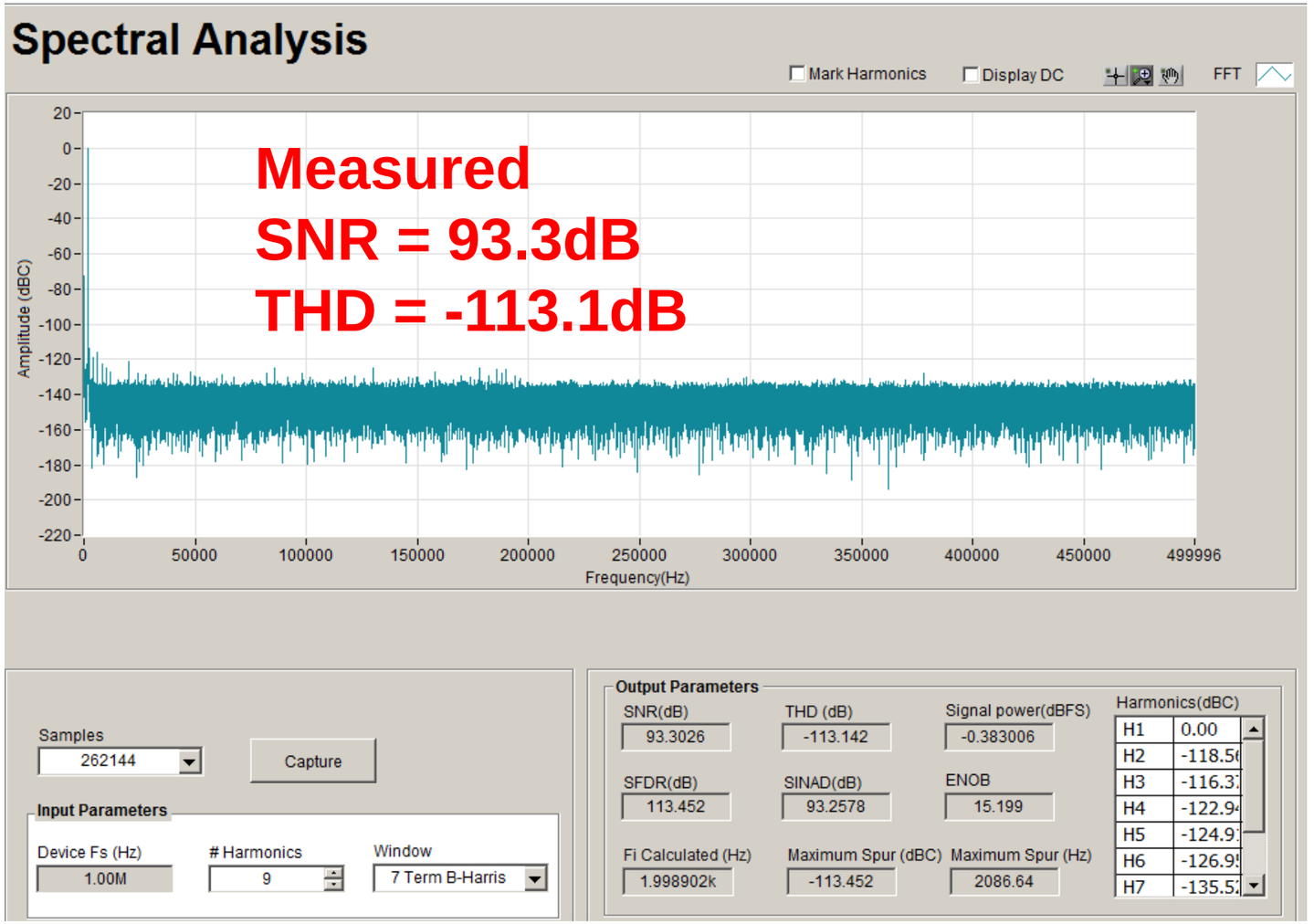
Measured AC Performance for Optimized Circuit

ADS8860 Data Sheet (1Msps)

Parameter	Min	Typ	Max	Unit
SNR	92	93		dB
THD (1kHz)		-108		dB

Circuit from TINA



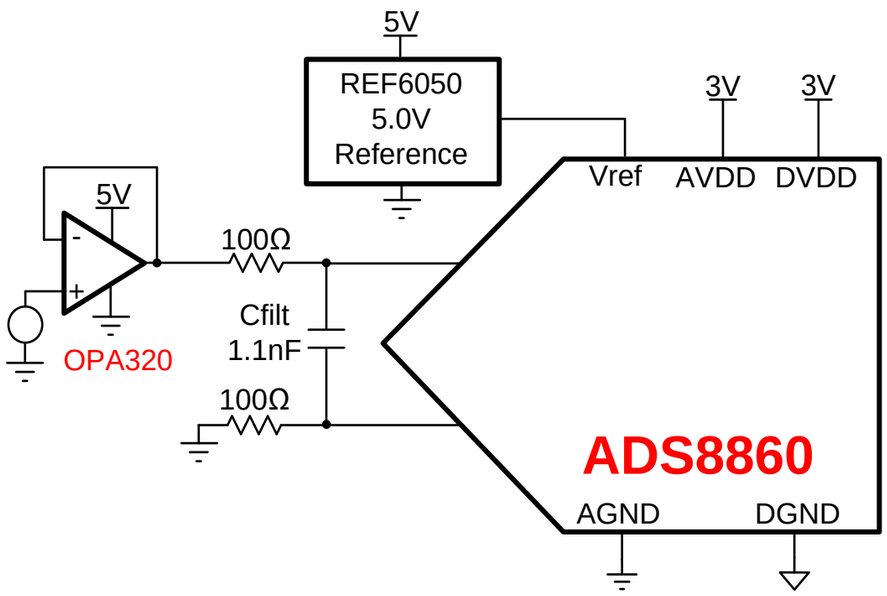


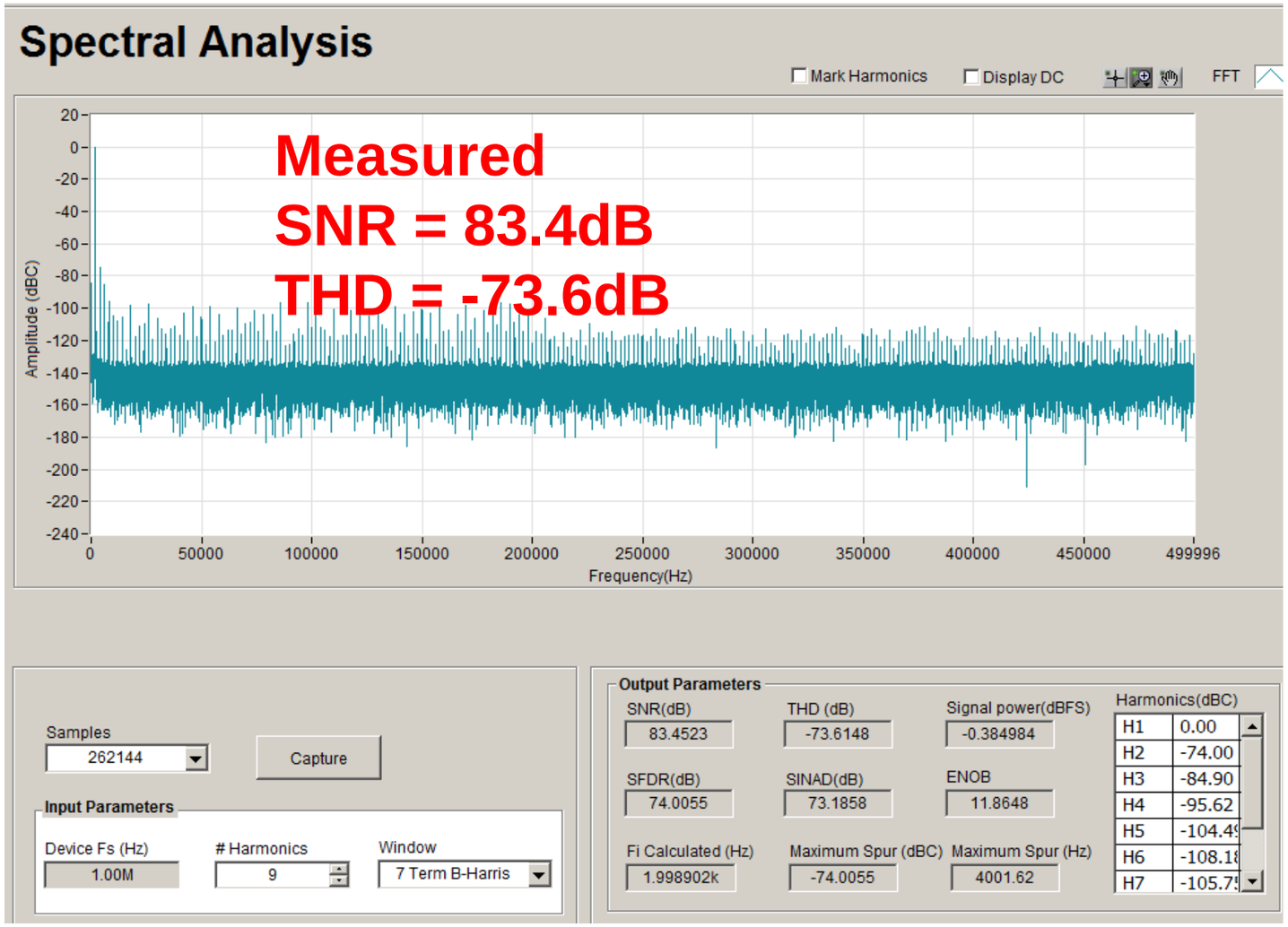
Measured AC Performance: Wrong RC

ADS8860 Data Sheet (1Msps)

Parameter	Min	Typ	Max	Unit
SNR	92	93		dB
THD (1kHz)		-108		dB

Wrong R_{filt}



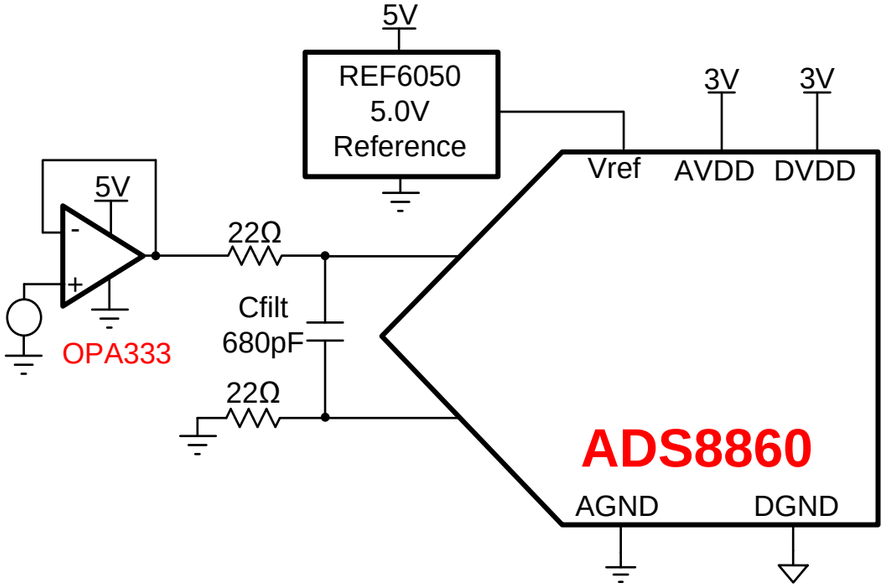


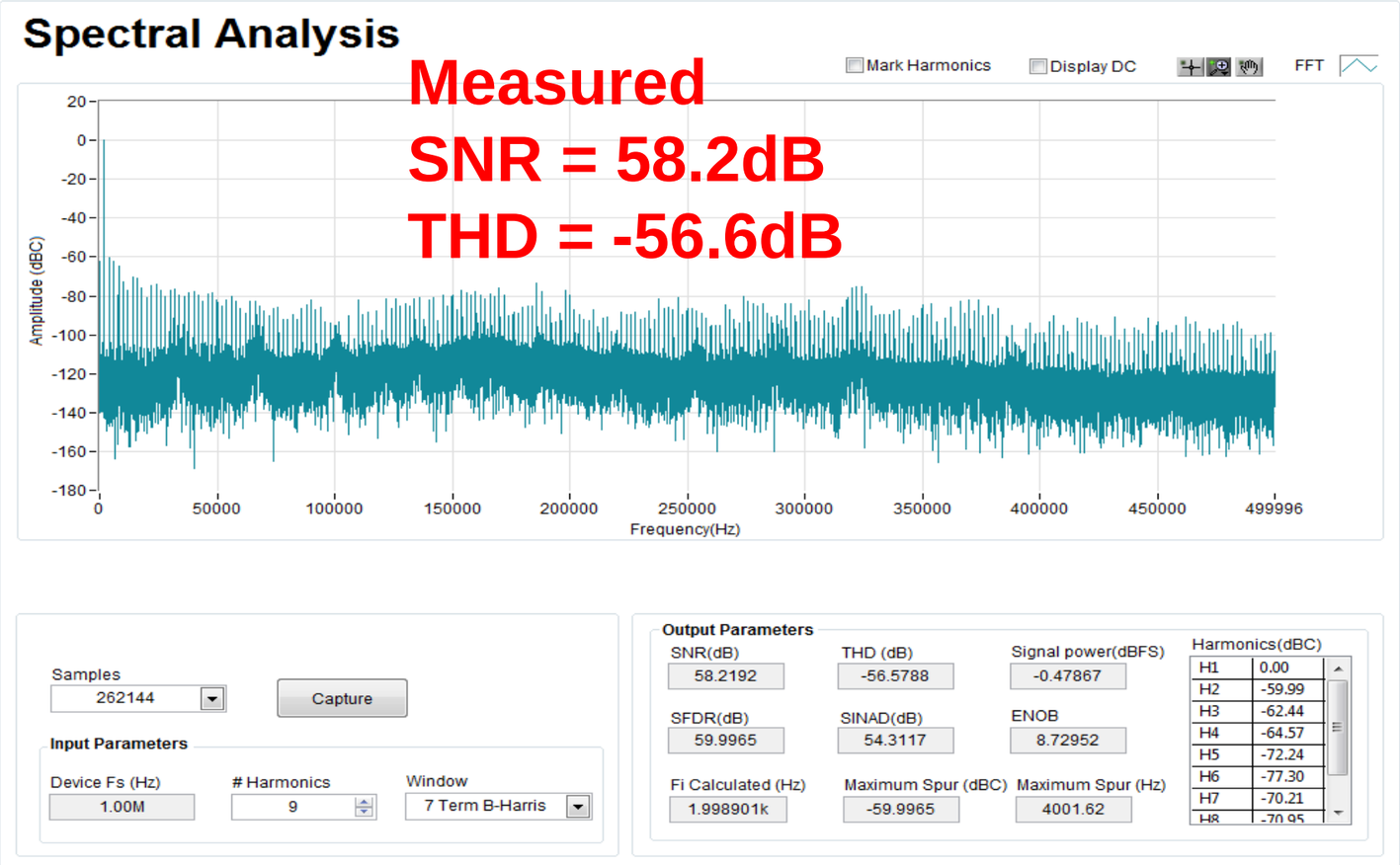
Measured AC Performance: Wrong Amplifier

ADS8860 Data Sheet (1Msps)

Parameter	Min	Typ	Max	Unit
SNR	92	93		dB
THD (1kHz)		-108		dB

Op Amp BW Not Sufficient





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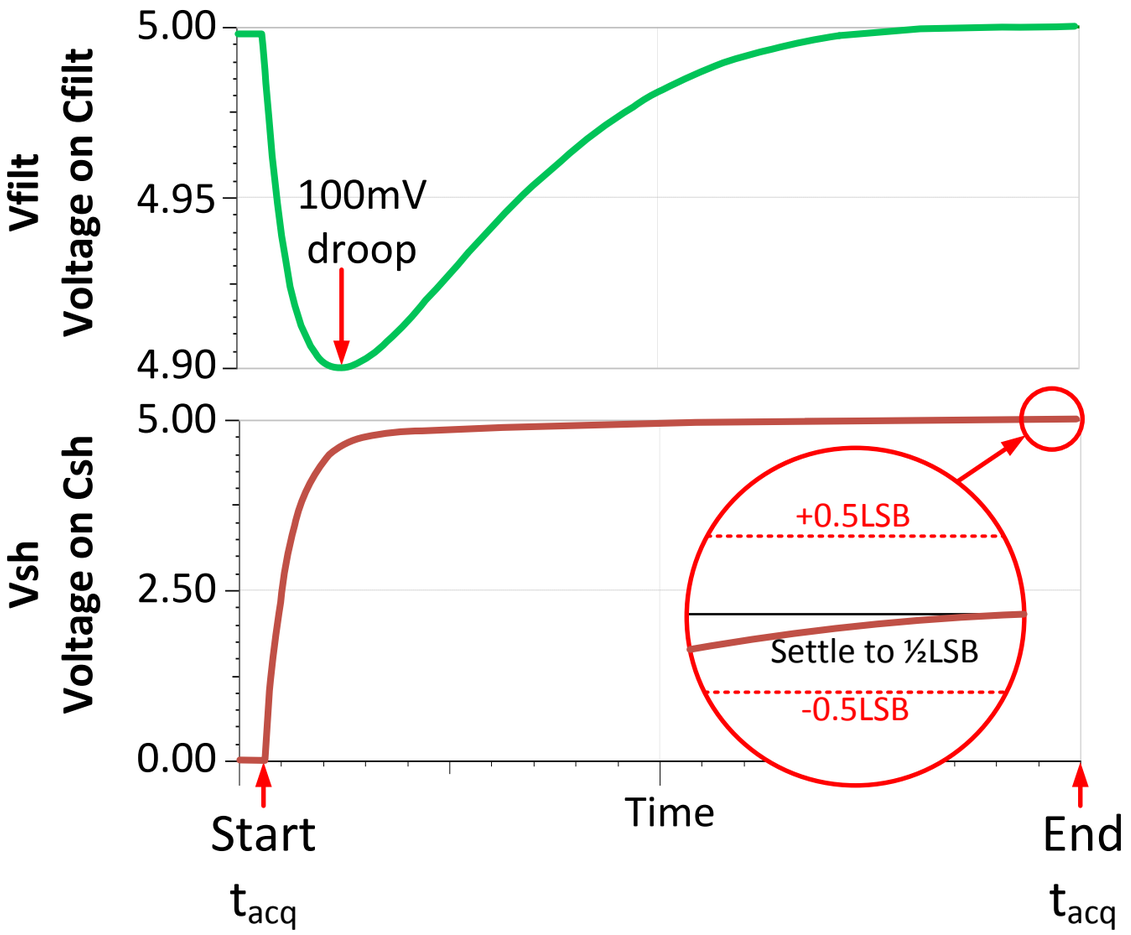
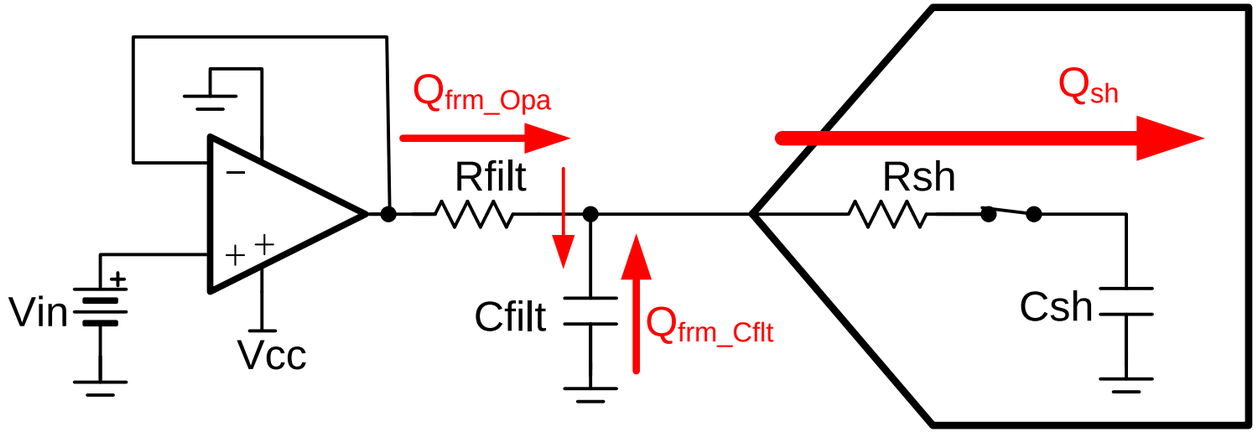
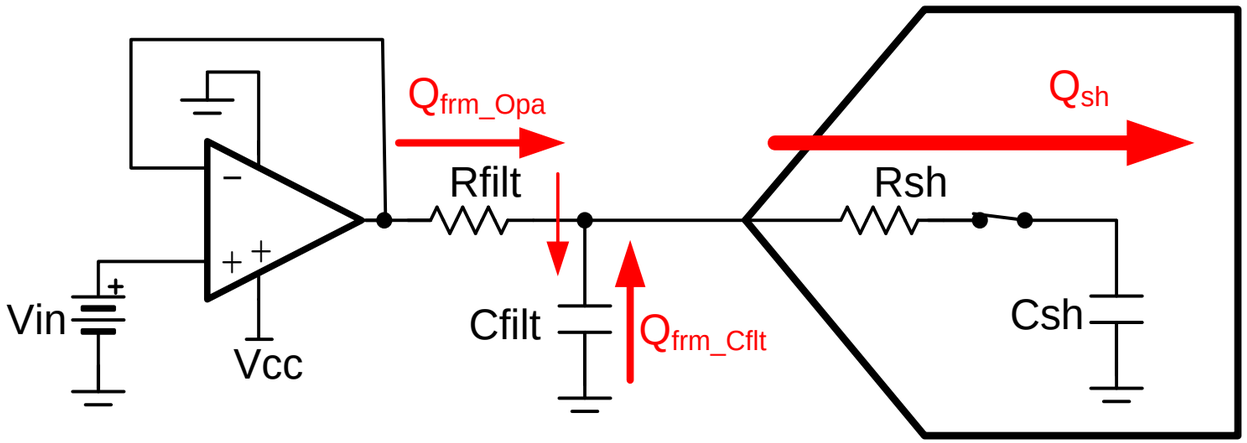
Concept behind the math





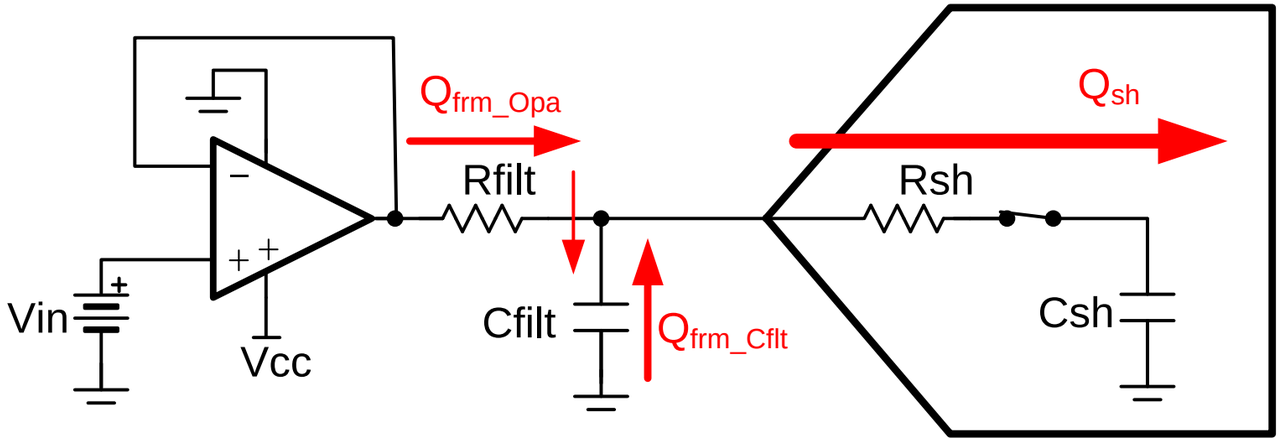
- Assumptions based on multiple designs
- Vin = Full Scale
- ½ of Q_{sh} is from C_{filt} & ½ from Op Amp
- 100mV Droop – small signal response
- Error target = 0.5·LSB
- Op amp approximated as second order system
- Op amp four times faster than filter

C_{filt} Selection



$Q_{sh} = V_{FSR} \cdot C_{sh}$	(1)	Total Charge in Csh and the end of acquisition period.
$Q_{sh} = Q_{frmOpa} + Q_{frmCfilt}$	(2)	Charge is from amplifier and filter capacitor
$\Delta Q_{Cfilt} = 0.5 \cdot Q_{sh}$	(3)	Half the sample and hold charge (Q_{sh}) is delivered from the filter. This results in a change in the charge on Cfilt.
$\Delta Q_{Cfilt} = 0.5 \cdot V_{FSR} \cdot C_{sh}$	(4)	From (1), and (3)
$\Delta Q_{Cfilt} = \Delta V_{filt} \cdot C_{filt}$	(5)	The change in charge on Cfilt will cause a droop in voltage. ΔV_{filt}
$C_{filt} = \left(\frac{0.5 \cdot V_{FSR}}{\Delta V_{filt}}\right) C_{sh}$	(6)	From (4), and (5). This is the general relationship for scaling Cfilt, given a droop in filter voltage (Vfilt)

C_{filt} Scaling Continued



$C_{filt} = \left(\frac{0.5 \cdot V_{FSR}}{\Delta V_{filt}}\right) C_{sh}$	(6)	From previous slide: This is the general relationship for scaling Cfilt, given a droop in filter voltage (Vfilt).
Assume $V_{FSR} = 4V,\ \Delta V_{filt} = 100mV$		
$\boldsymbol{C_{filt} = 20 \cdot C_{sh}}$	(7)	**Typical value for Cfilt**
$C_{filt} = 30 \cdot C_{sh}$	(8)	Maximum value for Cfilt
$C_{filt} = 10 \cdot C_{sh}$	(9)	Minimum value for Cfilt

Note 1: Experience shows that using the fixed factors of 20 yields good results.
Note 2: In rare cases, you may need to sweep Cfilt. Thus the factors of 10 and 30.

Time constant required for settling to error target

$V_{filt} = (V_{init} - V_{final}) \cdot e^{-t/\tau_c} + V_{final}$	(9)	This is the standard RC charge equation. τ_c = time constant for charging C_{sh}. V_{init} = initial voltage at start of t_{acq} V_{final} = final voltage for fully charged C_{filt}
$-0.5 \cdot LSB = V_{filt} - V_{final}$	(10)	Error is less than ½ LSB
$V_{init} - V_{final} = -100mV$	(11)	Droop is 100mV
$-0.5 \cdot LSB = (-100mV) \cdot e^{-t/\tau_c}$	(12)	Substitute 10 and 11 into 9
$\tau_c = \dfrac{-t_{acq}}{\ln\left(\dfrac{0.5 \cdot LSB}{100mV}\right)}$	(13)	Solve (12) for τ_c Note: τ_c includes effects from Op Amp and C_{filt} The op amp is being modeled as a second order system (RC circuit)

Find Rfilt and Amplifier Bandwidth

$\tau_c = \sqrt{(\tau_{RC})^2 + (\tau_{OA})^2}$	(15)	τ_c can be approximated as the RSS of the time constant of the filter and the op amp.
$\tau_{RC} = 4 \cdot \tau_{OA}$	(16)	Rule of thumb for good settling
$\tau_c = \sqrt{(4 \cdot \tau_{OA})^2 + (\tau_{OA})^2}$	(17)	Substitute (16) into (15)
$\tau_{OA} = \frac{\tau_c}{\sqrt{17}}$	(18)	Solve (17)
$\tau_{RC} = 4 \cdot \left(\frac{\tau_c}{\sqrt{17}}\right)$	(19)	Substitute (18) into (16)
$R_{filt} = \frac{\tau_{RC}}{C_{filt}}$	(20)	Nominal filter resistance.
$\boldsymbol{R_{filt_min} = 0.25 \cdot R_{filt}}$	**(21)**	**Minimum value of Rfilt used in SPICE iteration**
$\boldsymbol{R_{filt_max} = 2 \cdot R_{filt}}$	**(22)**	**Maximum value of Rfilt used in SPICE iteration**
$\boldsymbol{UGBW = \frac{1}{2 \cdot \pi \cdot \tau_{OA}}}$	**(23)**	**Minimum amplifier bandwidth**

Thanks for your time!