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Testing and Troubleshooting Your Ethernet Phy Design Using TI's Embedded Phy Diagnostics

Kevin Herring – TI Field Applications Engineer

Minneapolis Tech Day – October 24th 2017

Agenda

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- Ethernet Signal Chain Review
- DIY Diagnostic Cables and Tools
- Tools and Techniques for Debug
- Frequently Asked Questions

Applications | Ethernet is Everywhere

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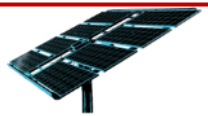




- Motor Drivers
- E-meter Concentrators
- IP Network Cameras
- Power Relays

- Factory Robots
- Network Printers
- Inspection Equipment
- Medical Equipment

- Solar Panels
- Communication Repeaters
- Human Sensing Equipment
- Cash Machines

Factory Automation

Remote Motor Drive and Control

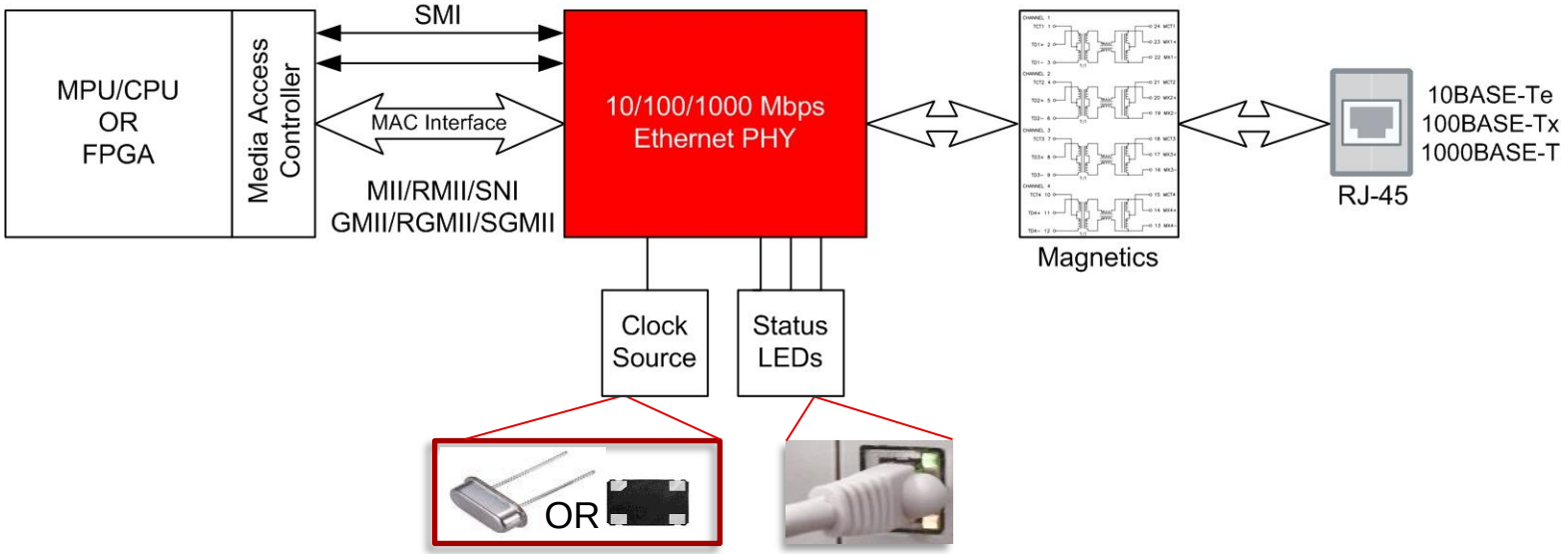
Building Automation

Smart Grid

Test and Measurement

Why Use TI Ethernet Phy's?

The Ethernet signal chain from MAC to RJ45 is complex. Fortunately, TI Phys have built in diagnostics and great support to make your designs go smoothly. You will be glad you chose TI Ethernet Phy's!

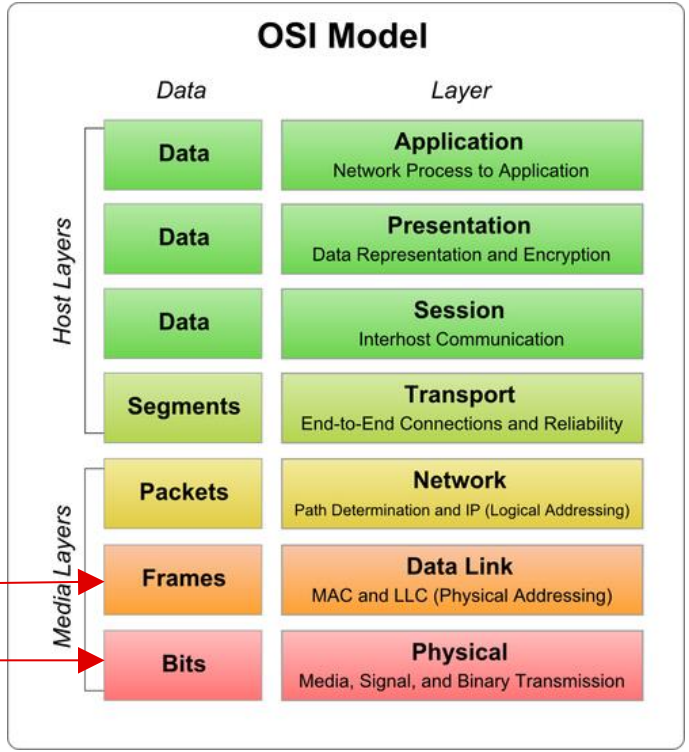


Common Terminology

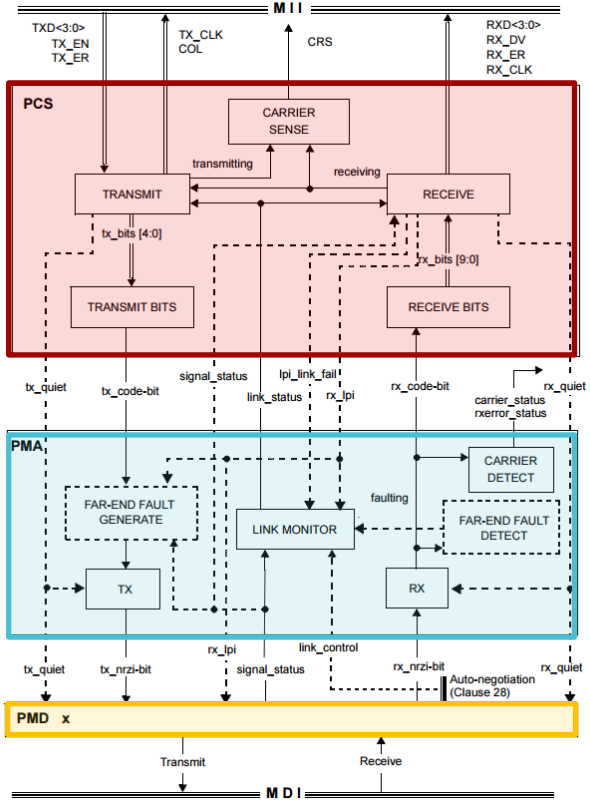
- PHY (Physical Layer Transceiver/Device) provides a way to transfer digital data from one node (processor, FPGA, ASIC…) to another node via analog signaling over either copper or fiber optic cable
- Three important processes a PHY handles:
  - PCS, Physical Coding Sublayer
  - PMA, Physical Medium Attachment
  - PMD, Physical Medium Dependent
- Other Key Terms:
  - MDI, Medium Dependent Interface (TD±/RD±)
  - MII, Media Independent Interface (Digital pins, TX_D[3:0]/RX[3:0] etc…)

Networking and Ethernet PHYs

- OSI Model describes the different layers of a networking system according to their functions
- Each layer communicates with layers above and below
- Information is passed via a Protocol Data Unit (PDU)
- Every layer will re-format and process the PDU before sending it over to the other layer.
- Ethernet MACs operate on Layer 2.
- Ethernet PHYs operate on Layer 1



Complex System within each PHY!



Ethernet Signals on the Cable Media

10BASE-T Transmission

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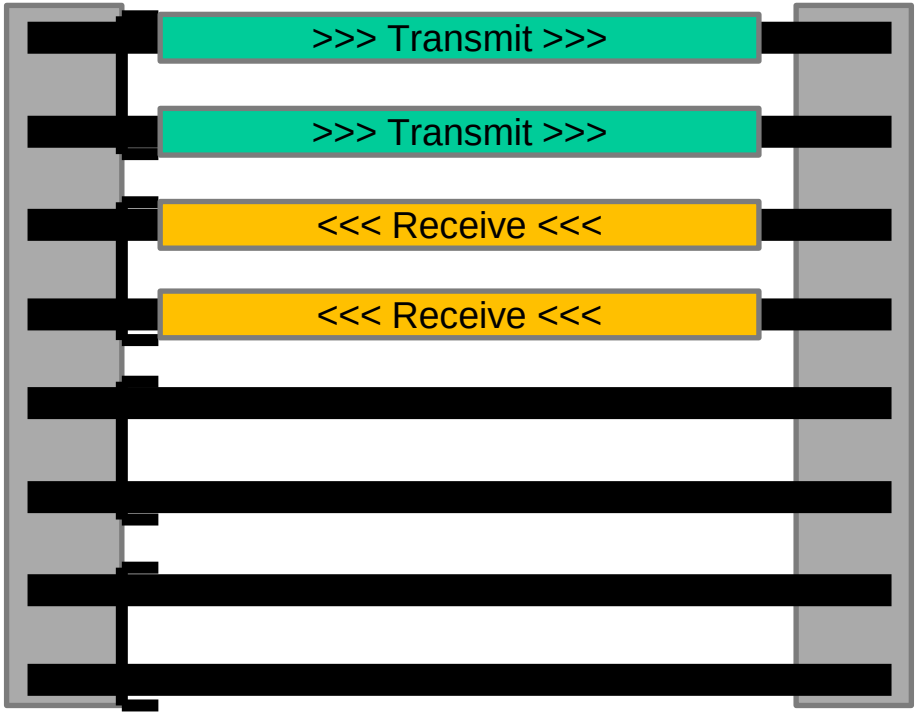
Coding

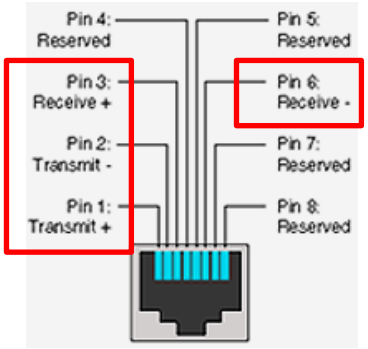
+1

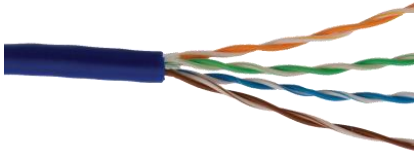
0

Manchester

UTP Category 5 Cabling Utilization



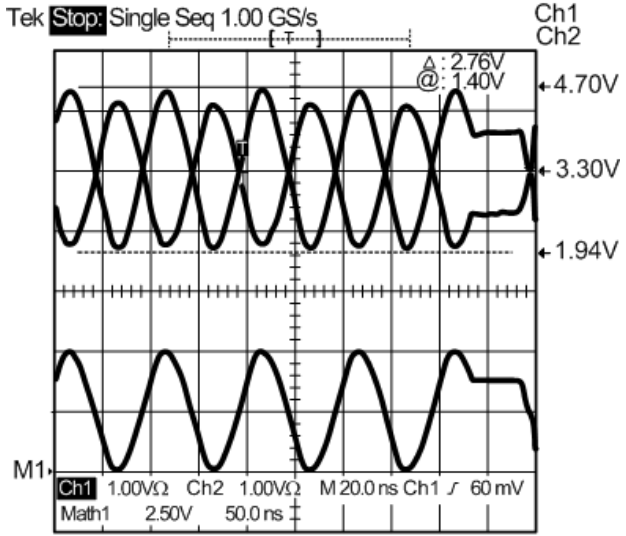




10Base-T Overview

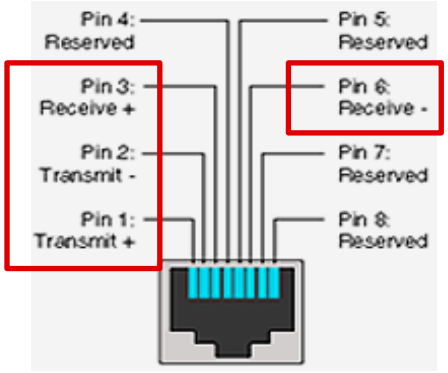
10 Mb/s has the following characteristics:

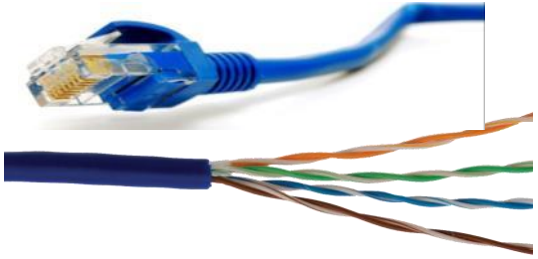
- Data rate: 10 Mb/s
- Signaling: 10 MHz, Differential, Manchester
- Return Loss: >15.0dB @5 – 10 MHz
- Encoding: Manchester
- Maximum Required Cable Length (per IEEE standard): 100m
- Cabling: CAT-5 twisted pair, 100 Ohm
- Wires used: 2 pair
- Specification: IEEE 802.3
- Bit error rate: 1 error in 10e8 bits



100BASE-TX Signal Transmission

Coding	UTP Category 5 Cabling Utilization
-1 0 +1 3-Level MLT	>>> Transmit >>> >>> Transmit >>> <<< Receive <<< <<< Receive <<<





100BASE-TX Signal Overview

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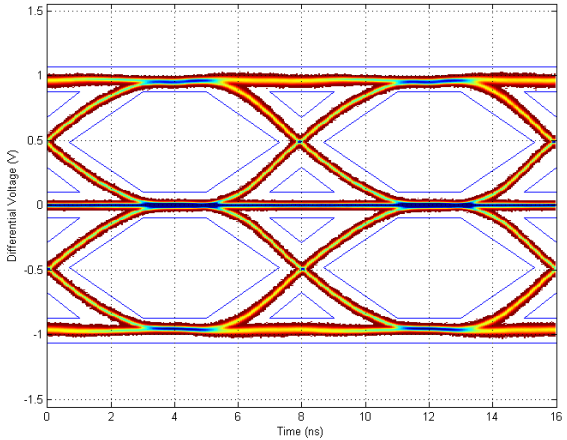
100 Mb/s or Fast Ethernet has the following characteristics:

- Data rate: 100 Mb/s
- Signaling: 125 MHz, Differential, MLT-3 (3 level Multi Level Transitions)
- Return Loss: 16.0dB @2 - 30 MHz, 10.0dB @60 - 80 MHz
- Encoding: 4b5b (4 bits of data for 5 bits transferred)
- Max Cable Length (per IEEE standard): 100m
- Cabling: CAT-5 twisted pair, 100 Ohm
- Wires used: 2 pair
- Specification: IEEE 802.3u
- Bit error rate: 1 error in 10e8 bits

Figure 1: MLT-3 Eye Diagram (Informative)



DP83822 – TI's Latest 10/100Mbps PHY

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Highlights

- **Industry's Lowest Power 10/100Mbps PHY**
  - 1.8V operation <110mW
- Small package **QFN32** (5mmx5mm)
- Long cable reach >150m
- **100BASE-TX, 100BASE-FX** and **10BASE-Te**

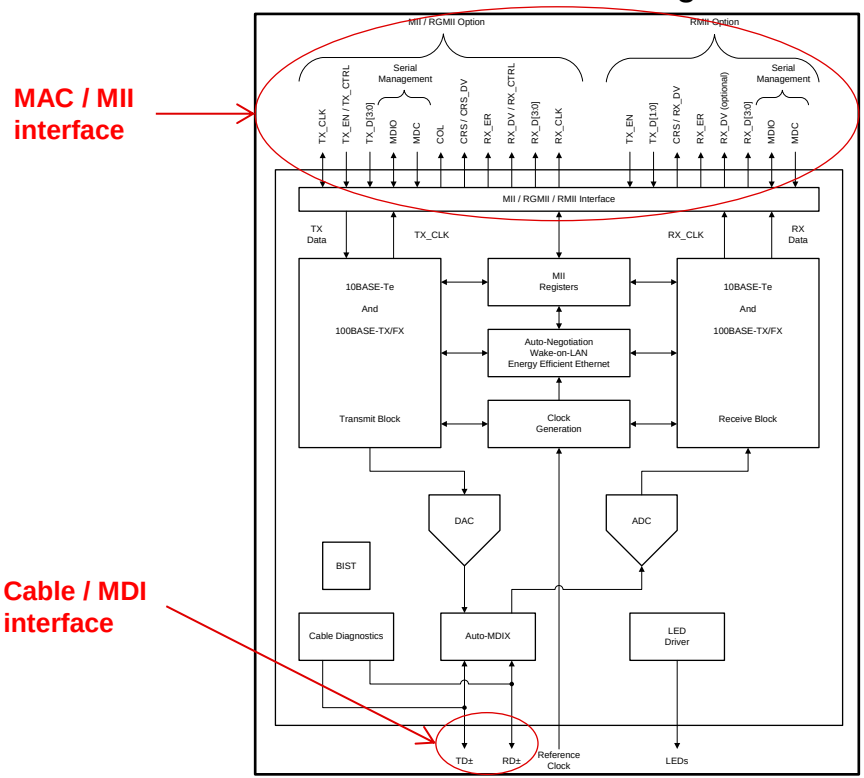
Key Specs

- MII / RMII / RGMII MAC Interfaces
- HBM (**+/-16kV**), IEC61000-4-2 (**+/-8kV**)
- **Start of Frame Detection for IEEE1588**
- Industrial Temperature Range **-40C to 85C/125C**

Applications

- Factory Automation, Motor Drives, Power Automation, Industrial Lighting

DP83822 Block Diagram



1000-BASE-T Transmission

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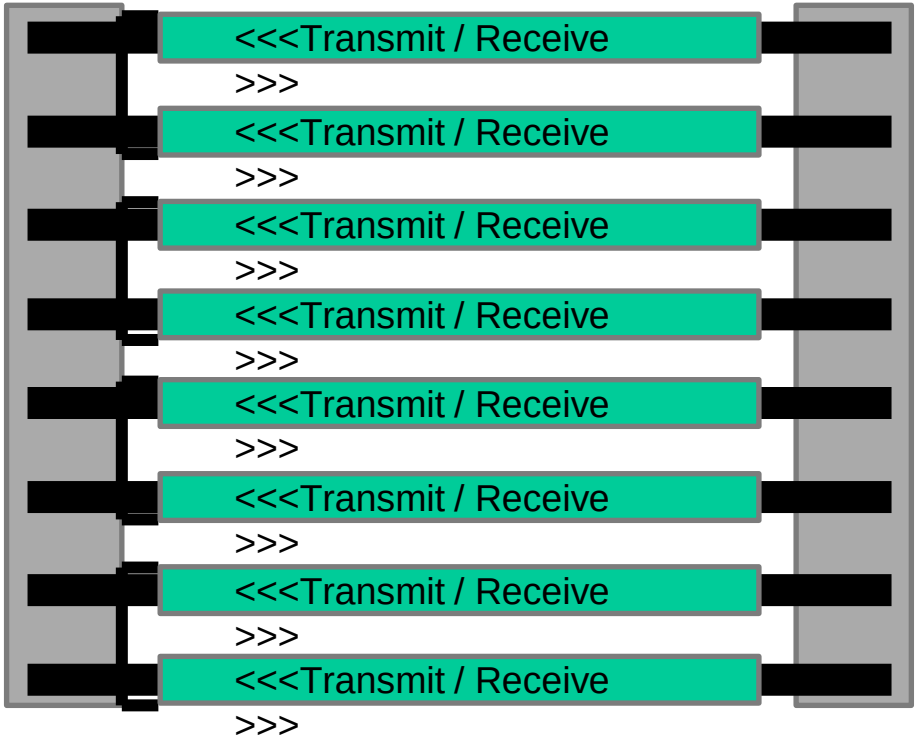
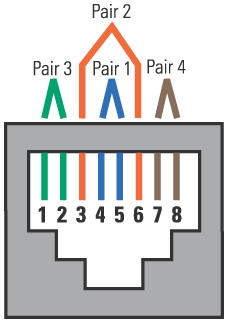
Coding

+2
+1
0
-1
-2

5-Level
PAM-5

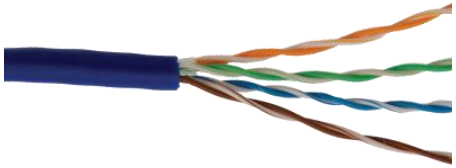
UTP Category 5 Cabling Utilization





Pair ID	PIN #
T1	5
R1	4
T2	3
R2	6
T3	1
R3	2
T4	7
R4	8

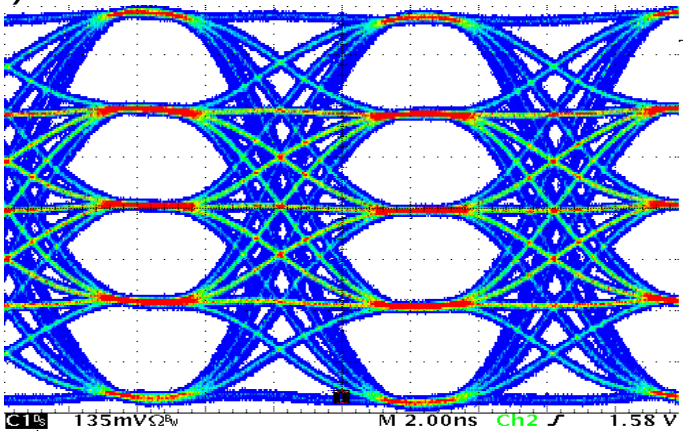
T568A



Ethernet Signaling – 1000BASE-T

1000 Mb/s or Gigabit Ethernet has the following characteristics:

- Data rate: 1000 Mb/s
- Signaling: 125 MHz, Differential, PAM-5 (Pulse Amplitude Modulation)
- Return Loss: 19.0dB @1 - 100 MHz (~100m)
- Encoding: 8b10b (8 bits of data for 10 bits transferred)
- Maximum Required Cable Length (per IEEE standard): 100m
- Cabling: CAT-5 twisted pair, 100 Ohm
- Wires used: 4 pair (each Full Duplex)
- Specification: IEEE 802.3
- Bit error rate: 1 error in 10e10 bits



DP83867 – TI's Latest 1Gb Phy

10/100/1000 Low Power and Robust Ethernet PHY

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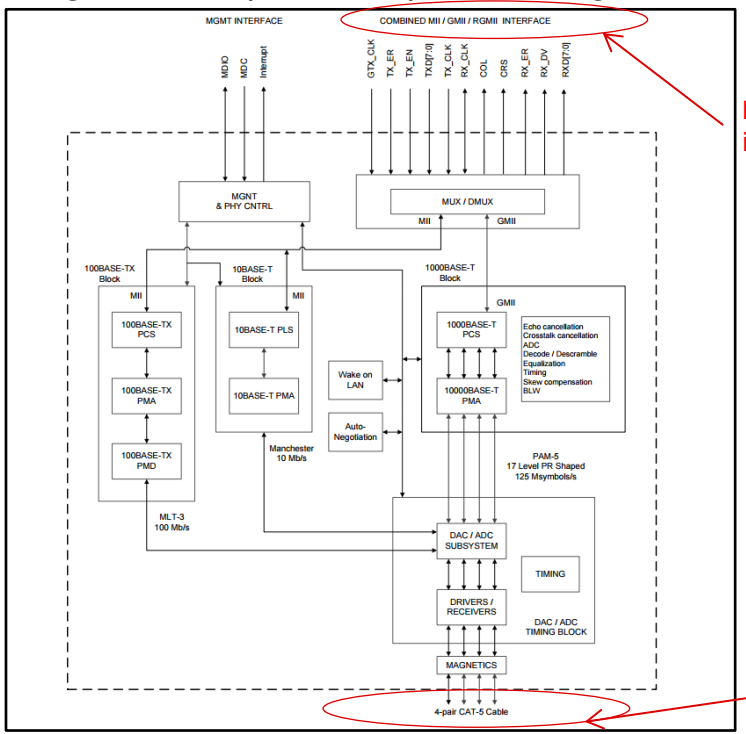
- **Highlights**
  - **IEC 12kV specification!**
  - Lowest latency for both 100Mbps and 1Gbps modes, <400ns
  - Power saving features: WoL
  - **Pass EN55011 class B**
  - **Low power 1GbE solution, <400mW**

- **Key Specifications**
  - GMII/RGMII/MII/SGMII
  - **Start of Frame Detect for IEEE 1588 time stamp**
  - JTAG (IEEE 1149.1)
  - 25MHz or 125MHz Output clock
  - Pin to pin temperature grades (0 to 70C) through **(-40C to 105C)**
  - **QFN48** or QFP64

- **Applications**
  - Industrial: Automation, Test Equipment, Sensors
  - Communications: Debug /Management Port, Small Cell
  - Commercial: Network Printers, Broadband gateways

Gigabit PHY (DP83867) Block Diagram



Where to look for more information?

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- 100BASE-X PCS and PMA specifications located in Clause 24 of the IEEE802.3 Standard (Section Two)
- 100BASE-TX PMD specifications located in Clause 25 of the IEEE802.3 Standard (Section Two)
- 100BASE-FX PMD specifications located in Clause 26 of the IEEE802.3 Standard (Section Two)

Agenda

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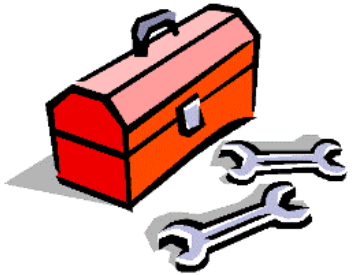
- Ethernet Signal Chain Review
- **DIY Diagnostic Cables and Tools**
- Tools and Techniques for Debug
- Frequently Asked Questions

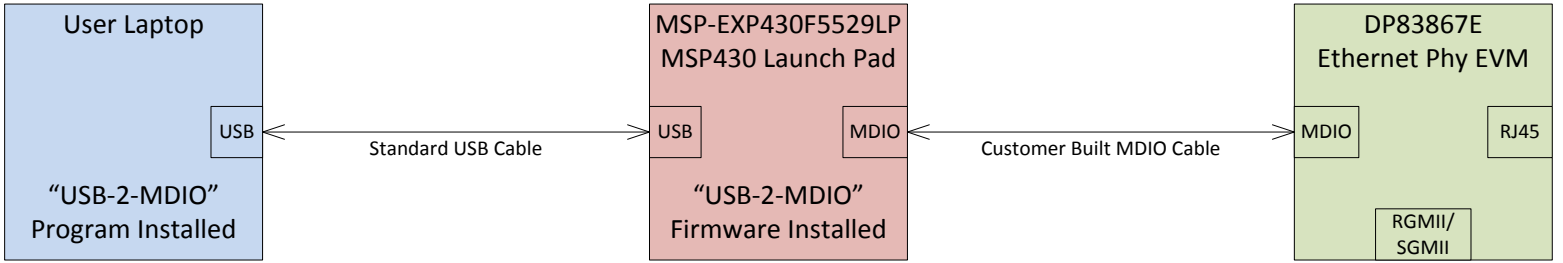
Building an Ethernet Debug Toolbox
What Will You Need?

- Interface Board and GUI to Control Phy Registers Through SMI Port
- A Library of Control Scripts to Use and Modify as Needed
- The Embedded Diagnostic Tools that TI Provides in the DP83867 Gig Phy and DP83822 10/100Mb Phy
- Build Your Own Custom Cables for Diagnostics



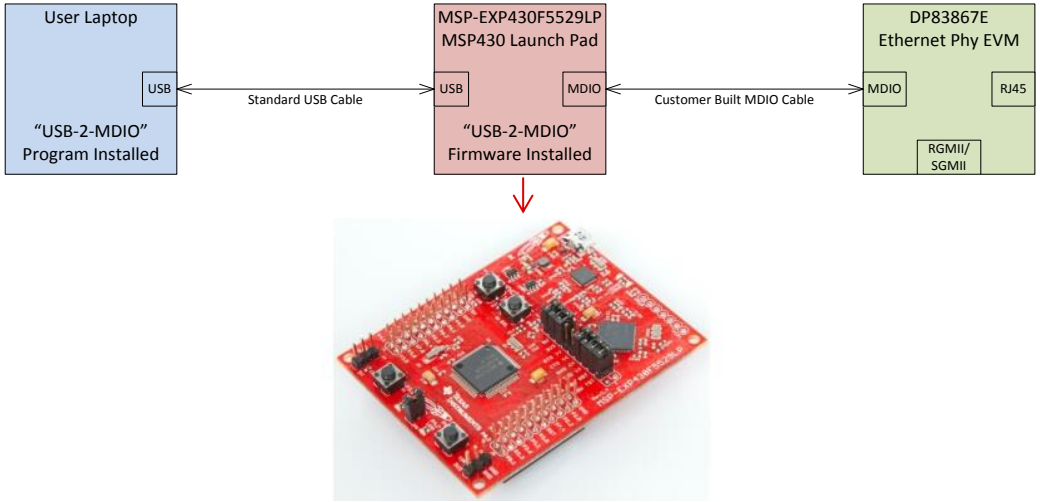
Create Interface Board to R/W the Registers

- TI Phys contain a Serial Management Interface (SMI) port that allows complete Read/Write access of the internal registers.
- The SMI port is sometimes called an MDIO port and can be useful for debugging a new Phy design even when you don't have your host firmware complete.
- You can also use the SMI to execute scripts that aid you in IEC61000-4-x or other compliance testing by generating Ethernet traffic or test signals.
- TI provides a free GUI called "USB-2-MDIO" and instructions to create the hardware needed to unlock this powerful SMI port. The image below shows how the "USB-2-MDIO" hardware blocks work together.



Creating the MDIO Interface Board

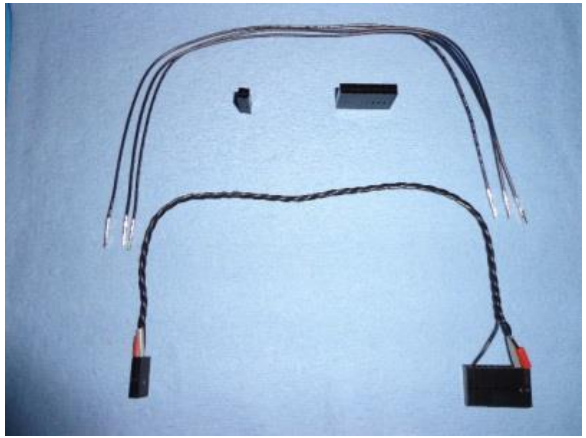
- The hardware board that converts the laptop USB signals to MDIO signals is a standard MSP430 Launch Pad EVM that can be purchased from the TI store for $12.99.
- When you purchase the board you will need to do a one time install of a special flash image that does the USB to MDIO signal conversion. The flash image is included in the “USB-2-MDIO” software.
- The example below shows the MSP-EXP430F5529LP but other MSP430 EVMs can be used. See the “USB-2-MDIO” User Guide for a complete list of compatible MSP430 EVMs.

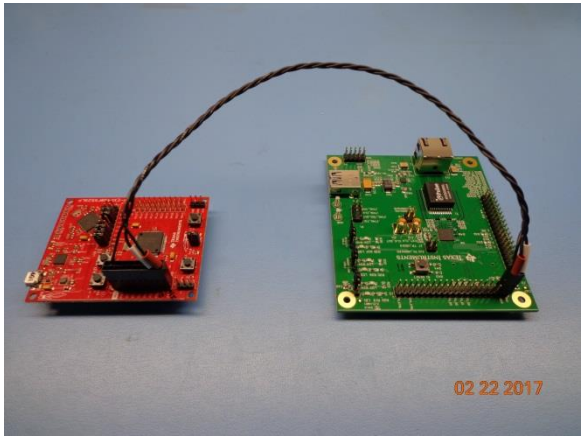


Creating the MDIO Cable

- You will need to build a custom MDIO cable that connects the MPS430 Launch Pad EVM to the MDIO port of the Phy.
- Any easy method is to purchase wires with pre-crimped pins and blank headers from DigiKey.
- Install the wires in the proper positions to match the MDIO pinout of the Phy EVM.
- The images below shows an example MDIO cable for the “DP83867ERGZ-R-EVM” Gig Phy

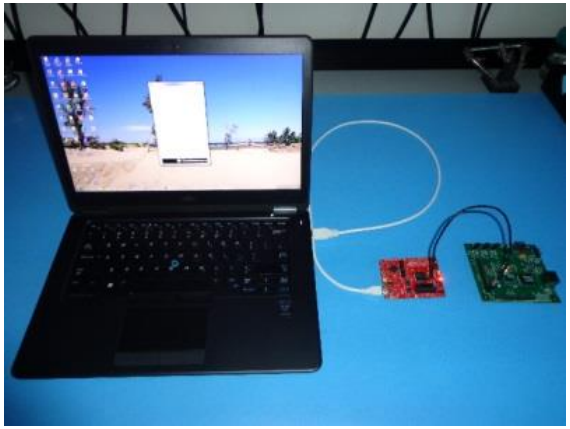
Qty	DigiKey Part #	Description
1	WM2519-ND	4 Position Connector Housing
1	WM2527-ND	20 Position Connector Housing
3	797580011	Pre-Crimped Wires

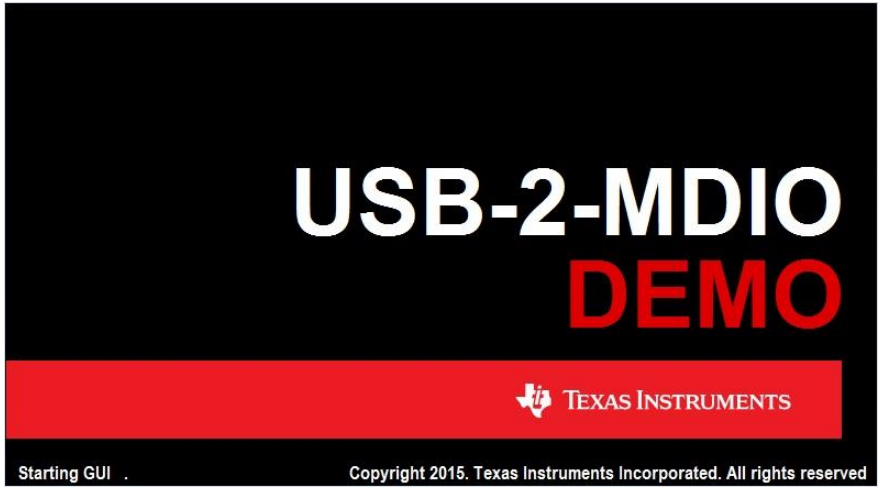




USB-2-MDIO Software

- The ability to access registers of the PHY is a important debug tool.
- PHY registers can be accessed through the MDIO data pin and MDC clock pin using the MDIO cable you build.
- USB-2-MDIO Software uses a MSP430 Launchpad that has a special flash image loaded to read and write registers on TI PHYs.
- The USB-2-MDIO software can be downloaded at: http://www.ti.com/tool/usb-2-mdio
- The software comes with installation instructions and User's guide.
- Download and install the USB drivers for the MSP430-EXP430F5529LP Launch Pad Here: http://software-dl.ti.com/msp430/msp430_public_sw/mcu/msp430/MSP430_FET_Drivers/latest/index_FDS.html





USB-2-MDIO Software

Select Extended Register Access

Set the Phy ID

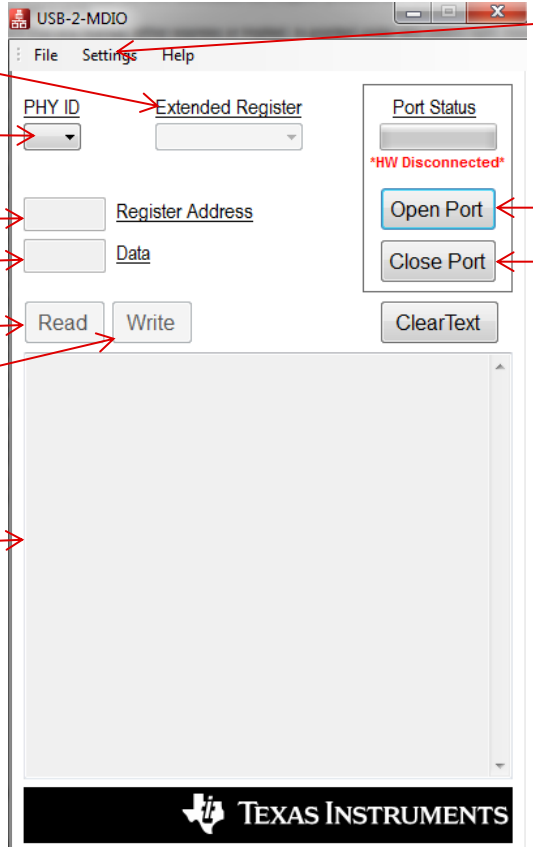
Address of desired Register

Desired Data to be written

Read Command

Write Command

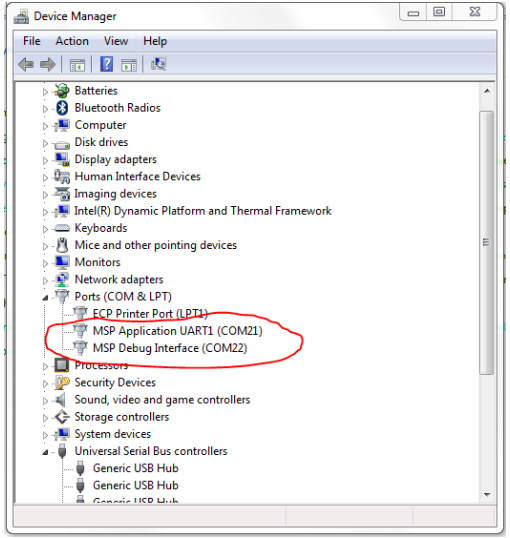
Text Box for displaying Register Read/Write



The MSP430 will show two COM Ports in Device Manager. Under “Settings” select the COM port address that corresponds to “MSP Application UART1”. This is COM21 in the screen shot below.
Under “Settings” select Baud Rate 9600.

Open COM Port

Close COM Port



Register Description

- Registers serve dual purpose
  - Indicators of PHY status
  - Control functionality of the PHY
- Register tables will list the position of the bit, name, Default value, Read Only or Read Write and Bit Description.
- Using the USB2MDIO Software and Register table from Datasheets, the PHY can be configured to operate in the desired mode.

Basic Mode Status Register (BMSR)

Basic Mode Status Register (BMSR), Address 0x0001

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	100BASE-T4	0, RO/P	100BASE-T4 Capable: 0 = Device not able to perform 100BASE-T4 mode.
14	100BASE-TX FULL DUPLEX	1, RO/P	100BASE-TX Full Duplex Capable: 1 = Device able to perform 100BASE-TX in full duplex mode.
13	100BASE-TX HALF DUPLEX	1, RO/P	100BASE-TX Half Duplex Capable: 1 = Device able to perform 100BASE-TX in half duplex mode.
12	10BASE-Te FULL DUPLEX	1, RO/P	10BASE-Te Full Duplex Capable: 1 = Device able to perform 10BASE-Te in full duplex mode.
11	10BASE-Te HALF DUPLEX	1, RO/P	10BASE-Te Half Duplex Capable: 1 = Device able to perform 10BASE-Te in half duplex mode.
10	100BASE-T2 FULL DUPLEX	0, RO/P	100BASE-T2 Full Duplex Capable: 0 = Device not able to perform 100BASE-T2 in full duplex mode.
9	100BASE-T2 HALF DUPLEX	0, RO/P	100BASE-T2 Half Duplex Capable: 0 = Device not able to perform 100BASE-T2 in half duplex mode.
8	EXTENDED STATUS	1, RO/P	1000BASE-T Extended Status Register: 1 = Device supports Extended Status Register 0x0F.
7	RESERVED	0, RO	RESERVED: Write as 0, read as 0.
6	MF PREAMBLE SUPPRESSION	1, RO/P	Preamble Suppression Capable: 1 = Device able to perform management transaction with preamble suppressed, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. 0 = Normal management operation.
5	AUTO-NEGOTIATION COMPLETE	0, RO	Auto-Negotiation Complete: 1 = Auto-Negotiation process complete. 0 = Auto-Negotiation process not complete.
4	REMOTE FAULT	0, RO/LH	Remote Fault: 1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far End Fault Indication or notification from Link Partner of Remote Fault. 0 = No remote fault condition detected.
3	AUTO-NEGOTIATION ABILITY	1, RO/P	Auto Negotiation Ability: 1 = Device is able to perform Auto-Negotiation. 0 = Device is not able to perform Auto-Negotiation.
2	LINK STATUS	0, RO/LL	Link Status: 1 = Valid link established. 0 = Link not established. The criteria for link validity is implementation specific. The occurrence of a link failure condition will causes the Link Status bit to clear. Once cleared, this bit may only be set by establishing a good link condition and a read via the management interface.

Register reference for DP83867

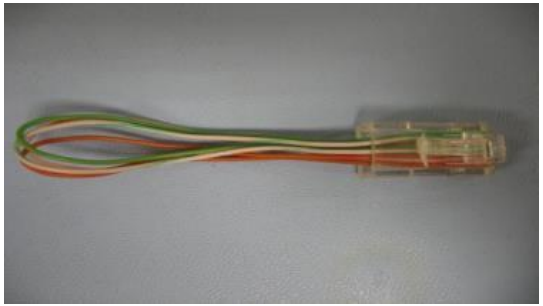
Important Registers

- Following are some of the common registers which are important for configuration and status check:
  - Basic Mode Control Register (BMCR) Register Address 0x00h
  - Basic Mode Status Register (BMSR) Register Address 0x01h
  - Auto-Negotiation Advertisement Register (ANAR) Register Address 0x04h
  - Auto-Negotiation Link Partner Ability Register (ANLPAR) Register Address 0x05h
  - PHY Status Register (PHYSTS) Register Address 0x10h
- There will be other important registers specific to the device.
- Refer to respective datasheet for more information on registers.

More Useful Cables You Can Build!

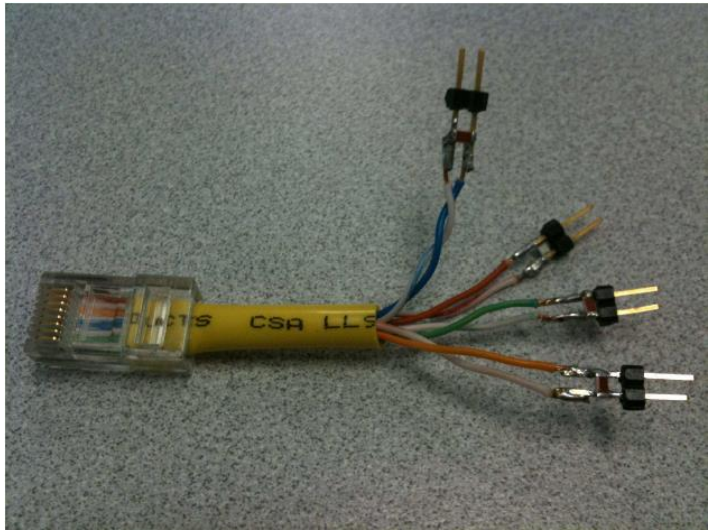
Create an External Loopback Cable

- The External Loopback cable is used for 10/100Mbps Loopback testing. This cable does not work for 1Gbps testing.
- The Loopback cable connects the Tx output to the Rx input at the RJ45 connector.
- This cable allows you to test the entire Ethernet signal path including the Ethernet transformer using TI's built in diagnostics.
- Using a loop of wire to make the connections will provide best signal path and reduce reflections. Simply twisting the two wires together could create an unwanted stub.



Create a 100Ω Terminated Cable

- The 100Ω terminated cable is used for multiple diagnostic tests.
- Cut of the end of an Ethernet CAT 5e cable. Then solder on a 0.10” two pin header with 100Ω termination resistor on each twisted pair.
- This cable is useful for scope waveform capture with differential probe or when using the internal analog loopback of the Phy.



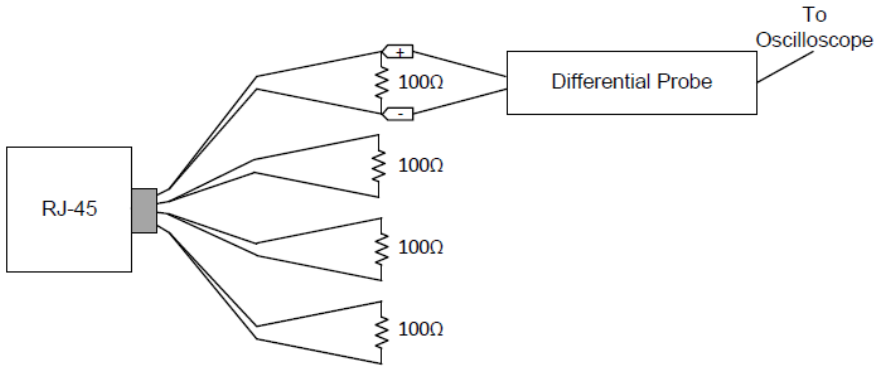


Figure 6. Connection Diagram for 100M Terminated Cable

Agenda

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- ✓ Ethernet Signal Chain Review
- ✓ DIY Diagnostic Cables and Tools
- ✓ **Tools and Techniques for Debug**
- ✓ Frequently Asked Questions

Hardware Debug – Start with Simple Stuff

Application Notes Show How to Use Your New Tools for Testing and Troubleshooting

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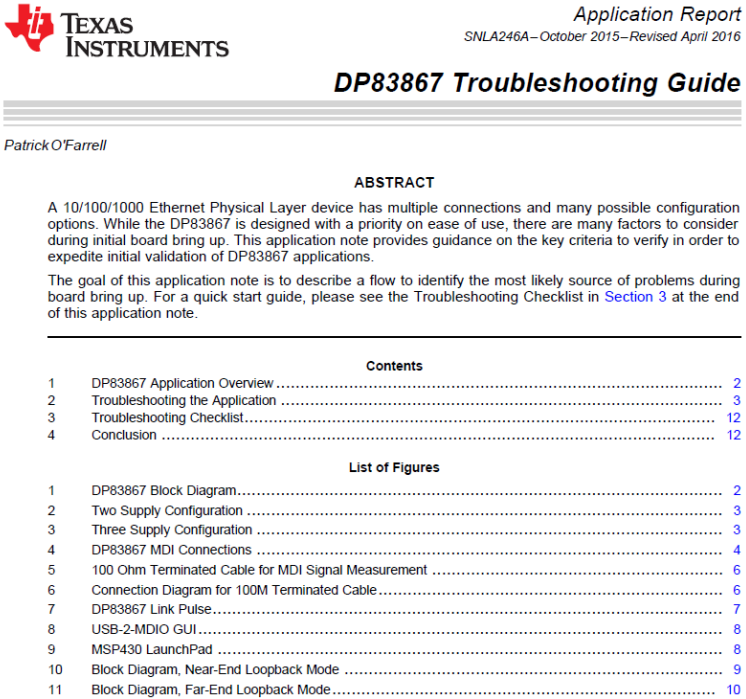
Don’t forget to read the datasheet first for troubleshooting ideas. Not all Phys have the same diagnostics. The datasheet will show what is available for each device.

Example Application Note Descriptions	App. Note File Name
DP83867 Troubleshooting Guide	snla246a.pdf
DP83822 IEEE 802.3u Compliance and Debug	snla266.pdf
How to Configure DP838xx for Ethernet Compliance Test	Snla239a.pdf
4-Level Strap Device Configuration	Snla258.pdf
DP83822 Energy Efficient Ethernet	Snla265.pdf
Reducing Radiated Emissions in Ethernet	Snla107a.pdf

Example App Note – DP83867



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Application Report

SNLA246A–October 2015–Revised April 2016

DP83867 Troubleshooting Guide

Patrick O'Farrell

ABSTRACT

A 10/100/1000 Ethernet Physical Layer device has multiple connections and many possible configuration options. While the DP83867 is designed with a priority on ease of use, there are many factors to consider during initial board bring up. This application note provides guidance on the key criteria to verify in order to expedite initial validation of DP83867 applications.

The goal of this application note is to describe a flow to identify the most likely source of problems during board bring up. For a quick start guide, please see the Troubleshooting Checklist in Section 3 at the end of this application note.

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Ethernet Debug Techniques

TECH DAYS
Texas Instruments

Power down the board and **verify key resistances**

1. Verify resistance to ground across the RBIAS resistor
2. Verify resistance across the transmit and receive
3. Verify resistance across the MDIO
   – Problems can occur when a very small (10's of Ohms) pull-up resistor is used.
4. Verify magnetics connections

Power up the board and **verify key voltages**

1. Probe the **Power rails**
2. Probe the **PFBOUT** and **PFBIN** pins (only for 10/100 PHYs)
   - The PFBOUT pin is a regulated 1.8V supply generated inside the device from the 3.3V supply. The device will not operate correctly if the PFBIN pins do not receive this 1.8V supply.
3. Probe the **RBIAS** pin
   - Voltage should be ~1.2V for 10/100 PHY and ~1.0V for DP83867

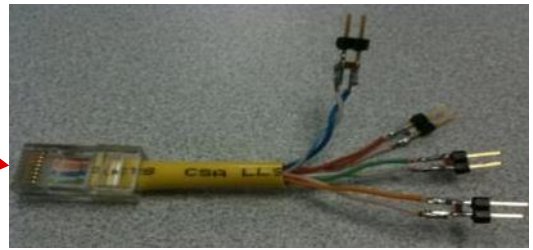
More information: DP83867 Troubleshooting Guide (SNLA246)

Ethernet Debug Techniques

TECH DAYS Texas Instruments

Power up the board and **verify key signals**

1. Probe the **RESET_N** signal
   – The reset input is active low and is connected to a 10 kOhm pull down resistor. It is important to confirm that the controller is not driving the RESET_N signal low. Otherwise, the device will be held in reset and will not respond.
2. Probe the **X1 clock**
   – Verify the frequency and signal integrity. For link integrity the clock needs to be within +/- 50ppm of the default (25MHz for MII / 50MHz for RMII).
3. Probe **strap pins** during initialization.
   – In some cases, other devices on the board (e.g. MAC) will pull or drive these pins unexpectedly.
4. Probe the **TD+/- transmit signals**
   – Measure the transmit voltages using a 100 Ohm terminated Pig-tail cable



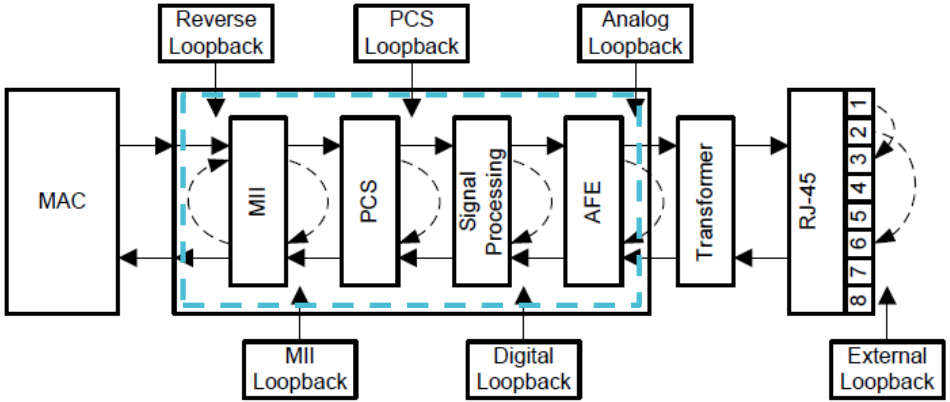
More information: DP83867 Troubleshooting Guide (SNLA246)

Putting Your New Tools to Work!

Examples of Diagnostic Tests

Loopback Test Modes

- TI provides several diagnostic loop back test modes in the Phy that allow data to pass from the MAC to the Phy and then back to the MAC.
- Some loops are closed within the Phy and some loops are closed externally using a loopback cable.
- These test modes allow the digital and analog sections of the Phy to be tested.



Register Scripts for Loopback – SNLA266

Loopback and BIST Mode Scripts for the DP83822

B.1 MII Loopback 100BASE-TX Script

```
begin
001F 8000      //software reset (clears register)
0000 6100      //programs DUT to 100BASE-TX mode and enables MII Loopback
001F 4000      //digital reset (doesn't clear register)
end
```

B.2 MII Loopback 10BASE-Te Script

```
begin
001F 8000      //software reset (clears register)
0000 4100      //programs DUT to 10BASE-Te mode and enables MII Loopback
001F 4000      //digital reset (doesn't clear register)
end
```

B.3 Analog Loopback 100BASE-TX Script

```
begin
001F 8000      //software reset (clears register)
0000 2100      //programs DUT to 100BASE-TX mode
0019 0021      //programs DUT to Forced MDI mode, set to 4021 for MDIX mode
0016 0108      //enables analog loopback mode
001F 4000      //digital reset (doesn't clear register)
end
```

B.4 Analog Loopback 10BASE-Te Script

```
begin
001F 8000      //software reset (clears register)
0000 0100      //programs DUT to 10BASE-Te mode
0019 0021      //programs DUT to Forced MDI mode , set to 4021 for MDIX mode
0016 0108      //enables analog loopback mode
001F 4000      //digital reset (doesn't clear register)
end
```


B.5 Reverse Loopback 100BASE-TX Script

```
begin
001F 8000      //software reset (clears register)
0000 2100      //programs DUT to 100BASE-TX mode
0016 0110      //enables reverse loopback mode
001F 4000      //digital reset (doesn't clear register)
end
```

B.6 Reverse Loopback 10BASE-Te Script

```
begin
001F 8000      //software reset (clears register)
0000 0100      //programs DUT to 10BASE-Te mode
0016 0110      //enables reverse loopback mode
001F 4000      //digital reset (doesn't clear register)
end
```

B.7 BIST 100BASE-TX Script

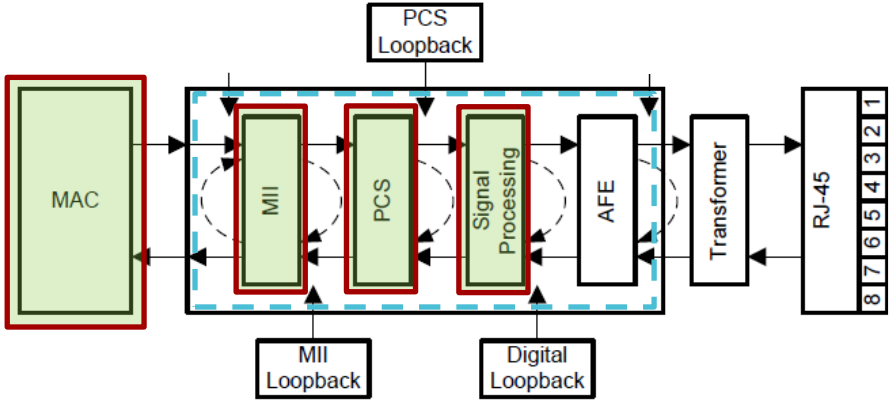
```
begin
001F 8000      //software reset (clears register)
0000 2100      //programs DUT to 100BASE-TX mode
001B 007D      //bits[7:0] determine IPG, default 0x7D is equal to 125 bytes
001C 05EE      //bits[10:0] determine packet length, default 0x05EE is equal to 1518 bytes
0016 7100      //enable continuous error check BIST mode
001F 4000      //digital reset (doesn't clear register)
end
```

B.8 BIST 100BASE-TX with Analog Loopback Script

```
begin
001F 8000      //software reset (clears register)
0000 2100      //programs DUT to 100BASE-TX mode
0019 0021      //programs DUT to Forced MDI mode
001B 007D      //bits[7:0] determine IPG, default 0x7D is equal to 125 bytes
001C 05EE      //bits[10:0] determine packet length, default 0x05EE is equal to 1518 bytes
0016 7108      //enable continuous error check BIST mode with analog loopback mode
001F 4000      //digital reset (doesn't clear register)
end
```

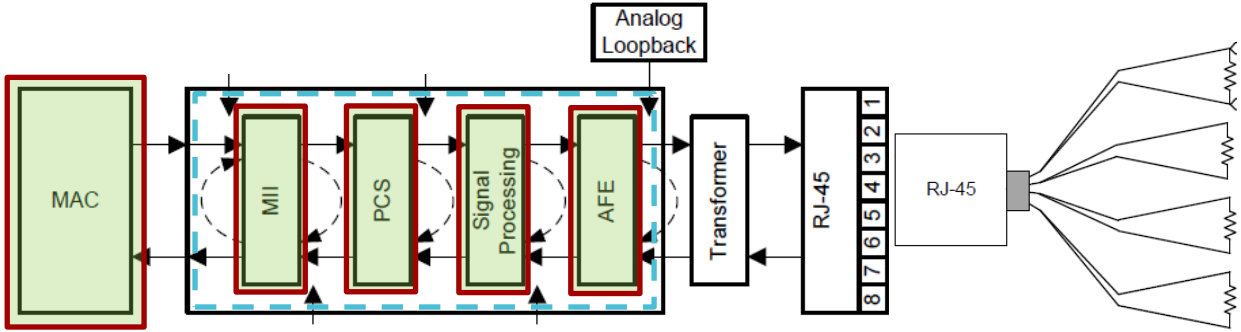
Near-End Digital Loopback Test Modes

- “Near-End” loop back means the test signals originate in the MAC.
- Near-End Digital Loopback will test the following blocks:
  - MII Block
  - PCS Block
  - Signal Processing Block



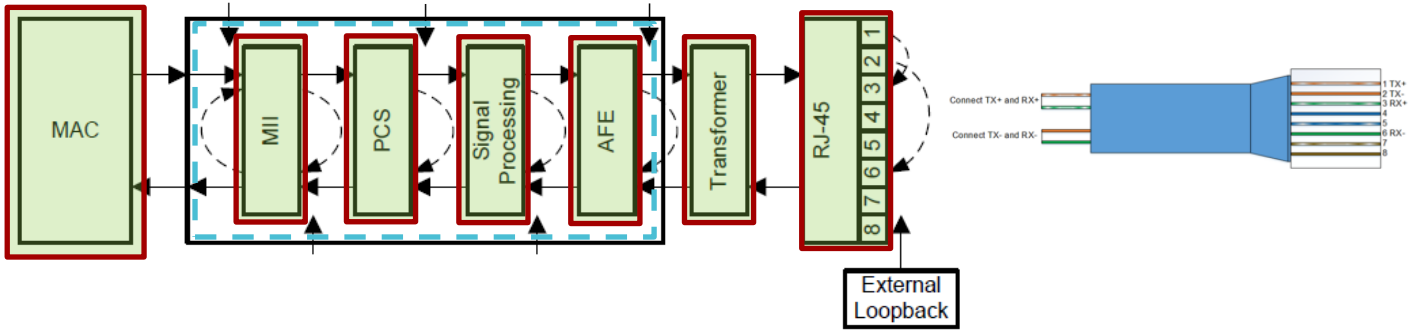
Near-End Analog Loopback Test Modes

- “Near-End” loop back means the test signals originate in the MAC.
- Near-End Analog Loopback can test the following blocks:
  - MII Block
  - PCS Block
  - Signal Processing Block
  - AFE (Analog Front End) Block



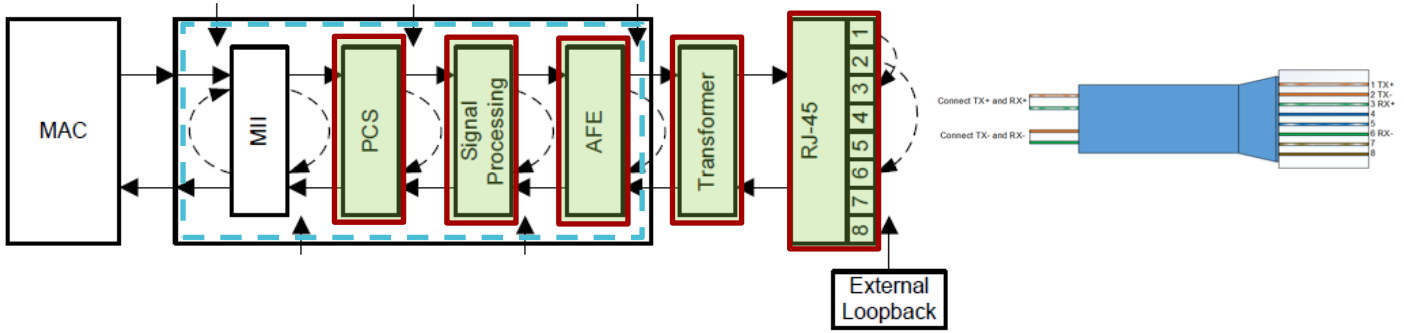
Near-End External Loopback Test

- External loopback tests all blocks in the Phy and the external Ethernet components. This test requires the external loopback cable that you build. This test only works for 10/100Mb speeds which have dedicated Tx/Rx pairs. Gigabit speeds cannot be tested this way.
- External Loopback will test:
  - All Phy Blocks
  - The Ethernet Transformer
  - The RJ45 and Associated Passive Components



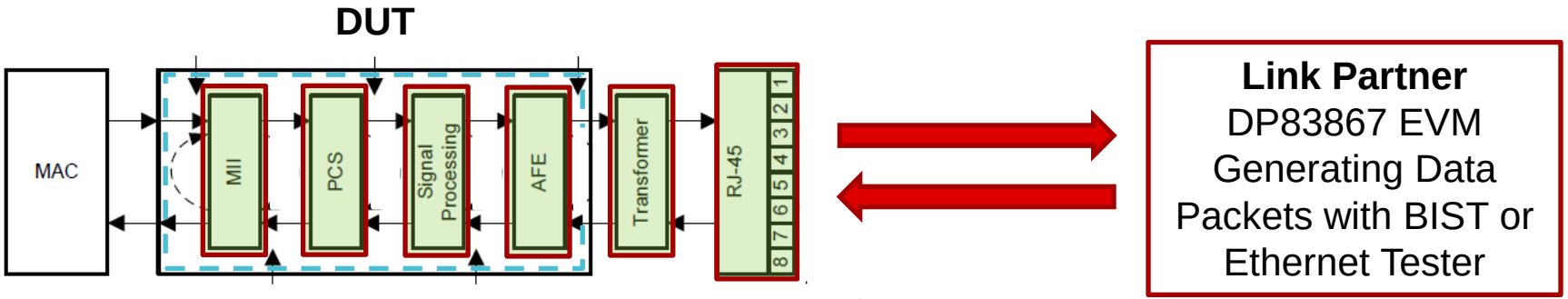
BIST Packet Generator – DP83867 / DP83822

- Built In Self Test (BIST) data is generated in the PCS block so no MAC host is needed.
- BIST simulates pseudo-random data transfer in the format of real packets and Inter-Packet Gap (IPG) on the data lines. You can configure packet size and IPG.
- The BIST circuit can be used to test the integrity of the transmit and receive data paths.
- The receive path has a packet checker that counts and reports errors.
- BIST supports internal loopback of digital or analog blocks. BIST will support external loopback at 10/100Mb.



Far-End (Reverse) Loopback

- Far-end (Reverse) Loopback is a special test mode to allow testing the PHY from the link-partner side. No MAC is required on the Device Under Test (DUT) side of link.
- In this mode, data that is received from the link partner passes through the PHY's receiver, is looped back at the MAC interface and transmitted back to the link partner.
- While in Reverse Loopback mode, all data signals that come from the MAC are ignored.



Cable Diagnostics – TDR and ALCD

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- Many TI Phys support Time Domain Reflectometry (TDR) and Active Link Cable Diagnostics (ALCD). DP83867 is example used in following descriptions.
- For TDR the Phy sends a pulse of known amplitude down each cable pair and measure the time for return pulses. This method does not work when data is on the line.
- TDR can detect cable opens, shorts, miswired pairs, damaged connectors and cable length to within +/-1m.
- TDR registers save up to five reflections for each pair. The host controller performs simple math to determine the length to reflection point.
- The DP83867 can be programed to automatically run TDR when link is dropped to aid in troubleshooting intermittent connections.
- The ALCD is a passive method to measure cable length when data present in active link.
- ALCD relies on uses passive digital signal processing based on adapted data. Accuracy is +/-5m and can be measure only in the receive pair.

Time Domain Reflectometer (TDR) with DP83822/DP83867

In Design

TI-Design: Proof of concept

TIDesigns

Features

- Detect Ethernet cable faults
  - Open connection, Shorted lines, Single-pair failure, Single-line failure, Connector corrosion
- TI Ethernet PHYs
  - DP83822 (10/100Mbit)
  - DP83867 (10/100/1000Mbit)
- C-Software source code
  - Manual trigger of TDR by industrial application / host stack
  - Automatic trigger of TDR when Ethernet PHY link-down

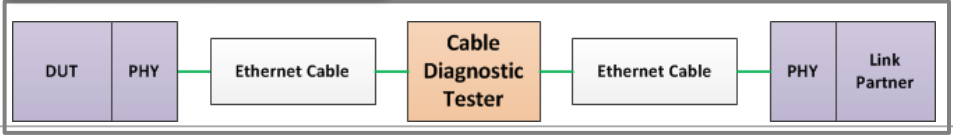
Benefits

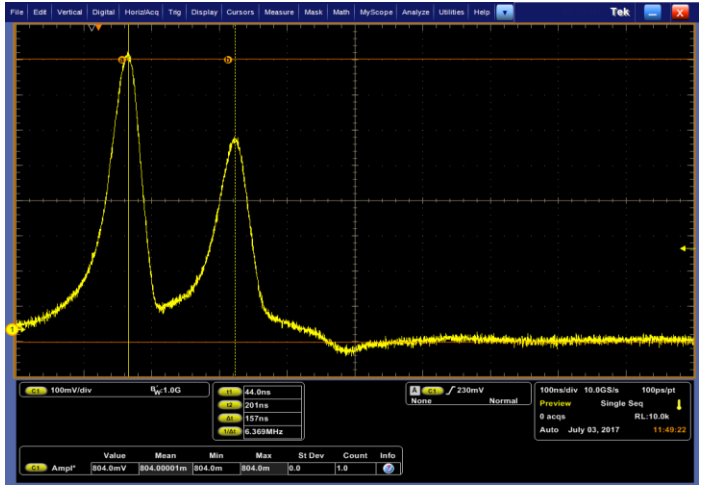
- Predictive maintenance for industrial Ethernet
- Detect cable fault types and cable fault distance (meters) from PHY
- TDR configuration library for ARM host integration
- Simulated with Cable Diagnostic Tester to simulate cable faults

Target Applications

- Industrial
- Factory Automation and Process Control
  - Communication Module
  - CPU (PLC Controller)

System Diagram





Agenda

TECH DAYS
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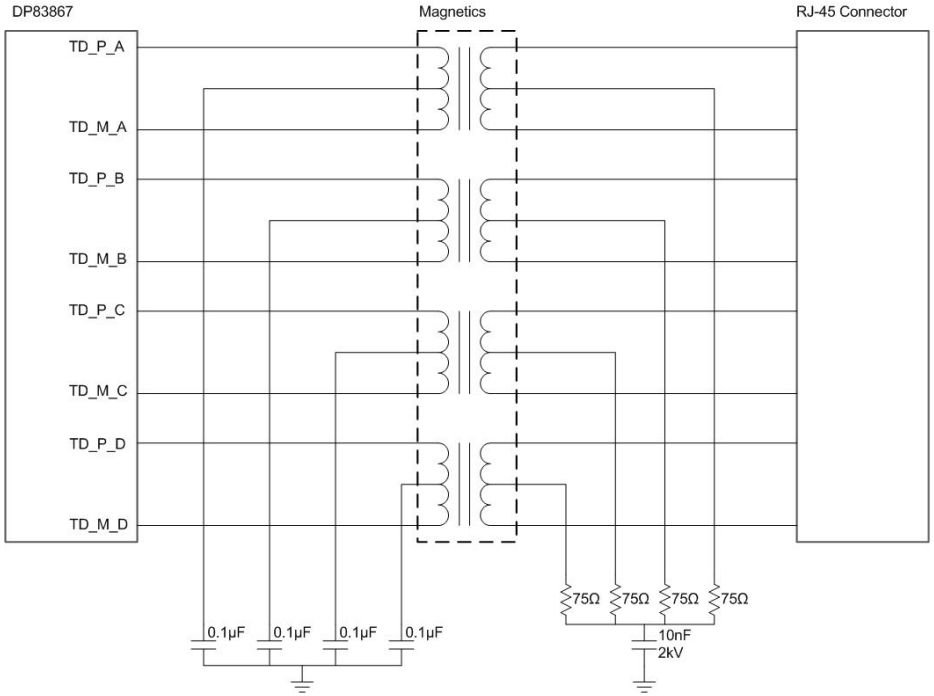
- ✓ Ethernet Signal Chain Review
- ✓ DIY Diagnostic Cables and Tools
- ✓ Tools and Techniques for Debug
- ✓ **Frequently Asked Questions**

FAQ

FAQ

What type of Line Driver is used by the DP83867?

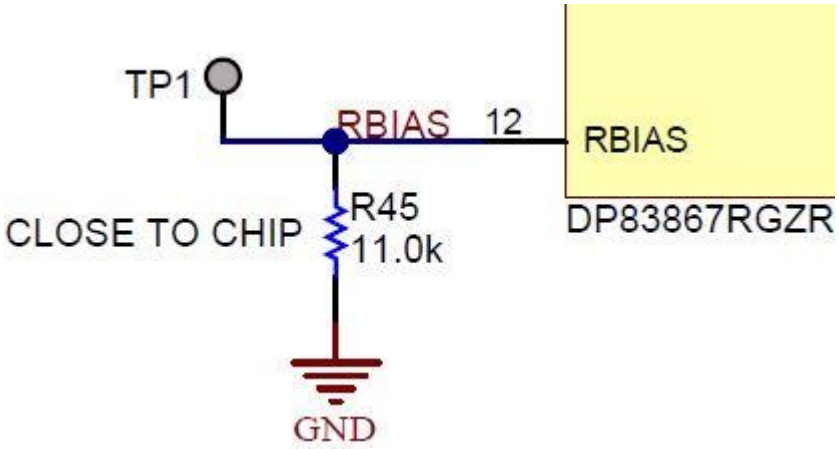
- The DP83867 has a voltage mode line driver.
- Connecting the magnetics center tap to a supply voltage is not necessary. No current is drawn from the magnetics by the PHY.
- No external 50 Ohm termination resistors are necessary. Terminations are inside the device.



FAQ (2)

What is the significance of the RBIAS resistor?

This resistor is used to develop the internal bias currents and voltages in the PHY. It is specified for 1% tolerance so that the PHY can meet the tightest IEEE 802.3 specifications.



FAQ (3)

What are some simple debug tests?

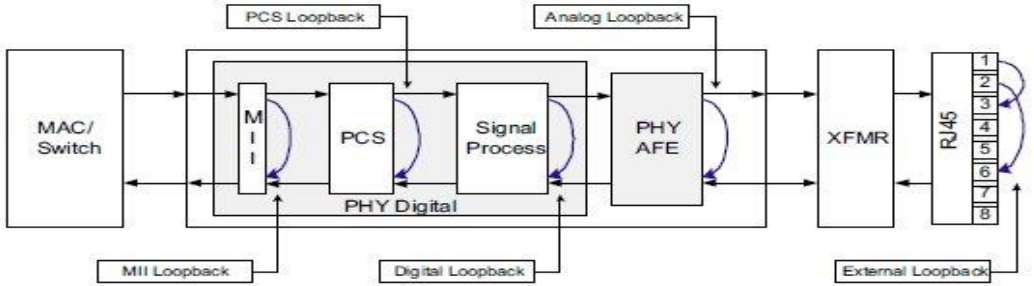
Loopback modes and Packet BIST (Built-in Self Test) can be used to loop packets through different paths within the PHY. This helps confirm functionality of individual portions of the PHY.

Perform packet testing from a link partner with far-end or reverse loopback.

Perform packet testing from the MAC with near-end loopback:

1. MII loopback
2. Digital loopback

** Packet BIST and internal loopback are configured via register access.



FAQ (4)

Do we have Linux Drivers?

We do have Linux driver for DP83848 and DP83867

DP83848 Linux Driver: http://www.ti.com/product/DP83848C/toolssoftware

DP83867 Linux Driver: http://www.ti.com/product/DP83867E/toolssoftware

FAQ (5)

Is it possible for customers to run IEEE compliance tests?

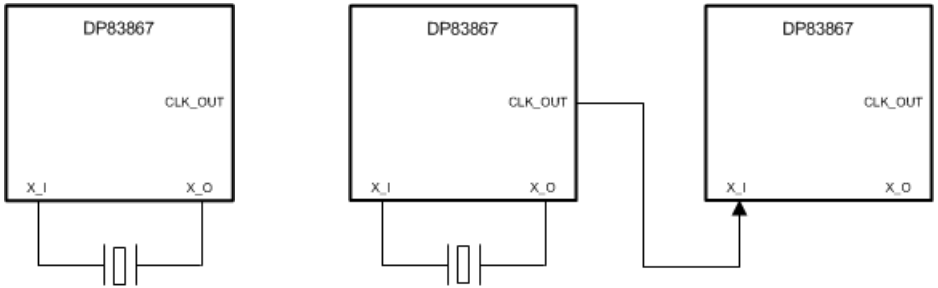
Yes, customers can use our EVMs to run compliance tests on our PHYs. Our Phys support IEEE test modes which can be activated through Register access.

Example App Note: http://www.ti.com/lit/an/snla239/snla239.pdf

FAQ (6)

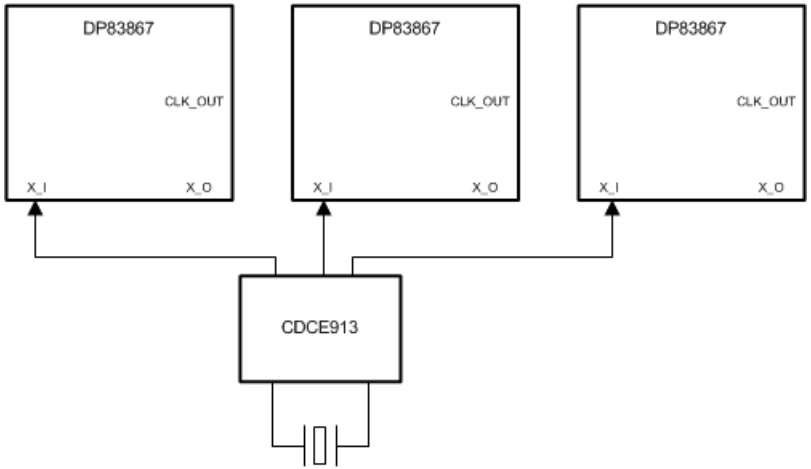
What are the clocking options for the DP83867?

Clocking is as easy as 1, 2, 3 (or more).



Use a crystal or oscillator for one DP83867

Use clock output to daisy chain two DP83867s



Use a TI clock generator for three or more DP83867s or multiple DP83867s and a uP/MCU/FPGA

FAQ (7)

Can I use my existing software with a TI PHY?

If the driver uses device specific functionality and uses registers that are not defined by IEEE 802.3, it should not be used.

- Is there device specific functionality?
  - Does current driver use features specific to the device (registers not defined by IEEE 802.3)?
  - Will new application require device specific features (interrupts, IEEE 1588, etc.)?
  - Does the driver check the IEEE 802.3 defined PHY Identifier Registers – PHYIDR1 (address 0x02) and PHYIDR2 (address 0x03)?
  - Does the driver require a specific PHY address (e.g. 0x00)?
- Which operating system is being used (Linux)?
  - Android runs on top of Linux (Android inherits the Linux environment) and should not be impacted by PHY initialization

FAQ (8)

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Steps to help customers new to Ethernet

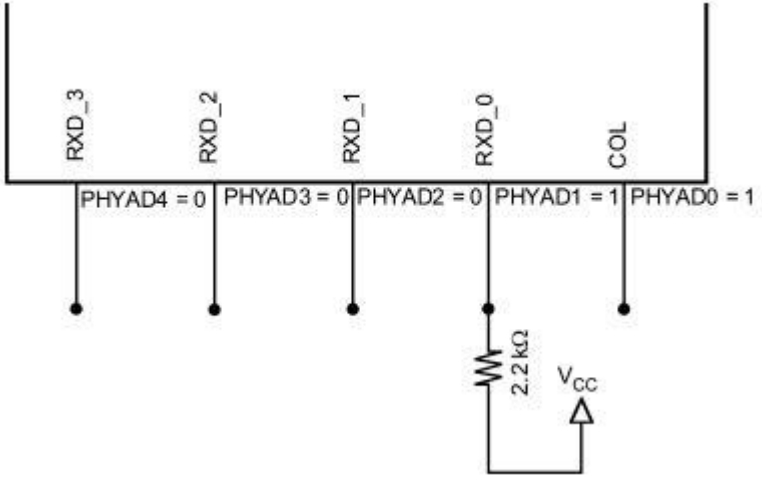
- Schematic and Layout Review
- Hardware debug techniques
- Register verification
- Apps Team engagement
  - E2E
  - Email

What are straps?

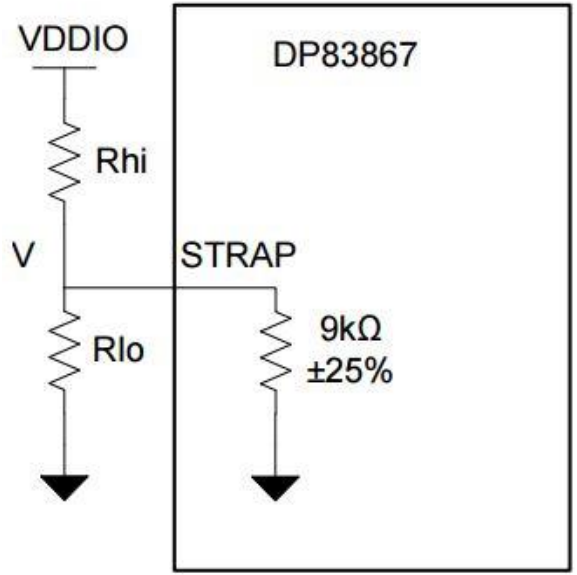
- Straps pins of the PHY are dual-functional pins.
- On Power-on or Reset, the voltage on strap pins are sampled.
- Depending on the voltage on these pins, the PHY will be configured in pre-determined functions.
- Two types of straps in TI Ethernet Portfolio devices
  - 2 level straps
  - 4 level straps
- Functions such as operating speed, Auto-MDIX, Auto-negotiation, MAC interface etc. can be controlled via straps
- Provides additional flexibility and removes needs of register writes. Faster bring up times!

2-Level vs 4-Level Straps

2-Level Straps



4-Level Straps



2-Level vs 4-Level Straps

2-Level Straps

- Relative simple, only 2 voltage levels
- One pin controls one function
- A single 2.2Kohm resistor to Vcc or GND.

4-Level Straps

- Comparatively complex, 4 voltage levels
- One pin can control 2 functions
- 2 resistor network may be needed.

Get Started Today!

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Customers can get started by:

- Purchase the DP83867IRPAP-EVM
  - Link for the e-store
- Visit links below for the latest documentation and product information
  - TIDA-00204 Design Page
  - DP83867IR Product Folder
  - DP83867 RGMII Linux Drivers
- Looking for a 10/100 PHY Ethernet solution from TI Designs?

  Visit the link below for the EN55011 Compliant, Industrial Temperature, 10/100Mbps Ethernet PHY Brick Reference Design
  - TIDA-00207 Design Page

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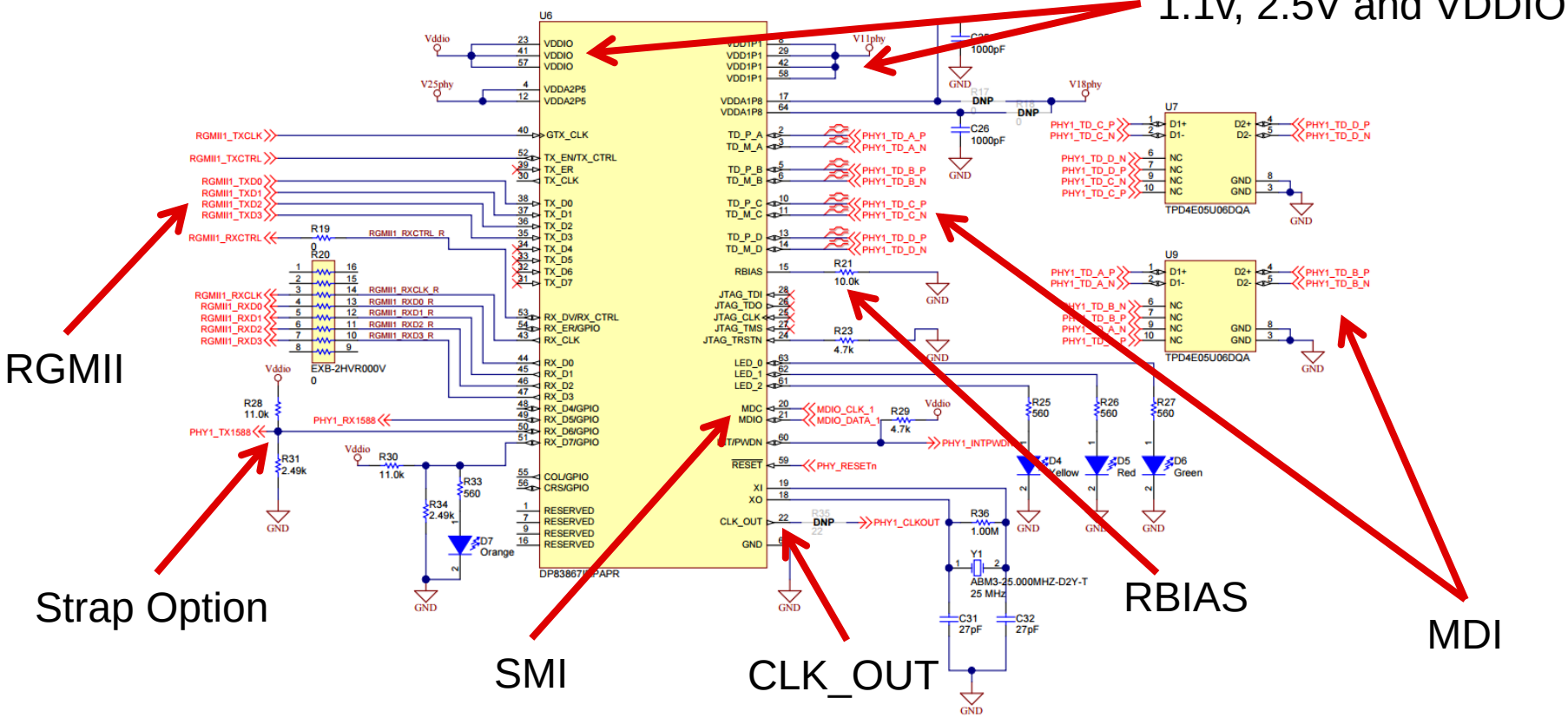
Thank You!

Backup Slides

DP83867IR PHY Design



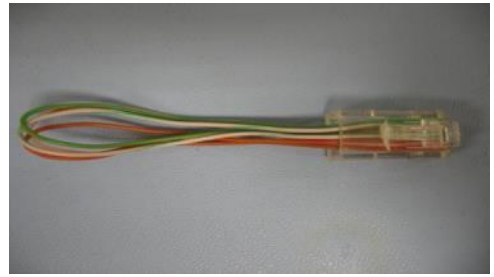
Things to look out for

- Verify voltage levels are within spec
  - Check decoupling on power rails with device datasheet recommendations
- Verify if Power sequencing is required
- Verify RBIAS resistor as per Datasheet
- Verify Termination resistors if required
- Verify that Crystal/Oscillator and Magnetics meet the requirements (SNLA079)
  - Check Loading capacitor with Crystal datasheet
  - Check recommended magnetics connections
- Verify strap resistors are as per requirements
- Check pull up resistor on MDIO
- Confirm LEDs configured as per strapping options
- Check Power Down and Reset pins
- Verify MDI traces are differentially coupled
- Check unused pins

Ethernet Debug Techniques

Power up the board and verify link

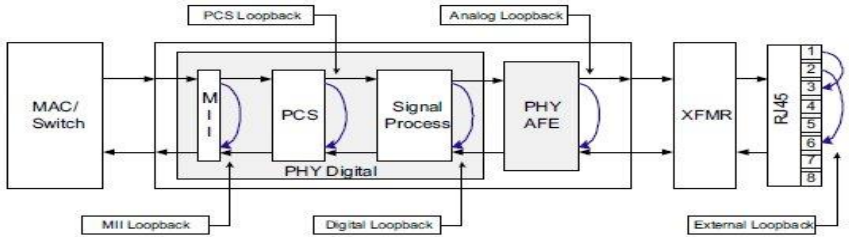
1. Verify link with known good link partner
2. For 10/100 PHYs a loopback cable can be used to verify link with itself.



Power up the board and perform packet testing

1. Packet BIST using internal loopback
2. Packet BIST using external loopback plug
3. MAC transmit and receive using internal loopback
4. MAC transmit and receive using external loopback plug
5. MAC transmit and receive with a known good partner

** Packet BIST and internal loopback are configured via register access.

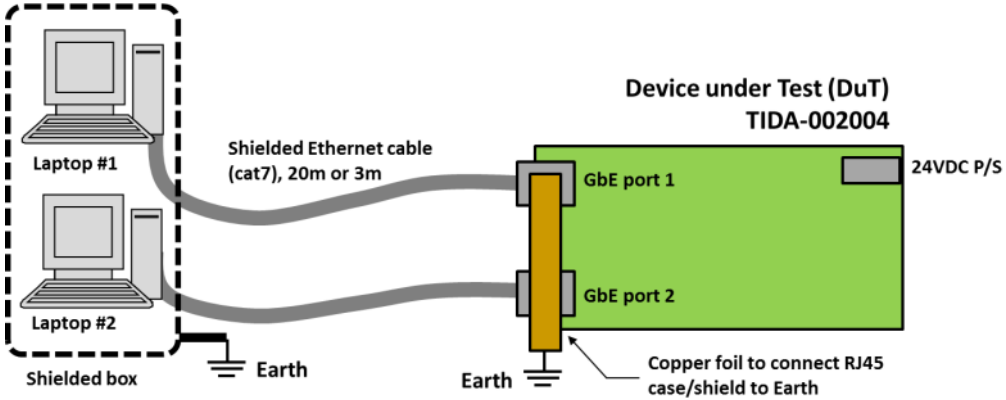


Phy loopback modes

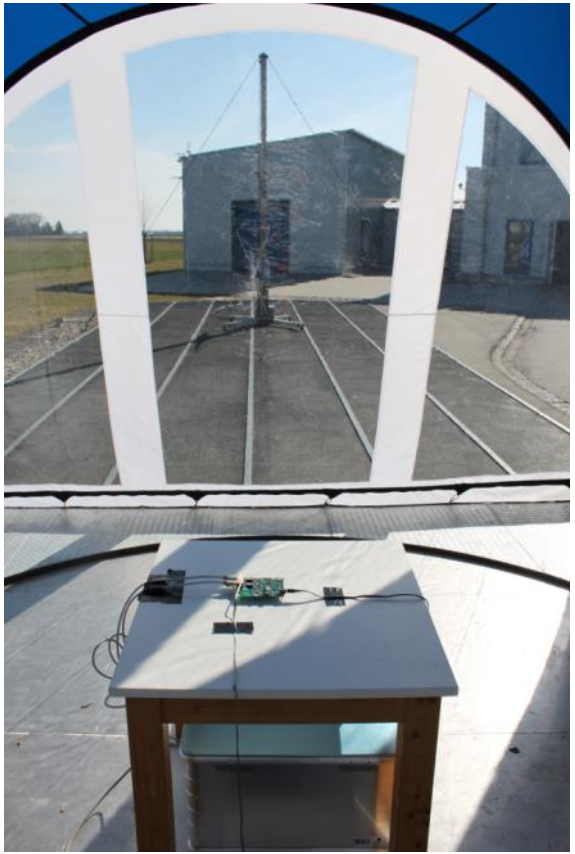
More information: DP83867 Troubleshooting Guide (SNLA246)

EMI (EN55011) Test Setup

Console: Monitor data integrity during and after test for each port under test



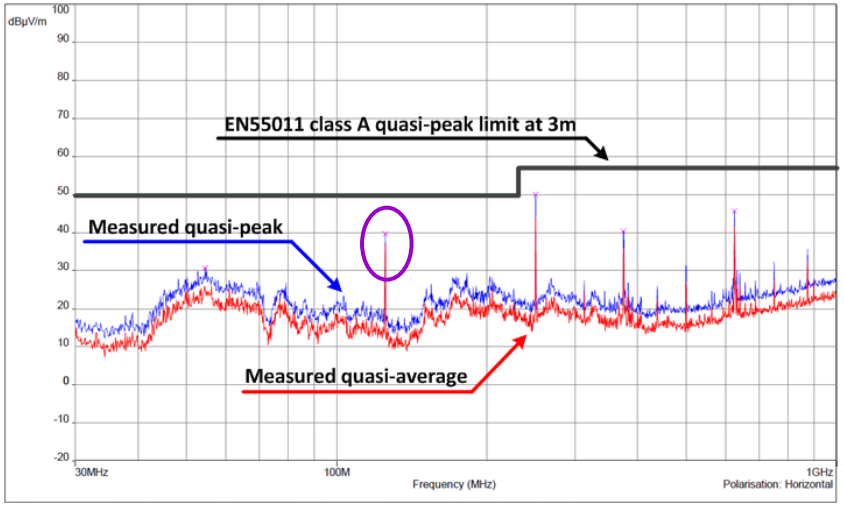
2 ports at the same time
Tested at 20% network utilization on each with UDP packet transfer



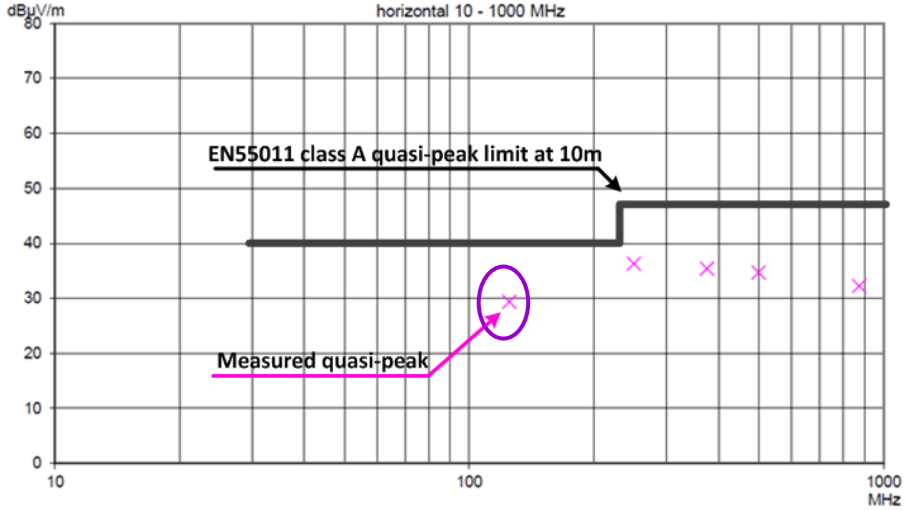
EN55011 / CISPR 11 EMI Test Results

Requirements			TIDA-00204 Measurements	
Phenomenon	**Basic Standard**	**Category 2 electric field strength component quasi-peak dB(uV/m)**	**Measured minimum margin to limit**	**Test**
EMI	EN55011/ CISPR 11 class A	40 (30-230MHz) 47 (230-1000MHz)	Horizontal: 10.6dB (125MHz) Vertical: 4.3 dB (125Mhz)	PASS

pre-test Horizontal polarization at 3m antenna distance

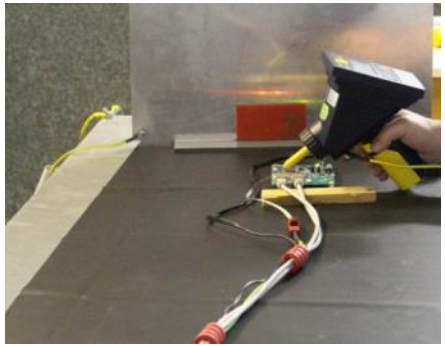


test Horizontal polarization at 10m antenna distance

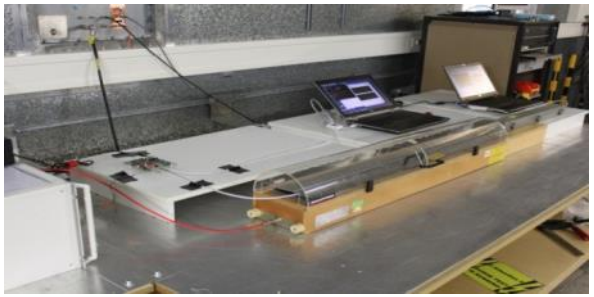


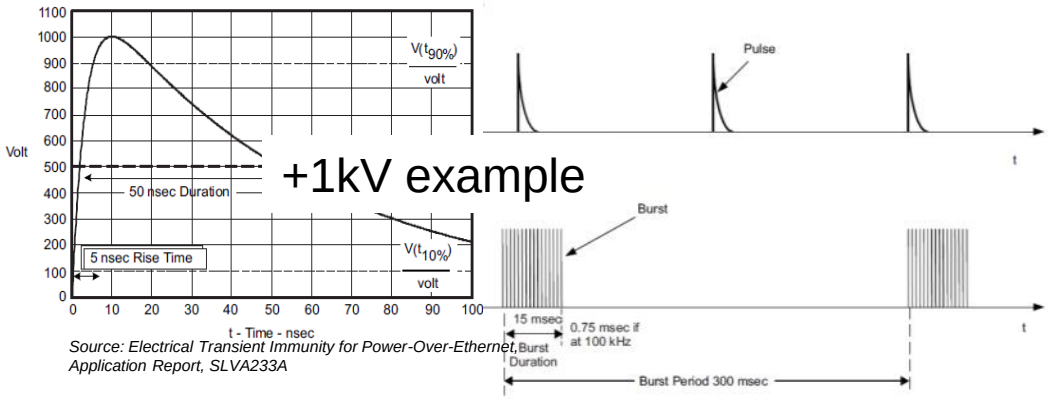
EMC Test Setup

IEC61000-4-2 ESD



IEC61000-4-4 EFT (fast transient burst)

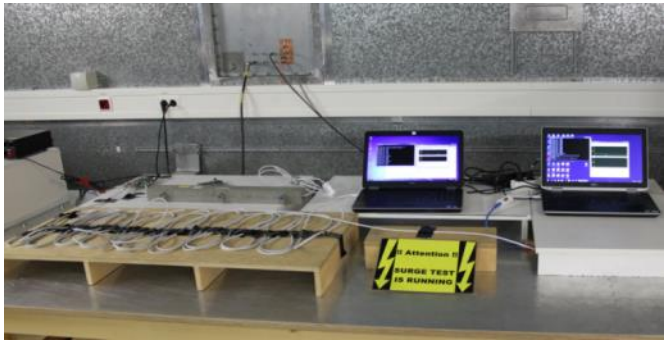


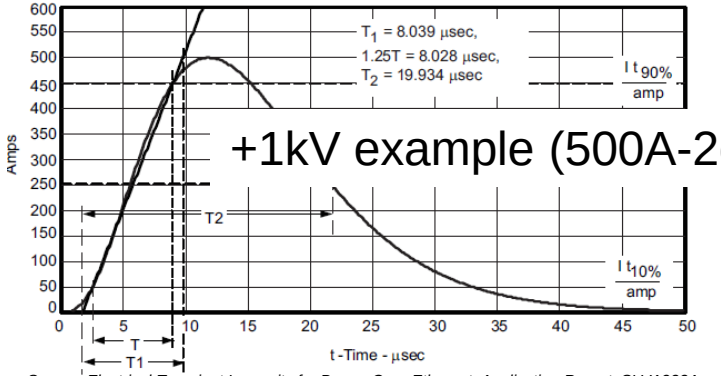


Source: Electrical Transient Immunity for Power-Over-Ethernet, Application Report, SLVA233A

EMC Test Setup

IEC61000-4-5 Surge





+1kV example (500A-2ohm)

Source: Electrical Transient Immunity for Power-Over-Ethernet, Application Report, SLVA233A

EMC Test Results

All immunity tests EXCEED the levels defined by the IEC standards.

IEC618000-3 and IEC61000-6-2 EMC immunity requirements

Requirements					**TIDA-00204 Measurements**		
Port	**Phenomenon**	**Basic standard**	**Level**	**Performance (acceptance) criterion**	**Level**	**Performance Criterion** (1)	**Test**
Enclosure ports	ESD	IEC61000-4-2	+/-4kV CD or 8kV AD, if CD not possible	B	**+/-6kV CD**	B	PASS (EXCEED)
Ports for control lines and DC auxiliary supplies <60V	Fast transient Burst (EFT)	IEC61000-4-4	+/-2kV/5kHz, capacitive clamp	B	**+/-4kV**	B	PASS (EXCEED)
	Surge 1,2/50us, 8/20us	IEC61000-4-5	+/-1kV. Since shielded cable >20m, direct coupling to shield (2Ohm/500A)	B	**+/-2kV**	B (2)	PASS (EXCEED)

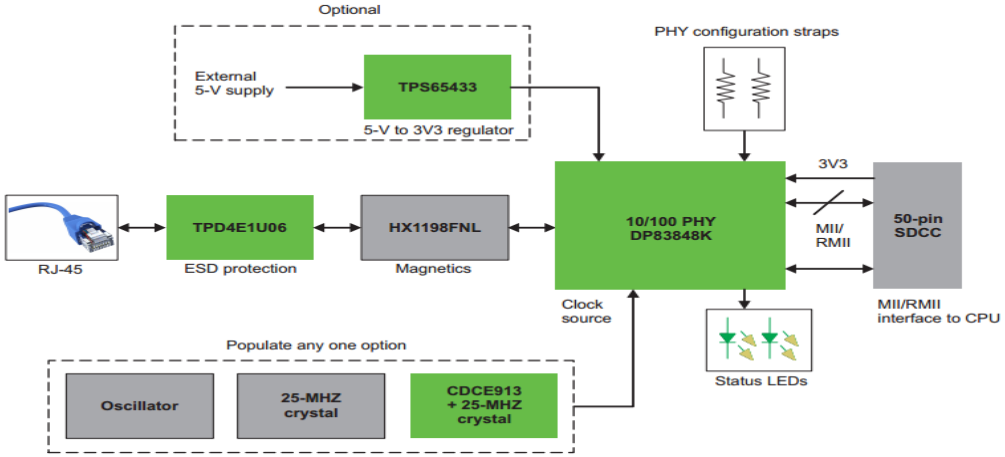
Performance Criterion

Performance (acceptance) criterion	**Description**
A	The module shall continue to operate as intended. No loss of function or performance even during the test. (1)
B	Temporary degradation of performance is accepted. After the test, the module shall continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module shall continue to operate as intended automatically, after manual restart, or power off, or power on.

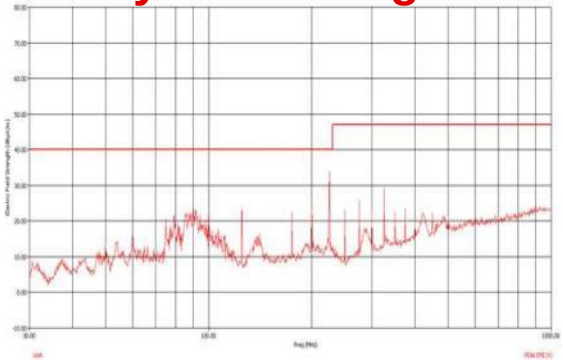
(2) Class A is considered when there are less than 2-consecutive UDP packet losses and no major drop in network utilization. One UDP packet loss will be tolerated by the system, if the following UDP packet is echoed back successfully. The test has been conducted w/ a UDP error packet test program at around 5% network bandwidth.

TI Designs – Ethernet Brick

EN55011 Compliant, Industrial Ethernet PHY Brick Reference Design



Passed the RE test (Class A) by ~6dB Margin

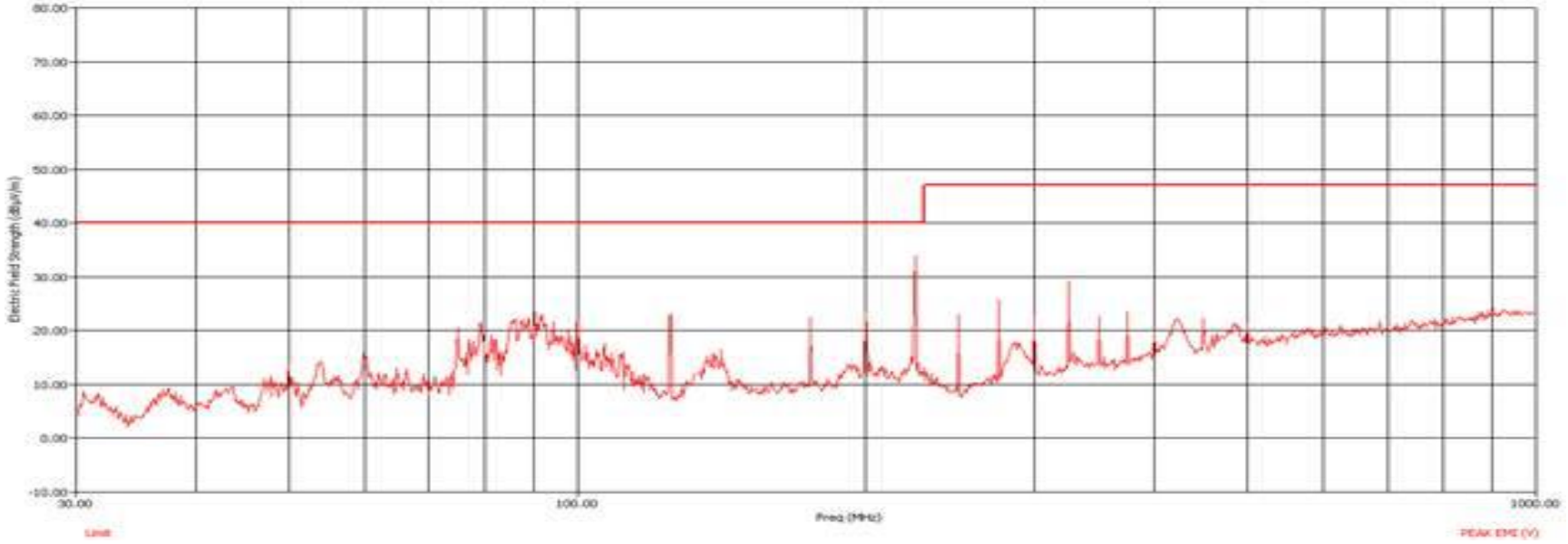


PEAKS - Vertical Polarization

DP83848 EMI Testing

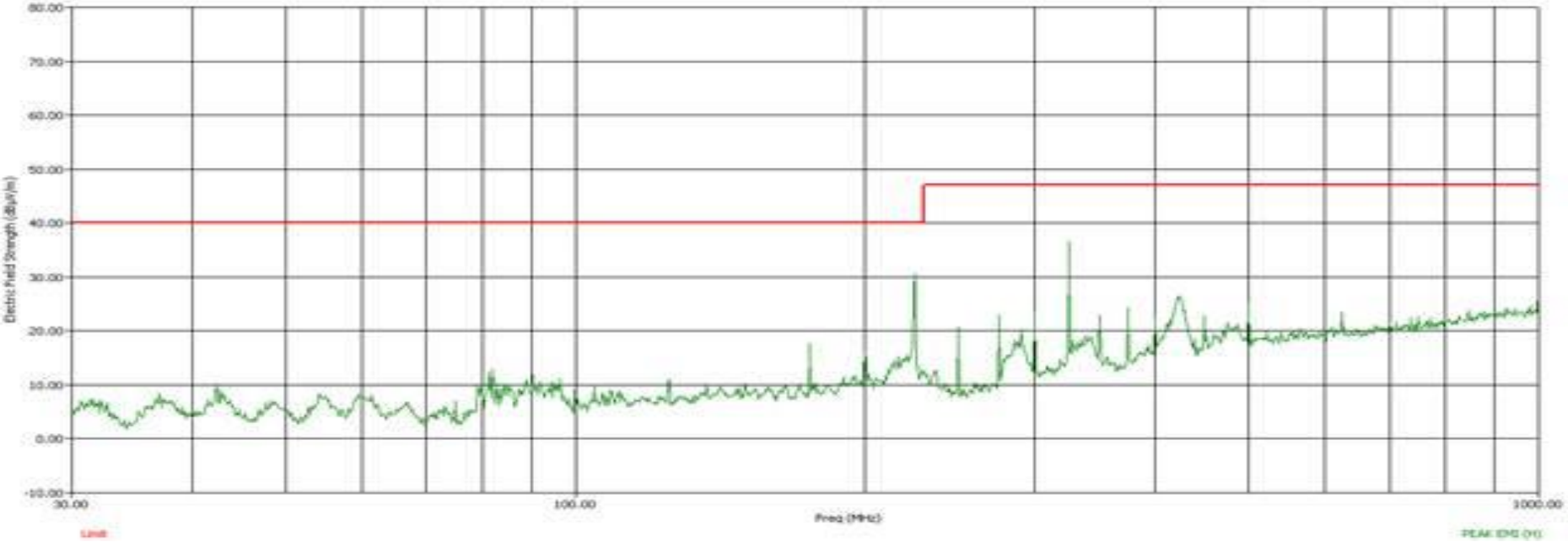
Passed the RE test (Class A) by ~6dB Margin

PEAKS - Vertical Polarization



DP83848 EMI (continued)

PEAKS - Horizontal Polarization



Key Learnings

- **Identify the Source, Path and Sink**
  - ESD
  - EMI
  - EMS
- **“Good” Layout Practices**
  - Decrease Loops
  - Board Zoning

Ethernet PHY Design & Layout Guidelines

Inductance Issues

- Close the loop FAST!
  - Return path is #1 priority
- Thick traces have minimal effect on inductance
- Loop diameter is key

$$L = N^2 \mu_0 D \left[\ln\left(\frac{8D}{d}\right) - 0.2 \right]$$

Example:

- #24 Gauge Wire, diameter 0.5105mm
- #18 Gauge Wire, diameter 1.0236mm
- Loop diameter @ 10mm and 20mm

Gauge Wire	10mm Loop	20mm Loop
#24 0.5105mm	19.2nH	47.1nH
#18 1.0236mm	14.8nH	38.4nH

Inductance Issues (2)

- Reframe from return path breaks
  - Return path should be directly below