TECH DAYS
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Industrial Ethernet Buses

Kevin Herring – TI Field Applications Engineer

Minneapolis Tech Day – October 24th 2017

Agenda

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- TI Ethernet Presence
- Ethernet Signaling Differences
- Key Features of Industrial Ethernet PHYs
- Review of Ethernet Industrial Buses

TI Ethernet Presence

Ethernet PHY Success in Industrial

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Factory Automation
PLCs, Motor Drives

- **Rugged and reliable**
- Meet stringent regulatory requirements for ESD & EMC w/o expensive externa components
- Improved **accuracy** down to **<10ns**

Smart Grid
E-meter Concentrators

- **Integrated ESD** protection >4kV
- Industrial temperature grade offering as well as p2p temp upgradable options allowing for **-40C to 105C and even 125C**

Other Industrial
IPNC, Power Relays

- **Low output power** including magnetics, 16% lower than KZ8051
- **Integrated ESD** protection >4kV
- Offered in p2p temperature options allowing -40 to **105 and even 125C**

Why This is Significant:

- Brand name providing tailored Ethernet PHYs for factory automation, motor drives, & power automation
- Our DP83848 is the industry's gold standard due to its robustness & high-reliability
- Easier to design-in and less external components
- Partnered with industry leaders to develop industry's first industrial grade gigabit ENET

History | Who are we?

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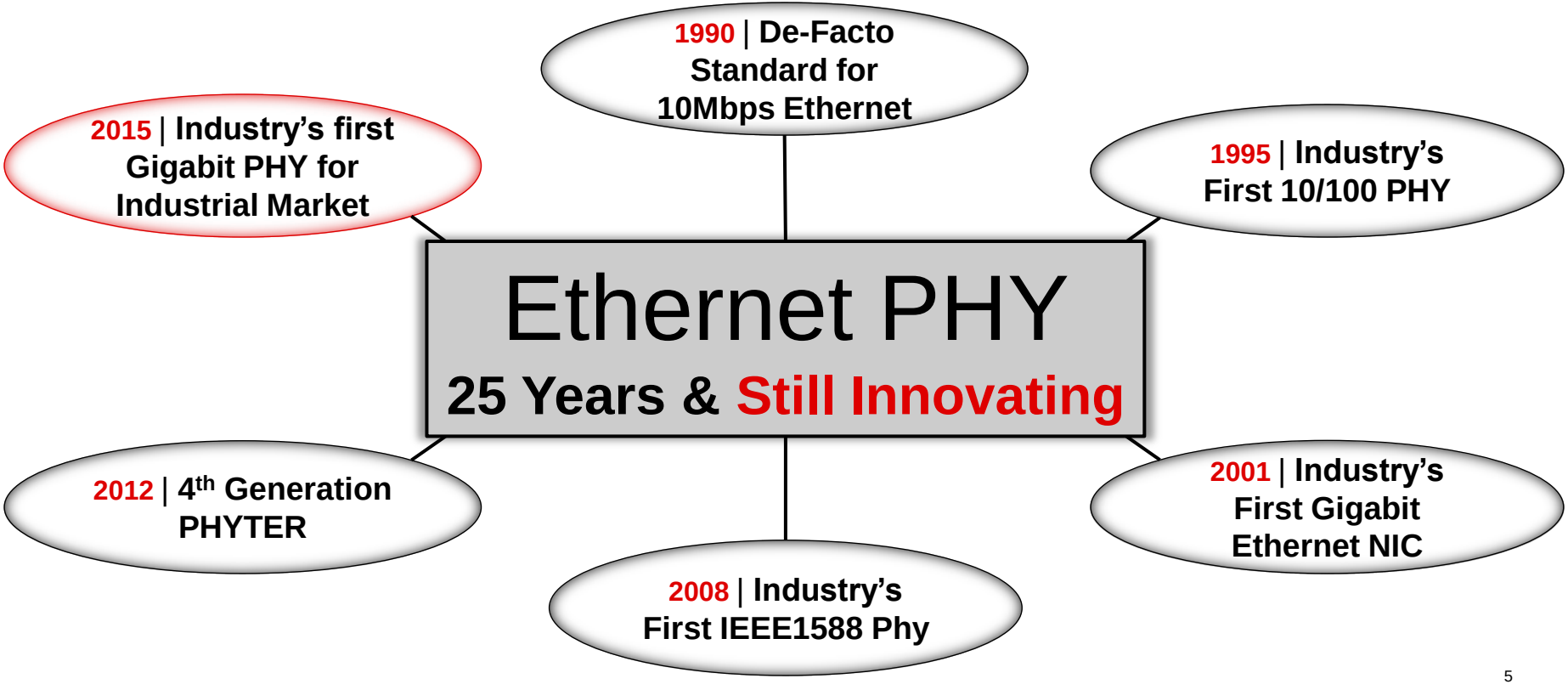
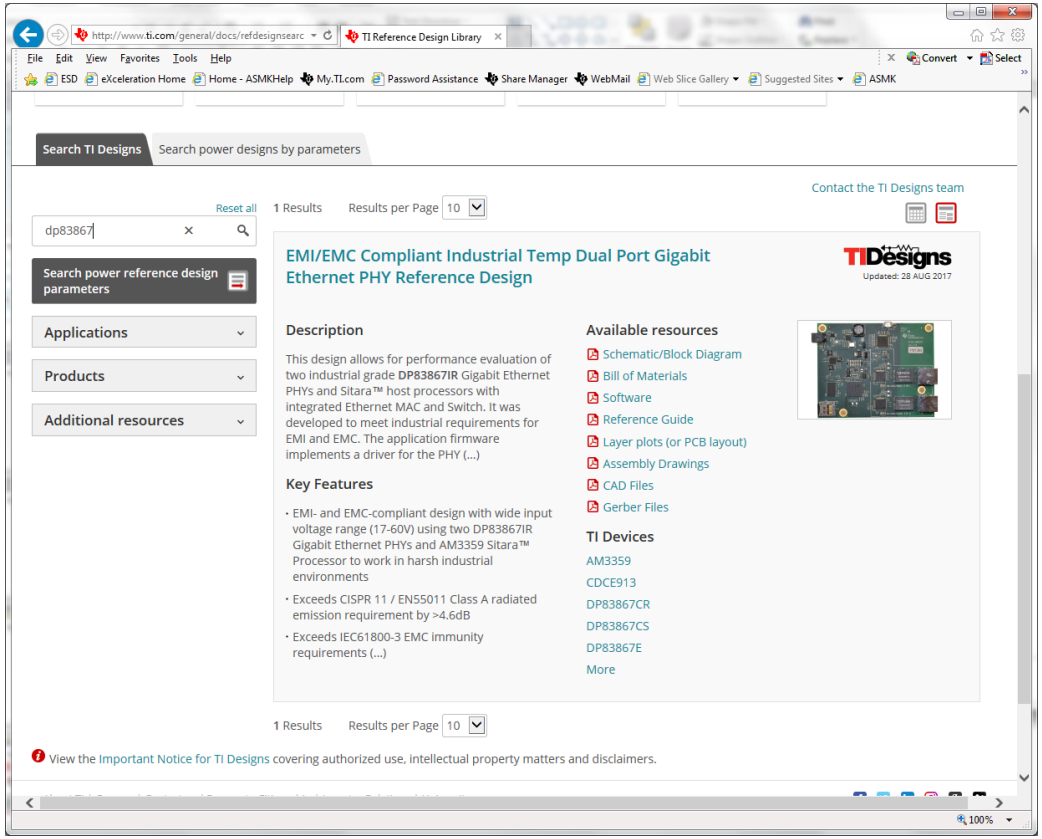


TI Phy Design Resources



TI Phys Tested and Certified by UNH

Gigabit Ethernet Consortium
Clause 40 PMA Conformance Test Suite v3.0 Report

UNH-IOL — 121 Technology Drive, Suite 2 — Durham, NH 03824 — +1-603-862-0090
Gigabit Ethernet Consortium — ethernet@iol.unh.edu — +1-603-862-0203

Patrick O'Farrell
Texas Instruments, Inc.

October 06, 2015
Report Rev. 1.0

Device Information	
Device Under Test (DUT)	Texas Instruments DP83867ERGZ
UNH-IOL Device Identification Number	21040
1000BASE-T PHY	
Manufacturer	Texas Instruments
Model	PDP83867E
Version	A96Y
Magnetics	
Manufacturer	Pulse
Model	HX5008FNL
Version	1451-PP

Agenda

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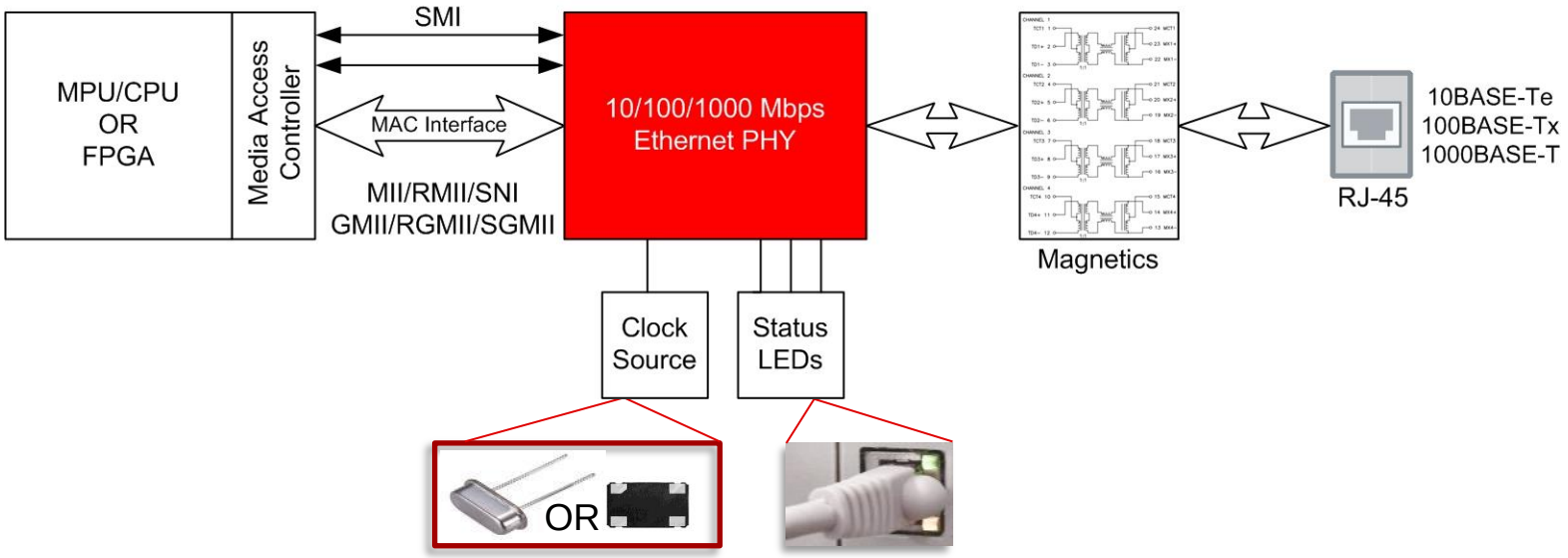
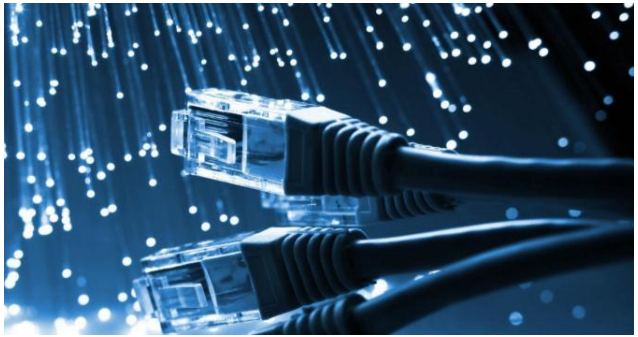
- TI Ethernet Presence
- **Ethernet Signaling Differences**
- Key Features of Industrial Ethernet PHYs
- Review of Ethernet Industrial Buses

Ethernet Typical Application Circuit



100Mb Ethernet Background

- 100Mb Ethernet was Introduced back in 1995!
- Handles definition of PCS, PMA and PMD for transferring data over copper cable or fiber optic cable at 100Mbps data rate
- Fast Ethernet is synonymous with 100BASE-TX
  - Technically also includes: 100BASE-T4, 100BASE-T2, 100BASE-FX, etc..
  - 100BASE-T encompasses the 100Mbps standards for twisted pair cabling
  - 100BASE-FX is concerned with 100Mbps over fiber optic cable rather than copper cabling
- 100BASE-X is commonly used when referring to specifications that concern both 100BASE-TX and 100BASE-FX



Common Terminology

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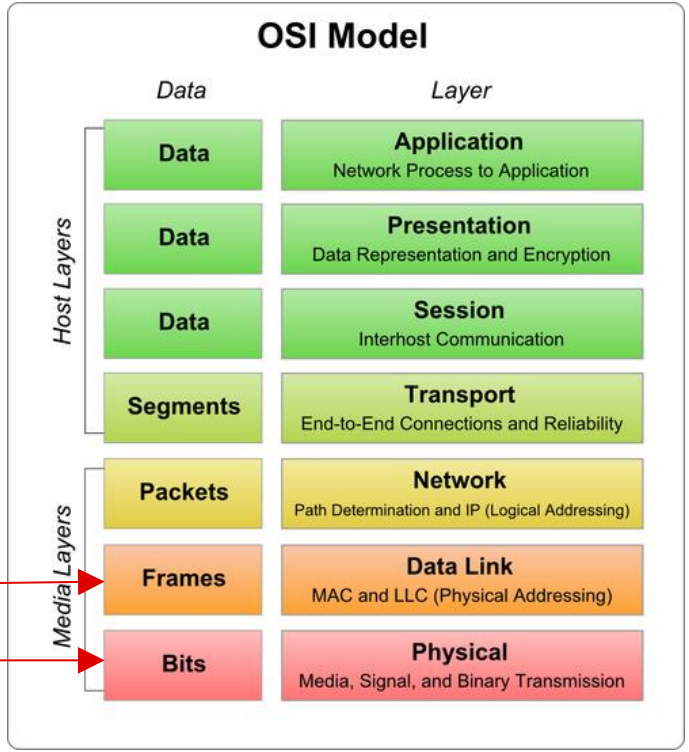
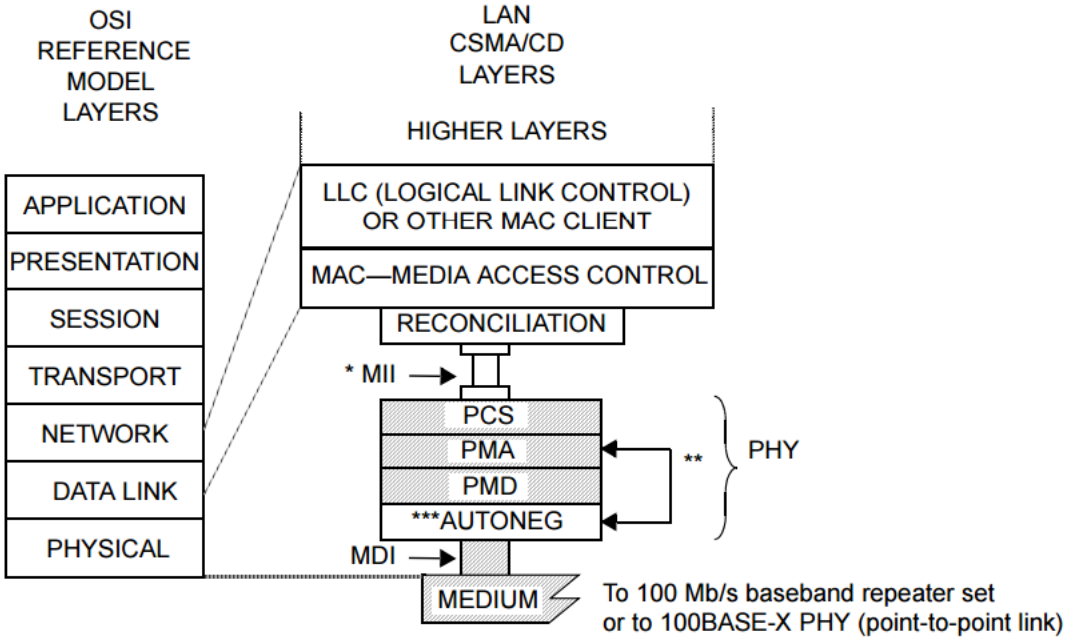
- PHY (Physical Layer Transceiver/Device) provides a way to transfer digital data from one node (processor, FPGA, ASIC…) to another node via analog signaling over either copper or fiber optic cable
- Three important processes a PHY handles:
  - PCS, Physical Coding Sublayer
  - PMA, Physical Medium Attachment
  - PMD, Physical Medium Dependent
- Other Key Terms:
  - MDI, Medium Dependent Interface (TD±/RD±)
  - MII, Media Independent Interface (Digital pins, TX_D[3:0]/RX[3:0] etc…)

Networking and Ethernet PHYs

- OSI Model describes the different layers of a networking system according to their functions
- Each layer communicates with layers above and below
- Information is passed via a Protocol Data Unit (PDU)
- Every layer will re-format and process the PDU before sending it over to the other layer.
- Ethernet MACs operate on Layer 2.
- Ethernet PHYs operate on Layer 1

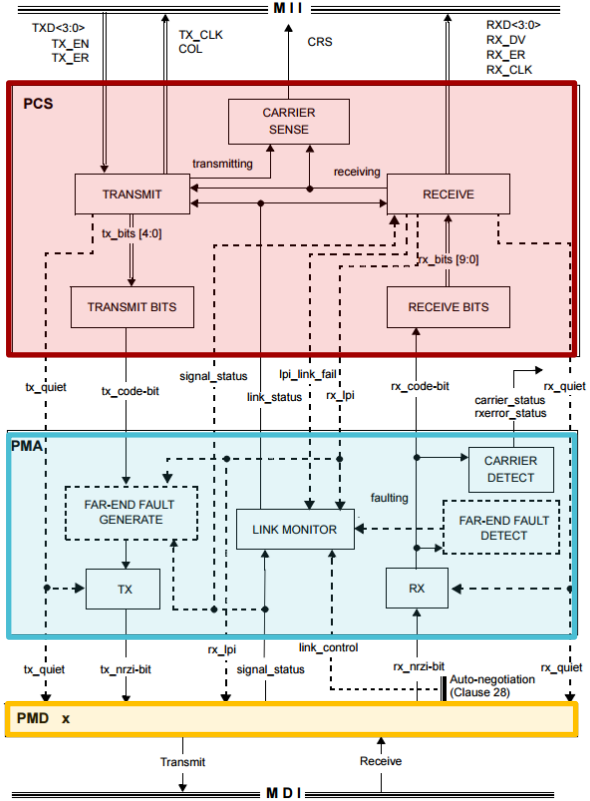


100BASE-X Reference Model



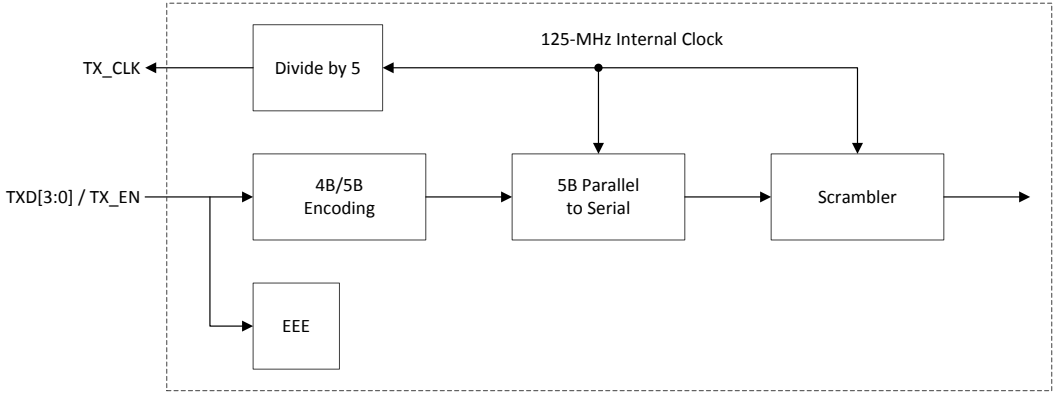
MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

Complex System within each PHY!



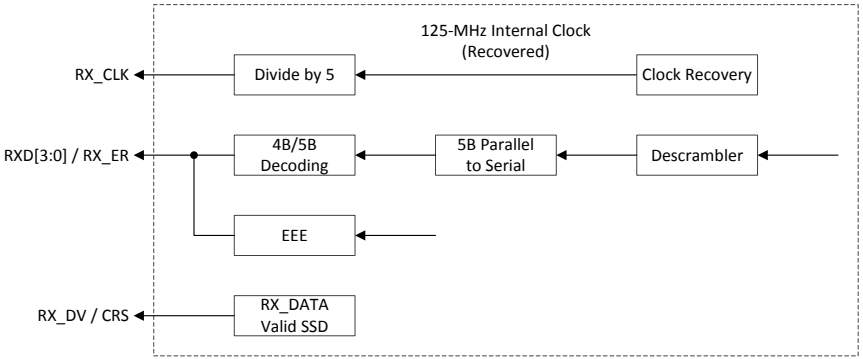
Physical Coding Sublayer (PCS)

- Provides a uniform interface to the Reconciliation sublayer for all 100BASE-T PHY implementations: 100BASE-X and 100BASE-T4
- PCS provides the following services (additional on next slide):
  - Encoding/Decoding of MII data nibbles to/from five-bit code groups (4B/5B)
  - Generating Carrier Sense and Collision Detect indications
    - Collision Detection is key for Half-Duplex configurations, which is not allowed Industrial Ethernet



Physical Coding Sublayer (PCS)

- PCS provides the following services (continued from previous slide):
  - Serialization/Deserialization of code groups for transmission/reception
  - Mapping of Transmit, Receive, Carrier Sense and Collision Detection between MII and underlying PMA
  - (Optional) Also, interpreting and generating MII data signals to enable or disable the LPI mode for Energy Efficient Ethernet (EEE) applications
    - EEE is generally not supported by Industrial Ethernet

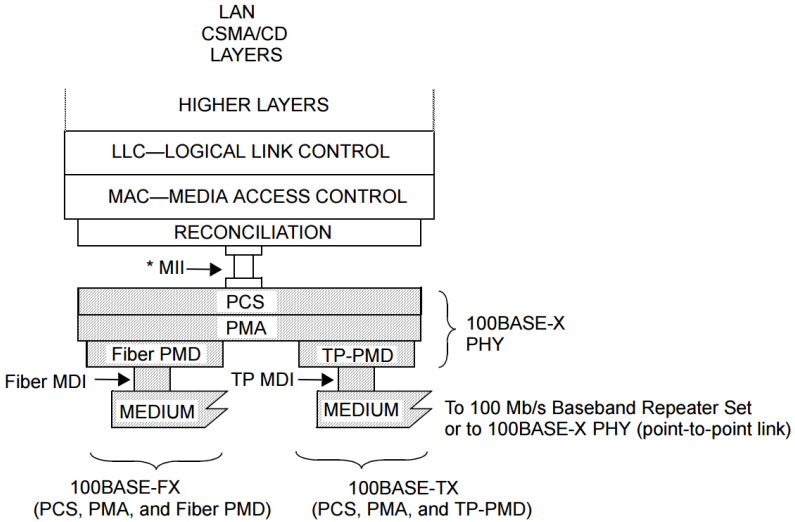


Physical Medium Attachment (PMA) sublayer

- PMA provides medium-independent means for the PCS to support the use of a range of physical media
- PMA provides the following services:
  - Mapping of transmit and receive code-bits between PMA's client and underlying PMD
  - Generating a control signal indicating the availability of the PMD to the PCS or other client, also synchronizing with Auto-Negotiation when implemented
  - (Optional) Generating indications of activity and carrier errors from underlying PMD
  - (Optional) Sensing receive channel failures and transmitting the Far-End Fault Indication, detecting the Far-End Fault Indication
  - (Optional) Receiving and processing LPI control signals from the PCS
  - Recovery of clock from the NRZI data supplied by the PMD

Physical Medium Dependent (PMD) sublayer

- 100BASE-X uses FDDI signaling standards:
  - ISO/IEC 9314-3:1990
  - ANSI X3.263-1995 (TP-PMD)
  - 125Mb/s over either fiber optic cable or twisted-pair copper cable



Ethernet Signals on the Cable Media

10BASE-T Transmission

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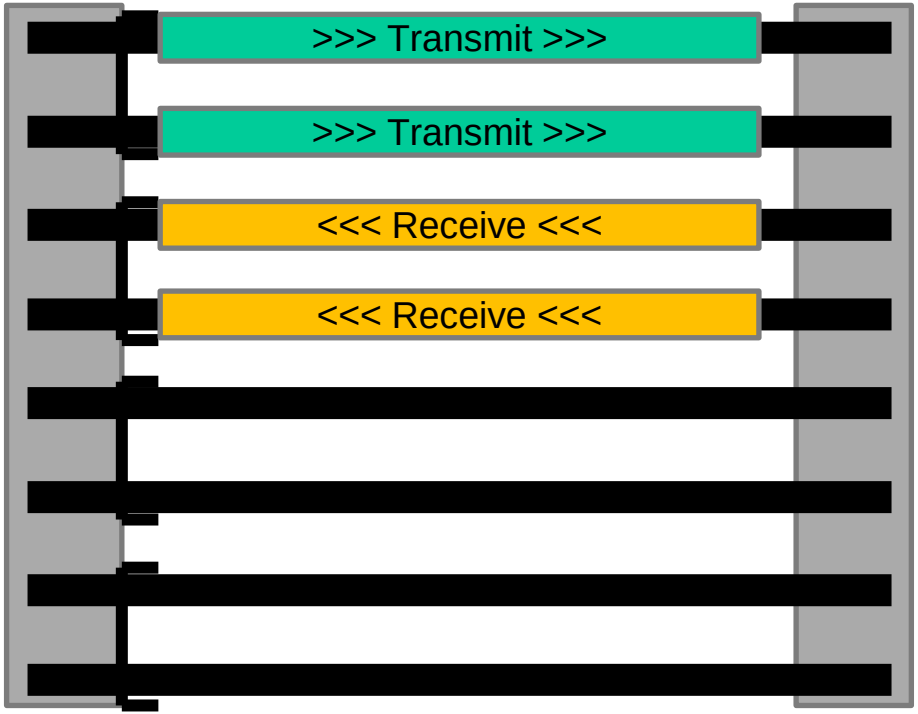
Coding

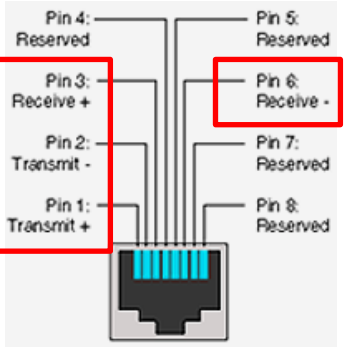
+1

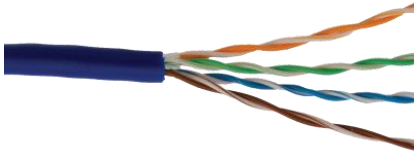
0

Manchester

UTP Category 5 Cabling Utilization



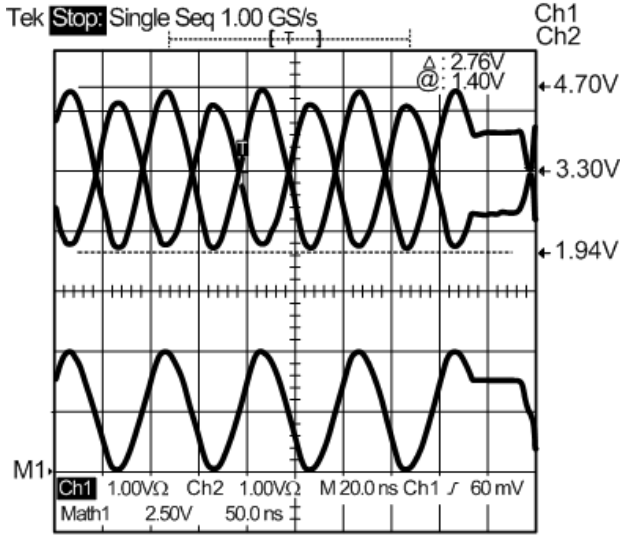




10Base-T Overview

10 Mb/s has the following characteristics:

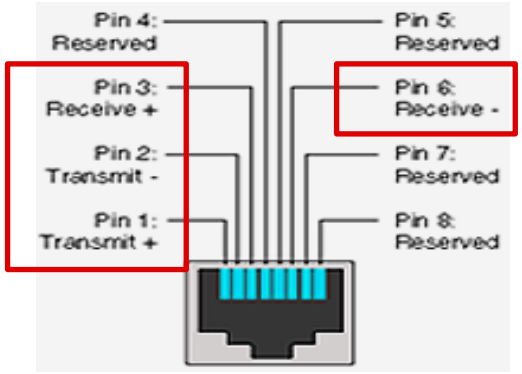
- Data rate: 10 Mb/s
- Signaling: 10 MHz, Differential, Manchester
- Return Loss: >15.0dB @5 – 10 MHz
- Encoding: Manchester
- Maximum Required Cable Length (per IEEE standard): 100m
- Cabling: CAT-5 twisted pair, 100 Ohm
- Wires used: 2 pair
- Specification: IEEE 802.3
- Bit error rate: 1 error in 10e8 bits

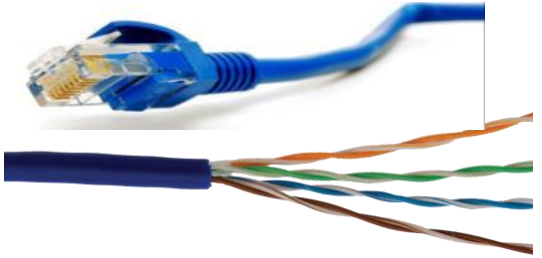


100BASE-TX Signal Transmission

Coding
-1
0
+1

3-Level MLT





100BASE-TX Signal Overview

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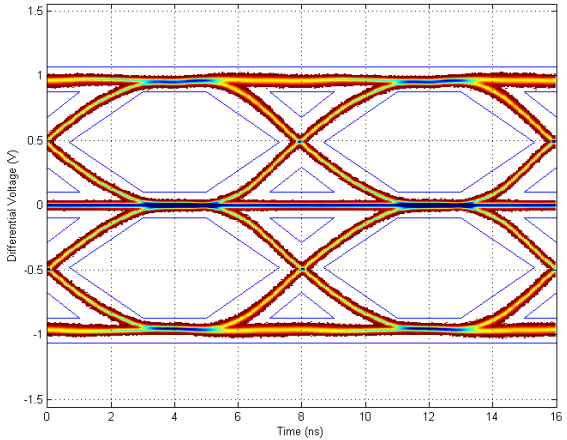
100 Mb/s or Fast Ethernet has the following characteristics:

- Data rate: 100 Mb/s
- Signaling: 125 MHz, Differential, MLT-3 (3 level Multi Level Transitions)
- Return Loss: 16.0dB @2 - 30 MHz, 10.0dB @60 - 80 MHz
- Encoding: 4b5b (4 bits of data for 5 bits transferred)
- Max Cable Length (per IEEE standard): 100m
- Cabling: CAT-5 twisted pair, 100 Ohm
- Wires used: 2 pair
- Specification: IEEE 802.3u
- Bit error rate: 1 error in 10e8 bits

Figure 1: MLT-3 Eye Diagram (Informative)



DP83822 – TI's Latest 10/100Mbps PHY

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Highlights

- **Industry's Lowest Power 10/100Mbps PHY**
  - 1.8V operation <110mW
- Small package **QFN32** (5mmx5mm)
- Long cable reach >150m
- **100BASE-TX, 100BASE-FX** and **10BASE-Te**

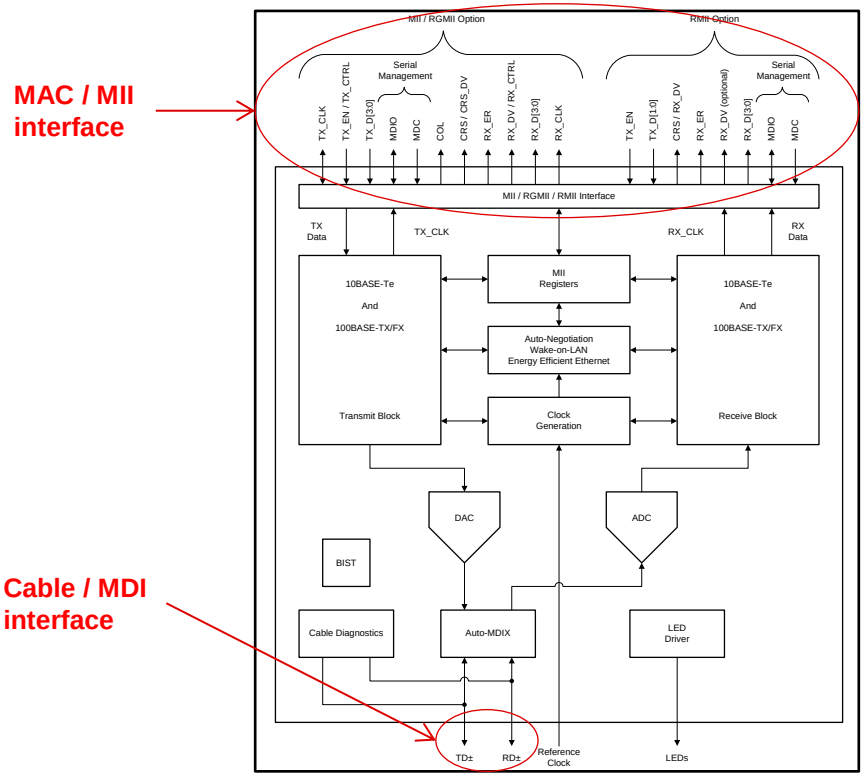
Key Specs

- MII / RMII / RGMII MAC Interfaces
- HBM (**+/-16kV**), IEC61000-4-2 (**+/-8kV**)
- **Start of Frame Detection for IEEE1588**
- Industrial Temperature Range **-40C to 85C/125C**

Applications

- Factory Automation, Motor Drives, Power Automation, Industrial Lighting

DP83822 Block Diagram



1000-BASE-T Transmission

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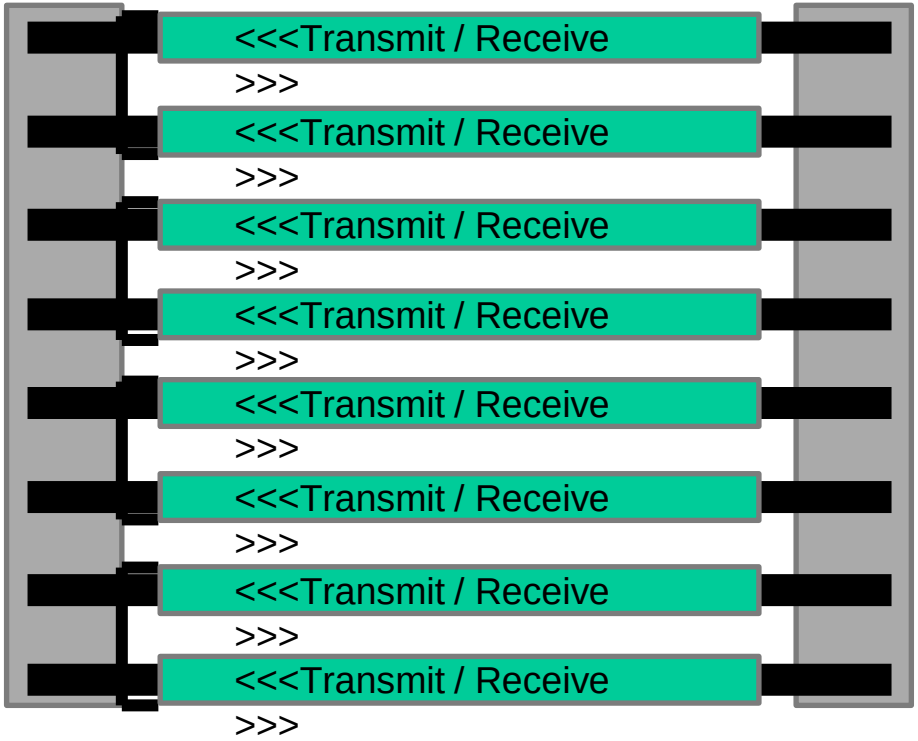
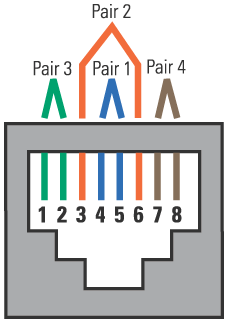
Coding

+2
+1
0
-1
-2

5-Level
PAM-5

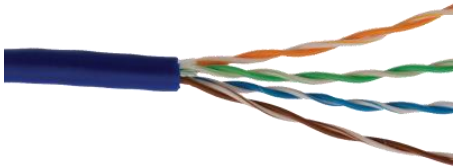
UTP Category 5 Cabling Utilization





Pair ID	PIN #
T1	5
R1	4
T2	3
R2	6
T3	1
R3	2
T4	7
R4	8

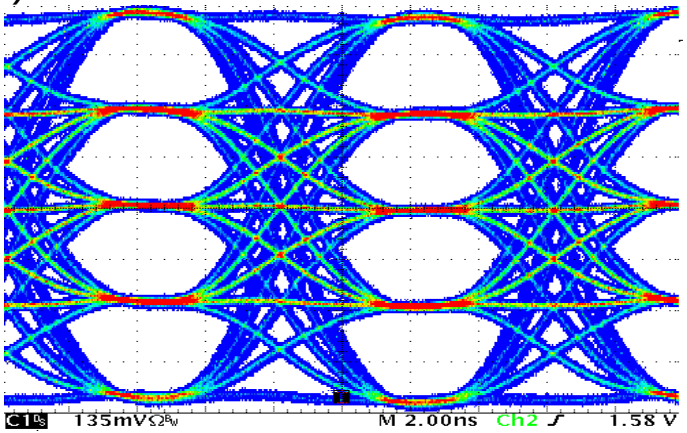
T568A



Ethernet Signaling – 1000BASE-T

1000 Mb/s or Gigabit Ethernet has the following characteristics:

- Data rate: 1000 Mb/s
- Signaling: 125 MHz, Differential, PAM-5 (Pulse Amplitude Modulation)
- Return Loss: 19.0dB @1 - 100 MHz (~100m)
- Encoding: 8b10b (8 bits of data for 10 bits transferred)
- Maximum Required Cable Length (per IEEE standard): 100m
- Cabling: CAT-5 twisted pair, 100 Ohm
- Wires used: 4 pair (each Full Duplex)
- Specification: IEEE 802.3
- Bit error rate: 1 error in 10e10 bits



DP83867 – TI's Latest 1Gb Phy

10/100/1000 Low Power and Robust Ethernet PHY

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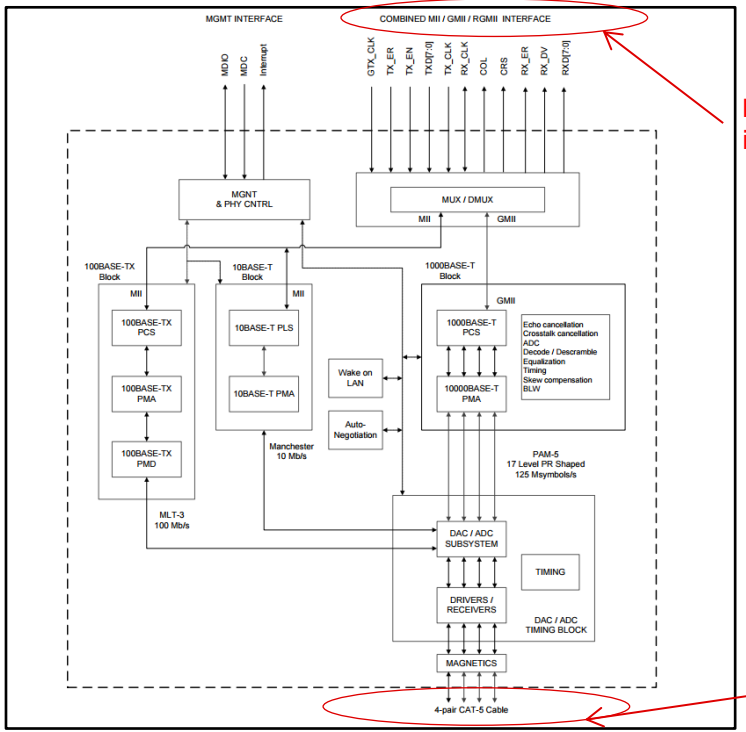
- **Highlights**
  - **IEC 12kV specification!**
  - Lowest latency for both 100Mbps and 1Gbps modes, <400ns
  - Power saving features: WoL
  - **Pass EN55011 class B**
  - **Low power 1GbE solution, <400mW**

- **Key Specifications**
  - GMII/RGMII/MII/SGMII
  - **Start of Frame Detect for IEEE 1588 time stamp**
  - JTAG (IEEE 1149.1)
  - 25MHz or 125MHz Output clock
  - Pin to pin temperature grades (0 to 70C) through **(-40C to 105C)**
  - **QFN48** or QFP64

- **Applications**
  - Industrial: Automation, Test Equipment, Sensors
  - Communications: Debug /Management Port, Small Cell
  - Commercial: Network Printers, Broadband gateways

Gigabit PHY (DP83867) Block Diagram



Where to look for more information?

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- 100BASE-X PCS and PMA specifications located in Clause 24 of the IEEE802.3 Standard (Section Two)
- 100BASE-TX PMD specifications located in Clause 25 of the IEEE802.3 Standard (Section Two)
- 100BASE-FX PMD specifications located in Clause 26 of the IEEE802.3 Standard (Section Two)

Agenda

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- Ethernet Signaling Differences
- **Key Features of Industrial Ethernet PHYs**
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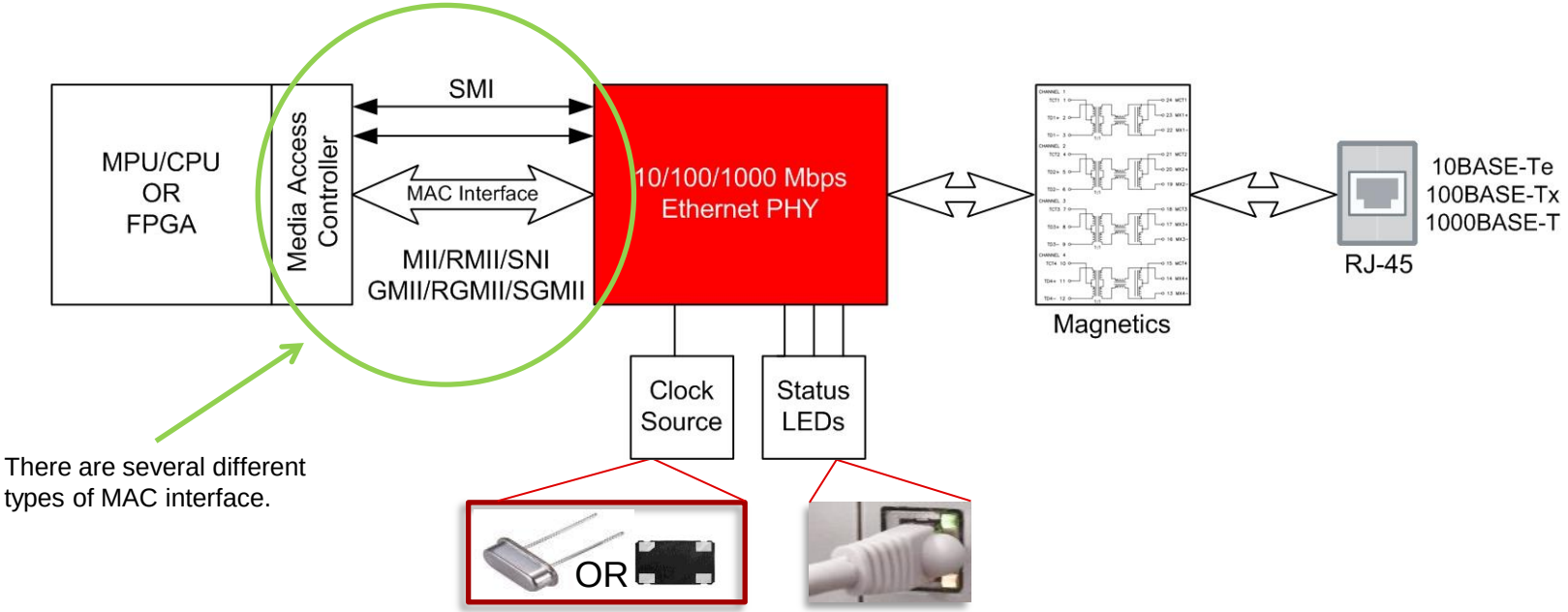
Key Requirements for Industrial Ethernet

Ethernet Typical Application Circuit



MAC Interfaces Types - 10Mb / 100Mb

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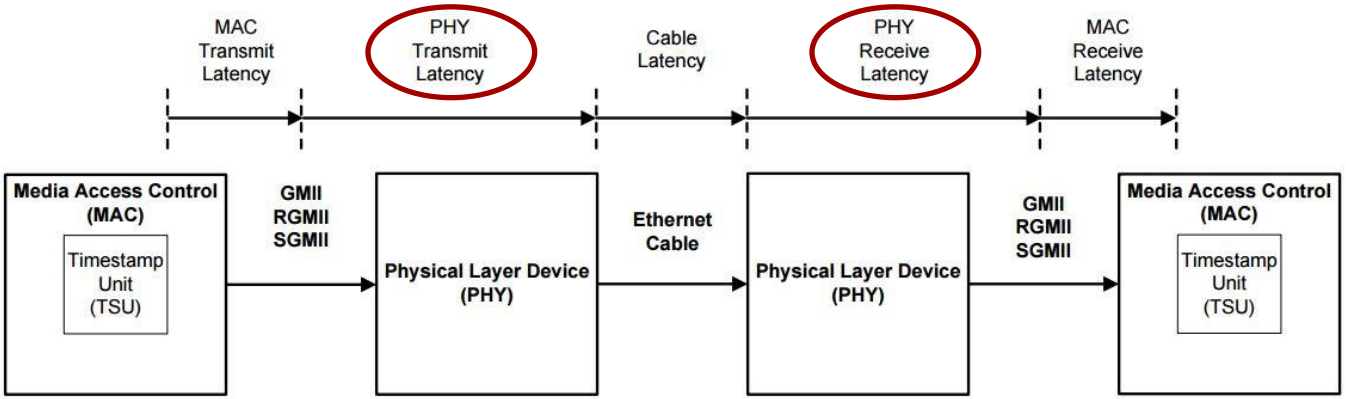
Interface Details	MII	RMII	SNI
Full Name	Media Independent Interface	Reduced-Media Independent Interface	Serial Network Interface
Pin Count	15	9	7
Clock Speed	25MHz – 100Mbps 2.5MHz – 10Mbps	50MHz – 10Mbps and 100Mbps	10MHz – 10Mbps
Transmit Pins	TX_D[3:0], TX_EN, TX_CLK	TX_D[1:0], TX_EN	TX_D[0], TX_EN, TX_CLK
Receive Pins	RX_D[3:0], RX_DV, RX_ER, COL, CRS, RX_CLK	RX_D[1:0], CRS_DV	RX_D[0], CRS, COL, RX_CLK

MAC Interfaces Types – 10Mb / 100Mb / 1Gb

Interface Details	GMII	RGMII	SGMII
Full Name	Gigabit Media Independent Interface	Reduced-Gigabit Media Independent Interface	Serial Gigabit Media Independent Interface
Pin Count	24	12	4
Clock Speed	125MHz – 1Gbps	125MHz – 1Gbps DDR	625MHz – 1.25Gbaud data, DDR
Transmit Pins	TX_D[7:0], TX_EN, TX_CLK, GTX_CLK, TX_ER	TX_D[3:0], TX_CTRL, TX_CLK	TX_P, TX_N (Optional) TX_CLKP, TX_CLKN
Receive Pins	RX_D[7:0], RX_DV, RX_ER, COL, CRS, RX_CLK	RX_D[3:0], RX_CTRL, RX_CLK	RX_P, RX_N (Optional) RX_CLKP, RX_CLKN

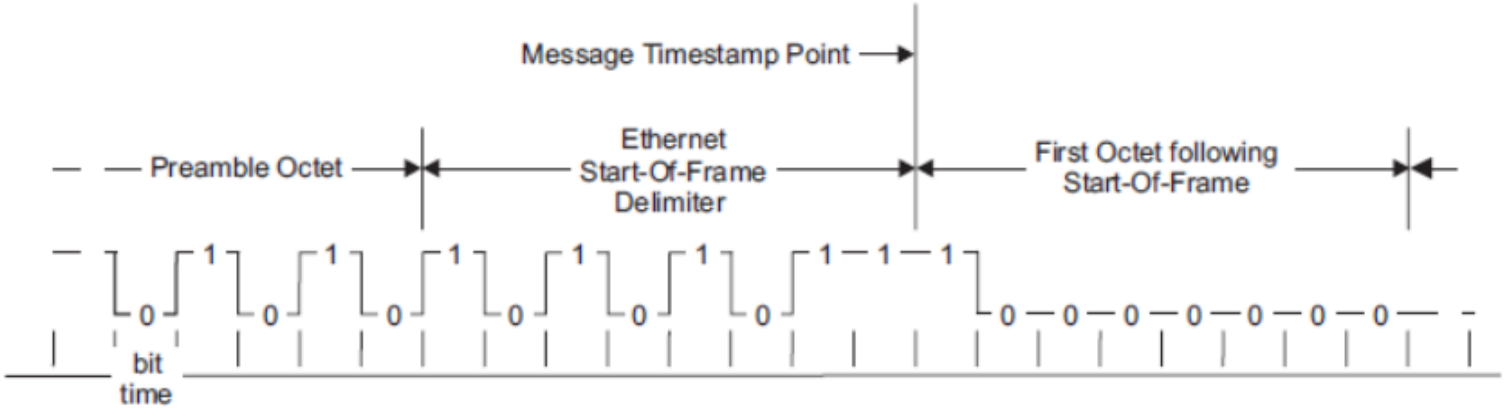
Latency

- Latency is the time taken by the packet to travel from source to destination.
- If latency is constant across packets, it is said to be deterministic.
- It is desired that Latency should be Low and Deterministic.
- Latency of concern are:
  - PHY Transmit Latency
  - PHY Receive Latency
- More information can be found in the Application Note: '[Latency in Factory Automation]'



Start of Frame Delimiter (SFD)

- Ethernet frame is preceded by preamble and Start of Frame Delimiter.
- SFD detect can be routed to GPIO pins of the PHY.
- TX SFD and RX SFD can be used to calculate PHY Latencies.
- SFD can also be used for time stamping and for IEEE 1588
- More information can be found in the Application Note: 'How to Configure DP83867 SFDs'



Power

- Power consumption is usually calculated as a product of current consumed by the PHY and the operating voltages.
- Power consumption is affected by the operating conditions;
  - Operational Mode: 10M 100M or 1000M
  - I/O Pin Loading: VDDIO voltage and load conditions of the IO pins
  - Channel Utilization: Higher percentage of channel utilization leads to higher power consumption
  - Payload: Size of data packet along with utilization also affect power
  - Temperature: Higher operating temperature leads to increase in power consumption
- More information can be found in the Application Note: 'DP83867 Power Consumption Data'

Electrostatic Discharge (ESD)

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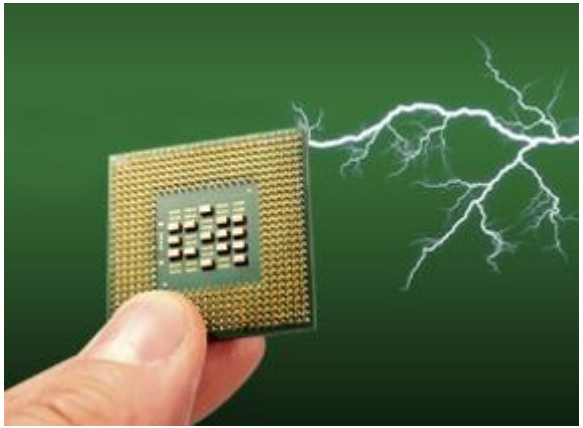
- ESD events occur when electricity suddenly flows between two electrically charged objects
- ESD events can permanently damage devices
- Not all ESD events show visible signs of damage
- 2 Types of ESD Testing
  - Device Level ESD: Tested Directly on the IC pins.

  For E.g.: Human Body Model (HBM), Charge Device Model (CDM), Machine Model (MM)
  - System Level ESD: Tested on the entire system

  For E.g.: IEC 61000-4-2 ESD test specifications



ESD Things to Know

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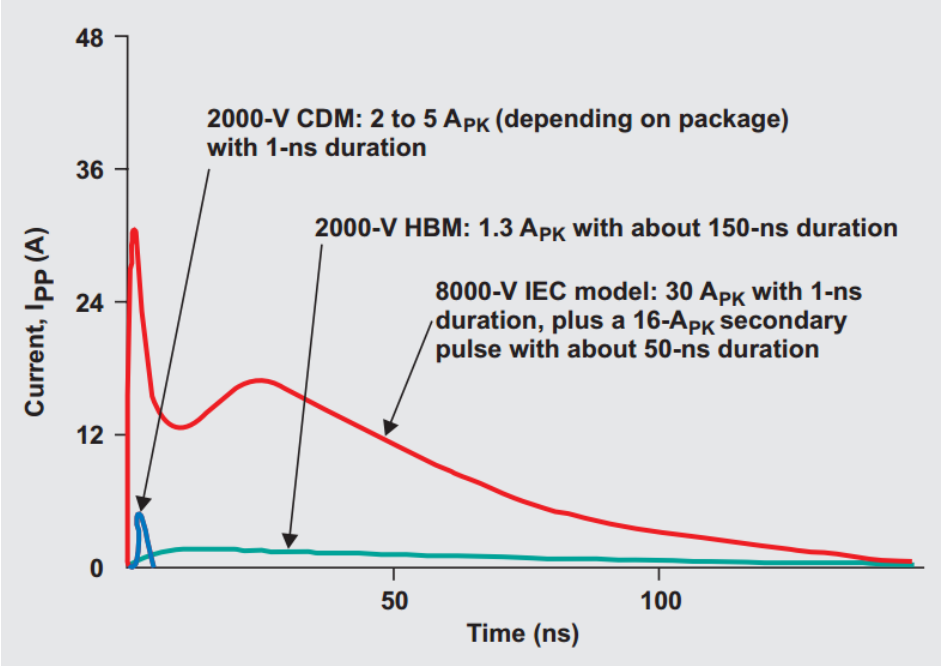
- Device Level
  - HBM
  - MM
  - CDM

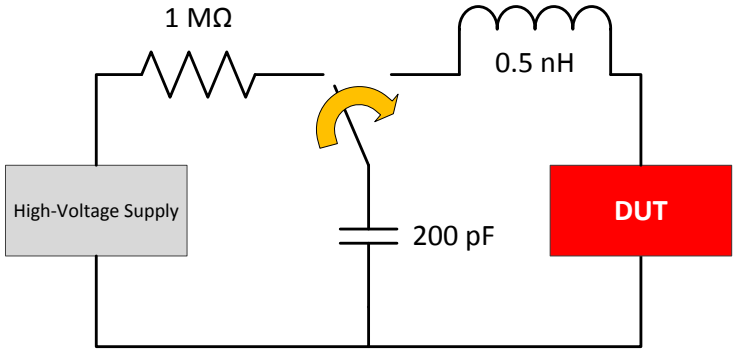
	HBM	MM	CDM	IEC 61000-4-2
Definition	Human body discharging accumulated static	Robotic arm discharging accumulated static	Charged device being grounded	Real-world ESD events
Test Levels (V)	500 – 2000	100 – 200	250 – 2000	2000 – 15000
Pulse Width (ns)	~ 150	~ 80	~ 1	~ 150
Peak Current at Applied 2kV (A_{PK})	1.33	-	~ 5	7.5
Rise Time	25 ns	-	< 400 ps	< 1 ns
Number of Voltage Strikes	2	2	2	20

- System Level
  - IEC 61000-4-2
  - Contact vs Air-Gap Discharge

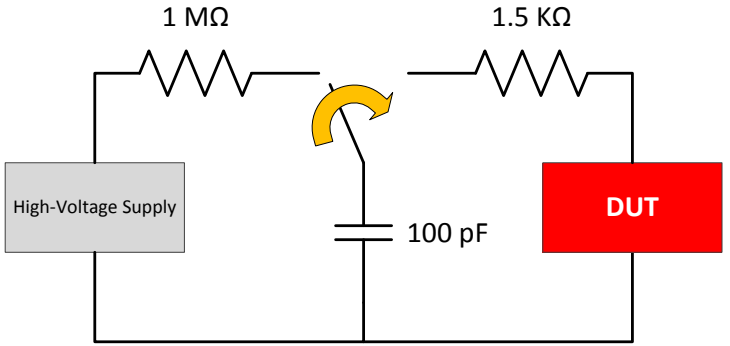
ESD Things to Know (2)



MM Test Setup

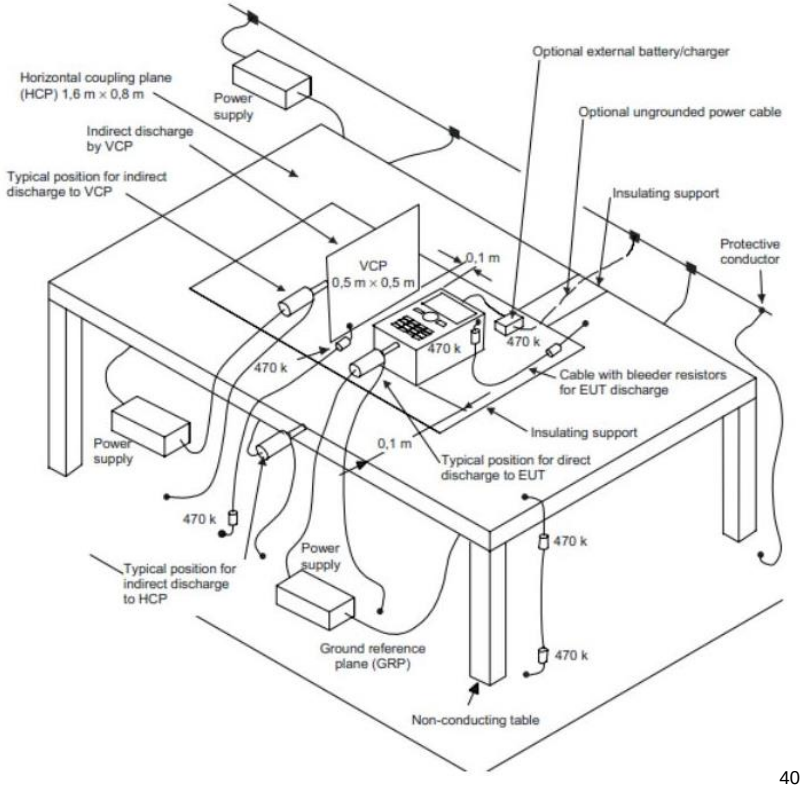


HBM Test Setup



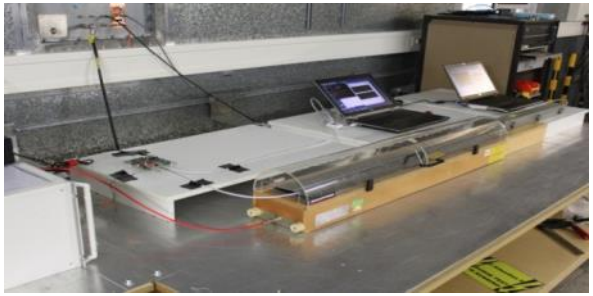
IEC 61000-4-2 ESD Test Bench

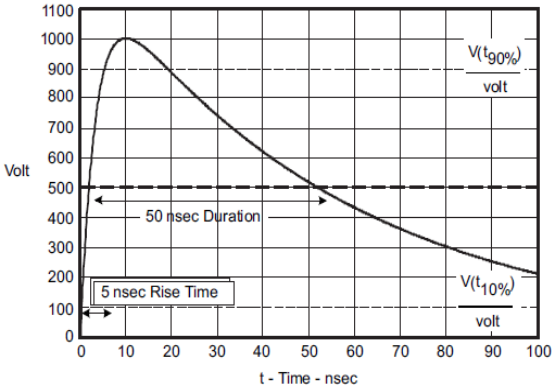
- Industrial applications usually require 6kV or higher ESD testing.
- Different levels of passing criteria
  - Class A: No effect on performance
  - Class B: Some effect but device self-recovers
  - Class C: Some effect, user intervention required
  - Class D: Device damaged
- Passing criteria differs as per customer requirement.
- Contact Discharge and Air Discharge are two methods of testing.

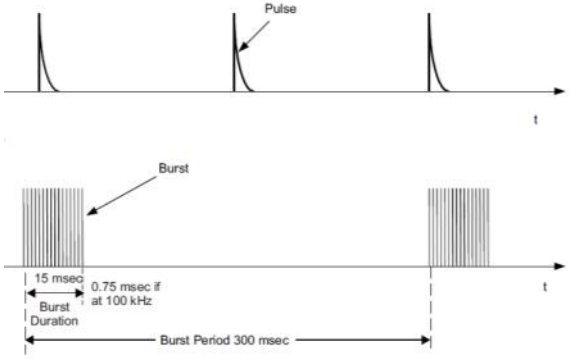


IEC 61000-4-4 EFT Test Bench

- Simulates transient noise on lines from inductive loads and switching
- In case of Ethernet, these transients can couple to signal lines
- Industrial applications can require 2kV or higher EFT testing on signal ports
- Different levels of performance criteria
  - Class A: No effect on performance
  - Class B: Some effect but device self-recovers
  - Class C: Some effect, user intervention required
  - Class D: Device damaged
- Passing criteria and levels differs as per customer requirement

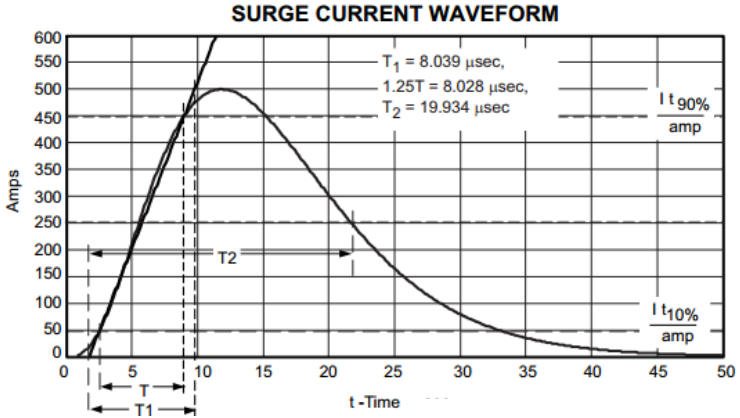


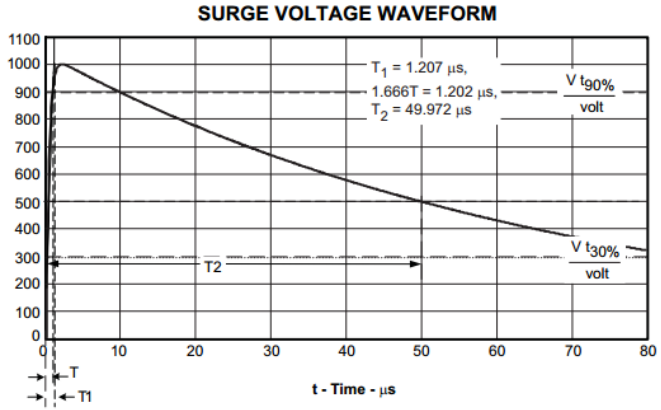




IEC 61000-4-5 Surge

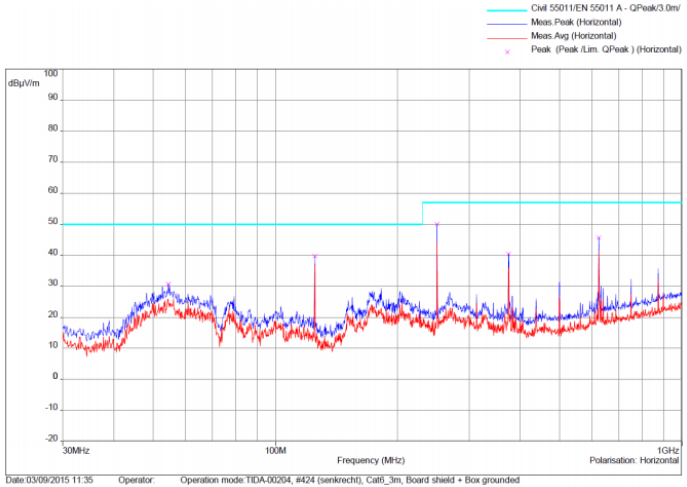
- Simulates extremely high energy events like direct/indirect lightning strikes and main power events
- Deployment of system dictates required surge rating
- Up to 2kV in deployments where cables are outdoors
  - IEEE 802.3 requires only 1.5kV isolation to ground making 2kV difficult
- Different levels of performance criteria
  - Class A: No effect on performance
  - Class B: Some effect but device self-recovers
  - Class C: Some effect, user intervention required
  - Class D: Device

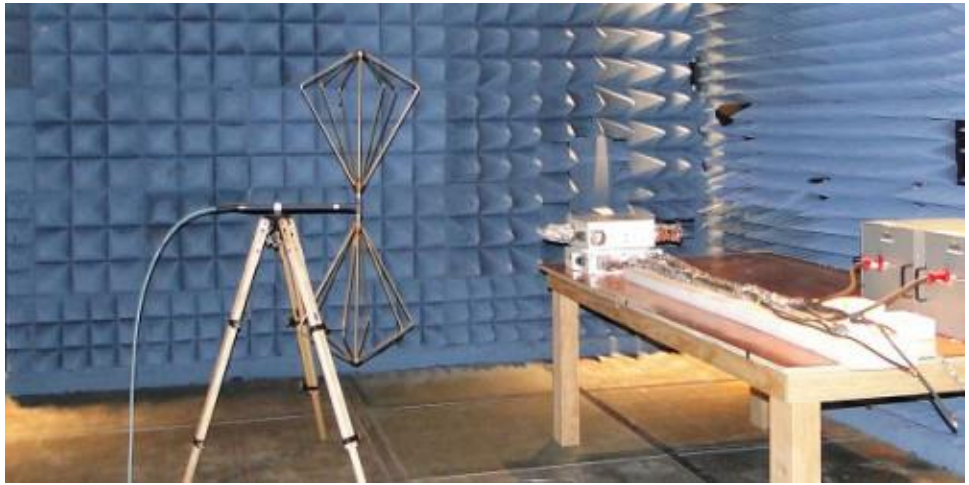




EN55011(22) Emissions

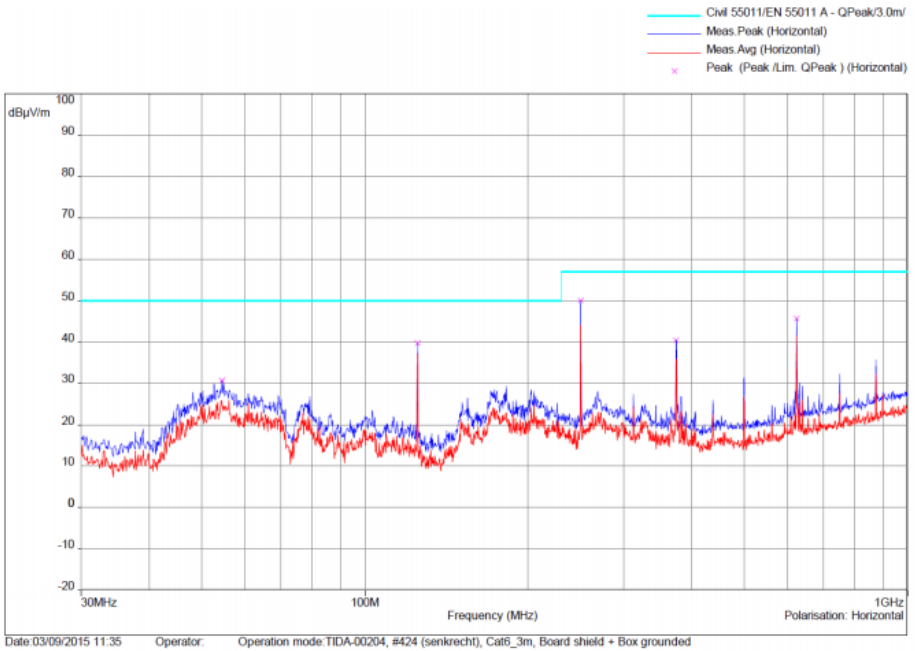
- Unintentional emissions generated by the system can cause disturbance in other systems by electromagnetic induction or coupling
- EMI testing of a system is done by two methods
  - Radiated Emissions
  - Conducted Emissions





ElectroMagnetic Inteference(EMI)

- Standards define the test setup and the distance between Equipment Under Test (EUT) and the antenna
- The limits are also defined by the standards and the radiations from EUT need to be below those limits to qualify for a pass.
- Example Standards;
  - IEC 61000-4-x
  - CISPR-xx
  - EN550xx
- Different applications require different standards.
- Within the same standards, there are different classes and levels of testing.



- For more information refer to EMI-EMC test report for TIDA-00204

Agenda

TECH DAYS
Texas Instruments

- TI Ethernet Presence
- Ethernet Signaling Differences
- Key Features of Industrial Ethernet PHYs
- **Review of Ethernet Industrial Buses**

Industrial Ethernet
Fieldbuses

Industrial Ethernet Fieldbus Protocols

- EtherCAT
- PROFINET
  - PROFINET IO / IRT
- SERCOS III
- EtherNET/IP
- VARAN
- Ethernet POWERLINK
- Modbus TCP/IP

Key PHY requirements…

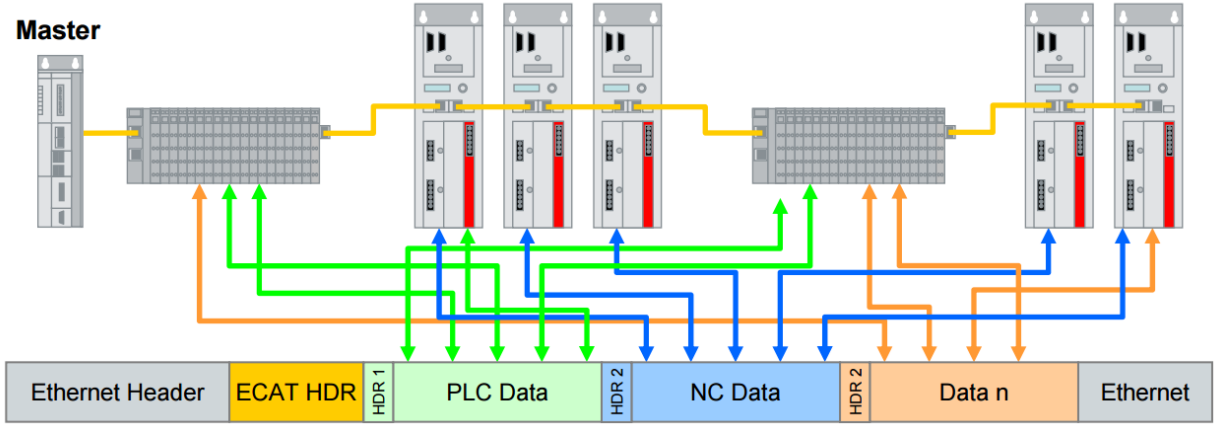
- **100Mbps Full-Duplex**
  - 100BASE-TX (optional - 100BASE-FX) is what Fieldbuses currently use
  - Auto-MDIX is often required in a forced 100Mbps operation
- **Latency** must be reduced to a minimum
  - Each bus specifies its own number of Hops (Nodes)
  - More Hops = increased delay, which adds up quickly in a Line Topology!
- **Determinism** (Latency Jitter) must be kept to a minimum for IRT applications
  - Most specify sub 100ns jitter and even lower depending on precision needed
  - Single MII clock cycle is 40ns! PHY must not skip a beat on either TX or RX
- **Fast Link Loss**
  - <15µs from loss of link to indication of link loss

Other common requirements…

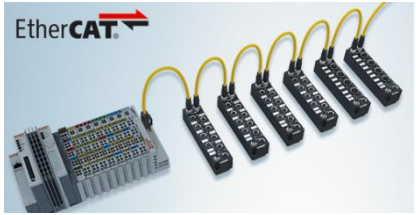
- **IPG** (Interpacket Gap) necessary for some but not all Fieldbuses
  - VARAN has a specific 120ns IPG requirement to reduce IPG bandwidth
- **Low Level Emissions**
  - Optimized by ensuring proper termination on both digital and analog sides
  - Reduced drive strength for shorter cables (most PHYs built to exceed 100m cable length but it is not often needed)
- **Excellent Immunity**
  - Both ESD and Radiated Immunity is key when operating in an environment with high voltage and motors
- **Low Power Consumption**
  - More Power = More Heat
  - Reducing power consumption helps decrease heat budget (board size and components)

EtherCAT - Ethernet “On the Fly”

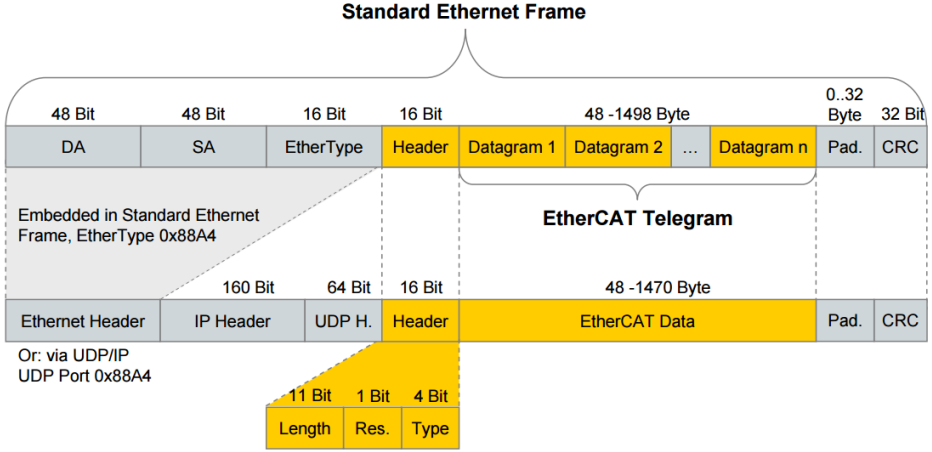
- Ethernet “On the Fly” allows for insertion and extraction of single bits or bytes of data without having to stop the entire Ethernet Frame
  - Allows 1 Bit to thousands of Bytes to be extracted or inserted on the fly
  - One Ethernet Frame can contain multiple Slave Devices using Datagrams



EtherCAT



- Developed by Beckhoff Automation
- Built for Real-Time applications with emphasis on bandwidth usage
- Transmission Rate: 2 x 100Mbps (100BASE-TX or 100BASE-FX, Full-Duplex)
- Employs Ethernet “On the Fly”
- IEEE 1588 used for clock synchronization



EtherCAT Slave Booster Pack with SPI Interface/ *TI Design TIDA-00299*

TIDesigns

Features

- EMC-compliant, industrial temp dual port EtherCAT slave with SPI interface
- 5-V Input Supply, to power entire board including optional DDR3 memory (not needed for EtherCAT with stack external)
- AM335x configured to boot EtherCAT firmware from SPI Flash or option to boot through SPI host processor.
- SPI slave interface (16MHz) or SPI master or McASP serial interface (40MHz) to host processor like C2000 to run the EtherCAT slave stack
- No external RAM required when EtherCAT slave stack runs on external host processor
- TI LaunchPad Compatible BoosterPack format with 3.3V TTL logic

Benefits

- Cost-Optimized Dual port EtherCAT slave with HW option for PROFIBUS and Multi-protocol RT Ethernet
- TPS650250 PMIC used to generate all power rails needed
- DP83822, low latency, robust 10/100 PHY, EtherCAT conformance tested and/or certified with Fast Link Drop
- Designed to meet IEC61000-4-2, 4-4, 4-5 EMC Immunity

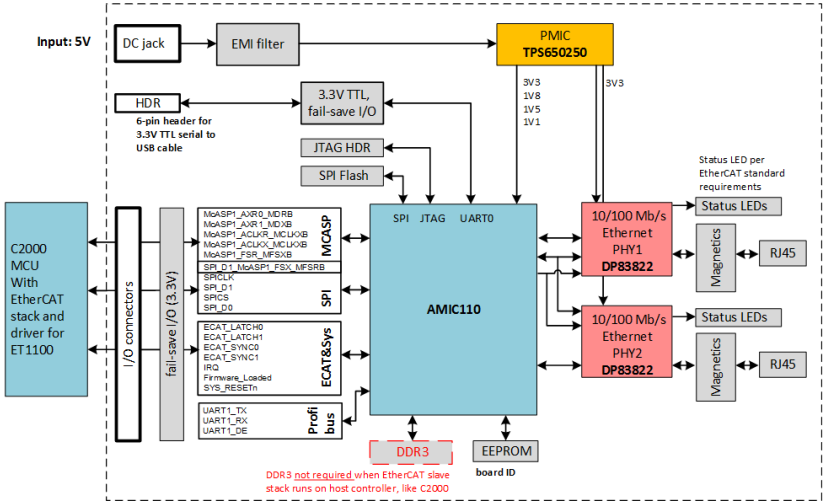
Target Applications

Industrial drives
Industrial sensors
Industrial automation

Tools & Resources

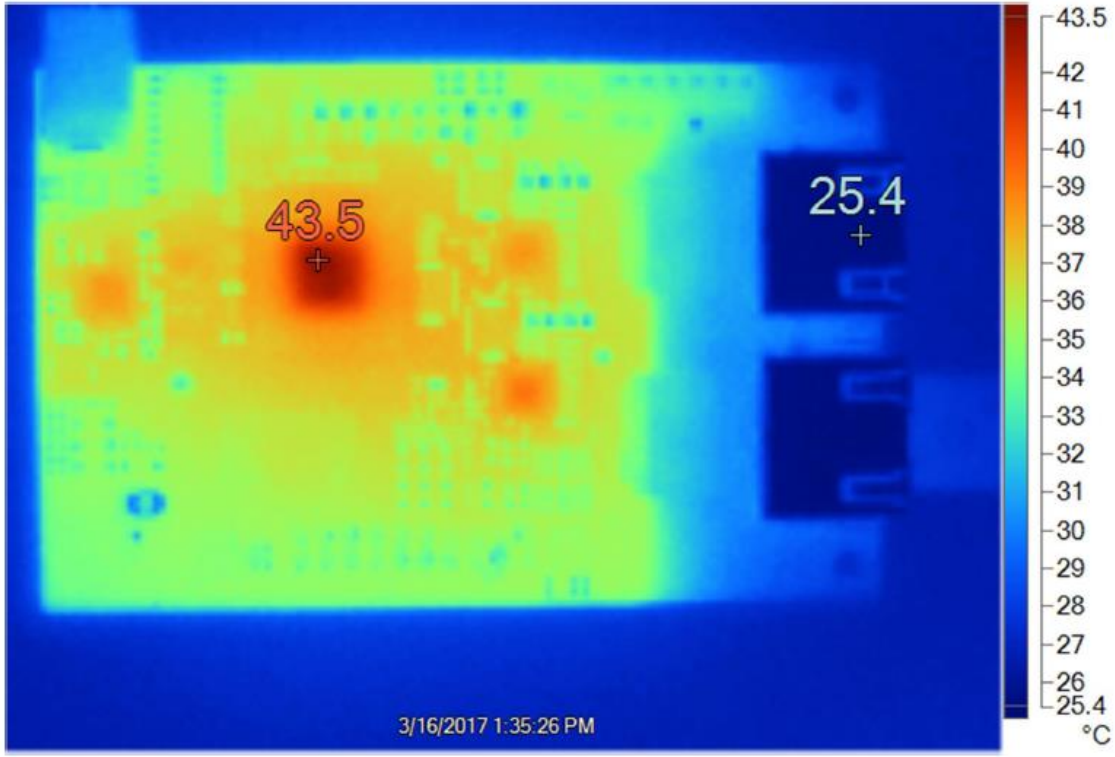
Board Image

- **TIDA-00299 and Tools Folder**
- **Design Guide**
- **Design Files:** Schematics, BOM, Gerbers, and more
- **Device Datasheets:**
  - DP83822I, AMIC110, TPS650250



Texas Instruments

Thermal Image of TIDA-00299

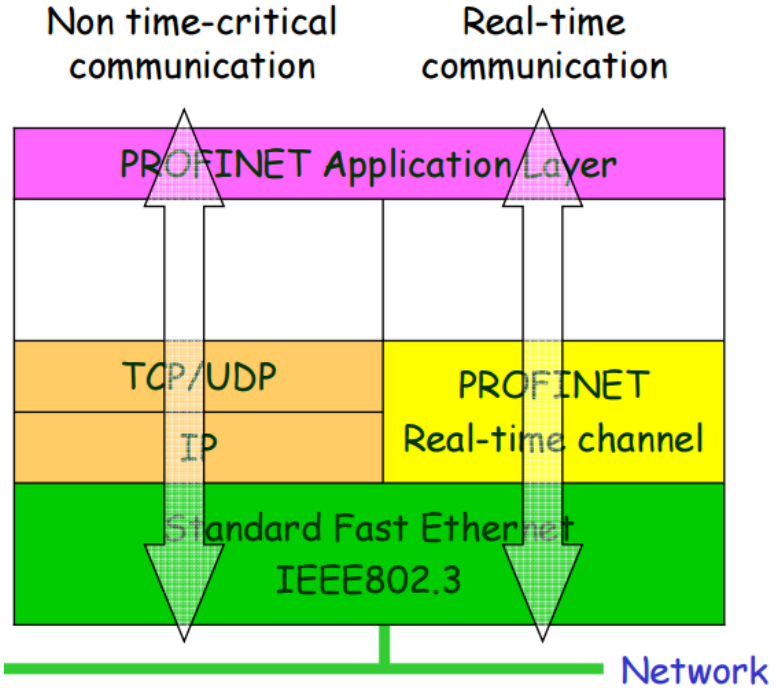


PROFINET

- PROFINET – Process Field Network
- Transmission Rate: 2 x 100Mbps (100BASE-TX or 100BASE-FX, Full-Duplex)
- Three main protocol levels:
  - TCP/IP for PROFINET CBA applications, 100ms reaction times
  - RT (Real-Time) for PROFINET IO applications, 1ms cycle times
  - IRT (Isochronous Real-Time) for PROFINET IRT applications, <1ms cycle times
- Makes use of both Non time-critical communication and Real-Time communication through the use of separate PROFINET stacks depending on system requirements
- Topologies: Line, Star, Ring

PROFINET RT and IRT

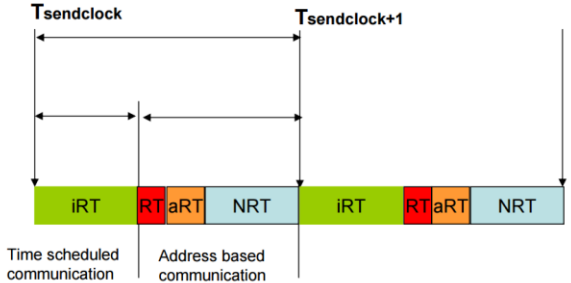
- Real-Time typically used in Factory Automation
  - Response time in the tens of milliseconds
- Isochronous Real-Time typically used in Motion Control
  - Response in around 1ms with jitter <1µs
  - IEEE 1588 PTP
  - Segmentation
  - Time Scheduled Communication
    - Reserved Bandwidth



PROFINET RT and IRT

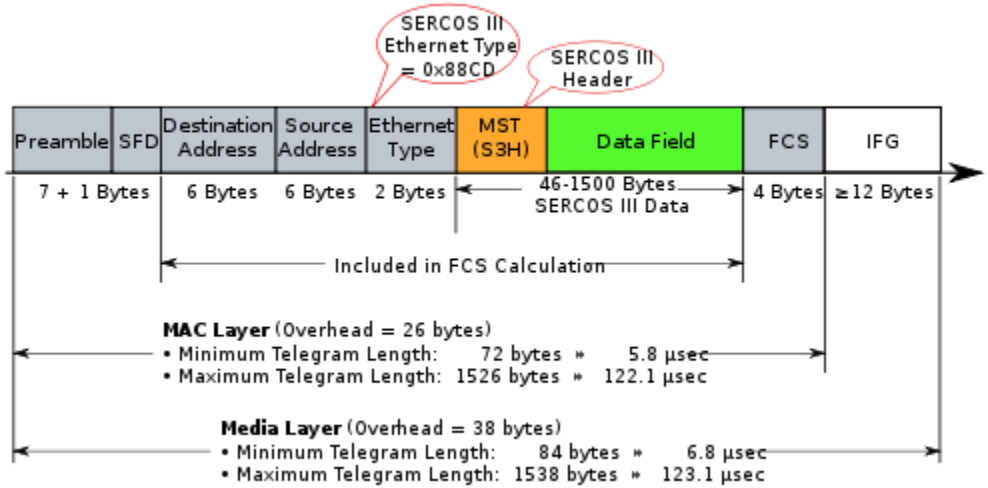
- Real-Time must share bandwidth with TCP/IP data
  - 1 minimum frame for RT communication is 64 bytes
  - 8 Bytes Preamble + SFD
  - 12 Bytes IPG
  - Total 84 Bytes @ 80ns per Byte = 6.7µs
- IRT is allocated its own dedicated time schedule
  - 1 µs jitter permitted through 30-32 hops from first to the last device!

$$T_{sendclock1} \_ Ts_{endclock} = 1ms$$



SERCOS III

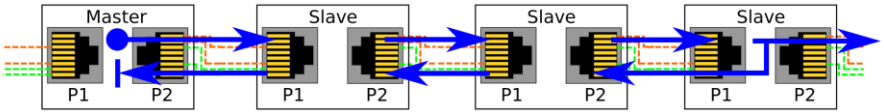
- Built for Real-Time applications with cycle times as low as 31.25µs
- Transmission Rate: 2 x 100Mbps (100BASE-TX or 100BASE-FX, Full-Duplex)
- Minimum Frame of 84 Bytes and Maximum Frame of 1538 Bytes (including all layer overhead)



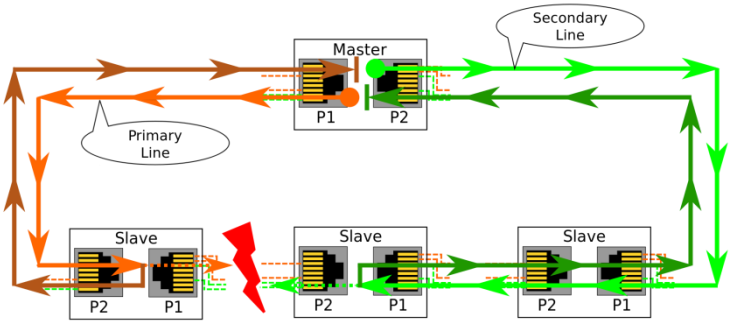
SERCOS III

- Two main topologies used by SERCOS III
  - Line Topology
  - Ring Topology
- Ring Topology allows for redundancy by enabling the use of secondary path
  - Break Recovery <25µs

Line Topology



Ring Topology



EtherNET/IP

- Developed by Rockwell Automation in 2000
- EtherNET/IP is sublayer within the CIP
  - Common Industrial Protocol
  - Built for Automation applications with two types of data: TCP/IP and UDP/IP
- Star Topology with cycle times <10ms
- Node synchronization with distributed clocks from IEEE 1588 PTP

VARAN, Modbus TCP/IP and POWERLINK

TECH DAYS
Texas Instruments

- VARAN
  - **V**ersatile **A**utomation **R**andom **A**ccess **N**etwork founded in 2006
  - Built for Isochronous Real-Time applications with maximum 0.1µs jitter and <100µs cycle times
- Ethernet POWERLINK
  - Developed by B&R in 2001, The Ethernet POWERLINK Standardization Group (EPSG)
  - Built for Isochronous Real-Time applications with maximum 0.1µs jitter
- Modbus TCP/IP
  - Developed by Schneider Automation in 1999
  - Limitations on Real-Time applications due to stack overhead

TI's Industrial Ethernet Portfolio
Recommended PHYs

TI's DP83822 10/100 Ethernet PHY

DP83822
10/100 Ethernet PHY

TECH DAYS
Texas Instruments

Highlights

- **Industry's Lowest Power 10/100Mbps PHY**
  - 1.8V operation <110mW
- Small package **QFN32** (5mmx5mm)
- Long cable reach >150m
- **100BASE-TX, 100BASE-FX** and **10BASE-Te**

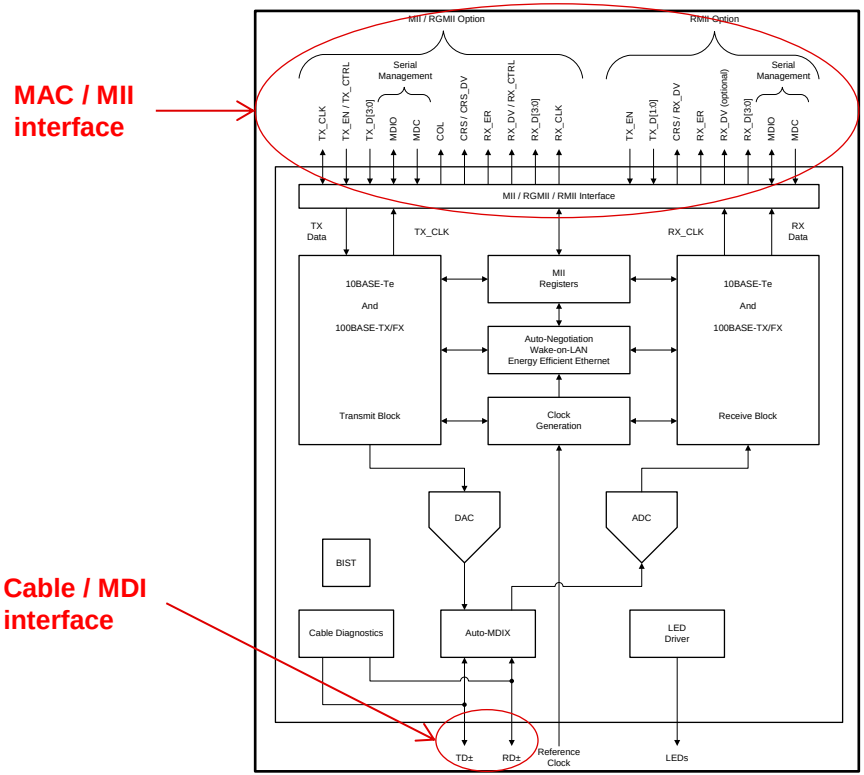
Key Specs

- MII / RMII / RGMII MAC Interfaces
- HBM (**+/-16kV**), IEC61000-4-2 (**+/-8kV**)
- **Start of Frame Detection for IEEE1588**
- Industrial Temperature Range **-40C to 85C/125C**

Applications

- Factory Automation, Motor Drives, Power Automation, Industrial Lighting

DP83822 Block Diagram



DP83867 Gigabit Ethernet PHY Overview

DP83867

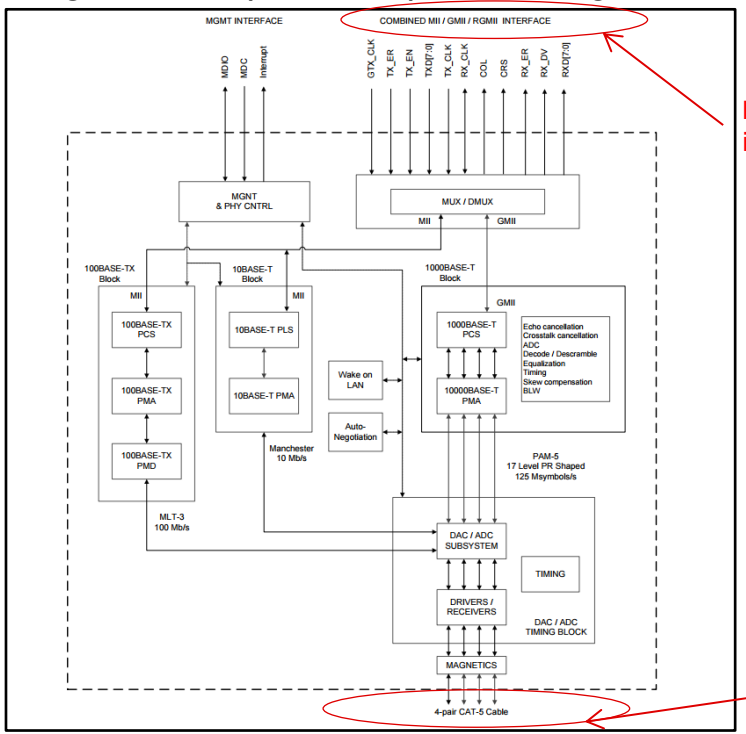
10/100/1000 Low Power and Robust Ethernet PHY

- **Highlights**
  - **IEC 12kV specification!**
  - Lowest latency for both 100Mbps and 1Gbps modes, <400ns
  - Power saving features: WoL
  - **Pass EN55011 class B**
  - **Low power 1GbE solution, <400mW**

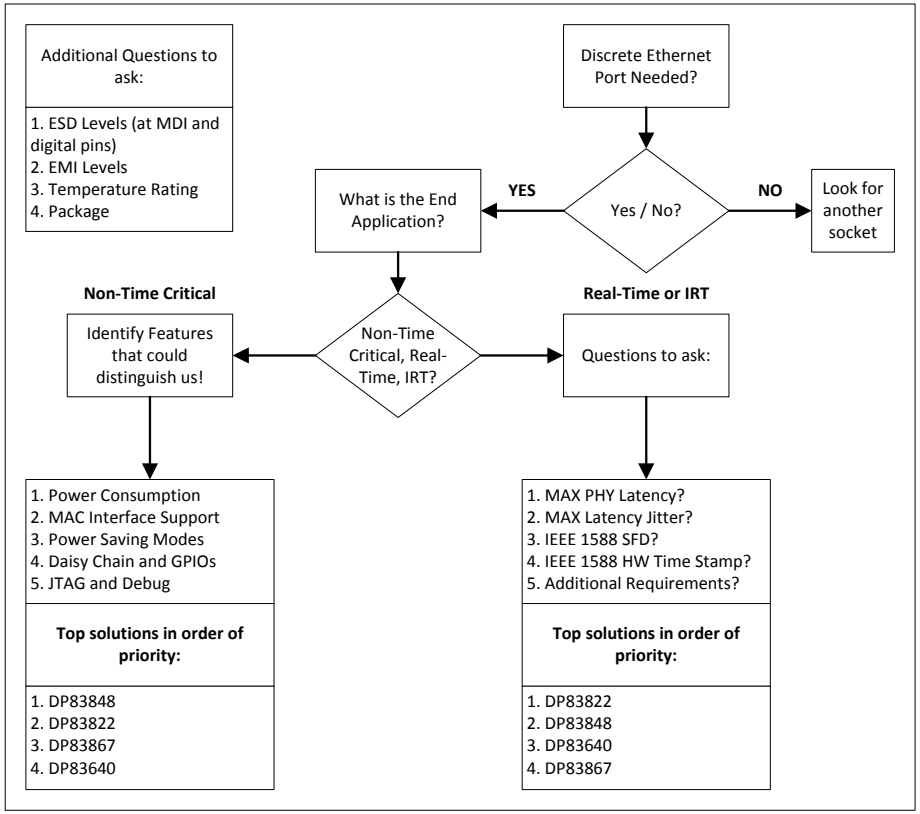
- **Key Specifications**
  - GMII/RGMII/MII/SGMII
  - **Start of Frame Detect for IEEE 1588 time stamp**
  - JTAG (IEEE 1149.1)
  - 25MHz or 125MHz Output clock
  - Pin to pin temperature grades (0 to 70C) through **(-40C to 105C)**
  - **QFN48** or QFP64

- **Applications**
  - Industrial: Automation, Test Equipment, Sensors
  - Communications: Debug /Management Port, Small Cell
  - Commercial: Network Printers, Broadband gateways

Gigabit PHY (DP83867) Block Diagram



Industrial Ethernet Decision Tree



TIDA-00204:

EMI/EMC Compliant Industrial Temp Dual Port Gigabit Ethernet Reference Design

TIDA-00204

Industrial EMI Compliant Dual-Port Gigabit Ethernet PHY Eval Kit

TIDesigns

TECH DAYS Texas Instruments

Features

- EMI- and EMC-compliant design with wide input voltage range (17-60V) using **two DP83867IR Gigabit Ethernet PHYs** and AM3359 Sitara™ processor with integrated Ethernet MAC and Switch
- Configured for RGMII and SMI interface to PHYs
- Sitara™ AM3359 firmware with UDP, TCP/IP stack and HTTP web server examples
- AM3359 configured to boot from on-board SD-Card allowing easy standalone operation
- **DP83867IR register access via USB virtual COM port**
- On-board JTAG interface for own firmware development
- Hardware support for Start-of-Frame Detect allows implement **IEEE1588 PTP**

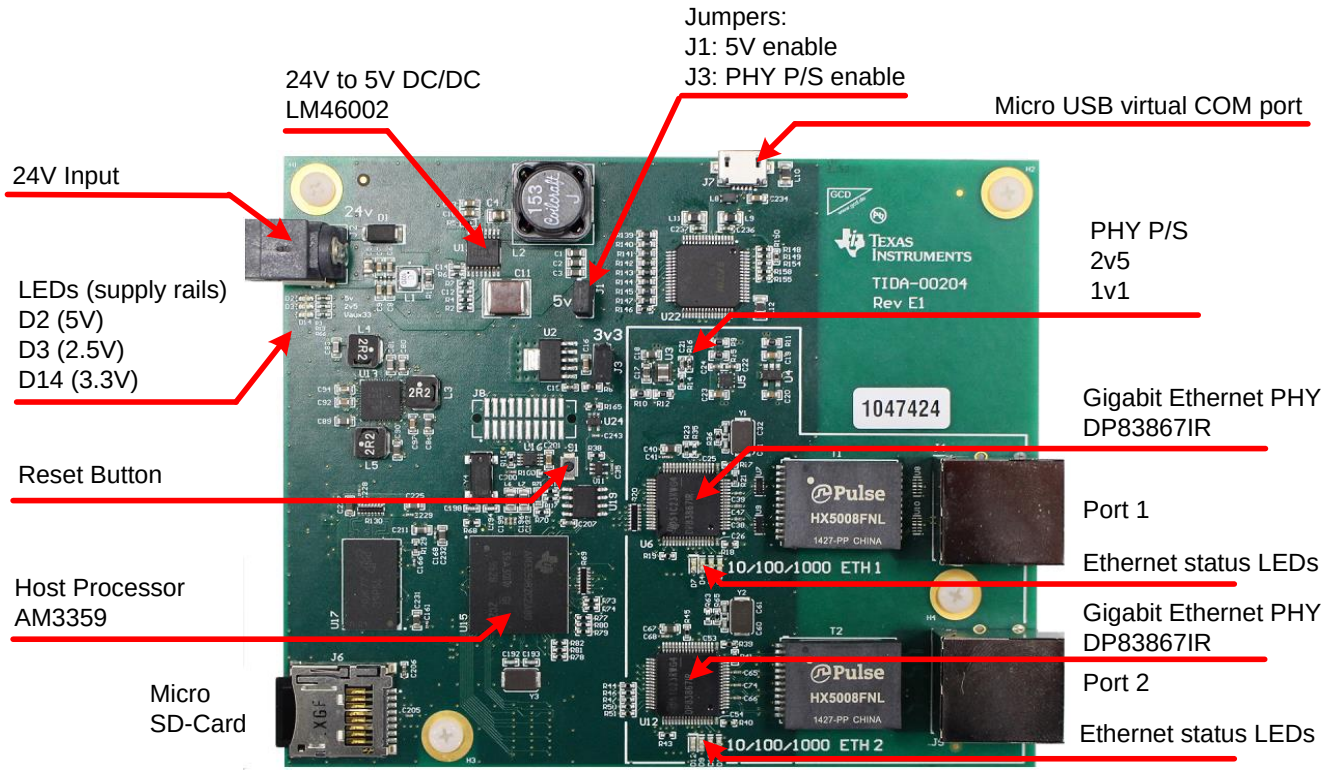
Benefits

- **Allows for easy PHY performance evaluation**
- Exceeds CISPR 11 / EN55011 Class A radiated emission requirement by > 4.3dB
- **Exceeds IEC61800-3 EMC immunity requirements**
  - +/-6kV ESD CD per IEC 61000-4-2
  - +/-4kV EFT per IEC 61000-4-4
  - +/-2kV Surge per IEC 61000-4-5
- Designed for Industrial Temperature Range
- Option for custom specific PHY configurations, like RGMII Delay Mode

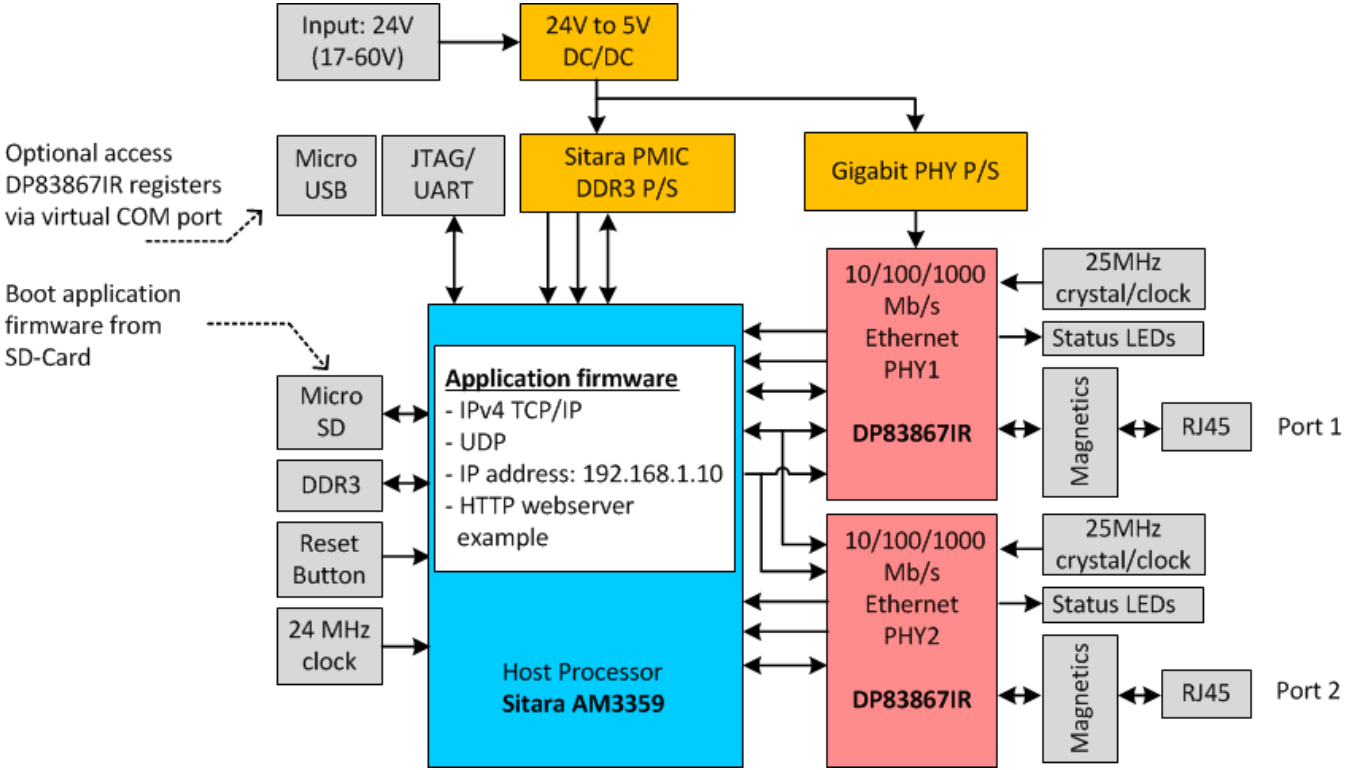
Applications

- Industrial drives
- Factory automation and control
- Industrial networks
- Smart energy
- Test and measurement

TIDA-00204 PCB Overview



TIDA-00204 Block Diagram



TI Devices

- AM3359
- DP83867IR
- LM46002
- LMZ10501
- SN74AHC1G08
- SN74AUP2G08
- SN74LVC1G06
- TPD4E05U06
- TPD4S012
- TPD6E001
- TPS51200
- TPS717
- TPS720
- TPS737

Get Started Today!

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Customers can get started by:

- Purchase the DP83867IRPAP-EVM
  - Link for the e-store
- Visit links below for the latest documentation and product information
  - TIDA-00204 Design Page
  - DP83867IR Product Folder
  - DP83867 RGMII Linux Drivers
- Looking for a 10/100 PHY Ethernet solution from TI Designs?

  Visit the link below for the EN55011 Compliant, Industrial Temperature, 10/100Mbps Ethernet PHY Brick Reference Design
  - TIDA-00207 Design Page

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Thank You!

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Back Up Slides

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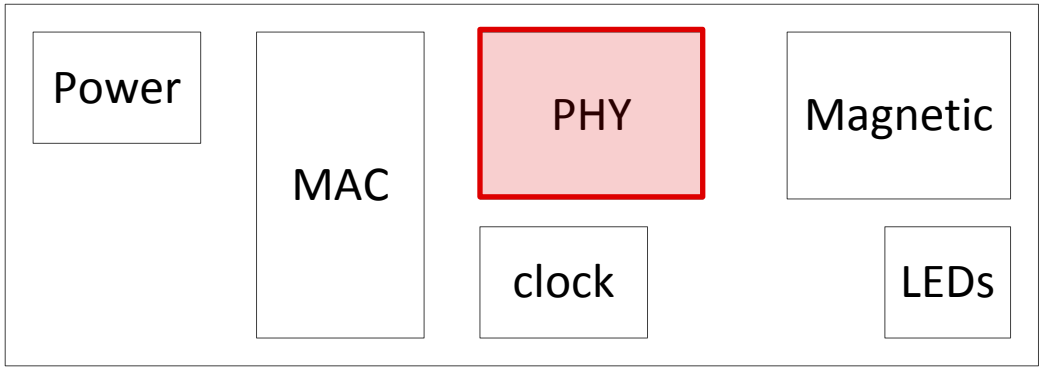
Layout For EMC/EMI

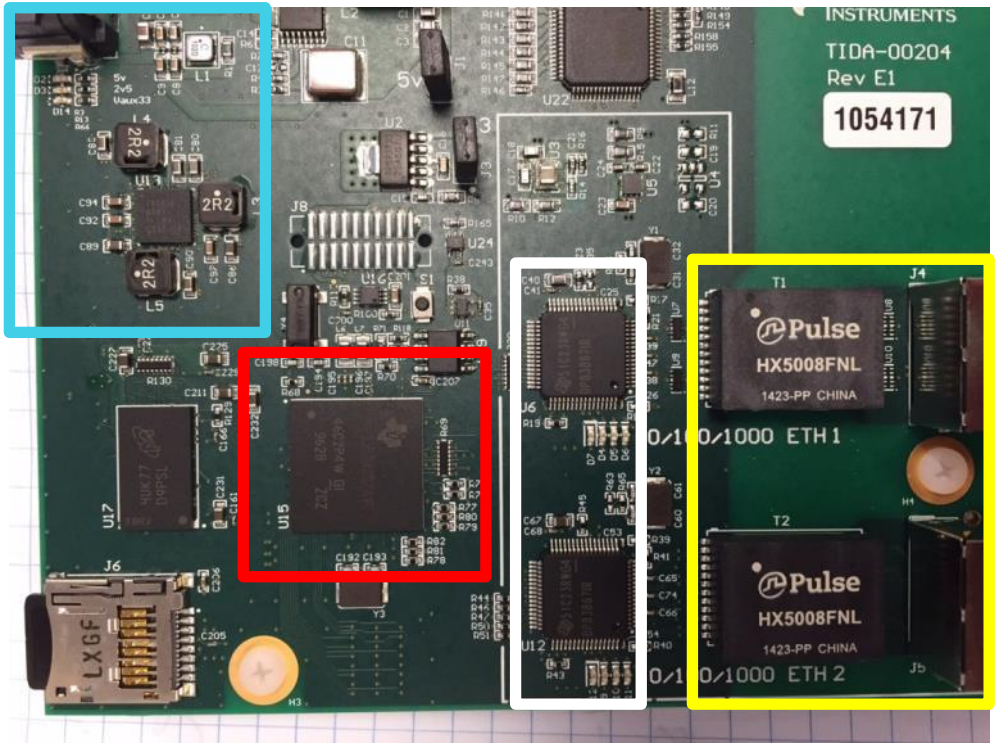
Board Zoning

- Identify key components in the design
  - Centrally locate them
- Differential signaling should be routed first
- High frequency paths close to destination and away from analog signals
- Lower frequency can be moved further away



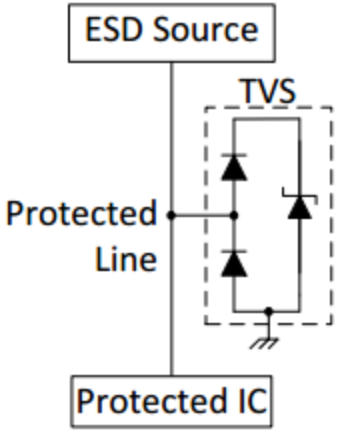
Board Zoning (2)

- De-coupling capacitors close to pins
  - VDDIO
  - AVD25
  - AVD11
- 4 Layer Boards vs 2 Layer Boards
  - Signal Return
  - Small Loops
  - Buried Lines
  - Fewer via



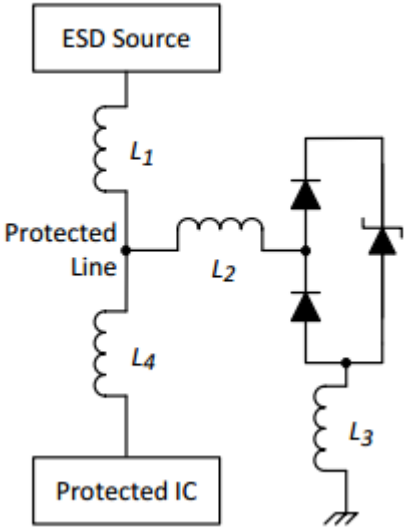
Visualizing the Strike

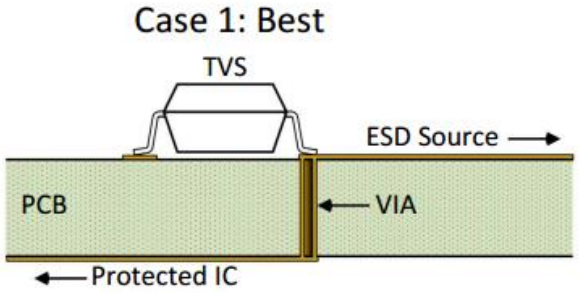
- ESD/EFT/Surge events should not be allowed to find their own path to ground
- Careful control of PCB impedances is critical for high immunity performance
  - Present low impedance path to earth ground quickly!

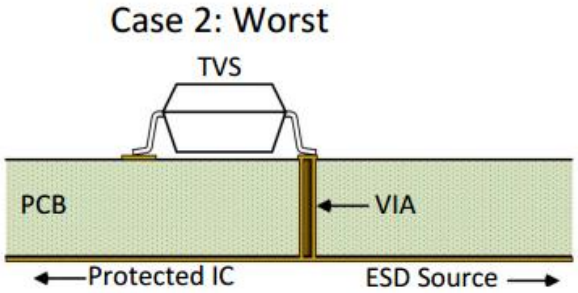


Directing the Energy

- Parasitics of PCB traces play a large role in where the energy of the strike flows
- In the example diagram, we can intuitively see that if L1>>L4, the current of the strike will mainly flow through the TVS device
  - This can be achieved by placing the TVS closer to the ESD source than the device
- Vias can also be used to control the impedance
  - See the example below where the lowest impedance path for the ESD source is through the TVS

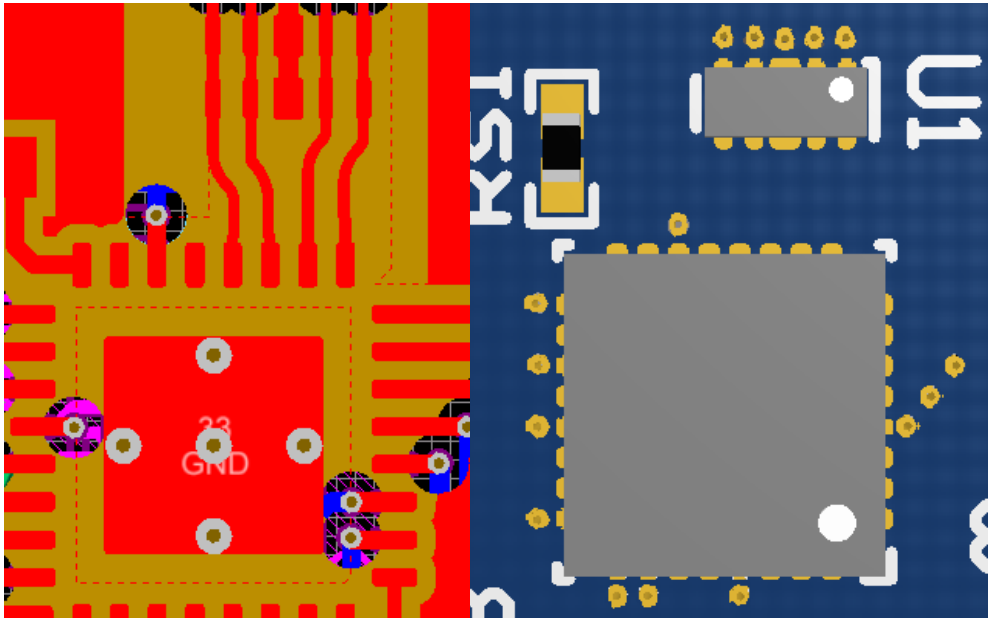




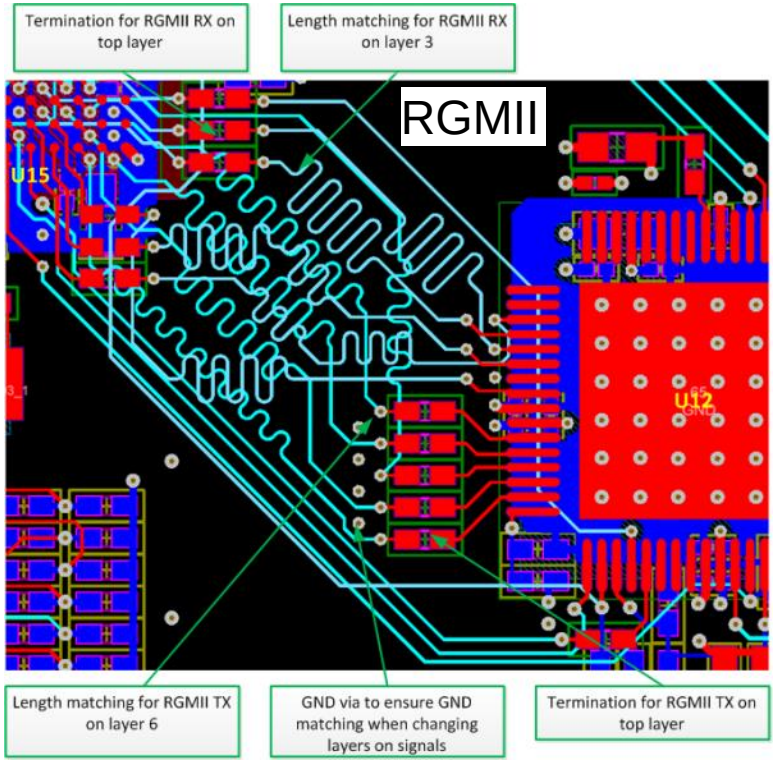


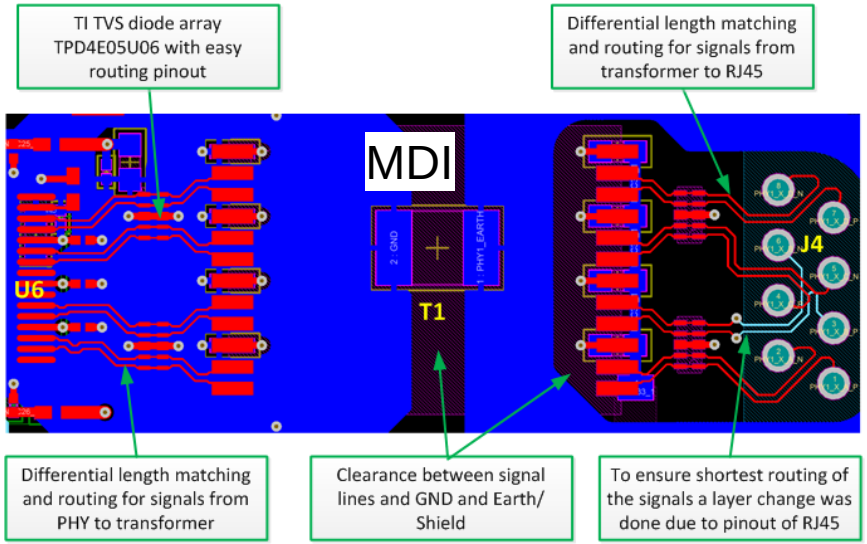
Layout For ESD

- TVS diode array in-line
- Low capacitance
  - Return Loss
- Differential routing
  - Min effect on impedance control
- Placement between IC and Magnetic



Layout for EMI and EMC





Things to look out for

- Solid return path beneath critical signal traces
  - No break in return path
- Termination Resistors, if needed, should be near the PHY
- PHY power supply decoupling caps should be kept near the device
- No metal between differential pair
- No floating metal
- No stubs on high frequency critical signals
  - If stubs are unavoidable, they should be short as possible
- No metal beneath the magnetics
- All TX traces should be matched and also the RX traces.