PCB Layout for SMPS

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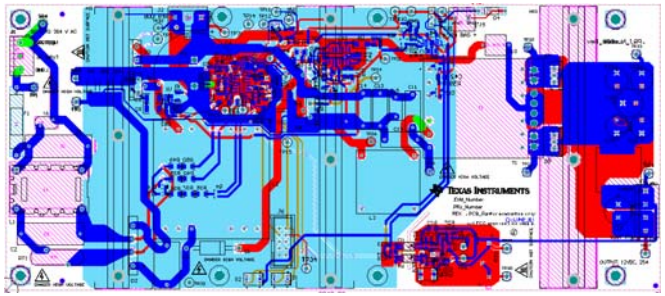
Agenda

- Introduction
- The Schematic
- Parasitic Components
- SMPS Characteristics
- PCB Layout – General
- PCB Layout – Effect on EMI
- PCB Layout – An Example
- PCB Layout – Review
- PCB Layout – Things you don’t have to worry about
- PCB Layout – Summary



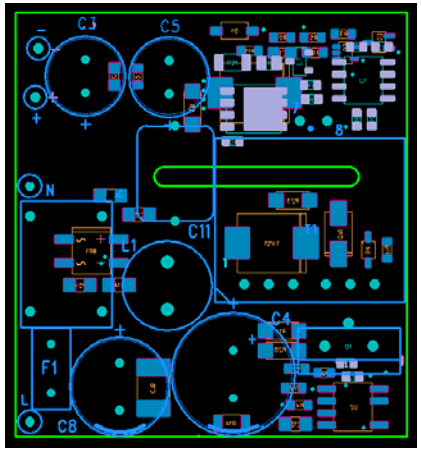
Introduction

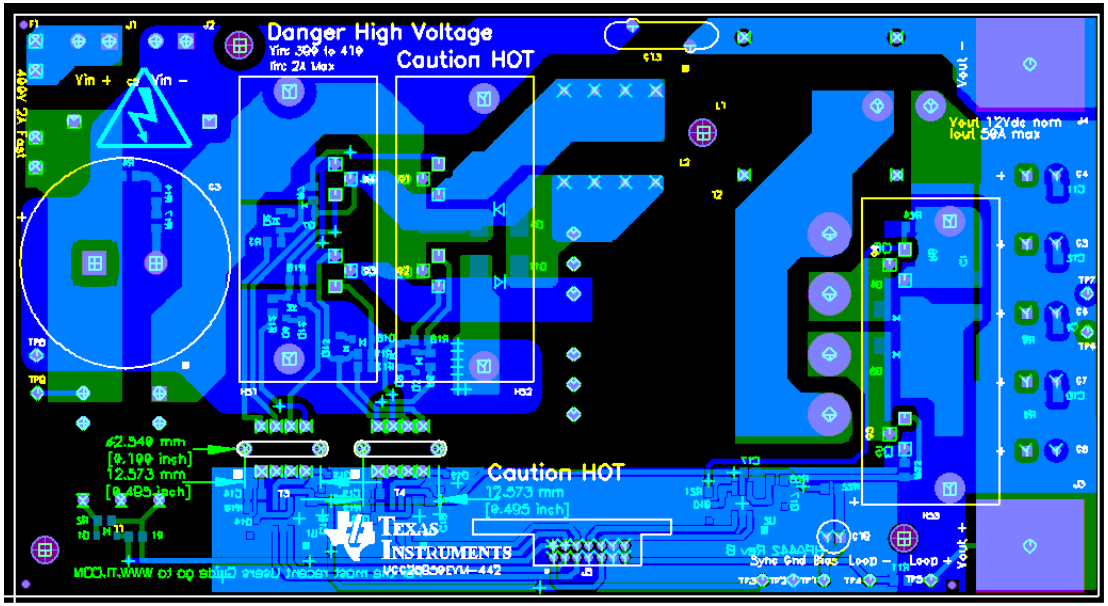
PCB Layout for SMPS

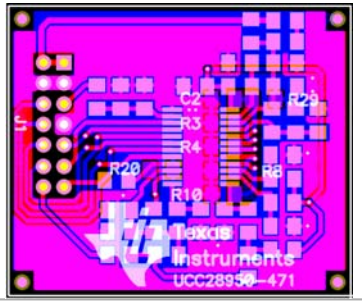
Introduction:

I would suggest that

- The PCB is usually the single most complex custom component in the design



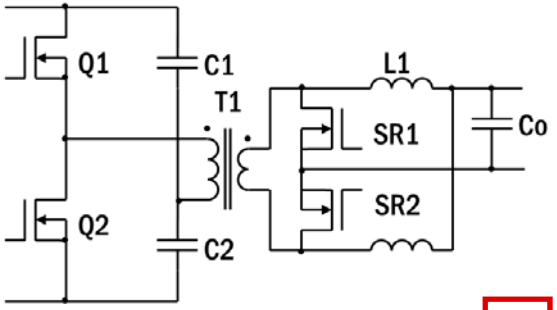




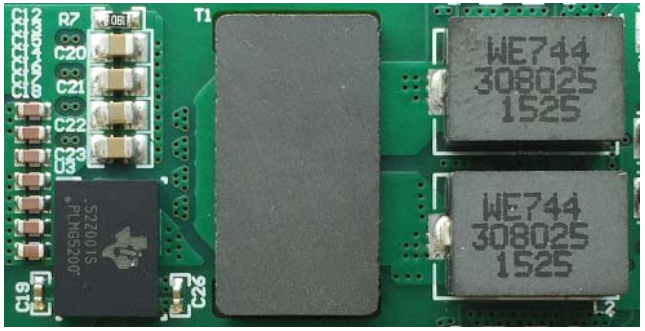
Introduction:

What issues must be considered when laying out a PCB for a Switched Mode Power Supply (SMPS) ?

- A high proportion of the PCB layouts I see have critical defects
- The best controller in the world cannot work well if embedded in a poor layout
- PCB layout for SMPS is difficult
- The same general principles govern low and high power layouts –
- The difficulty is how to apply the principles in practice



How to translate a schematic into working hardware

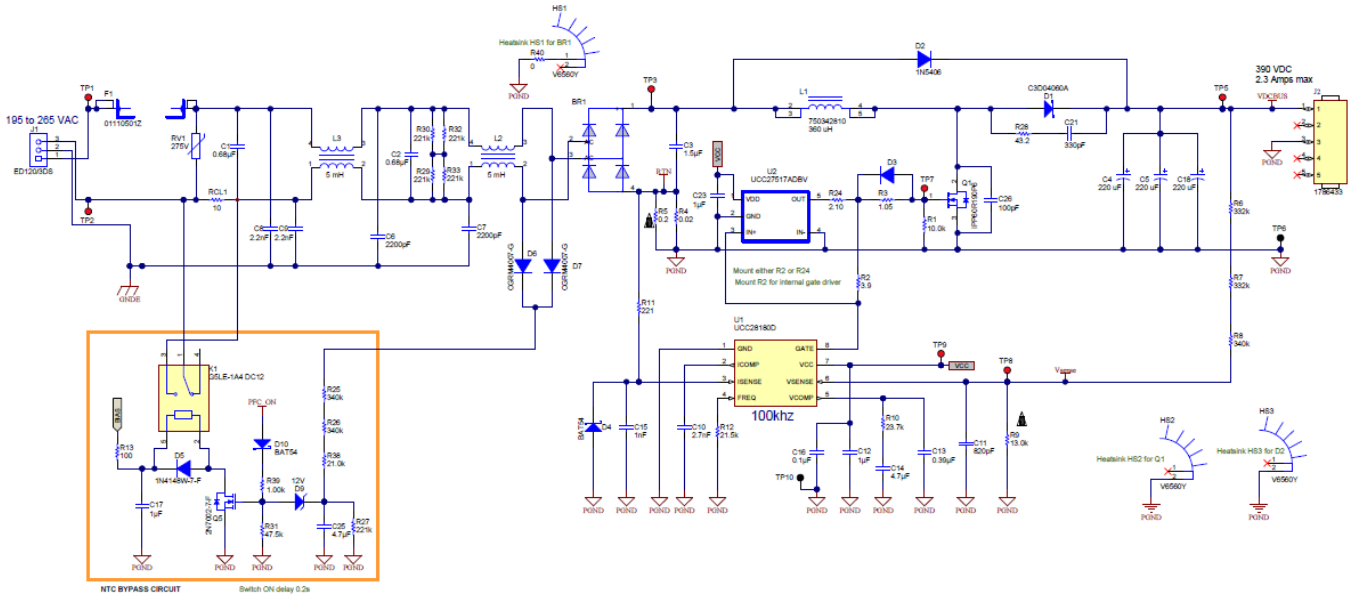


The Schematic

PCB Layout for SMPS

The Schematic:

Typical schematic of a CCM boost converter



The Schematic:

Typical schematic of a CCM boost converter – Shows about 1/3 of the components !

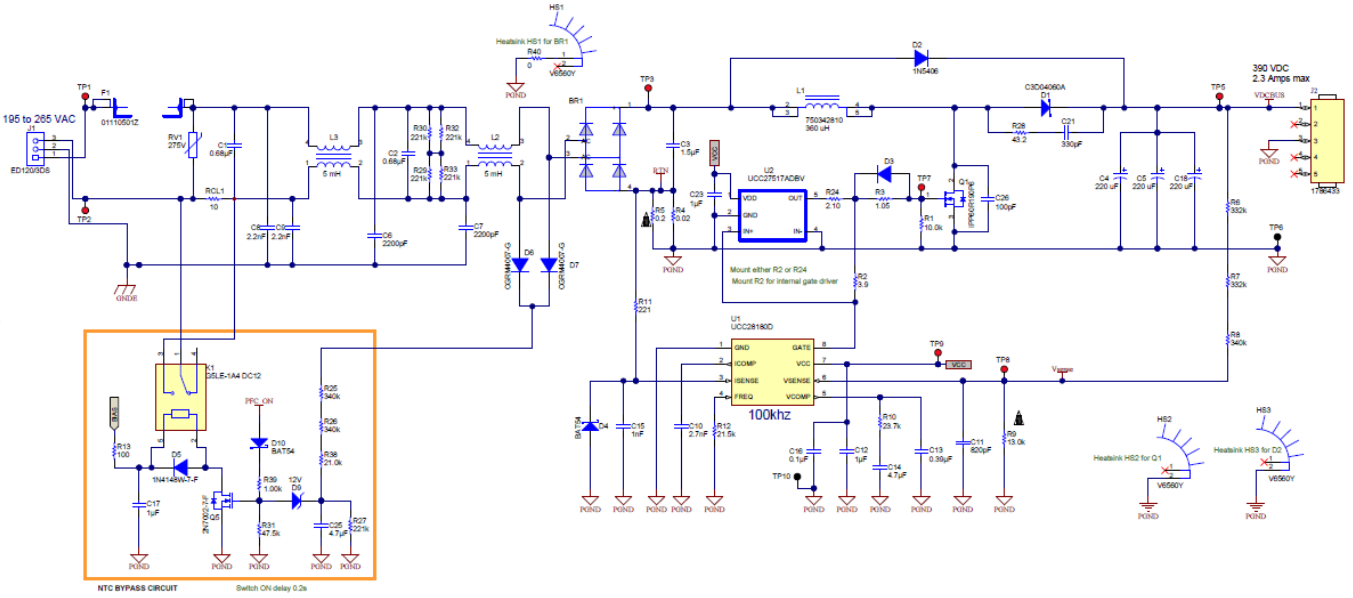
Does NOT include component or PCB parasitics !

Component parasitics.

- ESR in capacitors
- Coss in MOSFETs
- Leakage inductances

Layout parasitics

- Track resistance
- Stray capacitances
- Stray inductances



Key to a successful layout is understanding the circuit, including the parasitic components

Parasitic Components

PCB Layout for SMPS

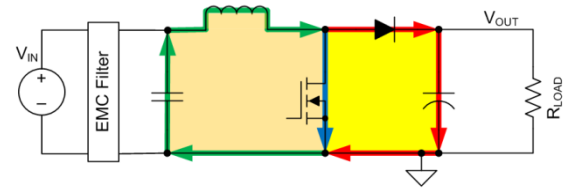
Know the effect of component parasitics:

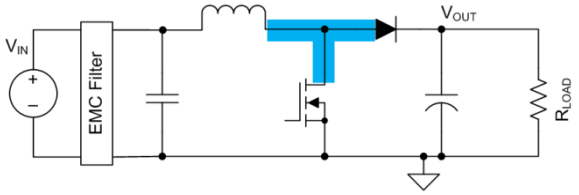
You get parasitic components for free,

but you have to pay a performance penalty for them.

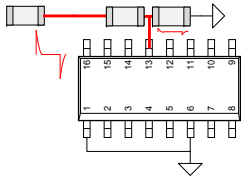
Ideal components DO NOT EXIST

- Capacitors have ESR, ESL, C varies with Temp and V
- Inductors have inter-winding C
- Leakage inductance in transformers
- Stray capacitances around MOSFETs
- Even Resistors have parasitic L and C
- PCB tracks have R, L and C





- This is NOT an exhaustive list



Parasitics: Capacitance

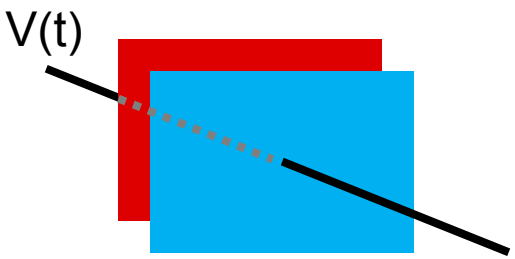
Building a capacitor is easy – two conductors separated by an insulator.

No simple formula for the general case – (non standard geometries)

For a flat plate capacitor $C = \varepsilon_0 \varepsilon_r \frac{A}{d}$

Permittivity of free space $\varepsilon_0 = 8.85\, x10^{-12}\, F\, m^{-1}$
Relative permittivity $\varepsilon_r \approx 4.4$ (Fiberglass)

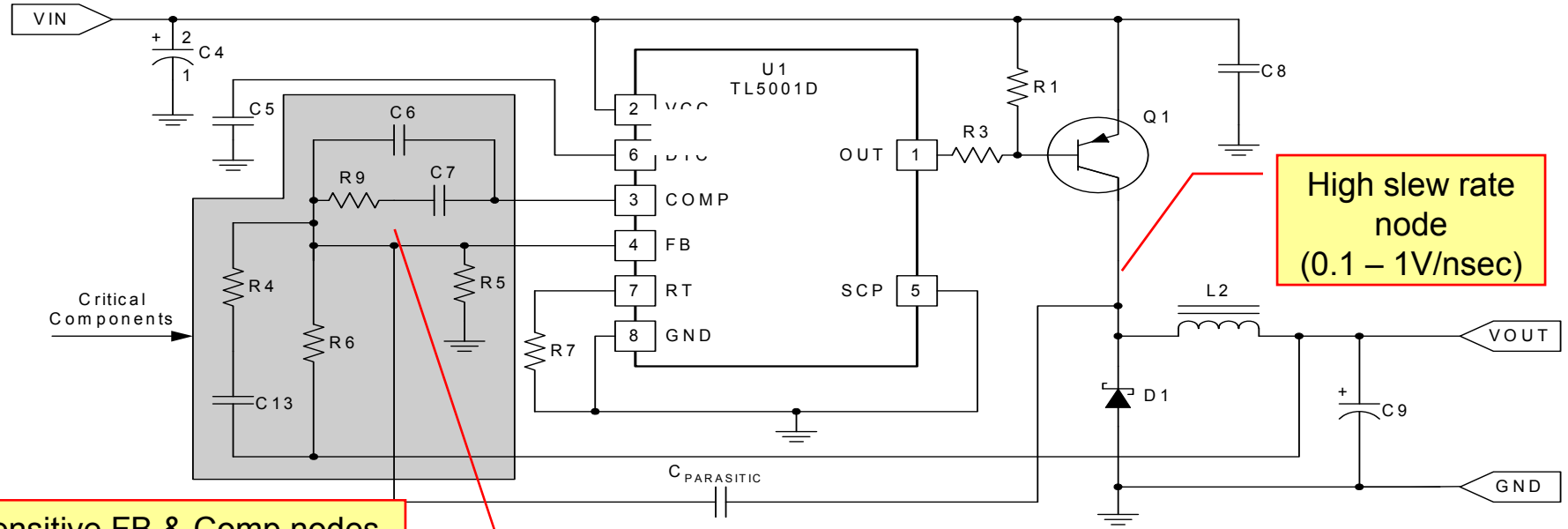
Stray capacitance should be minimised



Chaos Created by Noise Injection

Ten 0.05 x 0.02 in^2 pads in summing junction can increase parasitic capacitance to 2 pF

High Slew rate can inject 1mA current from only 1pF parasitic cap



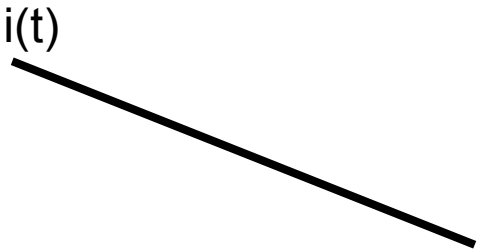
Parasitics: Inductance

Building an inductor is even easier – inductance is a measure of the energy contained in the magnetic field set up by an electric current – all you need is a conductor with a current in it.

Simple formulae exist for specific geometries – toroids, E cores etc.

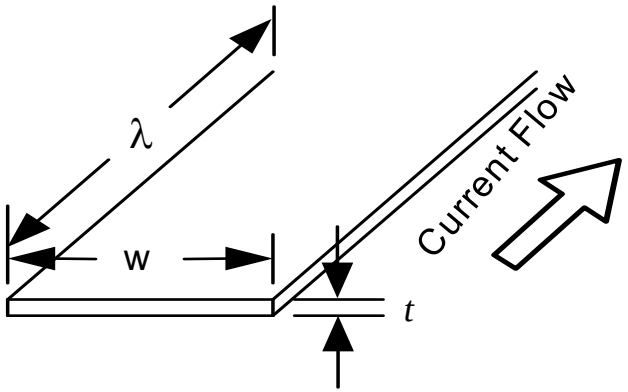
In general no simple formula for stray inductance. ‘Shorter is better’ 1nH per mm – rule of thumb.

Wider tracks = lower parasitic L (ONLY WITH A GROUND PLANE)



Self Inductance of PWB Traces

Due to the natural logarithmic relationship, large changes in conductor *width* have minimal impact on inductance.



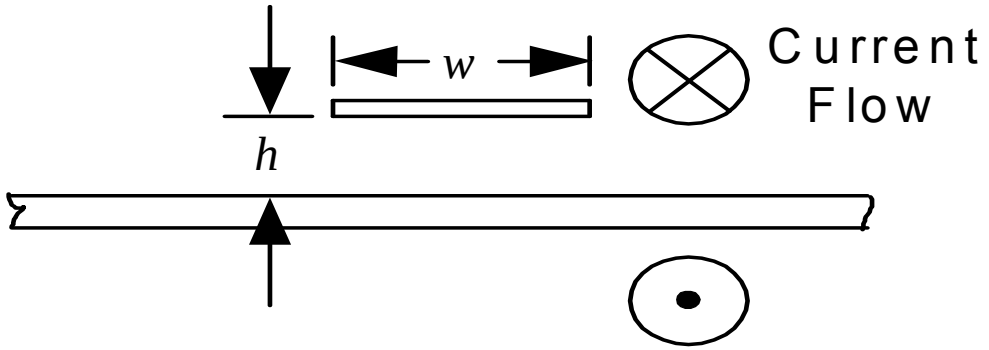
$$L = 2\lambda\left(\lambda n\left(\frac{\lambda}{t+w}\right)+\frac{1}{2}\right)\ nH\ \ (cm)$$

$$L = 5\lambda\left(\lambda n\left(\frac{\lambda}{t+w}\right)+\frac{1}{2}\right)\ nH\ \ (in)$$

W (mm/in)	T (mm/in)	Inductance (nH/cm or nH/in)
0.25 / 0.01	0.07 / 0.0028	10 / 24
2.5 / 0.1	0.07 / 0.0028	6 / 14
12.5 / 0.5	0.07 / 0.0028	2 / 6

PWB Traces Over Ground Planes

- Substantial inductance reduction
- Inductance inversely proportional to width



$$L = \frac{2\,hl}{w}\ \text{nH/cm}$$

$$L = \frac{5\,hl}{w}\ \text{nH/in}$$

Metric			English		
h (mm)	w (mm)	Inductance (nH/cm)	h (in)	w (in)	Inductance (nH/in)
0.25	2.5	0.2	0.01	0.1	0.5
1.5	2.5	1.2	0.06	0.1	3.0

Parasitics: Resistance

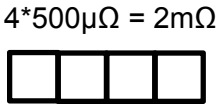
All conductors exhibit resistance – (except superconductors).

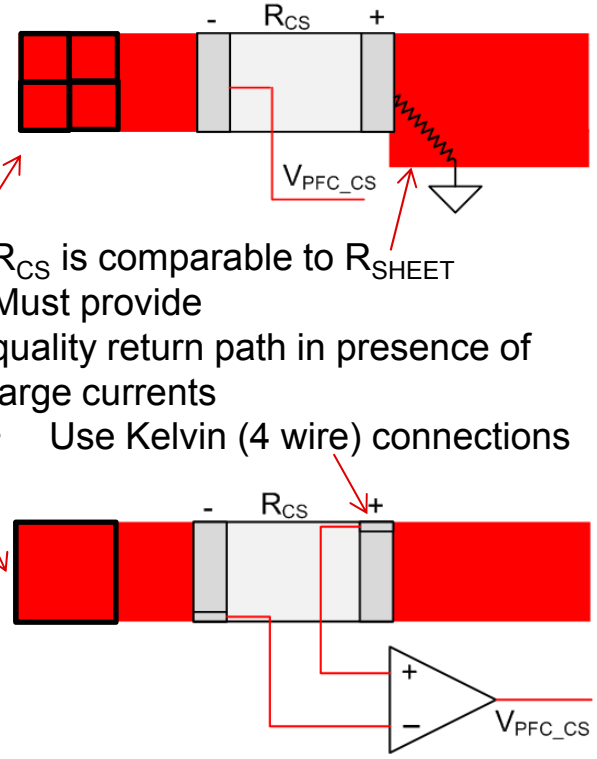
- Simple formulae exist for specific geometries
- Sheet Resistivity: $R_{sheet} = \rho \frac{l}{A}$
- ≈ 500μΩ per square for 1oz (34μm) cu

This is important where currents are high

Current sensing resistors – 20 mΩ typical

Copper has a large temperature co-efficient of resistance
$TCR_{cu} \approx 4000\, ppm\, °C^{-1}$ (+40% for 100°C rise)





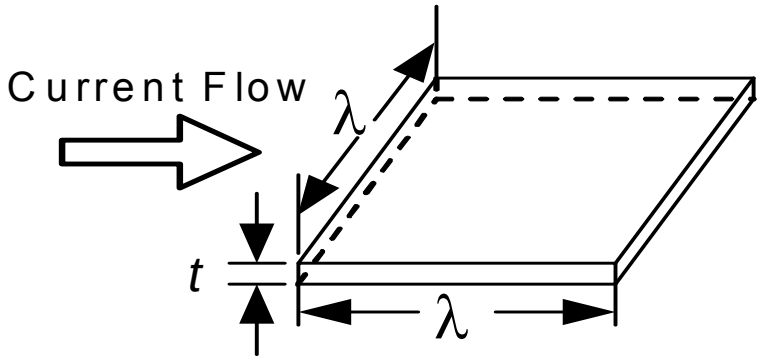
R_{CS} is comparable to R_{SHEET}
Must provide
quality return path in presence of large currents

- Use Kelvin (4 wire) connections

Blog: Why should I count squares

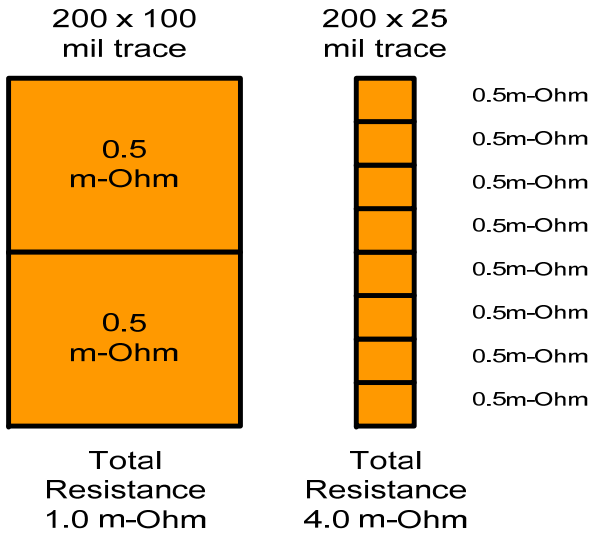
Trace Resistance Estimate: Count Squares

- Copper resistivity is 0.67μΩ in. at 25°C and doubles (linearly) for 254°C rise



$$R = \frac{\rho(\lambda)}{t(\lambda)}$$

$$R = \frac{\rho}{t}$$

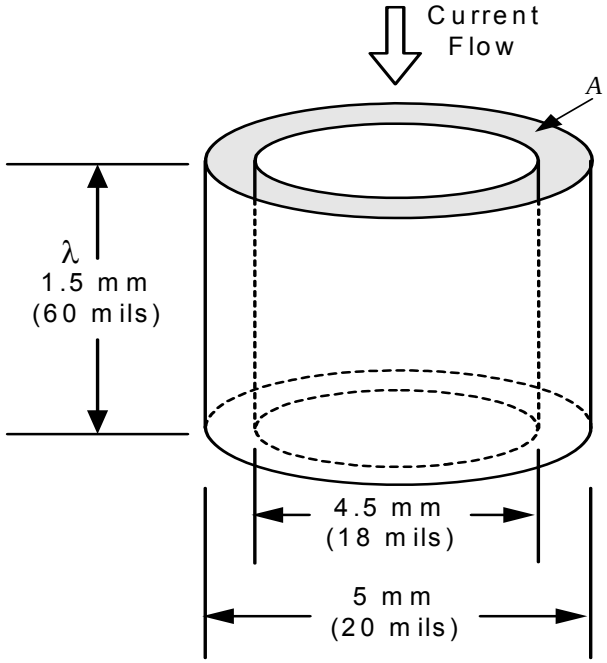


Copper Weight (Oz.)	Thickness (mm / mils)	mΩ per Square (25°C)	mΩ per Square (100°C)
1/2	0.02 / 0.7	1.0	1.3
1	0.04 / 1.4	0.5	0.65
2	0.07 / 2.8	0.2	0.26

TI specifies 2oz base copper for all power supply PCBs

Vias Have Resistance Too

- Typical rule of thumb is 1 A to 3 A per via
  - Create multiple vias for higher currents



$$R = \frac{\rho l}{A}$$

$$R = \frac{\rho l}{\pi (r_o^{\,2} - r_i^{\,2})}$$

$$R = \frac{2.36 \times 10^{-6} \times 0.06}{\pi (0.01^{\,2} - 0.009^{\,2})} = 2.4\ m\Omega$$

SMPS – Characteristics

PCB Layout for SMPS

Understand the operation of the circuit:

Identify the loops with high di/dt

- Especially the paths where the current is switched on and off
- Stray inductance here will cause voltage spikes

Identify the nodes with high dv/dt, (switched nodes)

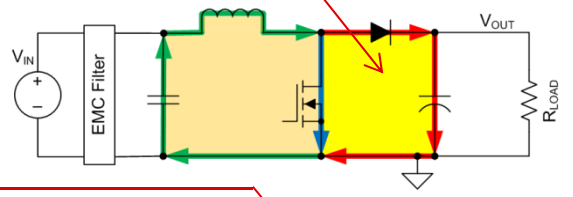
- Stray capacitance will couple noise currents into other nodes

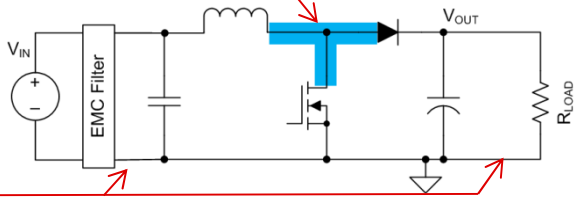
Identify the lines with high DC (or low frequency AC) currents.

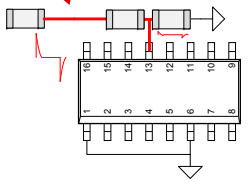
- Resistance causes voltage drops and control errors

Identify the signal connections

- These are susceptible to having noise coupled onto them (Victims)
- Noise can cause control upsets – jitter, instability etc.







PCB Layout: Switched Loops (High di/dt)

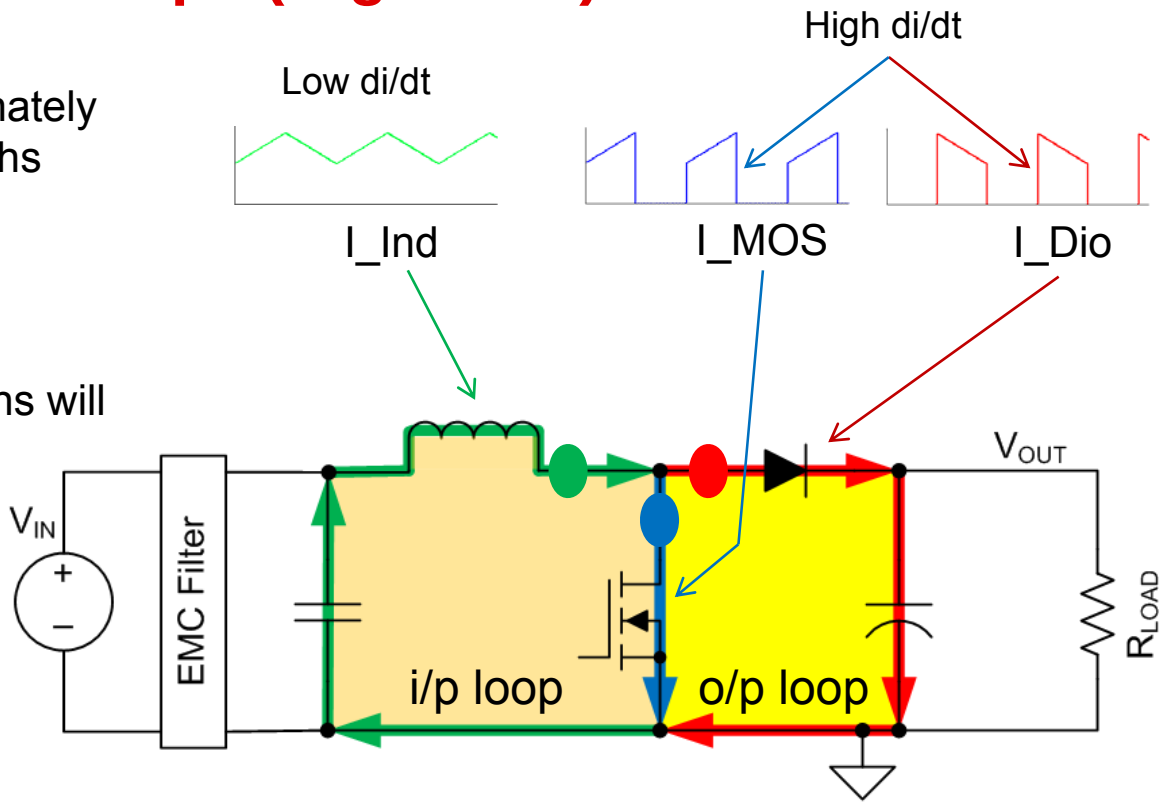
Inductor current is switched alternately between MOSFET and Diode paths

- Pulsating currents in Diode and MOSFET paths – o/p Loop (Red/Blue)
- Inductance in the high di/dt paths will cause voltage spikes

i/p loop inductance less critical

- di/dt rates much lower

Cin provides local low impedance source



Simplified schematic of a CCM boost converter

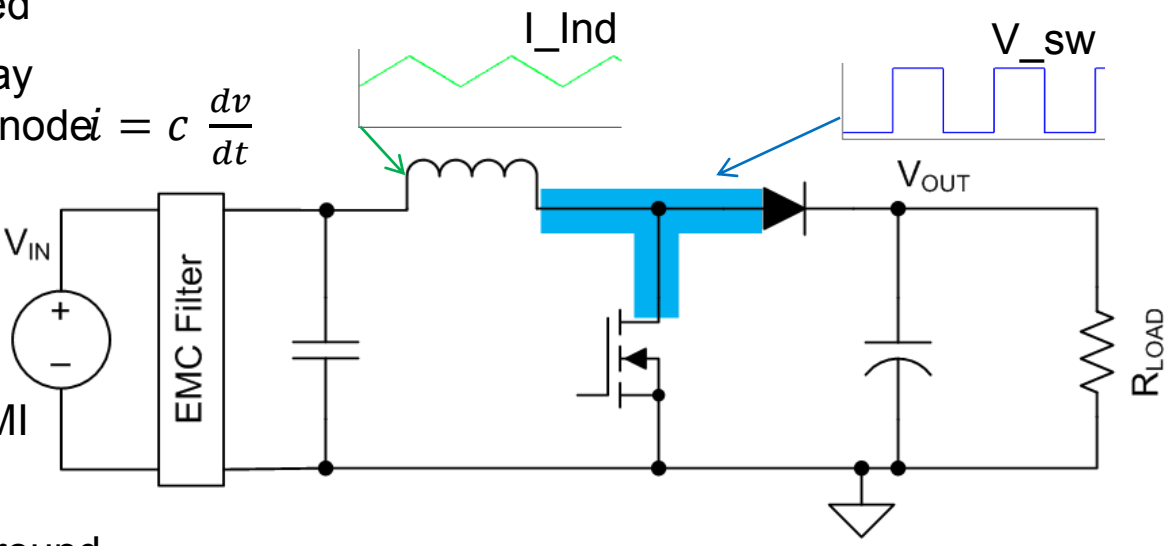
PCB Layout: Switched Nodes (High dv/dt)

High dv/dt at switched node (Blue)

Switched between 0V and V_{OUT}

- High dv/dt rates imply node capacitance MUST be minimised
- Currents proportional to the stray capacitance between switched node and other circuit nodes $i = c\,\frac{dv}{dt}$
- Implies unwanted noise pickup
  - MOSFET Heatsink adds capacitance
  - Floating heatsink => high EMI
  - Ground the heatsink !
- Other nodes are at DC or AC ground

Minimise total conductor area at this node. Short narrow tracks. Inductor, MOSFET and Diode terminals as close together as possible.
Low C much more important than low R.



PCB Layout: Switched Nodes: Gate Drives

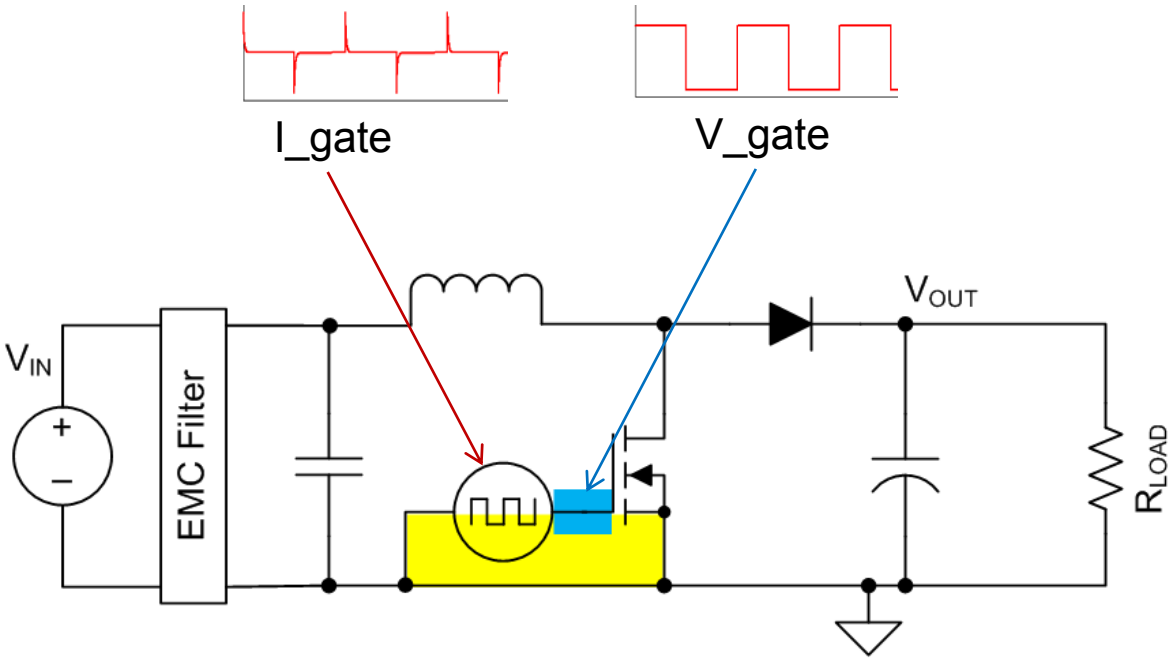
High dv/dt at switched node (blue)

Hi di/dt in gate drive loop (yellow)

- High peak currents
- Minimise loop inductance

Study your schematic

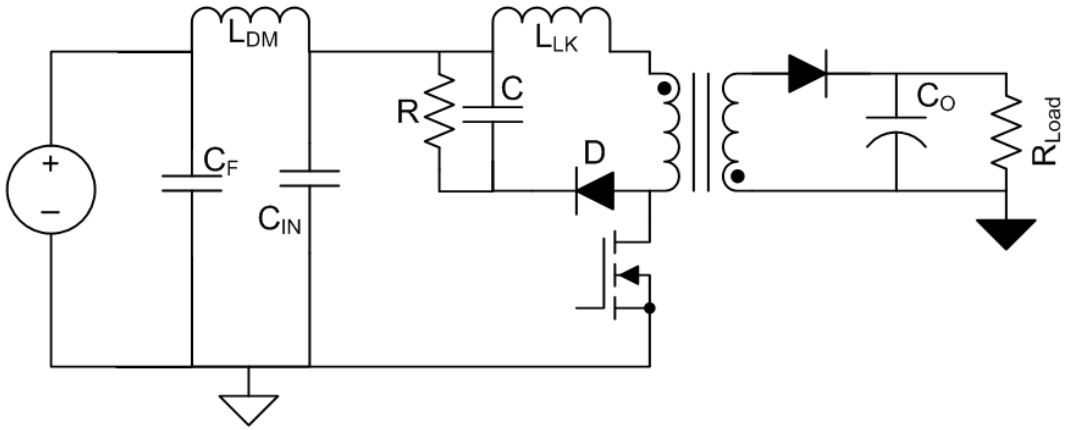
- Know the paths with high di/dt - minimise INDUCTANCE
- Know the nodes with high dv/dt minimise CAPACITANCE



PCB Layout: Switched Nodes: Snubbers

Snubbers absorb unclamped inductive energy

- High di/dt rates with high instantaneous currents
- High dv/dt rates
- High Temperatures due to power dissipation

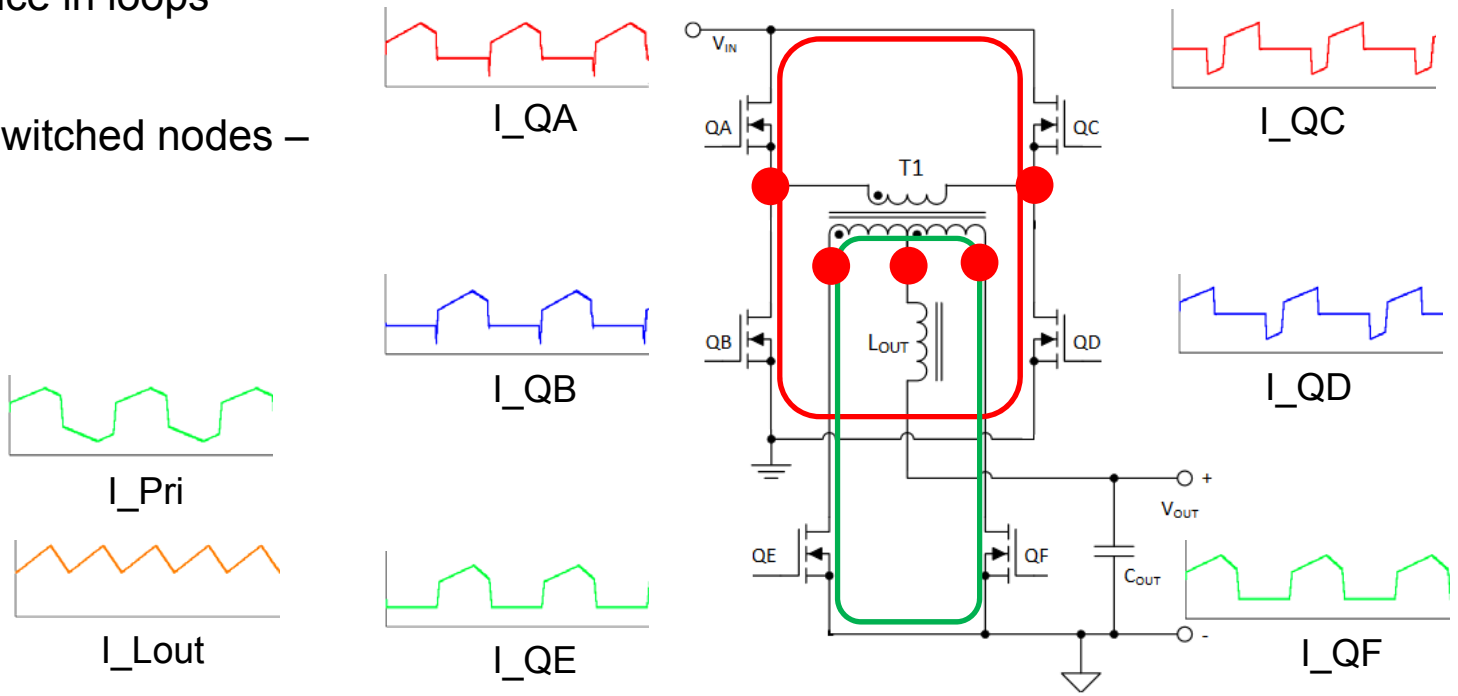


PCB Layout: Phase Shifted Full Bridge

- Minimise inductance in loops

(Red, Green)

- Minimise size of switched nodes – red dots



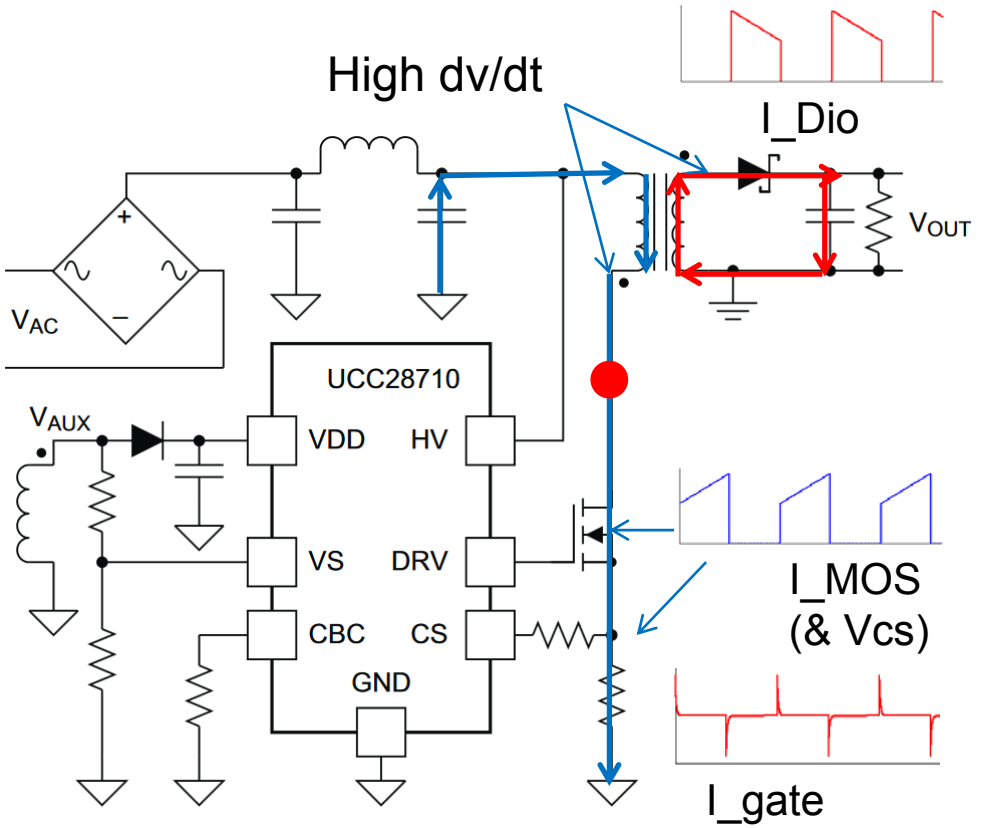
PCB Layout: Flyback

Low power but often used in off line applications where Vin is high

Input and Output currents are pulsating

Gate drive currents as before

High dv/dt rates at the MOSFET drain – red dot



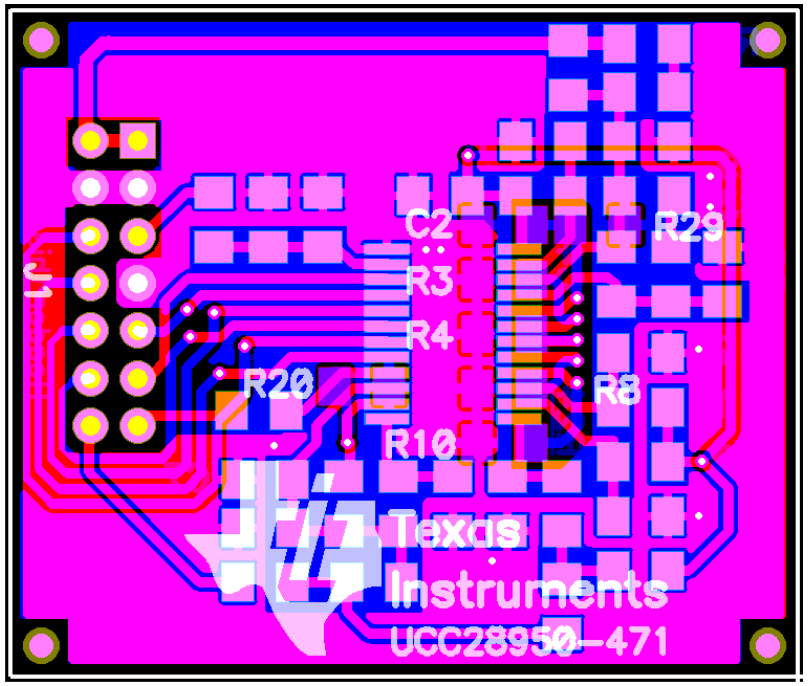
PCB Layout - General

PCB Layout for SMPS

PCB Layout: Layer assignment

How many layers ?

- Single Layer: Lowest cost – consumer goods, TV, domestic appliances etc.
- Two Layer: One signal and one power, ground planes are possible
- Four Layer: Medium complexity digital/mixed signal boards. Two signal and two ground layers. > 4 layers: Luxury !
- Spacing between layers is potentially important
- What process is to be used to build the product – reflow + wave or wave only etc.
- Many constraints on component placement, spacing, orientation etc. etc.



Ground Planes:

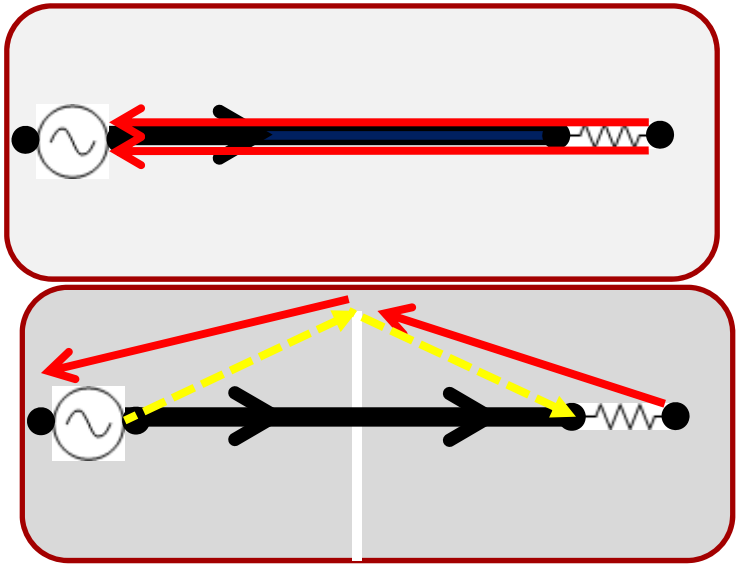
Ground Plane – an infinite, equipotential surface

When is a ground plane not a ground plane ?

- When it has a slot in it – current has to flow around the slot – increased loop area, increased Inductance and impedance
- When the currents flowing cause significant voltage drops (Significant depends on context)

Use under ICs to provide E field screening and clean GND reference

Currents flow in the lowest impedance path – black is outward current on a top side track, red is the return current in the ground plane



Yellow is a better top side routing around a slot

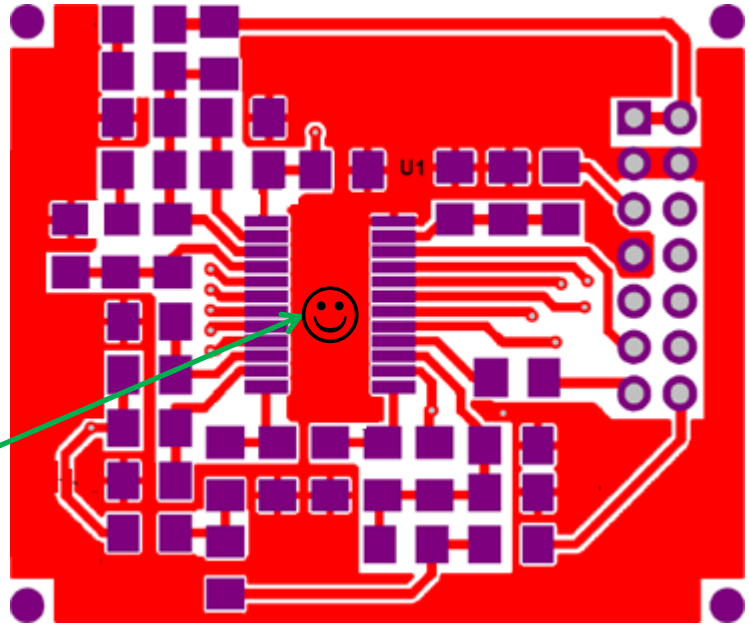
Ground Planes:

Don’t put slots in the ground plane

- Or if you do be careful

Ground planes are not possible on a single sided board

- Take extra care to minimize the impedance in the ground connections in a Single Sided Board
- Low impedance from AGND to PGND is desirable
- Place as much grounded copper under the IC as possible
- Remember that DC tracks are an AC Ground



PCB Layout: Noise Pickup

Stray Capacitance couples noise onto sensitive nodes –

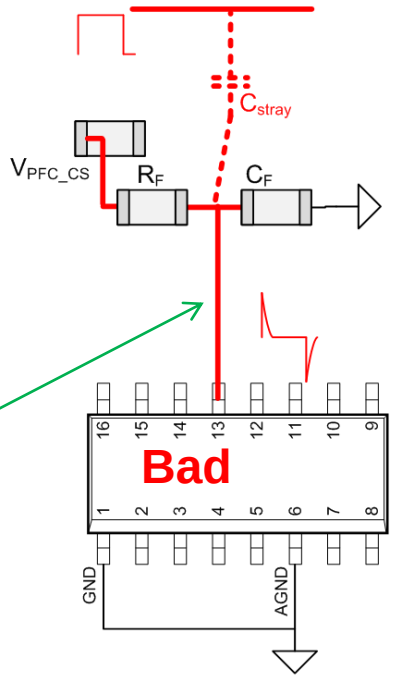
- V and I sensing inputs, FB pins, Slope Comp, Ramp, Timing Cap etc.

Example – CS signal

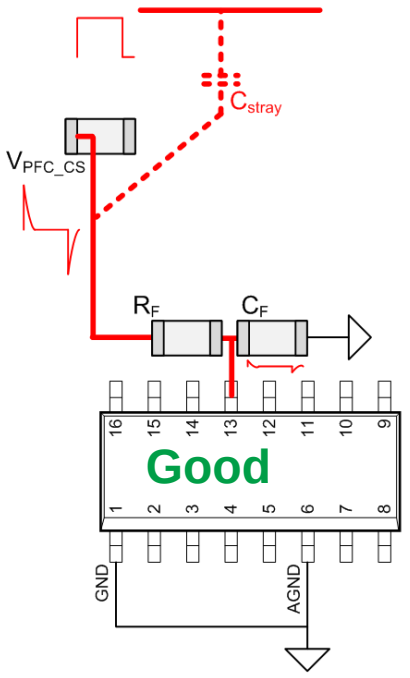
- Place R_F and C_F AT the IC pins
- Good ground connection from C_F

  Ground connections are ALWAYS important and often neglected
- Minimise the unfiltered track length
- Maximise the separation
  - Move the source, Reduce C_{stray}

C_{stray} couples to long track
R_F, C_F ineffective
Large, noise signal at IC



C_{stray} couples to long track
Noise signal is filtered
Lower noise signal at IC



PCB Layout: Noise Pickup

Stray Capacitance couples noise onto sensitive nodes –

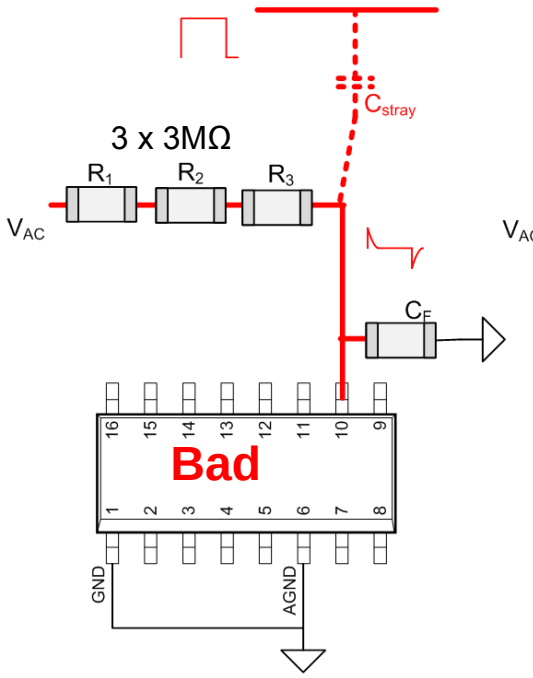
- V and I sensing inputs, FB pins, Slope Comp, Ramp, Timing Cap etc.

Example – CS signal

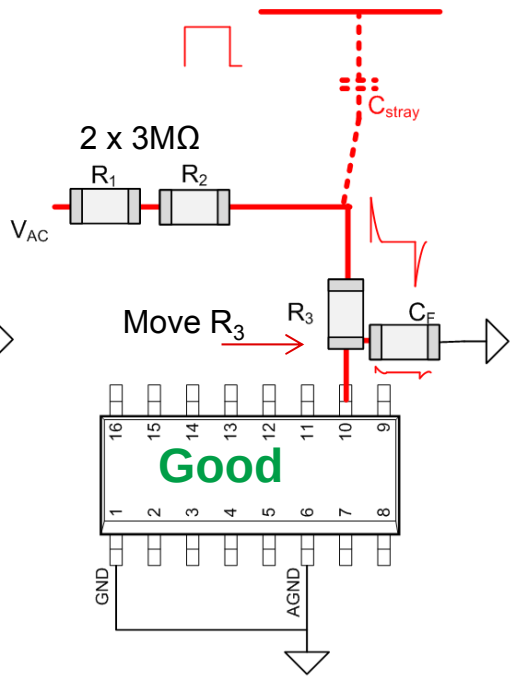
- Place R_F and C_F AT the IC pins
- Good ground connection from C_F

  Ground connections are ALWAYS important and often neglected
- Minimise the unfiltered track length
- Maximise the separation
  - Move the source, Reduce C_{stray}

C_{stray} couples to long track
R_3, C_F ineffective
Some noise signal at IC



C_{stray} couples to long track
Repositioned R_3, C_F effective
Lower noise signal at IC



Parasitics: Trading off L & C

- Capacitance is proportional to the area of the plates supporting the electric field
- Inductance is proportional to the area of the loop enclosed by the current

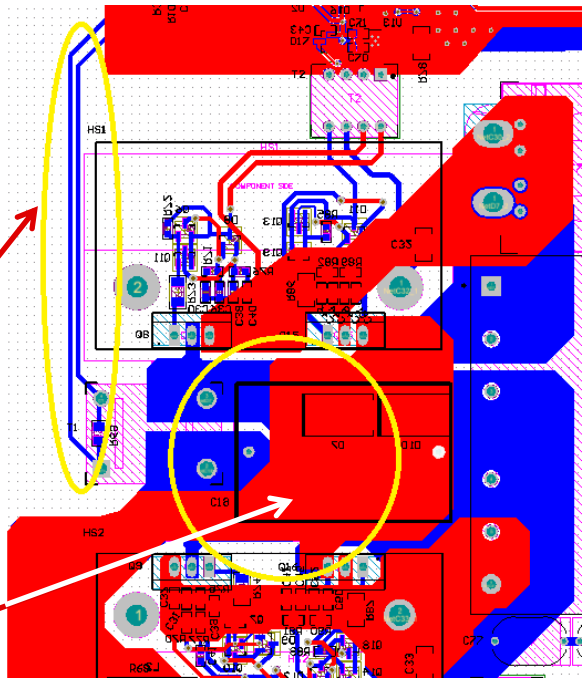
- There is an INHERENT trade-off

Low capacitance tracks will have high inductance

- Long, thin tracks with large signal to ground separation

Low inductance paths will have high capacitance

- Short, wide tracks with minimum area enclosed

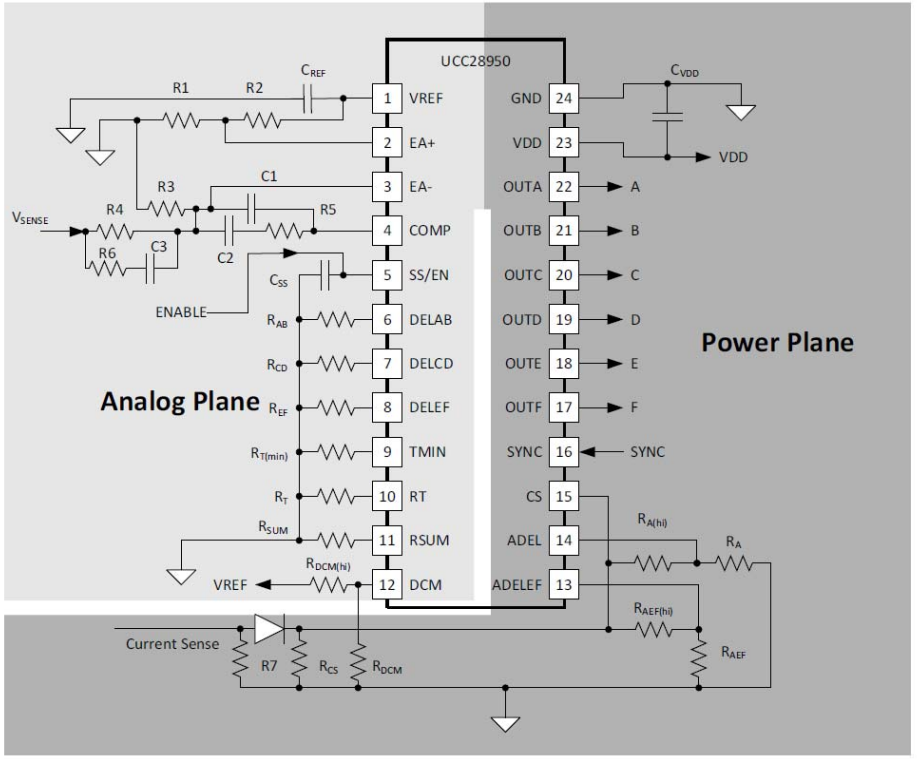


PCB Layout: Tracking

10.1 Layout Guidelines

In order to increase the reliability and robustness of the design, TI recommends the following layout guidelines.

- VREF pin. Decouple this pin to GND with a good quality ceramic capacitor. A 1-uF, X7R, 25V capacitor is recommended. Keep VREF PCB tracks as far away as possible from sources of switching noise.
- EA+ pin. This is the non-inverting input to the error amplifier. It is a high impedance pin and is susceptible to noise pickup. Keep tracks from this pin as short as possible.
- EA– pin. This is the inverting input to the error amplifier. It is a high impedance pin and is susceptible to noise pickup. Keep tracks from this pin as short as possible.
- COMP pin. The error amplifier compensation network is normally connected to this pin. Keep tracks from this pin as short as possible.
- SS/EN pin. Keep tracks from this pin as short as possible. If the Enable signal is coming from a remote source then avoid running it close to any source of high dv/dt (MOSFET Drain connections for example) and add a simple RC filter at the SS/EN pin.
- DELAB, DELCD, DELEF, TMIN, RT, R_{SUM}, DCM, ADELEF and ADEL pins. The components connected to these pins are used to set important operating parameters. Keep these components close to the IC and provide short, low impedance return connections to the GND pin.
- CS pin. This connection is arguably the most important single connection in the entire PSU system. Avoid running the CS signal traces near to sources of high dv/dt. Provide a simple RC filter as close to the pin as possible to help filter out leading edge noise spikes which will occur at the beginning of each switching cycle.
- SYNC pin. This pin is essentially a digital I/O port. If it is unused, then it may be left open circuit or tied to ground via a 1-kΩ resistor. If Synchronisation is used, then route the incoming Synchronisation signal as far away from noise sensitive input pins as possible.
- OUTA, OUTB, OUTC, OUTD, OUTE and OUTF pins. These are the gate drive output pins and will have a high dv/dt rate associated with their rising and falling edges. Keep the tracks from these pins as far away from noise sensitive input pins as possible. Ensure that the return currents from these outputs do not cause voltage changes in the analog ground connections to noise sensitive input pins. Follow the layout recommendation for Analog and Power ground Planes in Figure 45.
- VDD pin. This pin must be decoupled to GND using ceramic capacitors as detailed in the 'Power Supply Recommendations' section. Keep this capacitor as close to the VDD and GND pins as possible.
- GND pin. This pin provides the ground reference to the controller. Use a Ground Plane to minimize the impedance of the ground connection and to reduce noise pickup.



Take a ‘Walk’ around the pins

PCB Layout: Tracking

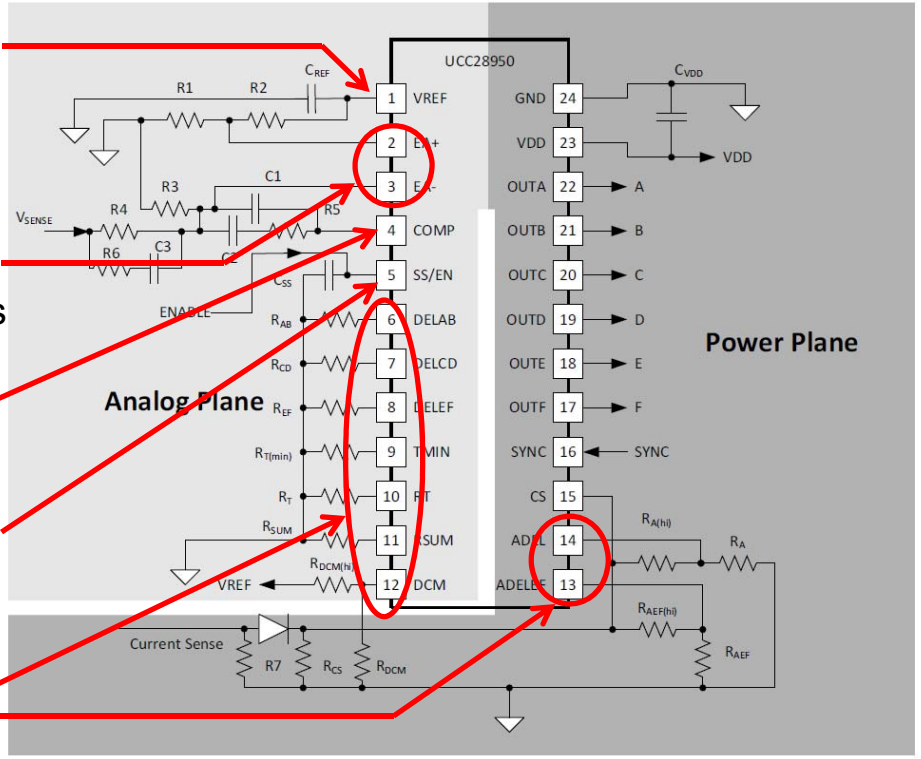
VREF pin. Keep VREF PCB tracks as far away as possible from sources of switching noise and decouple it to GND with a good quality ceramic capacitor.

EA+ and EA- pins. High impedance pins, susceptible to noise pickup. Keep tracks as short as possible.

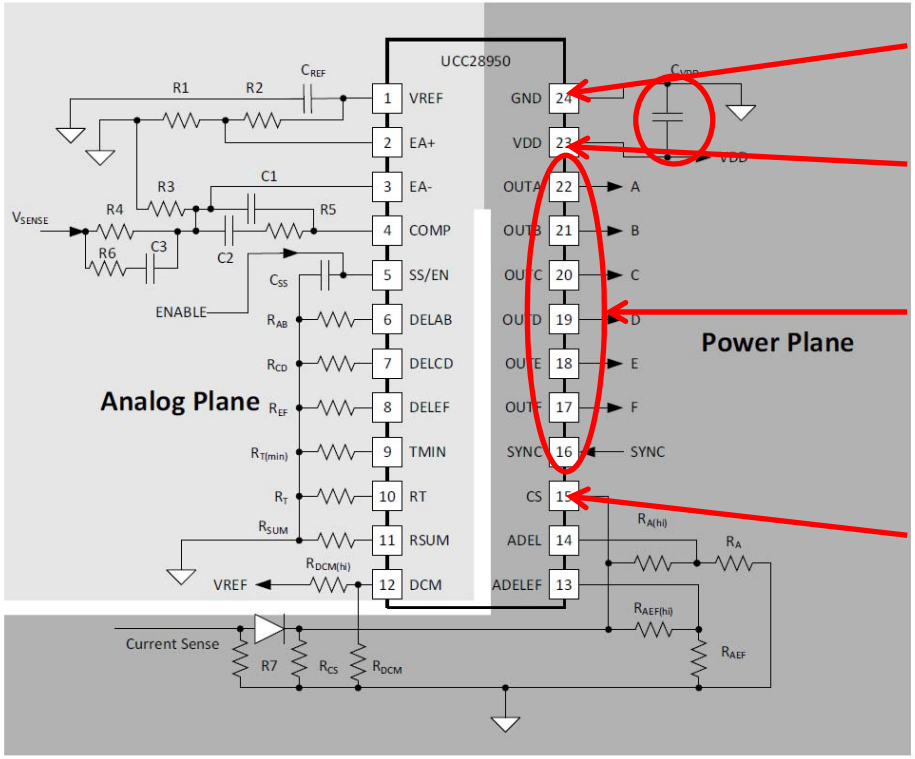
COMP pin. Keep tracks as short as possible

SS/EN pin. Keep tracks as short as possible, avoid running it close to any source of high dv/dt and add a simple RC filter at the pin.

The components connected to these pins set operating parameters. Keep them close to the IC and provide low impedance return paths to GND



PCB Layout: Tracking



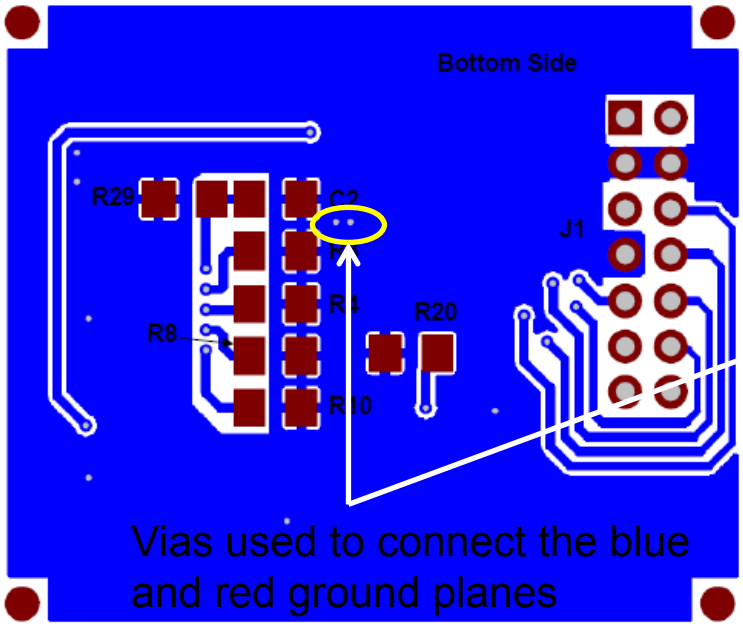
GND pin. Use a Ground Plane to minimize the impedance of the connection here.

VDD pin. Decouple to GND. Keep the capacitor as close to the VDD and GND pins as possible.

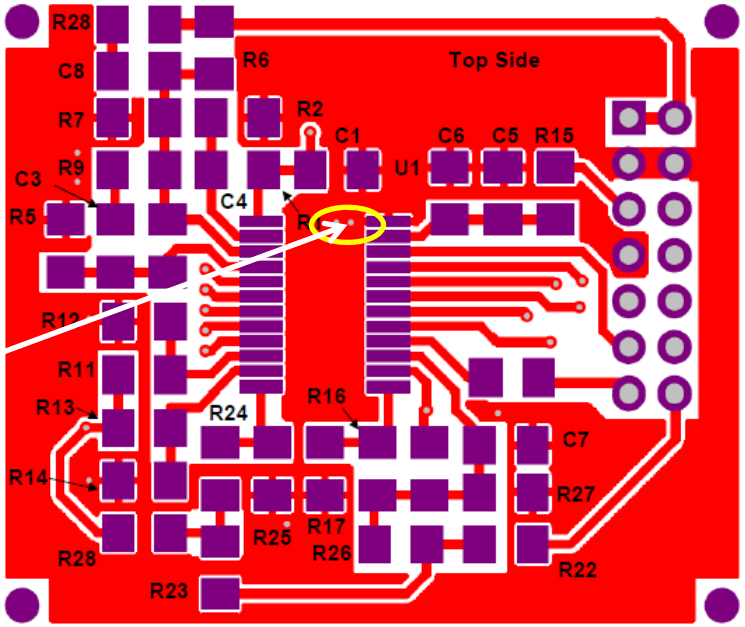
These pins are the gate drive and SYNC output pins and will have a high dv/dt. Keep the tracks from these pins as far away from noise sensitive input pins as possible.

CS pin. This connection is arguably the most important single connection in the entire PSU system. Avoid running the CS signal traces near to sources of high dv/dt. Put a RC filter at (not close to) the pin

PCB Layout: Tracking



VREF pin decoupled to GND (C1), close to the device



VDD decoupling as close to the device as possible. (C6, C5)

OUTA through OUTE signals routed as far as possible from signal pins. (pins 17 through 22)

RC filter close to CS pin. (C7, R27, pin 15)

Short tracks at EA+, EA-, COMP, SS/EN, DELAB, DELCD, TMIN, RT, RSUM, DCM, ADELEF, and ADEL pins. (pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13 and 14)

Add in slide showing stitching vias from one layer to another

PCB Layout: Regulatory requirements

- Safety Agencies will control:
  - The PCB material used
  - Creepage distances – shortest path between two parts along the SURFACE
    - Grooves don't count if less than a certain width
  - Clearance distances – shortest path between two parts through air
    - PCB slots can be used to increase creepage – but not always clearance
  - The use of Basic, Reinforced and Supplementary Insulation
- The Standard is the ultimate reference
- Usually UL60950 / EN60950 / EN 62368-1 or similar, depends on the application

PCB Layout – Effect on EMI

PCB Layout for SMPS

Transformer:

The transformer is the second most complex custom component in the design – after the PCB

Magnetics design has a BIG influence on EMI and performance – Efficiency etc.

Leakage inductance

Wire size and type

Safety Isolation

Physical construction of windings

Core Gapping

Internal Screens between primary and secondary

Some tips for transformers

- Cancellation windings
- Study skin and proximity losses
- Internal Screens from pri to sec
- Grounded 'Belly Bands'
- Quiet ends of windings at outside
- Swap pins to make layout easier

More information at http://www.ti.com/ww/en/power-training/login.shtml?DCMP=psdslibrary&HQS=tlead-power-psdslibrary-apec2015-pwrhouse-20150312-lp-en

Transformer Design:

Transformer is much, much more than simply its turns ratio and magnetizing inductance

‘Belly’ band to reduce external E and H field

Get a DETAILED construction diagram from the manufacturer

Or

Disassemble a sample and STUDY its construction !

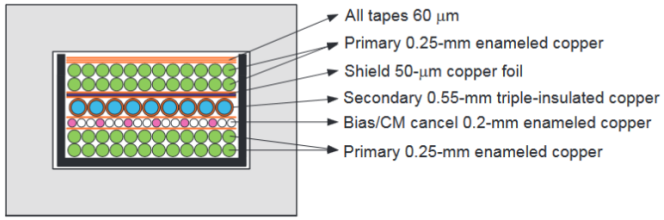


Figure 23. Interleaved flyback transformer winding structure.

Additional information at https://www.ti.com/seclit/ml/slup338/slup338.pdf

Conducted EMI: Common Mode and Differential Mode

CM sources

- Transformer (mainly)

DM sources

- Switched currents, high di/dt
- Switched nodes, high dv/dt

Common mode noise:

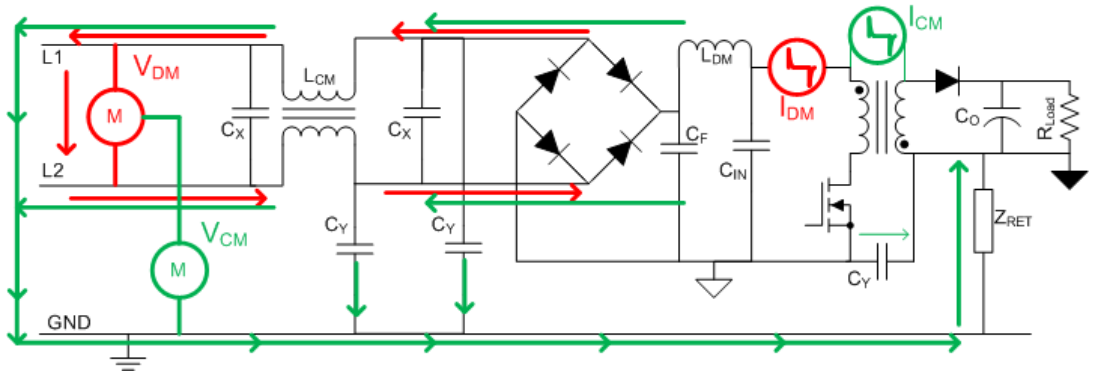
- Three wire system (at least), Out L1, L2 return via GND
- Transformer is main source of CM currents

Good Layout can SIGNIFICANTLY

- Reduce the generated signal
- Improve the Filter performance

Strategy –

- Minimise the source
  - Cheap, but requires thought
- Maximise the filtering
  - Expensive, requires lots of work



Conducted EMI: Common Mode and Differential Mode

Avoid creating parasitic capacitances across the inductors

- Separate the input and output tracks
- Avoid unwanted mutual inductances – eg between L_{CM} and L_{DM} or L_{PFC}

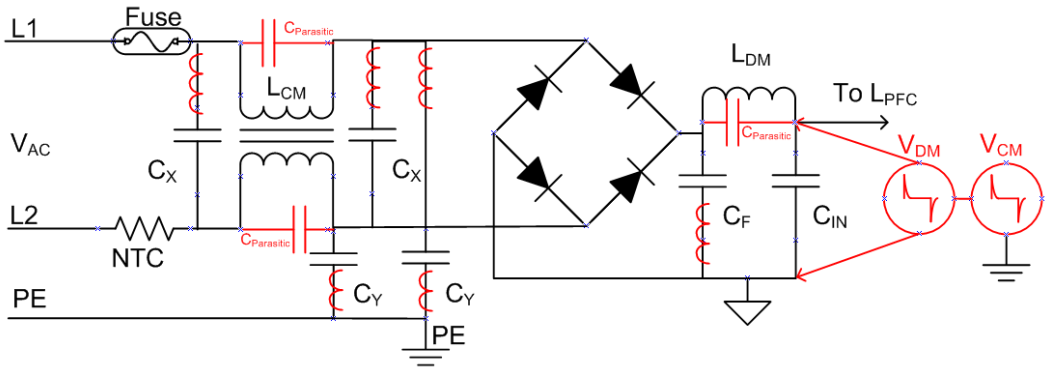
Avoid creating parasitic inductances in series with the capacitors

- Keep leads short

Try to lay the filter out 'in a straight line'

Route tracks directly to pins of Ls & Cs

- C_X , C_Y must have safety approvals
- C_F is a filter capacitor
- L_{CM} is a common mode choke
  - (BALUN)
- L_{DM} is a differential mode choke
- C_{IN} is the PFC input cap



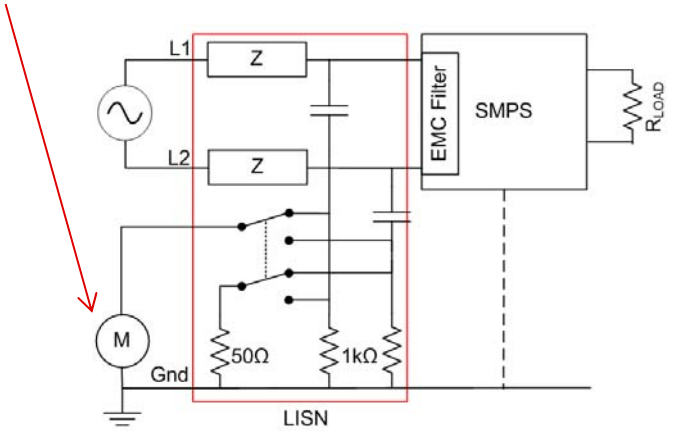
Conducted EMI: Common Mode and Differential Mode

Conducted EMI

LISN provides standard line impedance

L1 and L2 are measured, AVG and QP*

150kHz to 30 MHz



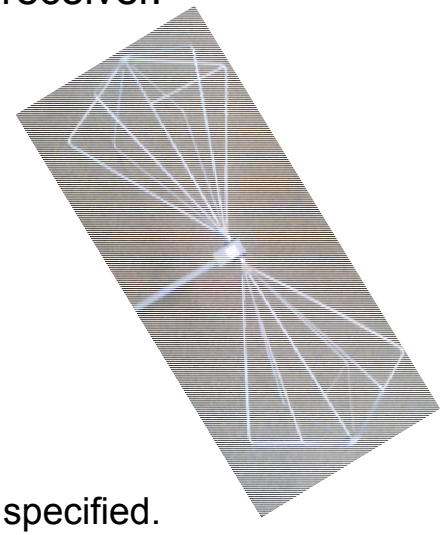
Radiated EMI

Bi-Conic antenna feeds receiver.

30MHz to 1GHz

Vert and Horiz

SMPS in all orientations



3m in Anechoic Chamber
Or
10m Open Air Test Site

*Avg and QP limits are specified.
Mfrs often test AVG and PK
because it is much faster and
if pass PK then pass QP is assured

PCB Layout – An Example

PCB Layout for SMPS

PCB Layout: Givens

PCB size (Too small, but no point in complaining !)

PCB type – layers, layer spacing, material

Position and type of Inlet and Outlet connections

Manufacturing Process – constraints on placement, orientation etc.

Standards to be met – IEC60950 / IEC62638-1 etc.

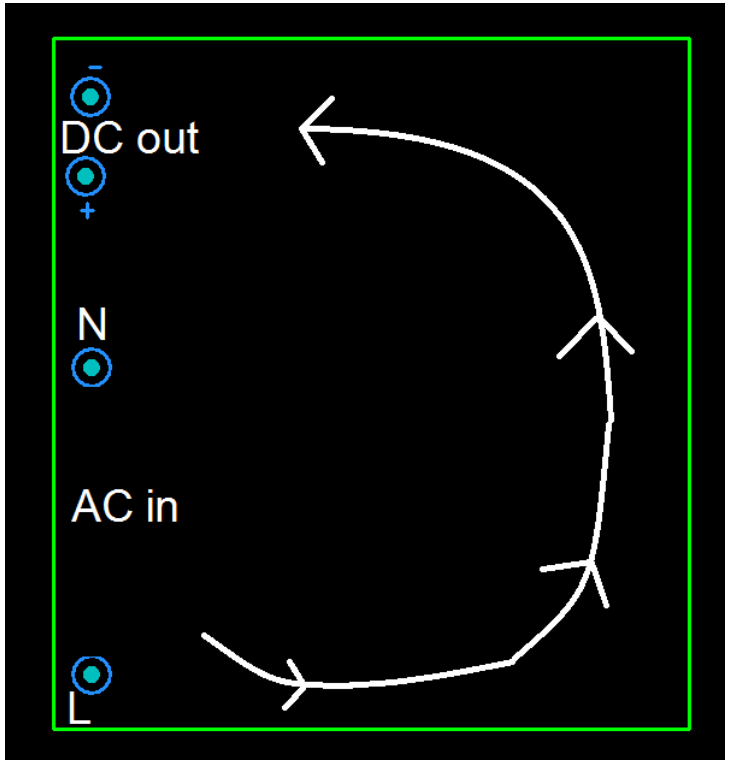
Know which parts are ‘important’ – write down the list

Know which loops and nodes are ‘important’

Know the creepage and clearance requirements

Know the heatsinking and other mechanical constraints

Imagine a general ‘Flow’ and begin to place the large components

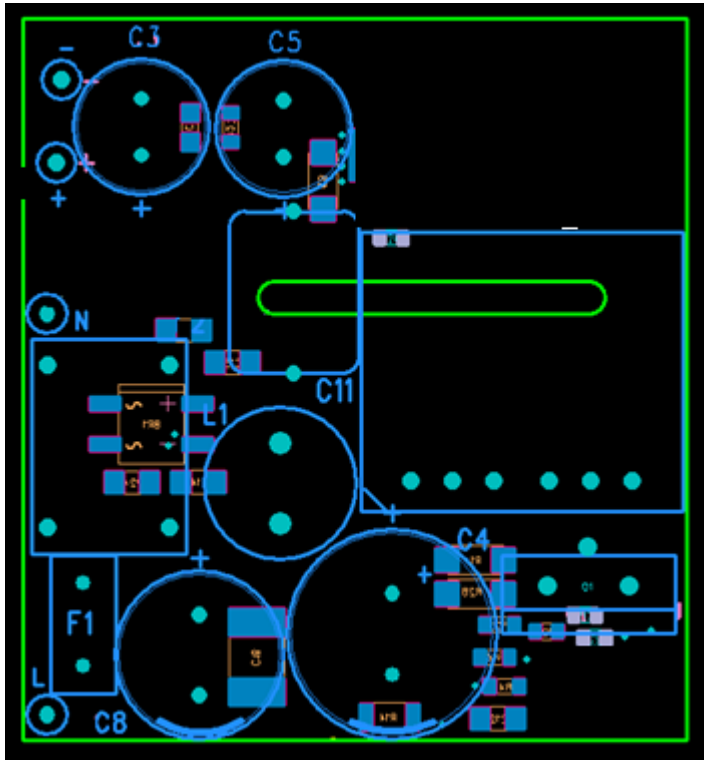


PCB Layout: Component Placement

Place the large parts in the power circuit first

- Trunk Packing Algorithm

Where should the controller go ?



PCB Layout: Component Placement

Place the large parts in the power circuit first

Reserve a ‘quiet’ location for the controller

- NOT under transformer or node with high dv/dt
- Place its associated parts nearby

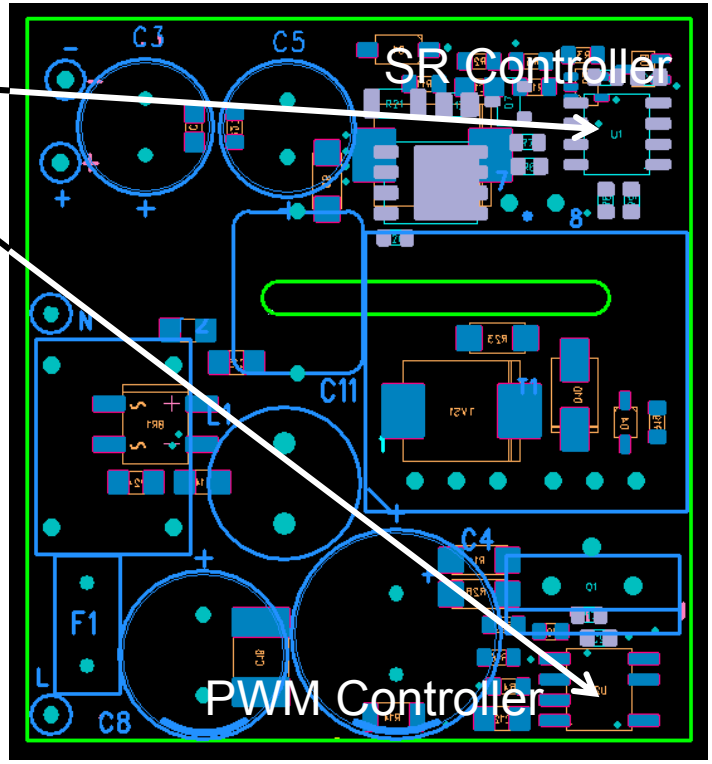
Reserve an area for the input filter

- Keep filter input away from output

Use ‘rats nest’ to simplify connections

- Rotate, Reposition, Reassign pins, Repeat

This is a typical small Flyback layout



PCB Layout: Tracking

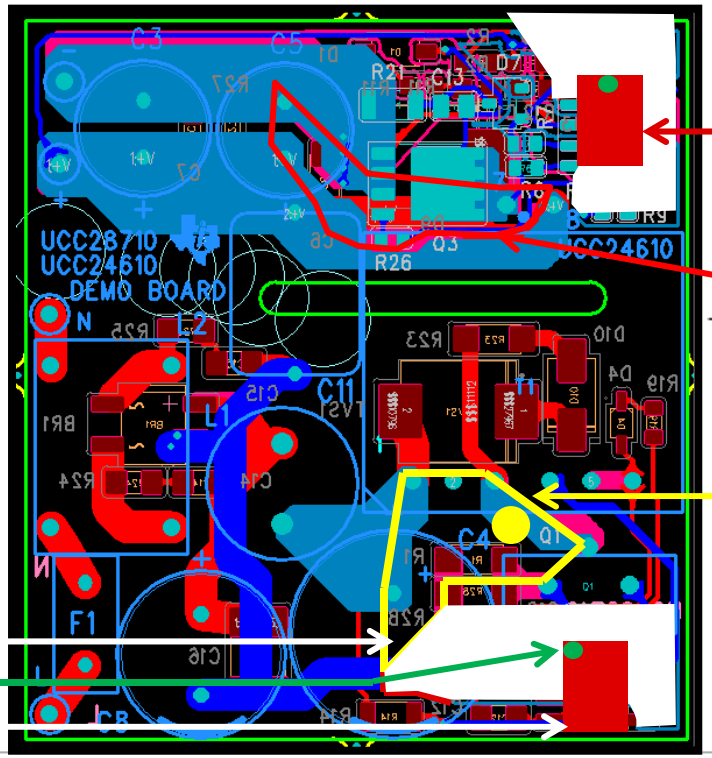
Typical small flyback – 2 layers

Minimise area of current loops

Minimise area of switched nodes

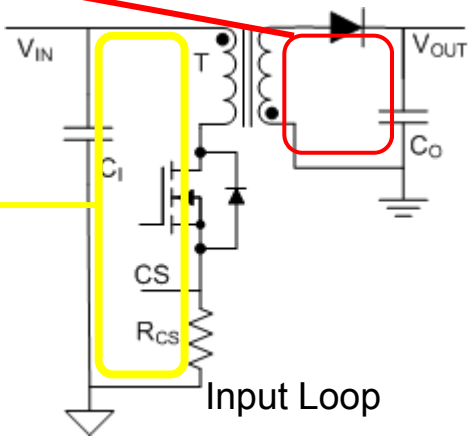
Ground planes under ICs

CS signal and return paths, short and low noise



Gnd Plane in White
SR Drive GND in GRN
SR Controller IC in Blue

Output Loop



Input Loop

Gnd Plane in White
Controller GND in GRN
Controller in Blue

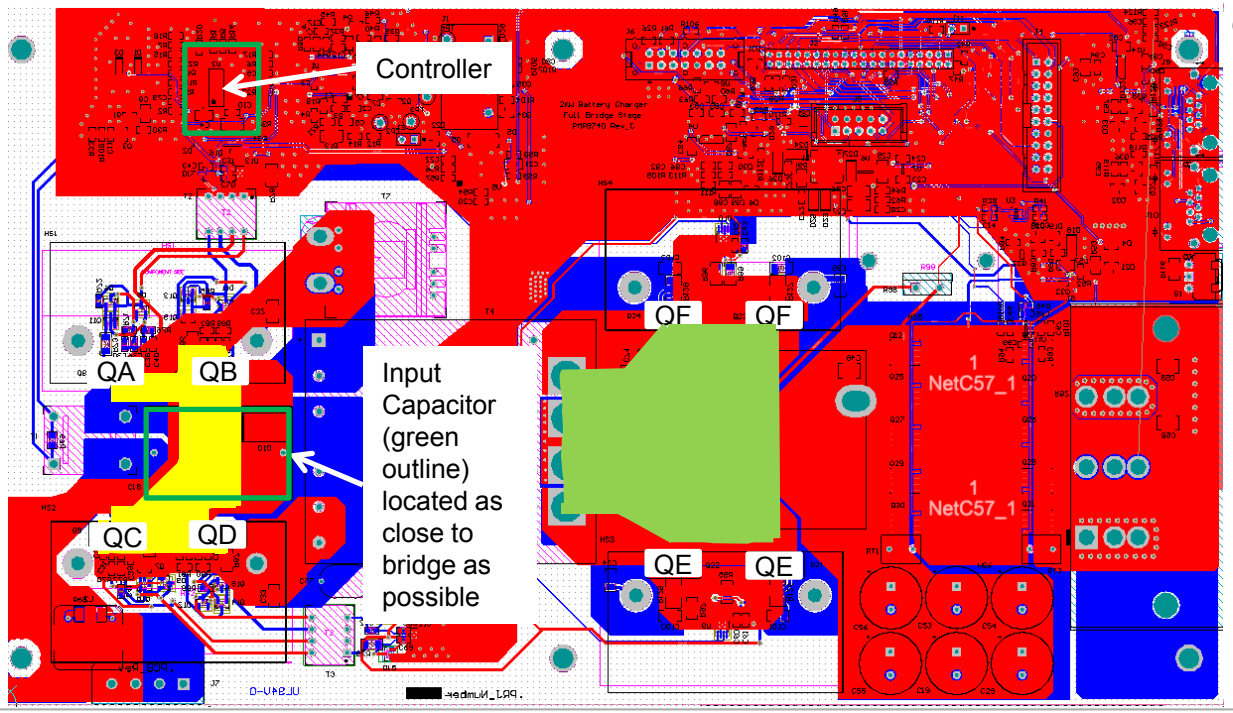
PCB Layout – A Review

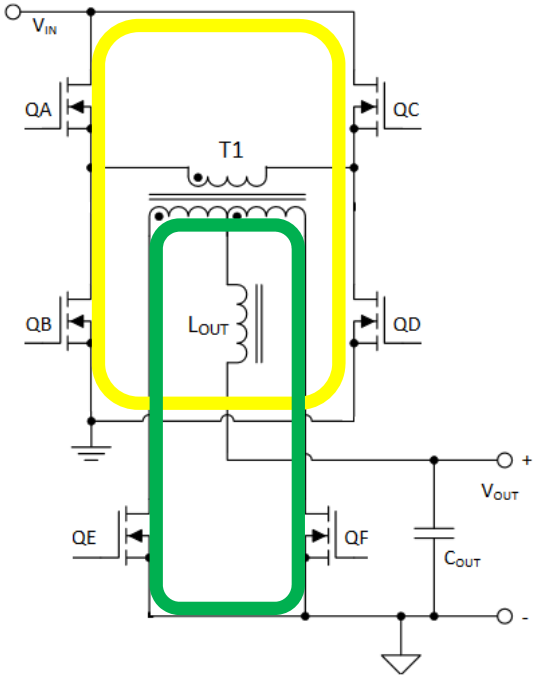
PCB Layout for SMPS

PCB Layout: Review – PMP8740, 2kW PSFB, UCC28950

Use of Ground planes reduces loop impedance

Yellow and Green loops are as small as possible



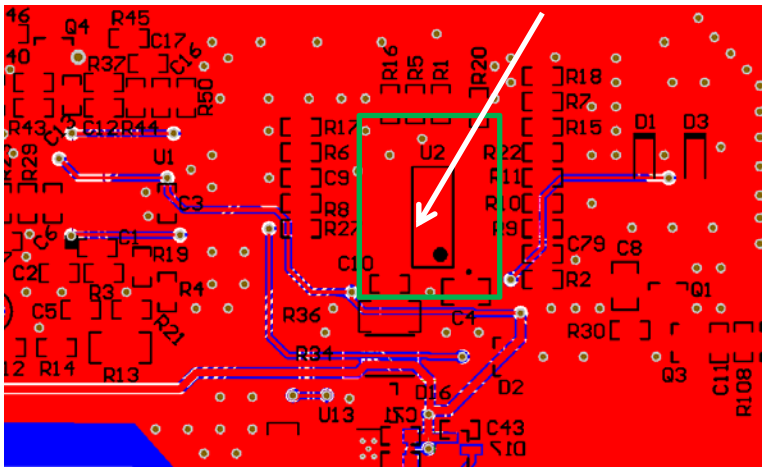


PCB Layout: Review – PMP8740, 2kW PSFB, UCC28950

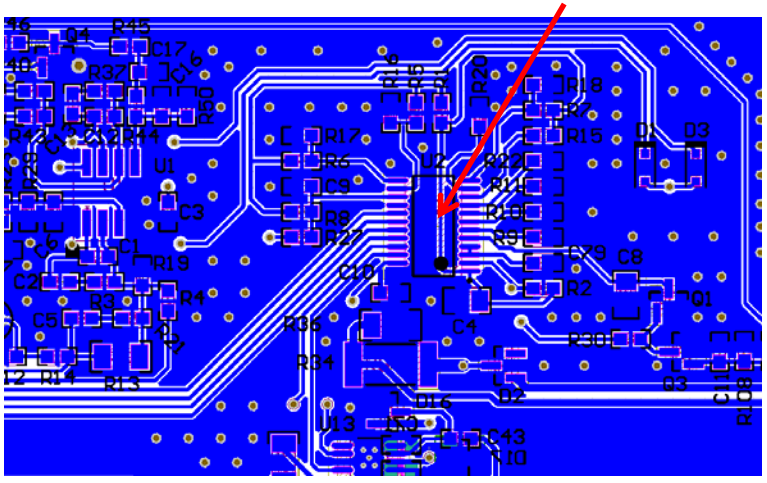
Two layer PCB

Ground plane under controller and associated components

Ground plane
under controller



Ground plane
under controller



PCB Layout: Review – PMP8740, 2kW PSFB, UCC28950

Two layer PCB

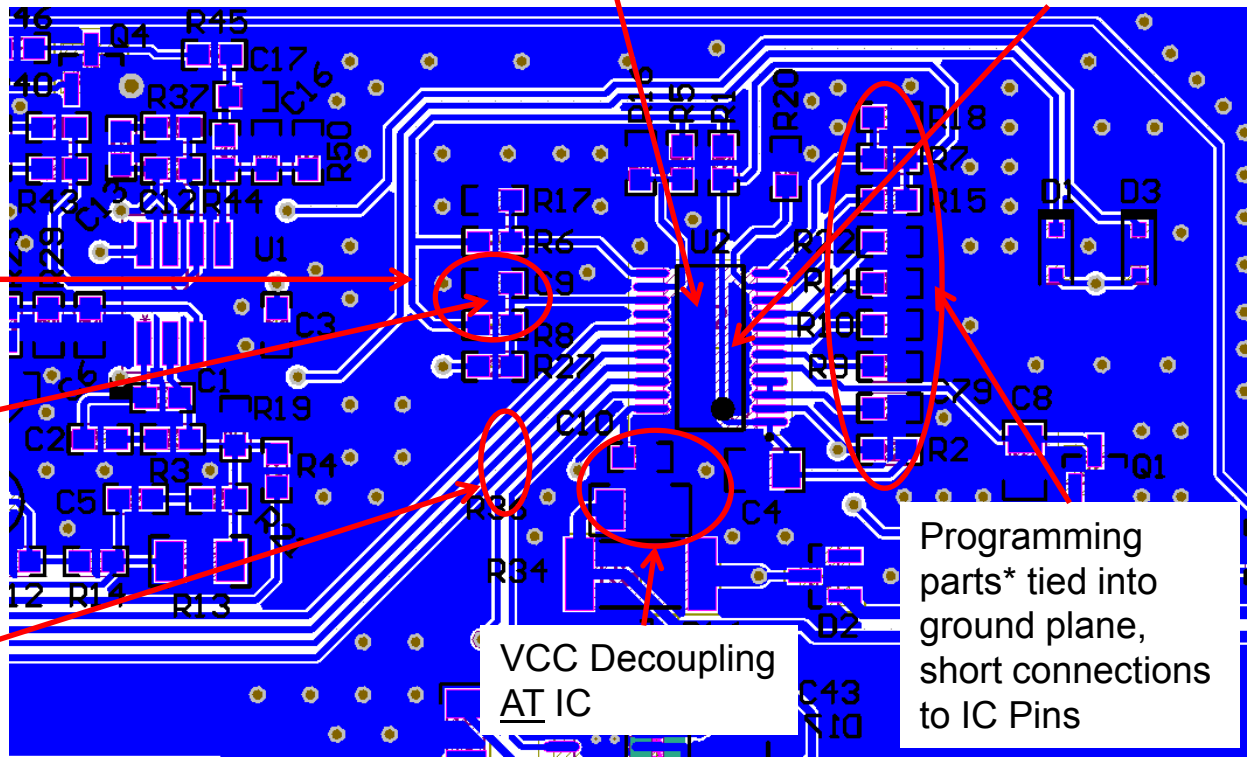
- Bottom Layer

Current Transformer signal,
Away from noisy lines

CS Filtering at CS pin

Gate drives kept away
from input signals

*used to set up Fsw etc.



PCB Layout – Things you don’t have to worry about

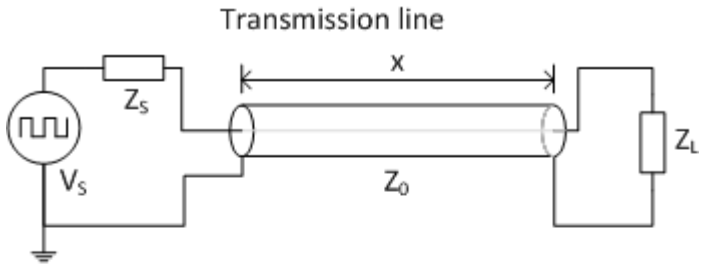
PCB Layout for SMPS

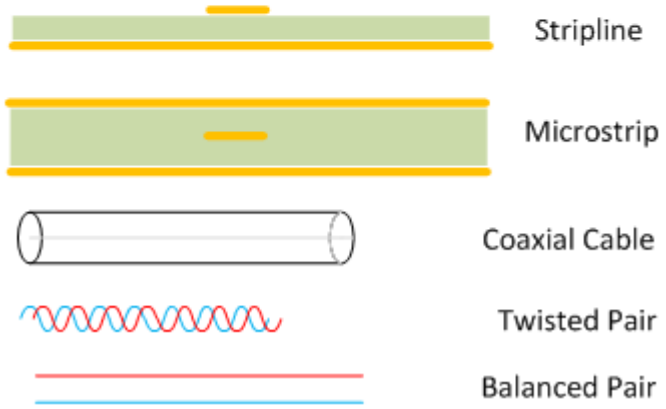
Transmission Lines and Controlled Impedance

Transmission line:

- Length of line is more than about 10% of the wavelength of the highest frequency of interest.

Assume a gate driver with a rise time of 10ns, the highest frequency component is about 30MHz with a wavelength of 10m. Transmission line effects won't be important unless the path is more than about 1m.





PCB Layout: Other considerations

Transmission Line effects

Controlled Impedance

Delay matching

Propagation delay

Speed of Light (30 cm per ns)

None of these are especially important in SMPS layouts but it's worthwhile knowing that they exist.

PCB Layout – Summary

PCB Layout for SMPS

PCB Layout

FINISHED ?

PCB Layout

FINISHED ? NO – a PCB layout is NEVER finished !

Take at least a half a day to review and rework the layout

Reviews ALWAYS improve the board

Use an INDEPENDENT reviewer –

one who can criticize, complain, compliment and help correct the layout.

If you take only one idea from this talk – take this one.

PCB Layout

FINISHED ? NO – a PCB layout is NEVER finished !

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Use an INDEPENDENT reviewer –

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If you take only one idea from this talk – take this one.

(You can always ~~get your revenge~~ return the compliment at a later date !)

Conclusions & Key Take-Aways

- The Schematic shows only some of the components
  - You need to know where the others are
- A full understanding of circuit operation is necessary
- Knowledge of parasitic elements in components AND in PCB tracks is key
- PCB Layout must take account of parasitic Inductance, Capacitance, Resistance
- EMI results are significantly affected by:
  - Transformer design, power circuit and input filter layout
- REVIEW, RELAYOUT, REPEAT – Before you build the board

References:

- PMP8740 design review at: https://www.ti.com/seclit/ml/slup349/slup349.pdf
- Ground Planes: http://www.ti.com/lit/an/slyt499/slyt499.pdf and http://www.ti.com/lit/an/slyt512/slyt512.pdf
- PCB Design Guidelines for Reduced EMI: http://www.ti.com/lit/an/szza009/szza009.pdf
- The PCB is a component of op amp design: http://www.ti.com/lit/an/slyt166/slyt166.pdf
- Blog: http://e2e.ti.com/blogs_/b/powerhouse/archive/2016/10/03/why-should-i-count-squares

Thank You

Colin Gillmor

Conducted EMI - Dithering

- EN55022 Class B Conducted Emissions – 150kHz to 30 MHz (there are others)
- Peak, Average and Quasi-Peak detectors
- Quasi-Peak – 1ms charge, 160ms discharge – energy has to remain outside of the QP receiver bandwidth (9kHz) for a long time if QP response is to be reduced
- Peak – no reduction with Dithering
- QP – little reduction
- Average – reduction with Dithering (probably)
- Dithering is a very complex topic – see 'Understanding Noise-Spreading Techniques and their Effects in Switch-Mode Power Applications', Rice et al. slup269