TECH DAYS
Texas Instruments

Hands On with TI's Free SPICE tool "TINA-TI"

(Beginner to Advanced in 30 minutes)

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Milwaukee Wisconsin

Hands on with TI's Free SPICE Tool "TINA-TI"

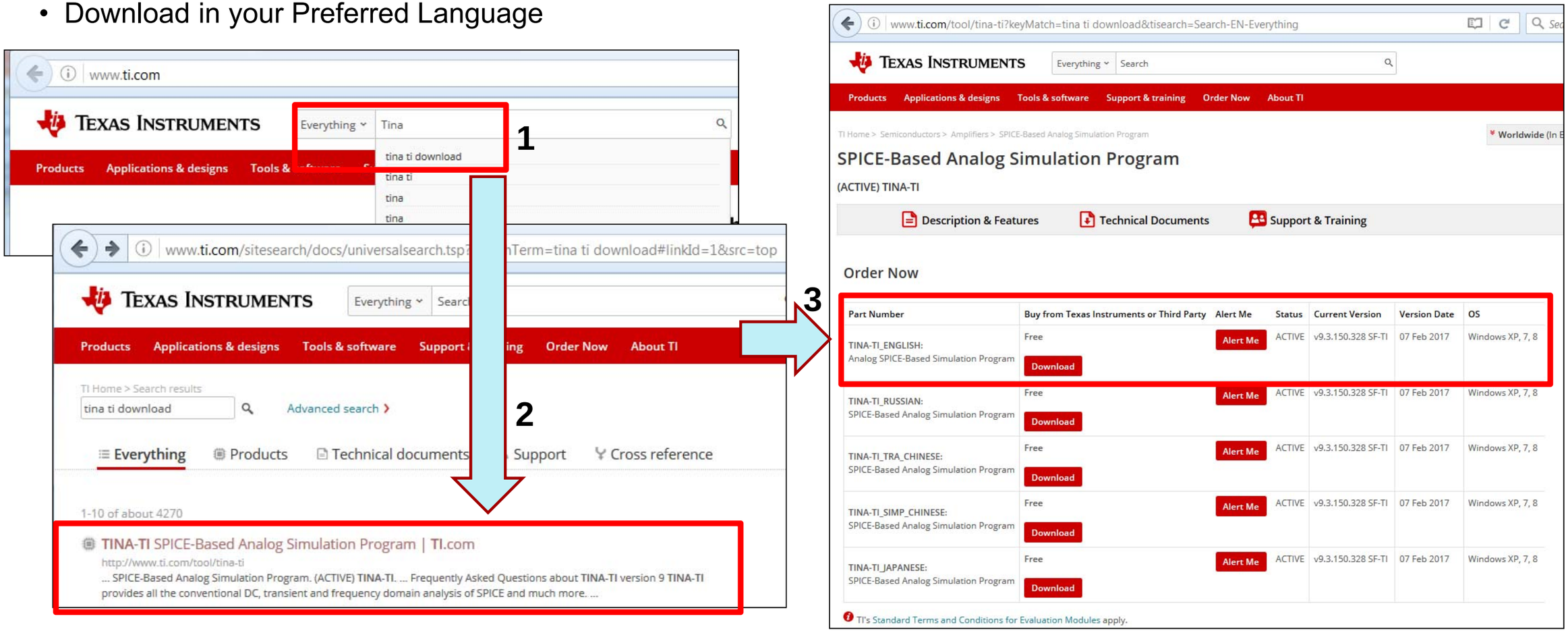
TECH DAYS
Texas Instruments

- Installing The Software
- Finding and Placing Components
- Example Circuits in TINA-TI
- "Trust but Verify" method for op amps.
- Average Model, Transient Model and Green-Lis
- TI ONLINE Precision Labs Training
- Get Models at WWW.TI.COM/SPICERACK
- Using a component already in TINA
- How to Import a .TSM File
- How to Import a .LIB File
- Results Window Overview
- Enable Instant Diagram Drawing
- Electric Rules Check
- Offset Voltage Measurement
- Transient Analysis Input / Output Voltage Swing
- Bandwidth testing
- Slew Rate
- Noise Analysis
- Voltage Generator as a Square Wave
- Voltage Generator as a Triangle Wave (Example Circuit)
- Voltage Generator as a Piecewise Linear Source
- Phase Delay Calculation
- Stability Calculation
- Adding and Removing Variable Sweep Feature
- Change Axis in Results Window
- SEPIC Converter Example LM5022 (Transient Model)
- Flyback Converter Example
- Adjusting Analysis Parameters when necessary
  - Will Not Converge / Need More Resolution
  - Capacitor on Operation Amplifier Input Causes Convergence Error
  - Need More Memory
  - Output Waveform is Truncated

TI E2E Online Support:
https://e2e.ti.com/support/development_tools/webench_design_center

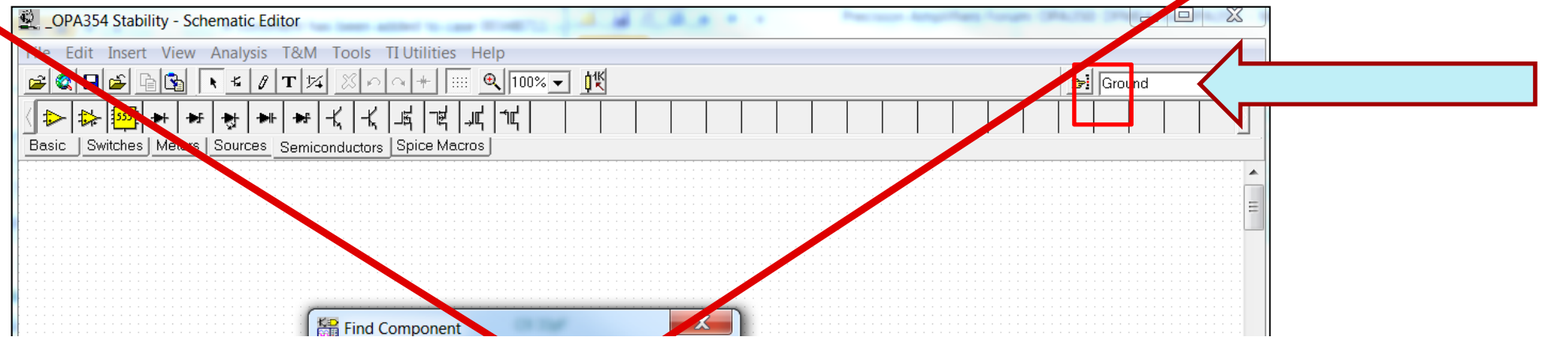
Installing Tina-TI

- Search Tina from www.ti.com
- Choose “tina ti download” link
- Choose Link: TINA-TI SPICE-Based Analog Simulation Program | TI.com
- Download in your Preferred Language



Components Already in TINA

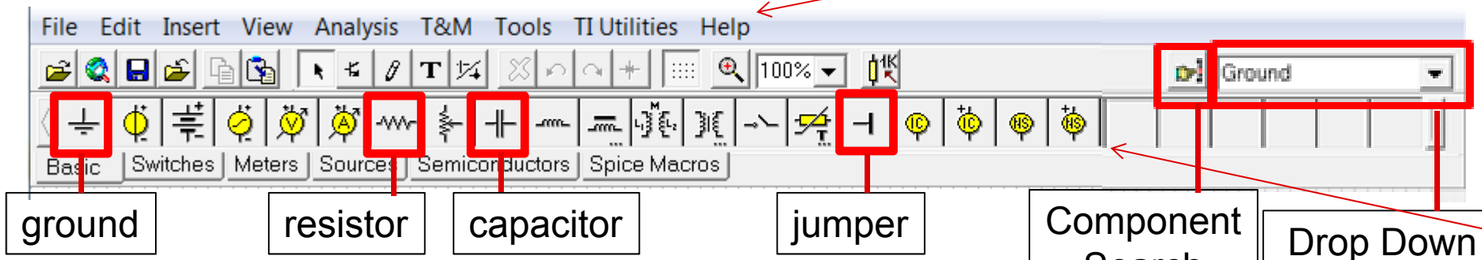
- Click on the Hand Symbol, Far Right, and Search OPA354



USE THE NEWEST MODELS FROM TI.COM

START WITH **.TSC** FILE IF POSSBILE

Getting Started



ground

resistor

capacitor

jumper

Component Search

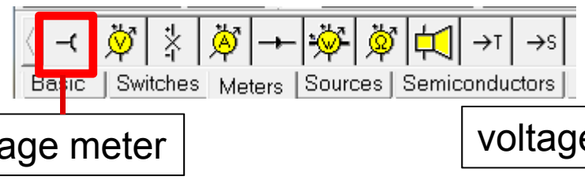
Drop Down for all these components

Top Row (Menus):
Commands associated with files, types of analysis, Test and measurement options, and help

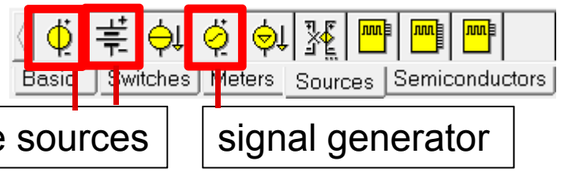
Second Row (Icons):
File operations, text, hide and wiring feature selection, etc

3rd and 4th rows (Icons and Tabs):
3rd Row icons select component type
4th row tabs select component group

toggle switch



voltage meter



voltage sources

signal generator

diode

zener

schottky

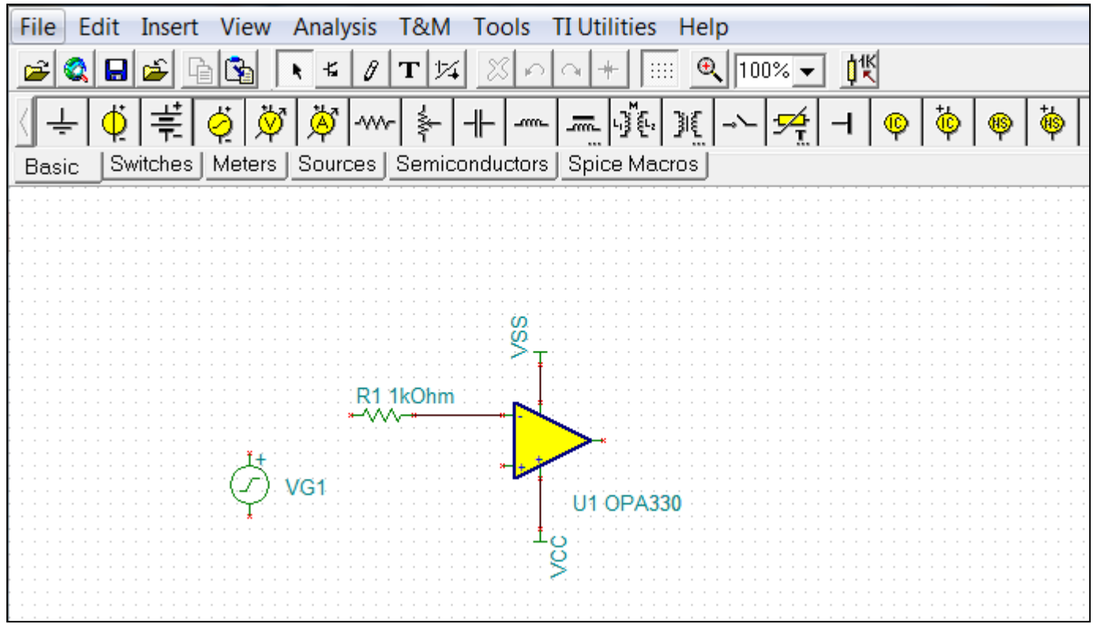
NFET

PFET

Op Amp

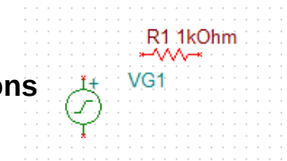
Example: Placing components & Wiring Tool

- Go to Spice Macros and Choose Operational Amplifier 
- Scroll Down to OPA330
- Choose a Resistor from the Basic Tab 
- Choose Signal Generator from Sources Tab 
- Add a Jumper for VCC and VSS to connect to other parts of the circuit 
- Practice using Wiring tool with
  1. Space Bar
  2. Hover over Red X
  3. Might need to hold down on right mouse button to draw



TIP: Wiring Tool

- **Hover over Red X on component for Wiring Tool**
- **Use Space Bar to Start Wiring Tool**
- **Choose Pencil from Second Row Icons**
- **Insert → Wiring from Menus**
- **Hold down on Right Mouse Button to keep Wiring Tool Up (if necessary)**



TRUST BUT VERIFY

- On TI's E2E Forums
- https://e2e.ti.com/blogs_/b/analogwire/archive/2017/07/27/trust-but-verify-spice-model-accuracy-part-1-common-mode-rejection-ratio-cmrr

"Trust, but verify" SPICE model accuracy, part 1: common-mode rejection ratio

SPICE simulation is an immensely valuable tool that allows engineers to have high confidence in their analog designs before ever stepping foot in a lab. While many of us live and die by our simulation results, have you ever stopped to question if your favorite operational amplifier's (op amp) SPICE model matches the specs promised by its data sheet?

Our competitors' models can often be inaccurate or oversimplified, as shown in the closed-loop output impedance (Zout) comparison in Figure 1. In this case, it's easy to see the difference between what's promised and what's measured. This difference can have a big impact on your designs, potentially causing some unwanted surprises when you fire up your circuit in the lab for the first time.

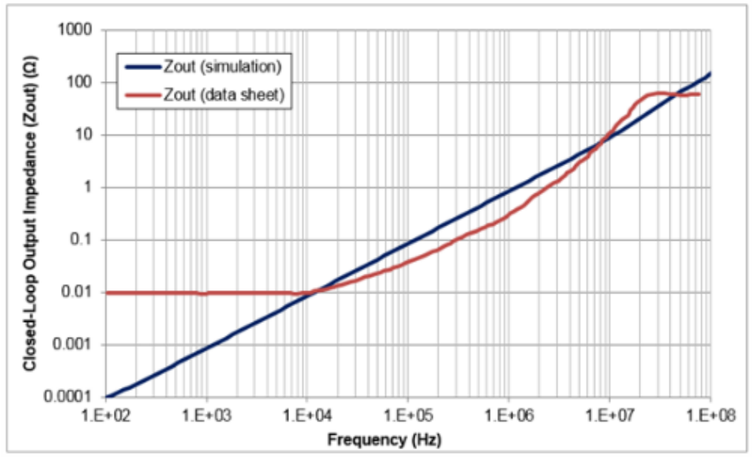


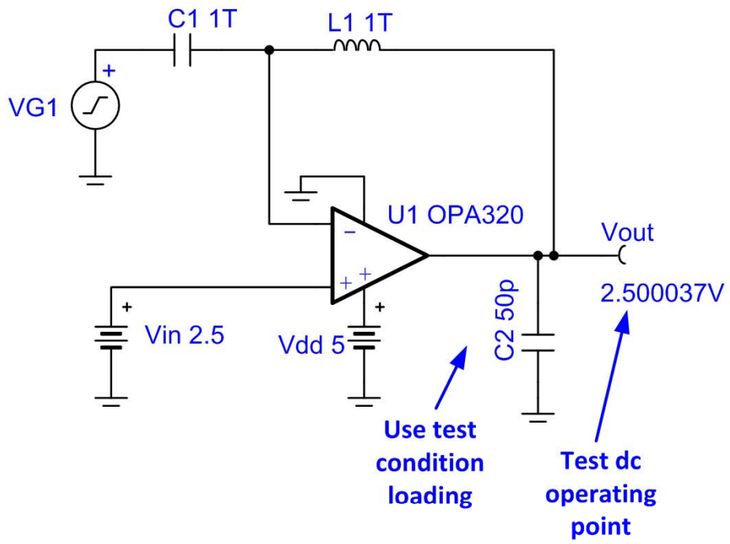
Figure 1: Competitor SPICE model Zout comparison

TI is proud to have some of the most accurate SPICE models in the industry. That being said, it's still a good practice to "trust, but verify" that the models used in your circuit are up to the task. In this blog series, I will show you the recommended test circuits for many of the most critical op amp parameters, starting with common-mode rejection ratio (CMRR).

An op amp's CMRR is formally defined as the ratio of its common-mode gain to its differential-mode gain. In practical terms, the CMRR spec tells you how much additional offset voltage is generated at the op amp's input when the input common-mode voltage changes. A high CMRR is desirable, meaning that you'll see less additional offset voltage. CMRR also changes over frequency, so TI data sheets provide a curve representing typical CMRR over frequency, as shown in Figure 2. For a deeper discussion of CMRR and its impact on circuit performance, watch our TI Precision Labs – Op Amps video on CMRR.

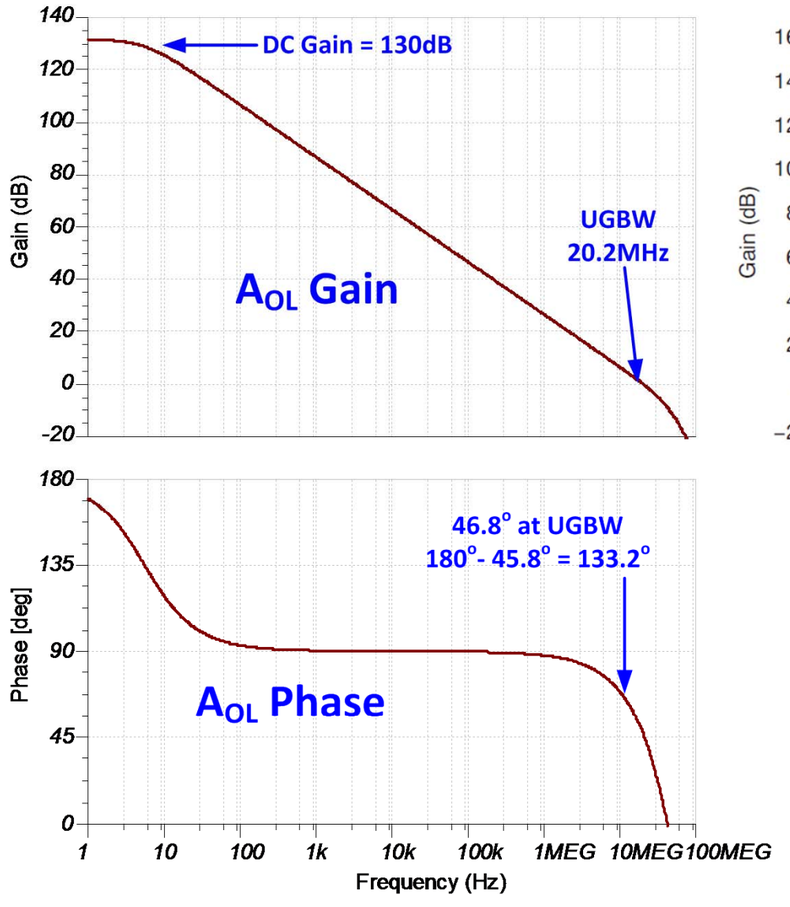
Op Amp Model: Open Loop Gain

Test Circuit for Aol

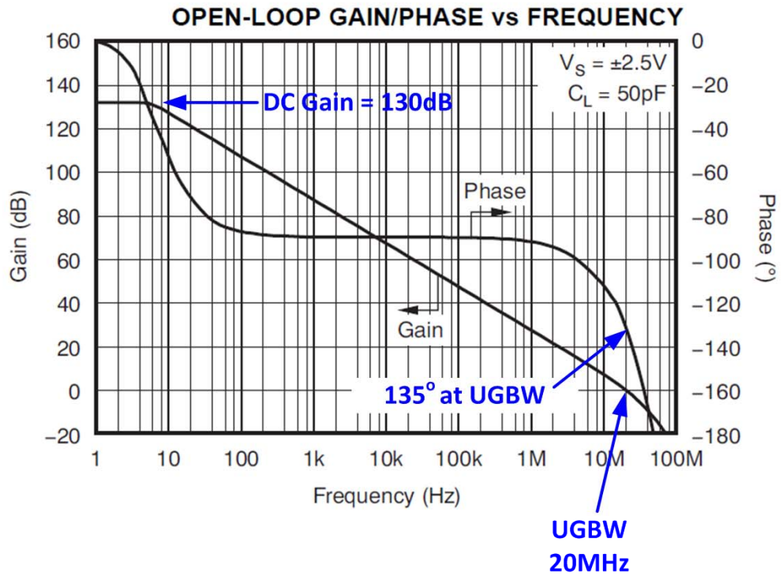


1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for A_{OL} curve
   A_{OL} = Vout

Simulated results



Data Sheet Specification

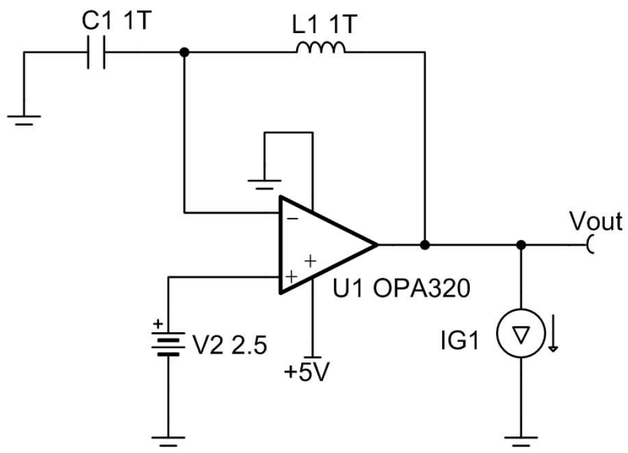


Compare key points on simulation results to data sheet curve.

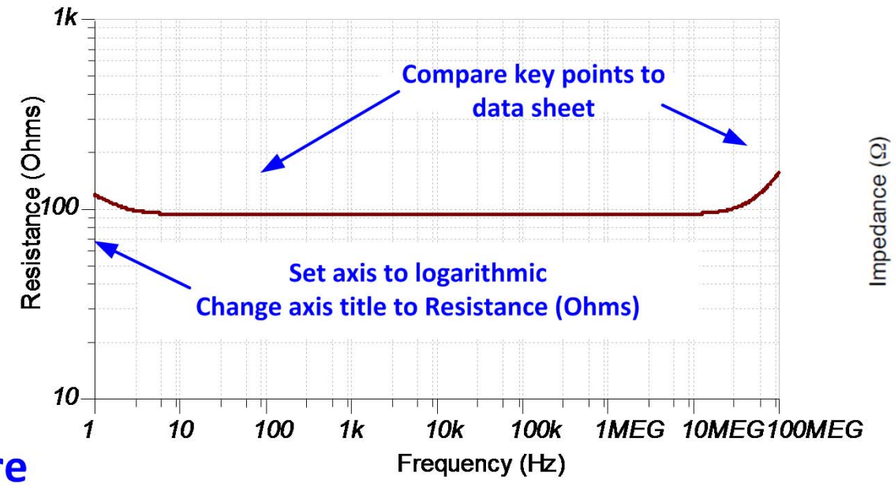
Aol opa320_TG.TSC

Op Amp Model: Open Loop Output Impedance

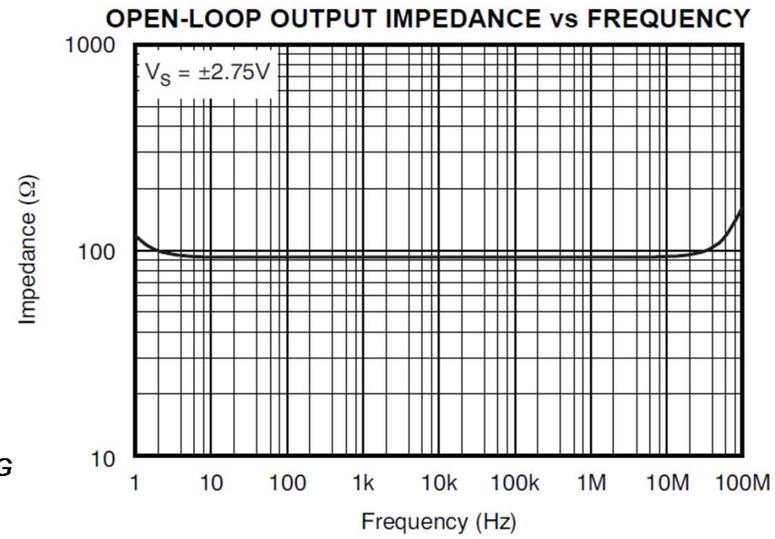
Test Circuit for Aol



Simulated results



Data Sheet Specification



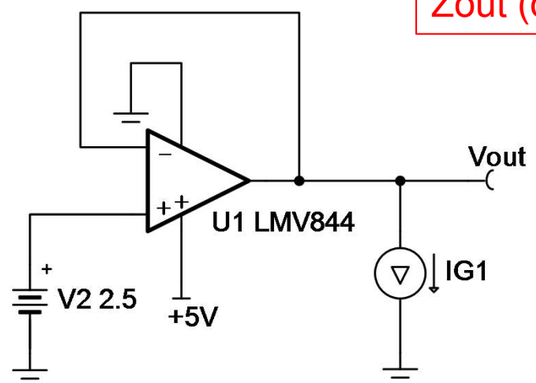
1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for Z_o curve.

Zo(dB) = Vout(dB)
Zo(ohms) = Vout(Logarithmic)

Zo opa320_TG.TSC

Op Amp Model: Closed loop output impedance

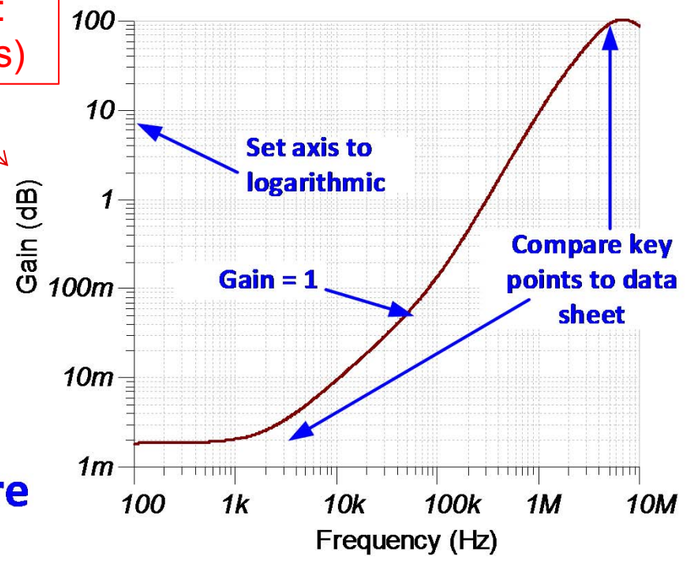
Test Circuit for Zout



Should Be:
Zout (ohms)

1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for Z_{out} curve. Z_{out}= Vout.
3. Change the vertical axis to logarithmic scale

Simulated results



Zout(dB) = Vout(dB)
Zout(ohms) = Vout(Logarithmic)

Data Sheet Specification

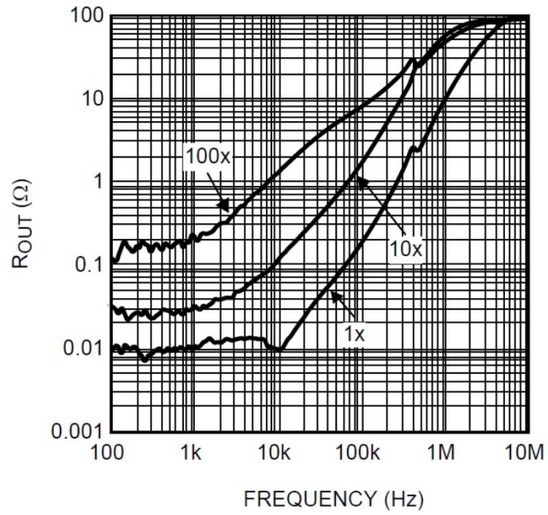


Figure 33. Closed-Loop Output Impedance vs Frequency

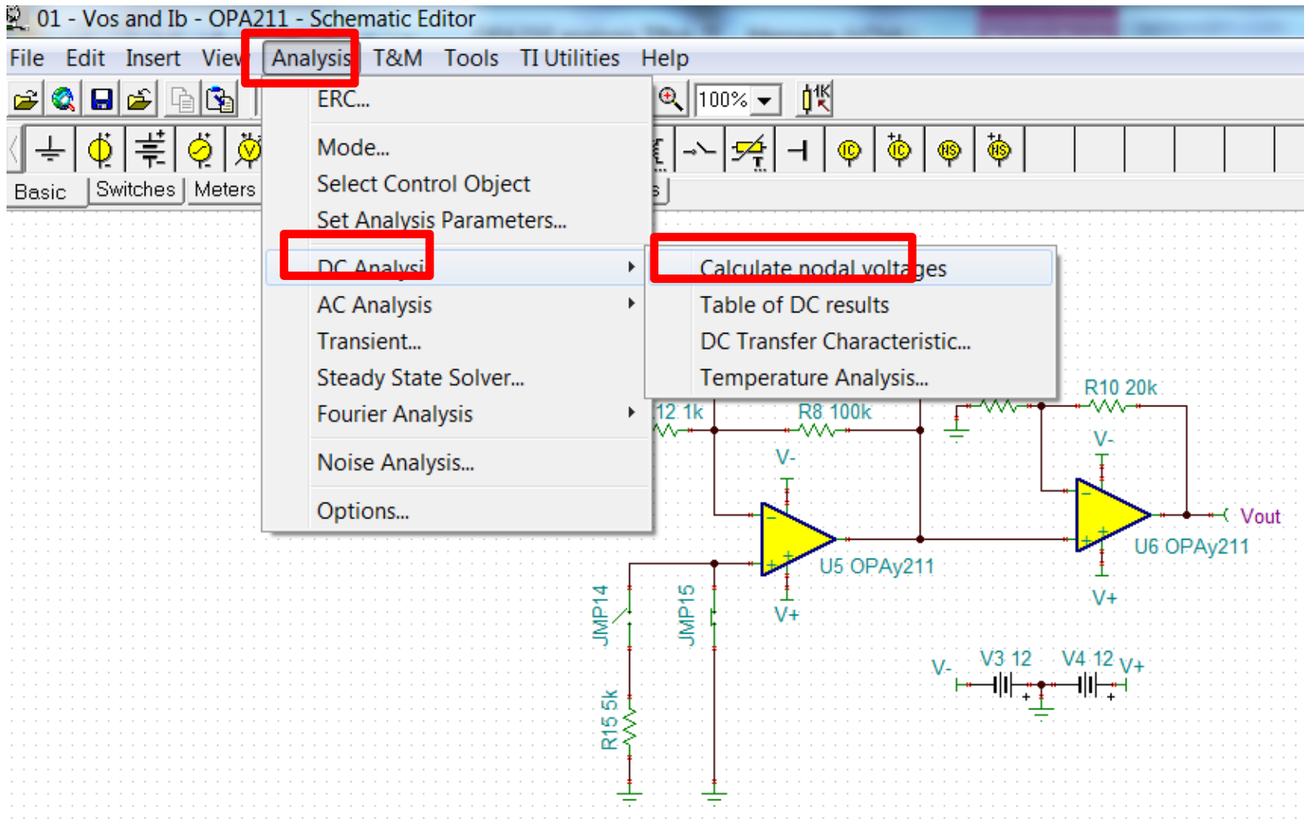
LMV844 Zout_TG.TSC

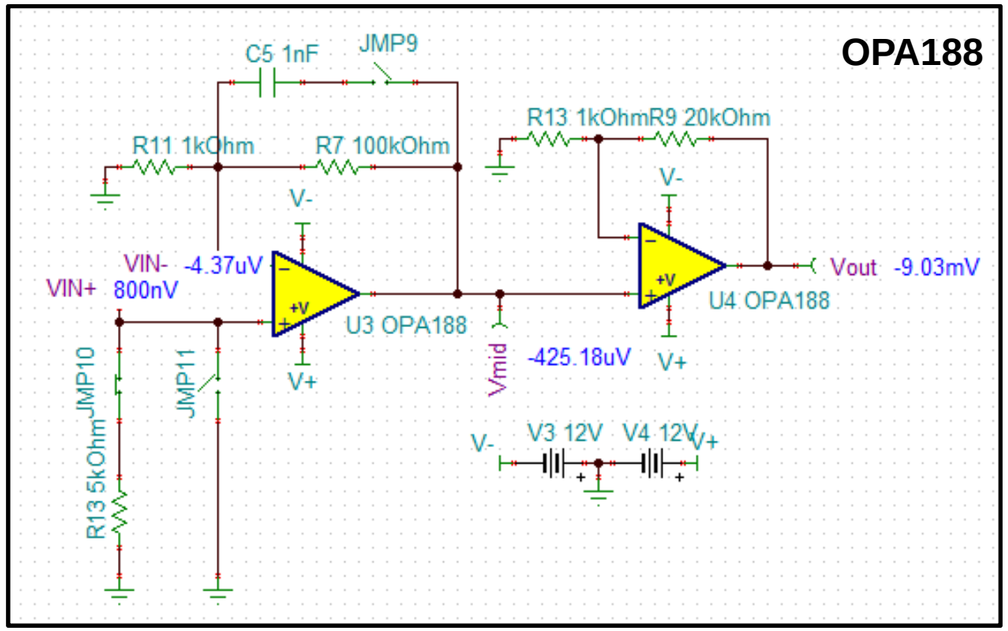
Offset Voltage Measurement

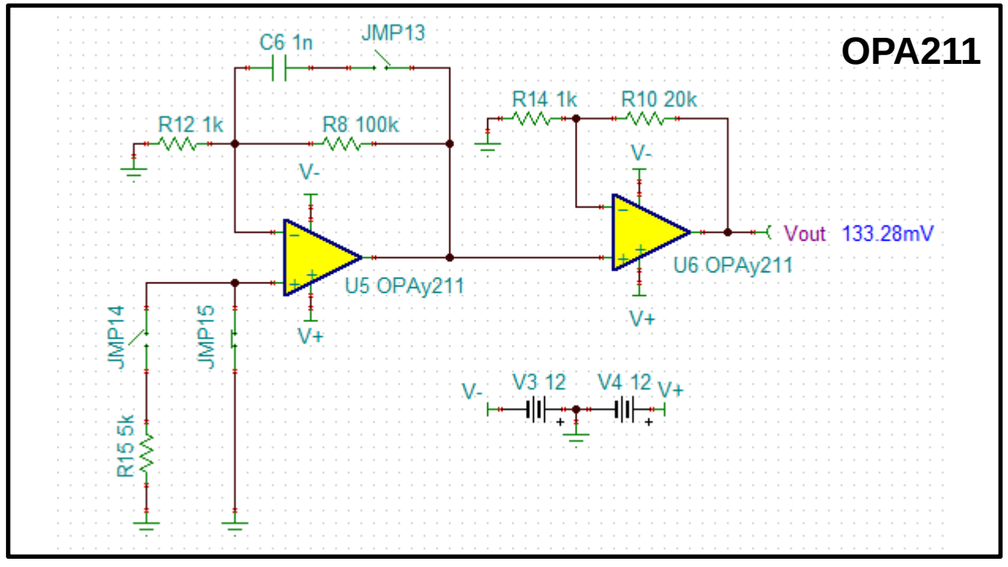
01 - Vos and Ib - OPA188.TSC

01 - Vos and Ib - OPA211.TSC

- Example Circuits:
  1. “01 - Vos and Ib - OPA188.TSC”
  2. “01 - Vos and Ib - OPA211.TSC”
- Analysis → DC Analysis → Calculate nodal voltages





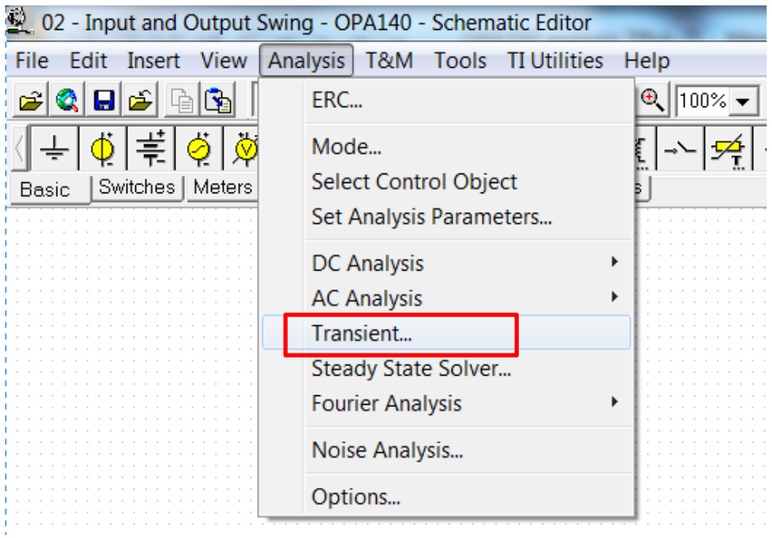


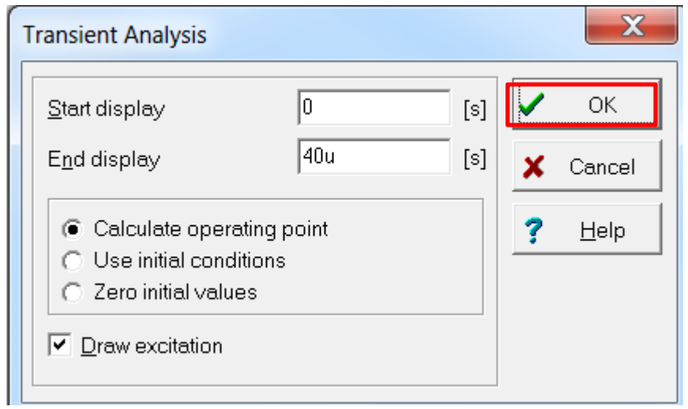
Transient Analysis Input / Output Voltage Swing

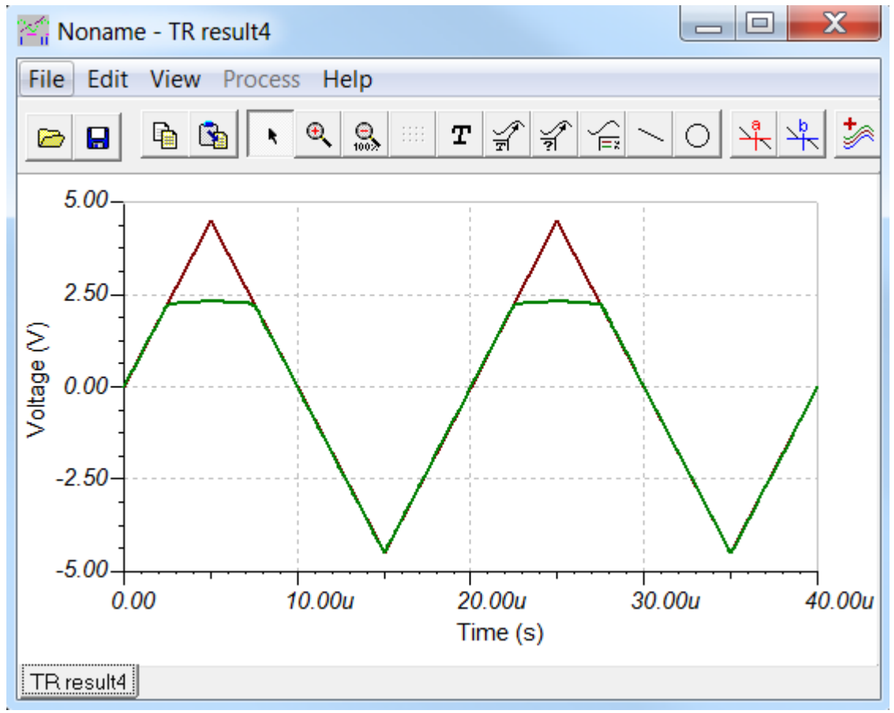
- Example Circuits:
  1. “02 - Input and Output Swing - OPA140.TSC”
  2. “02 - Input and Output Swing - OPA277.TSC”
- Analysis → Transient → OK
- View → Separate Curves

02 - Input and Output Swing - OPA140.TSC

02 - Input and Output Swing - OPA277.TSC

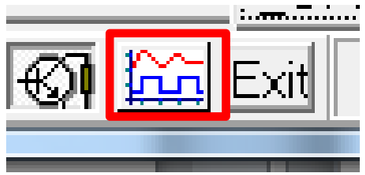




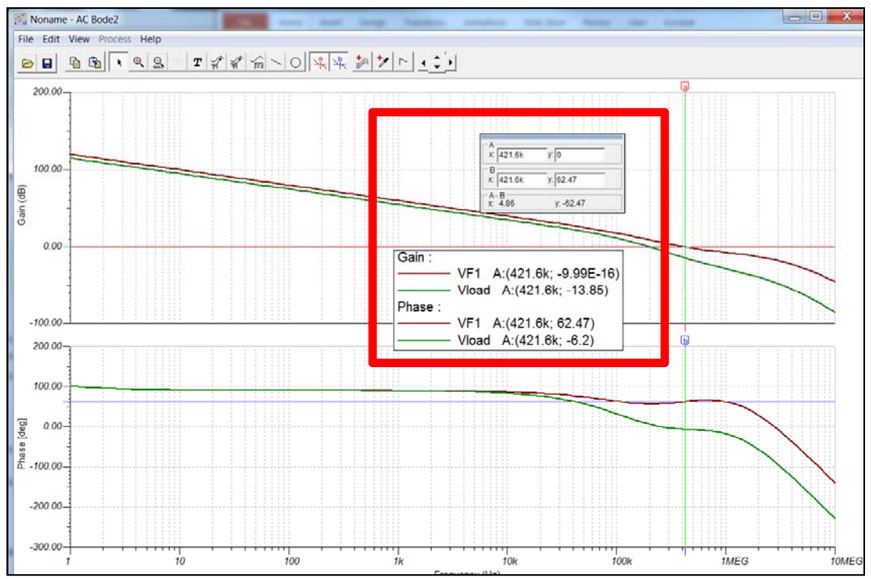


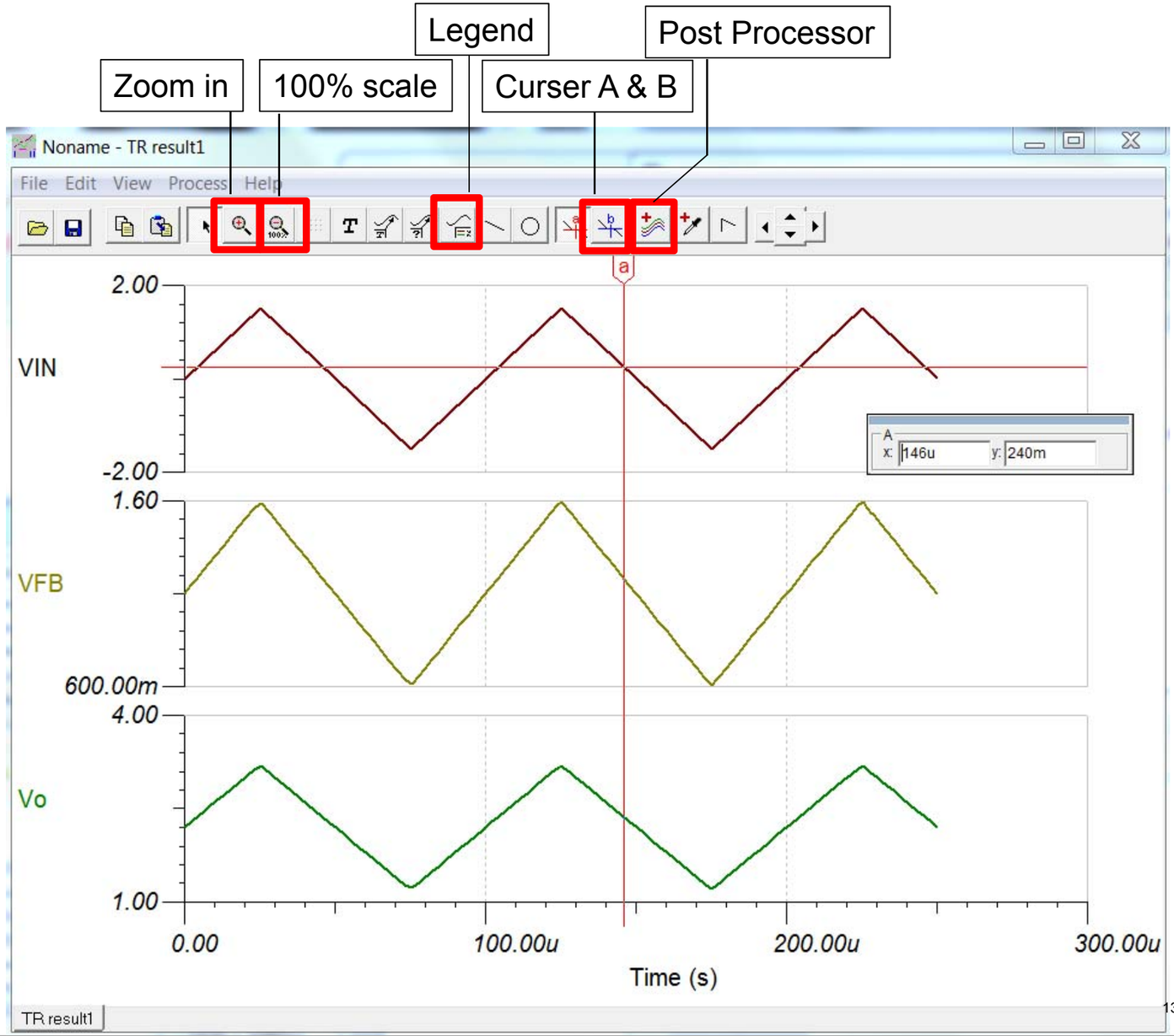
Results Window

- Curser Window Stays on Top
- Bottom Left Corner has Red & Blue Button to get Results Window Back



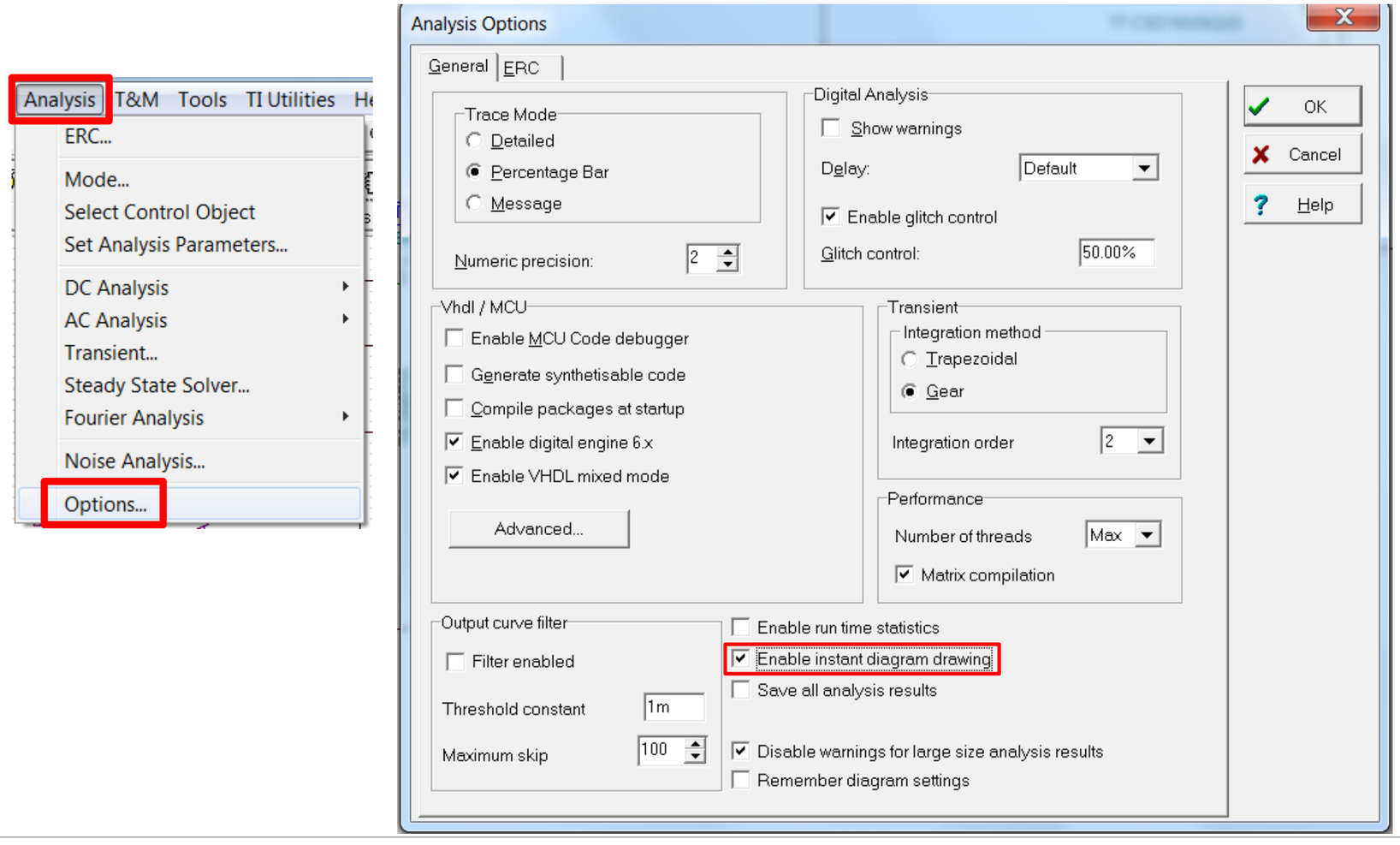
- Right Click Mouse for Automatic Gain and Phase Calculation





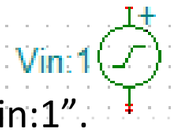
Enable Instant Diagram Drawing

- This has the results window refresh continuously during a simulation
- Analysis → Options → check box “Enable instant diagram drawing”

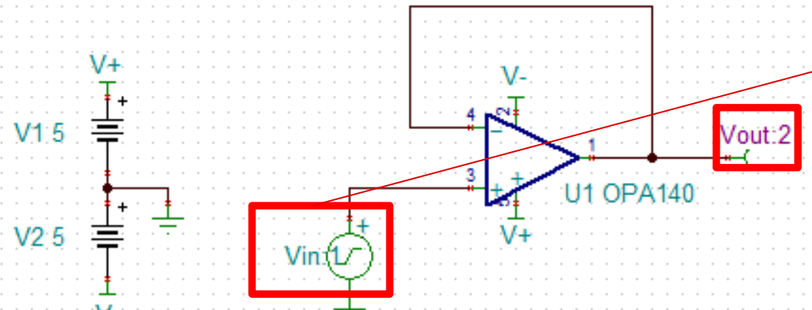


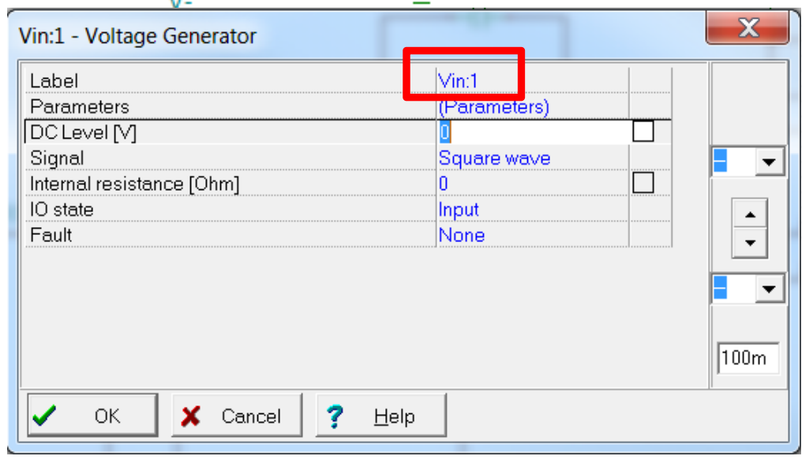
Separating

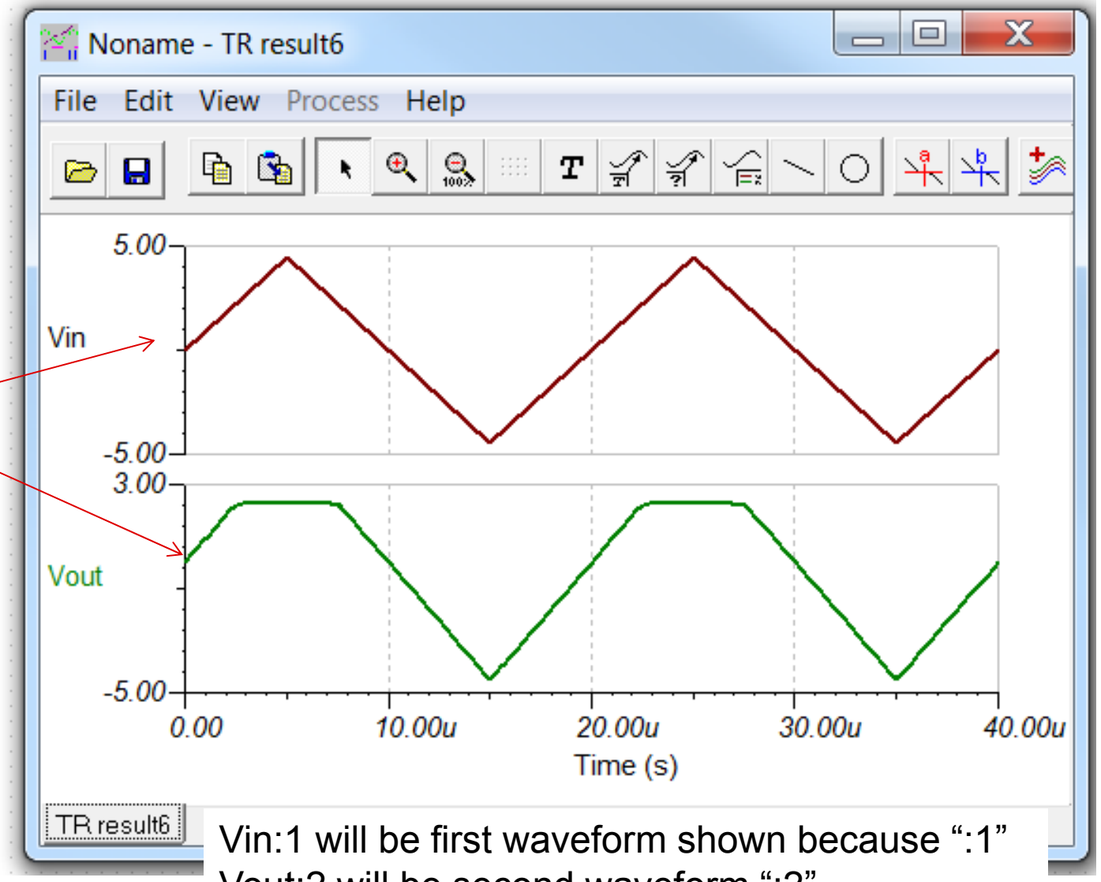
TIP: add ":1" to any meter name to show all output Waveforms separately.

Example Double Click "Vin" to  to open voltage generator menu and change Label to "Vin:1".

Voltage Meter





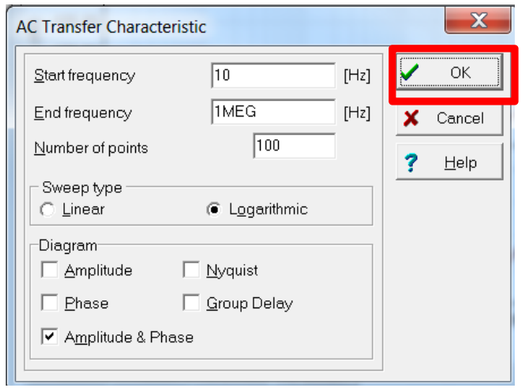


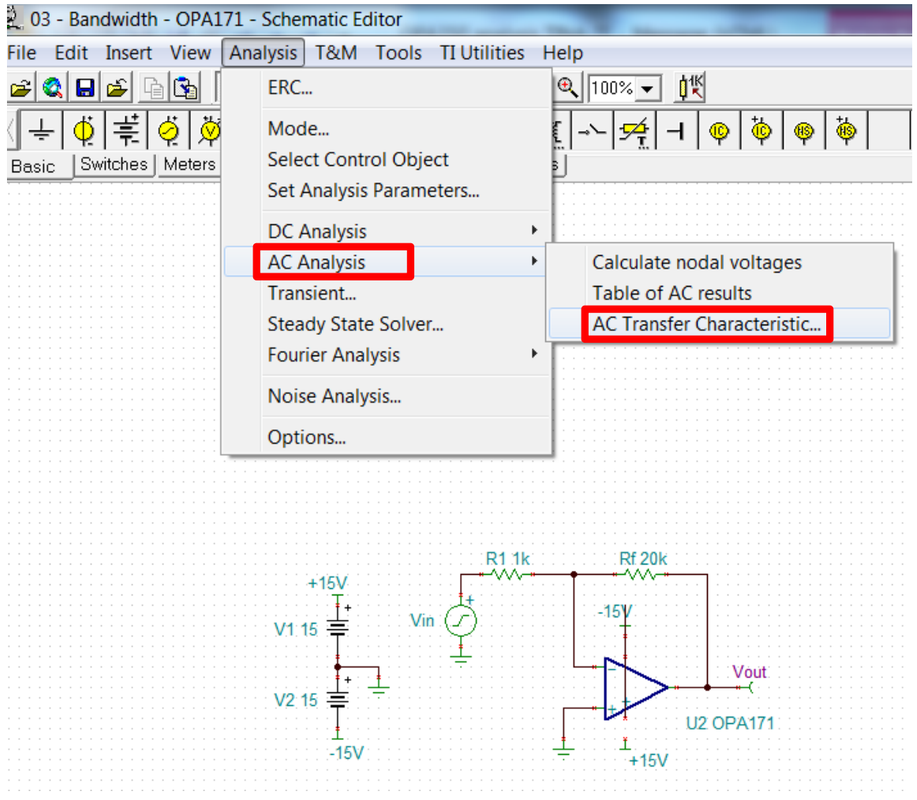
Vin:1 will be first waveform shown because ":1"
Vout:2 will be second waveform ":2"

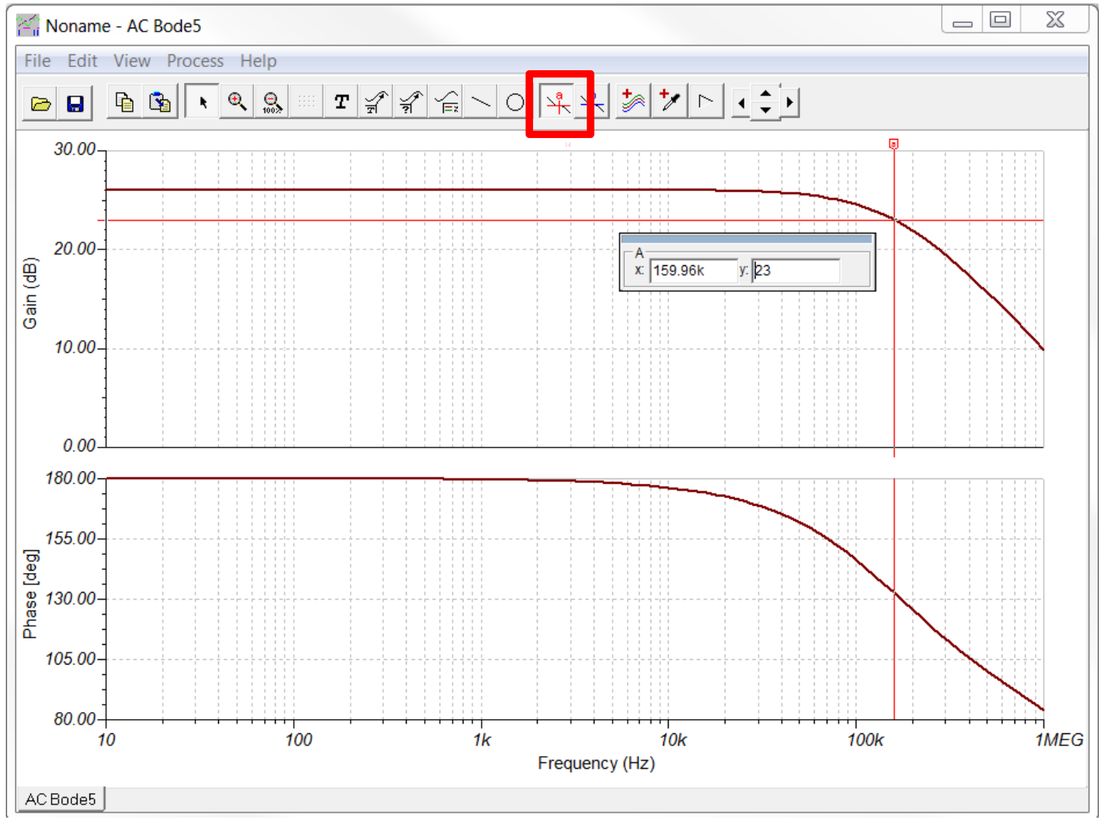
Bandwidth Testing

- Example Circuit:
  - o “03 - Bandwidth - OPA171.TSC”
- Analysis → AC Analysis → AC Transfer Characteristic → OK
- Use “a” “b” cursers for analysis.
- -3dB point is 23dB Gain & 160kHz Bandwidth

03 - Bandwidth - OPA171.TSC

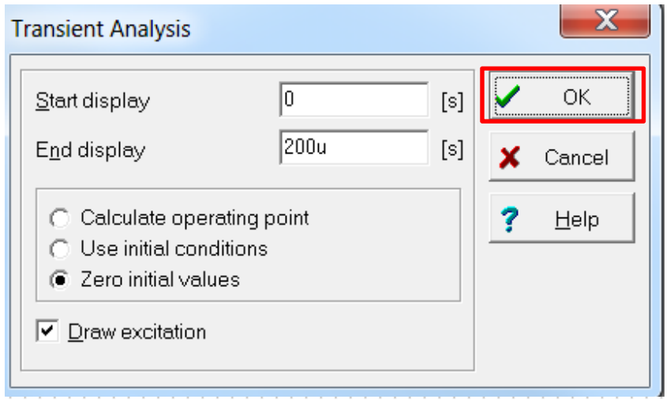


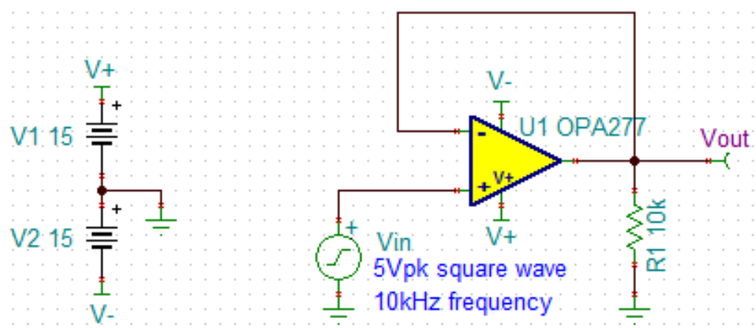


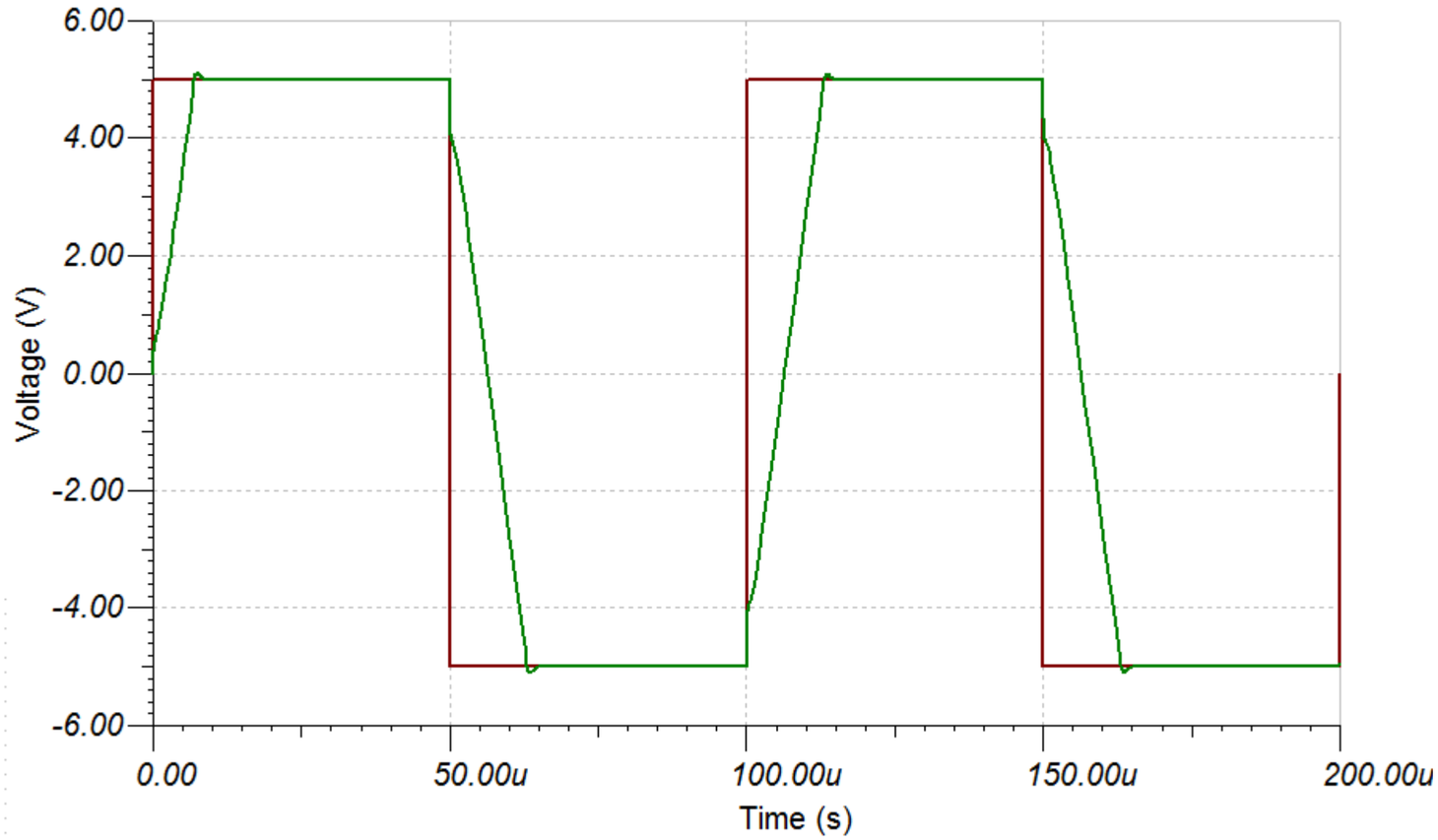


Slew Rate

- Example Circuit:
  - o “04 - Slew Rate - OPA277.TSC”
- Analysis → Transient → OK





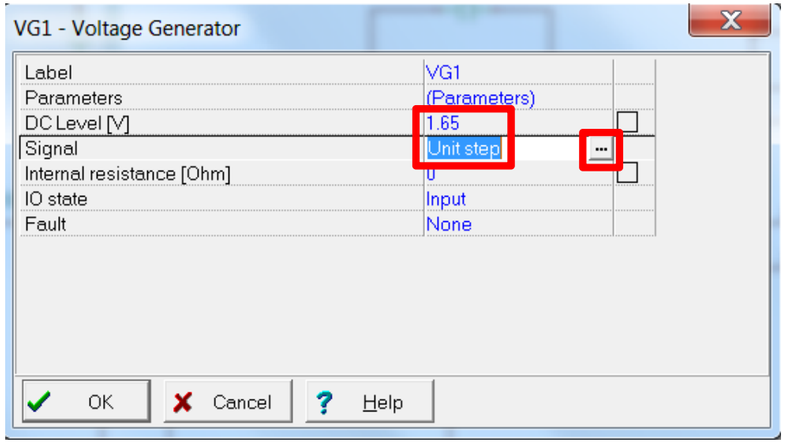


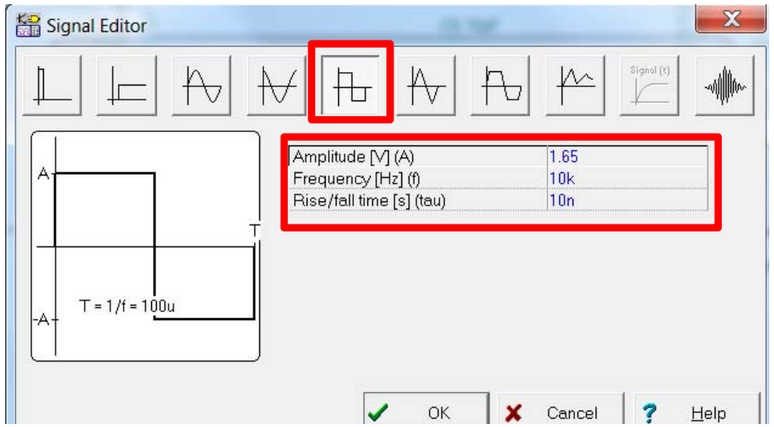
04 - Slew Rate - OPA277.TSC

Voltage Generator Configuration

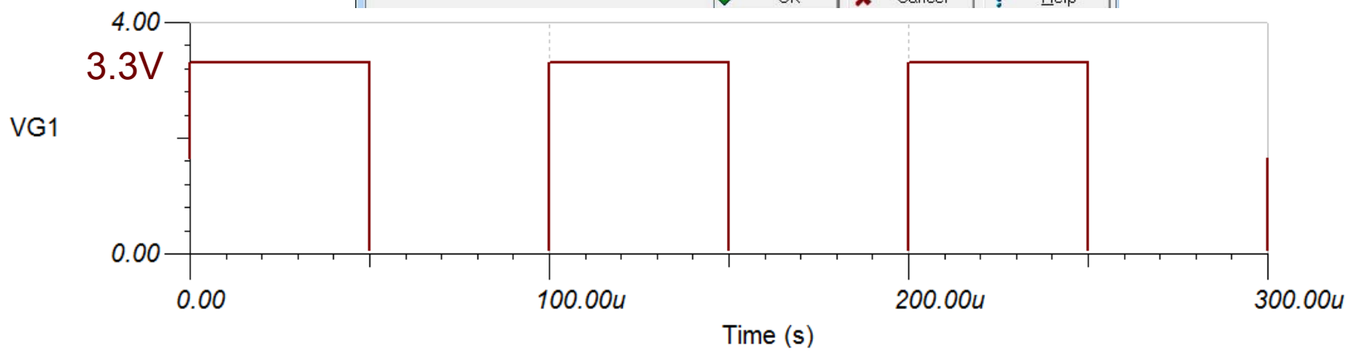
- Example:
  Set Voltage Generator for 0V to 3.3V 10kHz Square Wave

- Choose Voltage Generator Symbol 
- Double Click to Set Parameters
- Set DC Level [V] → 1.65V
- Go to Signal → Unit Step → Press  Button
- Set Amplitude [V] (A) → 1.65
- Set Frequency [Hz](f) → 10k
- Set Rise / fall time [s] (tau) 10n



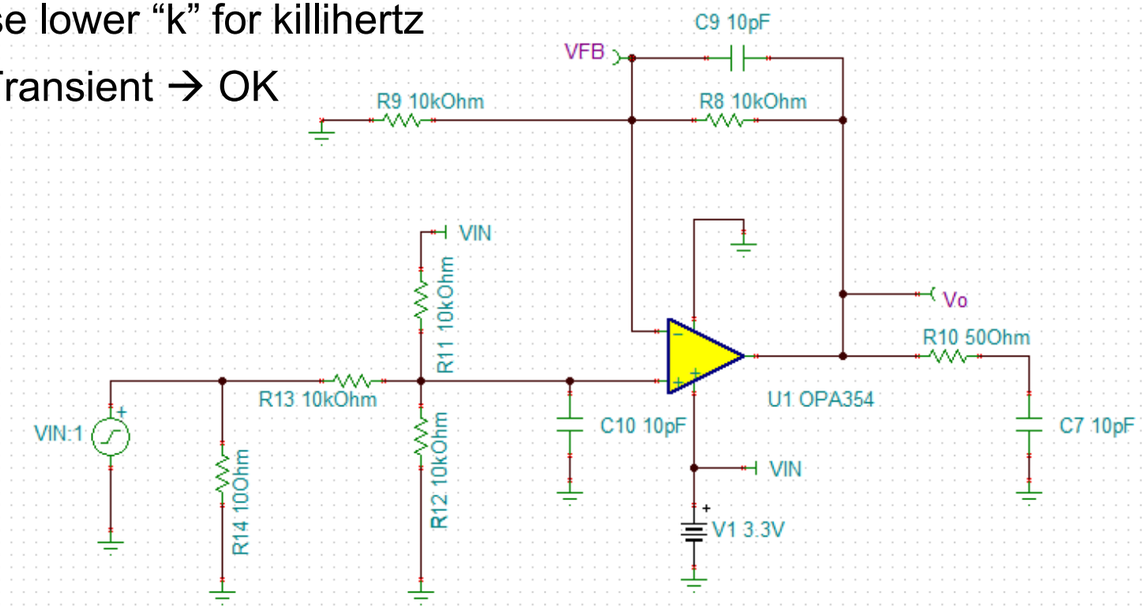


Waveform Results →

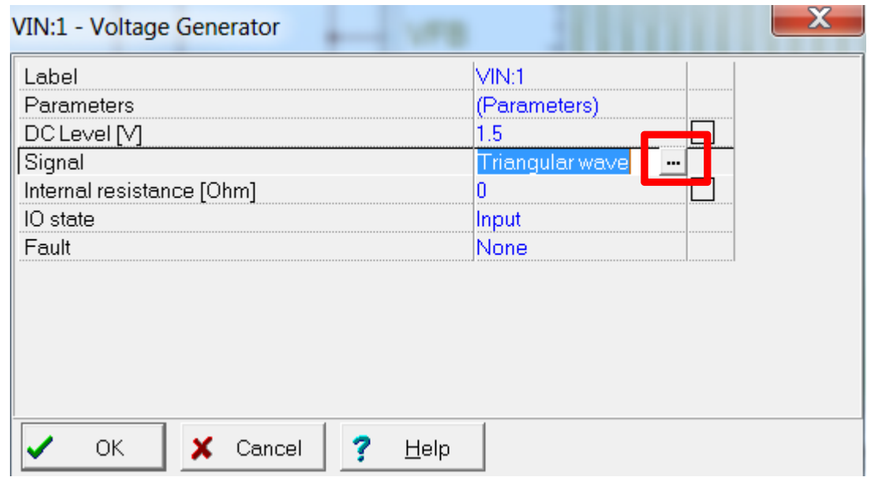


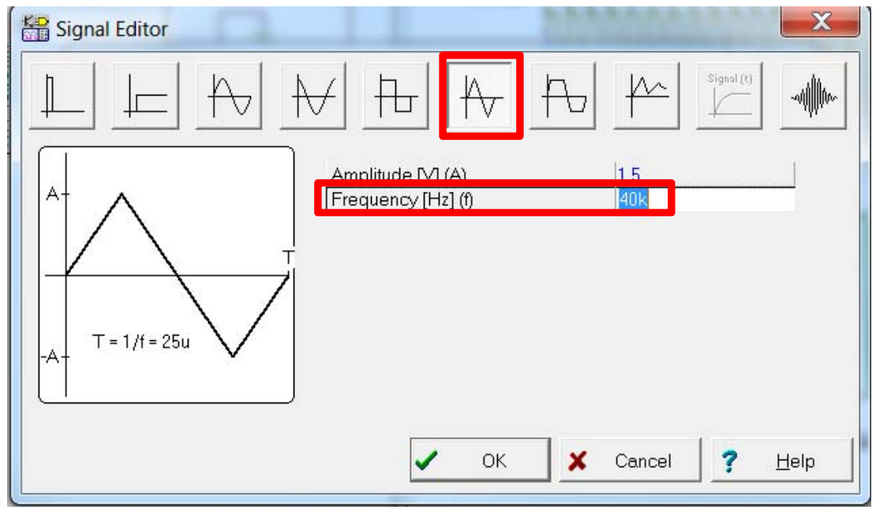
Voltage Generator as a Triangle Wave – OPA354

- Example Circuit:
  - o "_OPA354 Circuit.TSC"
- Double Click on "VIN:1" Voltage Generator Symbol
- Set a "DC Level [V]"
- Choose the ▪▪▪ 3 dots next to Signal
- Choose Triangle Waveform at Top
- Set Amplitude and Frequency
- Be sure to use lower "k" for killihertz
- Analysis → Transient → OK



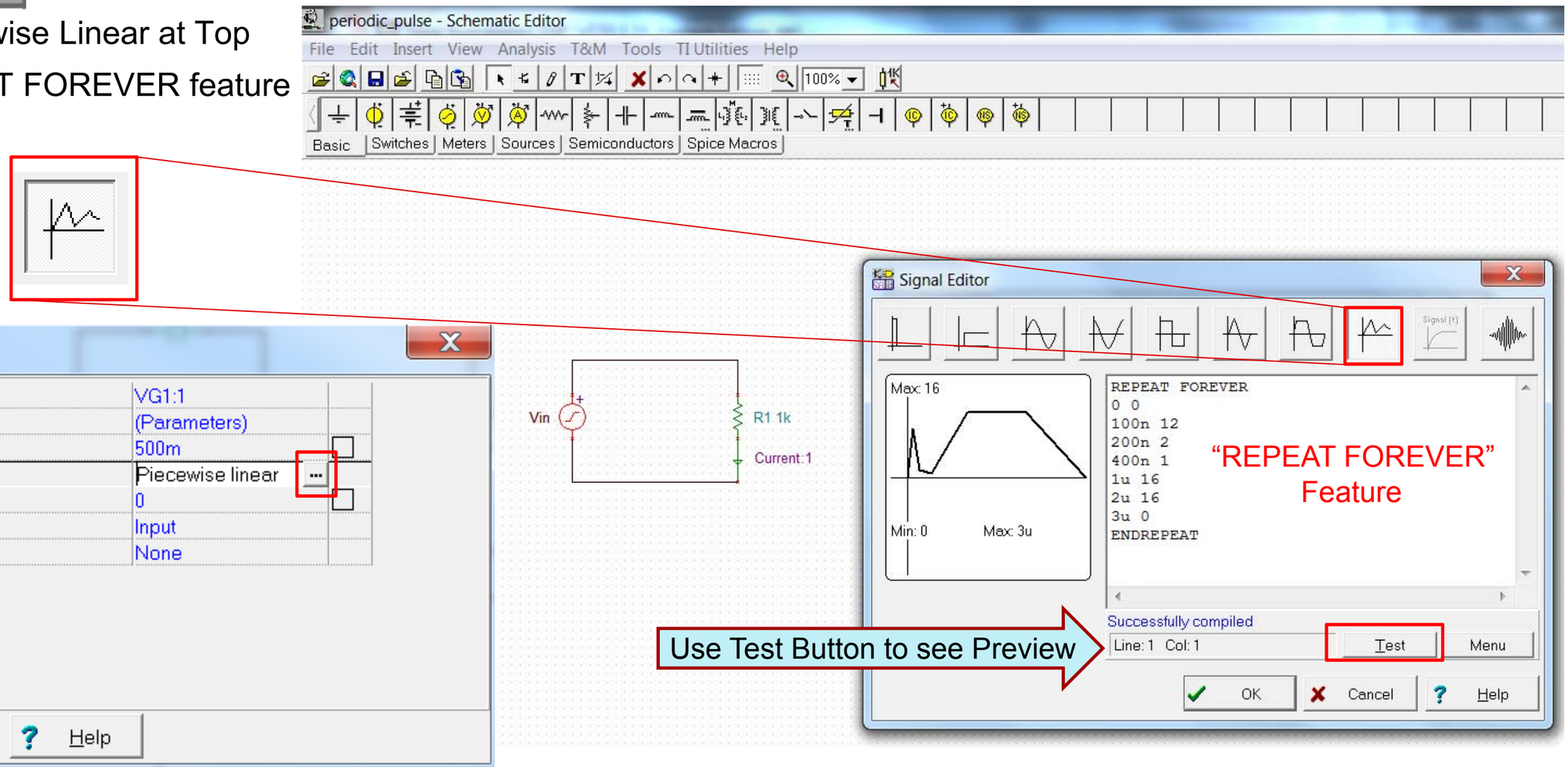
This Creates a Triangle Wave from 0 to 3.3V





Generating a Piecewise Linear Voltage Source

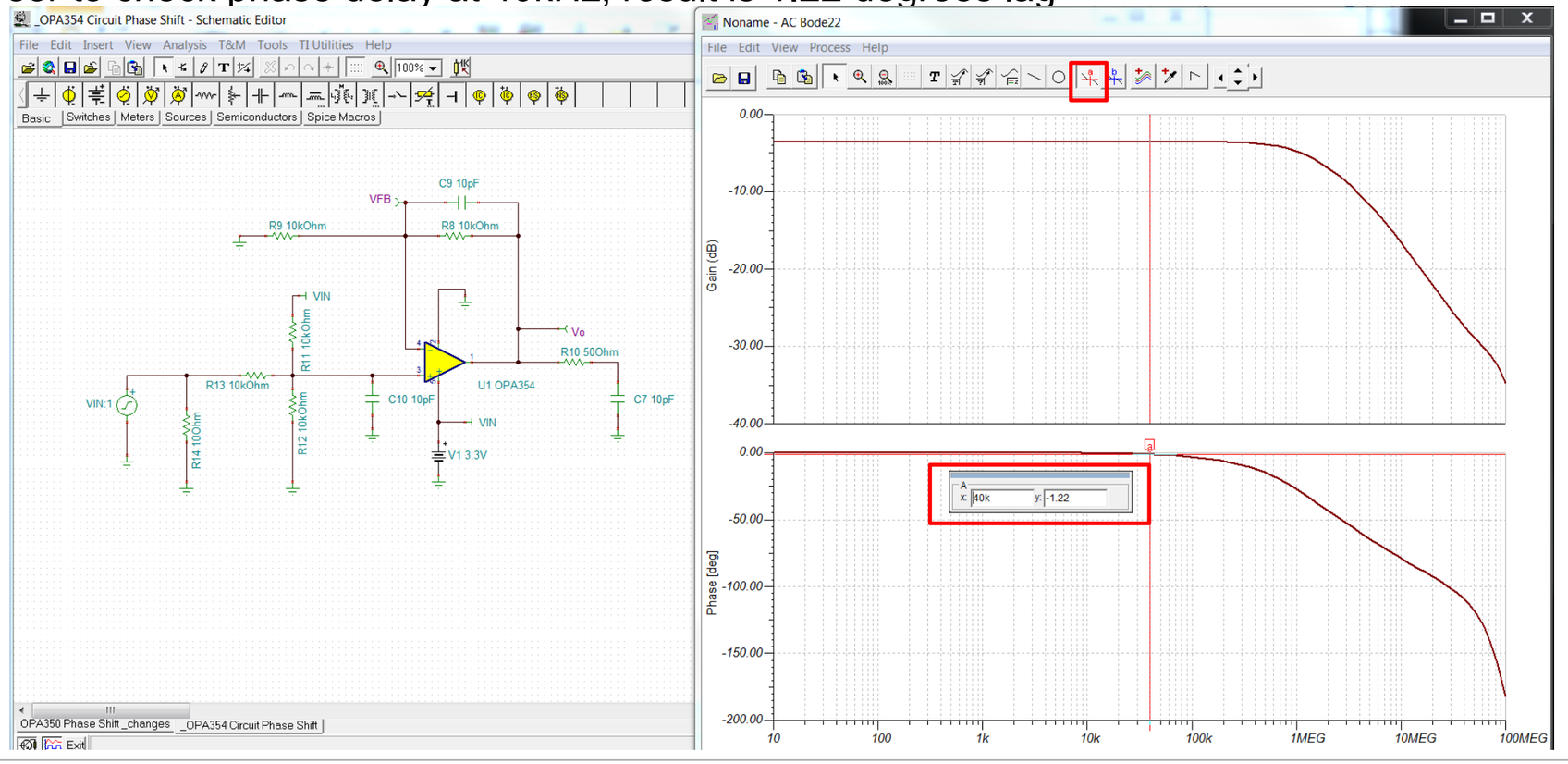
- Double Click on “Vin” Voltage Generator Symbol
- Choose the ▪▪▪ 3 dots next to Signal
- Choose Piecewise Linear at Top
- Add in REPEAT FOREVER feature



Phase Delay Calculation

- Example Circuit:
  - o “_OPA354 Circuit Phase Shift.TSC”
- Analysis → AC Transfer Characteristic → OK
- Delete VFB Curve
- User Curser to check phase delay at 40kHz, result is 1.22 degrees lag

_OPA354 Circuit Phase Shift.TSC

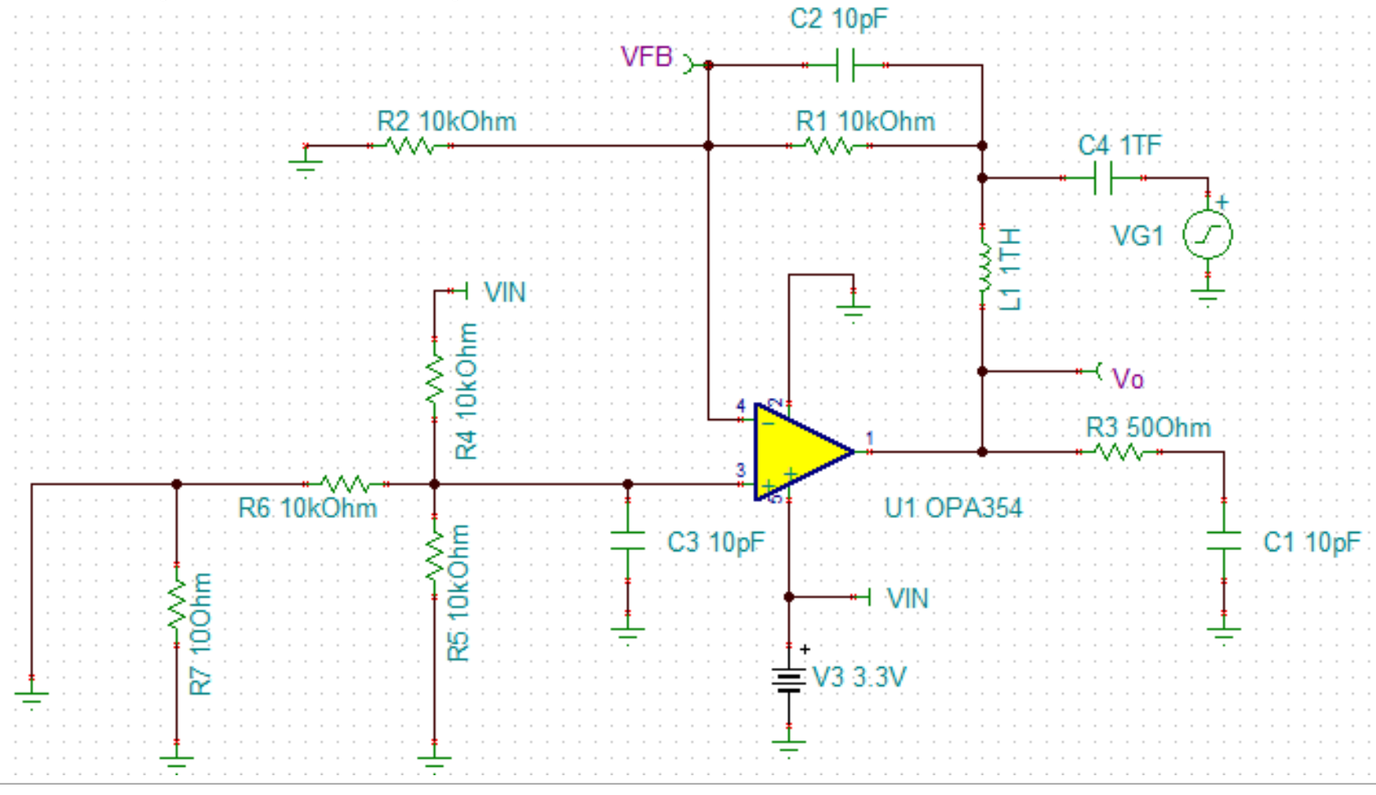


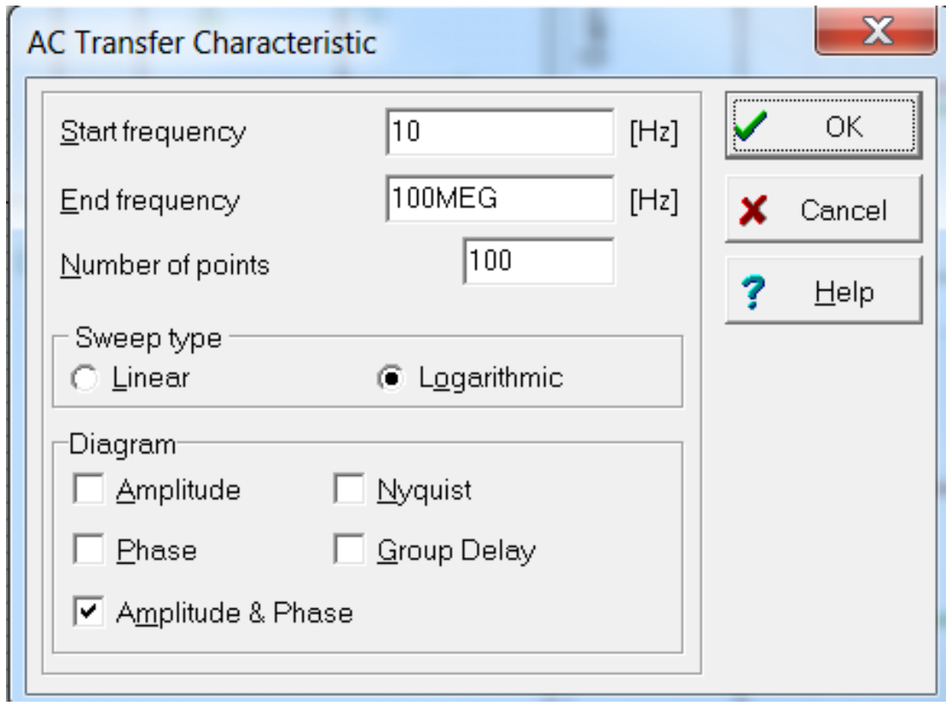
Stability Calculation – OPA354 (1 of 2)

- Example Circuit:
  - o “_OPA354 Stability.TSC”

_OPA354 Stability Measurement.TSC

- Add in 1TF capacitor and 1TH Inductor into Feedback Loop
- Add Voltage Generator VG1
- Analysis → AC Analysis → AC Transfer Characteristic → OK

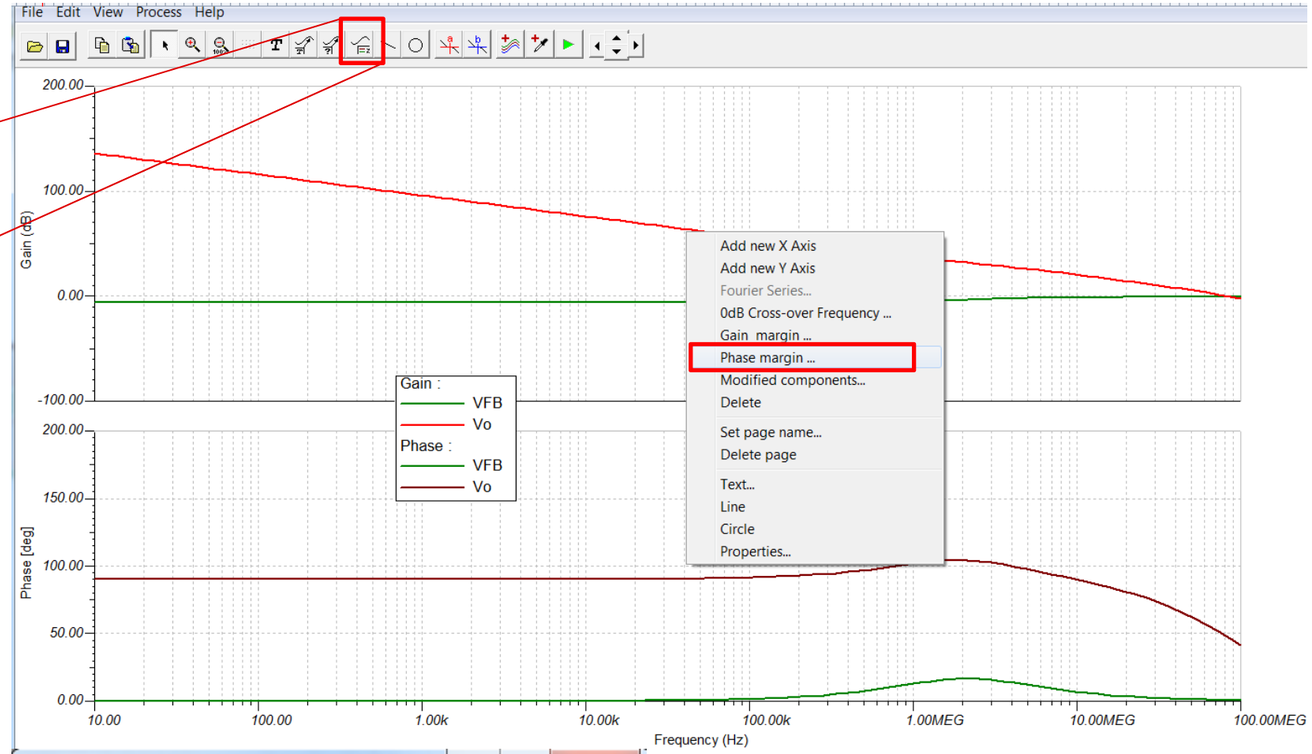




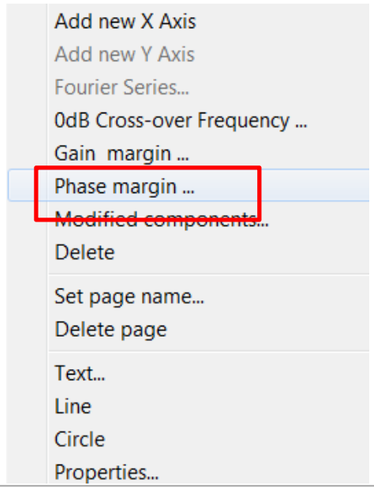
Stability Calculation – OPA354 (2 of 2)

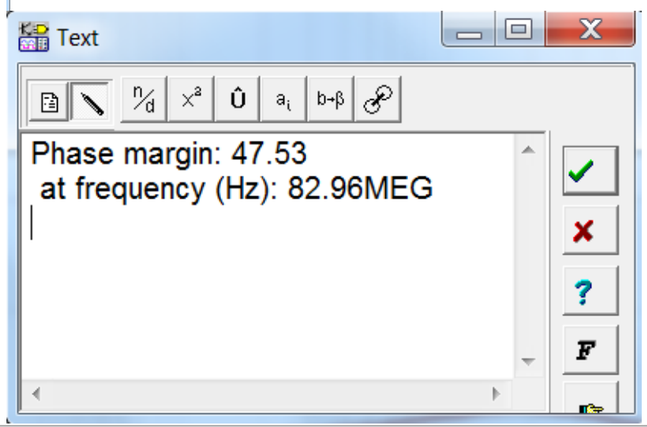
- Example Circuit:
  - o “_OPA354 Stability.TSC”
- Add
  - o Use Legend Feature and Delete: VFB and Vo curves.
  - o Choose Legend Feature

  - o Delete Phase Curves for: Aol, OneOverBeta, VFB
  - o Choose Vo Curve from top of Legend “Gain”
  - o Separate Curves
  - o Collect Curves (now see Vo Phase from 40 – 110)
  - o Right Click and Choose “Phase margin…”
  - o Box will display showing Calculated Phase Margin

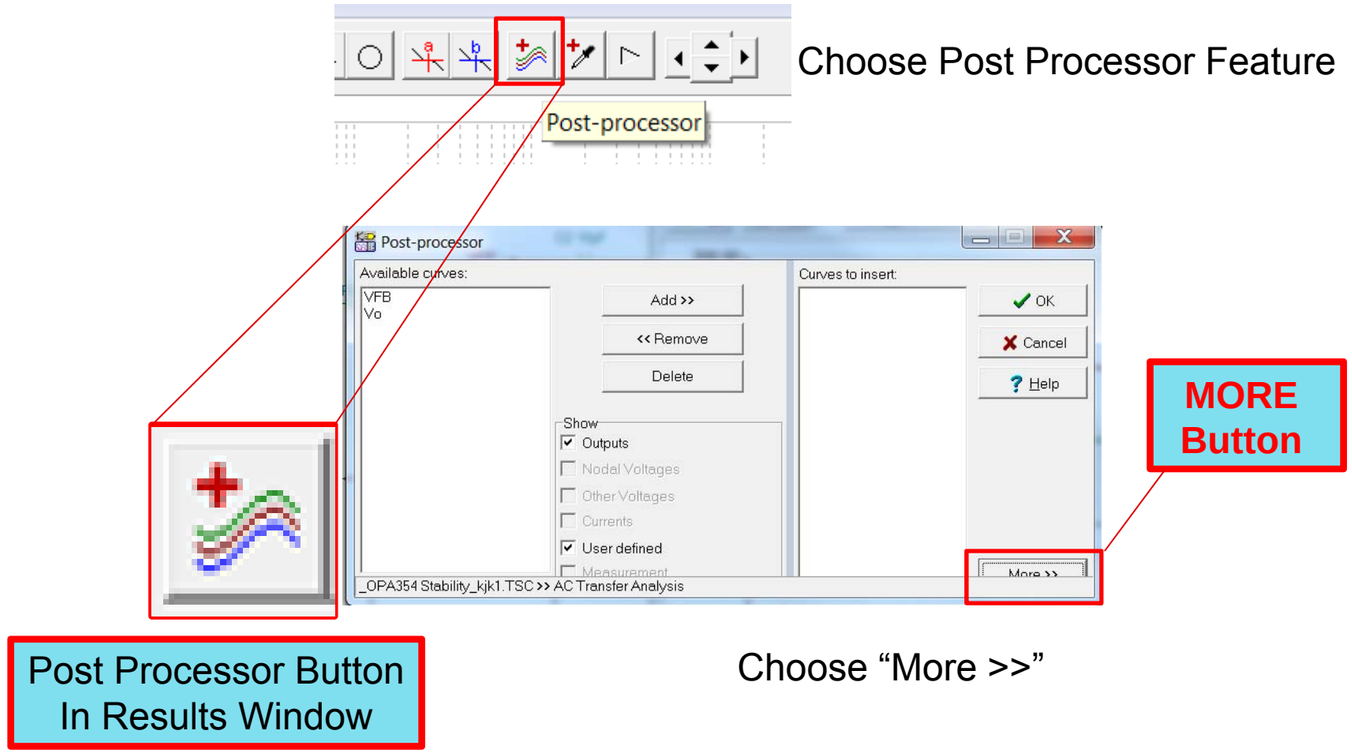


Right Mouse Button “Phase margin” Feature



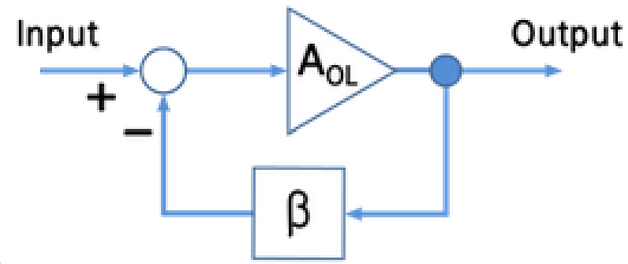


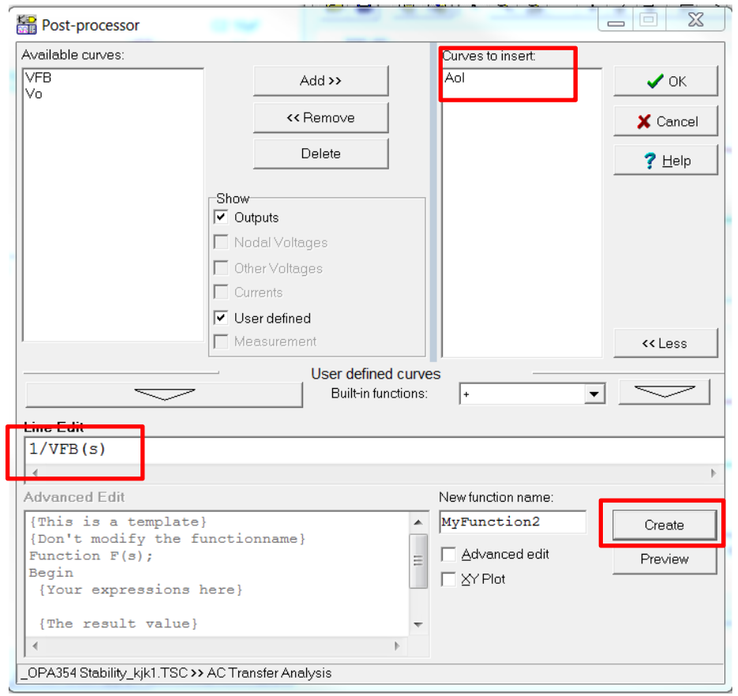
Post Processor Function (1 of 2)

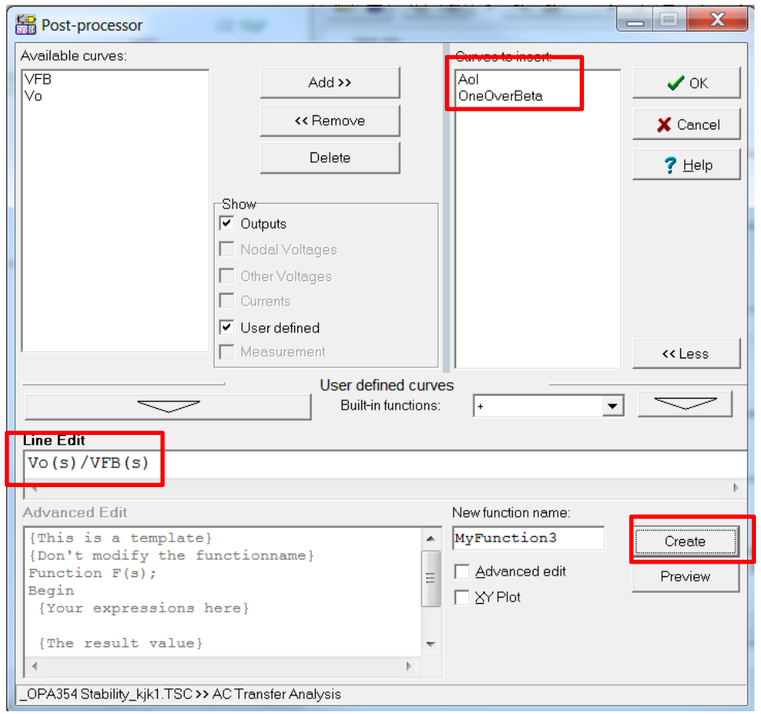


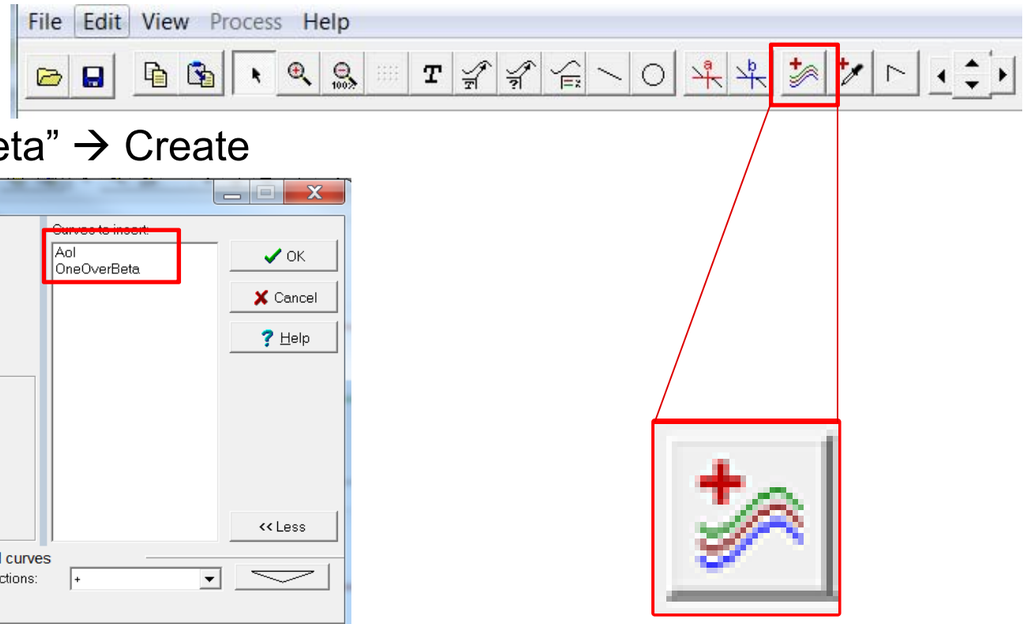
Post Processor Function (2 of 2)

- Example Circuit:
  - o “_OPA354 Stability.TSC”
- Add Calculations
  - o Open Loop Gain Aol = 1/VFB(s)
  - o Closed Loop Gain Curve 1/β = Vo(s)/VFB(s) (Tina does not allow a “1” to start, so name “OneOverBeta”)
  - o Vo is loop gain = Aol x β
- STEPS: Line Edit “1/VFB(s)”, New function Name “Aol” → Create
  Line Edit “Vo(s)/VFB(s)”, New function Name “OneOverBeta” → Create







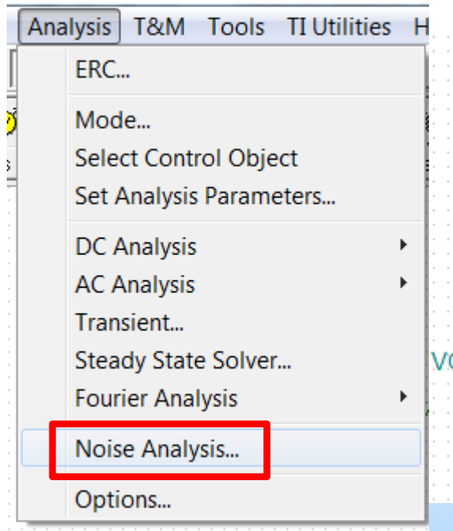


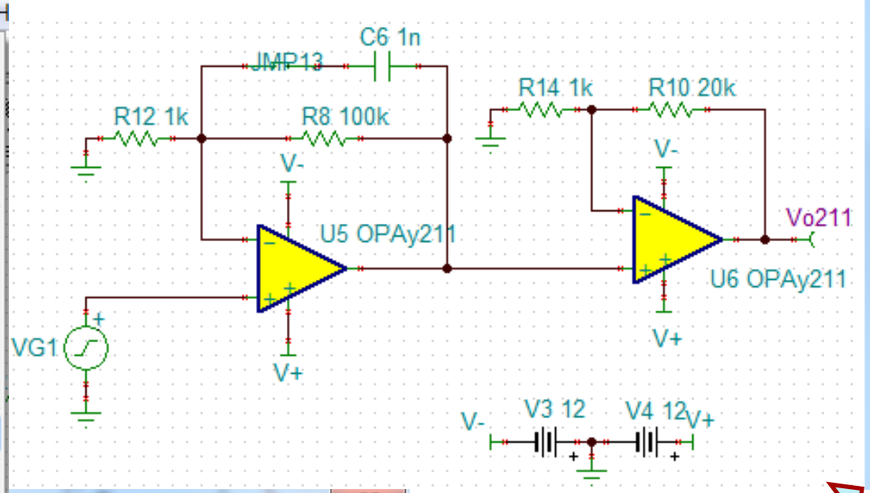
Post Processor Button In Results Window

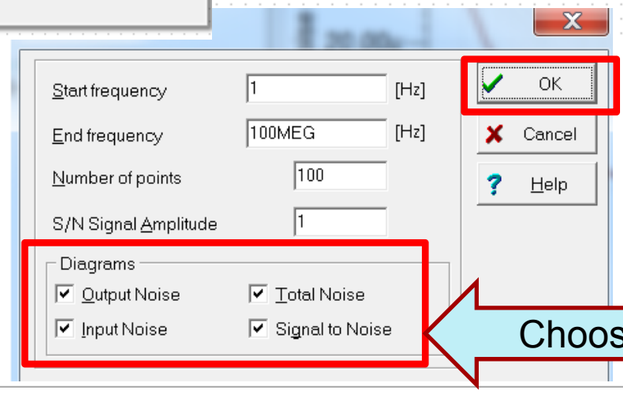
Noise Analysis

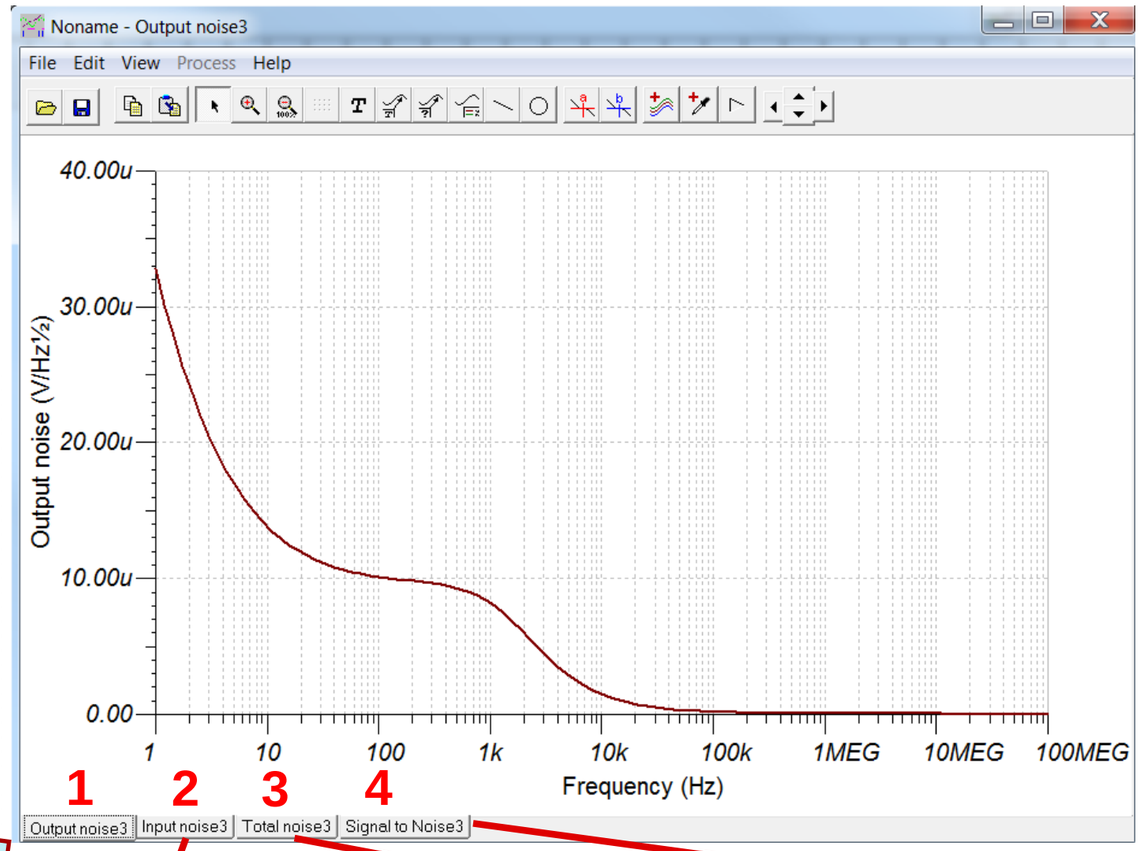
- Example Circuit:
  - o “05 - Noise - OPA211.TSC”
- Analysis → Noise Analysis → OK
- **4 Results** Are Calculated

05 - Noise - OPA211.TSC

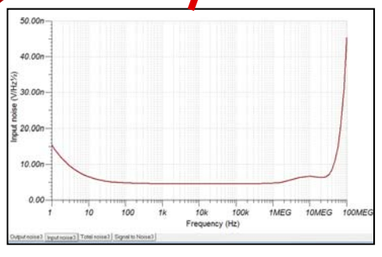


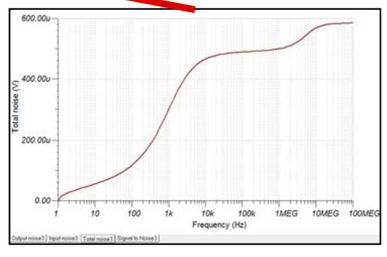


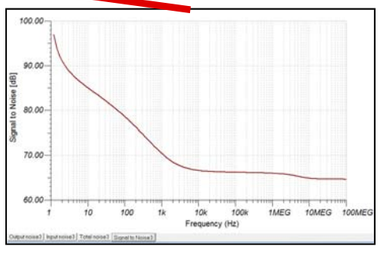




Choose all 4 check boxes



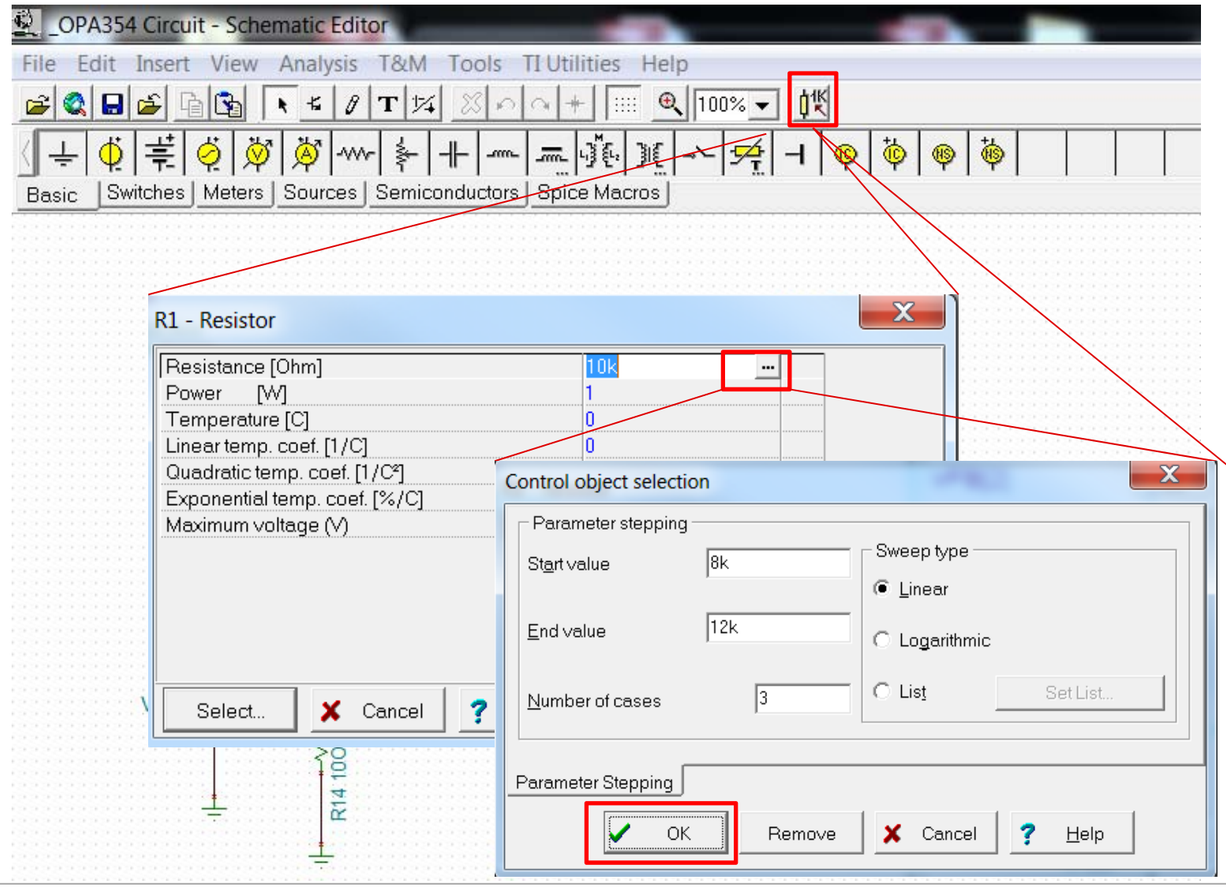




Adding & Removing Variable Sweep Feature

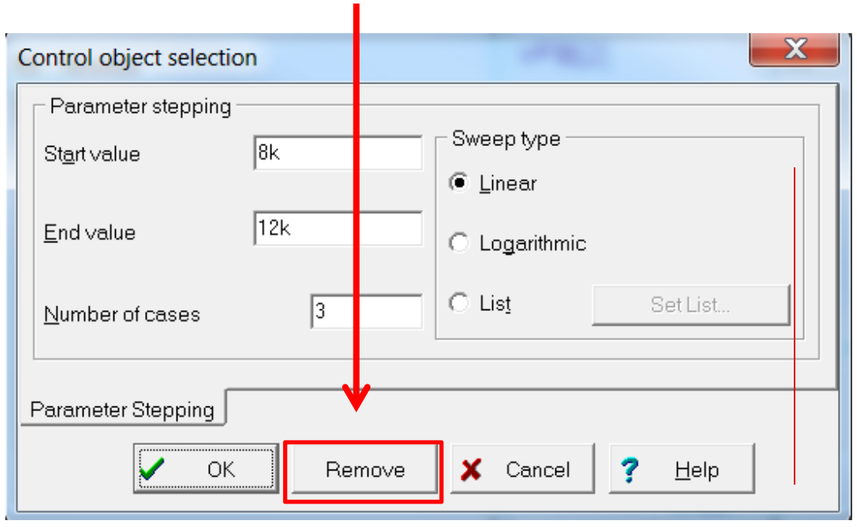
To Add Component Parameter Sweep

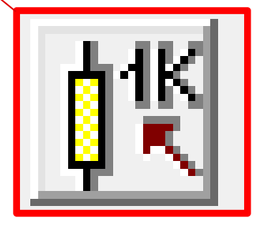
1. Example Circuit: "_OPA354 Circuit.TSC"
2. Click on  button next to zoom.
3. Click on  and choose Start/End/Number of Cases



To Remove Component Parameter Sweep

1. Follow the same steps to get to "Control object selection" 
2. Press "Remove"

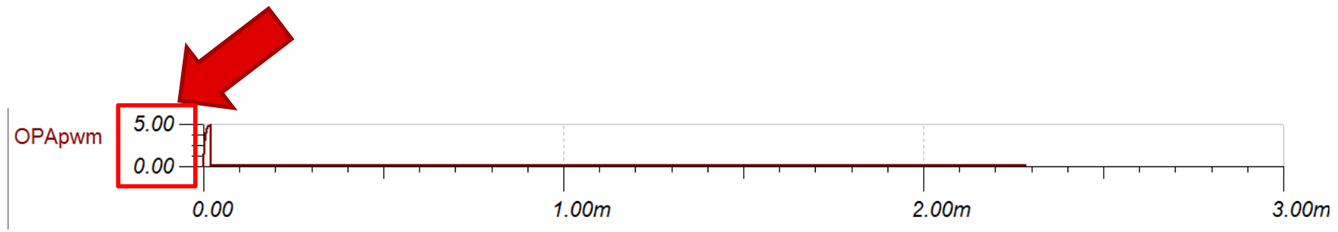


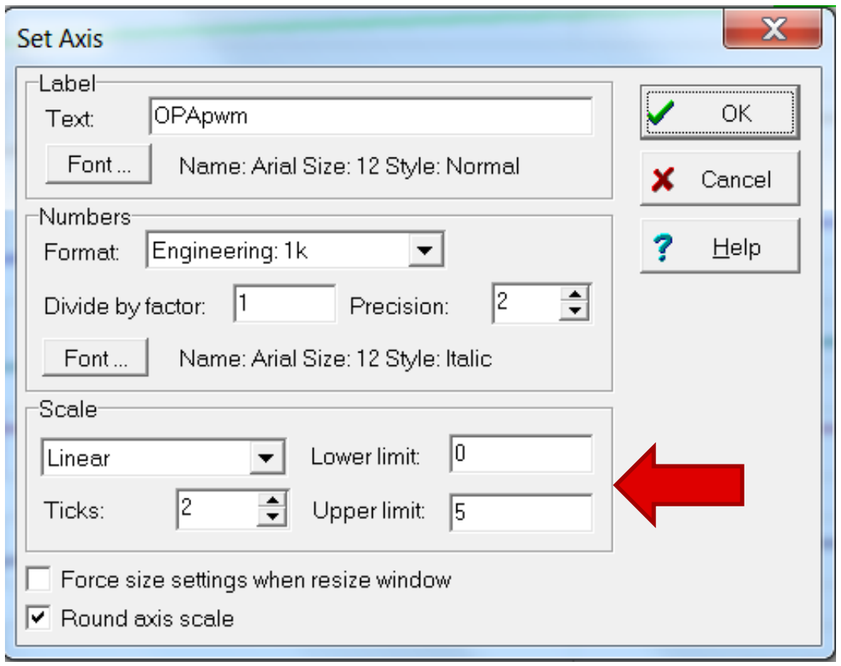


Variable Sweep Button

Double Click on Axis to Change Settings

- Double Click on Axis Values to Change

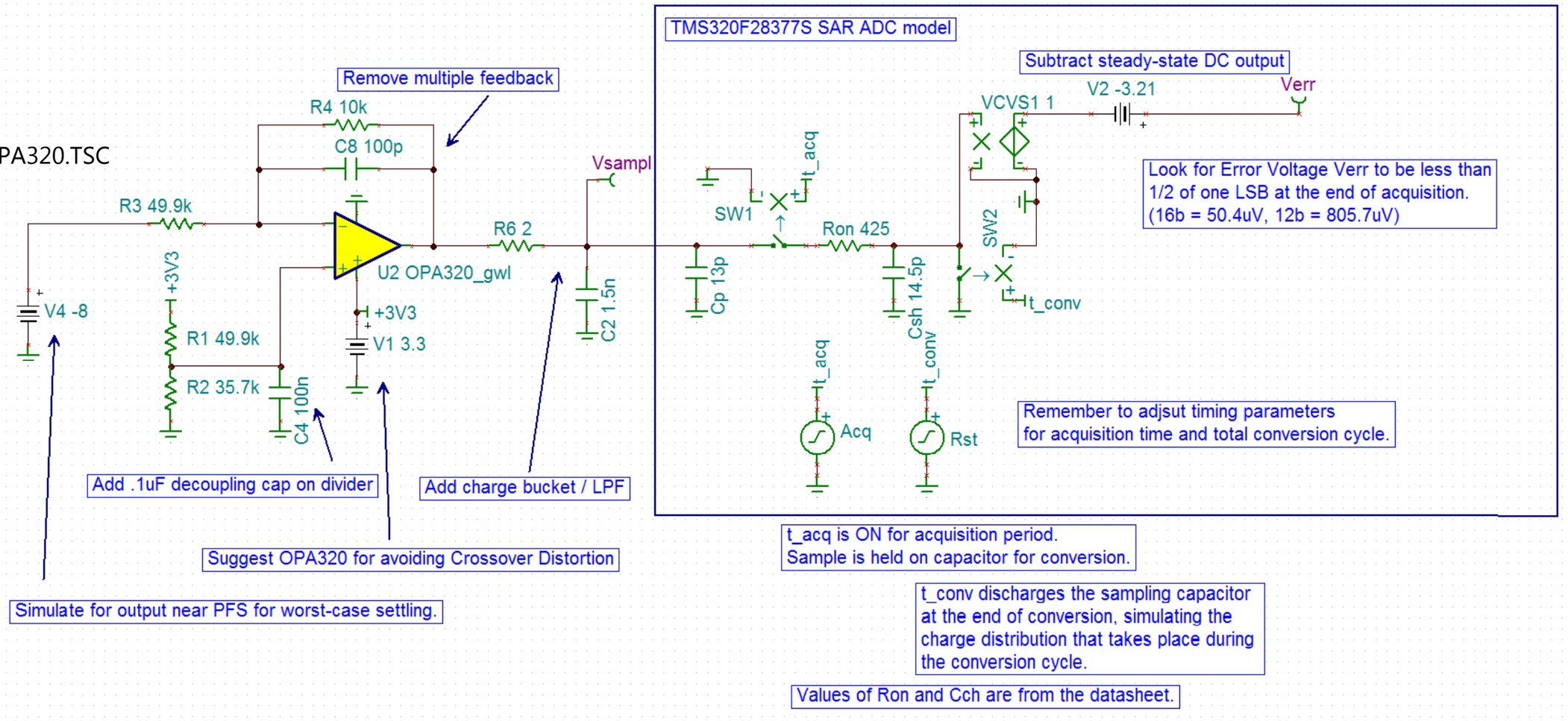




Op Amp to Drive SAR Converter

- Analysis → Transient → OK
- View → S

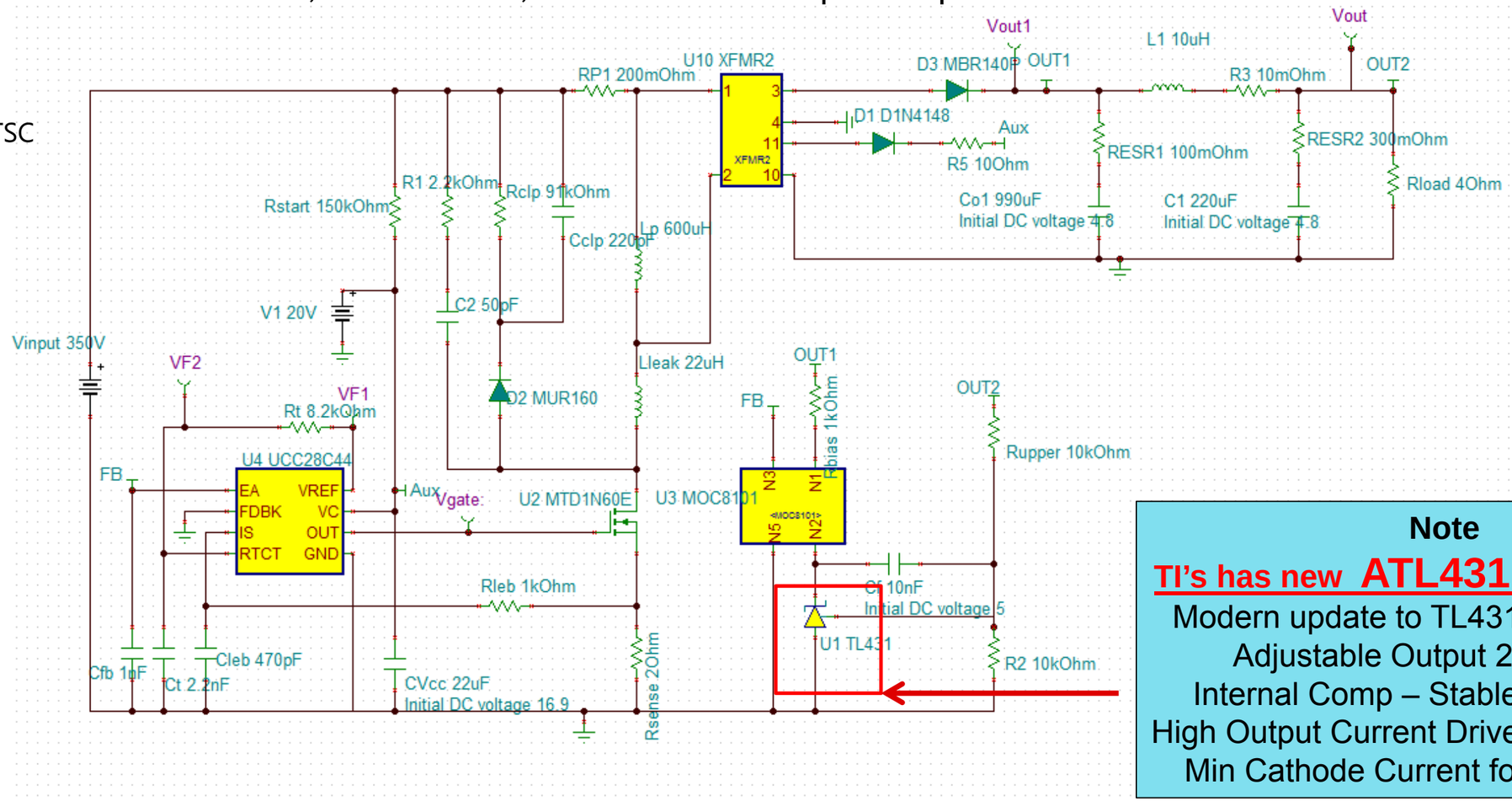
SAR drive with OPA320.TSC



Flyback Converter using UCC28C44 – Transient Model

- Example Circuit: _UCC28C44 Flyback.TSC
- Standard Flyback Converter with Optocoupler Feedback.
- Includes UCC PWM controller, Transformer, Vref TL431 and Opto-coupler

_UCC28C44 Flyback.TSC



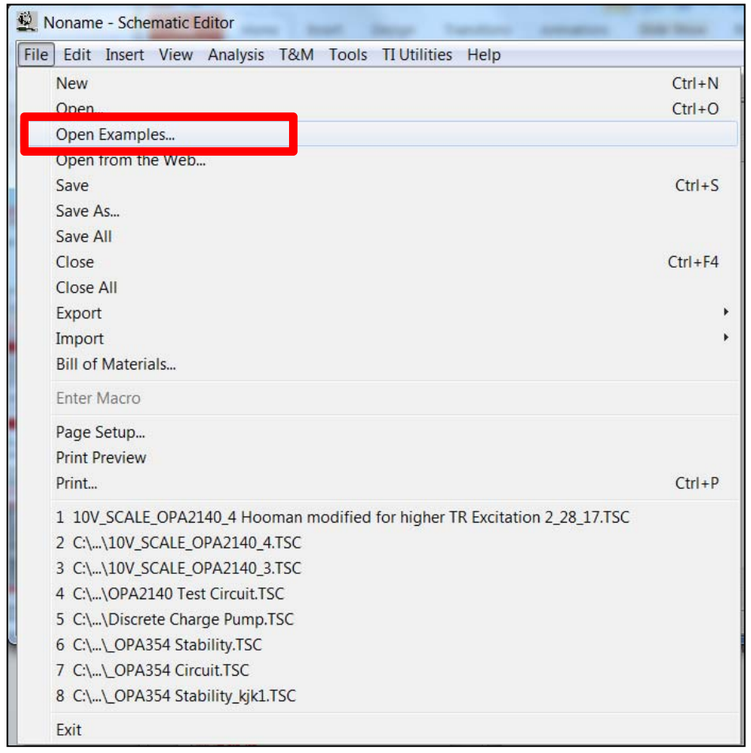
Note

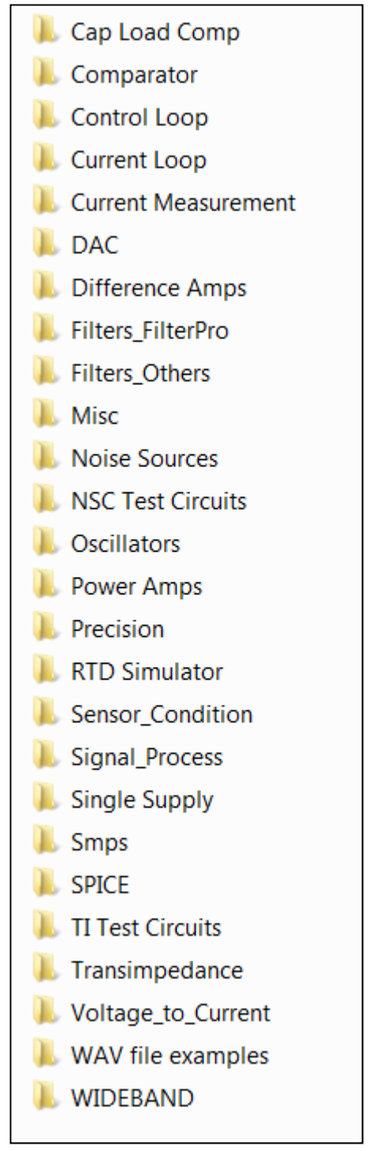
TI's has new ATL431 and ATL432

Modern update to TL431, TLV431, etc.
Adjustable Output 2.5 – 36Vin
Internal Comp – Stable with no Cap
High Output Current Drive 35uA – 100mA
Min Cathode Current for Reg = 35uA

Lots of Example Circuits

- In TINA-TI Examples Folder C:\Program Files (x86)\DesignSoft\Tina 9 - TI\EXAMPLES
- TI's online E2E Forum Community
- The circuits and models provided in this training





TI Precision Labs Training Online

- TINA-TI Video Training Series: https://training.ti.com/tina-ti-video-training-series
- Webench Power Designer Training Series: https://training.ti.com/webench%C2%AE-power-designer-training-series
- Webench Filter Designer Video: https://training.ti.com/webench%C2%AE-filter-designer-video

1. TINA-TI Training Series

Multiple Video courses showing how to use TINA-TI to solve Engineering problems with

#	Title	Duration
1.1	Introduction to TINA-TI(TM) Simulator	07:30
1.2	Using the TINA-TI(TM) simulator – ERC and Analysis types	07:03
1.3	Configuring Sources in TINA-TI(TM) simulator	06:31
1.4	TINA-TI(TM) Waveform Viewer, Part 1	07:12
1.5	TINA-TI(TM) Waveform Viewer, Part 2	05:32
1.6	Sweeping parameters in TINA-TI(TM) simulator	04:15
1.7	Noise, Fourier analysis and Signal Chain content in TINA-TI(TM) simulator	06:04
1.8	Power product simulation in TINA-TI(TM) simulator	08:23
1.9	Importing SPICE models into TINA-TI(TM) simulator	05:21
1.10	Tips and Tricks for TINA-TI(TM) simulator	12:54
1.11	How to use the Controlled Source Wizard in the TINA-TI(TM) simulator	06:51
1.12	Using WEBENCH® simulation export to create files for TINA-TI(TM) simulator	06:43

1. WEBENCH® Power Designer Training Series

#	Title	Duration
1.1	Learn WEBENCH® Power Series Overview	03:19
1.2	Starting WEBENCH® Power Designer	01:43
1.3	WEBENCH® Visualizer - Filtering	04:09
1.4	WEBENCH® Visualizer - Charting	02:17
1.5	WEBENCH® Optimizer Dial	05:14
1.6	WEBENCH® Power Designer	03:12
1.7	Viewing Your Schematic with WEBENCH® Power Designer	02:23
1.8	Viewing the BOM with WEBENCH® Power Designer	03:35
1.9	Using WEBENCH® Power Designer to View Operating Values and Charts	04:10
1.10	Optimize Circuit Design with WEBENCH® Power Designer	02:28
1.11	Electrical Simulation in WEBENCH® Power Designer	04:22
1.12	Thermal Simulation with WebTHERM™ Simulation	03:38
1.13	Creating Documentation with WEBENCH® Power Designer	01:57
1.14	Exporting from WEBENCH® Power Designer	01:30
1.15	Sharing Designs with WEBENCH® Power Designer	01:29

WEBENCH® Filter Designer Video

This video series takes you through Filter Designer and all its features inclu

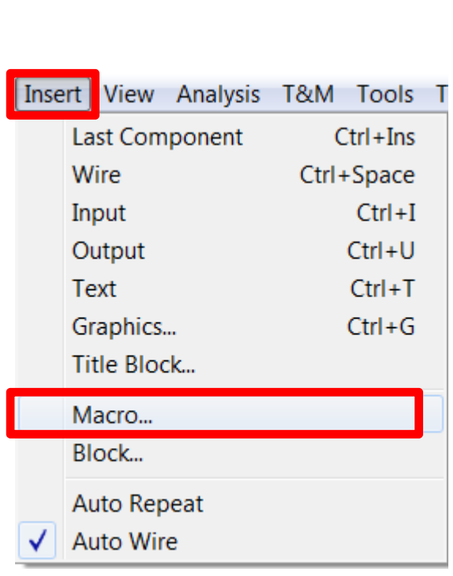
Table of contents

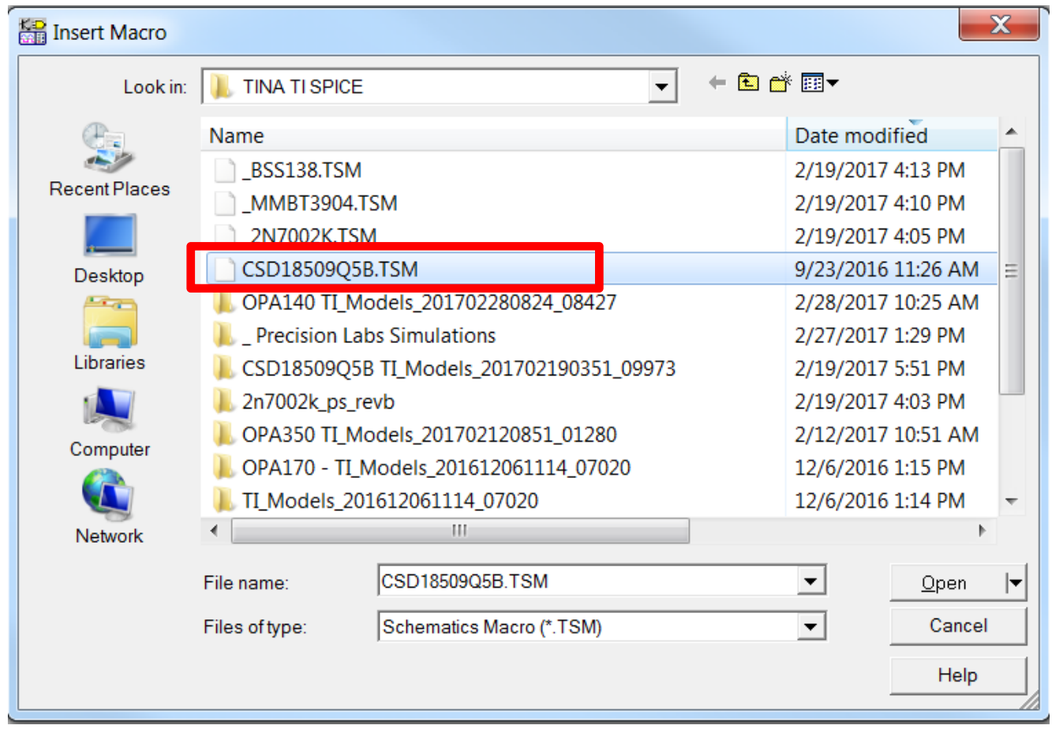
1. Videos

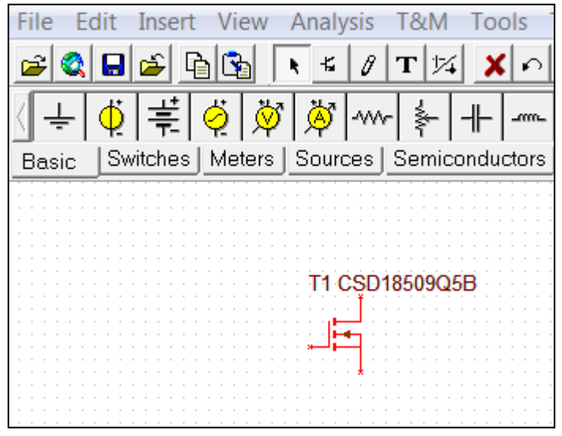
#	Title	Duration
1.1	Select, Design, Analyze	04:29
1.2	Lowpass Filter Selection	04:52
1.3	Filter Designer Visualizer	04:20
1.4	Filter Designer Design Summary	04:17
1.5	Highpass Filter Selection	05:16
1.6	Bandpass Filter Selection	05:26
1.7	Bandstop or Notch Filter Selection	05:43
1.8	Simulation Tool	05:59
1.9	Selecting Filter Order	04:18
1.10	Group Delay Step Response Specifications	05:42

How to Import a .TSM file ?

- Insert → Macro → find .TSM file → Open

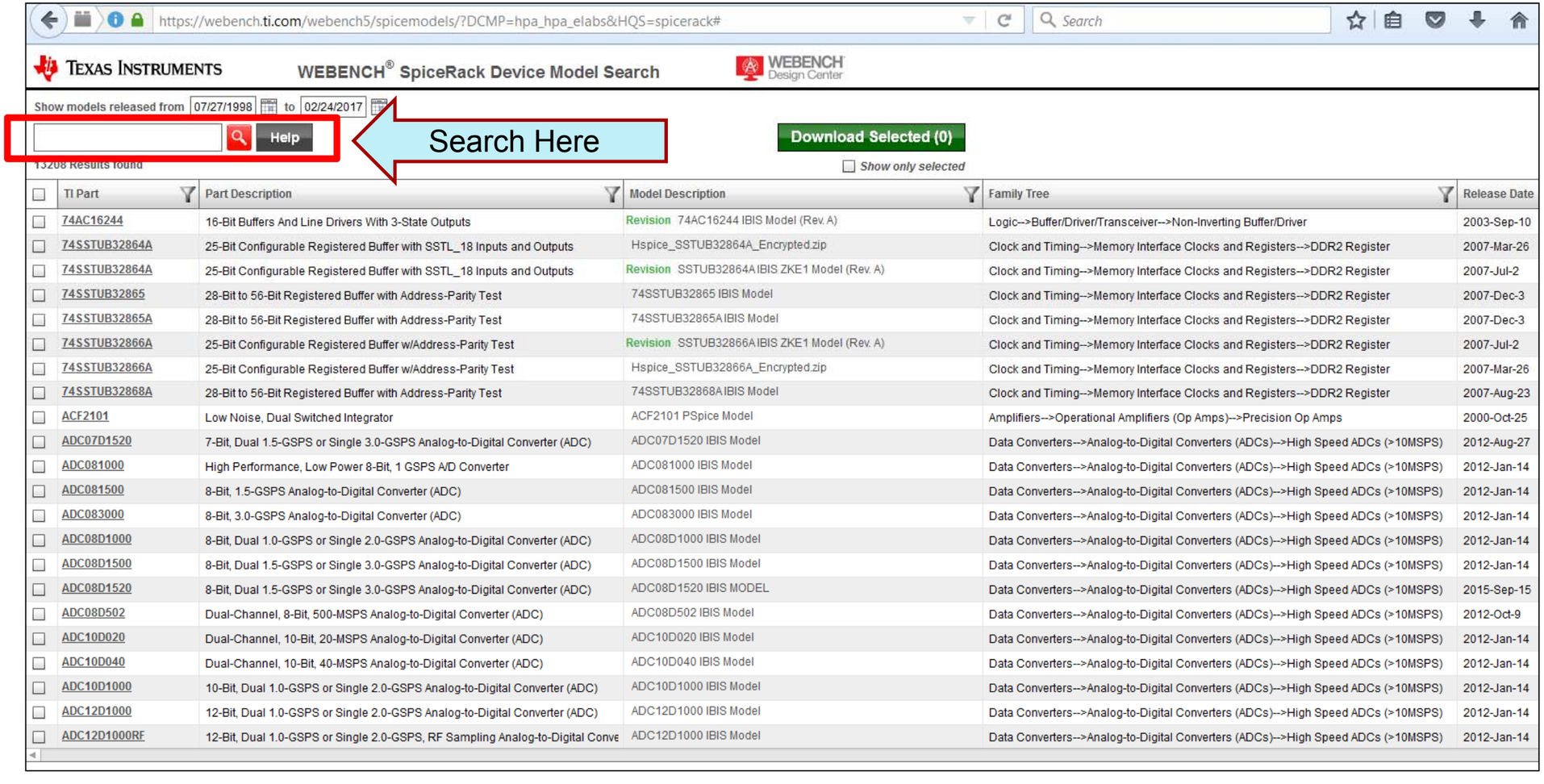






Where can you find SPICE Models?

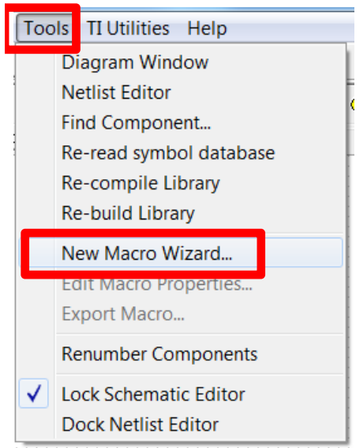
www.ti.com/spicerack

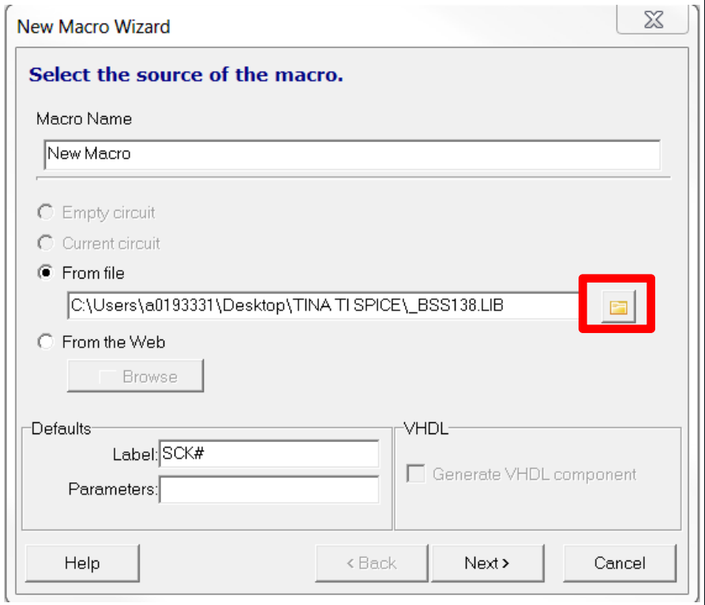


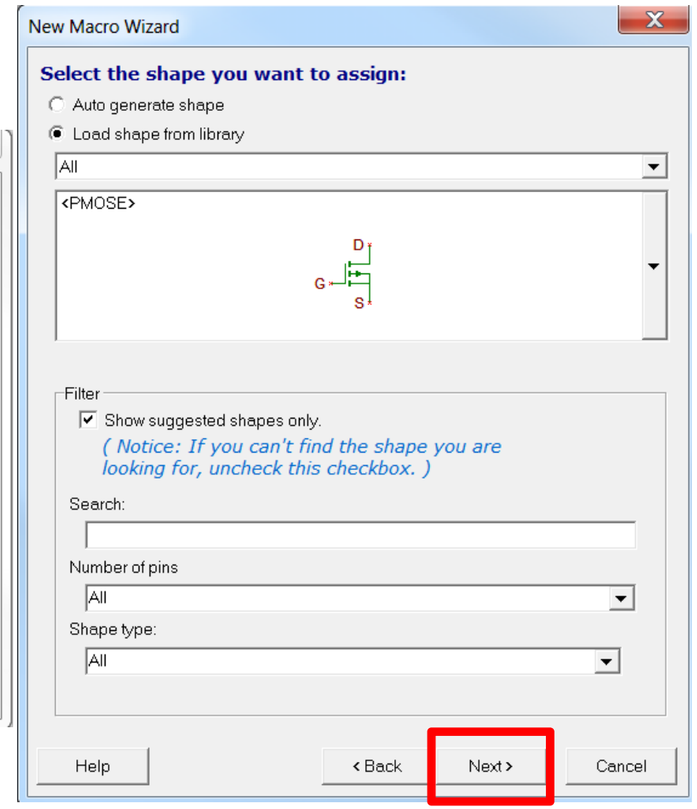
TI Part	Part Description	Model Description	Family Tree	Release Date
74AC16244	16-Bit Buffers And Line Drivers With 3-State Outputs	Revision 74AC16244 IBIS Model (Rev. A)	Logic-->Buffer/Driver/Transceiver-->Non-Inverting Buffer/Driver	2003-Sep-10
74SSTUB32864A	25-Bit Configurable Registered Buffer with SSTL_18 Inputs and Outputs	Hspice_SSTUB32864A_Encrypted.zip	Clock and Timing-->Memory Interface Clocks and Registers-->DDR2 Register	2007-Mar-26
74SSTUB32864A	25-Bit Configurable Registered Buffer with SSTL_18 Inputs and Outputs	Revision SSTUB32864A IBIS ZKE1 Model (Rev. A)	Clock and Timing-->Memory Interface Clocks and Registers-->DDR2 Register	2007-Jul-2
74SSTUB32865	28-Bit to 56-Bit Registered Buffer with Address-Parity Test	74SSTUB32865 IBIS Model	Clock and Timing-->Memory Interface Clocks and Registers-->DDR2 Register	2007-Dec-3
74SSTUB32865A	28-Bit to 56-Bit Registered Buffer with Address-Parity Test	74SSTUB32865A IBIS Model	Clock and Timing-->Memory Interface Clocks and Registers-->DDR2 Register	2007-Dec-3
74SSTUB32866A	25-Bit Configurable Registered Buffer w/Address-Parity Test	Revision SSTUB32866A IBIS ZKE1 Model (Rev. A)	Clock and Timing-->Memory Interface Clocks and Registers-->DDR2 Register	2007-Jul-2
74SSTUB32866A	25-Bit Configurable Registered Buffer w/Address-Parity Test	Hspice_SSTUB32866A_Encrypted.zip	Clock and Timing-->Memory Interface Clocks and Registers-->DDR2 Register	2007-Mar-26
74SSTUB32868A	28-Bit to 56-Bit Registered Buffer with Address-Parity Test	74SSTUB32868A IBIS Model	Clock and Timing-->Memory Interface Clocks and Registers-->DDR2 Register	2007-Aug-23
ACF2101	Low Noise, Dual Switched Integrator	ACF2101 PSpice Model	Amplifiers-->Operational Amplifiers (Op Amps)-->Precision Op Amps	2000-Oct-25
ADC07D1520	7-Bit, Dual 1.5-GSPS or Single 3.0-GSPS Analog-to-Digital Converter (ADC)	ADC07D1520 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Aug-27
ADC081000	High Performance, Low Power 8-Bit, 1 GSPS A/D Converter	ADC081000 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Jan-14
ADC081500	8-Bit, 1.5-GSPS Analog-to-Digital Converter (ADC)	ADC081500 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Jan-14
ADC083000	8-Bit, 3.0-GSPS Analog-to-Digital Converter (ADC)	ADC083000 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Jan-14
ADC08D1000	8-Bit, Dual 1.0-GSPS or Single 2.0-GSPS Analog-to-Digital Converter (ADC)	ADC08D1000 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Jan-14
ADC08D1500	8-Bit, Dual 1.5-GSPS or Single 3.0-GSPS Analog-to-Digital Converter (ADC)	ADC08D1500 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Jan-14
ADC08D1520	8-Bit, Dual 1.5-GSPS or Single 3.0-GSPS Analog-to-Digital Converter (ADC)	ADC08D1520 IBIS MODEL	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2015-Sep-15
ADC08D502	Dual-Channel, 8-Bit, 500-MSPS Analog-to-Digital Converter (ADC)	ADC08D502 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Oct-9
ADC10D020	Dual-Channel, 10-Bit, 20-MSPS Analog-to-Digital Converter (ADC)	ADC10D020 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Jan-14
ADC10D040	Dual-Channel, 10-Bit, 40-MSPS Analog-to-Digital Converter (ADC)	ADC10D040 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Jan-14
ADC10D1000	10-Bit, Dual 1.0-GSPS or Single 2.0-GSPS Analog-to-Digital Converter (ADC)	ADC10D1000 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Jan-14
ADC12D1000	12-Bit, Dual 1.0-GSPS or Single 2.0-GSPS Analog-to-Digital Converter (ADC)	ADC12D1000 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Jan-14
ADC12D1000RF	12-Bit, Dual 1.0-GSPS or Single 2.0-GSPS, RF Sampling Analog-to-Digital Conve	ADC12D1000 IBIS Model	Data Converters-->Analog-to-Digital Converters (ADCs)-->High Speed ADCs (>10MSPS)	2012-Jan-14

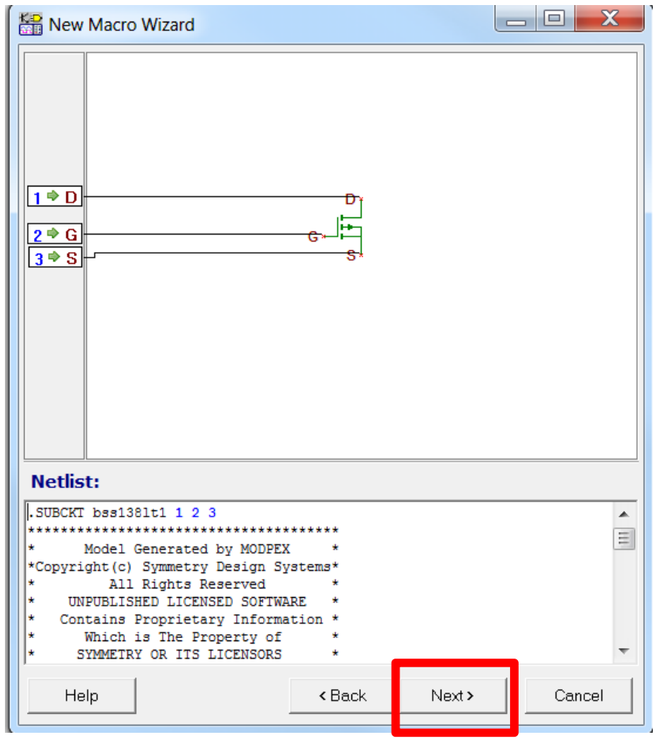
How to Import a .LIB file ?

- Tools → New Macro Wizard
- Press the Yellow Button and Choose your .LIB file. 
- Chose Next, then Nexts again.
- Save off new .TSM file





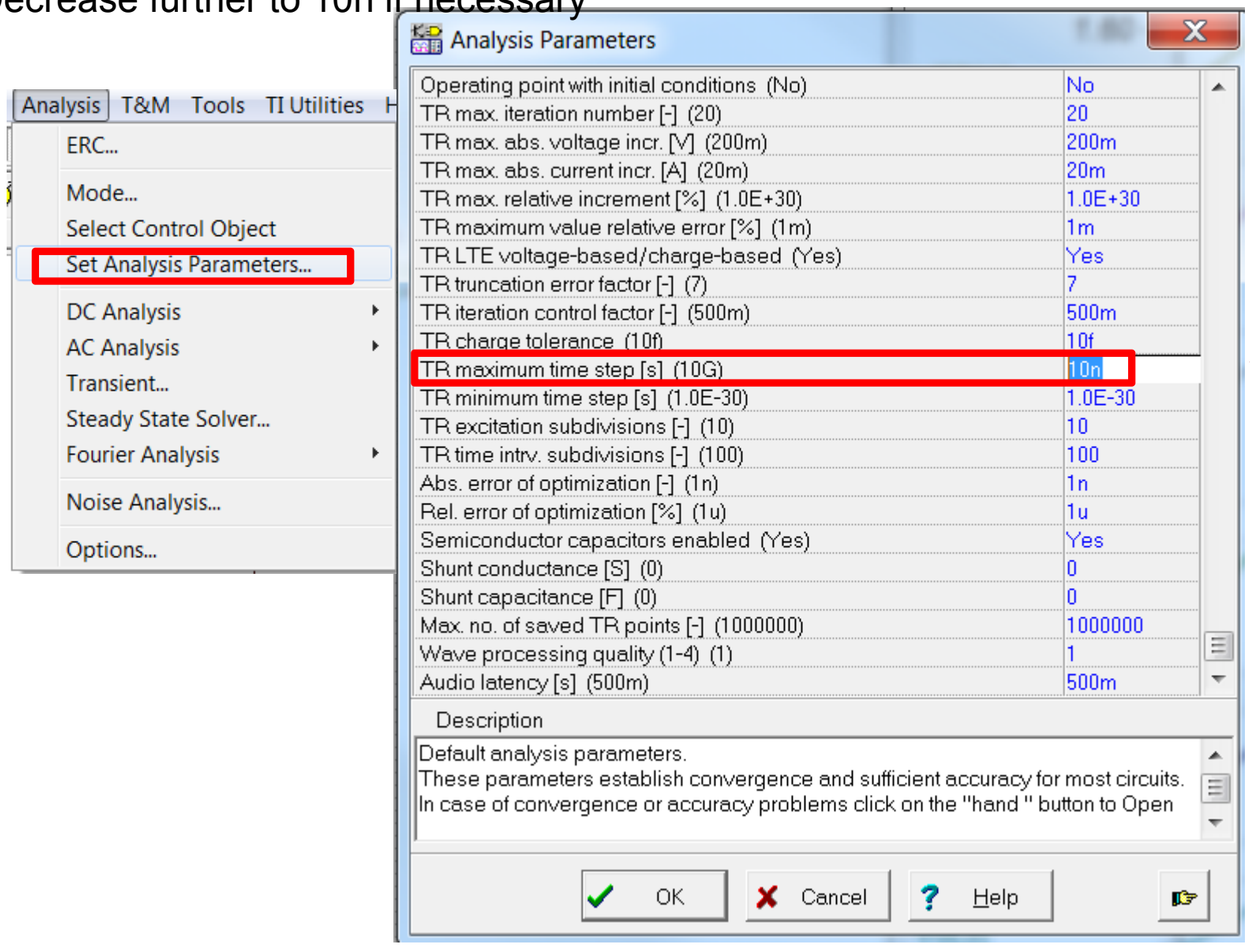




Will Not Converge / Need More Resolution

CONVERGENCE ISSUES

- Go to Analysis → Ste Analysis Parameters → “TR maximum time step [s]
  - Decrease from default 10G to 1u (to start)
  - Decrease further to 10n if necessary

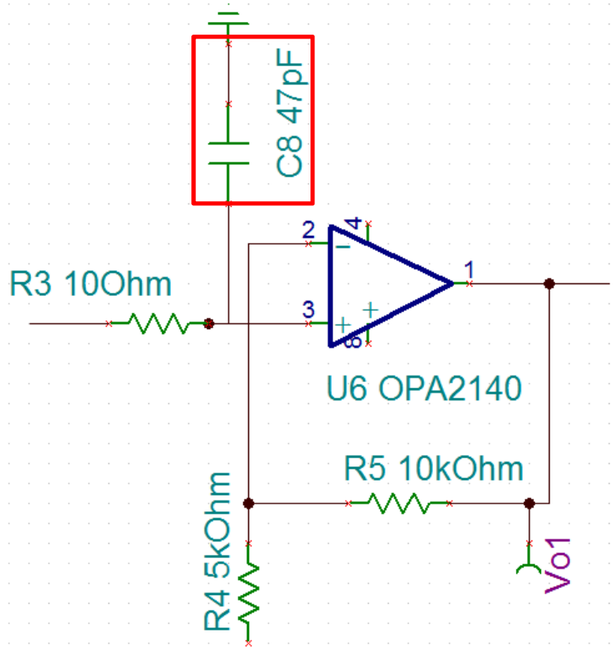


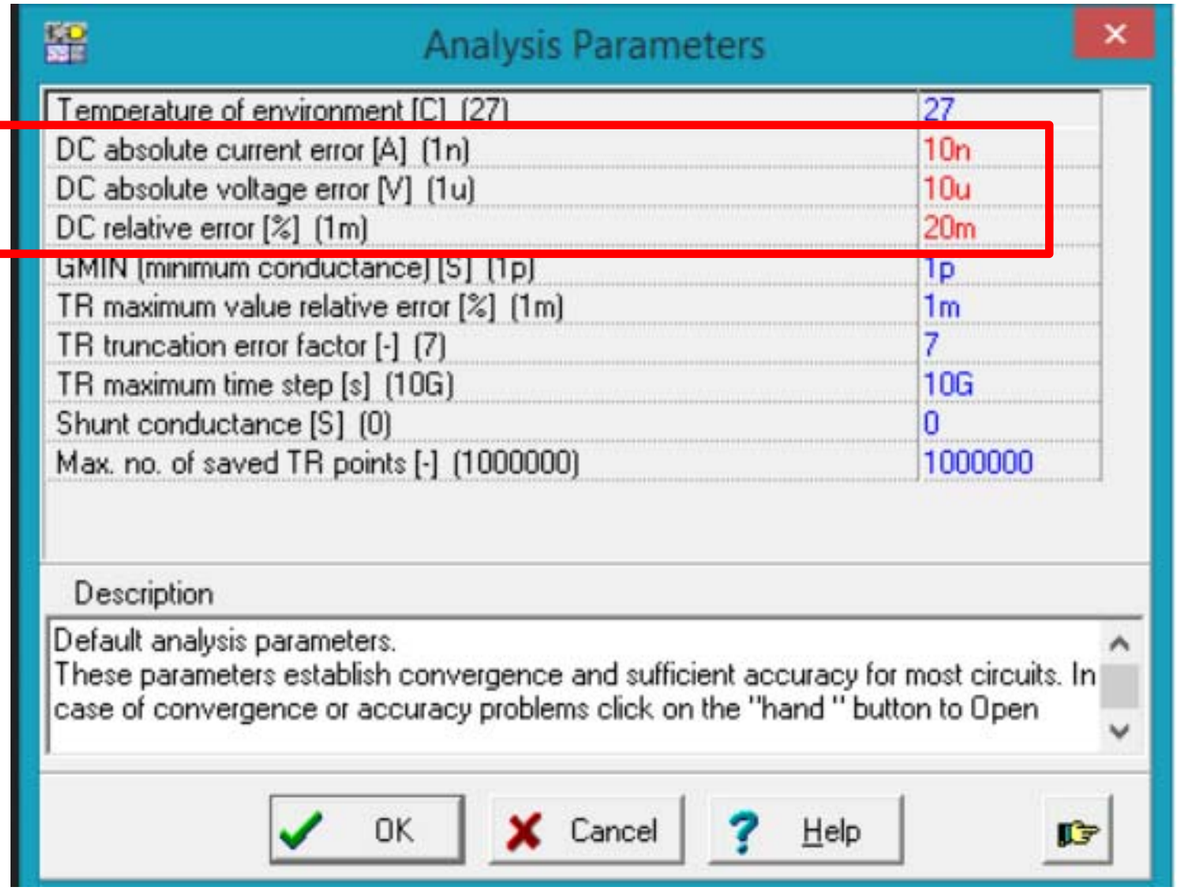
Try 1u to start
Then go to 10n or more

Capacitor on Operation Amplifier Input Causes Convergence Error

CONVERGENCE ISSUES

- Problem: Capacitor added to input of Operation Amplifier causes a Convergence Error.
- The problem is that due to the small capacitance value inserted, the program subdivides times steps in order to reach the required accuracy and the time step goes too low, which may cause numerical instability.
- Set Analysis Parameters
  - DC absolute current error [A] (1n) → set to 10n
  - DC absolute voltage error [V] (1u) → set to 10u
  - DC relative error [%] (1m) → set to 20ms

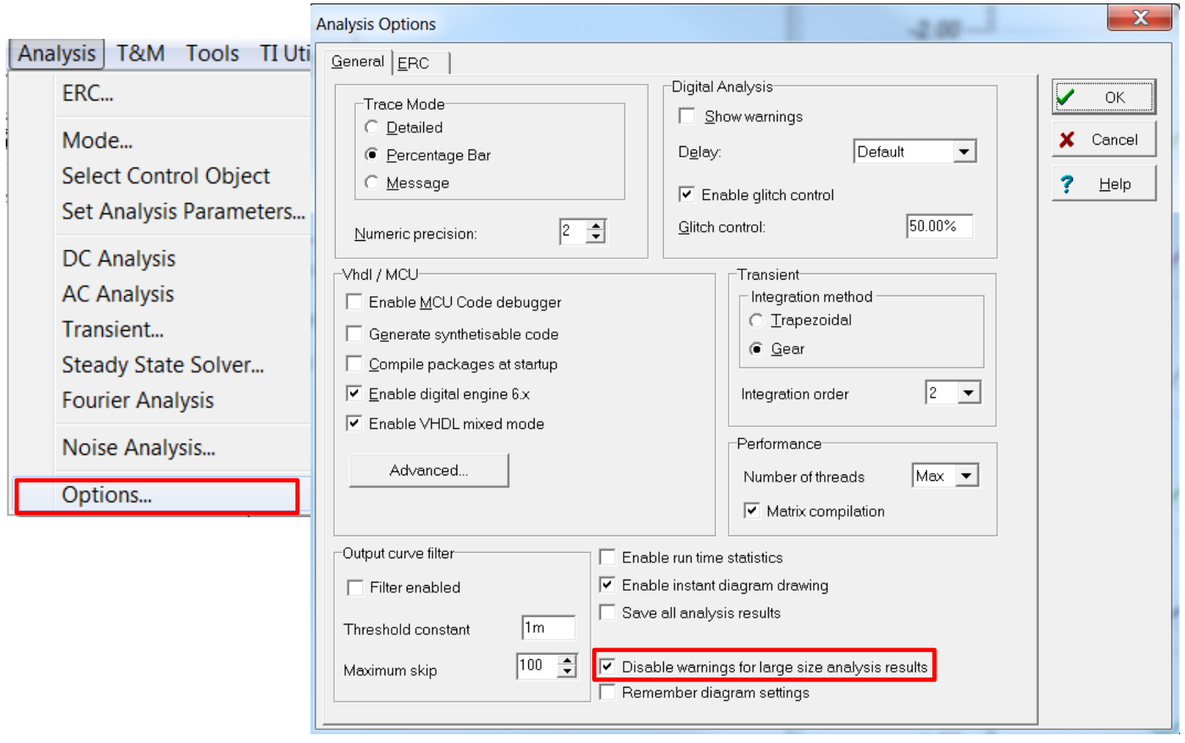


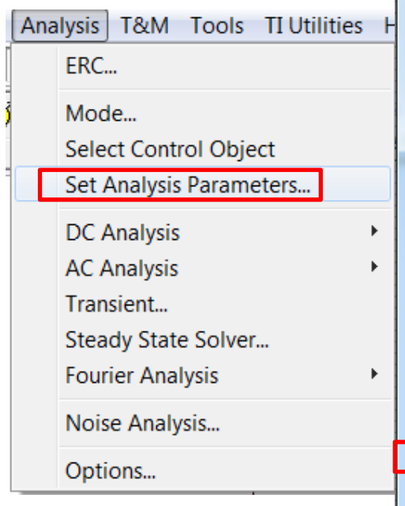


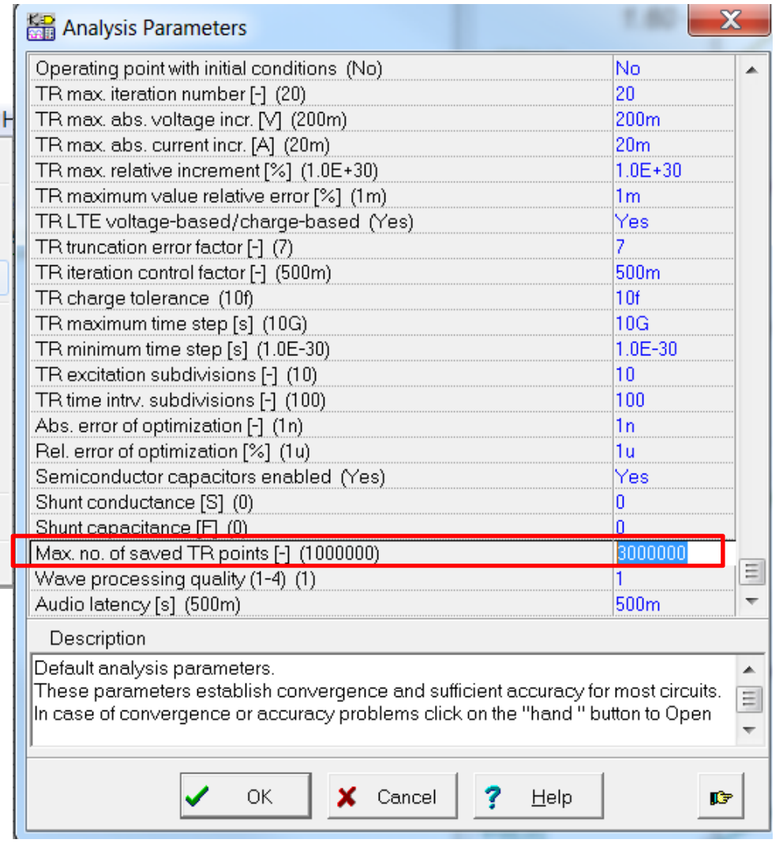
Need More Memory?

CONVERGENCE ISSUES

- Analysis → Options … → Check “Disable Warnings for Large Size…”
- Analysis → Set Analysis Parameters →Max no. of saved TR points
  - Increase to 3000000







Output Waveform is Truncated – Search our E2E Forums http://e2e.ti.com

CONVERGENCE ISSUES

- Square wave output of Signal Generator is truncated
- Solution is to change "**TR excitation subdivisions**" from default of 10 to 1000.
- Analysis → Set Analysis Parameters… → Scroll down to Bottom to find Parameter
- See all the details on this particular issue our E2E Forums: http://e2e.ti.com/support/development_tools/webench_design_center/f/234/t/371450
- TI's E2E forums are the place to ask questions of TI applications engineers