Design Considerations for Modern Op Amps

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Texas Instruments

Detailed agenda

- **Introduce debug problem**
- **Op-amp stability review**
  - Poles & zeros
  - Capacitive loading
  - Loop gain, Aol, 1/β and rate of closure
- **Op-amp output impedance**
  - Zo vs Zout
  - “Trust but verify” series
  - Interaction with reactive loads and impact on Aol
- **Real world applications and commonly encountered issues**
  - TLV07 vs. OP07
  - Driving an ADC
  - Using different op-amp topologies

Debug Problem

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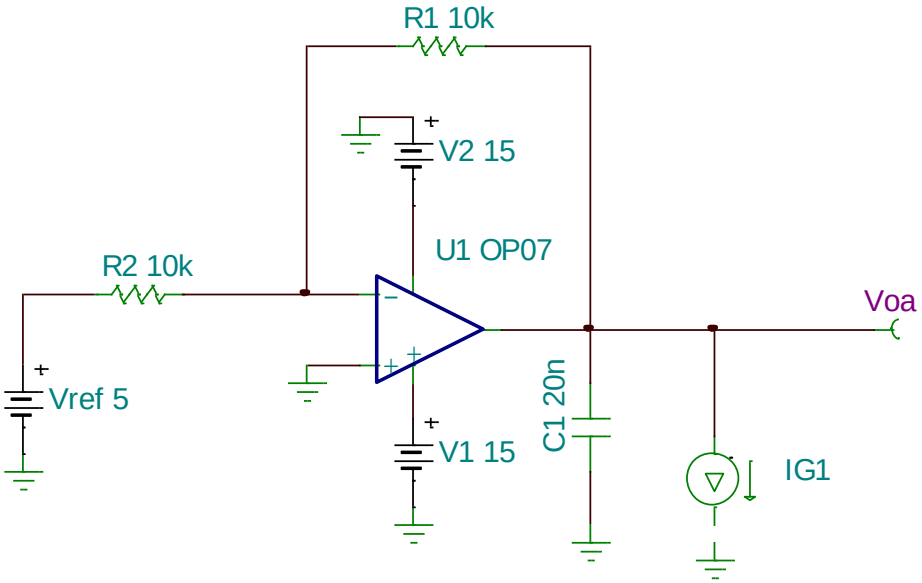
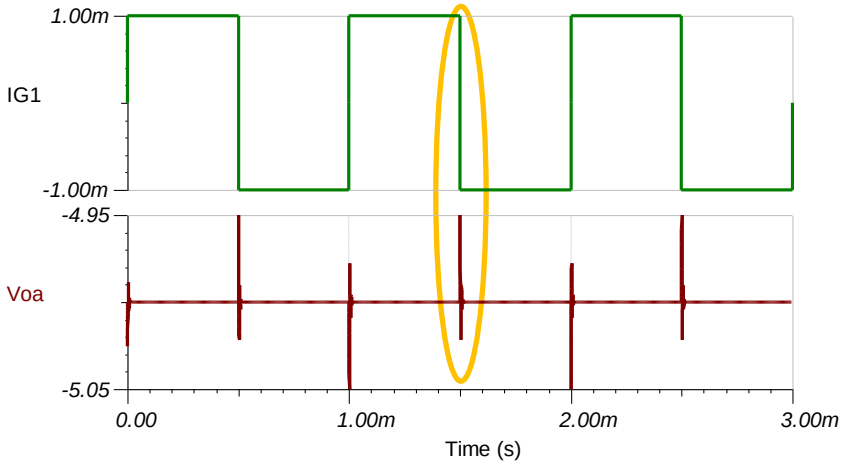
TLV07 versus OP07C

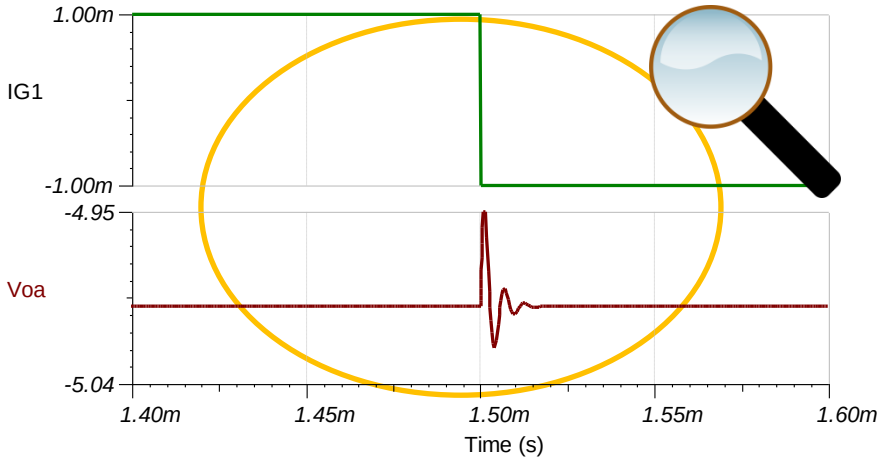
Specification Comparison

Parameter	Unit	OP07C	TLV07
Supply Voltage Range	V	6 to 36	2.7 to 36
GBW MHz	MHz (Typ)	0.6	1
Slew Rate	V/µs (typ)	0.3	0.4
Rail-to-Rail		-	Out
Vos	µV (Max)	-	100
Vos	µV (Typ)	60	50
Offset Drift	µV/°C (Typ)	0.5	0.9
Input Bias Current	nA (Typ)	1.8	0.04
Vn @ 1kHz	nV/√Hz (Typ)	9.8	19
Quiescent Current	mA (Typ, Max)	2.4, 5	0.95, 1.8
CMRR dB (typ)	dB (Typ)	120	120
Architecture		Bipolar	CMOS
Operating Temperature Range	°C	0 to 70	-40 to 125
Package Group		SOIC, PDIP, SO-8	SOIC
Price (1ku)	USD ($)	0.23	0.35

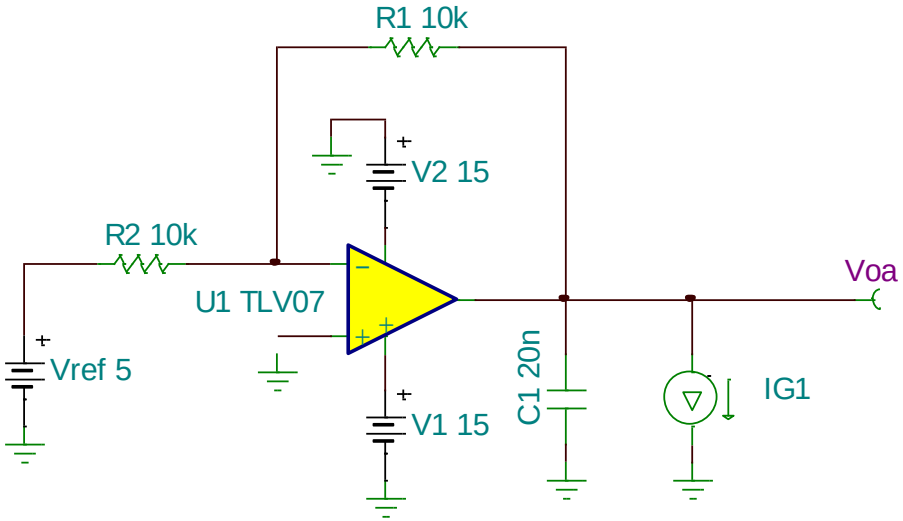
20nF Cap Load on OP07

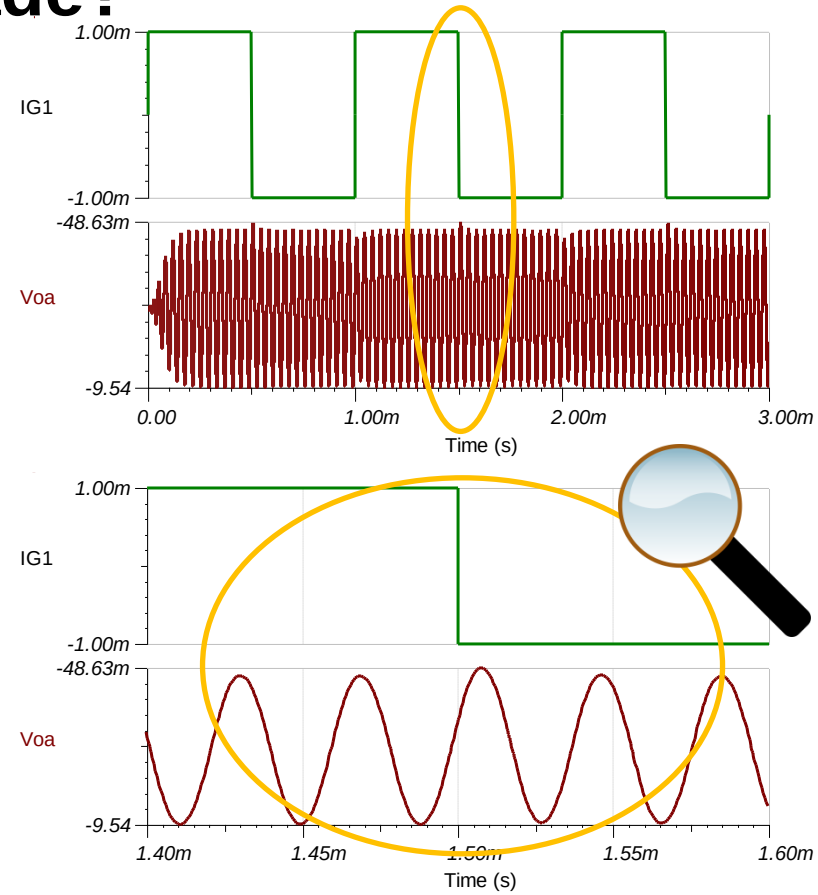






TLV07: Upgrade or downgrade?





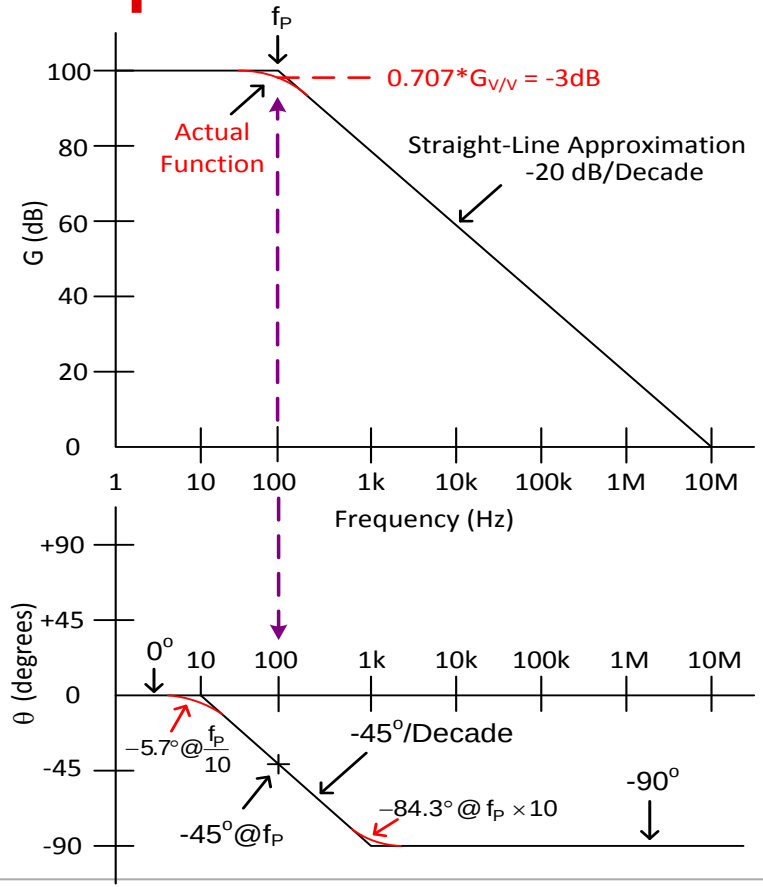
Oscillation at 25.97kHz!

TINA-TI Simulator

- All of the simulations in these slides are done with TINA-TI
- Free Download: http://www.ti.com/tool/TINA-TI
- Design files are embedded in this presentation

Op amp stability review

Bode plots: Pole



$$G_{v/v} = \frac{V_{out}}{V_{in}} = \frac{G_{dc}}{i\left(\frac{f}{f_P}\right) + 1}$$ As a complex number

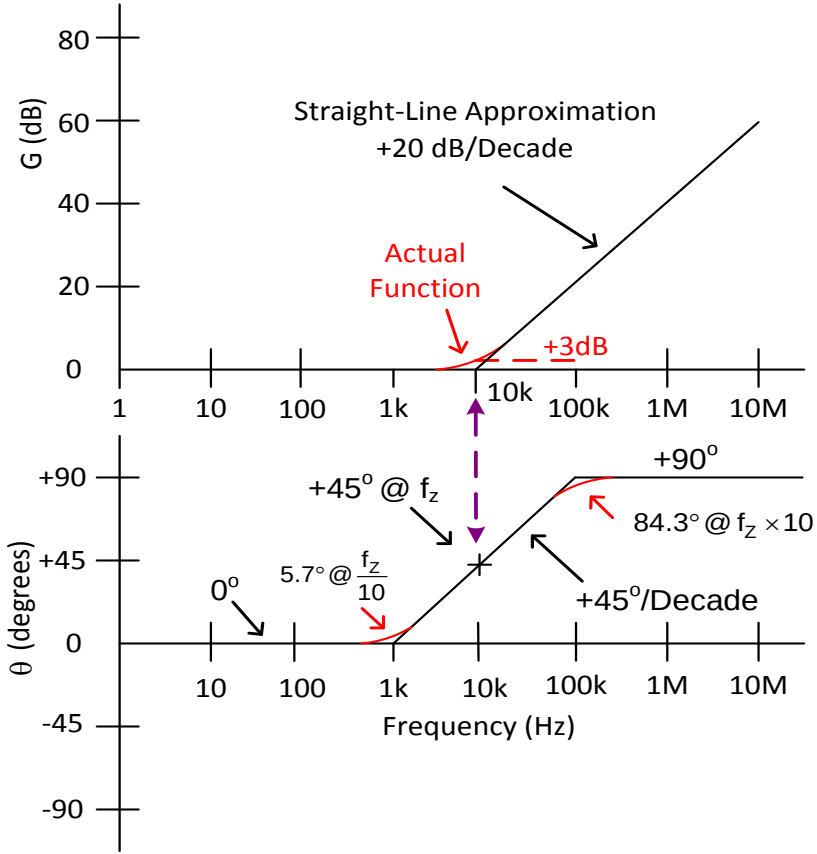
$$G_{v/v} = \frac{V_{out}}{V_{in}} = \frac{G_{dc}}{\sqrt{\left(\frac{f}{f_P}\right)^2 + 1}}$$ Magnitude

$$\Theta = -\tan^{-1}\left(\frac{f}{f_P}\right)$$ Phase

$$G_{dB} = 20\mathrm{Log}(G_{v/v})$$ Magnitude in dB

- Pole Location = f_P (Cutoff Freq)
- Magnitude ($f < f_P$) = G_{dc} (e.g. 100dB)
- Magnitude ($f = f_P$) = -3dB
- Magnitude ($f > f_P$) = -20dB/Decade
- Phase ($f = f_P$) = -45°
- Phase ($0.1f_P < f < 10f_P$) = -45°/Decade
- Phase ($f > 10f_P$) = -90°
- Phase ($f < 0.1f_P$) = 0°

Bode plots: Zero



$$G_{v/v} = \frac{V_{out}}{V_{in}} = G_{dc}\left[i\left(\frac{f}{f_Z}\right) + 1\right]$$ As a complex number

$$G_{v/v} = \frac{V_{out}}{V_{in}} = G_{dc}\sqrt{\left(\frac{f}{f_Z}\right)^2 + 1}$$ Magnitude

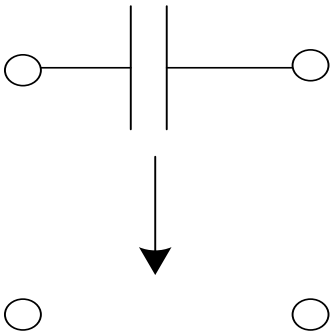
$$\Theta = \tan^{-1}\left(\frac{f}{f_Z}\right)$$ Phase

$$G_{dB} = 20\mathrm{Log}(G_{v/v})$$ Magnitude in dB

- Zero Location = f_Z
- Magnitude ($f < f_Z$) = 0dB
- Magnitude ($f = f_Z$) = +3dB
- Magnitude ($f > f_Z$) = +20dB/Decade
- Phase ($f = f_Z$) = +45°
- Phase ($0.1f_Z < f < 10f_Z$) = +45°/Decade
- Phase ($f > 10f_Z$) = +90°
- Phase ($f < 0.1f_Z$) = 0°

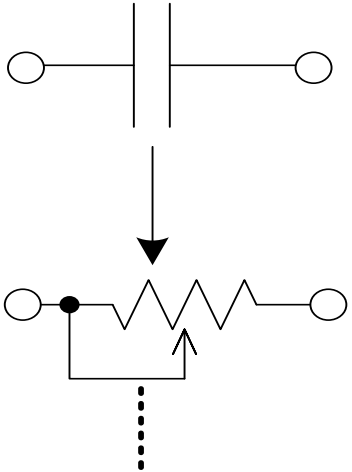
Capacitor: Intuitive model

DC X_C



OPEN

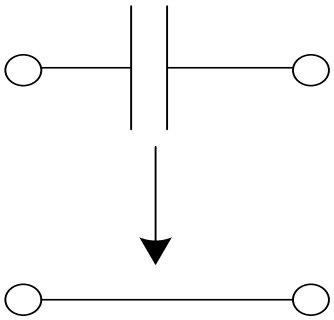
DC < X_C < Hi-f



frequency controlled resistor

$X_C = 1/(2\pi fC)$

Hi-f X_C



SHORT

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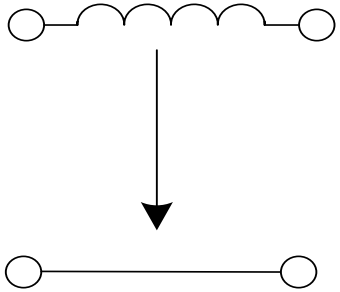
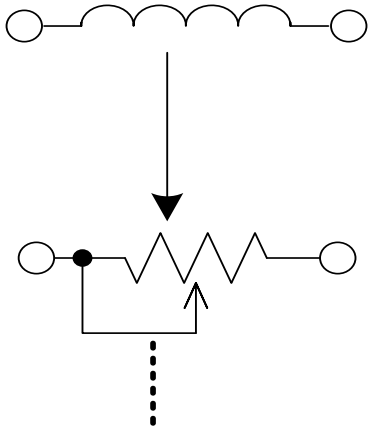
Inductor: Intuitive model

DC X_L



SHORT

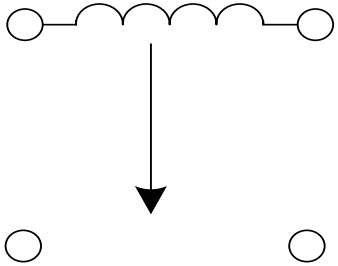
DC < X_L < Hi-f



frequency controlled resistor

$X_L = 2\pi fL$

Hi-f X_L



OPEN

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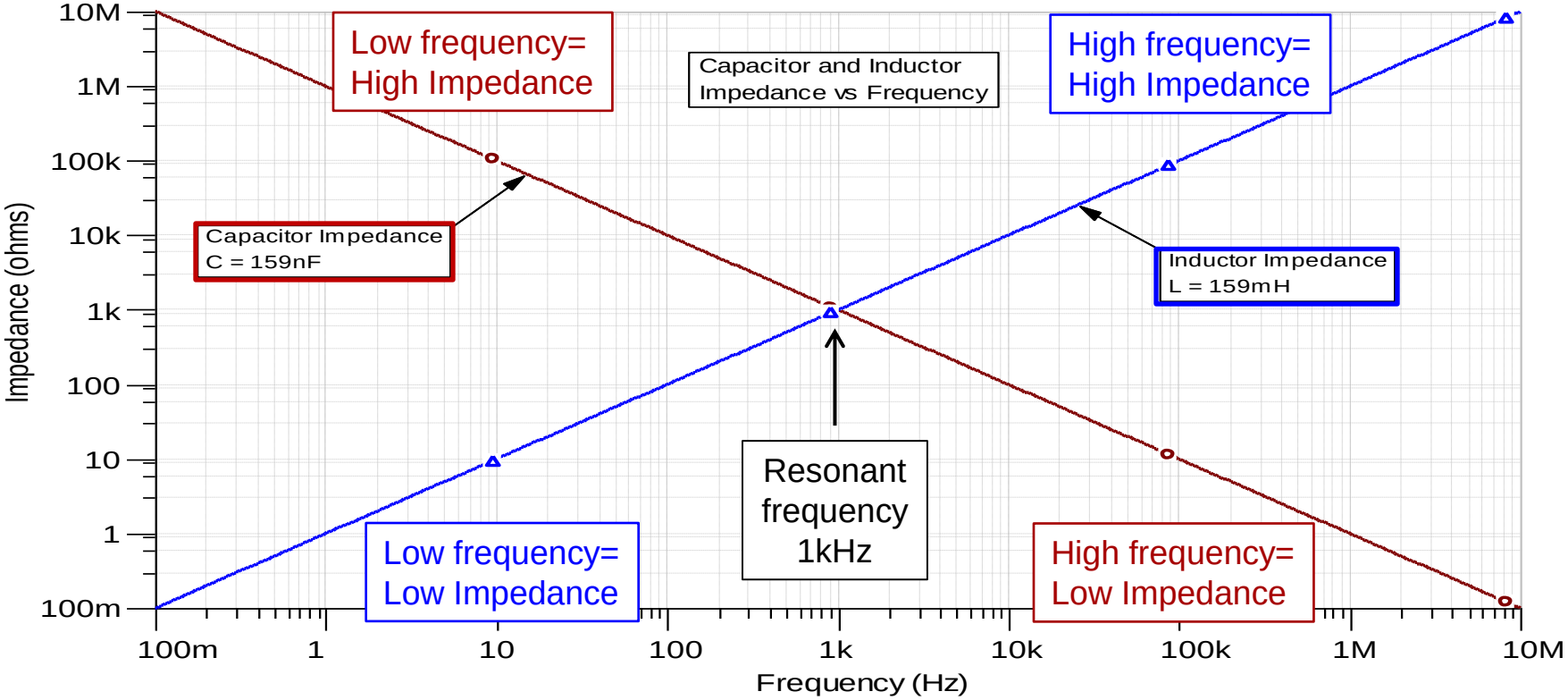
Capacitor and inductor: Impedance vs frequency



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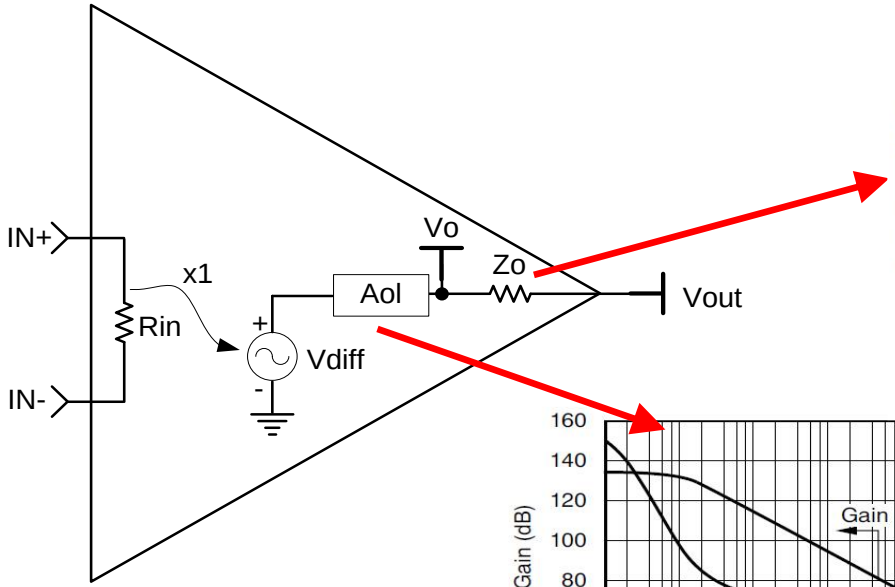
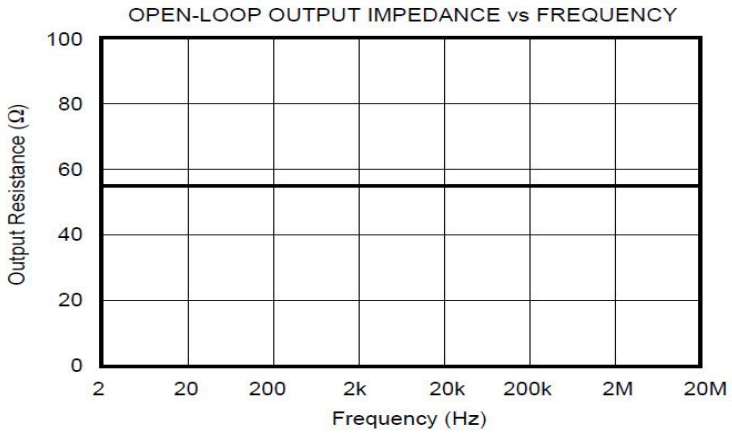
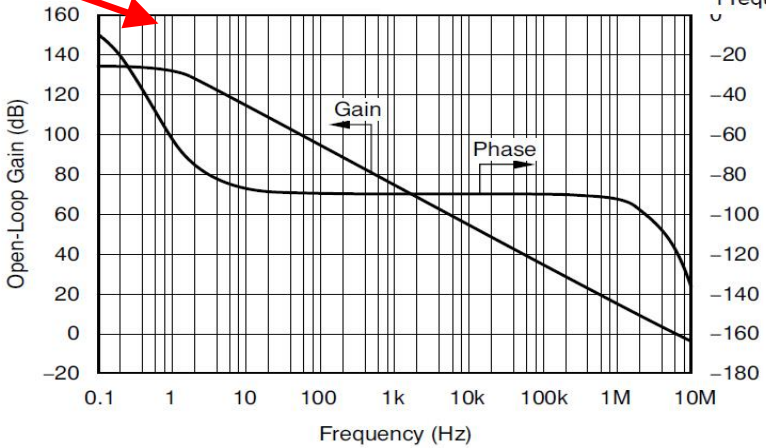
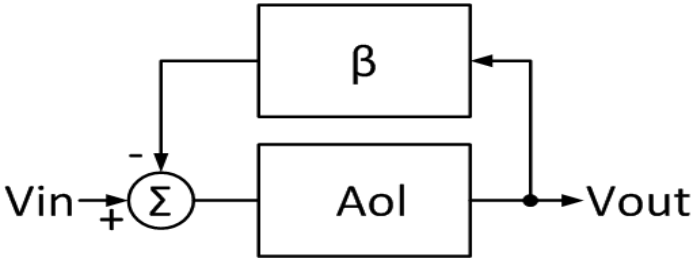
Op amp: Open loop model

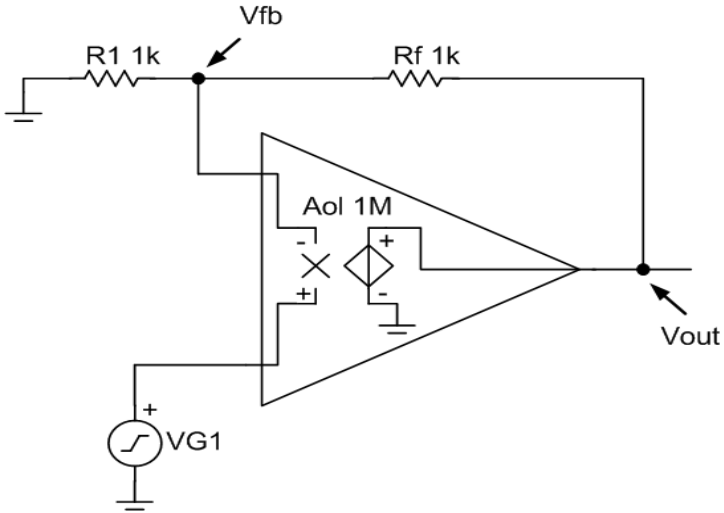






Op amp: Closed loop model





$$A_{ol} = \text{Open loop Gain}$$

$$\beta = \text{Feedback Factor} = \frac{V_{fb}}{V_{out}} = \frac{R_1}{R_1 + R_f}$$

$$A_{cl} = \text{Closed Loop Gain} = \frac{A_{ol}}{1 + A_{ol}\beta}$$

$$A_{ol}\beta = \text{Loop Gain}$$

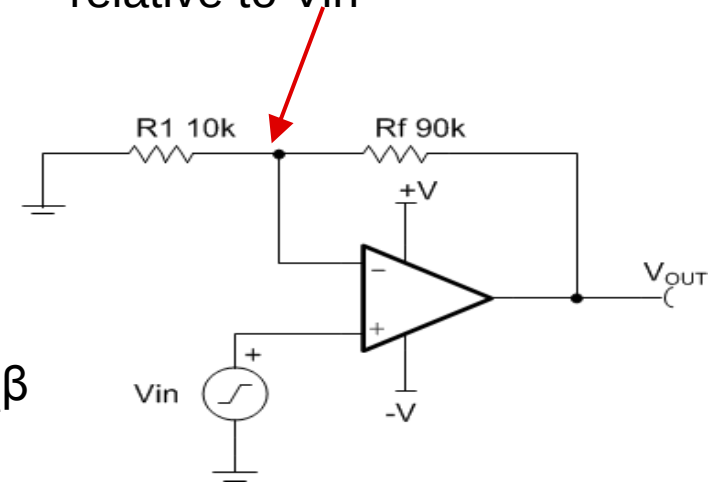
$$A_{cl} = \lim_{A_{ol} \to \infty} \left(\frac{A_{ol}}{1 + A_{ol}\beta} \right) = \frac{1}{\beta} = 1 + \frac{R_f}{R_1}$$

When is an amplifier unstable?

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}$$

- A circuit is unstable when $A_{OL}\beta = -1$
- $A_{OL}\beta = -1$ sets the denominator of $A_{CL} = 0$
- $A_{OL}\beta = -1$ when $A_{OL}\beta(dB) = 0dB$ and phase shift($A_{OL}\beta$) = 180°
  - Phase shift is relative to the DC phase

$A_{OL}\beta = -1$ when the phase at V_{FB} has shifted 180^0 relative to Vin



Phase Margin (PM)

How close the system is to a 180° phase shift in $A_{OL}\beta$

- PM = Phase($A_{OL}\beta$) when Gain($A_{OL}\beta$) = 0dB
- Ex: 10° phase margin = 170° phase shift in $A_{OL}\beta$

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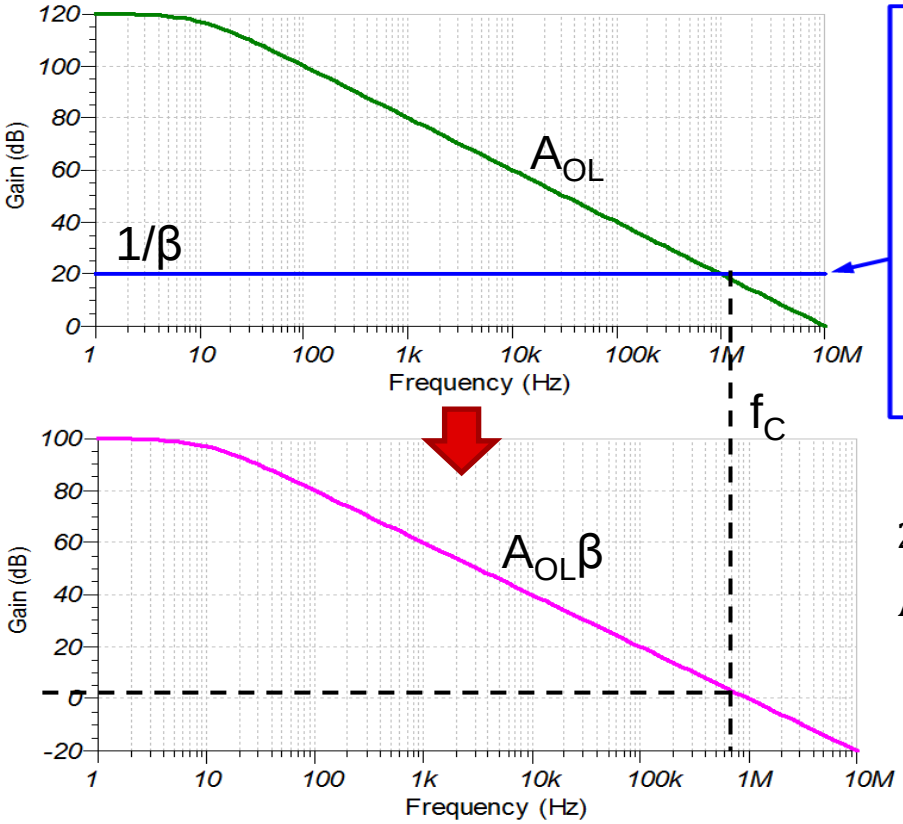
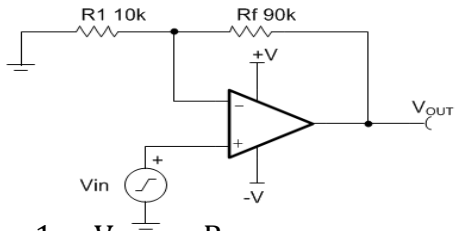
Loop gain magnitude: $A_{OL}\beta$





$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20\log(10) = 20dB$$

Loop gain in dB:

$$20\log(A_{OL}\beta) = 20\log(A_{OL}) - 20\log\left(\frac{1}{\beta}\right)$$

$$A_{OL}\beta(dB) = A_{OL}(dB) - \frac{1}{\beta}(dB)$$

Note: $A_{OL}\beta(dB) = 0dB$ when A_{OL} and $\frac{1}{\beta}$ intersect

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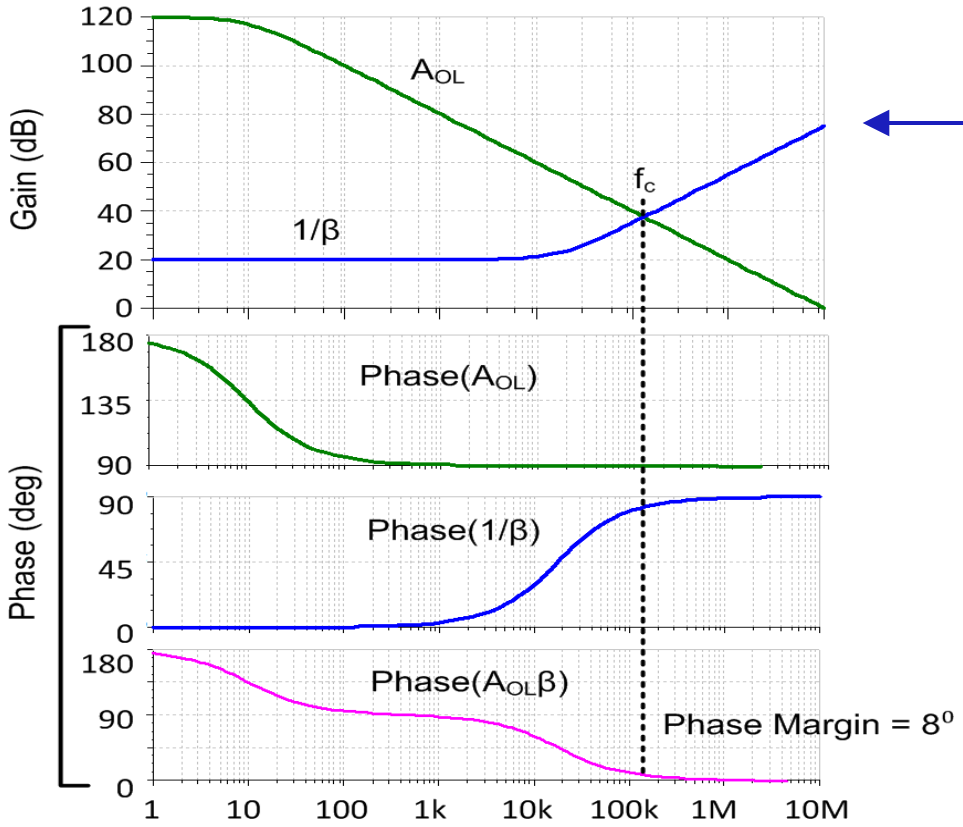
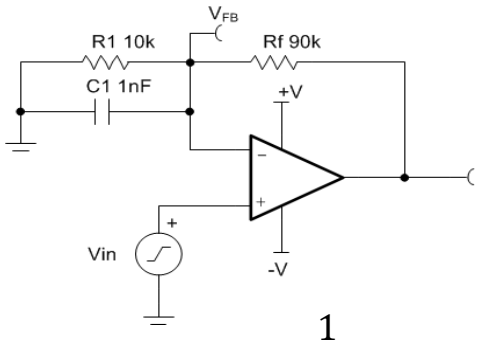
Loop gain phase: phase($A_{OL}\beta$)





C1 introduces a zero in $\frac{1}{\beta}$

$$\frac{1}{\beta} = \frac{Z_f}{Z_1} + 1$$

At DC the capacitor is open, so gain = 10V/V. At high frequency the capacitor causes Z_1 to decrease, so gain increases by +20dB/decade

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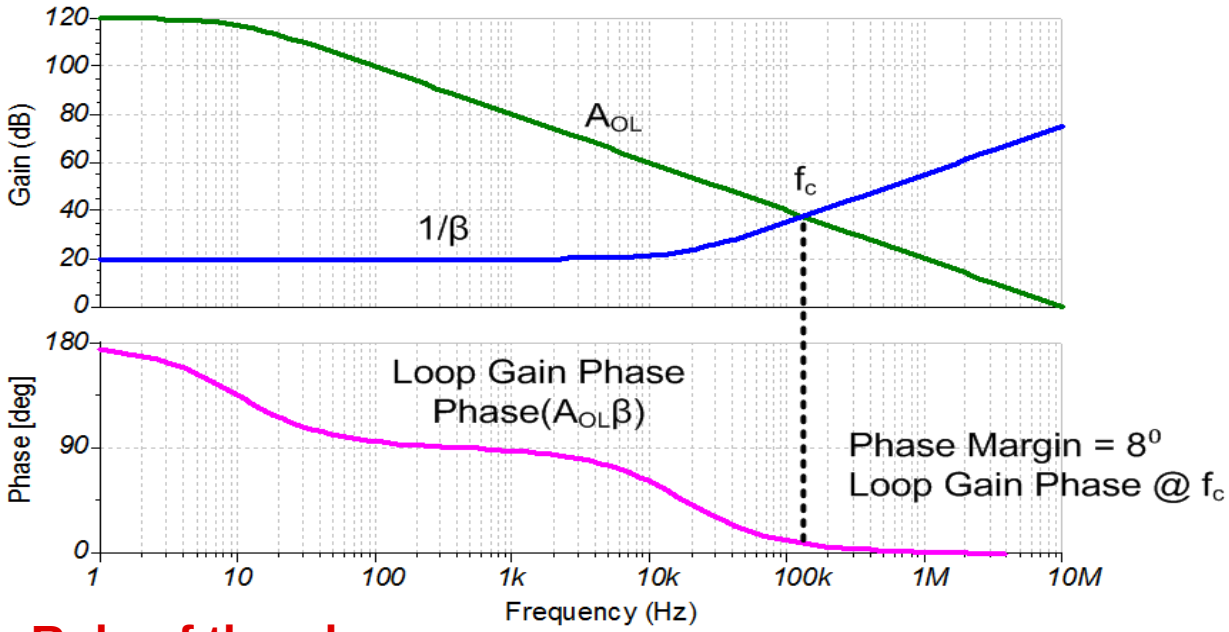
Phase margin



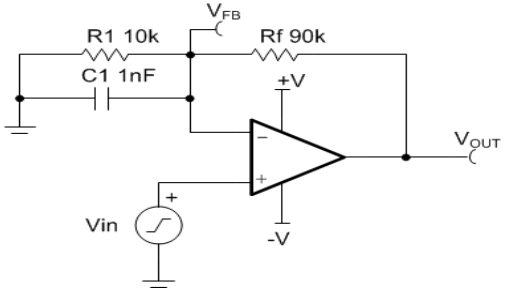
Rule of thumb:

Phase margin > 45° is required for optimal stability!

Phase margin < 45° is considered “marginally stable.”

This does not ensure a robust design over process variation

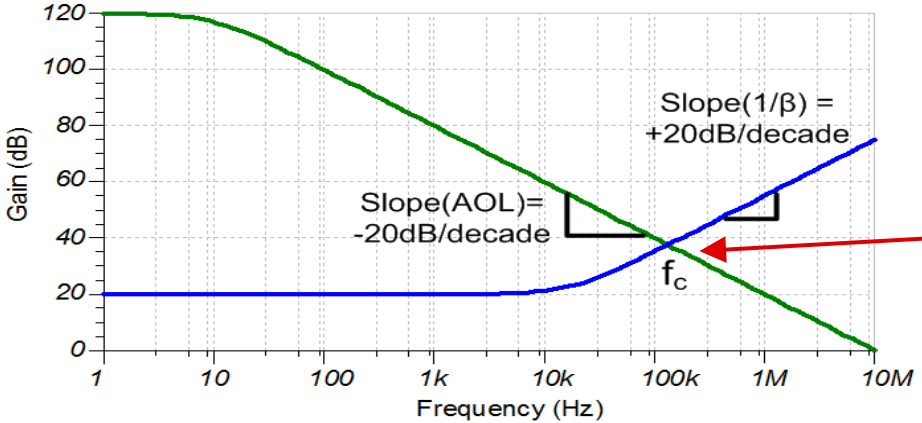
Rate of closure: Unstable example



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = 10\left(\frac{f}{f_C} + 1\right)$$

1/β(dB) = 20dB at DC, then increases by +20dB/decade after the zero frequency

Rule of thumb: Rate of closure = 20dB is required for optimal stability!



$$\text{Rate of Closure} = \left|\text{Slope}(A_{OL}) - \text{Slope}\left(\frac{1}{\beta}\right)\right|$$

$$\text{Rate of Closure} = |-20\text{dB} - (+20\text{dB})| = 40\text{dB}$$

Unstable because rate of closure > 20dB!

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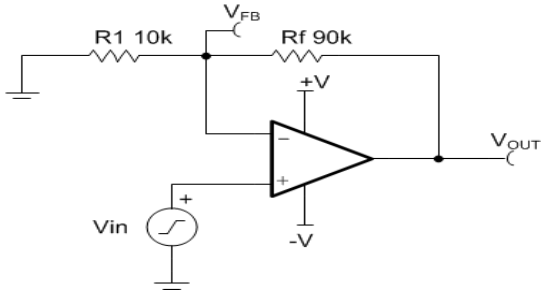
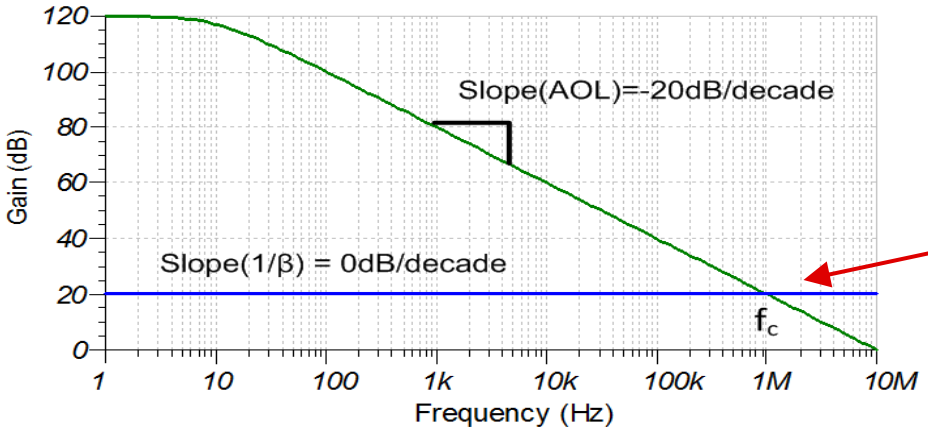
Rate of closure: Stable example



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20\log(10) = 20dB$$

Rule of thumb: Rate of closure = 20dB is required for optimal stability!



$$\text{Rate of Closure} = \left|\text{Slope}(A_{OL}) - \text{Slope}\left(\frac{1}{\beta}\right)\right|$$

$$\text{Rate of Closure} = |-20dB - 0dB| = 20dB$$

Stable because rate of closure = 20dB!

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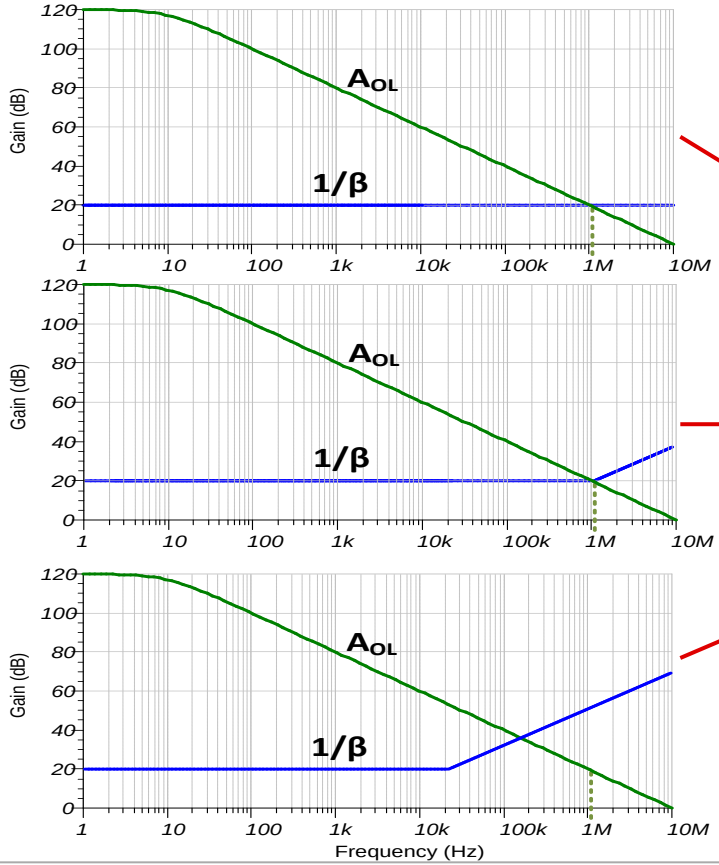
Rate of closure (ROC) and phase margin



ROC (dB/decade)	Phase Margin (°)
20	45 < PM < 90
20 < ROC < 40	45
40	0 < PM < 45

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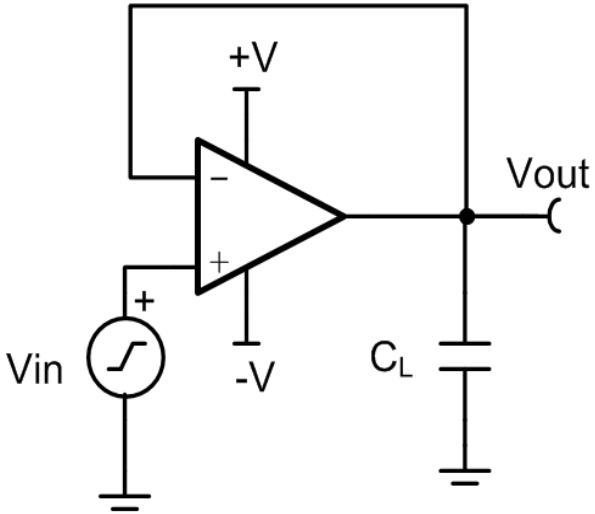
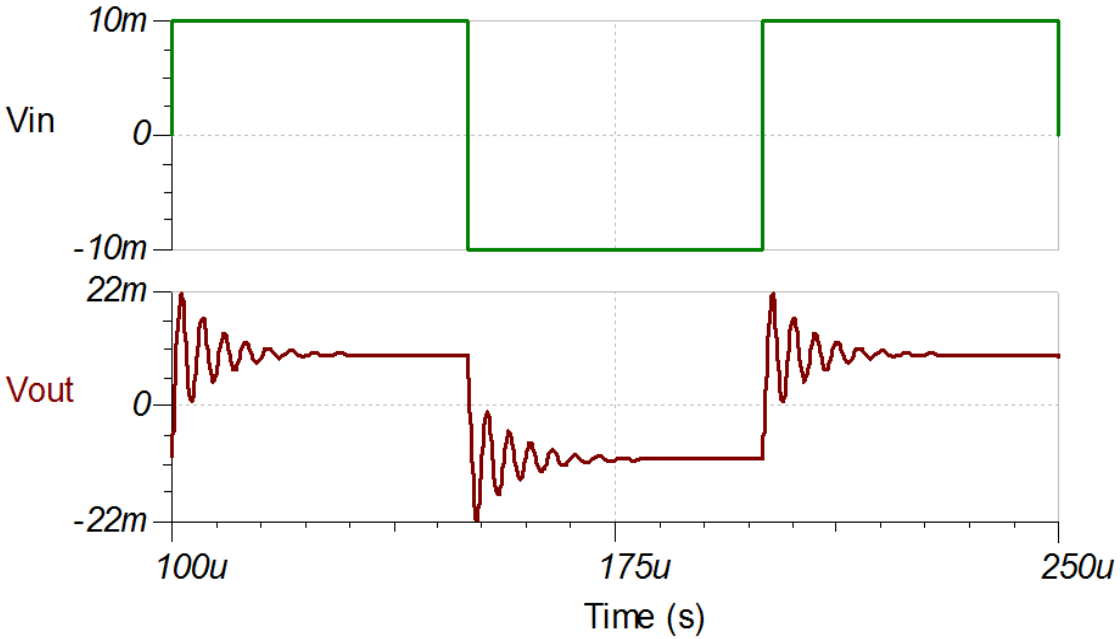
Why do capacitive loads cause instability?





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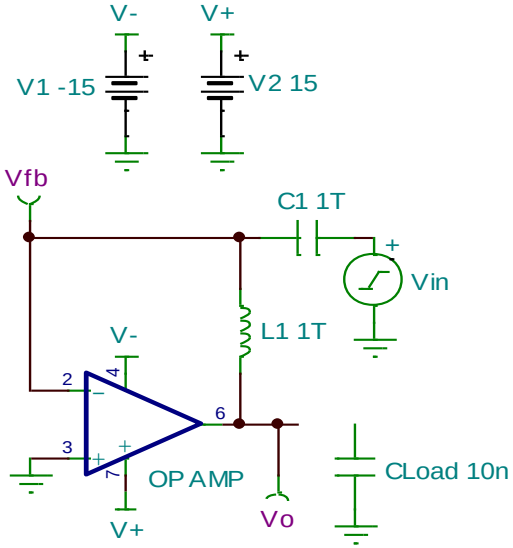
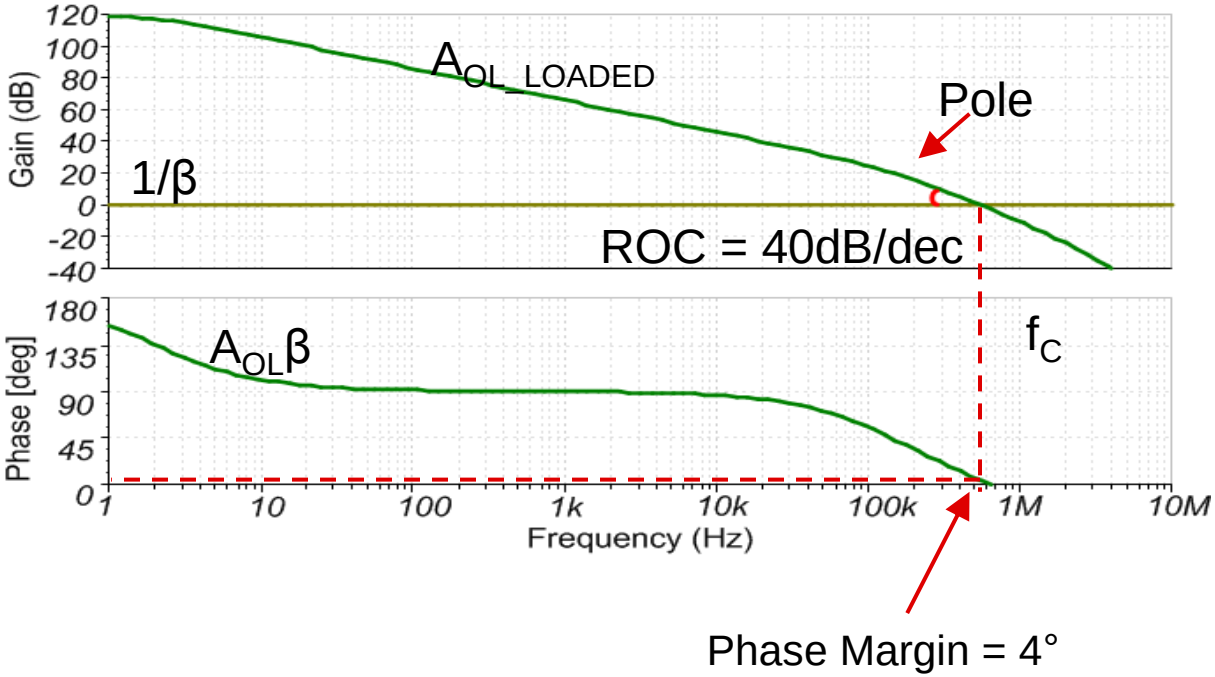
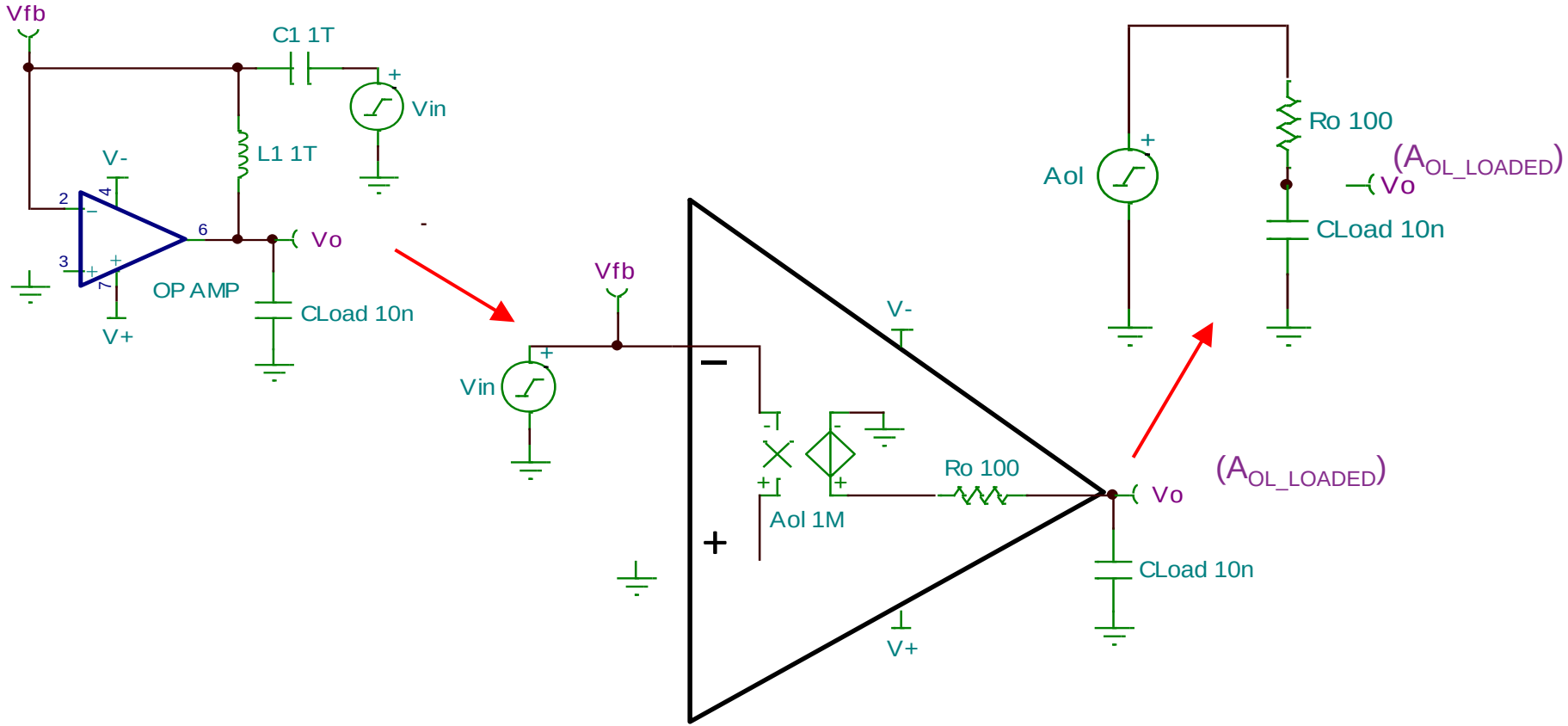
Simulating the effects of output capacitance

Run open-loop analysis on buffer circuit with capacitive load

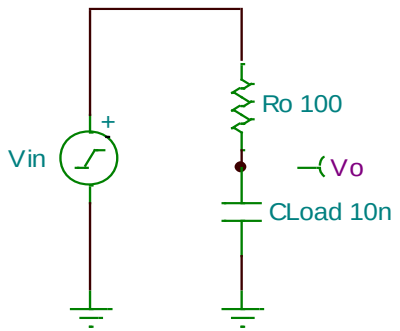


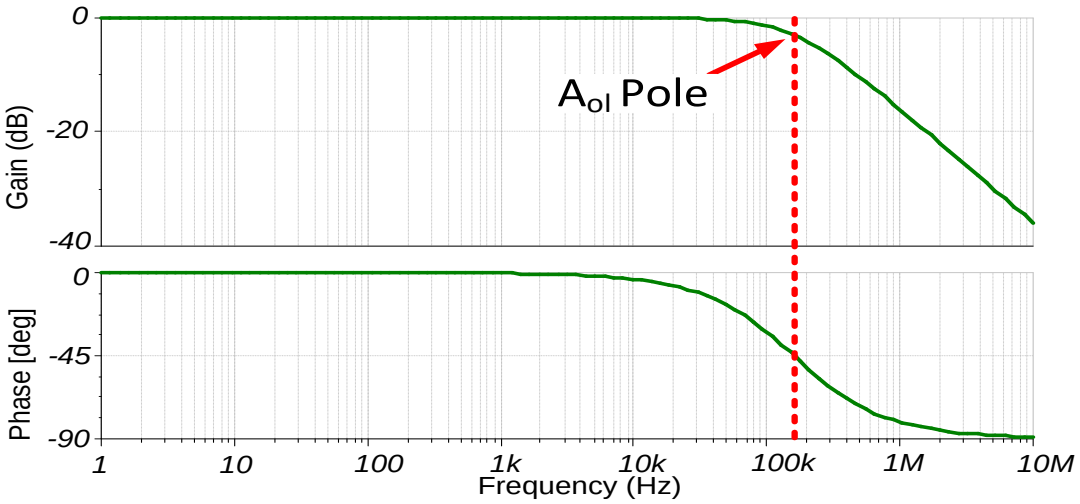


Capacitive loads: Stability theory



Capacitive loads: Pole in Aol





Transfer Function:

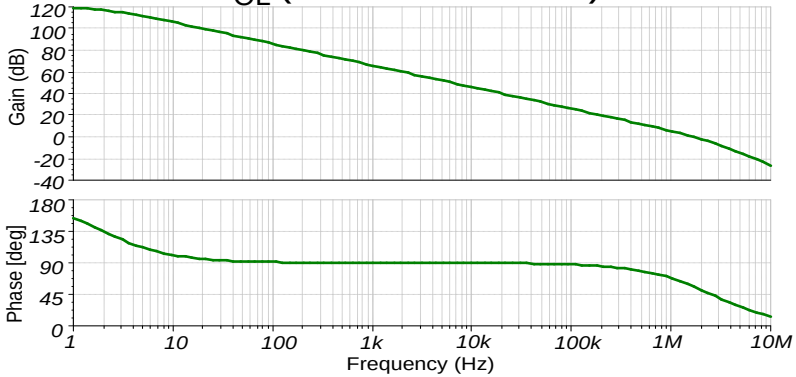
$$\frac{V_o}{V_{in}}(s) = \frac{1}{1 + s * Ro * C_{LOAD}}$$

Pole Equation:

$$f_{POLE} = \frac{1}{2 * \pi * Ro * C_{LOAD}}$$

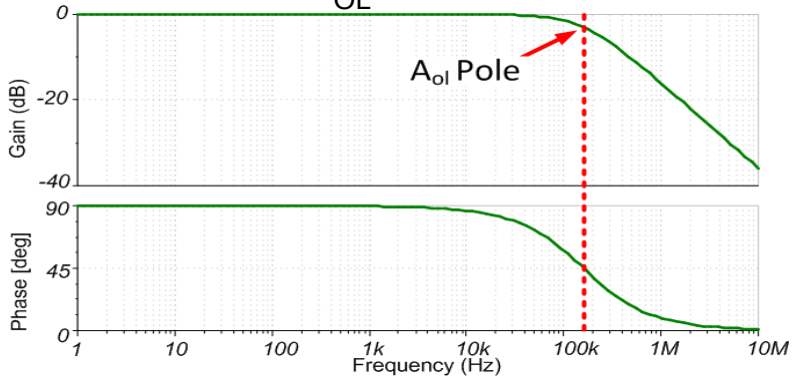
Capacitive loads: Loaded Aol

A_{OL} (from data sheet)

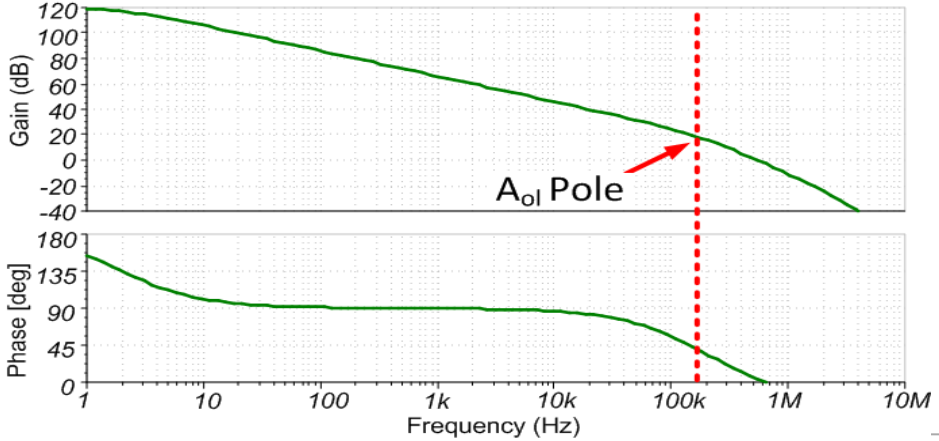


X

A_{OL} Load



Loaded A_{OL} =



There are only 2 things you need in an op amp macromodel to analyze stability problems:

Aol

(AC open loop gain)

Zo

(AC open loop output impedance)

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Op amp output impedance

Open loop (Z_O)
&
Closed loop (Z_{OUT})

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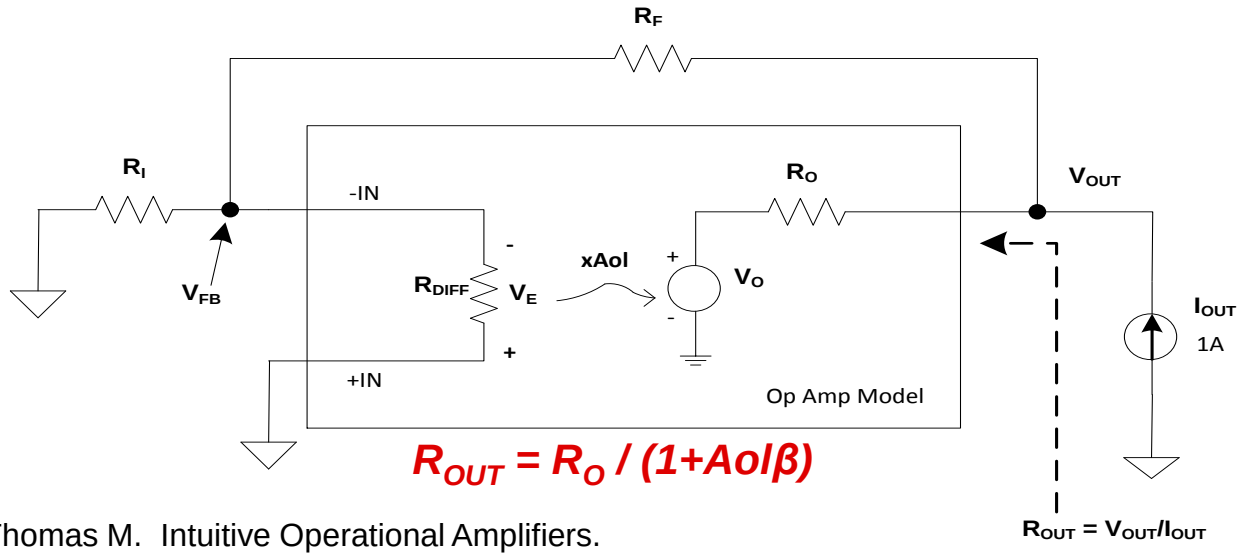
Op amp impedance: Output resistance

Definition of Terms:

R_O = Op Amp ***Open Loop*** Output Resistance

R_{OUT} = Op Amp ***Closed Loop*** Output Resistance



$$R_{OUT} = R_O / (1+Aol\beta)$$

From: Frederiksen, Thomas M. Intuitive Operational Amplifiers. McGraw-Hill Book Company. New York. Revised Edition. 1988.

Op amp Impedance: Derivation of R_{OUT}

1. $\beta = V_{FB} / V_{OUT} = [V_{OUT} (R_I / \{R_F + R_I\})]/V_{OUT} = R_I / (R_F + R_I)$
2. $R_{OUT} = V_{OUT} / I_{OUT}$
3. $V_O = -V_E \, Aol$
4. $V_E = V_{OUT} [R_I / (R_F + R_I)]$
5. $V_{OUT} = V_O + I_{OUT} R_O$
6. $V_{OUT} = -V_E Aol + I_{OUT} R_O$ *Substitute 3) into 5) for V_O*
7. $V_{OUT} = -V_{OUT} [R_I/(R_F + R_I)] \, Aol + I_{OUT} R_O$ *Substitute 4) into 6) for V_E*
8. $V_{OUT} + V_{OUT} [R_I/(R_F + R_I)] \, Aol = I_{OUT} R_O$ *Rearrange 7) to get V_{OUT} terms on left*
9. $V_{OUT} = I_{OUT} R_O / \{1+[R_I Aol/(R_F+R_I)]\}$ *Divide in 8) to get V_{OUT} on left*
10. $R_{OUT} = V_{OUT}/I_{OUT} =[I_{OUT} R_O / \{1+[R_I Aol / (R_F+R_I)]\}] / I_{OUT}$
    - *Divide both sides of 9) by I_{OUT} to get R_{OUT} [from 2)] on left*
11. $R_{OUT} = R_O / (1+Aol\beta)$ *Substitute 1) into 10)*

$$R_{OUT} = R_O / (1+Aol\beta)$$

Texas Instruments

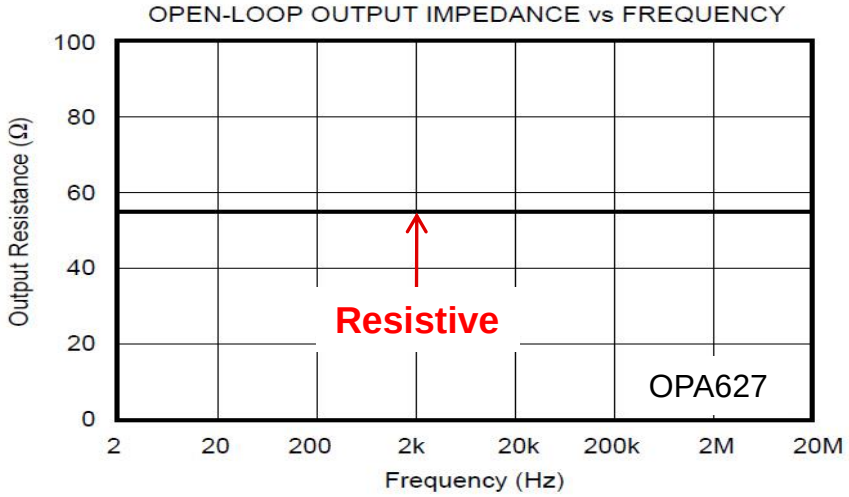
Op amp impedance: R_{OUT} vs R_O

- **R_O does *NOT* change when closed loop feedback is used**
  - It does change with output current

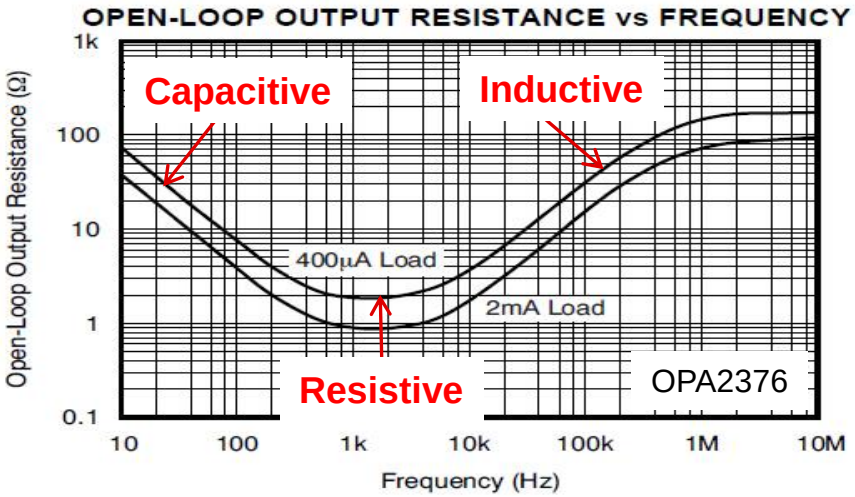
- **R_{OUT} is the effect of R_O, Aol, and β controlling V_O**
  - Closed Loop feedback (β) forces V_O to increase or decrease as needed to accommodate V_O loading
  - Closed Loop (β) increase or decrease in V_O appears at V_{OUT} as a reduction in R_O
  - R_{OUT} increases as Loop Gain (Aolβ) decreases

Op amp impedance: When R_O is really Z_O!

OPA627 has R_O



OPA2376 has Z_O



Note: **Some op amps have Z_O characteristics other than pure resistance – consult data sheet / manufacturer**

Texas Instruments

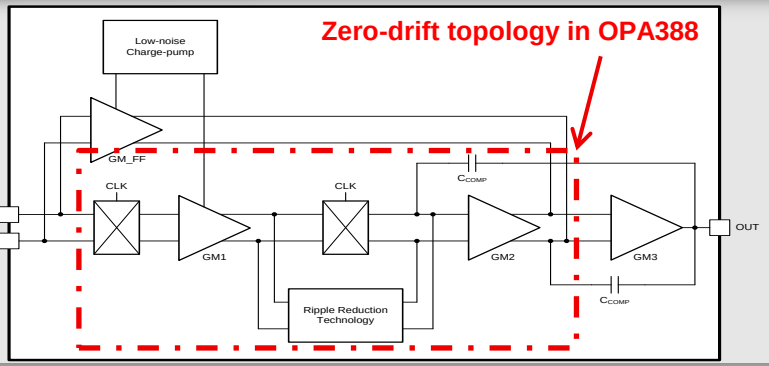
Amplifiers with reactive Zo: Zero drift

OPA388 | OPA333/0 | OPA188/0/9 | OPA334/5 | OPA2187 | OPA378 | LMP2021 | LMP2011

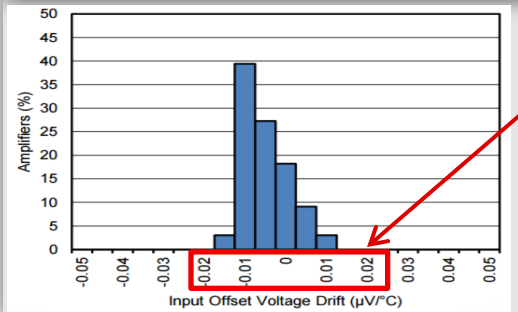
Overview

- Zero-drift (chopper stabilized or auto-zero) operational amplifiers continuously correct for error to achieve the lowest possible input offset voltage and drift, as well as minimized low-frequency noise.
- This circuitry also ensures excellent DC specifications (AOL, CMRR, and PSRR), allowing better performance in harsh environments.

Implementation

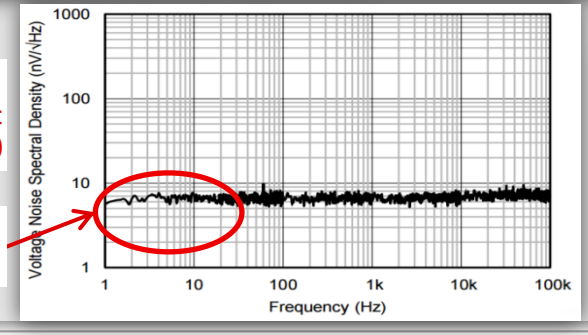


Problems solved



Ultra-low temperature drift (-40°C to +125°C)

Minimized low-frequency noise



Device Example:

Specifications	Zero-Drift OPA388	Non-Zero-Drift Amp
V_{os} (µV) (Typ, Max)	0.25, 5	200, 1000
V_{os} drift (µV/°C) (Typ, Max)	0.005, 0.05	0.3, 1.5
0.1Hz - 10Hz voltage noise ($µV_{pp}$)	0.14	2.5

Amplifiers with reactive Zo: Multi-stage feedback

OPA376 | OPA209 | OPA211 | OPA140 | TLV07 | OPA277 | LPV811

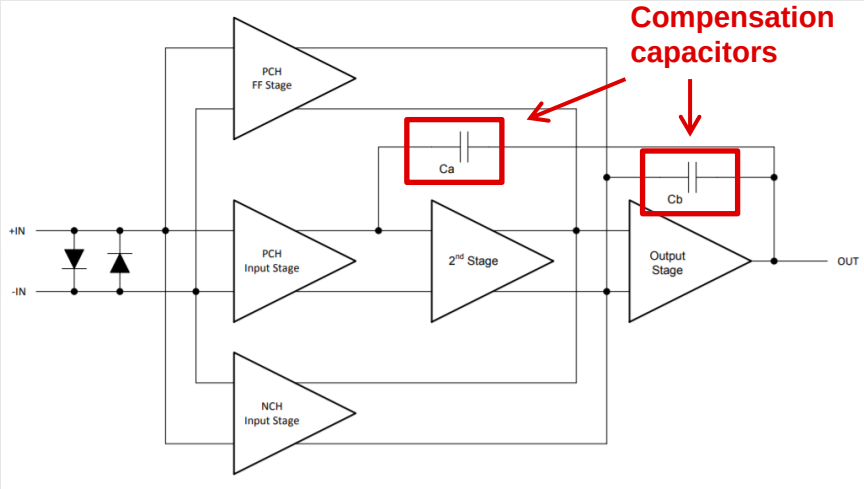
Overview

- Some Op amps use multiple gain stages to achieve the desired open loop gain.
- This is especially useful in low voltage rail-to-rail applications that want to avoid cascoded input stages.
- This requires compensation between stages for overall loop stability.

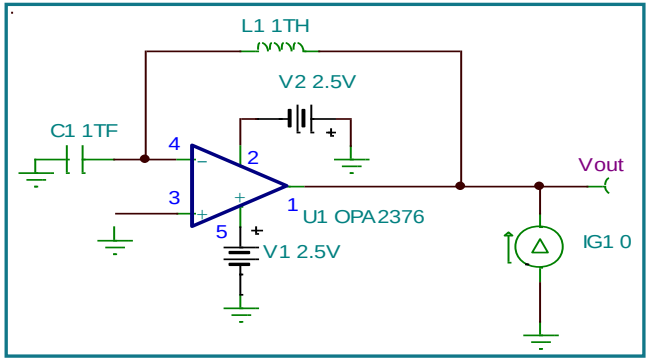
Advantages

- Many bipolar devices use this architecture to improve the output swing to the rail, because wider swing requires additional base current.
- Using a three-stage architecture allows for optimized distortion performance.

Implementation



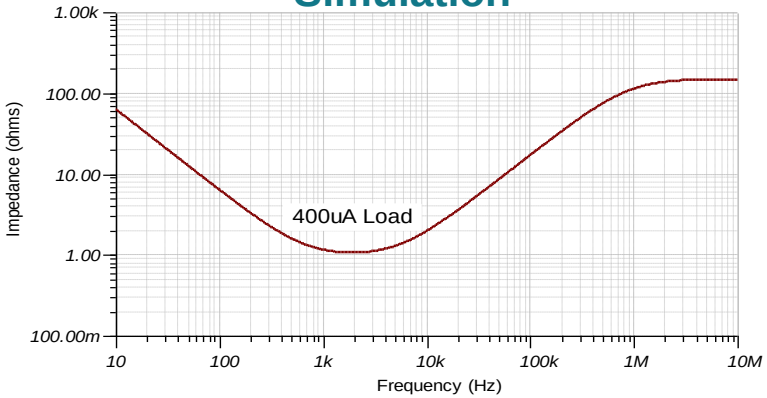
Complex Zo: Accurate models are key!



Z_O SPICE Test of Op Amp Macromodel:

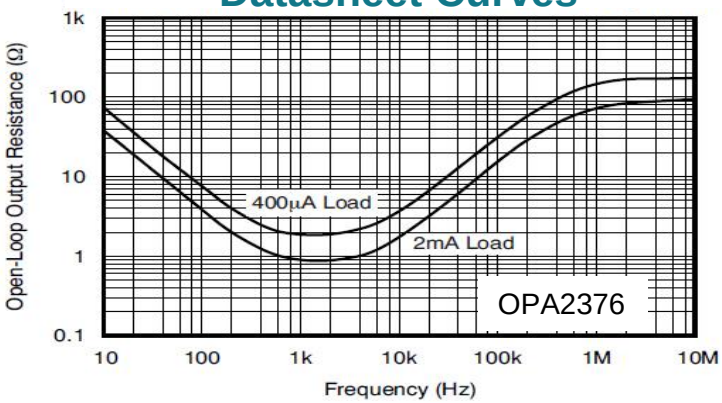
1. Run SPICE AC Analysis
   1. IG1 is an AC Current Generator
   2. IG1 DC Value=0A for unloaded Z_O
2. Z_O=V_{OUT}
3. Convert V_{OUT} (dB) to V_{OUT} (Logarithmic)
4. Z_{OUT} (ohms)=V_{OUT} (Logarithmic)

Simulation



VS

Datasheet Curves

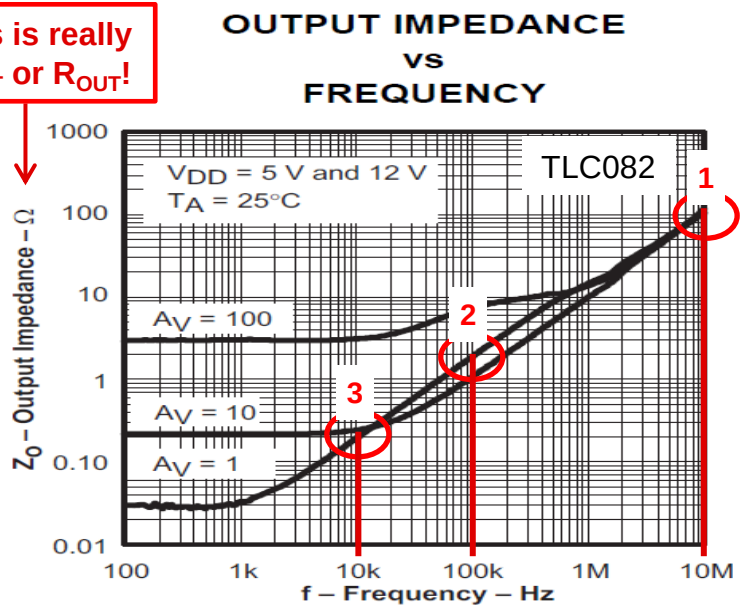


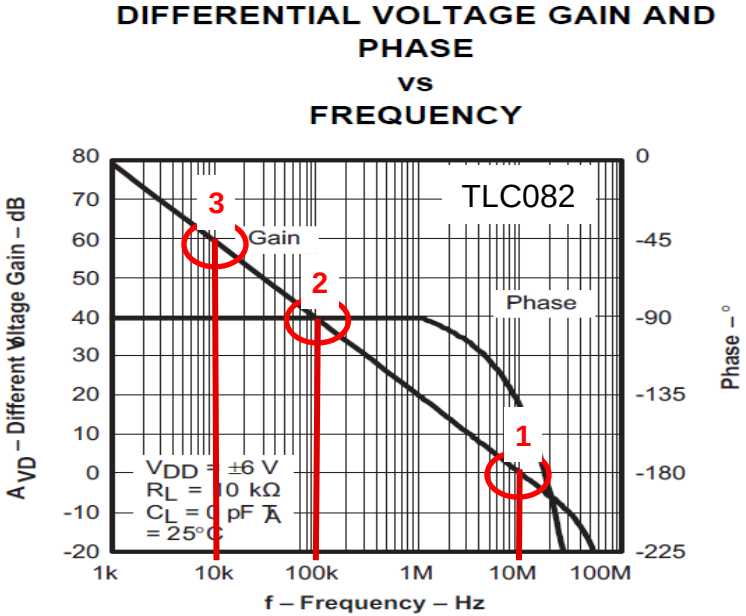
Some data sheets specify Z_{OUT} *NOT* Z_O

Recognize R_{OUT} instead of R_O:

- R_{OUT} inversely proportional to Aol
  - $R_{OUT} = \frac{R_O}{1+Aol\beta}$, where $R_{OUT} \propto \frac{1}{Aol}$
- R_{OUT} typically <100Ω at high frequency

This is really Z_{OUT} or R_{OUT}!





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Some data sheets specify Z_{OUT} *NOT* Z_O

Calculating R_O From R_{OUT}

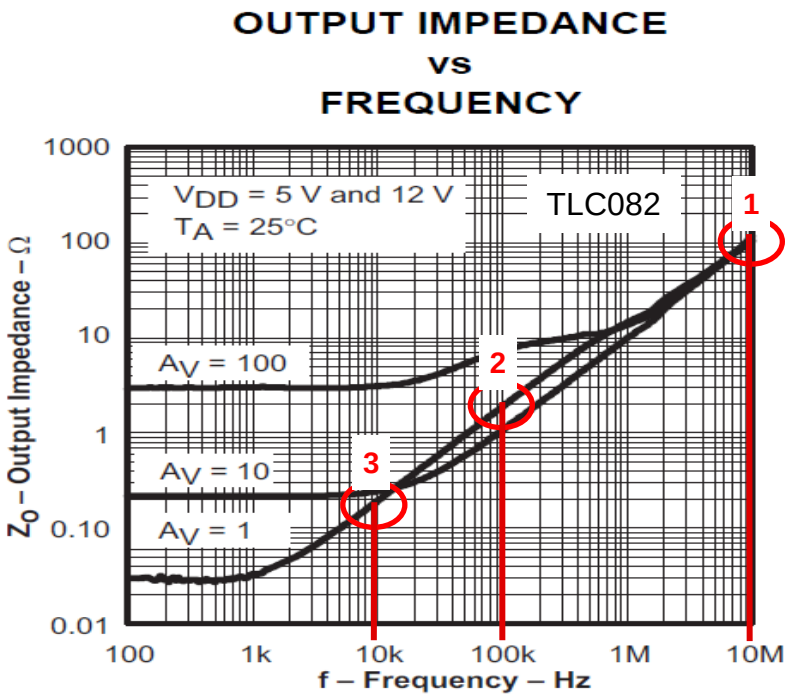
Computing R_O from R_{OUT} where $\boldsymbol{\beta = 1(0dB)}$:

R_{OUT}=100Ω for A_V=1, f=10MHz, Aolβ=1(0dB)

$$R_{OUT} = \frac{R_O}{1 + Aol\beta}$$

$$100\Omega = \frac{R_O}{1+1} \rightarrow R_O = 200\Omega$$

Point	frequency	Aol	R_{OUT} (A_V=1) Datasheet	R_{OUT} (A_V=1) Computed
----------	(Hz)	(dB)	(ohms)	(ohms)
1	10M	0	100	100
2	100k	40	2	2
3	10k	60	0.2	0.2



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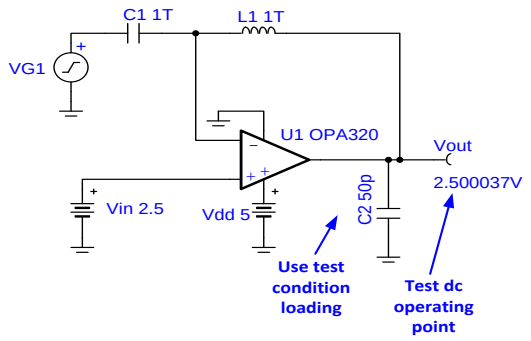
Op amp model: Open loop gain

STEP 1

Test Circuit for Aol

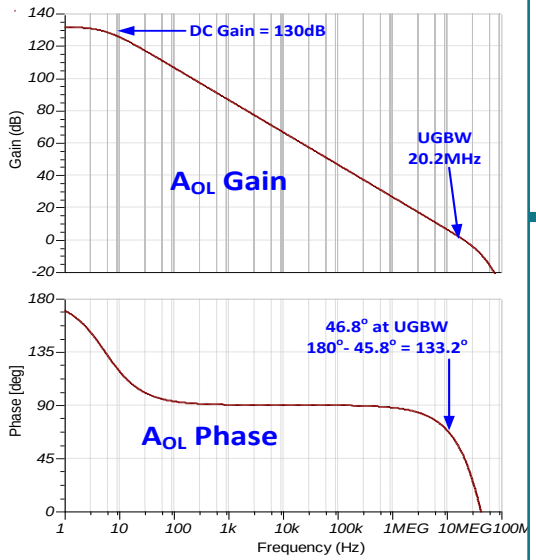


1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for A_{OL} curve

A_{OL} = Vout

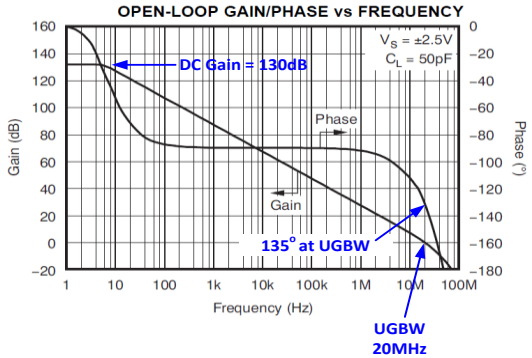
STEP 2

Simulated results



STEP 3

Data Sheet Specification



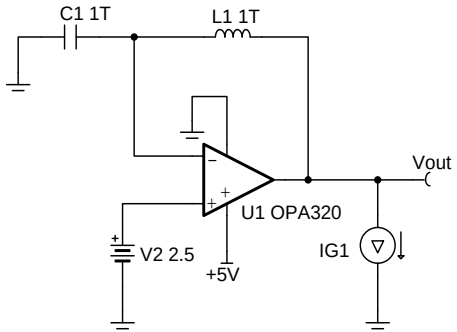
Compare key points on simulation results to data sheet curve.

Aol = -1*V_{OUT} for same phase in datasheet

Op amp model: Open loop output impedance

STEP 1

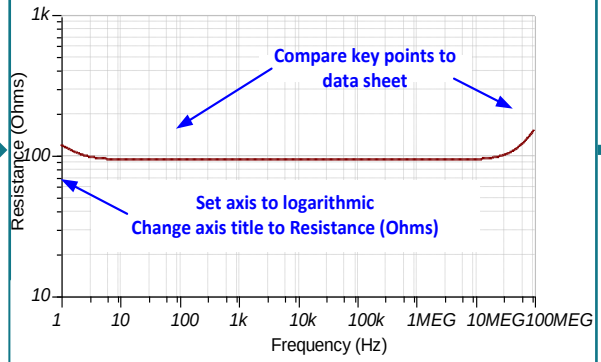
Test Circuit for Aol



1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for Z_o curve. Z_o = Vout.

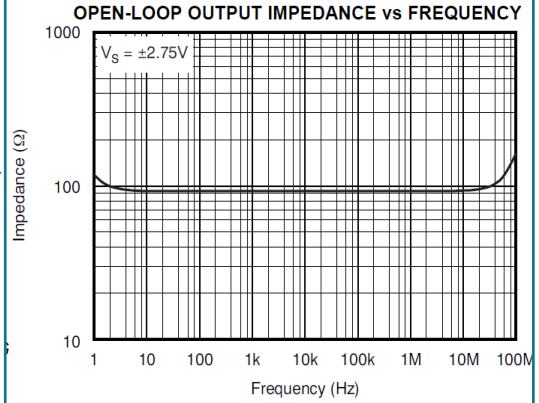
STEP 2

Simulated results



STEP 3

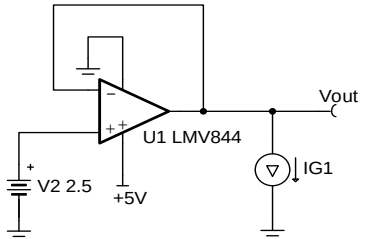
Data Sheet Specification



Op amp model: Closed loop output impedance

STEP 1

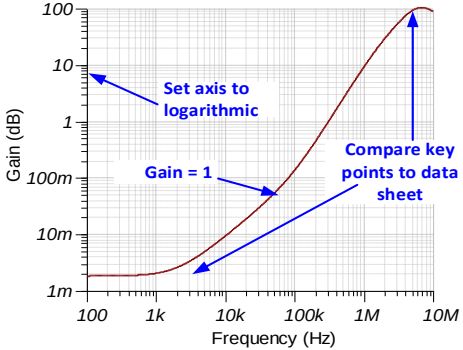
Test Circuit for Zout



1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for Z_{out} curve. Z_{out}= Vout.
3. Change the vertical axis to logarithmic scale

STEP 2

Simulated results



STEP 3

Data Sheet Specification

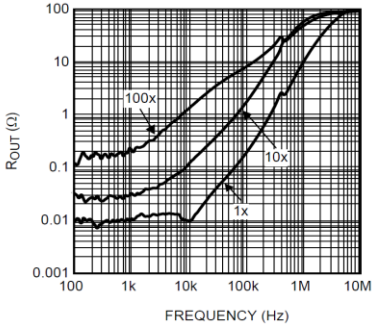


Figure 33. Closed-Loop Output Impedance vs Frequency

Summary: Overview

Op Amp Output Impedance

1) Before any stability analysis is done check the SPICE op amp macromodel for proper Aol.

2) Before any stability analysis is done check the SPICE op amp macromodel for proper Z_O (open loop output impedance).

2) Newer TI op amp datasheets give a Z_O curve. Test in SPICE for Z_O and compare.

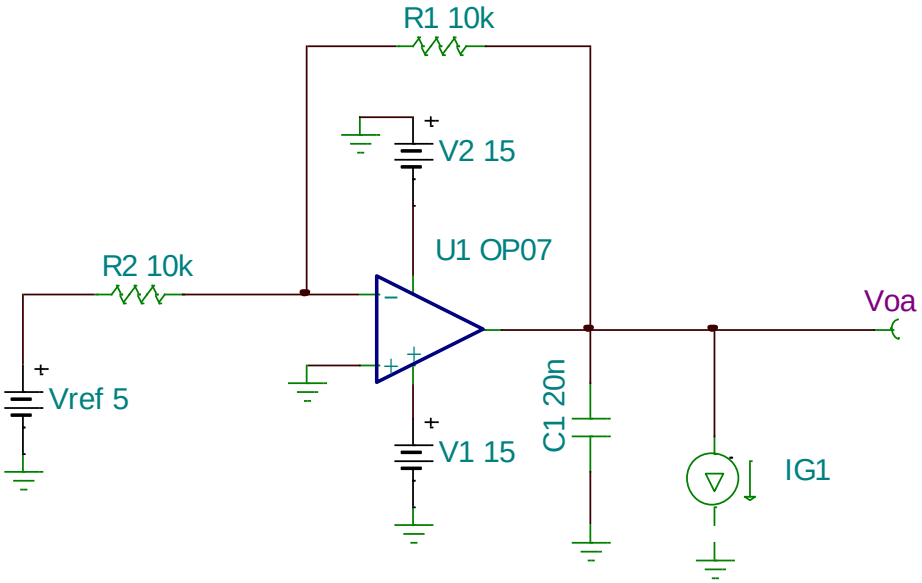
3) Older TI and competitor op amps usually have a Z_{OUT} (closed loop impedance) curve. Test for Z_{OUT}. If Z_{OUT} and Aol are correct then so is Z_O.

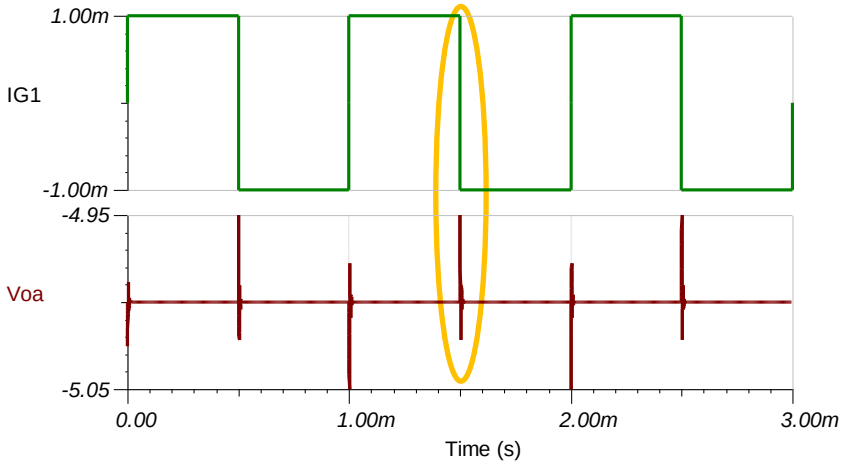
TLV07 versus OP07C

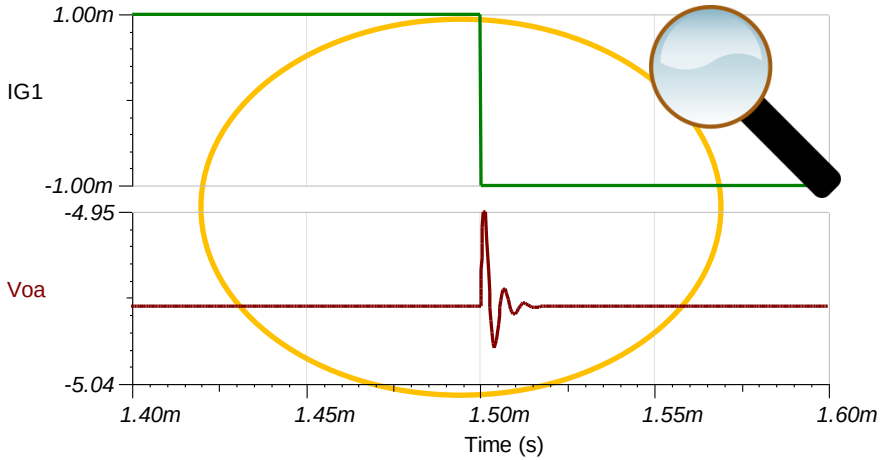
Specification Comparison

Parameter	Unit	OP07C	TLV07
Supply Voltage Range	V	6 to 36	2.7 to 36
GBW MHz	MHz (Typ)	0.6	1
Slew Rate	V/µs (typ)	0.3	0.4
Rail-to-Rail		-	Out
Vos	µV (Max)	-	100
Vos	µV (Typ)	60	50
Offset Drift	µV/°C (Typ)	0.5	0.9
Input Bias Current	nA (Typ)	1.8	0.04
Vn @ 1kHz	nV/√Hz (Typ)	9.8	19
Quiescent Current	mA (Typ, Max)	2.4, 5	0.95, 1.8
CMRR dB (typ)	dB (Typ)	120	120
Architecture		Bipolar	CMOS
Operating Temperature Range	°C	0 to 70	-40 to 125
Package Group		SOIC, PDIP, SO-8	SOIC
Price (1ku)	USD ($)	0.23	0.35

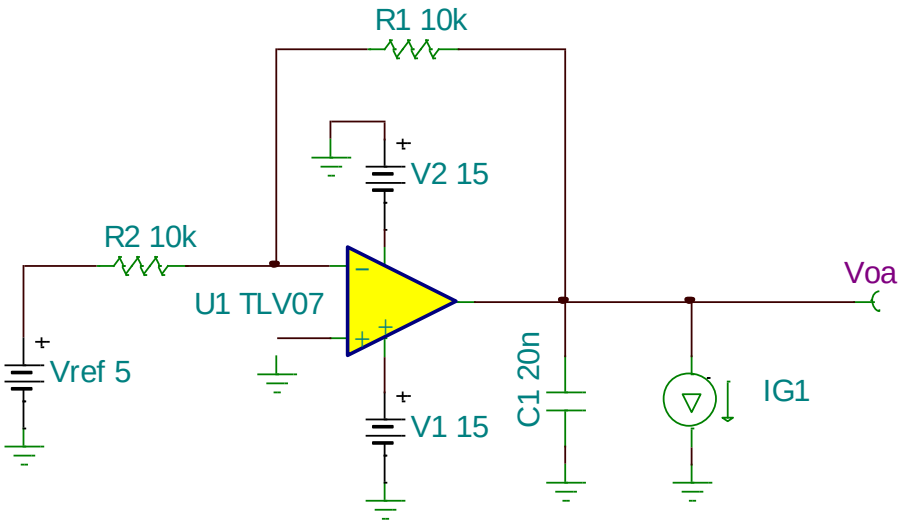
OP07: 20nF cap load

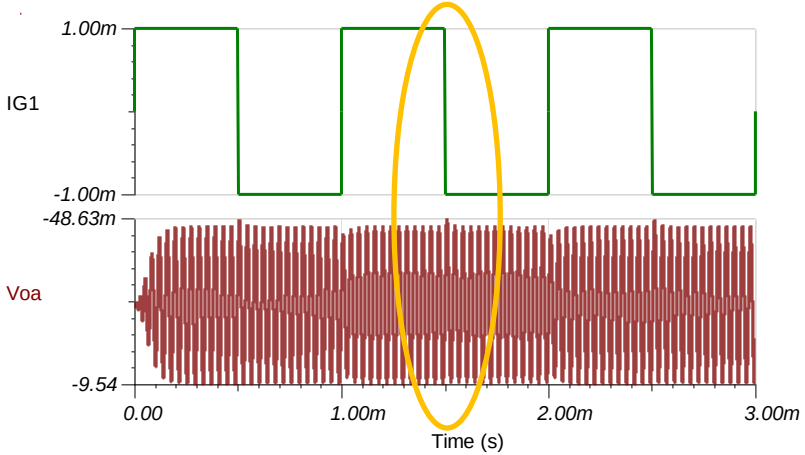


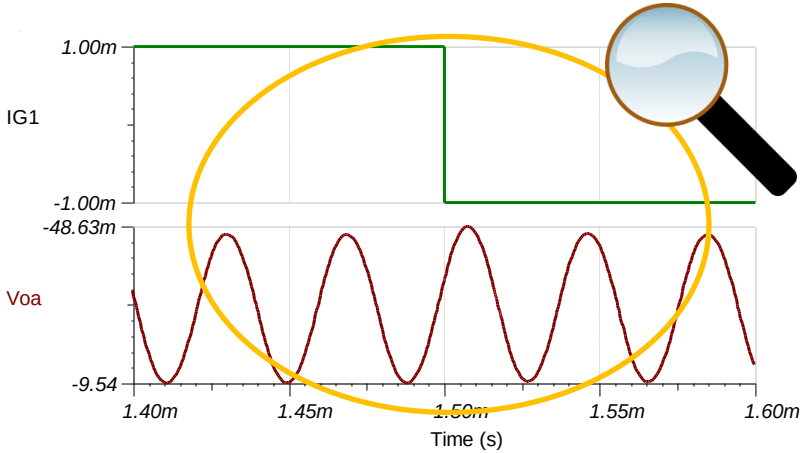




TLV07: 20nF cap load

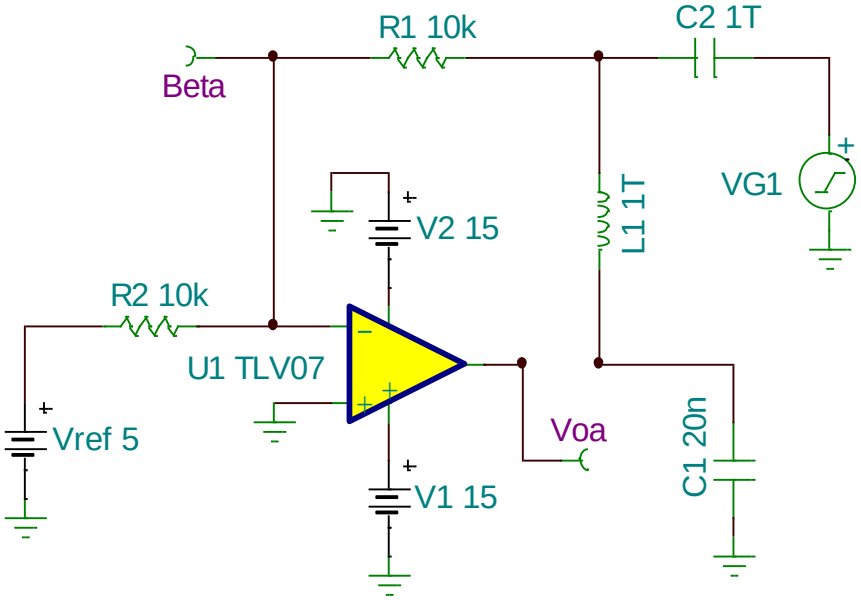




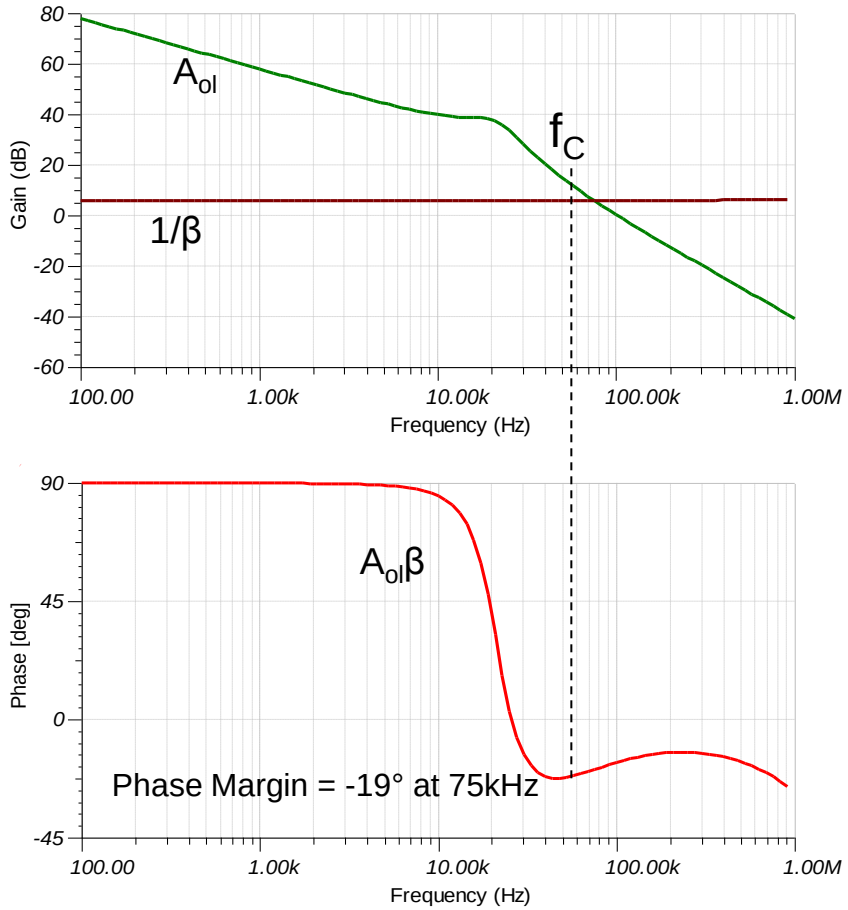


Oscillation at 25.97kHz!

TLV07: Loop stability

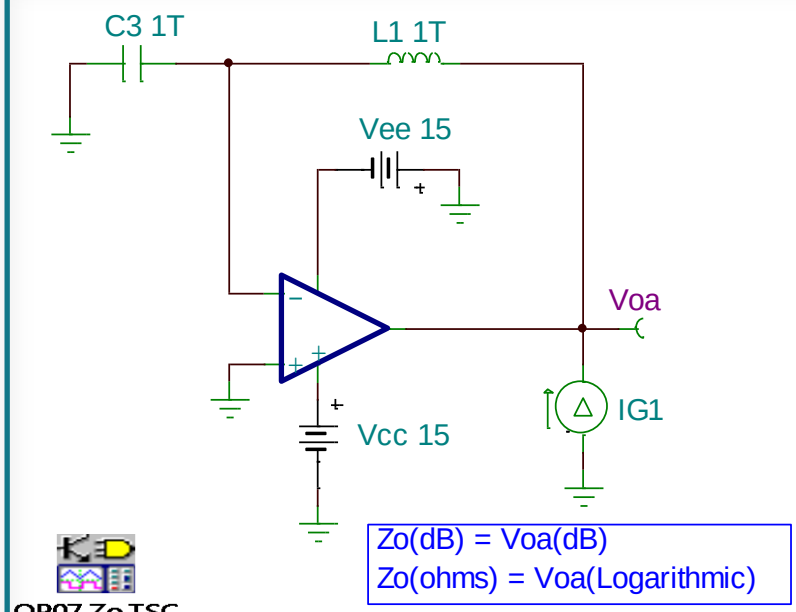


Voa = Aolβ
Voa/β = Aol



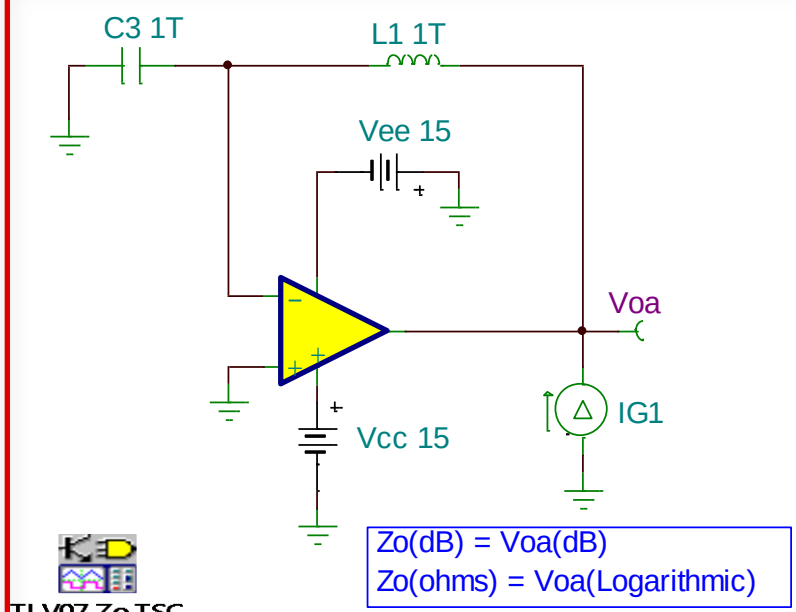
TLV07 vs OP07: Output impedance (Zo)

OP07



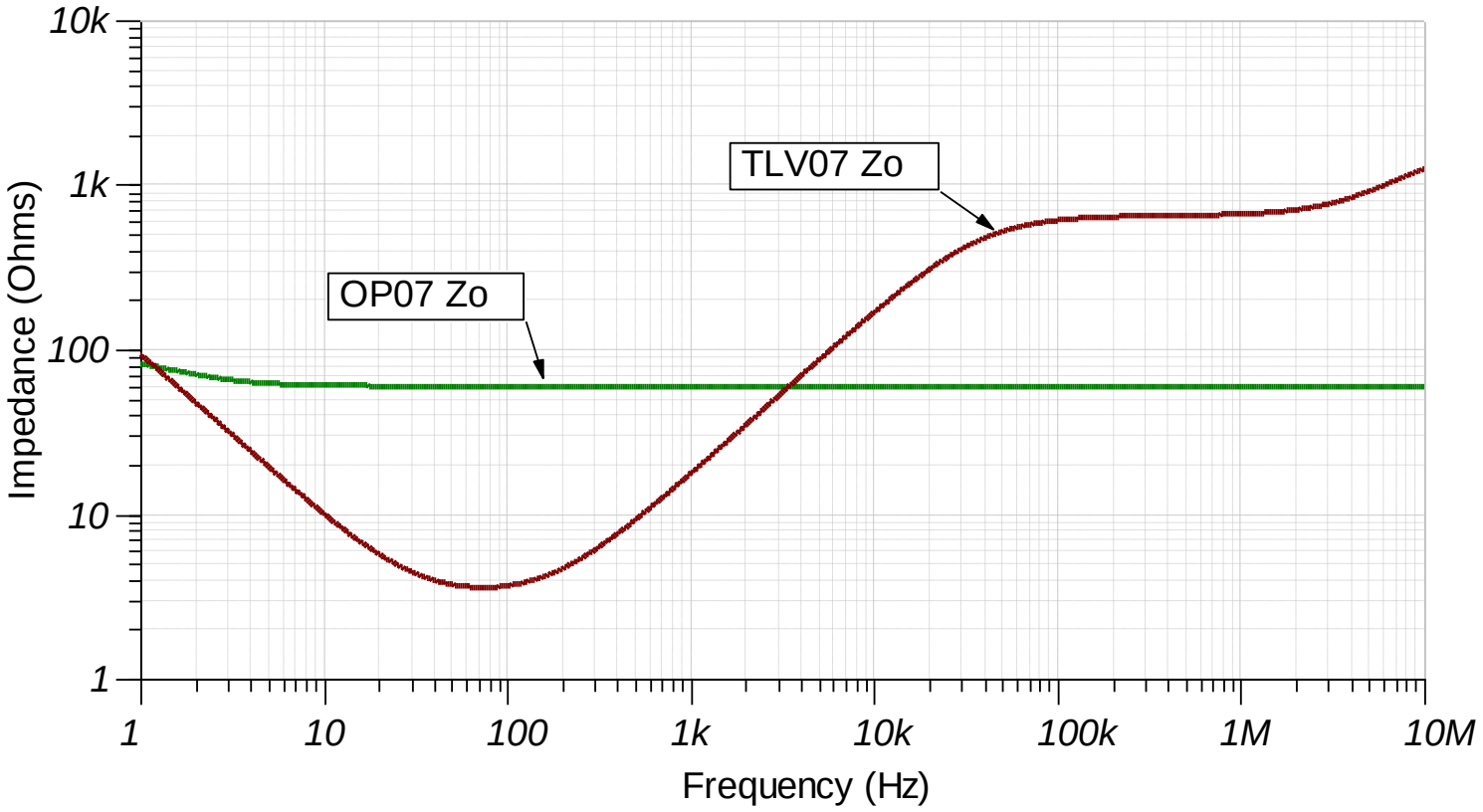
Zo(dB) = Voa(dB)
Zo(ohms) = Voa(Logarithmic)

TLV07

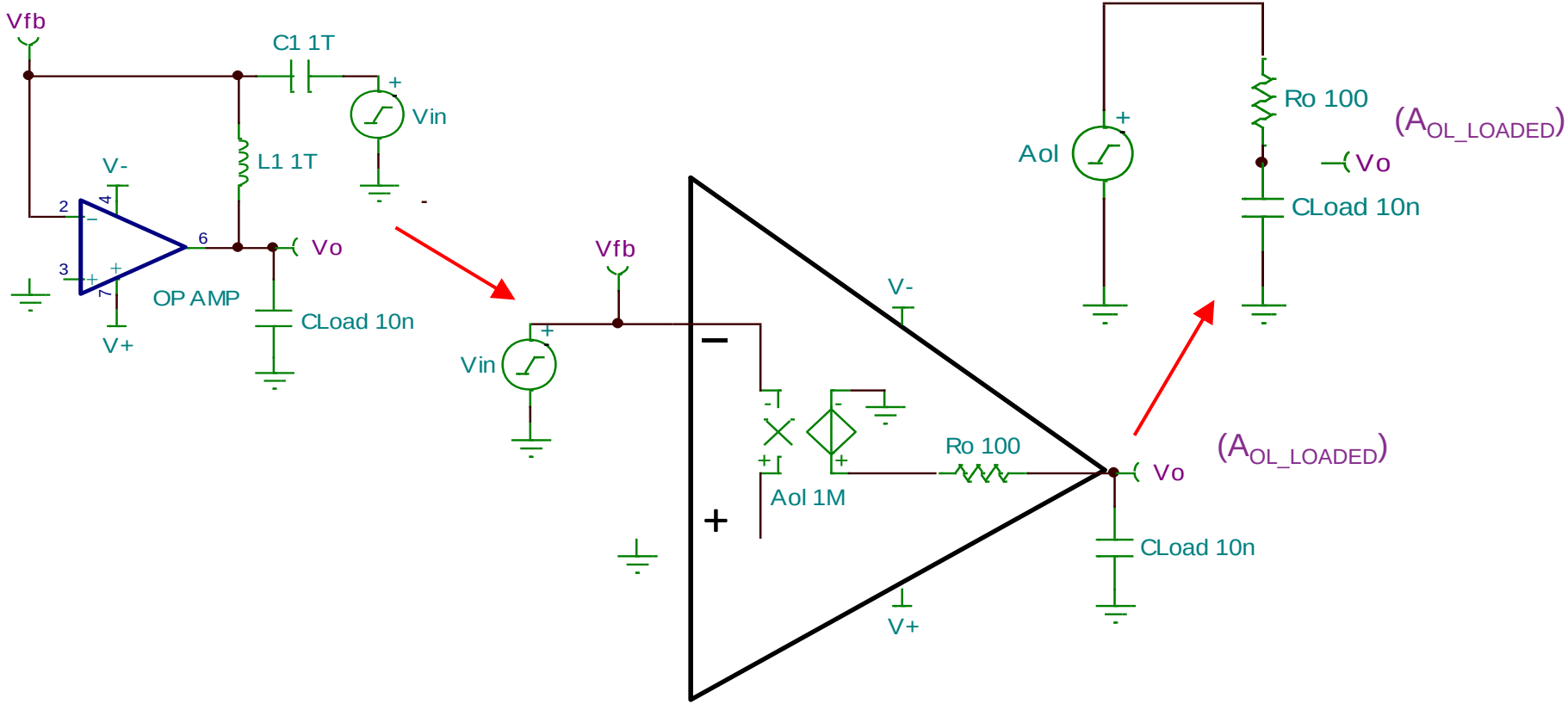


Zo(dB) = Voa(dB)
Zo(ohms) = Voa(Logarithmic)

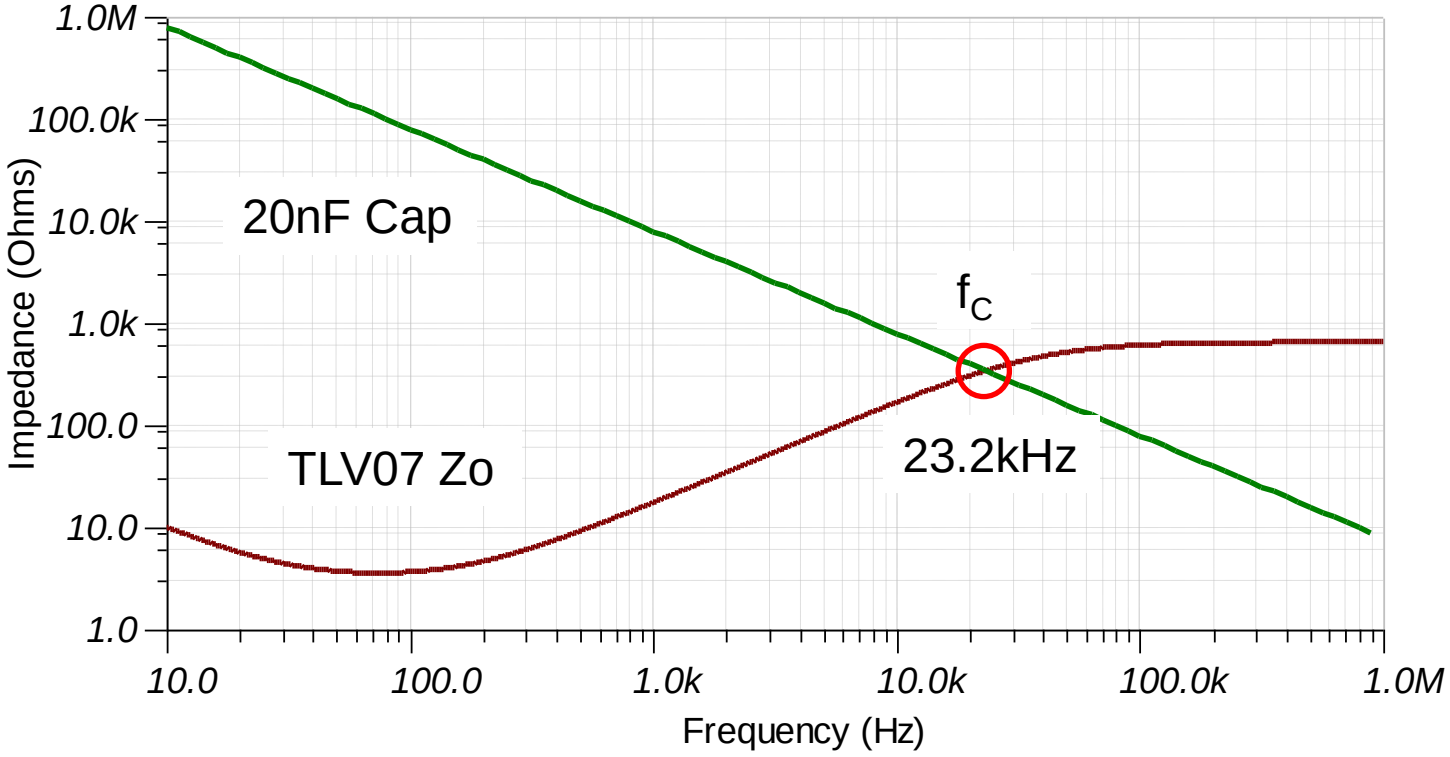
TLV07 vs OP07 Zo



Capacitive loads – Stability theory



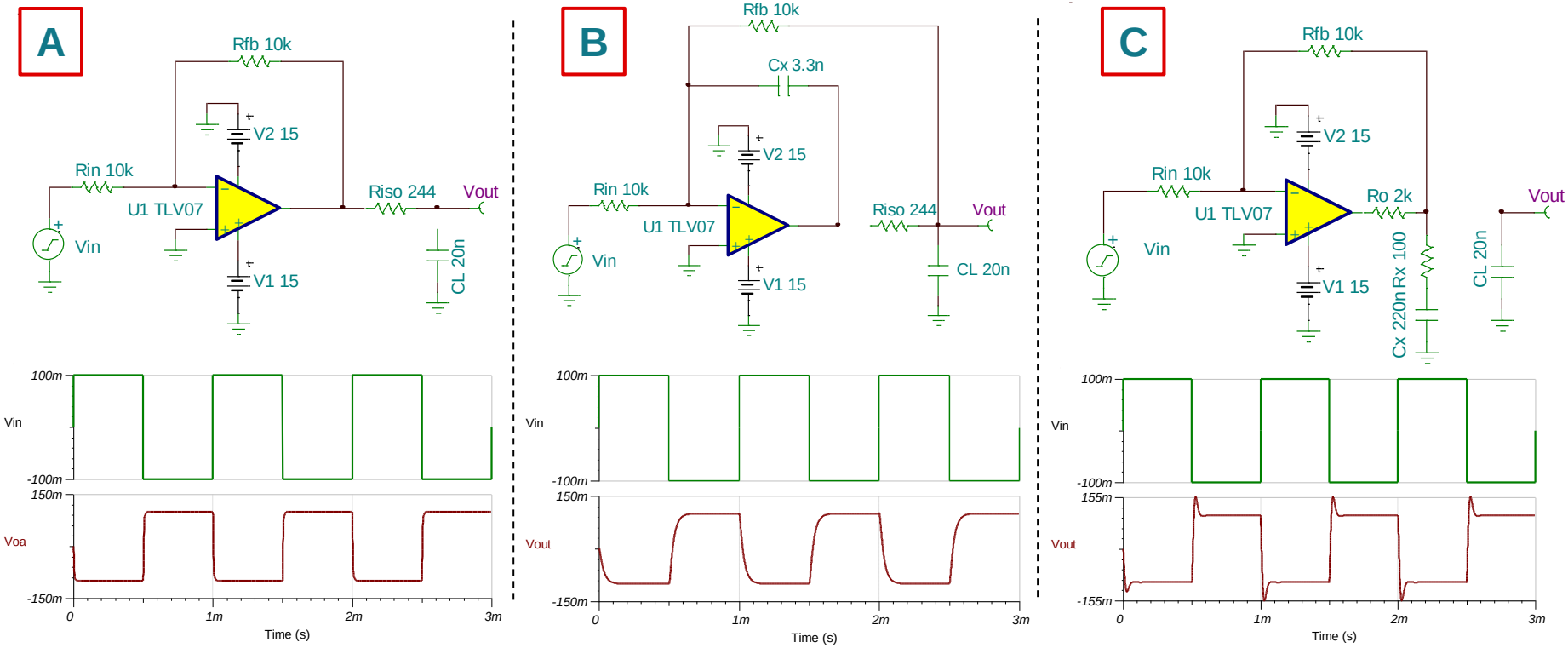
Is it really output impedance?



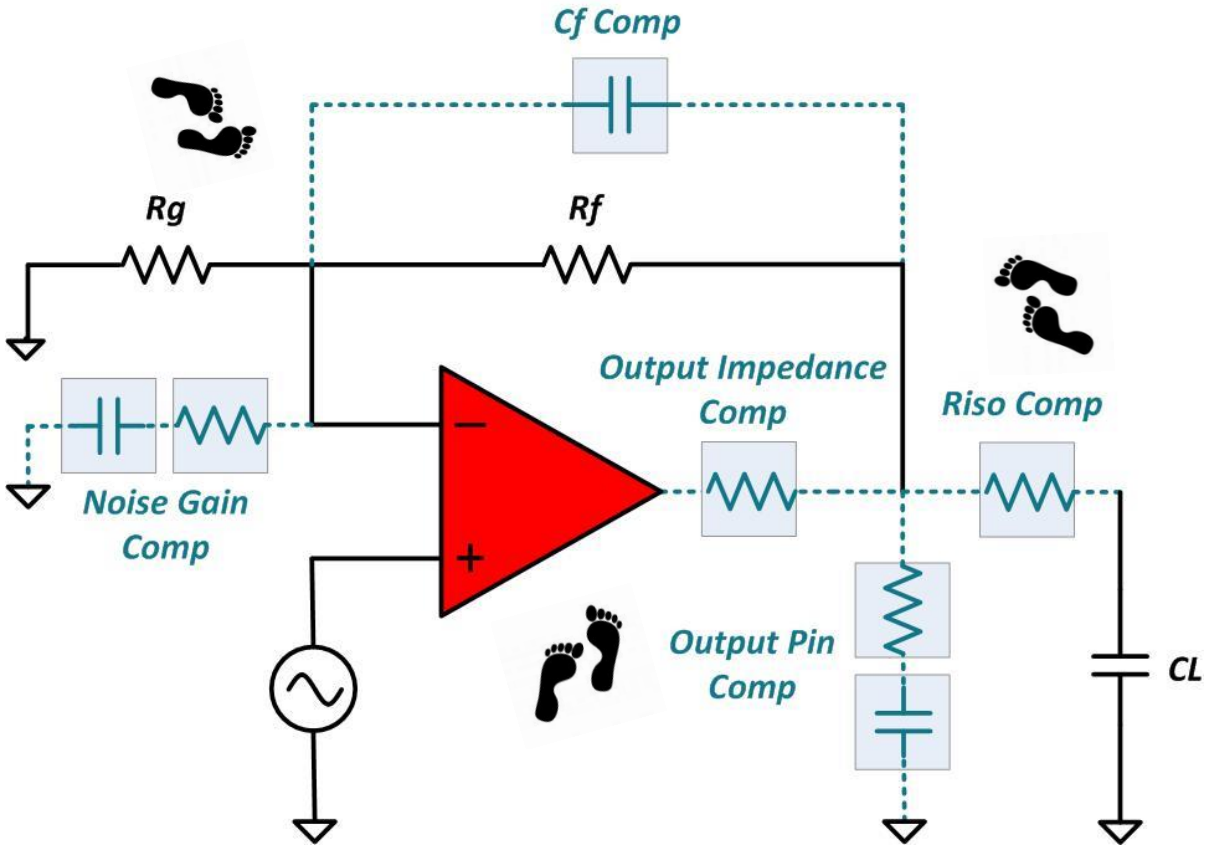
Looking at Aol vs. looking at output impedance

- Output impedance isn't resistive so it's not straightforward to understand how to comp the op amp!
- Most stability problems can be solved by manipulating the feedback **IF** the output impedance is resistive.
- With a complex output impedance there is potential for complex conjugate poles in Aol, and manipulating the feedback will never fix this resonance!

How do we fix it?



Compensation schemes: check for footprints



- An op-amp driving a cap load almost always requires compensation!
- Good design practice will leave space for these components!

Summary

1) OP07 Zo (open loop output impedance) is predominantly resistive within the unity gain bandwidth of the op amp.

2) TLV07 Zo (open loop output impedance) is predominantly inductive over four decades of its the unity gain bandwidth.

3) Any design replacing OP07 with TLV07 should be verified for stability!

4) ***Problem:*** Most designers with DC voltage circuits don't think to test for stability, but a disturbance on any pin could potentially cause erratic behavior and lead to invalid readings or system shutdown.

Output impedance and driving converters

ADS8363

1 MSPS | 16-bit | 4x2/2x2 Simultaneous Sampling ADC

Features

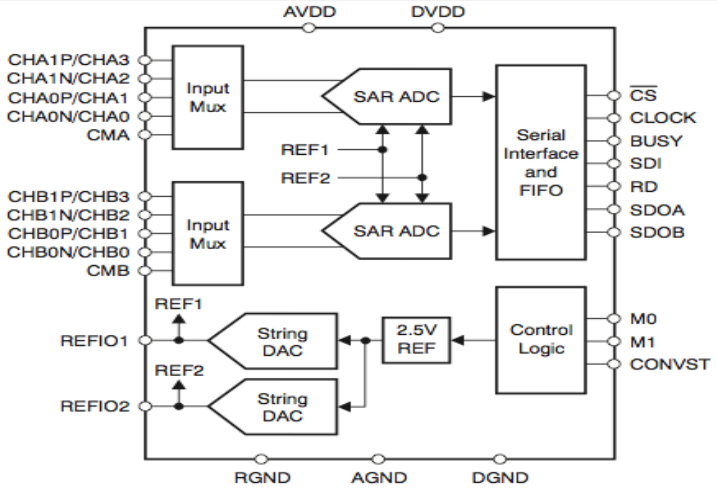
- Dual, 4-Ch pseudo-differential or 2-Ch differential configurable inputs coupled with a dual 2.5V programmable reference
- Dual ADCs with true 16-bit Performance
  - NMC @ 93dB SNR (typ)
- Integrated Industrial Solution
  - 4 deep per-channel FIFO
  - Auto-scan Mode

Applications

- Motor control
- Power quality measurement
- Protection relays
- Industrial automation

Benefits

- Input muxes and **dual programmable internal reference** enable input range scaling and monitoring up to 8 different signals
- Allows **resolution flexibility** without board or control software redesign



ADC input drive design

			MIN	MAX	UNIT
t_{DATA}	Data throughput, f_{CLK} = max		1		µs
t_{CONV}	Conversion time	Half-clock mode	17.5		t_{CLK}
		Full-clock mode	35		
t_{ACQ}	Acquisition time		100		ns
f_{CLK}	CLOCK frequency	Half-clock mode	0.5	20	MHz
		Full-clock mode	1	40	

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale input range	(CHxxP – CHxxN) or CHxx to CMx	$-V_{REF}$		$+V_{REF}$	V
V_{IN}	Absolute input voltage	CHxxx to AGND	–0.1		AVDD + 0.1	V
C_{IN}	Input capacitance	CHxxx to AGND		45		pF

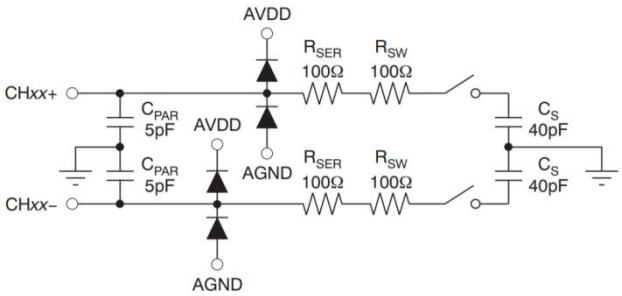
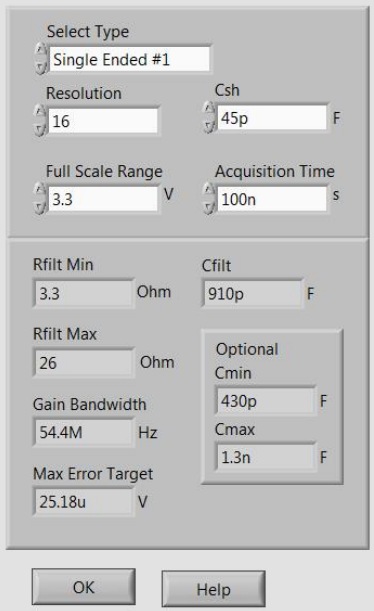
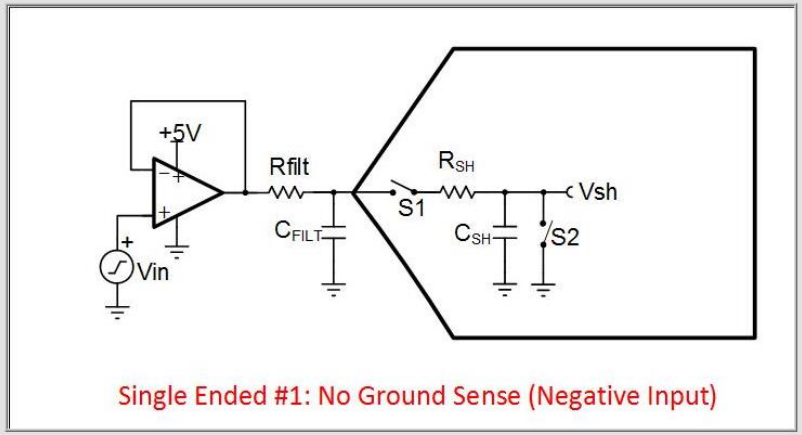


Figure 28. Equivalent Analog Input Circuit





http://www.ti.com/tool/ANALOG-ENGINEER-CALC

OPA835 Ultra-Low Power, 56MHz, RRO, Negative Rail In, VFB

Features

- Single/Dual Channel Options
- **Ultra-Low Power:**
  - 250µA/ch, Power-Down: <1µA
- **Ultra Low Distortion:** 0.00003%
- **Bandwidth:** = 56MHz G = 1V/V
- Input Voltage Noise: 9.3nV/√Hz
- RRO – Rail-to-Rail Output
- +2.5 to +5V Single Supply
- -40°C to 125°C Operating Temp

Channels	Packages	Body Size
1-Ch	6-pin SOT-23	2.9 mm x 1.6 mm
	10-pin QFN	2.0 mm x 2.0 mm

Benefits

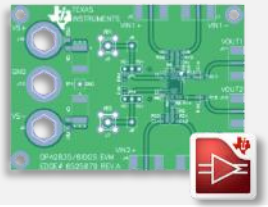
- Flexible supply for power sensitive applications
- Exceptional performance at very low power
- Increased dynamic range / sensitivity
- Low signal distortion
- Larger outputs in low voltage applications
- Integrated gain setting resistors enables smallest PCB footprint

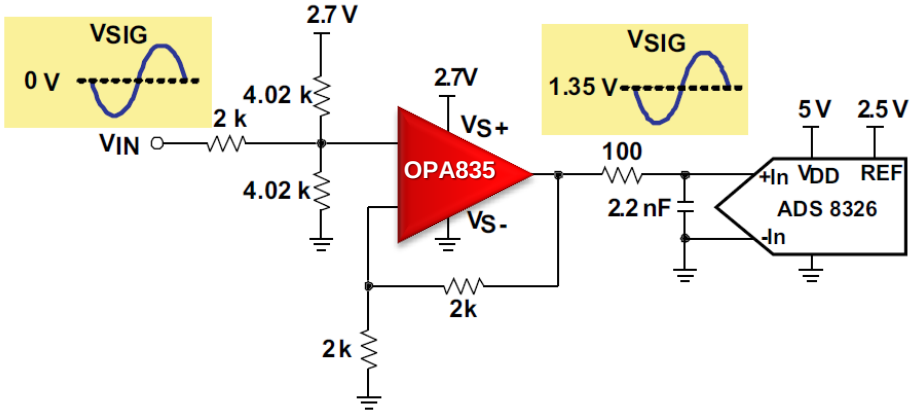
Applications

- Low Power Signal Conditioning
- Low Power SAR and ΔΣ ADC Driver
- Portable Audio Systems
- Ultrasonic Flow Meter

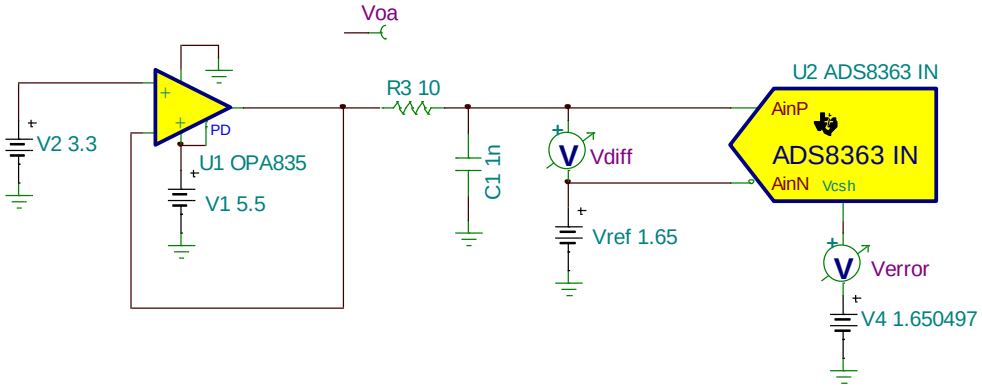
Tools & Resources

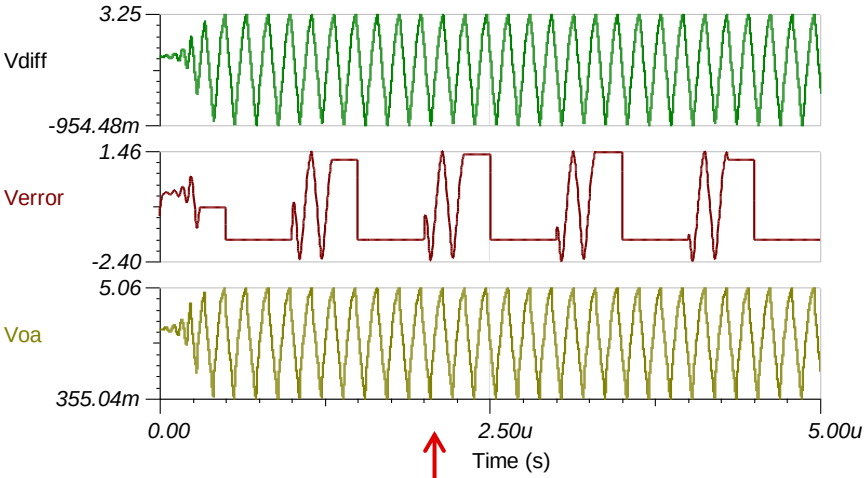
- Device Product Overview: LINK
- Device Evaluation Board (EVM): LINK
- Support: LINK
- Reference Design: LINK





OPA835: ADC drive





"TI Op-amp is too noisy!"

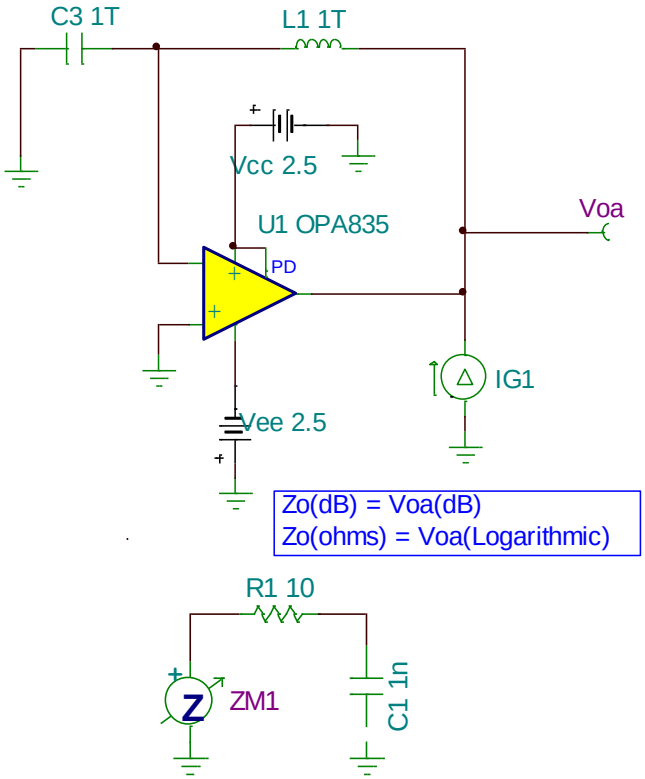
"Offset is out of spec!"

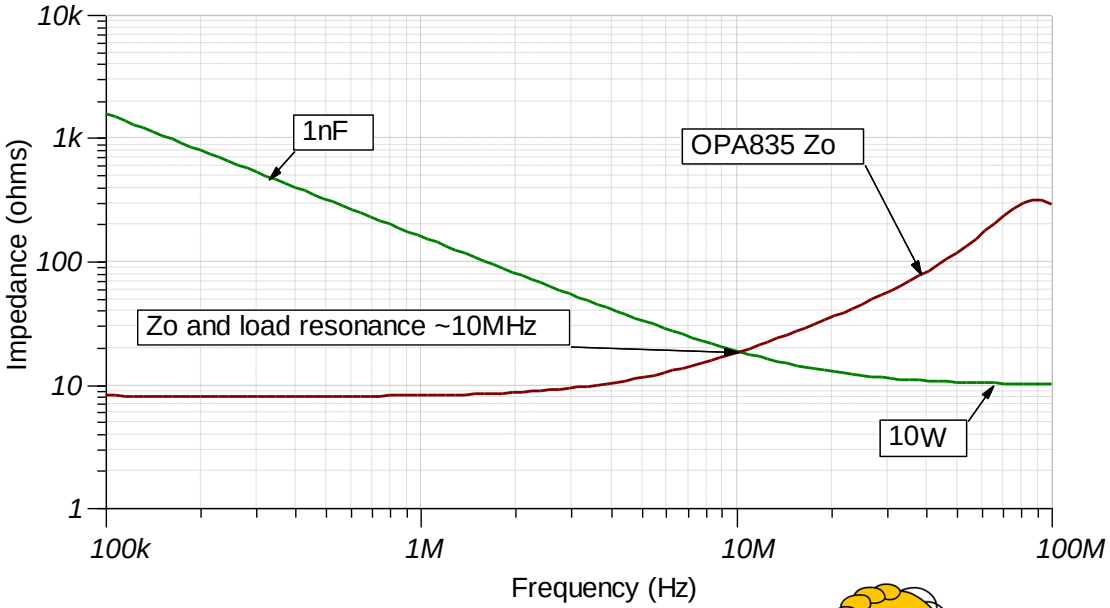
User

Me

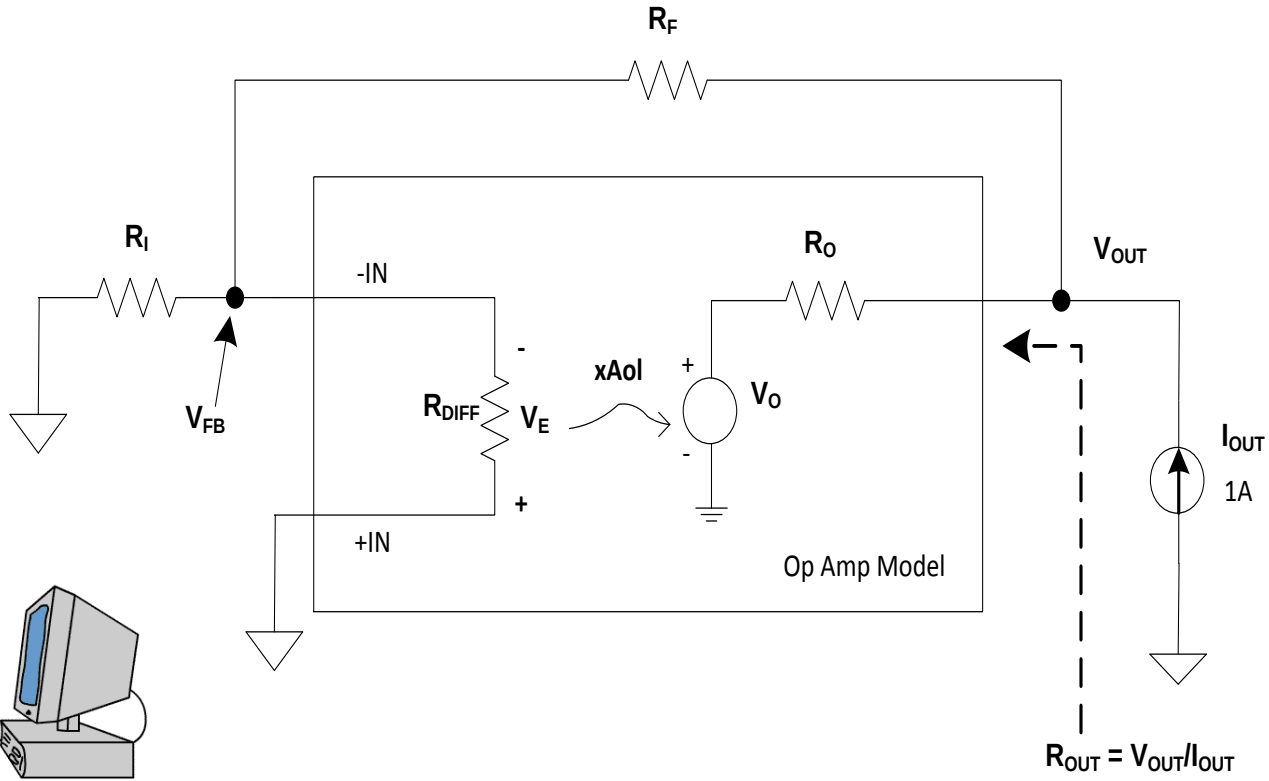
User usually read ADC codes and don't observe this directly!

OPA835: Zo and load impedance

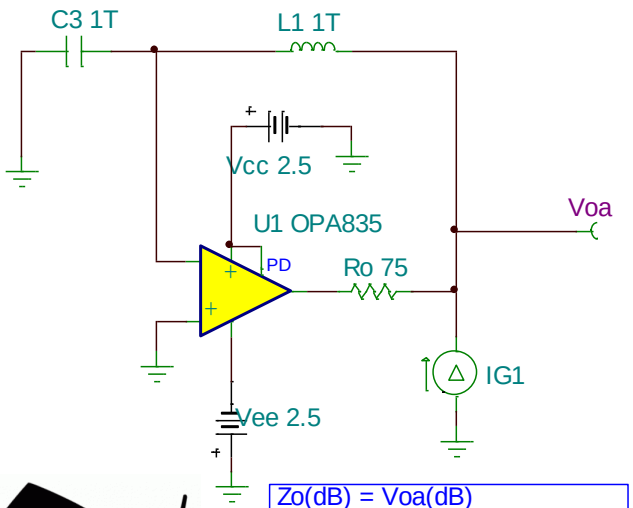




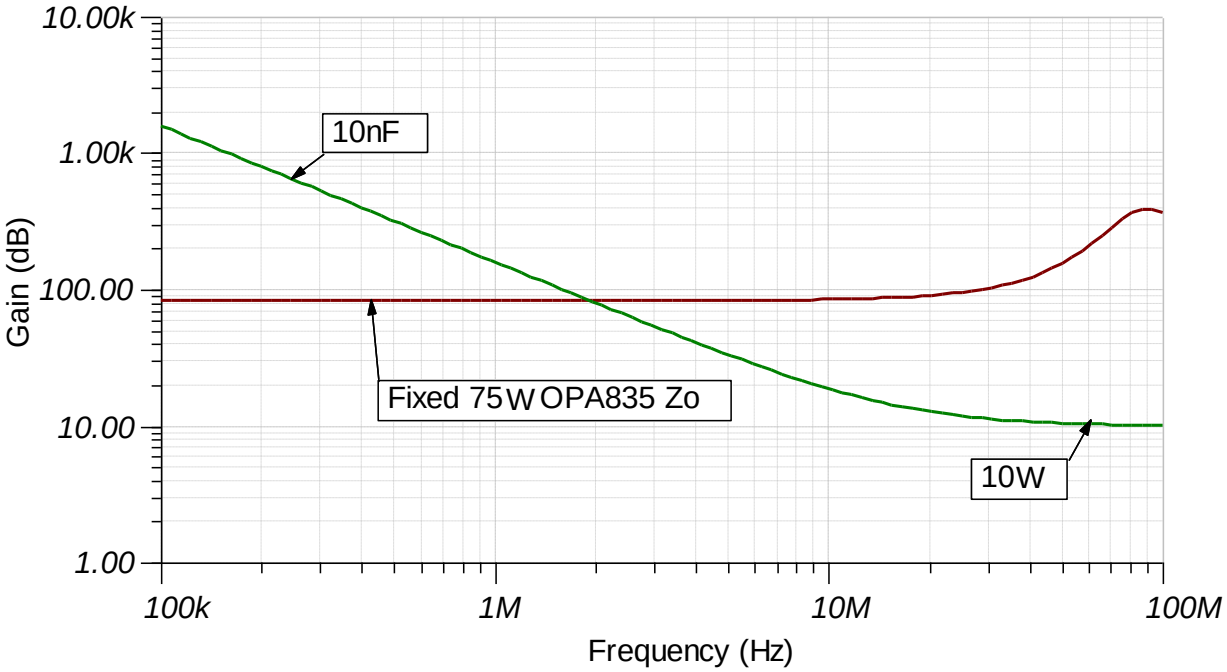
Open loop output impedance: Can I change it?



OPA835 Zo and load impedance: Compensated

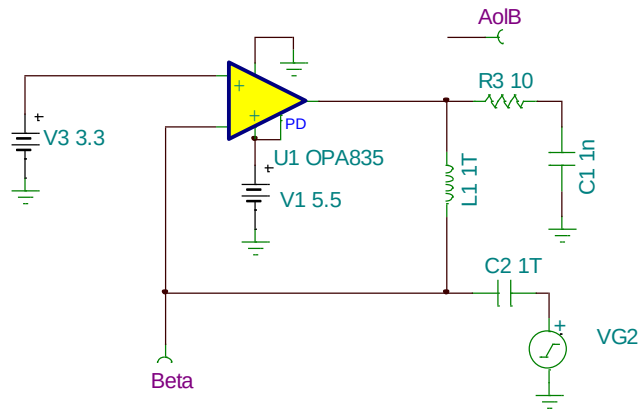


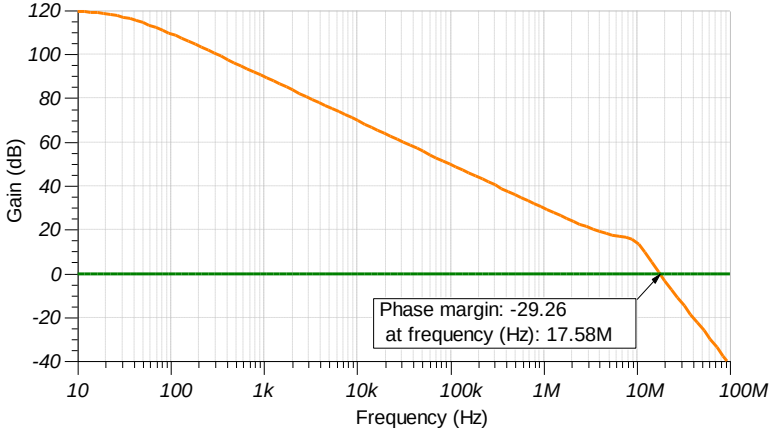
Zo(dB) = Voa(dB)
Zo(ohms) = Voa(Logarithmic)

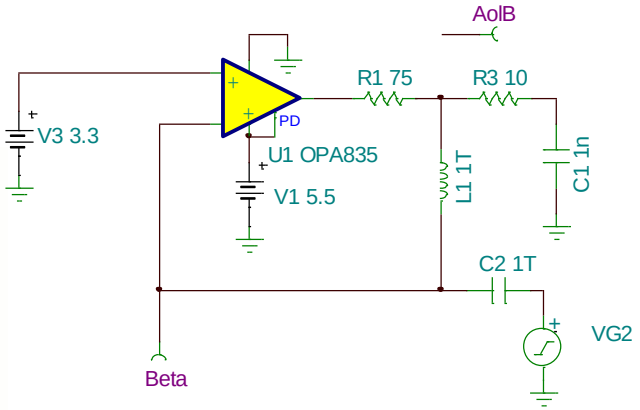


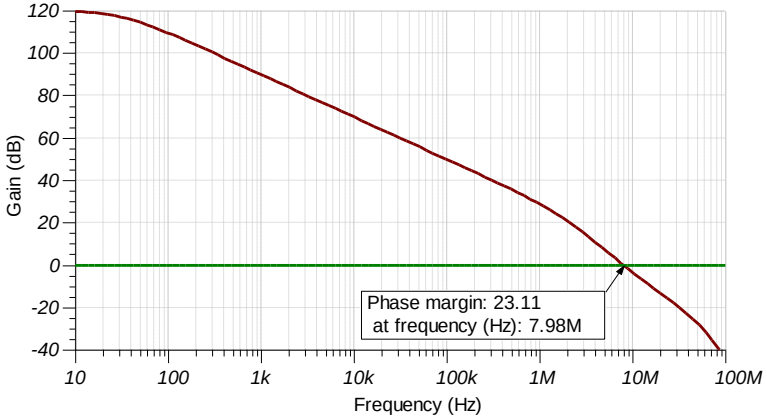
No resonance! Does this mean the circuit is stable???
Not necessarily…

Loaded Aol: With and without Ro

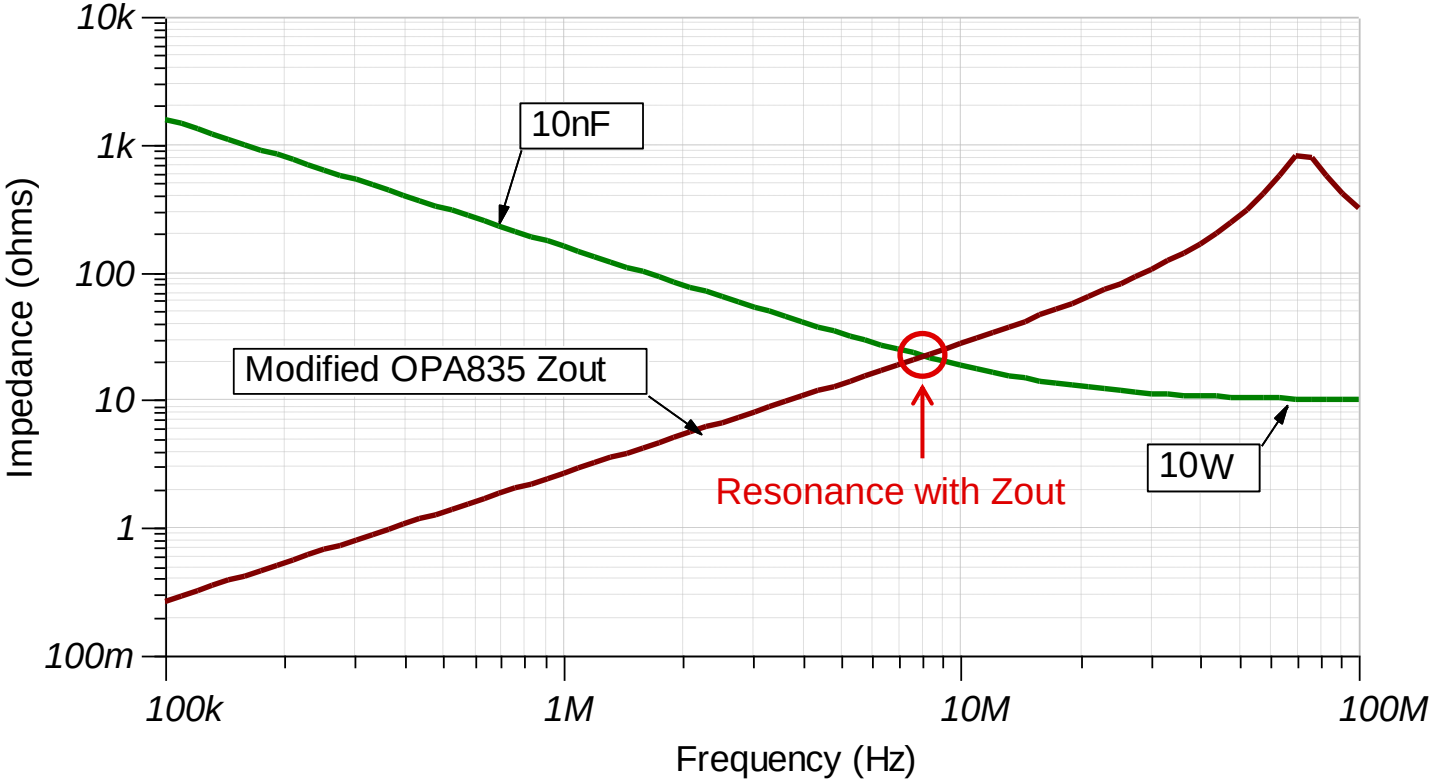




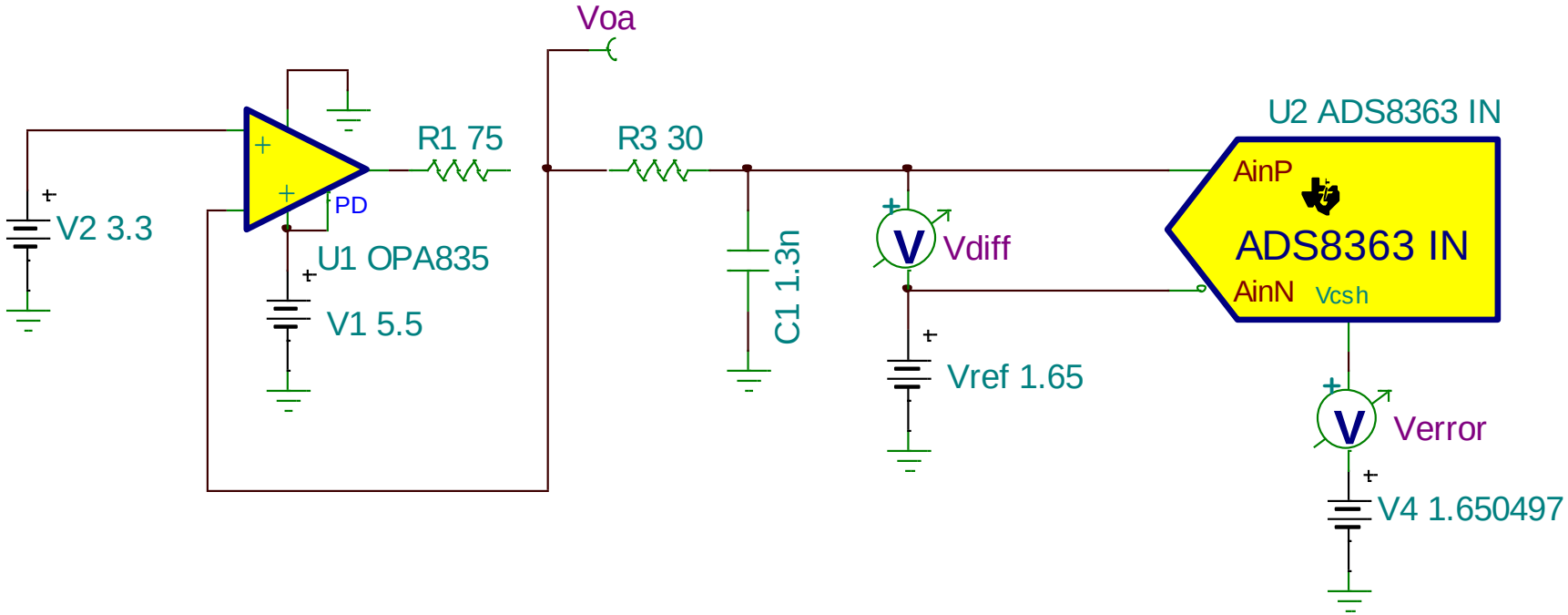




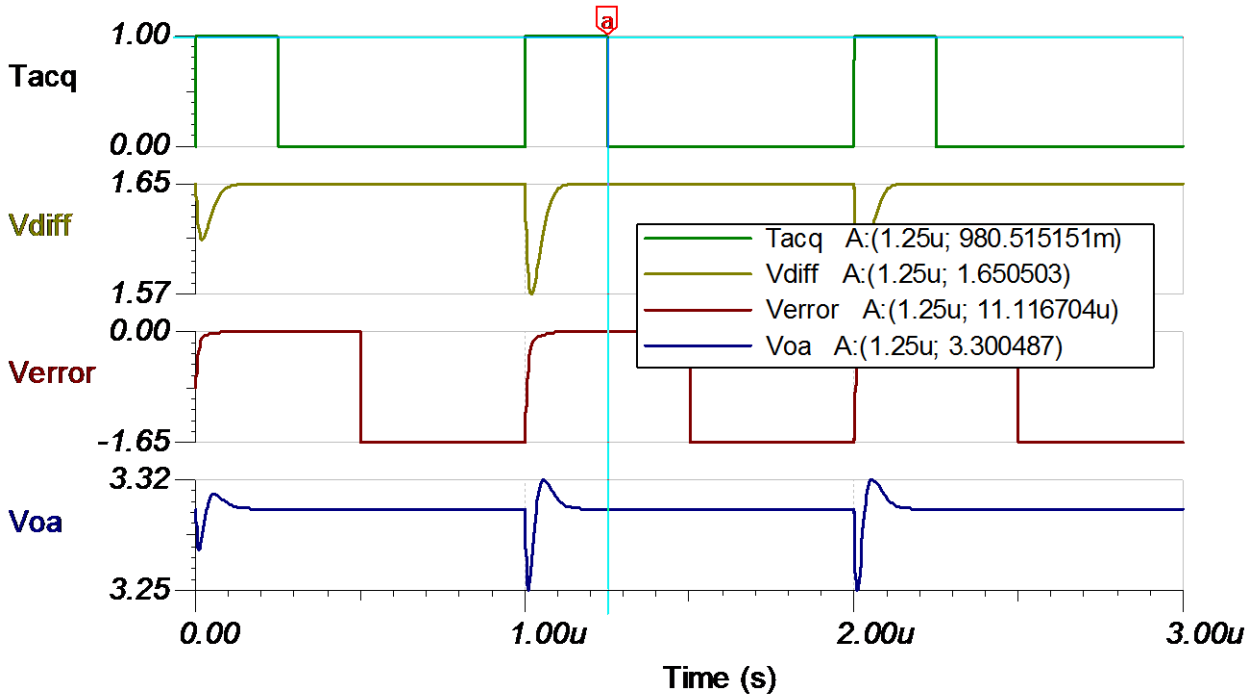
Another perspective: Zout and load impedance

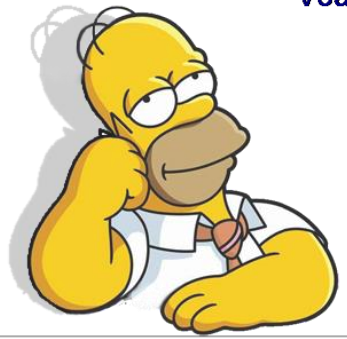


Final solution



Final solution

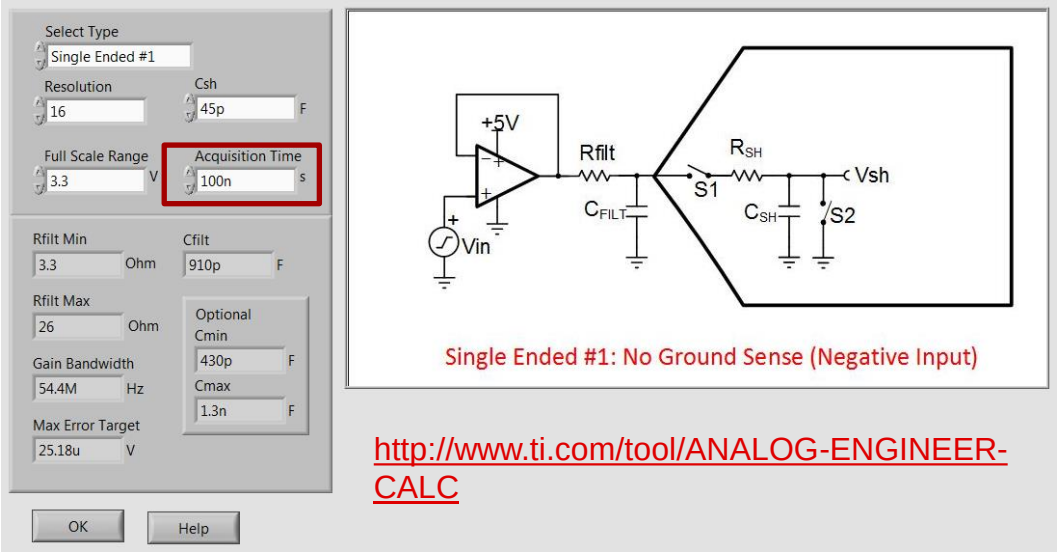




Target error: 25.81uV

Actual error: 11.11uV

What is the tradeoff?



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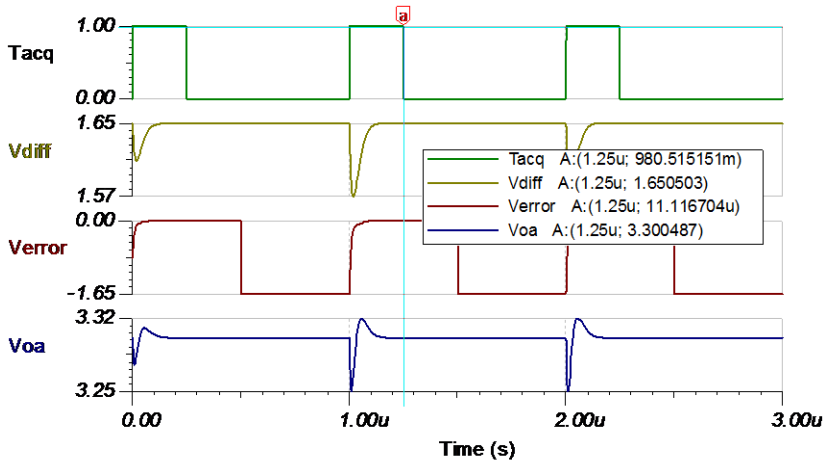
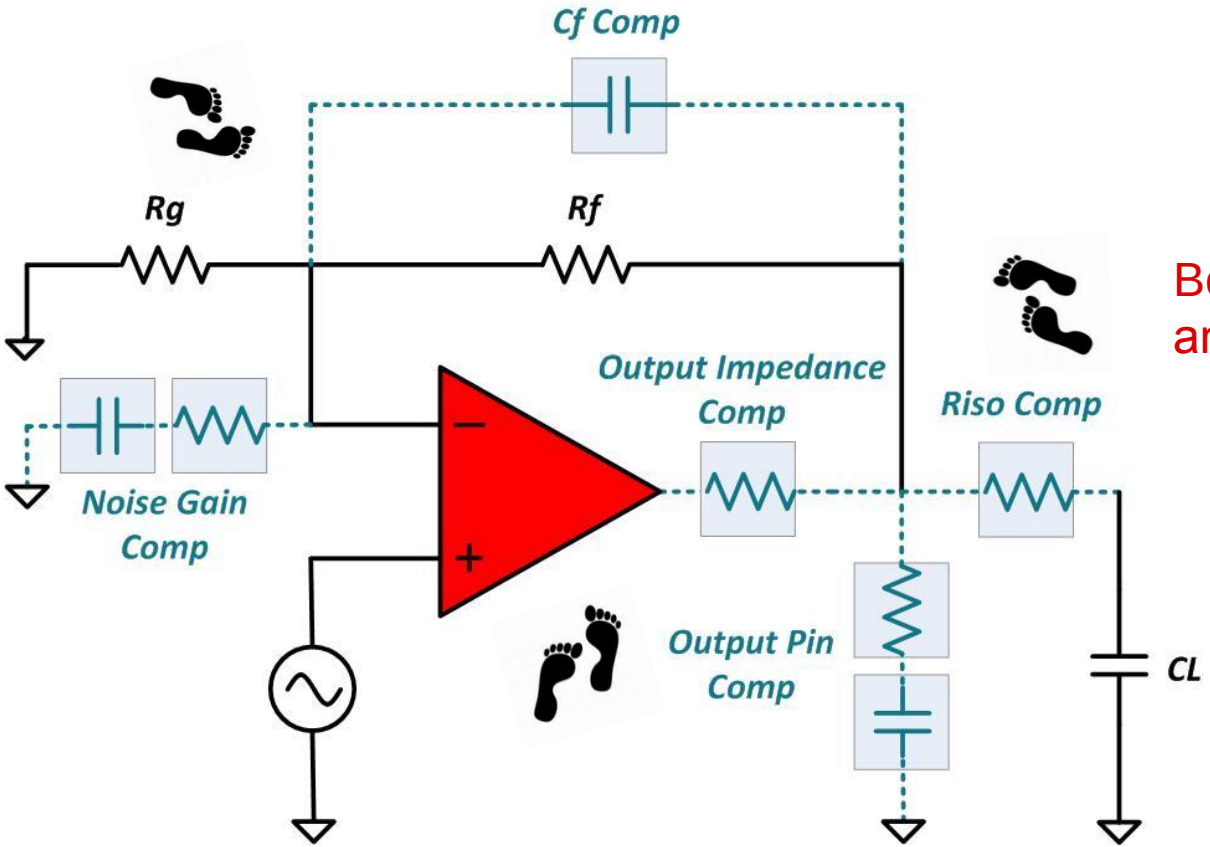


Acquisition time = 250ns

- ❑ Load transient response time depends on Zout, which depends on Zo, Aol, and 1/β
- ❑ Compensation usually sacrifices loop gain, which effectively increases Zout!

$$Z_{OUT} = Z_O / (1+Aol\beta)$$

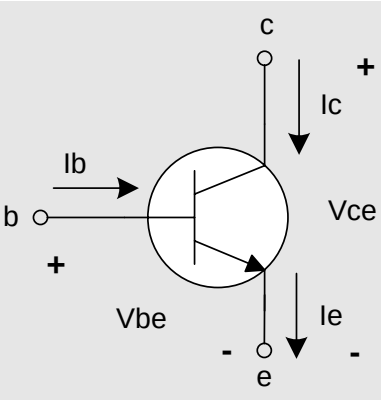
Compensation schemes: Revisited



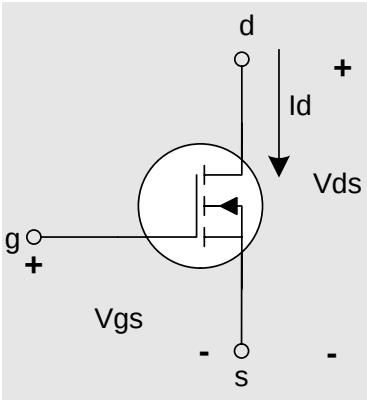
Better to have a footprint and not need it…

Choosing the right Op Amp

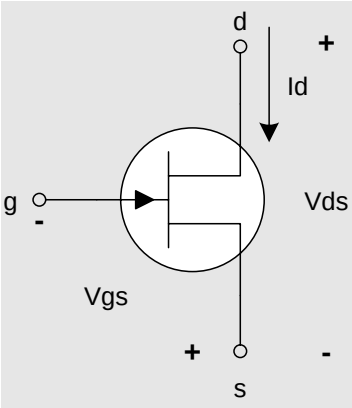
Bipolar, CMOS, JFET: Op Amp input device structures



NPN **Bipolar**



N-Channel **CMOS**



N-Channel **JFET**

1) **Current Controlled Device**
2) **"Current Controlled Current Source"**
3) **Ic = Ib *hfe**
4) **Ib = 0A turns bipolar off**
5) **Base is op amp +/- input**
6) **Highest Op Amp input current**

1) **Voltage Controlled Device**
2) **"Voltage Controlled Resistor"**
3) **Vgs > 2V controls Rds_on**
4) **Vgs=0V turns MOSFET off**
5) **Gate is op amp +/- input**
6) **Very Low Op Amp input current**

1) **Voltage Controlled Device**
2) **"Voltage Controlled Resistor"**
3) **0V< Vgs < -2V controls Rds_on**
4) **Vgs < -2V turns JFET off**
5) **Gate is op amp +/- input**
6) **Very Low Op Amp input current**

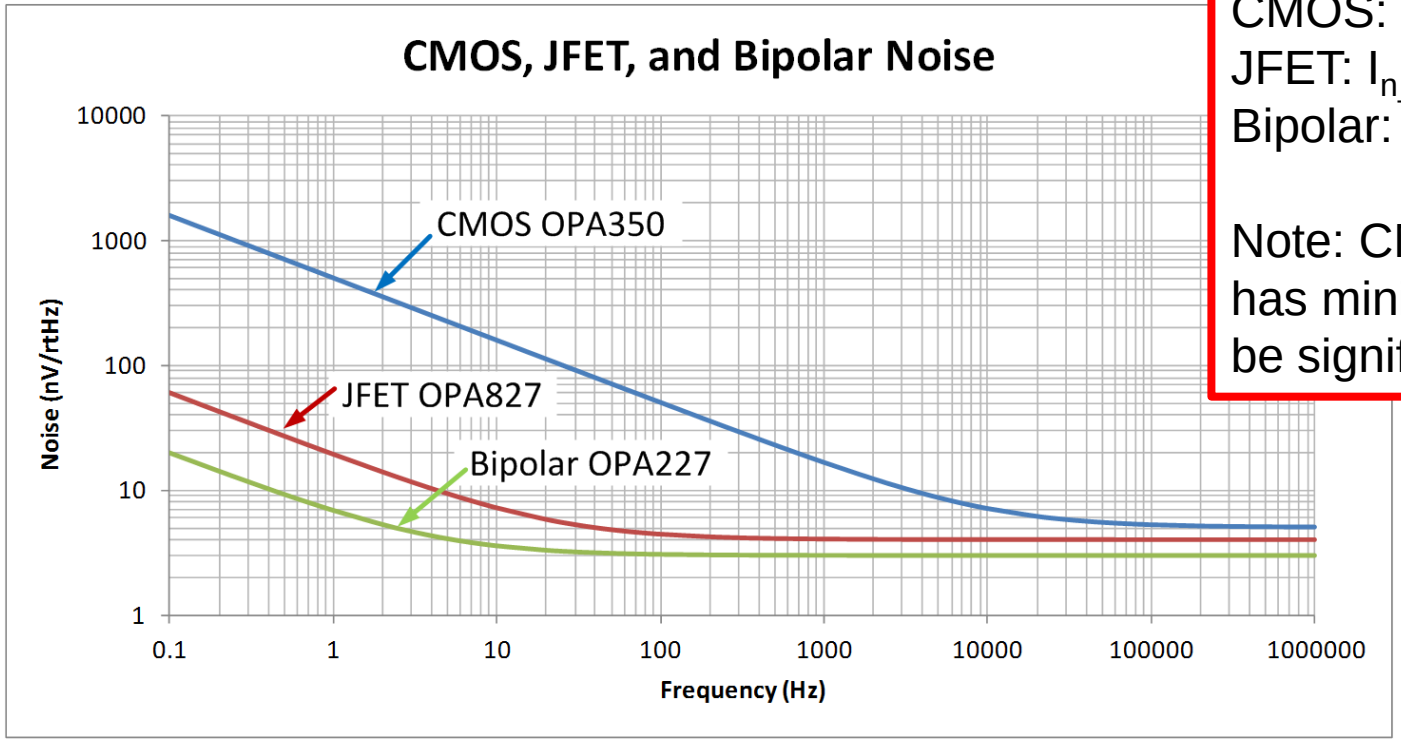
Summary CMOS vs. Bipolar vs. JFET

Parameter	CMOS	Bipolar	JFET
Vos	☒ Generally Larger than bipolar. Complex trim. Inherent ≈ 5mV, Trimmed ≈ 500uV ☑ Can use zero drift, and package trim.	☑ Generally smaller than JFET and CMOS. Laser Trim Only. Inherent ≈ 200uV, Trimmed ≈ 20uV	☒ Generally Larger than bipolar. Complex trim. Laser Trim Only. Inherent ≈ 1mV, Trimmed ≈ 100uV
Vos Drift	☒ Generally Larger than bipolar. Complex trim. ☑ Very good if using chopper.	☑ Inherently linear and easer to trim. Laser Trim Only.	☒ Generally Larger than bipolar. Complex trim. Laser Trim Only.
Ib	☑ Low compared with bipolar Ib ≈ 1pA @ 25C	☒ Much larger than CMOS and JFET. Can use bias current calculation. Inherent ≈ 100nA, Canceled ≈ 1nA	☑ Low compared with bipolar Ib ≈ 1pA @ 25C
Ib Drift	☒ Doubles every 10C, diode leakage I_{B_room} ≈ 1pA , T = 25C I_{B_hot} ≈ 1000pA , T = 125C	☑ Small compared to room temp I_{B_room} ≈ 1nA , T = 25C I_{B_hot} ≈ 3nA , T = 125C	☒ Doubles every 10C, diode leakage I_{B_room} ≈ 1pA , T = 25C I_{B_hot} ≈ 1000pA , T = 125C
Ibos	☒ Large offset current that is comparable to Ib. Don't use resistor to cancel effects. Ib ≈ ±1pA, Ibos = ±1pA	☑ When bias current cancellation is not used Ibos is low relative to Ib. Resistor can help cancel effects. Ib = 100nA, Ibos = ±1nA ☑ When bias current cancellation is used Ibos is comparable to Ib. Don't use resistor to cancel effects. Ib = ±1nA, Ibos = ±1nA	☒ Large offset current that is comparable to Ib. Don't use resistor to cancel effects. Ib ≈ ±1pA, Ibos = ±1pA

Summary CMOS vs. Bipolar vs. JFET

Parameter	CMOS (3xx)	Bipolar	JFET
Broadband Noise	☒ Generally Larger than bipolar. Noise decreases to the square root of Id.	☑ Generally smaller than JFET and CMOS. Noise decreases directly with Id.	☒ Slightly higher than Bipolar
1/f Noise	☒ Generally worse than bipolar. Noise Corner > 1kHz	☑ Generally better than CMOS. Noise Corner < 10Hz	☑ Generally better than CMOS, but not as good as bipolar. Noise Corner < 100Hz
Back-to-Back Diodes	☑ May or may not be required. Check Data Sheet!	☒ Generally required	☑ Not required. Check Data Sheet
Integrated Digital?	☑ Yes. i.e. Chopper, package trim	☒ No	☒ No
Rail to Rail Input	☑ Yes	☒ No.	☒ Not common. Difficult
Rail to Rail Output	Very close to the rail. 10mV	Close to the rail. 200mV	Same as bipolar
Output vs. Load	☒ Falls off quickly with load. Ron of output transistor.	☑ Relatively flat until you reach current limit. Vsat not related to Ron as with CMOS.	Same as bipolar

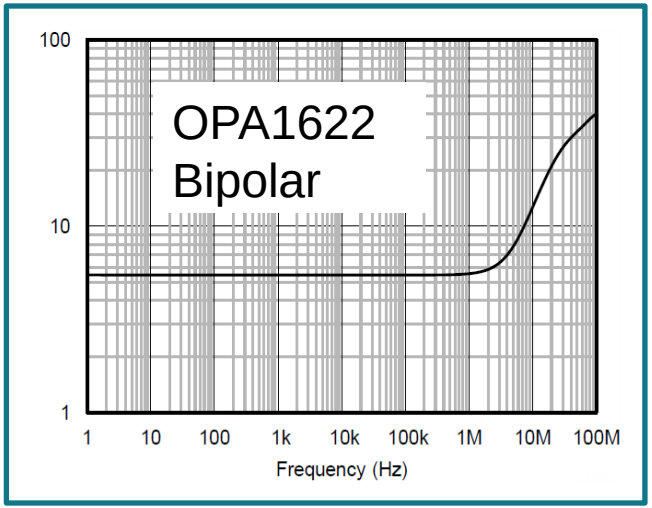
JFET, Bipolar, and CMOS: Noise

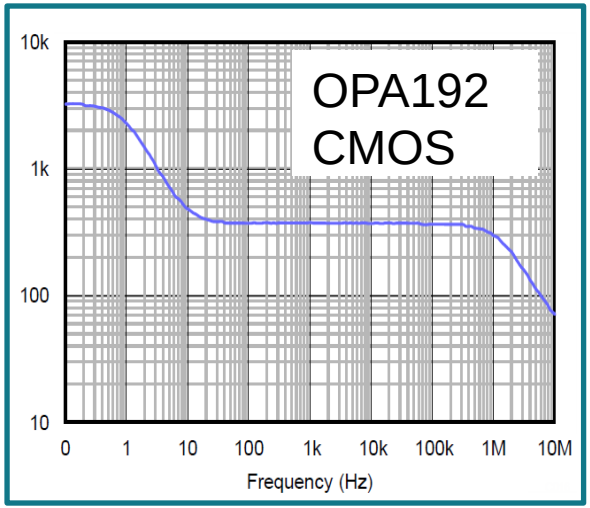


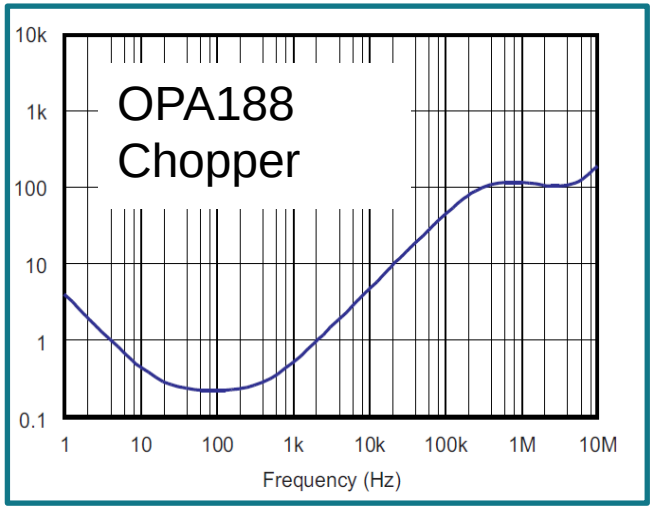
CMOS: I_{n_350} = 4fA/rtHz
JFET: I_{n_827} = 2.2fA/rtHz
Bipolar: I_{n_277} = 200fA/rtHz

Note: CMOS current noise has minimal 1/f, but it may be significant in bipolar

Bipolar vs. CMOS: Open loop output impedance







Bipolar is generally the flattest and lowest Zo

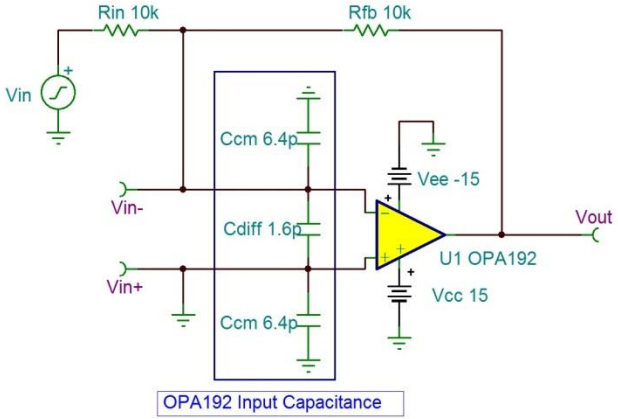
CMOS Zo is often higher and not as flat as Bipolar.

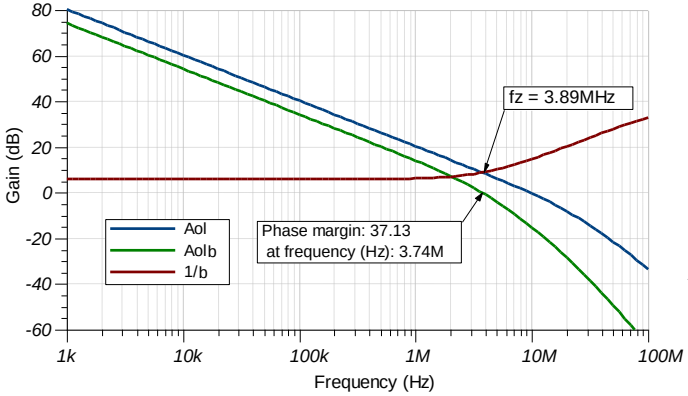
Zero Drift and µPower amplifiers often have complex Zo.

Common application issues

Input capacitance and the rule of 10: OPA192

INPUT IMPEDANCE				
Z_{ID}	Differential		100 || 1.6	MΩ || pF
Z_{IC}	Common-mode		1 || 6.4	10^{13}Ω || pF





$$Cin(eq) = Ccm + Cdiff = 8pF$$

$$Req = \frac{Rfb \times Rin}{Rfb + Rin} = 5k\Omega$$

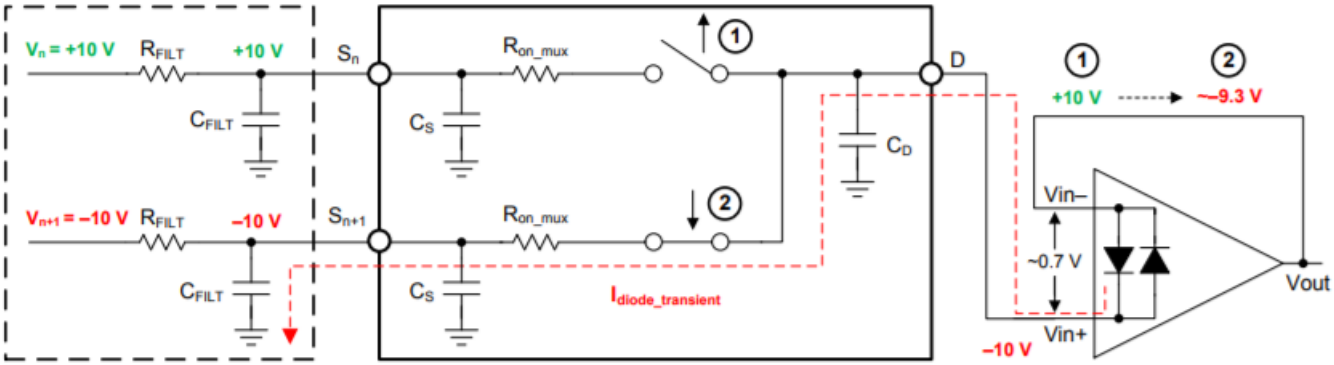
$$Fz = \frac{1}{2\pi \times Cin(eq) \times Req} = 3.98MHz$$

Problem: 10MHz amplifier + 10kΩ resistors results in instability from input capacitance

Solution: Place a capacitor in parallel with Rfb.

Choose Cfb ≥ Cin(eq)

Anti-parallel input diodes: Bipolar, Chopper, HV CMOS



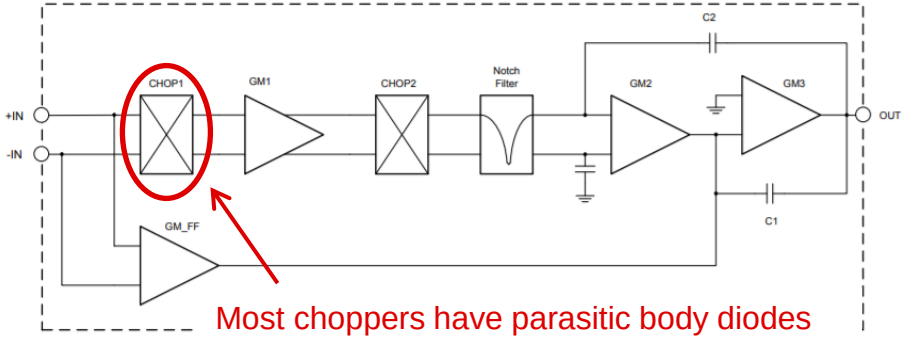
Input Low Pass Filter *Simplified Mux Model* *Buffer Amplifier*

Avoid input diodes in these applications:

- Comparators
- Multiplexed inputs
- Square wave input circuits that require fast settling

Use MUX friendly input devices!

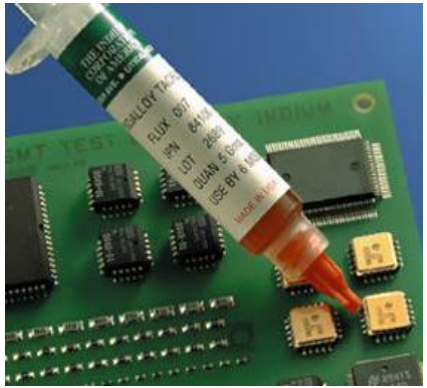
http://www.ti.com/lit/an/sbot040/sbot040.pdf

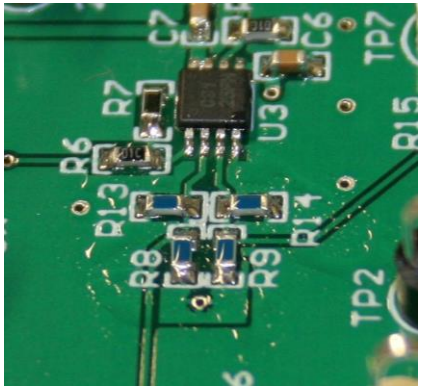


Most choppers have parasitic body diodes from MOSFET switches (OPA189 and OPA388 are exceptions)

Flux contamination

- Improper cleaning of solder flux can cause **huge** DC voltage errors!
  - These errors are random in nature and are nearly impossible to predict
- Use an Ultrasonic bath (or similar) for final cleaning of all hand-assembled or reworked PCBs
  - PCBs assembled by a contracted assembly house should already use suitable post-assembly cleaning methods
- Bake assembled and cleaned PCBs at slightly elevated temperature to remove any residual moisture
  - e.g. 70°C, 10 minutes
- Place guard rings around critical signal traces to reduce PCB surface leakage currents
  - See "Op Amp Precision Design: PCB Layout Techniques" for more information





Additional resources

DIYAMP-EVM: ti.com/diyamp-evm

The industry's most versatile amplifier EVM!

Universal Do-It-Yourself (DIY) Amplifier Circuit Evaluation Module

(ACTIVE) DIYAMP-EVM

Description & Features | Technical Documents | Support & Training | Order Now

Features

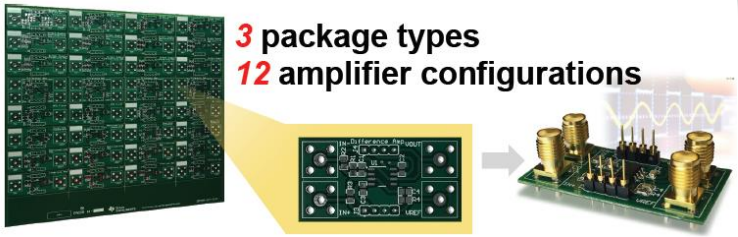
- **3 packages** to choose from (for single):
  - *SC70-5, SOT23-5, SOIC-8*
- **12 functions** to choose from, including:
  - *Noninverting, Inverting, Active Filters, Difference Amp, Comparator and more!*
- Optimized for robustness:
  - *Standardized layout is configured for optimum performance*
- Multiple interface options:
  - *SMA, Header, Bluewire, Breadboard*

Benefits

- Multiple package and function options increases speed and versatility of prototyping
- Flexible prototyping and debugging
- Efficient evaluation of multiple amplifiers or comparators under identical test conditions
- Allows for precise side by side comparisons

Applications

- Existing designs: performance enhancement
- New designs: prototyping, trouble shooting and debugging



Compatible with ADC and DAC EVMs

Includes: 32 coupon boards, Terminal strips

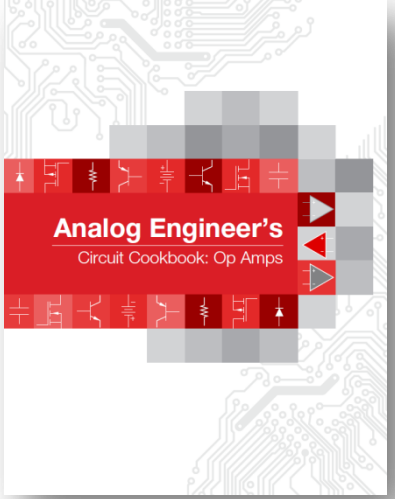
Click For More Information

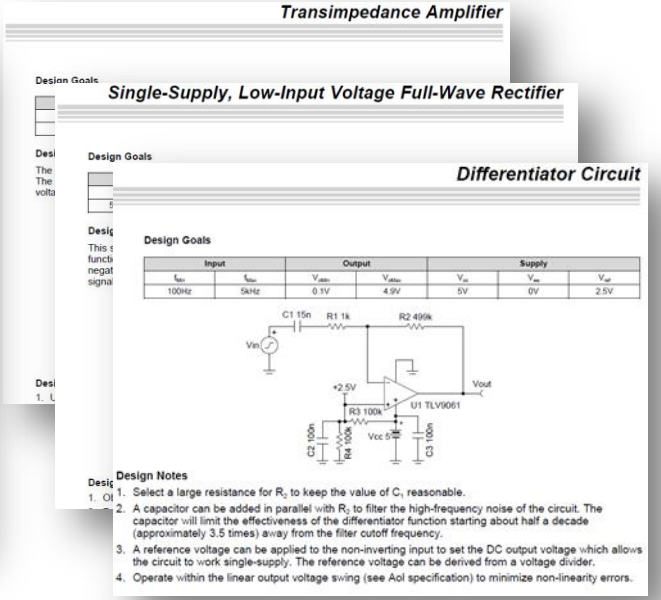
Analog Engineer’s Op-Amp Cookbook

Analog Engineer’s Op-Amp Cookbook:

- ❑ Includes examples of common op amp topologies
- ❑ Walks through design techniques
- ❑ Provides unique amplifier circuits, including SPICE models, for quick adaptation to any end equipment or product
- ❑ Includes >25 common op-amp circuits, from inverting amplifier to PWM generation and more
- ❑ ***Free download on ti.com***

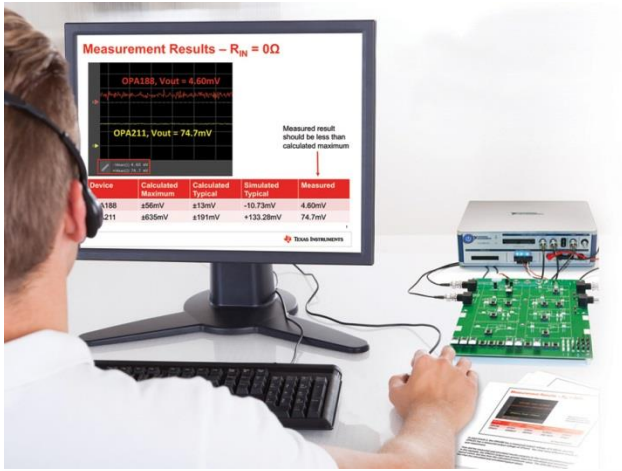
Coming 1Q18 to TI.com!



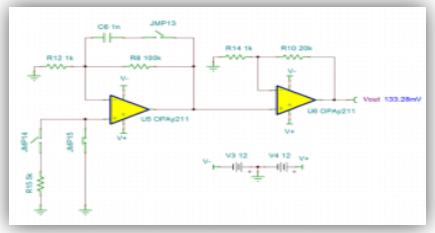


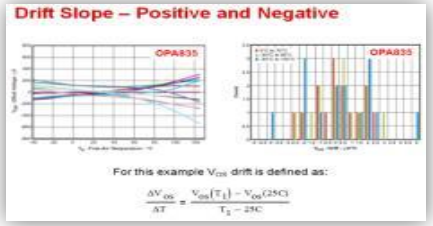
TI Precision Labs- online analog learning

www.ti.com/precisionlabs

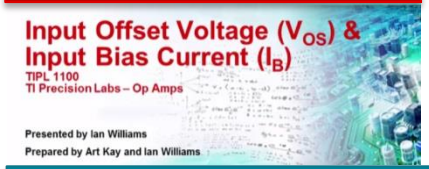


- < 15 minute each video
- Lectures & Labs with quizzes and experiments
- For both new and experienced engineers

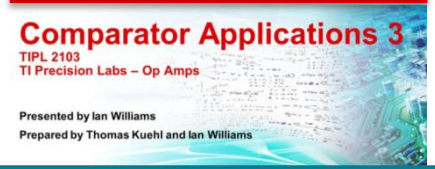




Op Amps

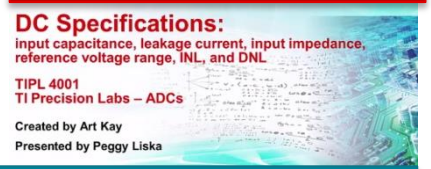


Comparators



MUXes

ADCs



More than 70 videos!

Additional resources

- Tim Green and Collin Wells' stability series
  - https://e2e.ti.com/support/amplifiers/precision_amplifiers/w/design_notes/2645.solving-op-amp-stability-issues
- How to verify a macromodel against the datasheet
  - Ian Williams' "Trust but Verify" series - https://e2e.ti.com/blogs_/b/analogwire/archive/2017/07/27/trust-but-verify-spice-model-accuracy-part-1-common-mode-rejection-ratio-cmrr

Thank you!

Questions?

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