TECH DAYS
Texas Instruments

Primary-side regulated (PSR) flyback converter design

– for low power DC/DC applications

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TI training – summary

PSR Flyback DC/DC Converter Design:
There is a growing demand for isolated, low-power bias supplies with wide V_{IN} range and accurate output voltage regulation for use in several industrial and automotive applications. In this presentation we describe the PSR flyback converter and identify a feature set that makes it suitable for these applications. We highlight both electrical and magnetic design considerations and showcase three PSR flyback design examples to illustrate efficiency and regulation performance attributes.

What you'll learn:

1. PSR flyback converter features and benefits and related end equipment
2. PSR flyback modes of operation and component selection guidelines
3. Magnetic design considerations and what to specify when dealing with a magnetics component vendor
4. Design tips for single- and dual-output configurations
5. How to choose between PSR flyback, Fly-Buck and push-pull topologies

Course Details:

- Type: PPT presentation
- Duration: 1:30h / English
- Audience: FAEs, Apps, System Apps

TI Products and Solutions:

- LM5180, LM5180-Q1
- LM5160/1
- LM5017/8/9
- SN6501/5

Agenda

Isolated converters

- Isolated topologies overview
- PSR flyback topology – features and benefits, end equipment serviced

PSR flyback converter

- Operating modes – BCM, DCM, FFM
- Circuit design considerations – C_{IN}, C_{OUT}, D_F, V_{SW} clamp, UVLO, SS, TC, FB
- Magnetic design considerations – turns ratio, L_{MAG}, L_{LEAK}, ladder model
- Cross regulation in dual-output designs – secondary current distribution

PSR flyback implementation

- Design examples & lab results – efficiency, regulation, key waveforms
- PCB layouts for single and dual outputs
- Common-mode EMI mitigation

Positioning PSR flyback converters

- Choosing between PSR flyback, Fly-Buck and push-pull topologies
- Competitive analysis and spec comparison

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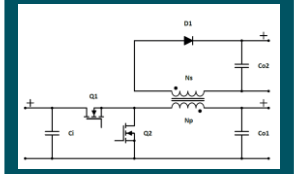
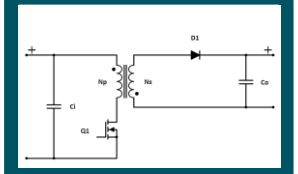
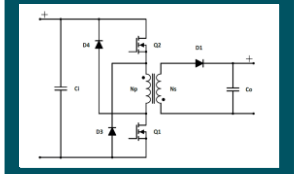
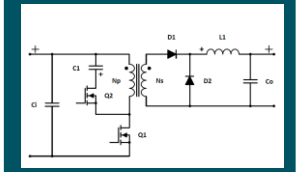
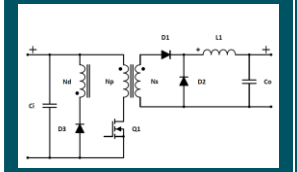
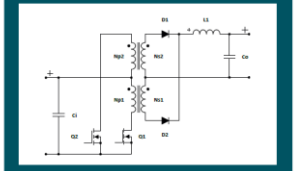
Different isolated power topologies

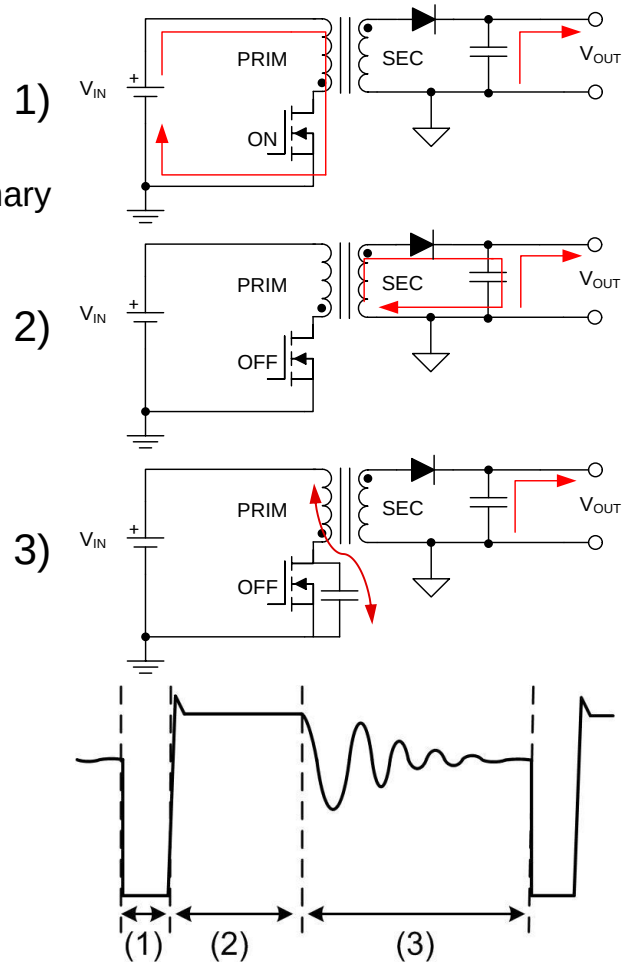
Coupled inductor (has an airgap)

Transformer (no airgap)

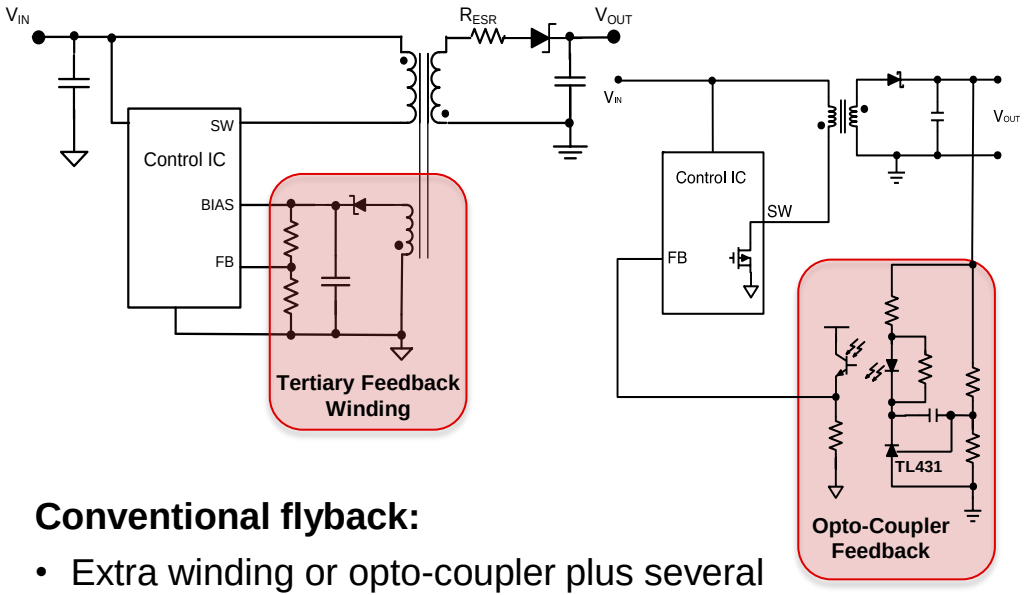
	Fly - Buck™	Flyback	Two Switch Flyback	Active Clamp Forward	Single Switch Forward	Push-Pull
						
Duty Cycle	$D = \frac{V_{out_pri}}{V_{in}}$	$D = \frac{(V_{out} + V_f) \cdot \frac{N_p}{N_s}}{V_{in} + (V_{out} + V_f) \cdot \frac{N_p}{N_s}}$	$D = \frac{(V_{out} + V_f) \cdot \frac{N_p}{N_s}}{V_{in} + (V_{out} + V_f) \cdot \frac{N_p}{N_s}}$	$D = \frac{(V_{out} + V_f)}{V_{in} \cdot \frac{N_s}{N_p}}$	$D = \frac{(V_{out} + V_f)}{V_{in} \cdot \frac{N_s}{N_p}}$	$D = \frac{1}{2} \cdot \frac{(V_{out} + V_f)}{V_{in} \cdot \frac{N_s}{N_p}}$
Q1 FET Voltage	$V_{Q1} = V_{in}$	$V_{Q1} = V_{in} + (V_{out} + V_f) \cdot \frac{N_p}{N_s}$	$V_{Q1} = \frac{V_{in} + (V_{out} + V_f) \cdot \frac{N_p}{N_s}}{2}$	$V_{Q1} = \frac{V_{in}}{(1-D)}$	$V_{Q1} = 2 \cdot V_{in} + V_f$	$V_{Q1} = 2 \cdot V_{in}$
D1 Diode Voltage	$V_{D1} = V_{out_sec} + (V_{in} - V_{out_pri}) \cdot \frac{N_s}{N_p}$	$V_{D1} = V_{out} + V_{in} \cdot \frac{N_s}{N_p}$	$V_{D1} = V_{out} + V_{in} \cdot \frac{N_s}{N_p}$	$V_{D1} = V_{clamp} \cdot \frac{N_s}{N_p} - V_f$	$V_{D1} = (V_{in} + V_f) \cdot \frac{N_s}{N_d} - V_f$	$V_{D1} = 2 \cdot V_{in} \cdot \frac{N_s}{N_p} - V_f$
D2 Diode Voltage				$V_{D2} = V_{in} \cdot \frac{N_s}{N_p} - V_f$	$V_{D2} = V_{in} \cdot \frac{N_s}{N_p} - V_f$	

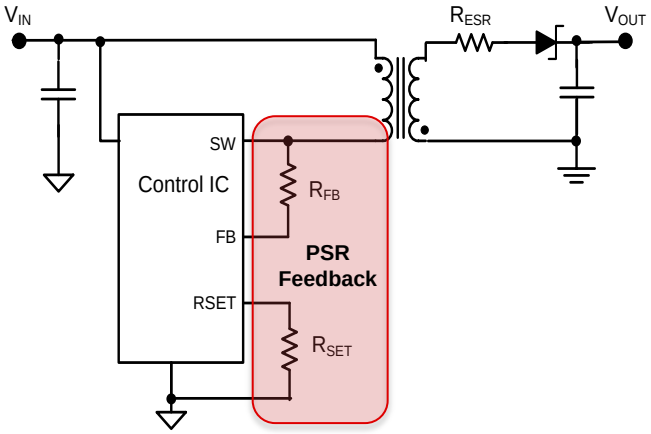
Flyback operation

- Conventional transformer stores minimal energy
- Flyback transformer – essentially a coupled inductor stores energy from primary and releases to secondary
  1) **FET ON** → only primary current flows
     - Energy transferred from source to air gap
     - Load current from output capacitor only
  2) **FET OFF** → only secondary current flows
     - Energy stored in air gap delivered to the load
  3) **FET OFF, diode OFF** →
     - DCM circulating current
     - Load current supplied by output capacitor
- CCM ⇒ not all stored energy delivered to load, primary current starts when secondary still non-zero
- DCM ⇒ all stored energy delivered to load each cycle



Conventional flyback vs. PSR flyback





Conventional flyback:

- Extra winding or opto-coupler plus several external components are required to achieve regulation with a conventional flyback topology
- Designing compensation can be challenging with an opto-coupler based solution
- **Operates in CCM or DCM mode**

PSR flyback advantages:

- Eliminates opto-coupler or tertiary winding
- Extremely tight load regulation achieved as errors from the transformer DCR, leakage inductance and secondary diode are avoided
- Smaller solution size than conventional flyback
- **Operates in DCM or Boundary Mode**

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- **Circuit design considerations – C_{IN}, C_{OUT}, D_F, V_{SW} clamp, UVLO, SS, FB**
- **Magnetic design considerations – turns ratio, L_{MAG}, L_{LEAK}, construction**
- **Cross regulation in dual-output designs – secondary currents**

PSR flyback implementation

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PSR flyback converter operation

Galvani – LM5180 / LM5180-Q1

Samples: Now
Release: 4Q'18

100V, 1.45A primary side regulated (PSR) flyback converter

Features

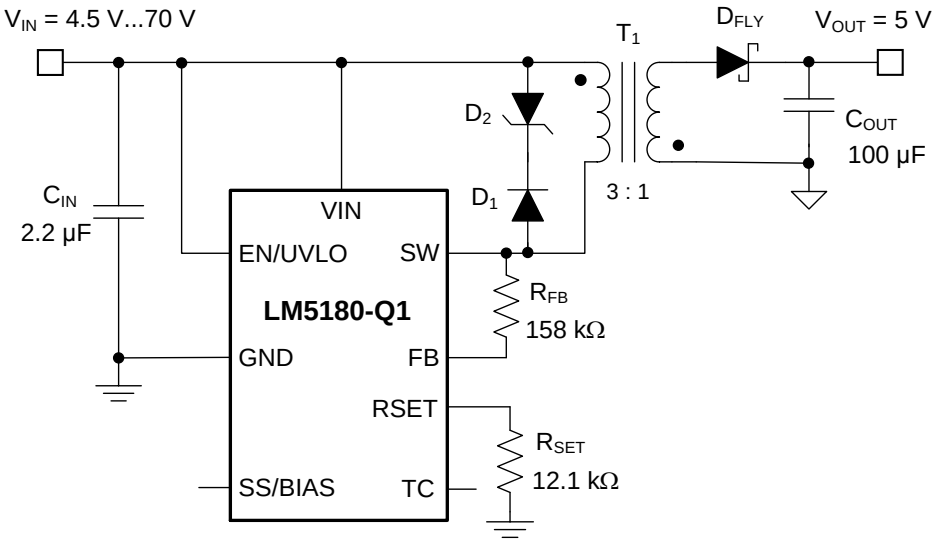
- **100V, 1.45A internal power MOSFET**
- **4.5V–70V wide V_{IN} range** (abs max 75V)
  - 3.5V minimum V_{IN} after start-up
- **V_{OUT} accuracy ±1% achievable**
  - V_{IN} = 18V–70V, V_{OUT} = 5V, 2% load to full load
  - T_A = –40°C to 125°C
- **Boundary mode**, quasi-resonant operation
- Internal loop compensation
- Adjustable input UVLO
- External V_{CC} bias option for improved efficiency
- Adjustable or fixed internal 6ms soft-start
- Optional V_{OUT} temperature compensation
- **4 mm × 4 mm WSON-8** WF package, 0.8mm pitch
- **AEC-Q100 grade 1** ⇒ 125°C operating ambient range

Applications

- Isolated DC-DC for factory automation I/O modules
- Gate drive bias in HEV/EV drives and battery chargers

Benefits

- No opto-coupler or transformer auxiliary winding needed
- Accurate V_{OUT} regulation performance with sensing at zero current
- Low I_Q operation and external BIAS rail option enable high efficiency at light loads



PSR flyback control method

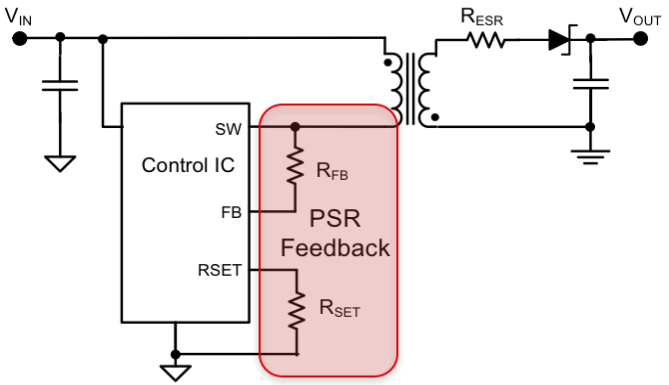
Discontinuous Conduction Mode (DCM) or Boundary Conduction Mode (BCM) are employed depending on load

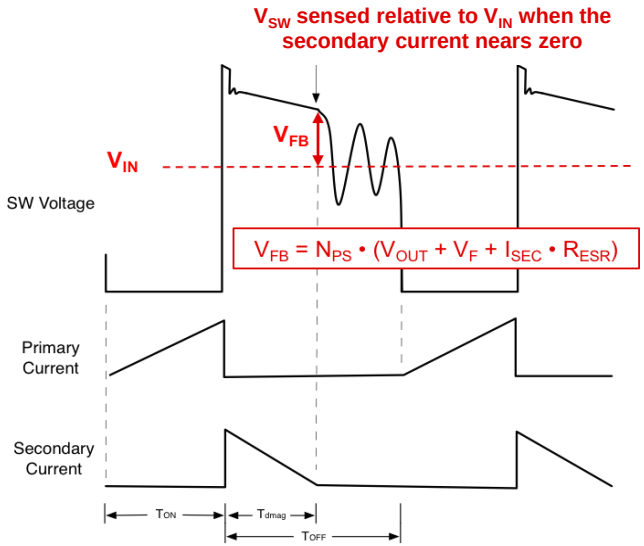
BCM from mid to max load:

- Switch turns on when secondary current reaches zero (ZCS)
- Switch turns off when peak current reaches level set by COMP output of the internal error amp
- F_{SW} decreases as peak current increases with increasing load

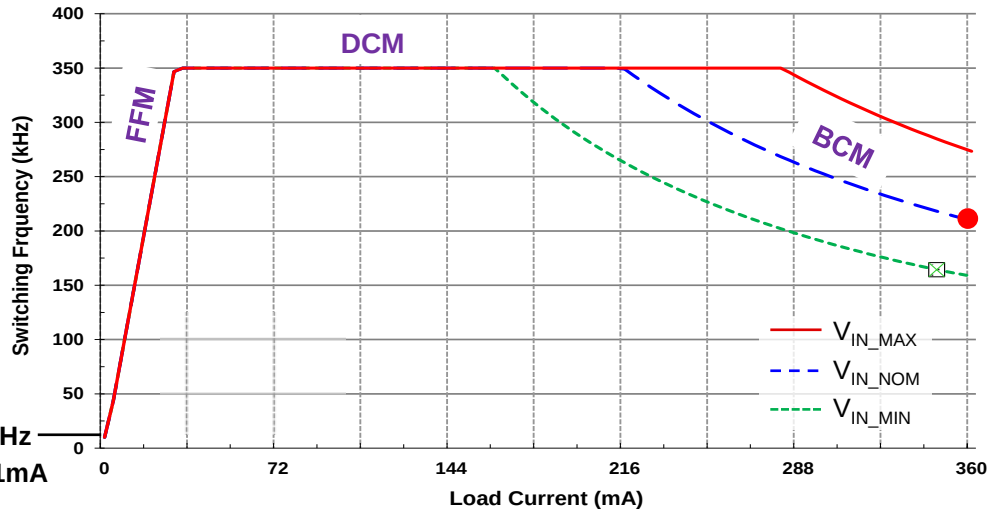
DCM for light loads:

- Peak current set by COMP decreases to minimum level (20%)
- Switch off-time increases (DCM operation) to decrease F_{SW} and output current
- Maximum off-time sets minimum F_{SW} in DCM ~12kHz
- Minimum peak current and F_{SW} set minimum load requirement to ~0.5% of full load



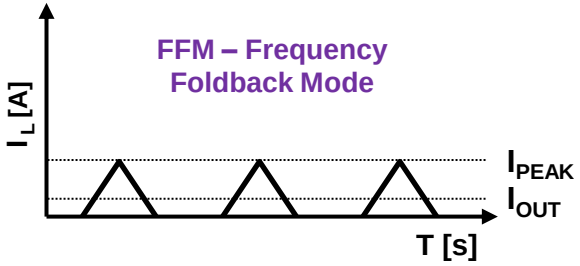


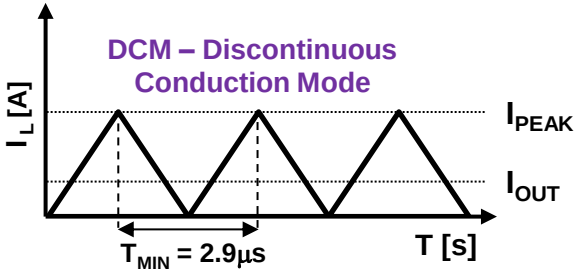
PSR flyback operating modes – F_{SW} vs. I_{OUT}

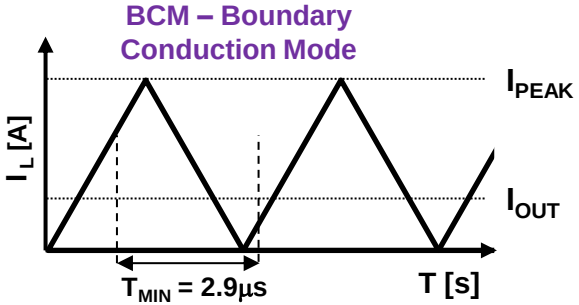


$$I_{OUT} = \frac{(1-D)\cdot I_{SEC\text{-}PK}}{2}$$

Minimum Frequency = 12kHz
Requires minimum load ~1mA



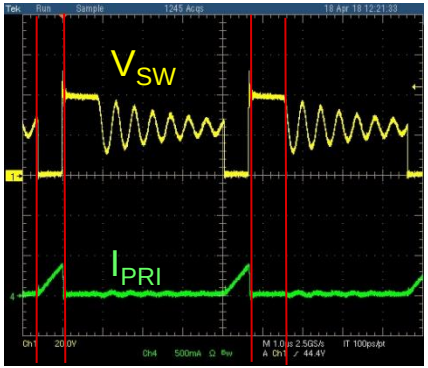




PSR flyback operating modes

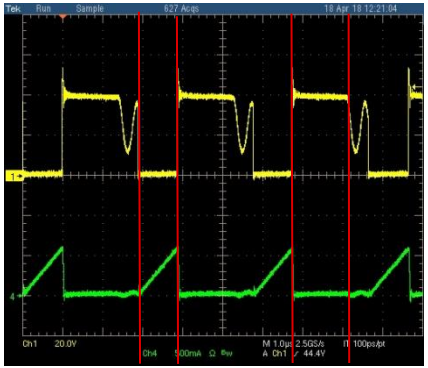
D_1 = switch conduction duty cycle
D_2 = diode conduction (flux-removing) duty cycle
$D_1 + D_2 \leq 1$

FFM (variable frequency DCM)



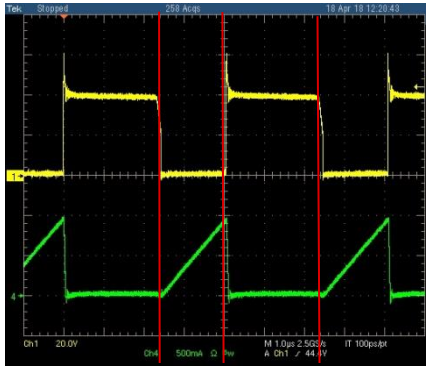
D_1 D_2

DCM



D_1 D_2

BCM



D_1 D_2

Advantages of DCM / BCM vs. CCM

- Lower switching losses
  - No diode reverse recovery loss
  - MOSFET turn-on at zero current
- Lower L_{MAG} value (higher ripple)
  - Fewer turns, lower DCR
- First-order system
  - No slope comp or RHPZ

Disadvantages of DCM / BCM vs. CCM

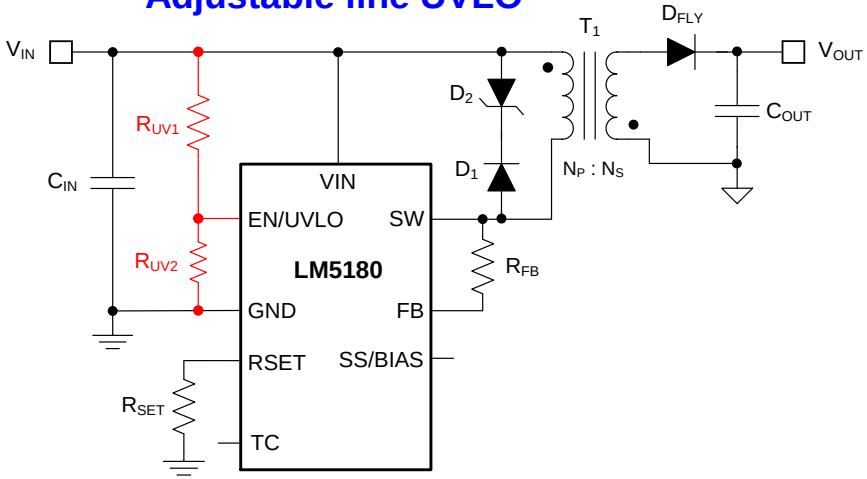
- Higher conduction loss
- Higher switch turn-off loss
- Higher core loss
- Variable F_{SW} (operating point dependent)
- Larger EMI filter, *possibly*

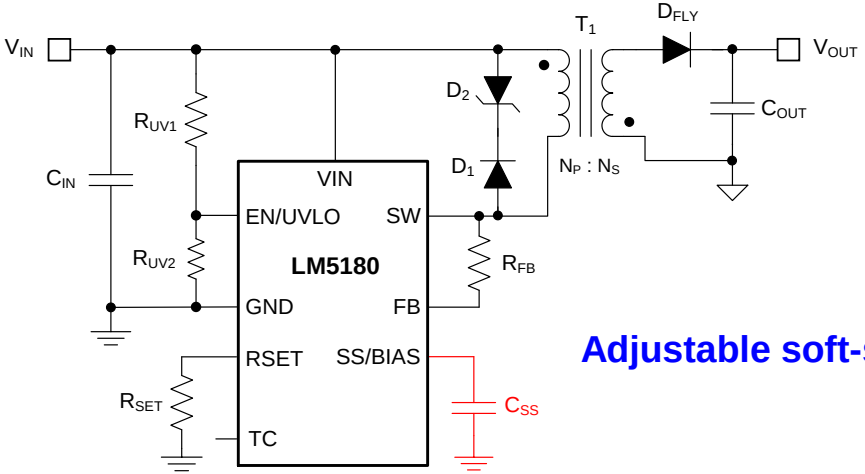
PSR flyback equations

Mode	BCM	DCM	FFM
D_1	$D_1 = \frac{(V_{OUT} + V_D) \cdot N_{PS}}{V_{IN} + (V_{OUT} + V_D) \cdot N_{PS}}$	$D_1 = \frac{\sqrt{2 \cdot I_{OUT} (V_{OUT} + V_D) \cdot F_{SW} \cdot L_{MAG}}}{V_{IN}}$	$D_1 = \frac{L_{MAG} \cdot I_{SW\text{-}PK(FFM)} \cdot F_{SW(FFM)}}{V_{IN}}$
$I_{SW\text{-}PK}$	$I_{SW\text{-}PK(BCM)} = \frac{2 \cdot V_{OUT} \cdot I_{OUT}}{\eta \cdot V_{IN} \cdot D_1}$	$I_{SW\text{-}PK(DCM)} = \sqrt{\frac{2 \cdot I_{OUT} \cdot (V_{OUT} + V_D)}{L_{MAG} \cdot F_{SW\text{-}DCM}}}$	$I_{SW\text{-}PK(FFM)} = \frac{I_{SW\text{-}PK(max)}}{5} = 0.29\,A$
F_{SW}	$F_{SW(BCM)} = \frac{1}{I_{SW\text{-}PK} \cdot \left[\frac{L_{MAG}}{V_{IN}} + \frac{L_{MAG}}{N_{PS} \cdot (V_{OUT} + V_D)} \right]}$	$F_{SW(DCM)} = F_{CLAMP} = 350\,kHz$	$F_{SW(FFM)} = \frac{I_{OUT(FFM)}}{T_{OFF(FFM)} \cdot N_{PS} \cdot I_{SW\text{-}PK(FFM)} / 2}$
T_{OFF}	$T_{OFF(BCM)} = \frac{L_{MAG} \cdot I_{SW\text{-}PK(BCM)}}{N_{PS} \cdot (V_{OUT} + V_D)}$	$T_{OFF(DCM)} = \frac{L_{MAG} \cdot I_{SW\text{-}PK(DCM)}}{N_{PS} \cdot (V_{OUT} + V_D)}$	$T_{OFF(FFM)} = \frac{L_{MAG} \cdot I_{SW\text{-}PK(FFM)}}{N_{PS} \cdot (V_{OUT} + V_D)}$
I_{OUT}	$P_{OUT(BCM)max} = \eta \cdot V_{IN} \cdot D_1 \cdot \frac{I_{SW\text{-}PK(max)}}{2}$	$I_{OUT(DCM)max} = \frac{T_{OFF} \cdot I_{SW\text{-}PK(DCM)} \cdot N_{PS} \cdot F_{SW(DCM)}}{2}$	$I_{OUT(FFM)max} = \frac{T_{OFF} \cdot I_{SW\text{-}PK} \cdot N_{PS} \cdot F_{SW(FFM)}}{2}$

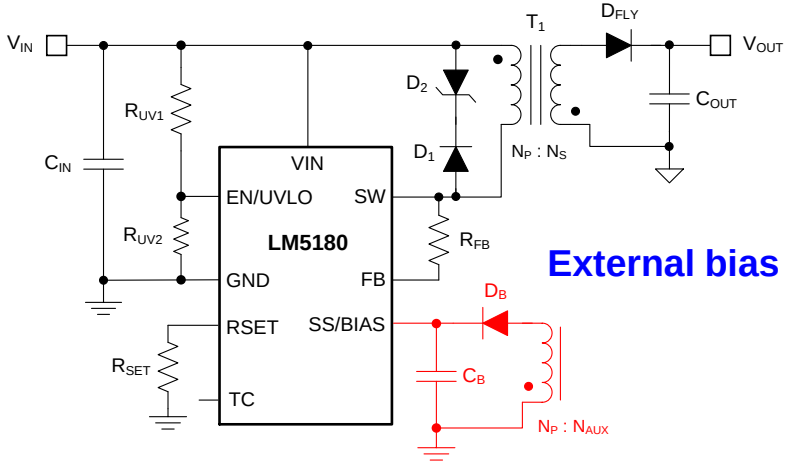
Application options

Adjustable line UVLO





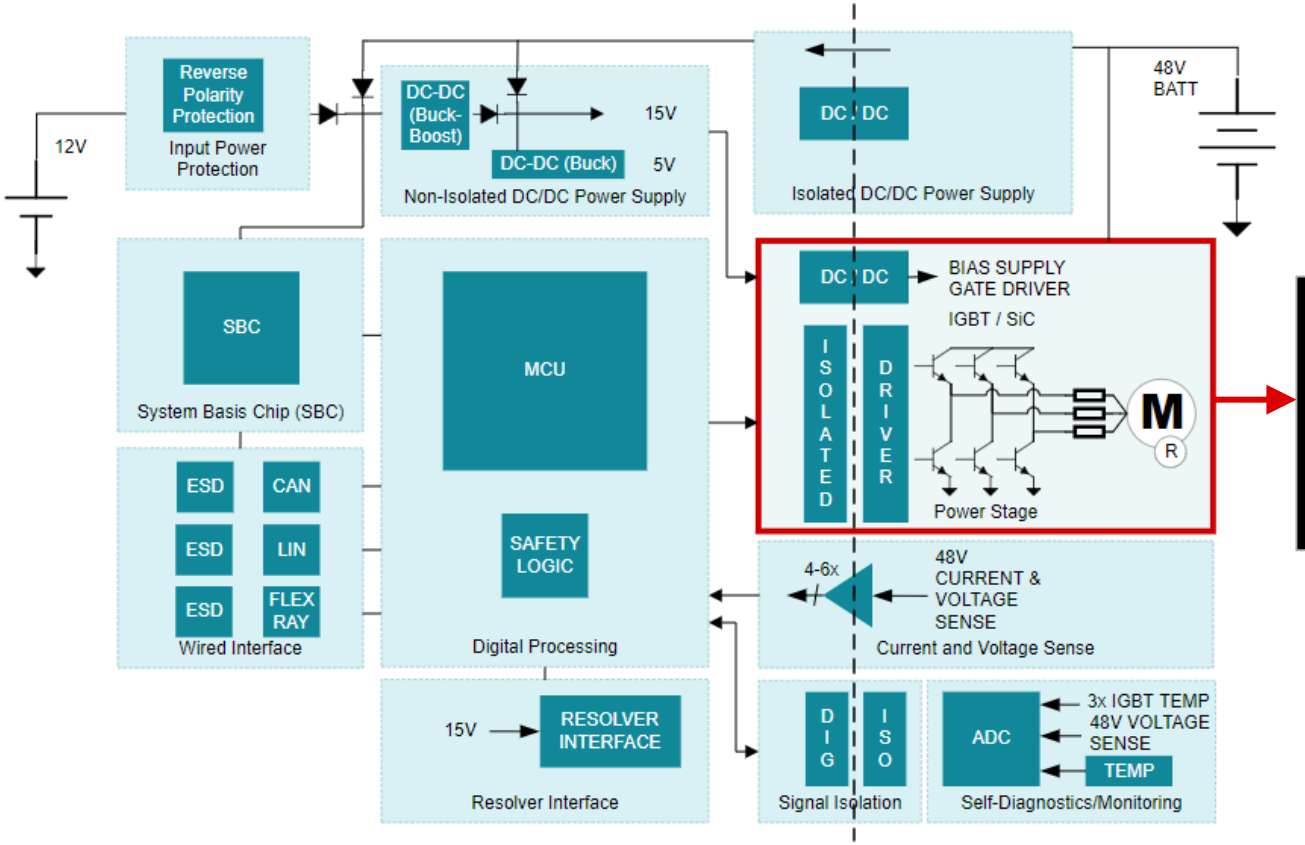
Adjustable soft-start



External bias supply

SS/BIAS pin	Soft-start time	Gate drive supply
Open	Fixed 6ms	V_{IN}
Capacitor	Adj > 6ms	V_{IN}
Bias winding	Fixed 6ms	V_{BIAS}

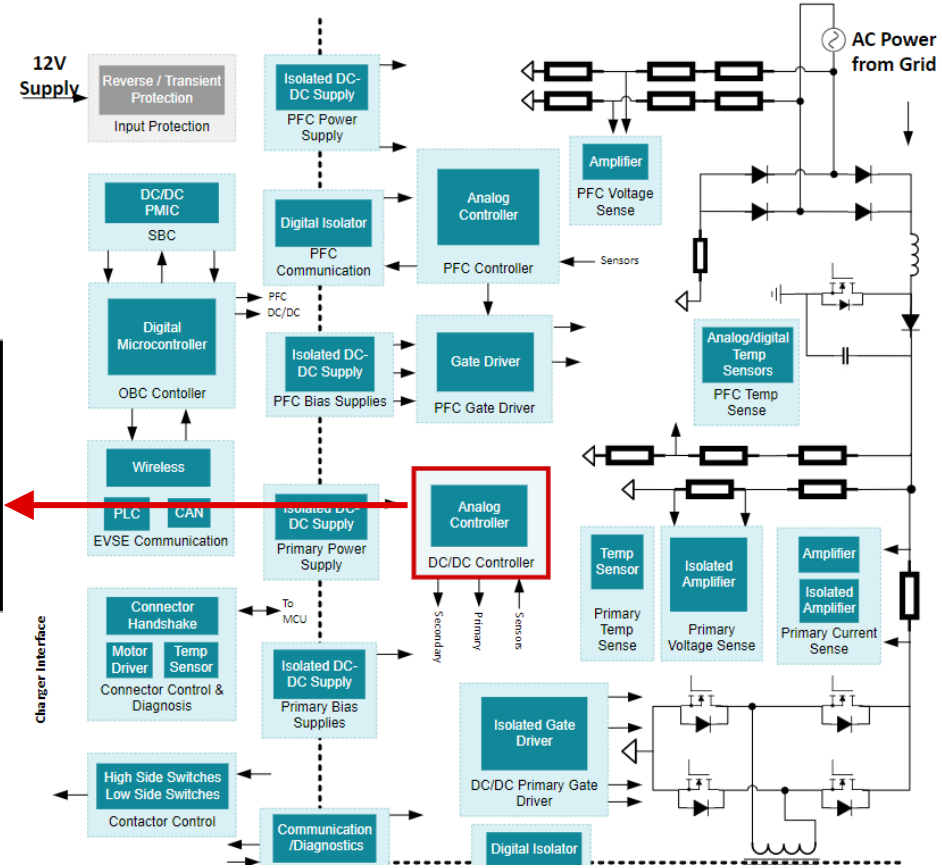
Inverter and motor control – reference diagram



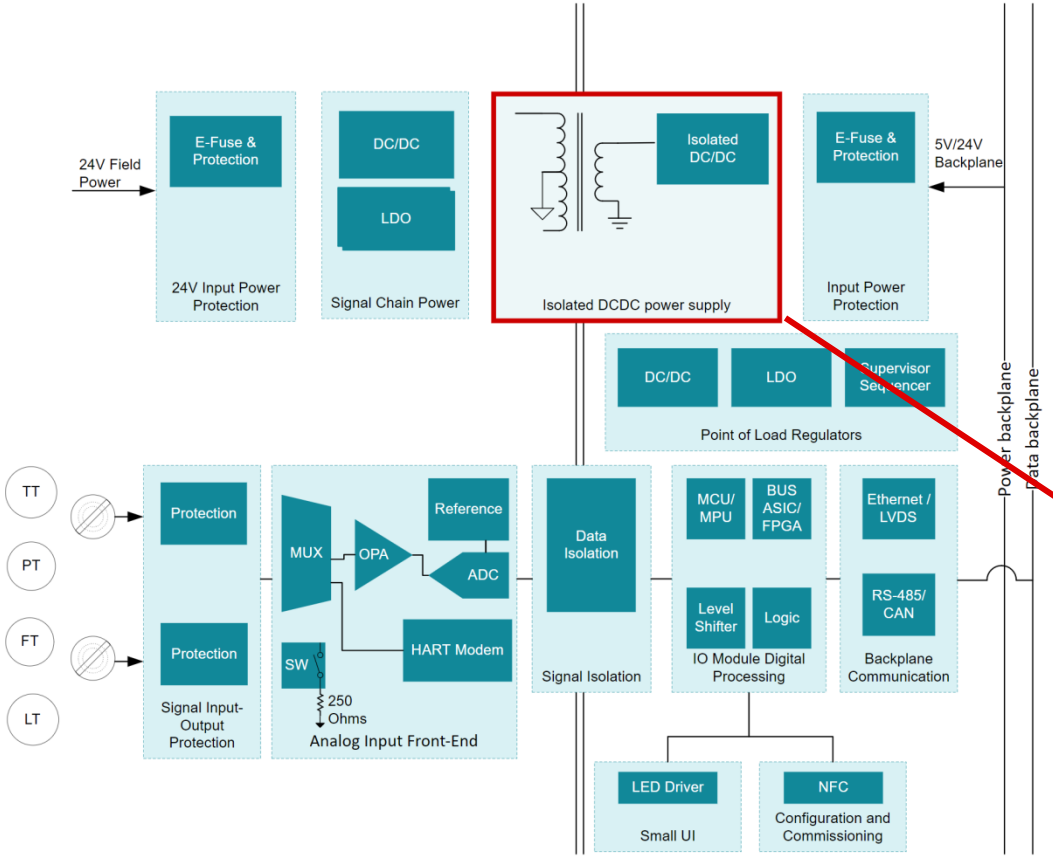
At least four galvanically-isolated bipolar power supplies are needed for a three-phase inverter with typical IGBT gate drive amplitudes of +15V, -8V

On-board charger (OBC) DC/DC – reference diagram

- On-board charger designs vary depending on OEM
- Isolated amplifier bias supply, SiC MOSFET driver bias supply are some examples within OBC



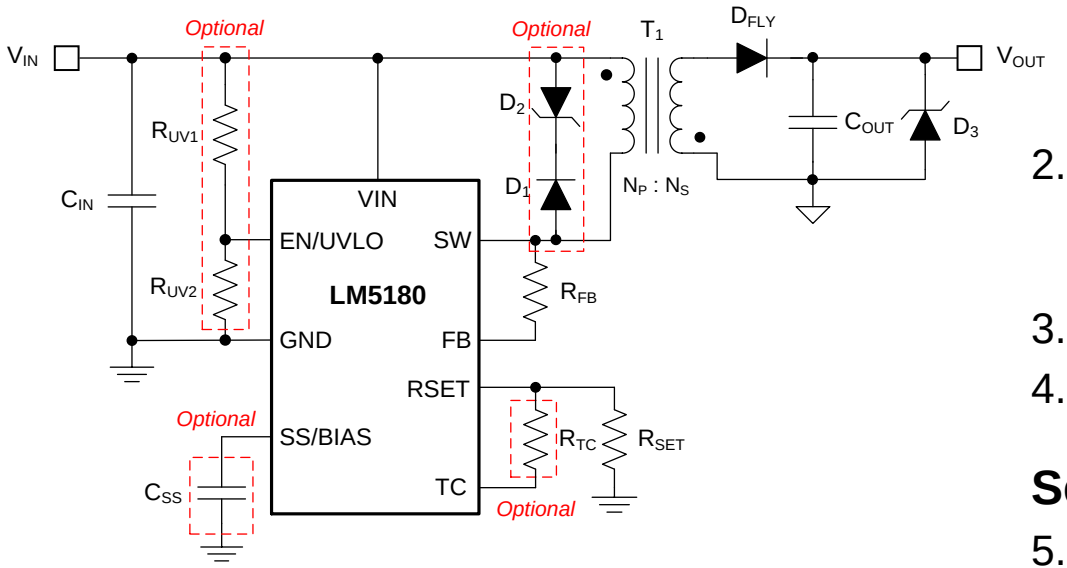
Analog I/O modules – reference diagram



Up to 8 channels may be needed in these modules…requiring 8 isolated bipolar power supplies

PSR flyback circuit design considerations

Component selection



Primary-side components

1. Transformer design
   - Turns ratio
   - Mag inductance
   - Leakage energy
2. Leakage energy management
   - Primary Zener clamp
   - RC snubber (only needed for high L_{LEAK})
3. Input capacitor(s)
4. Feedback, TC and UVLO setting resistors

Secondary-side components

5. Flyback diode
   - RC snubber (only needed for high L_{LEAK})
6. Output capacitor(s)
7. Output Zener clamp

Transformer – turns ratio sets duty cycle range and $P_{OUT(max)}$

Step 1. Select turns ratio (initial estimate), choose D_{MAX} = 50%-60%

$$N_{PS} = \frac{N_P}{N_S} = \frac{D_{MAX}}{1 - D_{MAX}} \cdot \left(\frac{V_{IN(min)}}{V_{OUT} + V_D} \right)$$

D_{MAX} = duty cycle at $V_{IN(min)}$ → set to 50-60%

Step 2. Check $\mathbf{V_{SW(max)}}$ and $\mathbf{V_{D\text{-}RRM}}$

$$V_{SW(max)} = V_{IN(max)} + N_{PS} \cdot V_{OUT} + V_{SW(spike)}$$

$$V_{D\text{-}RRM} = V_{OUT} + \frac{V_{IN(max)}}{N_{PS}} + V_{D(spike)}$$

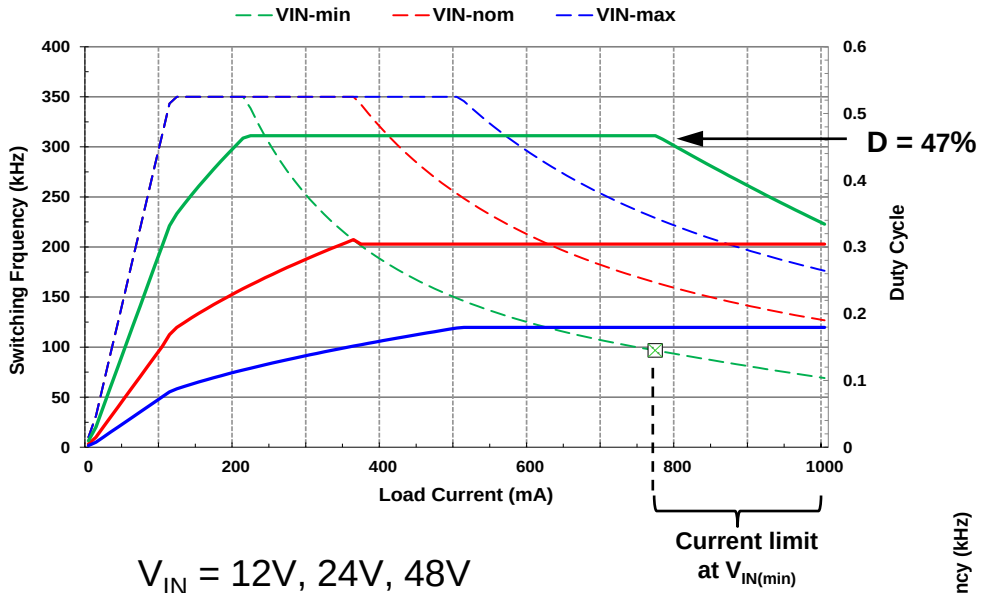
Step 3. Check $\mathbf{P_{OUT(max)}}$ and $\mathbf{F_{SW}}$ at $\mathbf{V_{IN(min)}}$, where $I_{SW\text{-}PK}$ = 1.45A typ.

$$P_{OUT(max)} = \frac{L_{MAG} \cdot I_{SW\text{-}PK}^{\,2}}{2} \cdot F_{SW(BCM)} = \frac{I_{SW\text{-}PK(BCM)}}{2 \cdot \left[\frac{1}{V_{IN}} + \frac{1}{N_{PS} \cdot (V_{OUT} + V_D)} \right]}$$

$$F_{SW(BCM)} = \frac{1}{I_{SW\text{-}PK(BCM)} \cdot L_{MAG} \cdot \left[\frac{1}{V_{IN}} + \frac{1}{N_{PS} \cdot (V_{OUT} + V_D)} \right]}$$

Step 4. Iterate by increasing N_{PS} if P_{OUT} is too low at $V_{IN(min)}$

Transformer – higher turns ratio increases $P_{OUT(max)}$



V_{IN} = 12V, 24V, 48V

V_{OUT} = 5V, I_{OUT} = 1A

N_{PS} = 2 : 1, L_{MAG} = 40µH

X **60V diode**

X **Higher C_{OUT}**

X **Lower $P_{OUT(max)}$**

V_{IN} = 12V, 24V, 48V

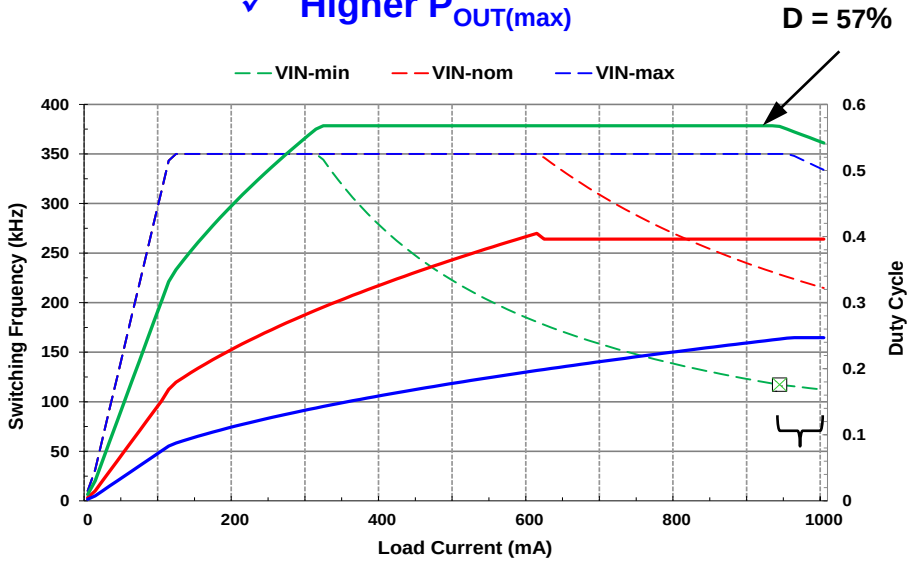
V_{OUT} = 5V, I_{OUT} = 1A

N_{PS} = 3 : 1, L_{MAG} = 40µH

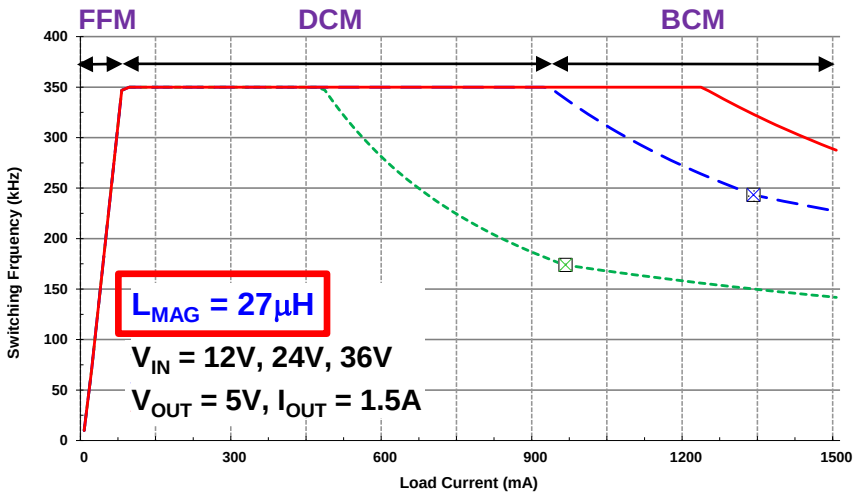
✓ **40V diode**

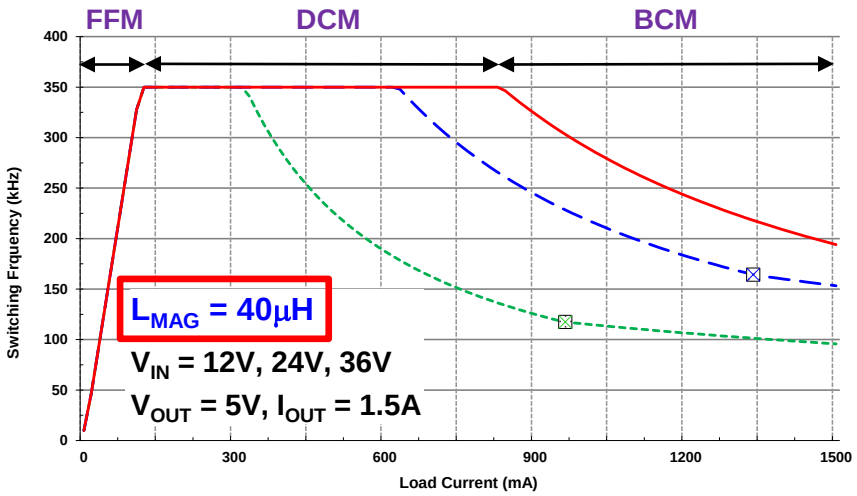
✓ **Lower C_{OUT}**

✓ **Higher $P_{OUT(max)}$**



Transformer – L_{MAG} sets BCM / DCM / FFM mode boundaries





1. Check **SW voltage margin**

$$N_{PS} \le \frac{V_{SW(max)} - V_{IN(max)} - V_{LK\text{-}SPIKE}}{V_{OUT} + V_D}$$

$$V_{LK\text{-}SPIKE} \approx I_{SW\text{-}PK}\sqrt{\frac{L_{LEAK}}{C_{OSS} + C_{TR}}},\ L_{LEAK} \approx 1\%L_{MAG}$$

2. Check **min off-time** constraint at $V_{IN(min)}$

$$L_{MAG} \ge \frac{(V_{OUT} + V_D)\cdot N_{PS}}{I_{SW\text{-}PK(min)}}\cdot T_{OFF(min)}$$

$T_{OFF(min)}$ = minimum switch off-time, 400ns

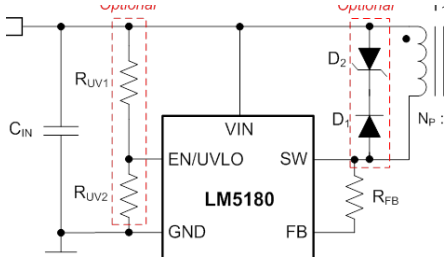
Higher L_{MAG} → Larger range of BCM and FFM, higher leakage inductance, possibly lower efficiency

Leakage energy management

DZ clamp / RC snubber

- Use **Zener clamp** if $\mathbf{V_{IN(max)}}$ is high
  $\Rightarrow$ keep $V_{SW(max)} < V_{SW(rated)} = 100V$
- Use **RC snubber** if leakage ringing duration at $\mathbf{V_{IN(min)}}$ exceeds blanking time of 400ns

$$P_{CLAMP} \square P_{LEAK} = \frac{L_{LEAK} \cdot I_{SW\text{-}PK}^{2}}{2} \cdot F_{SW}$$

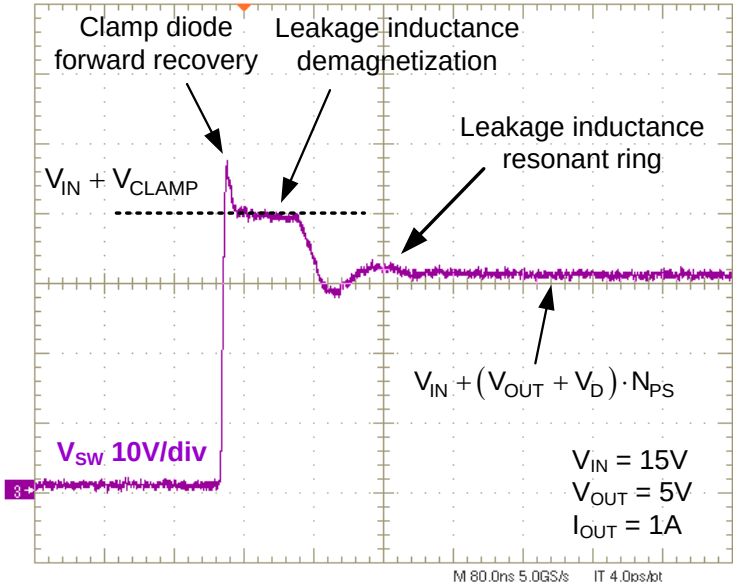


where:

L_{LEAK} = primary-referred leakage inductance (measured with shorted secondary)

$I_{SW\text{-}PK}$ = peak primary (switch) peak current at full load

Worst case = high $I_{SW\text{-}PK}$ current near current limit



$$V_{CLAMP} < V_{SW(rated)} - V_{IN(max)}$$

Target: $\boxed{V_{CLAMP} \approx 1.5 \cdot N_{PS} \cdot (V_{OUT} + V_D)}$

$$V_{SW\text{-}LK\text{-}SPIKE} \approx I_{SW\text{-}PK} \sqrt{\frac{L_{LEAK}}{C_{OSS} + C_{TR}}}$$

Input and output caps

Output capacitor

$$D_2 = \frac{2 \cdot I_{OUT}}{I_{SEC\text{-}PK}}$$

$$C_{OUT} \geq \frac{D_2 \cdot I_{COUT}}{F_{SW} \cdot \Delta V_{OUT}} = \frac{2 \cdot I_{OUT}}{I_{SEC\text{-}PK}} \cdot \frac{\frac{I_{SEC\text{-}PK}}{2} - I_{OUT}}{F_{SW} \cdot \Delta V_{OUT}}$$

$$\boxed{C_{OUT} \geq \frac{2 \cdot I_{OUT} \cdot \left(\frac{I_{SW\text{-}PK}}{2} - \frac{I_{OUT}}{N_{PS}} \right)}{I_{SW\text{-}PK} \cdot F_{SW} \cdot \Delta V_{OUT}}}$$

where:

C_{OUT} = output capacitance (ceramic, negligible ESR)

ΔV_{OUT} = pk-pk ripple voltage spec (typ = 1% Vout)

$I_{SW\text{-}PK}$ = peak primary (switch) current at full load

D_2 = diode conduction duty cycle at full load

$$D_1 = \frac{2 \cdot I_{IN}}{I_{SW\text{-}PK}}$$

Input capacitor

$$\boxed{C_{IN} \geq \frac{D_1 \cdot I_{CIN}}{F_{SW} \cdot \Delta V_{IN}} = \frac{2 \cdot I_{IN} \cdot \left(\frac{I_{SW\text{-}PK}}{2} - I_{IN} \right)}{I_{SW\text{-}PK} \cdot F_{SW} \cdot \Delta V_{IN}}}$$

where:

C_{IN} = input capacitance

ΔV_{IN} = input ripple voltage spec (typ: 5% Vin)

I_{IN} = input current at full load

D_1 = switch conduction duty cycle at full load

Flyback diode and Zener clamp

Flyback diode

$$V_{D\text{-}RRM} \geq \frac{V_{IN\text{-}MAX}}{N_{PS}} + V_{OUT} + V_{D\text{-}LK\text{-}SPIKE}$$

where:

$V_{D\text{-}RRM}$ = diode reverse voltage rating

$V_{LK\text{-}SPIKE}$ = diode voltage spike from leakage inductance ringing with parasitic capacitance

$N_{PS} = N_P/N_S$ = primary-secondary turns ratio

Note:

Schottky leakage current at **HOT** can result in high loss

⇒ use **ultra-fast switching** diode for $V_{D\text{-}RRM}$ > 100V

Output Zener clamp

$$P_{OUT(min)} = \frac{L_{MAG} \cdot I_{PRI(min)}^{2}}{2} \cdot F_{SW(min)}$$

$$I_{OUT(min)} = \frac{P_{OUT(min)}}{V_{OUT}}$$

where:

$I_{PRI(min)}$ = min. peak primary current (= $I_{PRI(max)}/5$)

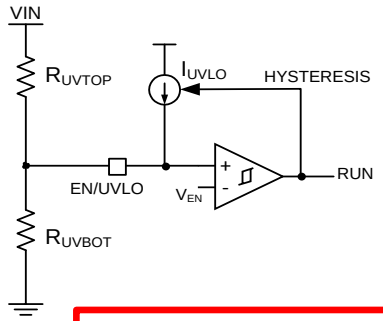
$F_{SW(min)}$ = min switching frequency (= 12kHz)

Choose

$$V_{OUT(clamp)} = 105\text{-}110\%\ V_{OUT(nom)}$$

Adjustable UVLO options

2-resistor UVLO network



EN voltage hysteresis $V_{UV\text{-}HYST}$ = 50mV

EN current hysteresis I_{UVLO} = 5µA

$$R_{UVTOP} = \frac{V_{IN(on)} \cdot \frac{V_{UVLO2}}{V_{UVLO1}} - V_{IN(off)}}{I_{UVLO}} - \frac{V_{IN(on)} \cdot R_{UVADJ}}{V_{UVLO1}}$$

$$R_{UVBOT} = R_{UVTOP} \cdot \frac{V_{UVLO1}}{V_{IN(on)} - V_{UVLO1}}$$

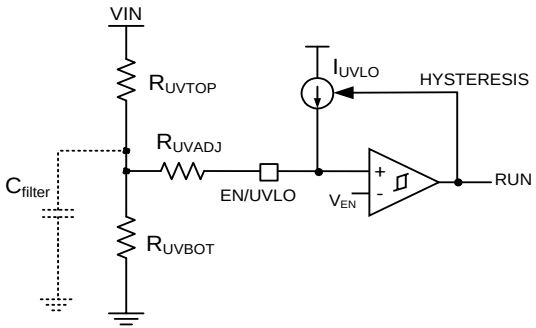
V_{UVLO1} = EN voltage when device turns on

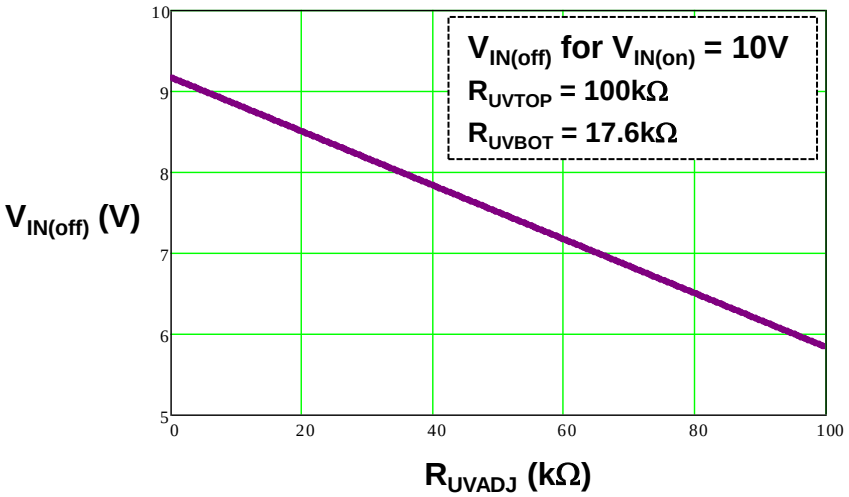
V_{UVLO2} = EN voltage when device turns off

I_{UVLO} = EN current hysteresis

3-resistor UVLO network

(to accommodate the automotive 100kΩ limitation)



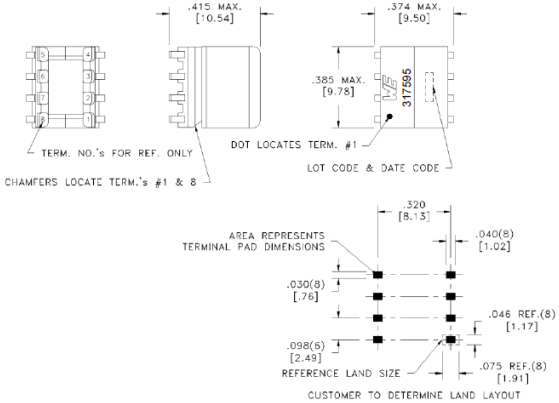


PSR flyback magnetic design considerations

Engaging with the magnetic component vendor

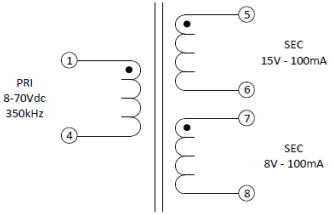
Key Specification	Symbol		Purpose
Turns ratio	N_{PS}	→	Optimize flyback duty cycle range
Switching frequency	F_{SW}	→	Control core loss
Magnetizing inductance	L_{MAG}	→	Set PSR flyback mode boundaries
Saturation current	I_{SAT}	→	Prevent magnetic saturation
Primary and secondary DCRs	R_{PRI}, R_{SEC}	→	Reduce copper loss
Winding arrangement – interleaving, # of layers		→	Minimize R_{AC} and L_{LEAK}
Leakage inductance	L_{LEAK}	→	Reduce power loss & voltage spikes
Interwinding capacitance	$C_{P\text{-}S}$	→	Mitigate common-mode EMI
Hi-pot test limits (dielectric withstand)	$V_{ISO(PRI\text{-}SEC)}$	→	Provide a robust design
Insulation rating – functional / basic / reinforced	IR	→	Comply with safety requirements
Operating temperature range	$T_{AMB} + T_{RISE}$	→	Ensure reliability
Mechanicals – pinout, footprint, height	$L \times W \times H$	→	Minimize size and cost

Flyback transformer spec sheets



ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1-4	@20ºC	0.075 ohms ±10%
D.C. RESISTANCE	5-6	@20ºC	0.570 ohms ±10%
D.C. RESISTANCE	7-8	@20ºC	0.290 ohms ±10%
INDUCTANCE	1-4	10kHz, 100mV, Ls	22.0µH ±10%
SATURATION CURRENT	1-4	20% rolloff from initial	___A
LEAKAGE INDUCTANCE	1-4	tie(5+6, 7+8),100kHz, 100mV, Ls	___µH typ., ___µH max.
DIELECTRIC	1-4	tie(6+7), 1500VAC, 1 second	
DIELECTRIC	5-8	625VAC, 1 second	
TURNS RATIO		(5-6):(7-8)	2:1, ±1%
TURNS RATIO		(5-6):(1-4)	2:1, ±1%



Application of the transformer allows for the leadwires between terminals 6&7 to solder bridge.

Customer to tie terminals 6+7 on PC board.

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

- Functional insulation only

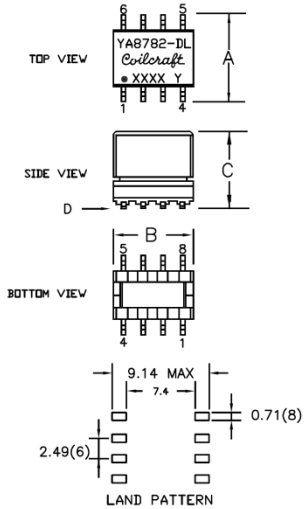
Preliminary

Product contains reportable levels of REACH SVHC component Dechlorane Plus ™ found in AM113 plast

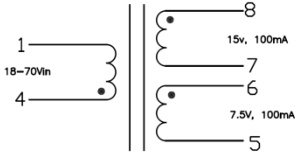
Coilcraft Cary, IL 60013
Coil Design Data

MECHANICAL SPECIFICATIONS

PHYSICAL PARAMETERS (MM)	
DIMENSIONS	MAX
A: WIDTH	9.14
B: LENGTH	10.00
C: HEIGHT	10.54
D: COPLANARITY WITHIN 0.10	



FLYBACK (DCM)
SCHEMATIC



ELECTRICAL SPECIFICATIONS

INDUCTANCE(uH) (CSC)

300 KHZ, 0.1 VRMS, 0 ADC

PINS	MIN	MAX
4-1	19.8	24.2

INDUCTANCE(uH) (100%)

300 KHZ, 0.1 VRMS, 2.0 ADC

PINS	MIN	
4-1	17.6	

HI POT (100%)

(VRMS, to be applied for 1 minute)

VOLTAGE:	FROM PINS	TO PINS
1500	4	8,6
200	8	5
750	ALL PINS	CORE

DC RESISTANCE (OHMS) (100%)

PINS		MAX
4-1		0.108
8-7		0.432
6-5		0.206

LEAKAGE INDUCTANCE (uH) (100%)

300 kHZ, 0.1 Vrms,

TEST PINS	SHORT PINS	MAX
4-1	5,6,7,8	0.192

TURNS RATIO (100%)

Apply .030 Vrms, 100KHZ to pins 4-1

MEASURE PINS:	MIN	MAX
8-7	1.940	2.060
6-5	0.970	1.030

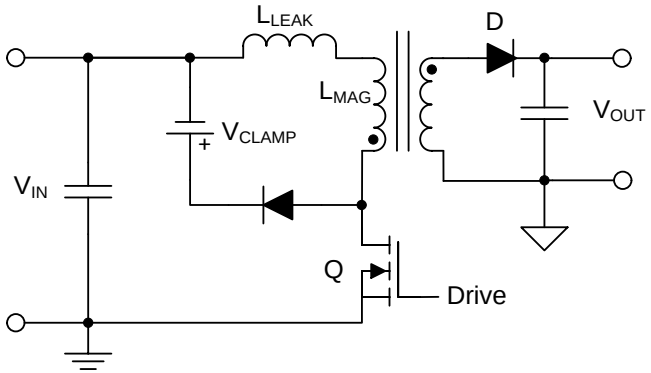
Flyback transformer losses

- **Copper** loss
  - DC resistance – depends on the wire cross-section and length (N, MLT)
  - AC resistance – depends on choice of wire diameter vs. F_{SW} and construction (layer stackup, proximity effects, gap effect)
- **Core** loss
  - Related to core material characteristics, B_{DC}, B_{AC}, F_{SW}
- **External** loss
  - Leakage inductance energy $$P_{LEAK} = \frac{L_{LEAK} \cdot I_{SW\text{-}PK}^{2}}{2} \cdot F_{SW}$$
    - Large percentage of this power dissipated in external clamp circuit or RC snubber
    - Magnetizing energy also dissipated – depends on clamp level and leakage inductance

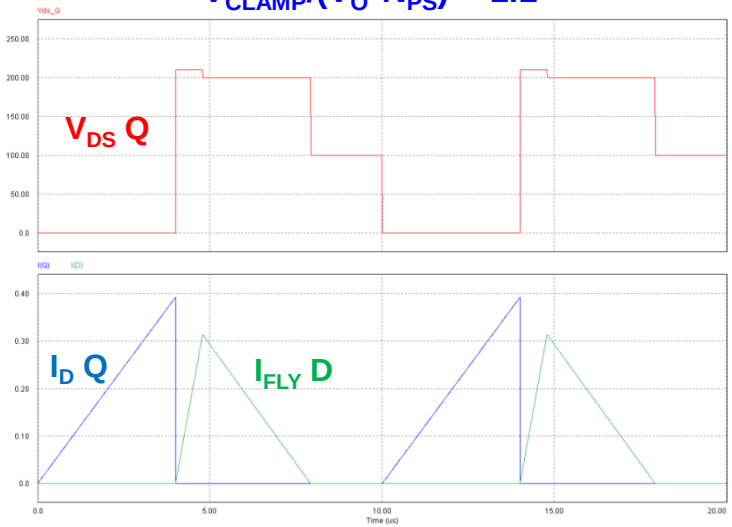
Leakage energy management

MOSFET turn-off

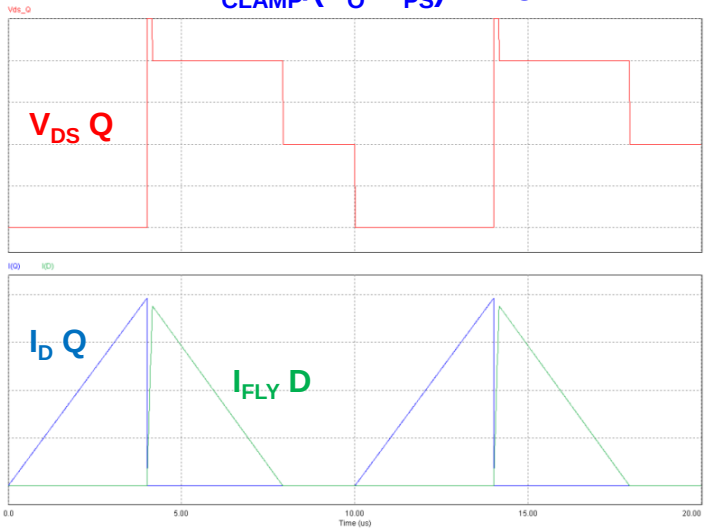
- Leakage energy → clamp until L_{LEAK} current → zero
- Reset time depends on ($V_{CLAMP} – V_{REFLECTED}$) & L_{LEAK} value
- Some magnetizing energy → clamp
- Smaller difference ($V_{CLAMP} – V_{REFLECTED}$)
  - **More magnetizing energy absorbed by clamp, longer reset time**



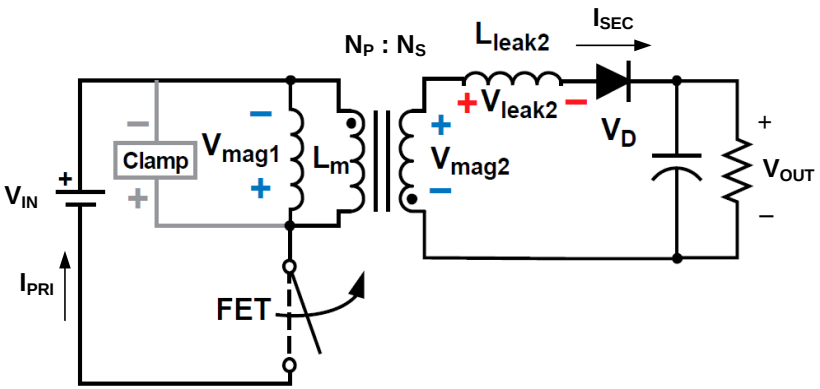
$V_{CLAMP}/(V_O*N_{PS}) = 1.1$

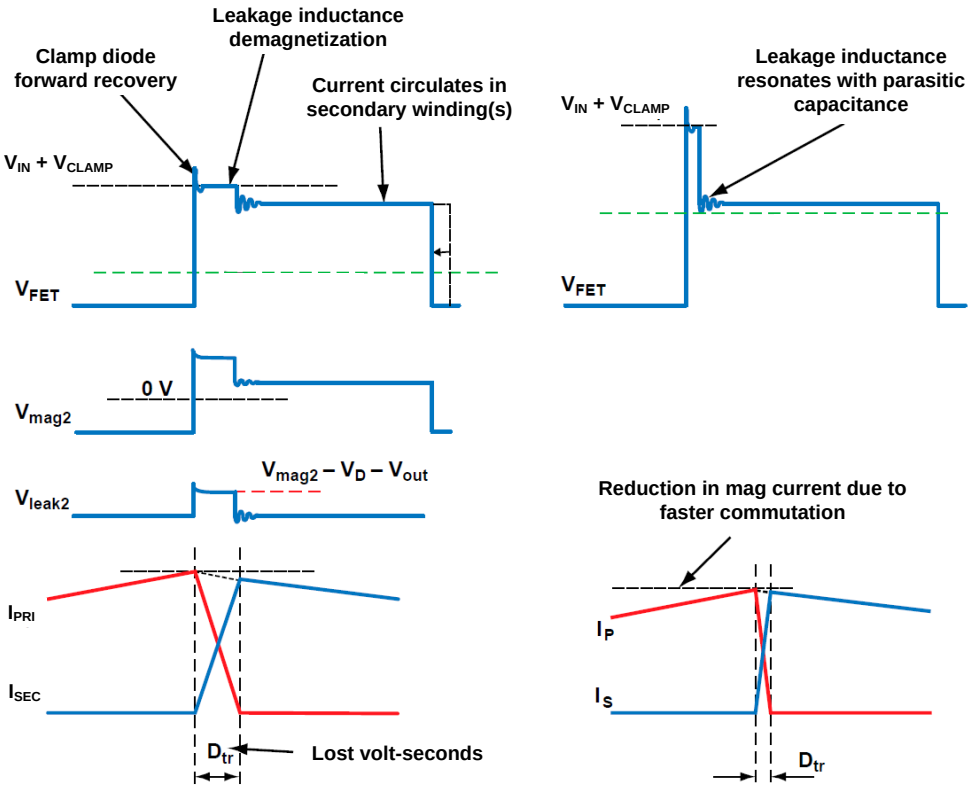


$V_{CLAMP}/(V_O*N_{PS}) = 1.5$



Flyback transformer – impact of leakage inductance





Low clamp voltage

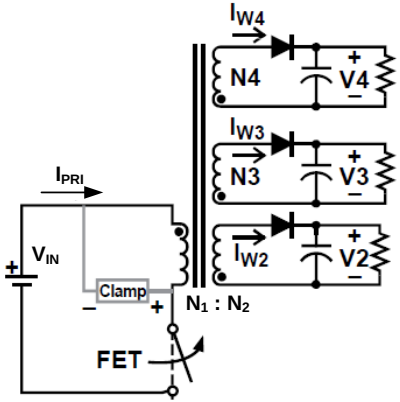
High clamp voltage

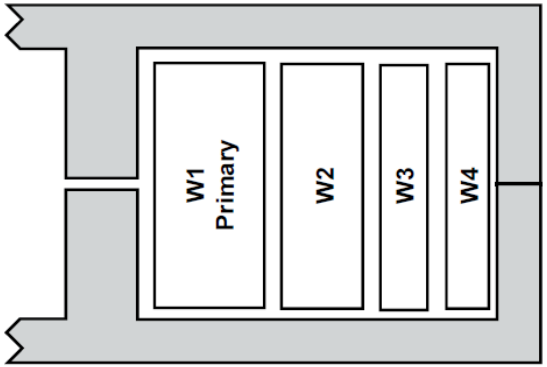
Leakage inductance affects:

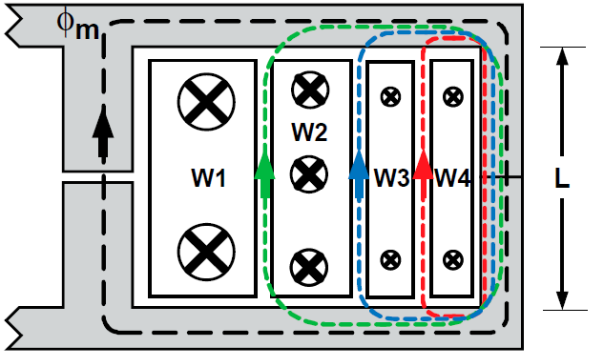
- Conversion efficiency
- Voltage spikes during commutation
  - clamp circuits and snubbers
- Current slew rate & loss of volt-seconds
- H-field radiated EMI
- Cross regulation in multi-output designs

[Ref] "Under the hood of flyback SMPS designs," TI PSDS 2010

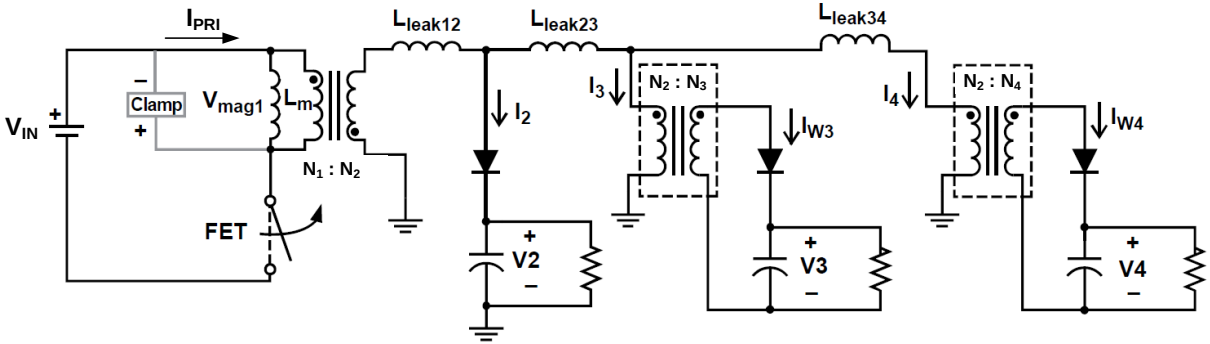
Multi-output transformer – physical / ladder model

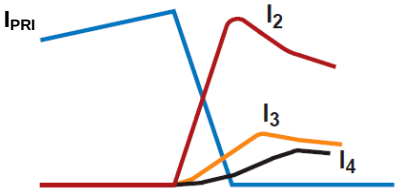






Current in all transformer windings during primary-to-secondary commutation

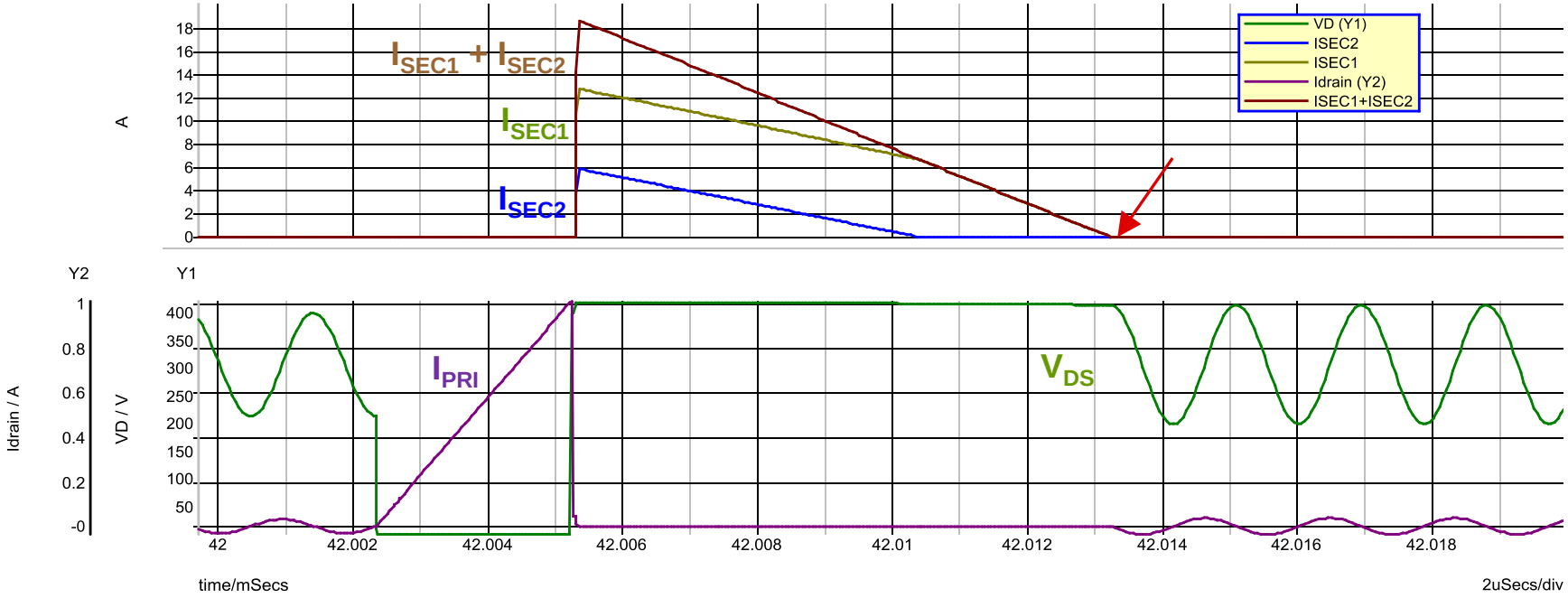




Secondary currents during commutation based on physical/ladder model

[Ref] "Under the hood of flyback SMPS designs," TI PSDS 2010

Dual outputs – distribution of secondary currents



Notes:

- Normalized secondary currents add up to the expected **triangular magnetizing current waveform**
- Secondary winding with the **largest conduction time** dictates regulation (I_{SEC1} in this example)

Flyback transformer design – impact on efficiency & x-reg

1. Guidelines to **optimize efficiency**
   - Choose the transformer **turns ratio** for best efficiency and duty cycle range
   - Minimize **leakage inductance** from primary to main (high-current) secondary
     - Interleave primary around secondary (or vice versa if $N_P < N_S$)
     - Reduces voltage spikes and power dissipation
     - Locate highest power secondary closest to primary (multi-output designs)
   - Minimize transformer high-frequency **conduction loss**
     - Use bifilar or multifilar wires when necessary to reduce AC resistance
     - Interleave primary and secondary windings
     - Select core shape for minimum number of layers (wide bobbin width)

2. Guidelines to **optimize cross regulation**
   - Minimize **leakage inductance** *between secondary windings* as it impacts cross regulation and secondary current wave shapes
     - Wind two highest power secondaries **bifilar** for best coupling
     - Consider **DC or AC stacking** for same polarity outputs that share common GND

Agenda

Isolated converters

- Isolated topologies overview
- PSR flyback topology – features and benefits, end equipment serviced

PSR flyback converter

- Operating modes – BCM, DCM, FFM
- Circuit design considerations – C_{IN}, C_{OUT}, D_F, V_{SW} clamp, UVLO, SS, TC, FB
- Magnetic design considerations – turns ratio, L_{MAG}, L_{LEAK}, ladder model
- Cross regulation in dual-output designs – secondary current distribution

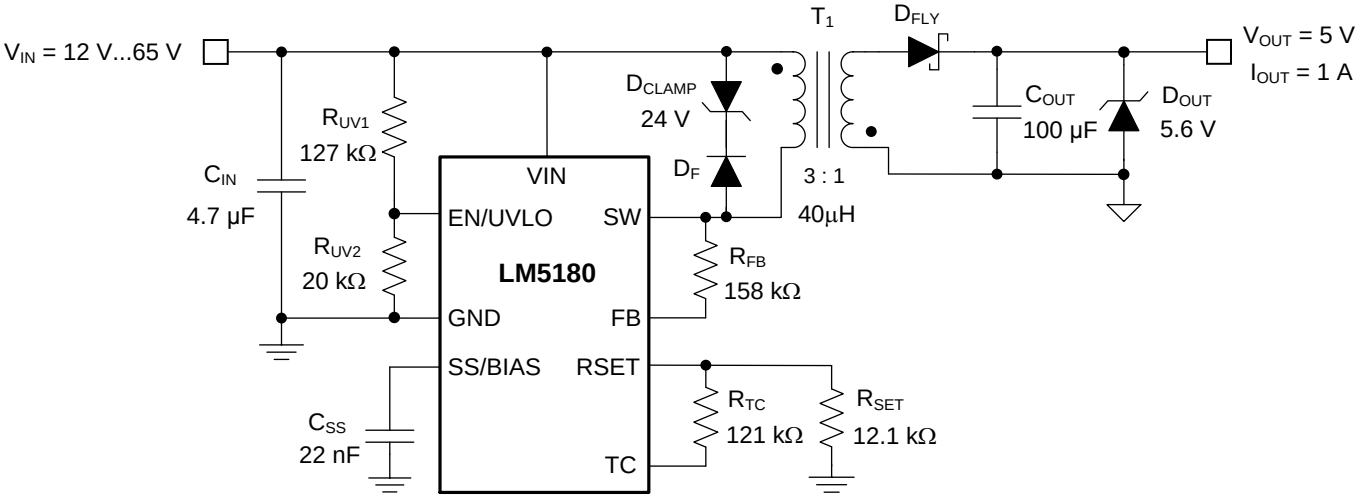
PSR flyback implementation

- **Design examples and lab results – efficiency, regulation, waveforms**
- **PCB layout for single and dual outputs**
- **Common-mode EMI mitigation**

Positioning PSR flyback converters

- Choosing between PSR flyback, Fly-Buck and push-pull topologies
- Competitive analysis and spec comparison

Design example 1: 5V @ 1A single output



Design parameter	Target spec
Input voltage range, $V_{IN(min)}$–$V_{IN(max)}$	12V–65V
Output voltage, V_{OUT}	5V
Maximum load current, $I_{OUT(max)}$	1A
Input UVLO thresholds, $V_{IN(on)}$, $V_{IN(off)}$	11V, 10V

LM5180 quickstart tool: 5V single output

WIDE VIN DC/DC Power Solutions
Reliable Power for Demanding Systems

LM5180 PSR Flyback Converter Design Tool

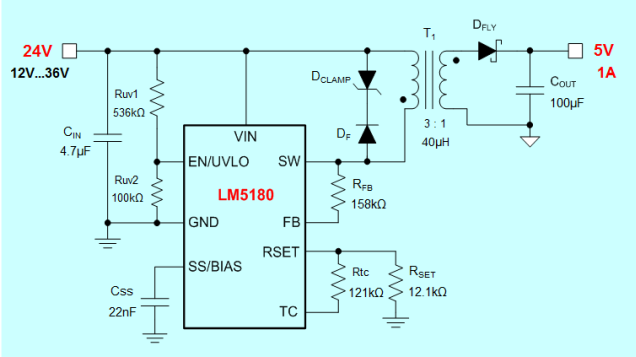
About | = Input Box | Terms Of Use

Step 1: Operating Specifications

Input Voltage – Min, $V_{IN(min)}$	12	V
Input Voltage – Nom, $V_{IN(nom)}$	24	V
Input Voltage – Max, $V_{IN(max)}$	36	V
Single Output or Dual Outputs	SINGLE	
Output Voltage, VOUT	5	V
Rated Output Current, IOUT	1	A

Step 2: Flyback Transformer

Recommended Magnetizing Inductance	40	µH
Magnetizing Inductance, L_{MAG}	40	µH
Primary Winding DCR	80	mΩ
Secondary Winding DCR	20	mΩ
Pri-Sec Leakage Inductance	500	nH
Transformer Turns Ratio, Pri : Sec	3 : 1	
Diode Max Rev Voltage (Spike Not Included)	17.00	V
Duty Cycle at $V_{IN(min)}$	57.2	%
Max Output Power at $V_{IN(min)}$	4.7	W



Step 3: Input & Output Capacitors

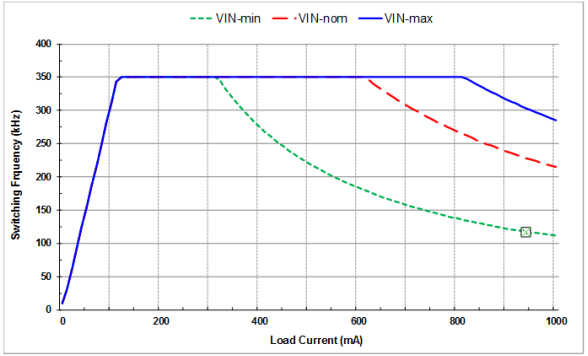
Minimum Input Capacitance	2.2	µF
Input Capacitance, C_{IN}	4.7	µF
Input Capacitor ESR	10	mΩ
Resulting Input Voltage Ripple	142	mV_{pk-pk}
Minimum Output Capacitance	36.9	µF
Output Capacitance, C_{OUT}	100	µF
Output Capacitor ESR	3	mΩ
Resulting Output Voltage Ripple	21	mV_{pk-pk}

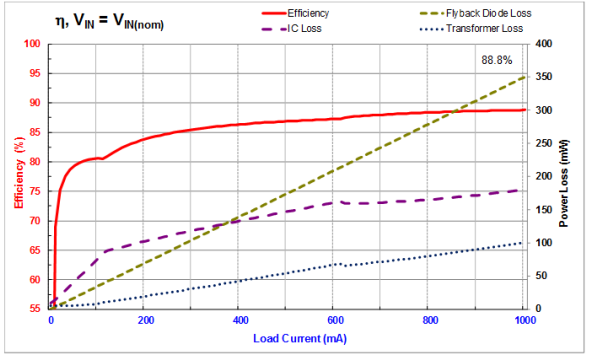
Step 4: Feedback, Soft-start, TC, UVLO

Recommended Feedback Resistor	157.5	kΩ
Selected Feedback Resistor, R_{FB}	158	kΩ
Soft-Start Configuration	Adjustable	
Soft-Start Time	5	ms
Soft-Start Capacitance, C_{SS}	22	nF
VOUT Thermal Compensation	YES	
Diode Voltage Drop Thermal Coefficient	-1.3	mV/°C
Thermal Compensation Resistor, R_{TC}	121	kΩ
Input UVLO Configuration	Adjustable	
Input UVLO Turn-On Threshold	9.5	V
Input UVLO Turn-Off Threshold	6.5	V
Upper UVLO Resistor, R_{UV1}	536	kΩ
Lower UVLO Resistor, R_{UV2}	100	kΩ

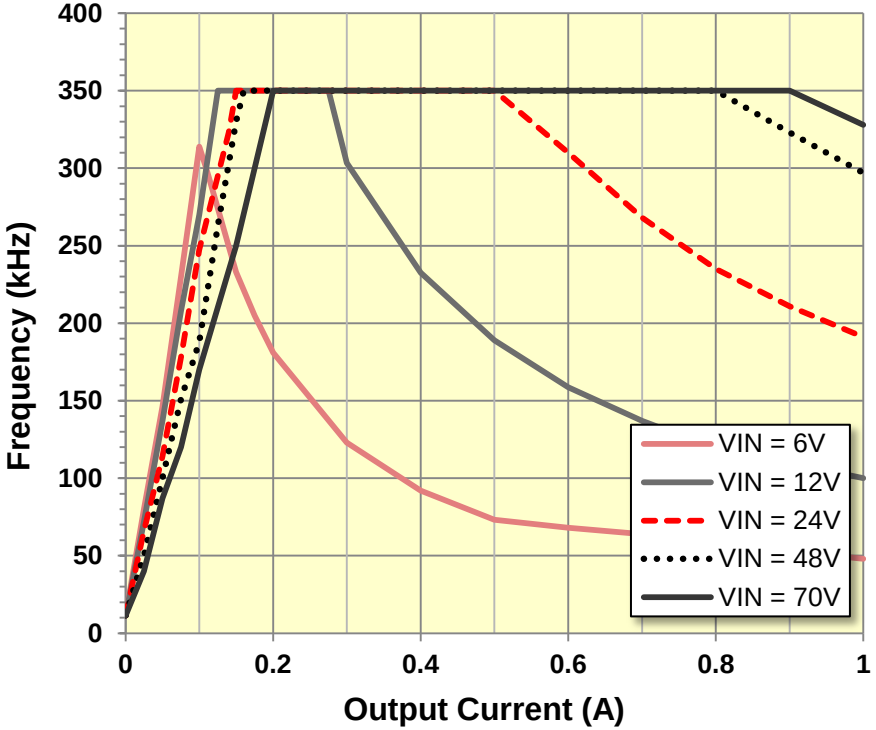
Step 5: Power Losses & Thermals

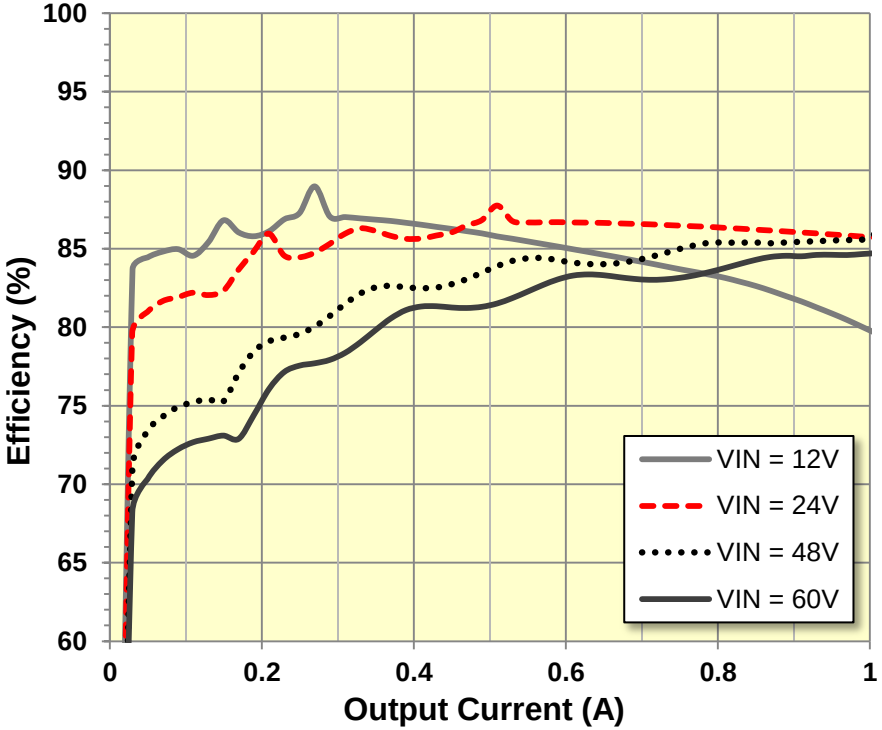
Flyback Diode Voltage Drop, $V_{D(no-load)}$	0.25	V
Flyback Diode Voltage Drop, $V_{D(full-load)}$	0.35	V
Estimated Thermal Impedance, ϑ_{JA}	60	°C/W
Ambient Temperature, T_A	85	°C
LM5180 Power Dissipation at Full Load, P_D	180	mW
LM5180 Junction Temperature at Full Load, T_J	96	°C



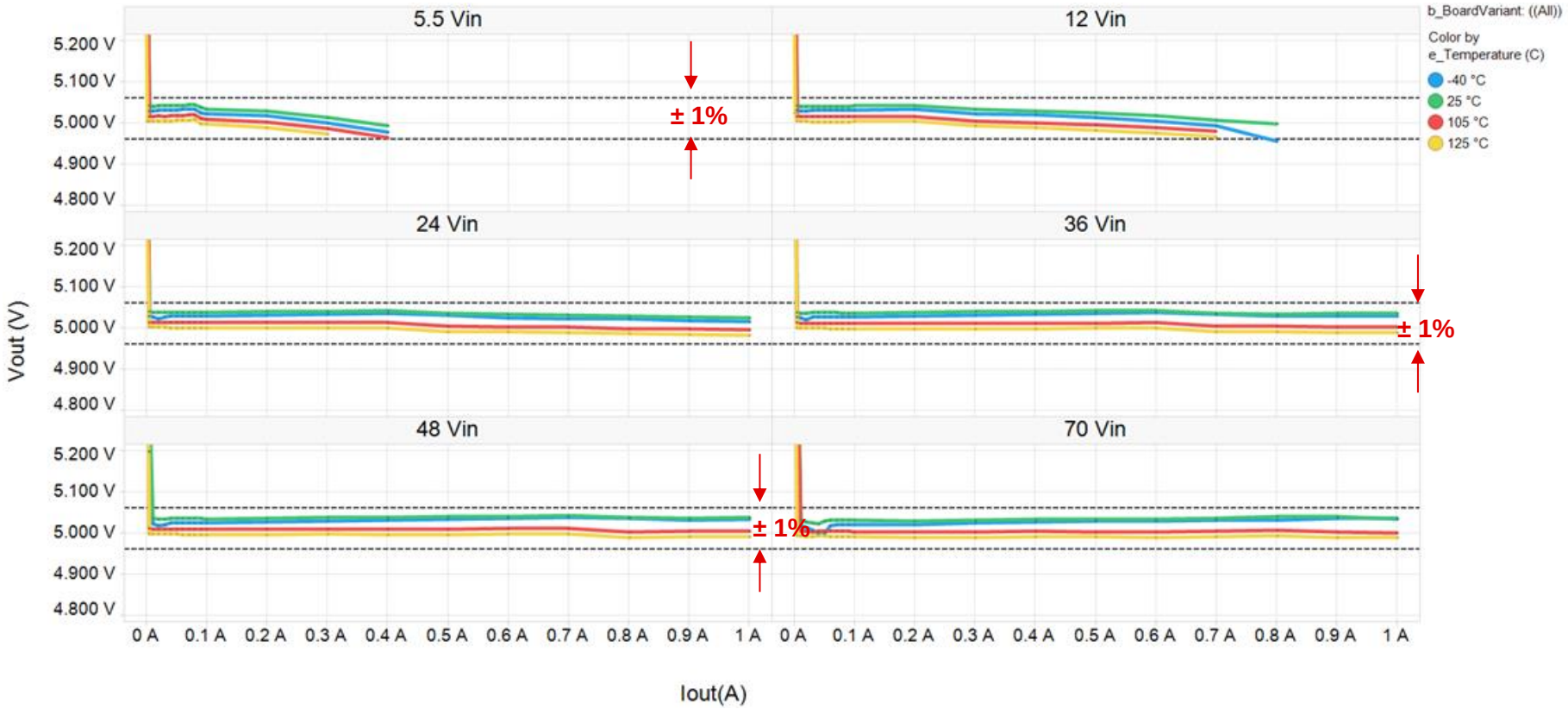


F_{SW} and efficiency

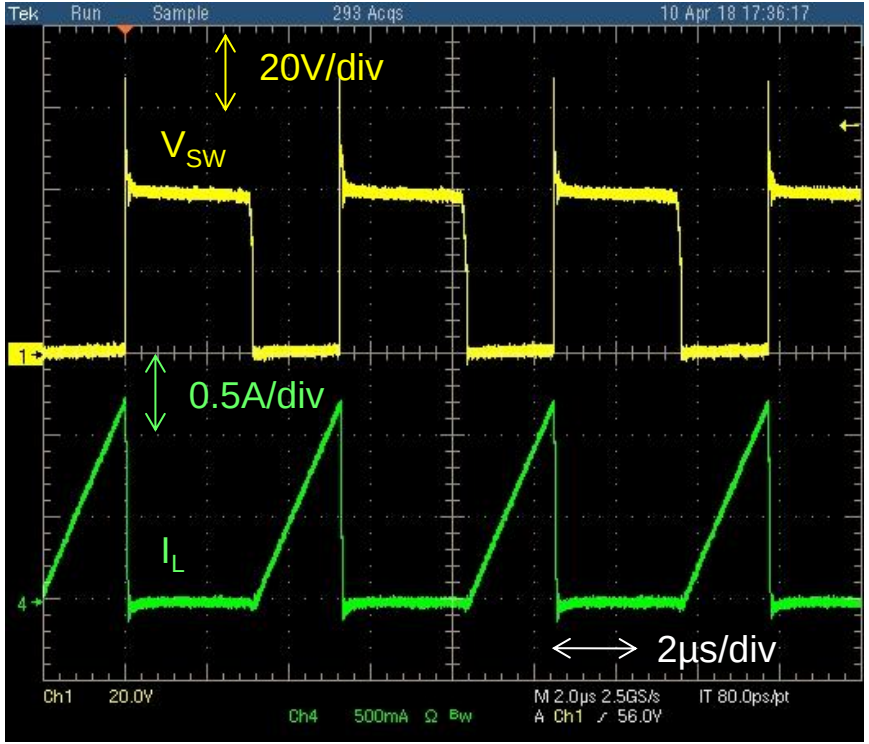


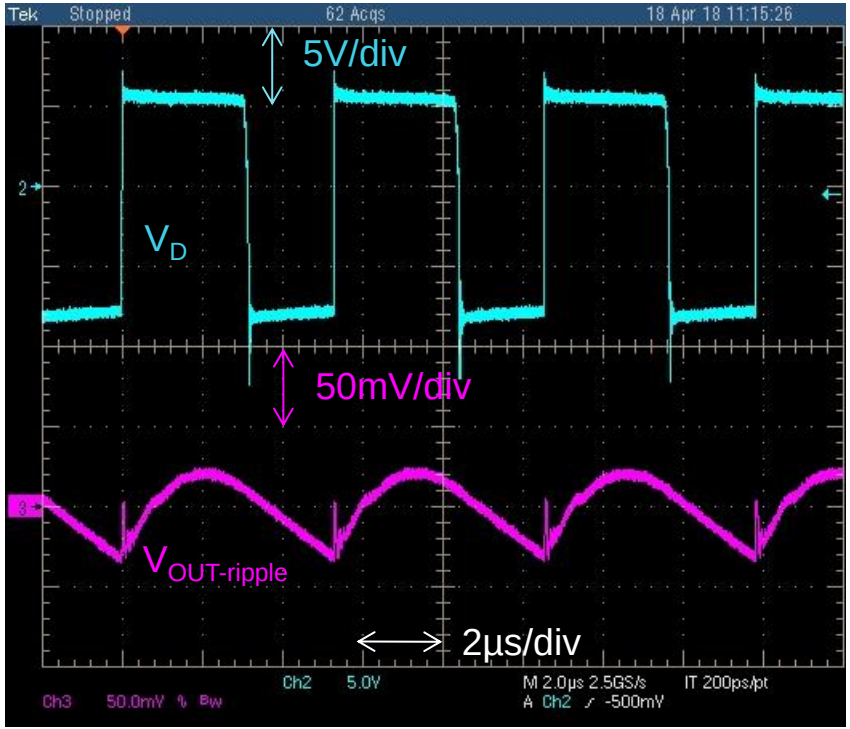


Load regulation vs. I_{OUT}, V_{IN} & T_A



Converter waveforms, V_{IN} = 24V, 1A load

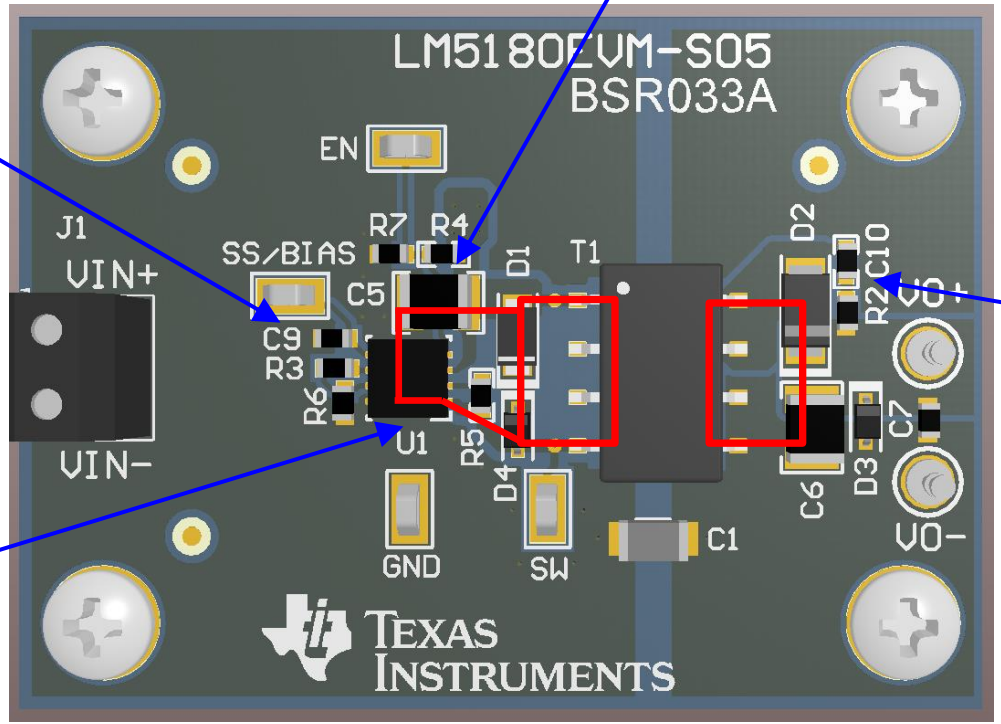




Layout example – single output

Locate C_{IN} close to VIN and GND pins

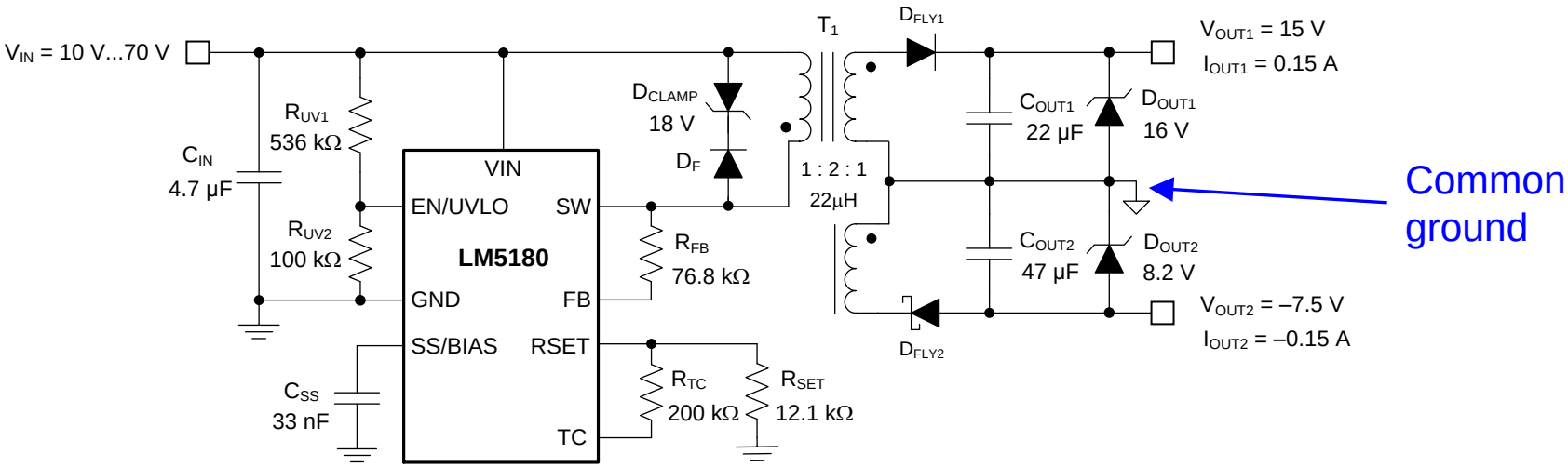
Place REF, TC and FB resistors near IC



Keep diode and output cap close to secondary winding, ***minimize area of switching loops***

Keep SW trace short and DZ clamp close to primary winding

Design example 2: 15V & -7.5V dual outputs @ 150mA



Design parameter	Target spec
Input voltage range, $V_{IN(min)}$–$V_{IN(max)}$	10V–70V
Output voltages, V_{OUT1}, V_{OUT2}	15V, –7.5V
Maximum load currents, $I_{OUT1(max)}$, $I_{OUT2(max)}$	150mA
Input UVLO thresholds, $V_{IN(on)}$, $V_{IN(off)}$	9.5V, 6.5V

$$\frac{N_{S1}}{N_{S2}} = \frac{V_{OUT1} + V_{D1}}{V_{OUT2} + V_{D2}} = \frac{15\ V + 0.7\ V}{7.5\ V + 0.35\ V} = 2$$

LM5180 quickstart tool: 15V & –7.5V dual outputs at 150mA

WIDEV_{IN} DC/DC Power Solutions
Reliable Power for Demanding Systems

LM5180 PSR Flyback Converter Design Tool

About = Input Box Terms Of Use

Step 1: Operating Specifications

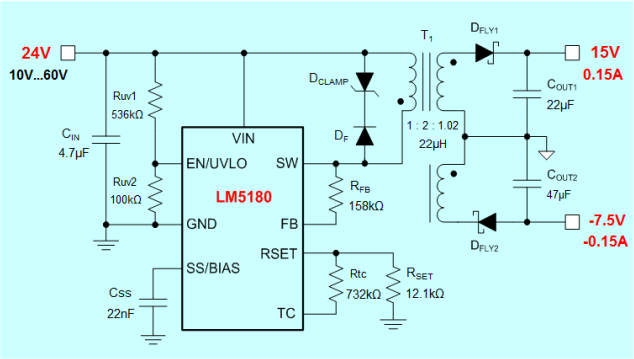
Input Voltage – Min, $V_{IN(min)}$	10	V
Input Voltage – Nom, $V_{IN(nom)}$	24	V
Input Voltage – Max, $V_{IN(max)}$	60	V
Single Output or Dual Outputs	DUAL	
Output Voltage, VOUT1	15	V
Rated Output Current, IOUT1	0.15	A
Output Voltage, VOUT2	-7.5	V
Rated Output Current, IOUT2	0.15	A

Step 2: Flyback Transformer

Recommended Magnetizing Inductance	22	µH
Magnetizing Inductance, L_{MAG}	22	µH
Primary Winding DCR	100	mΩ
Secondary Winding #1 DCR	200	mΩ
Secondary Winding #2 DCR	200	mΩ
Turns Ratio, PRI : SEC1	1 : 2	
Turns Ratio, SEC1 : SEC2	0.51	
Duty Cycle at $V_{IN(min)}$	43.4	%
Max Output Power at $V_{IN(min)}$	3.0	W

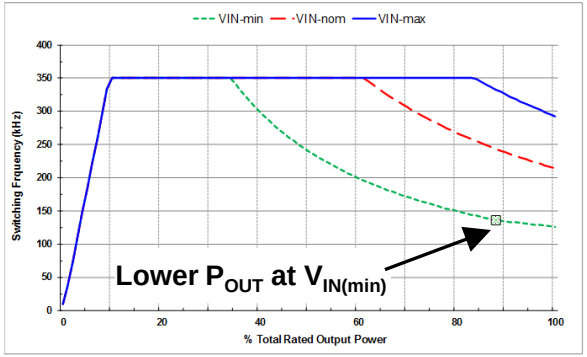
Step 3: Input & Output Capacitors

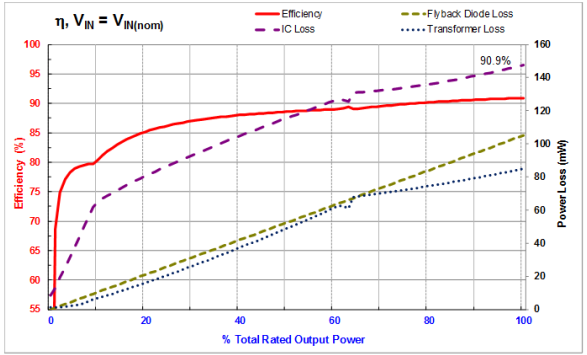
Minimum Input Capacitance	2.2	µF
Input Capacitance, C_{IN}	4.7	µF
Input Capacitor ESR	10	mΩ
Resulting Input Voltage Ripple	87	mV_{pk-pk}
Minimum Output Capacitance, Output #1	1.1	µF
Output Capacitance, C_{OUT}	22	µF
Output Capacitor ESR	3	mΩ
Resulting Output Voltage Ripple, Output #1	32	mV_{pk-pk}
Minimum Output Capacitance, Output #2	2.3	µF
Output Capacitance, C_{OUT2}	47	µF
Output Capacitor ESR	3	mΩ
Resulting Output Voltage Ripple, Output #2	15	mV_{pk-pk}



Step 4: Feedback, Soft-start, TC, UVLO

Recommended Feedback Resistor	76.3	kΩ
Selected Feedback Resistor, R_{FB}	158	kΩ
Soft-Start Configuration	Adjustable	
Soft-Start Time	5	ms
Soft-Start Capacitance, C_{SS}	22	nF
VOUT Thermal Compensation	YES	
Diode Voltage Drop Thermal Coefficient	-1.3	mV/°C
Thermal Compensation Resistor, R_{TC}	732	kΩ
Input UVLO Configuration	Adjustable	
Input UVLO Turn-On Threshold	9.5	V
Input UVLO Turn-Off Threshold	6.5	V
Upper UVLO Resistor, R_{UV1}	536	kΩ
Lower UVLO Resistor, R_{UV2}	100	kΩ

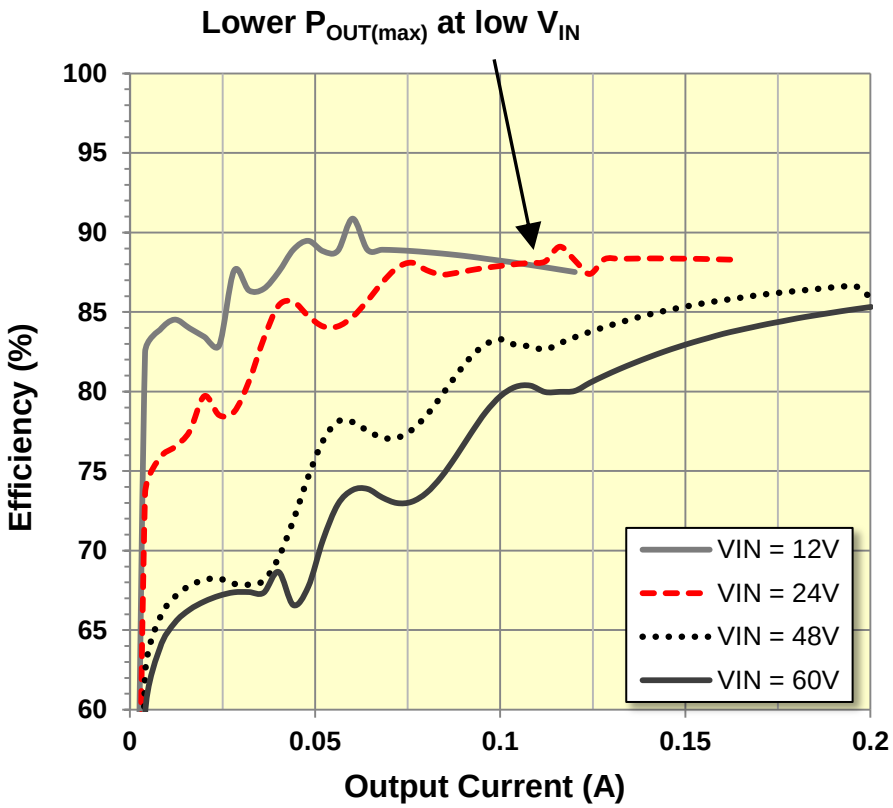


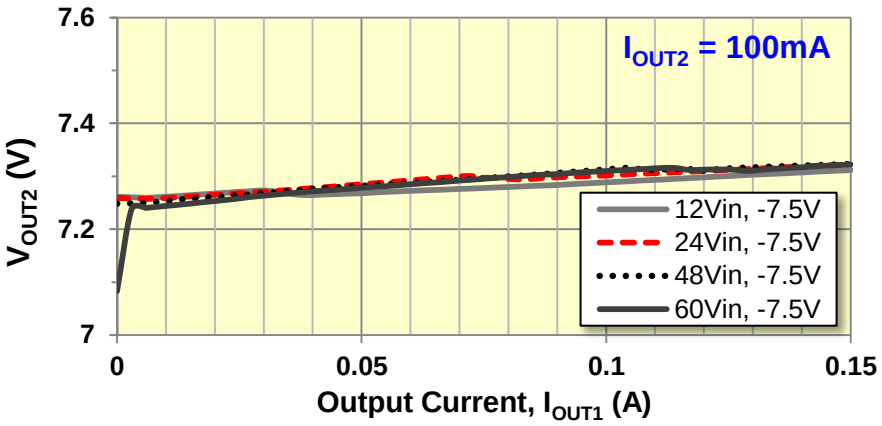


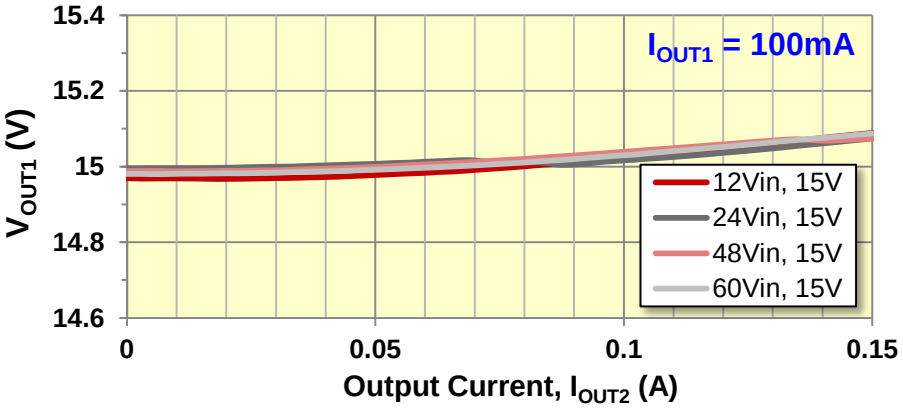
Step 5: Power Losses & Thermals

Flyback Diode Voltage Drop, $V_{D(no-load)}$	0.25	V
Flyback Diode Voltage Drop, $V_{D(full-load)}$	0.35	V
Estimated Thermal Impedance, ϑ_{JA}	60	°C/W
Ambient Temperature, T_A	85	°C
LM5180 Power Dissipation at Full Load, P_D	148	mW
LM5180 Junction Temperature at Full Load, T_J	94	°C

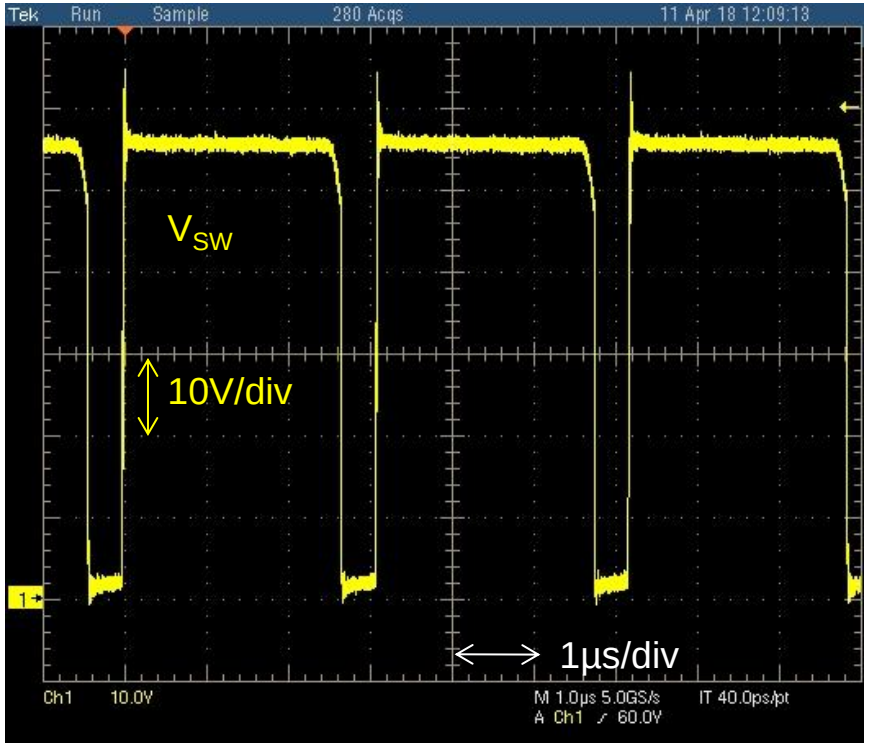
Efficiency, cross regulation

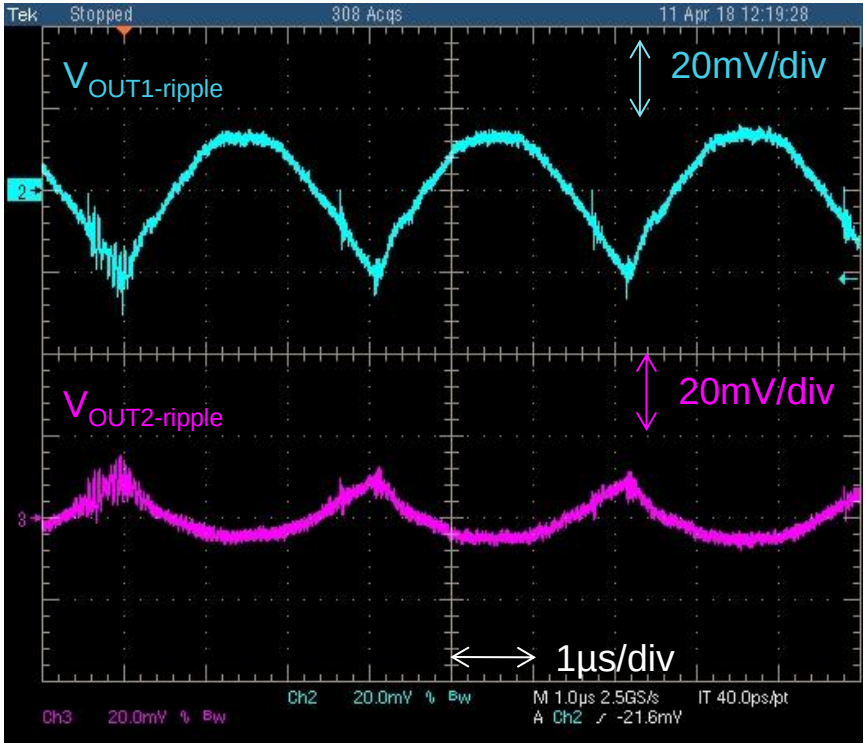






Converter waveforms, V_{IN} = 48V





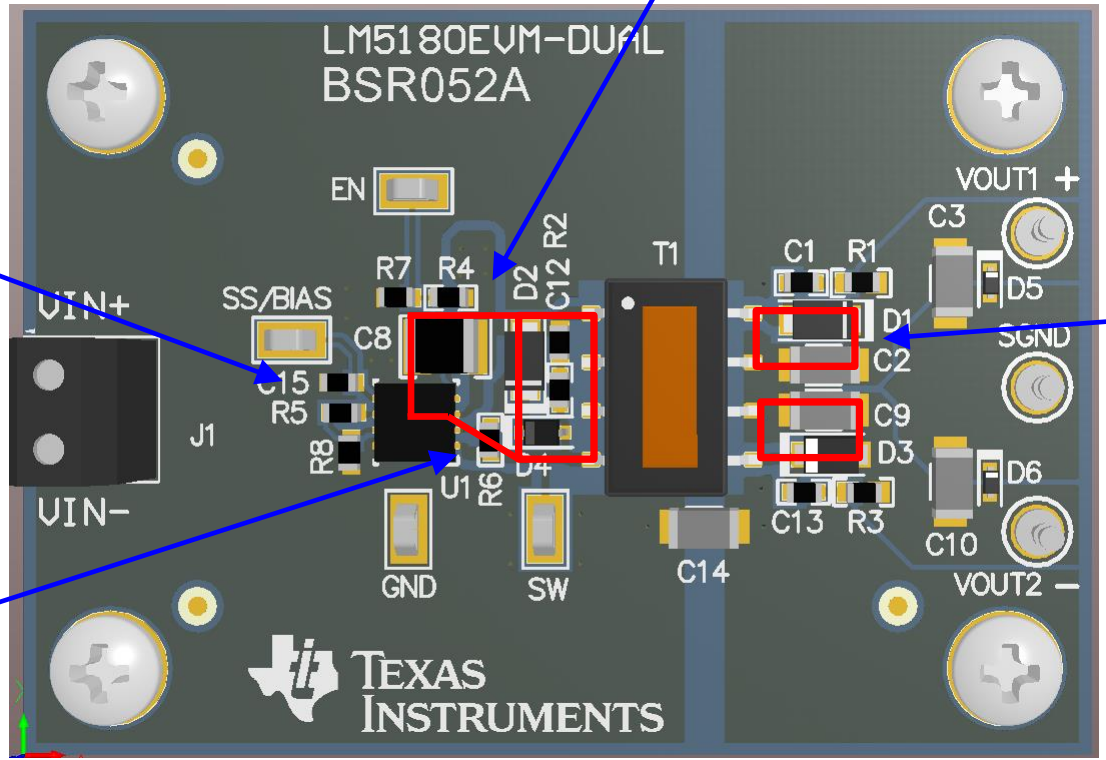
Layout example – dual output

Locate C_{IN} close to VIN and GND pins

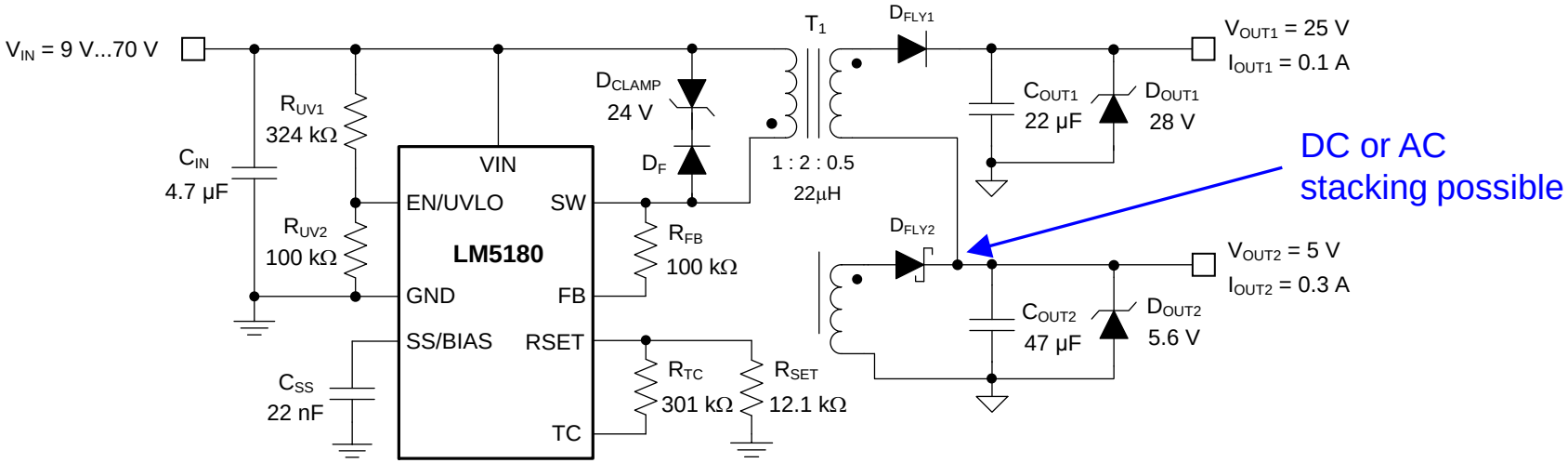
Place REF, TC and FB resistors near IC

Keep diodes and output caps close to secondary windings, ***minimize area of switching loops***

Keep SW trace short and DZ clamp and/or RC snubber close to primary winding



Design example 3: 25V/5V @ 0.1A/0.3A stacked dual outputs



Design parameter	Target spec
Input voltage range, $V_{IN(min)}$–$V_{IN(max)}$	9V–70V
Output voltages, V_{OUT1}, V_{OUT2}	25V (20V + 5V), 5V
Maximum load currents, $I_{OUT1(max)}$, $I_{OUT2(max)}$	50mA, 300mA
Input UVLO thresholds, $V_{IN(on)}$, $V_{IN(off)}$	6.35V, 4.5V

$$\frac{N_{S1}}{N_{S2}} = \frac{V_{OUT1} + V_{D1}}{V_{OUT2} + V_{D2}} = \frac{20\ V + 0.7\ V}{5\ V + 0.4\ V} = 3.8$$

LM5180 quickstart tool: 25V & 5V stacked dual outputs

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LM5180 PSR Flyback Converter Design Tool

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Step 1: Operating Specifications

Input Voltage – Min, $V_{IN(min)}$	9 V
Input Voltage – Nom, $V_{IN(nom)}$	18 V
Input Voltage – Max, $V_{IN(max)}$	60 V
Single Output or Dual Outputs	DUAL
Output Voltage, VOUT1	20 V
Rated Output Current, IOUT1	0.1 A
Output Voltage, VOUT2	5 V
Rated Output Current, IOUT2	0.3 A

Step 2: Flyback Transformer

Recommended Magnetizing Inductanc	22 µH
Magnetizing Inductance, L_{MA}	22 µH
Primary Winding DC	100 mΩ
Secondary Winding #1 DC	200 mΩ
Secondary Winding #2 DC	100 mΩ
Turns Ratio, PRI : SEC	1 : 2
Turns Ratio, SEC1 : SEC	0.26
Duty Cycle at $V_{IN(m}$	53.1 %
Max Output Power at $V_{IN(m}$	3.5 W

Step 3: Input & Output Capacitors

Minimum Input Capacitance	2.2 µF
Input Capacitance, C_{IN}	4.7 µF
Input Capacitor ESR	10 mΩ
Resulting Input Voltage Ripple	66 mV_{pk-pk}
Minimum Output Capacitance, Output #1	1.0 µF
Output Capacitance, C_{OUT}	22 µF
Output Capacitor ESR	3 mΩ
Resulting Output Voltage Ripple, Output #1	17 mV_{pk-pk}

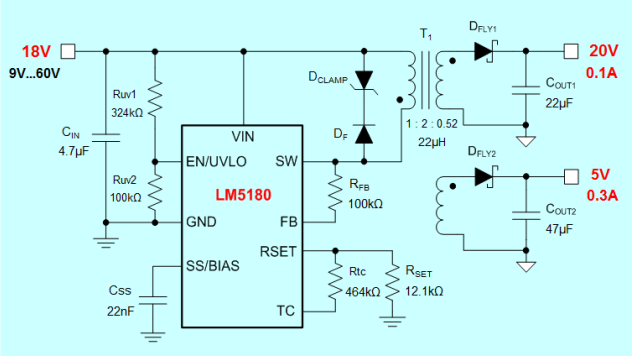
Minimum Output Capacitance, Output #2	7.9 µF
Output Capacitance, C_{OUT2}	47 µF
Output Capacitor ESR	3 mΩ
Resulting Output Voltage Ripple, Output #2	24 mV_{pk-pk}

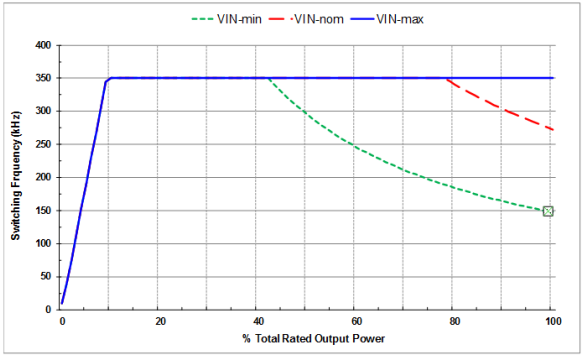
Step 4: Feedback, Soft-start, TC, UVLO

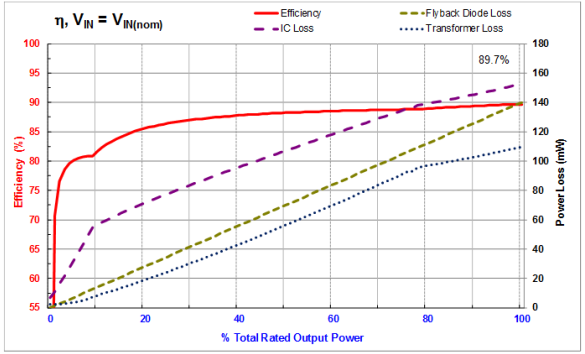
Recommended Feedback Resistor	101.3 kΩ
Selected Feedback Resistor, R_{FB}	100 kΩ
Soft-Start Configuration	Adjustable
Soft-Start Time	5 ms
Soft-Start Capacitance, C_{SS}	22 nF
VOUT Thermal Compensation	YES
Diode Voltage Drop Thermal Coefficient	-1.3 mV/°C
Thermal Compensation Resistor, R_{TC}	464 kΩ
Input UVLO Configuration	Adjustable
Input UVLO Turn-On Threshold	6.35 V
Input UVLO Turn-Off Threshold	4.5 V
Upper UVLO Resistor, R_{UV1}	324 kΩ
Lower UVLO Resistor, R_{UV2}	100 kΩ

Step 5: Power Losses & Thermals

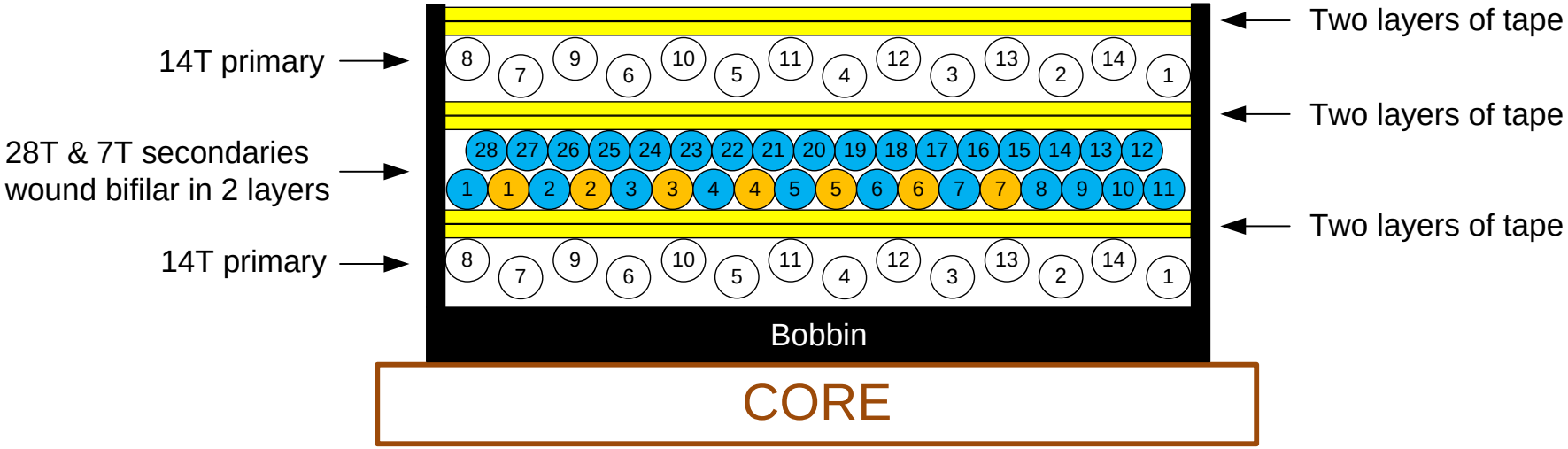
Flyback Diode Voltage Drop, $V_{D(no-load)}$	0.25 V
Flyback Diode Voltage Drop, $V_{D(full-load)}$	0.35 V
Estimated Thermal Impedance, ϑ_{JA}	60 °C/W
Ambient Temperature, T_A	85 °C
LM5180 Power Dissipation at Full Load, P_D	153 mW
LM5180 Junction Temperature at Full Load, T_J	94 °C







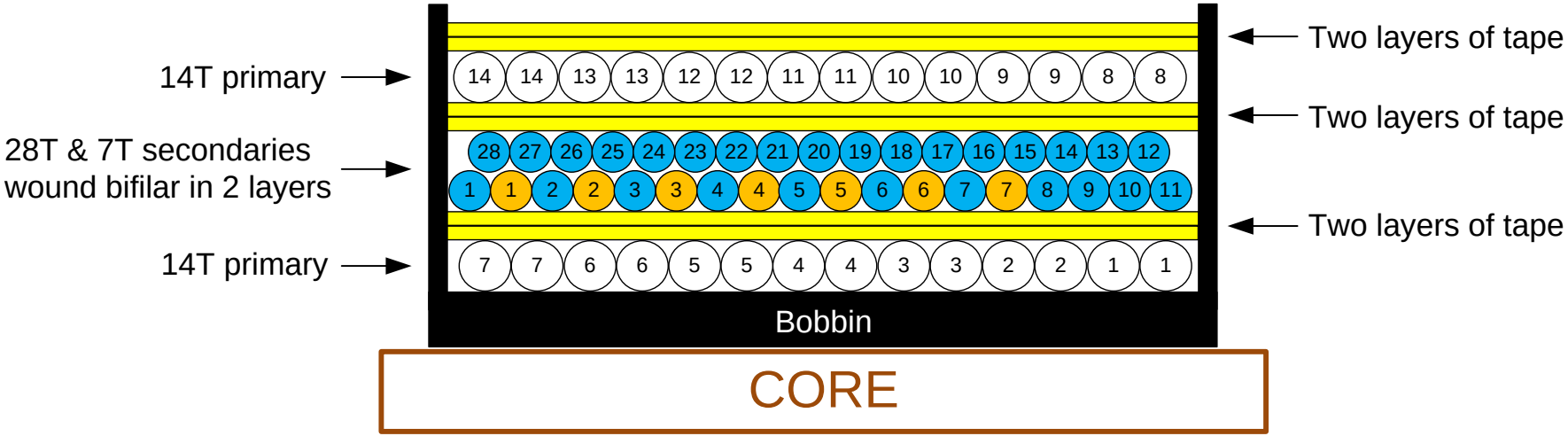
Dual-output transformer construction #1 14 : 28 : 7



Primary winding 50/50 parallel split

Parallel primary windings means that the **high dv/dt (noisy) SW node** also appears both on the inner and outer layers

Dual-output transformer construction #2 14 : 28 : 7



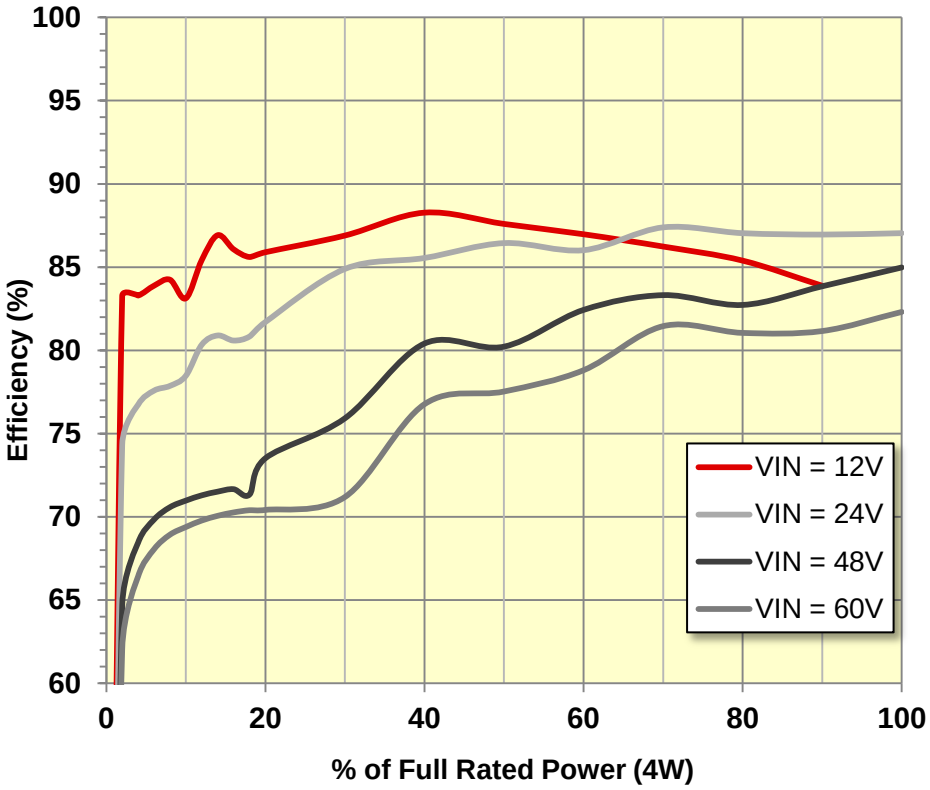
Primary winding 50/50 series split

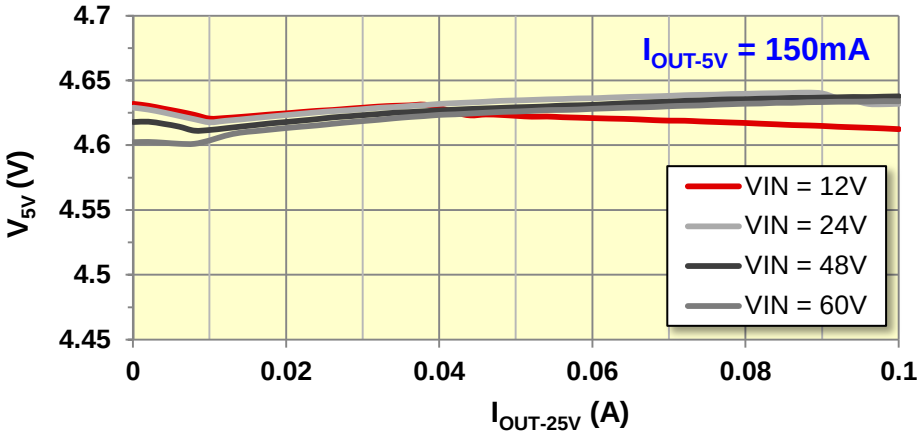
Wind first **half** of primary on inside layer nearest the bobbin and the other **half** on the outside

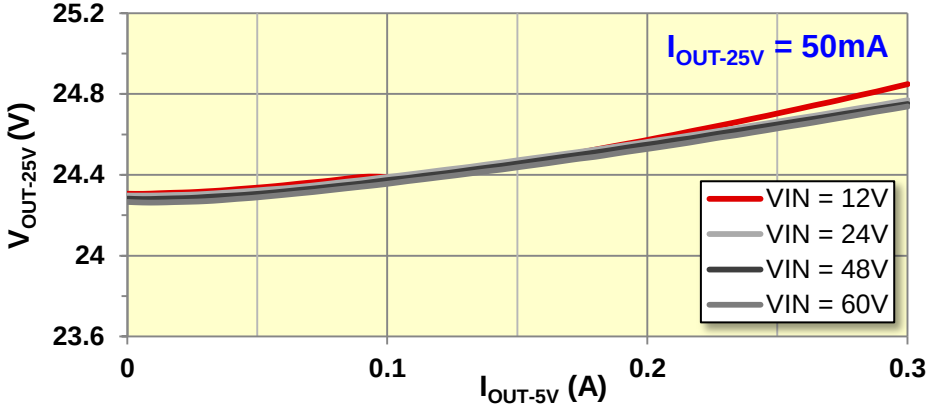
→ Noisy node (SW) **shielded** on inside & quiet node (VIN) connects to outside layer

→ Better EMI performance

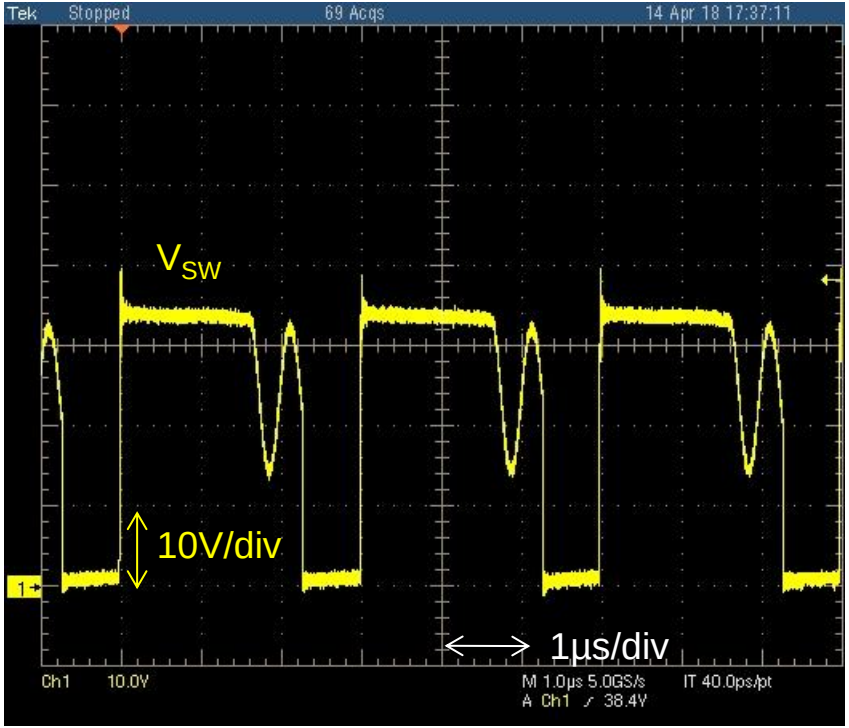
Efficiency, cross regulation

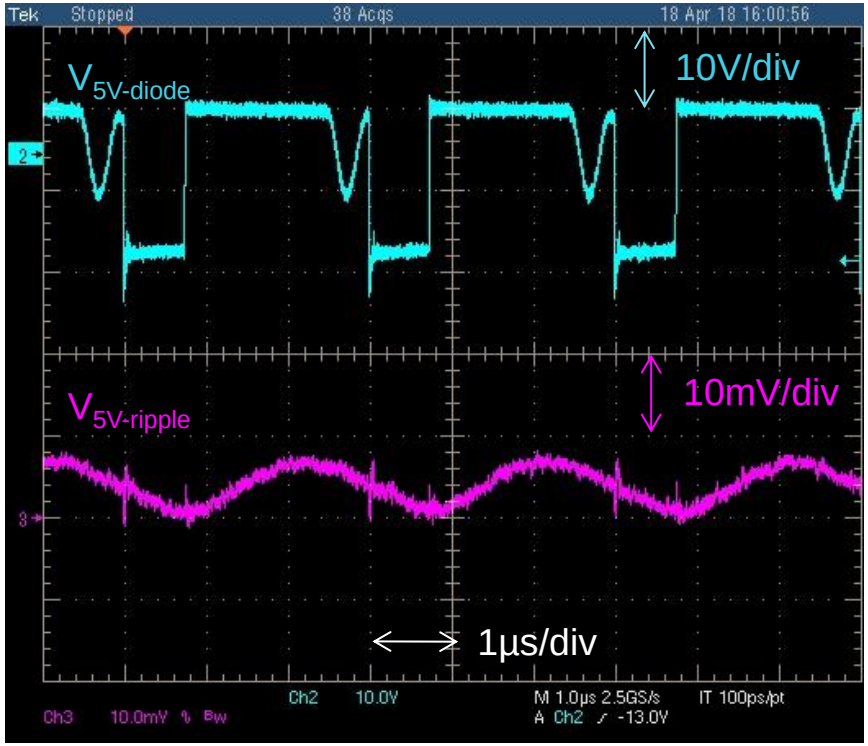






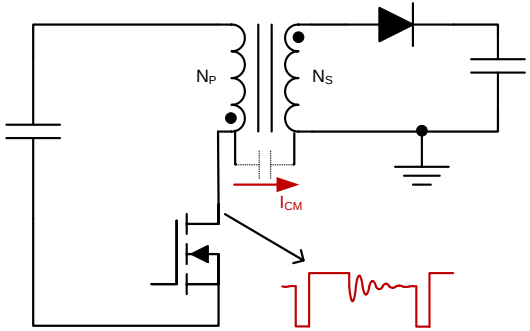
Converter waveforms, V_{IN} = 24V

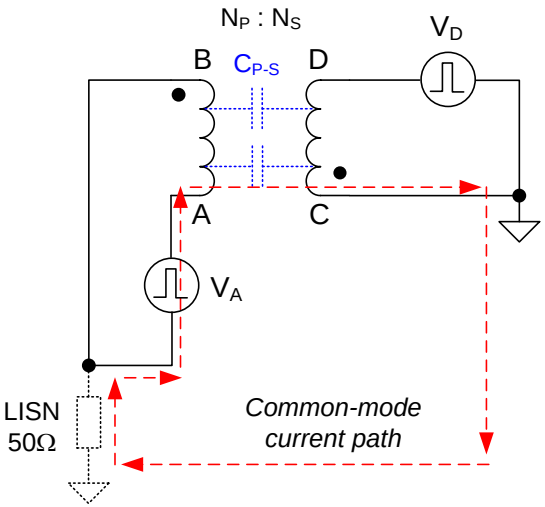




Common-mode EMI abatement

- Switching waveform at primary SW node couples common-mode current to the secondary side through interwinding capacitance $C_{P\text{-}S}$
  - This current can return to the primary side through the chassis GND connection (large loop area)
- In general, lower leakage transformer construction
  - ⇒ windings closer together
  - ⇒ higher interwinding capacitance, $C_{P\text{-}S}$
  - ⇒ worse EMI signature
- Connecting a cap from secondary to primary GNDs close to the transformer routes these currents directly back to their source (avoiding the LISN)
  - Not viable in IGBT/MOSFET gate driver designs due to large switch dv/dt ⇒ important to **minimize $C_{P\text{-}S}$**
  - **Input CM choke** and/or transformer **shield** are also helpful





Agenda

Isolated converters

- Isolated topologies overview
- PSR flyback topology – features and benefits, end equipment serviced

PSR flyback converter

- Operating modes – BCM, DCM, FFM
- Circuit design considerations – C_{IN}, C_{OUT}, D_F, V_{SW} clamp, UVLO, SS, TC, FB
- Magnetic design considerations – turns ratio, L_{MAG}, L_{LEAK}, ladder model
- Cross regulation in dual-output designs – secondary current distribution

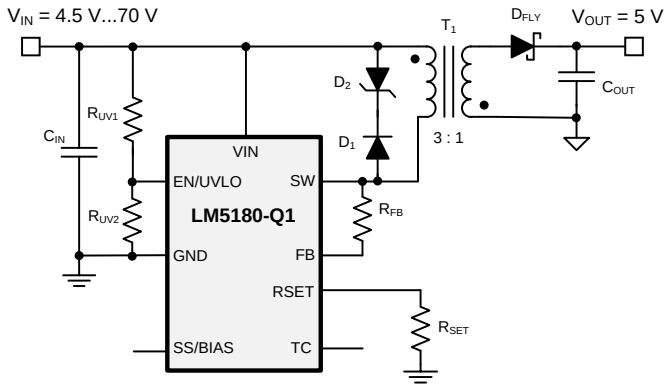
PSR flyback implementation

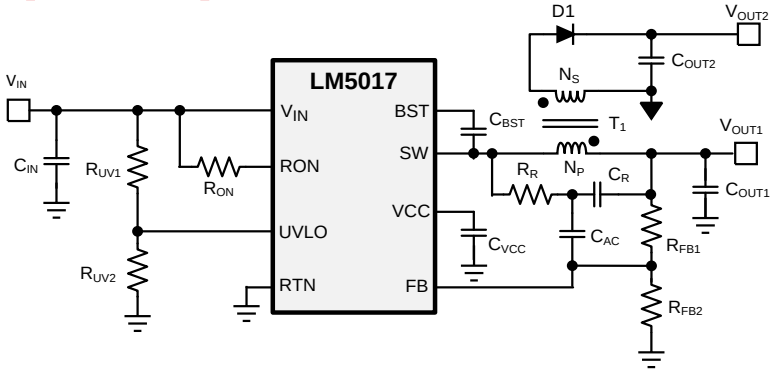
- Design examples and lab results – efficiency, regulation, key waveforms
- PCB layouts for single and dual outputs
- Common-mode EMI mitigation

Positioning PSR flyback converters

- **Choosing between PSR flyback, Fly-Buck and push-pull topologies**
- **Competitive analysis and spec comparison**

PSR flyback vs. Fly-Buck vs. push-pull



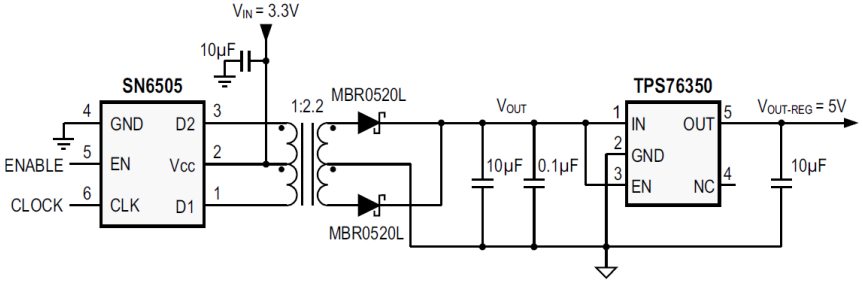


PSR flyback advantages:

- Extremely tight output regulation
- Operation at low Vin (> 4.5V)
- Fewer components & smaller solution size
- High light-load efficiency

Fly-Buck advantages:

- Regulated primary and secondary outputs
- Operation at high V_{IN} up to 100V
- Fast transient response & nearly constant F_{SW}



Push-pull advantages:

- Low cost, small size
- No feedback stability concerns
- Constant, synchronizable F_{SW}

Choosing between PSR flyback, Fly-Buck, push-pull

Feature	LM5180 PSR Flyback	LM5017/8/9 and LM5160/1 Fly-Buck	SN6501/5 Push-Pull
Output Voltage	**Precise output voltage regulation, 3% or better**	**Primary and secondary** outputs with better than 10% regulation	Secondary outputs with better than 10% regulation
Solution Size	Medium – low component count	Large – high component count	**Small – smallest magnetic**
Efficiency	**High light-load efficiency**	Conduction losses impact efficiency	Low efficiency since most solutions require an upstream buck converter
Frequency	Variable F_{SW}	Nearly constant F_{SW}	**Constant F_{SW}**
Input Range	**Wide input range with low minimum VIN ($V_{IN(min)}$ < 9V)**	Wide input range with high maximum VIN ($V_{IN(max)}$ > 70V)	Available regulated 3.3V or 5V input
Robustness	L_{LEAK} causes voltage spike	**Leakage energy clamped**	Leakage energy clamped
Application	V_{IN} = 4.5V–70V, P_{OUT} < 7W	V_{IN} = 9V–100V, P_{OUT} < 10W	V_{IN} = 3.3V or 5V, P_{OUT} < 3W

Customer collateral

The following information is available for you to send to customers

Content type	Content title	Link to content or more details
TI Design(s)	Compact 3-phase IGBT gate driver power supply using integrated switch PSR flyback converter	http://www.ti.com/tool/TIDA-010006
Customer training series or webinar session	Webinar – primary-side regulated flyback converter design	https://training.ti.com
Technical blog content or white paper	Flyback transformer design considerations for efficiency and EMI	https://www.ti.com/seclit/ml/slup338/slup338.pdf
	Under the hood of flyback SMPS designs	https://www.ti.com/seclit/ml/slup261/slup261.pdf
Selection and design tools and models	Excel quickstart calculator tool	http://www.ti.com/lit/zip/snvc218

Summary

- **PSR flyback applications** appear in many industrial and automotive end-markets
  - Sensing the flyback voltage enables tight load regulation and low component count
- **Circuit design** is relatively straight-forward
  - PSR flyback quickstart calculator expedites component selection
- **Understand transformer design**, whether in-house or using a magnetic vendor
  - Turns ratio selection may be an iterative process; mag inductance sets mode boundaries
  - Bifilar secondary windings improve dual-output cross regulation
- **Circuit examples** for single (5V/1A), dual (15V/-7.5V) and stacked dual (25V/5V)
  - Small solution size and wide V_{IN} range up to 70V
- **PCB layout** design begins with identifying high dv/dt nodes and high di/dt loops
  - Best performance is achieved with tight current loops and small switching node areas
- **Topologies** such as Fly-Buck, push-pull and conventional flyback also have merit
  - Best fit is chosen based on P_{OUT}, η, target load reg, solution size and cost goals

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