You Think LDOs are Simple?

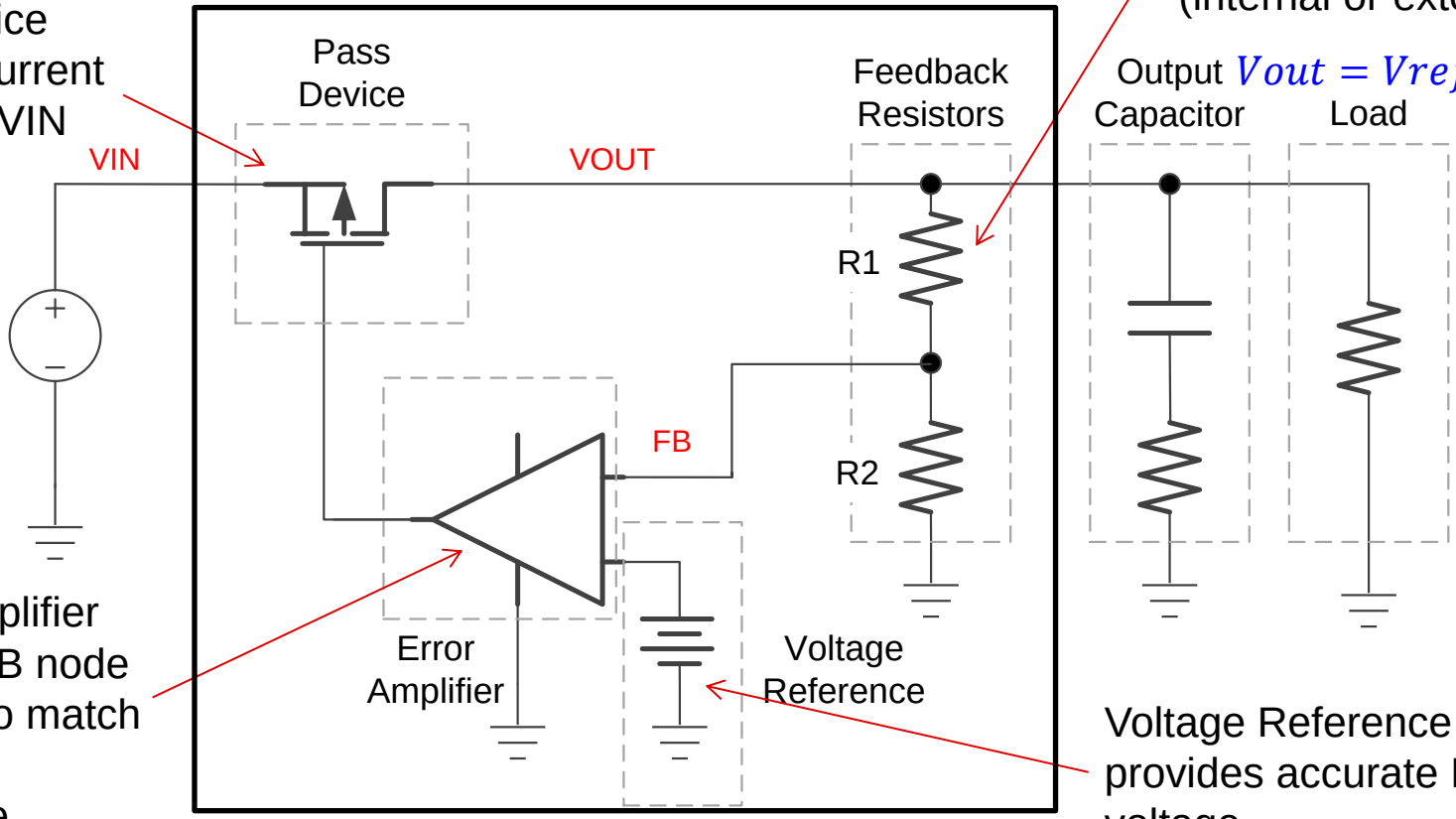
May 23rd 2018

Quick LDO Architecture Refresher

Feedback Resistors determine output voltage (internal or external)

Output $Vout = Vref * \frac{R1 + R2}{R2}$

Pass Device controls current flow from VIN to VOUT



Error Amplifier forces FB node voltage to match voltage reference.

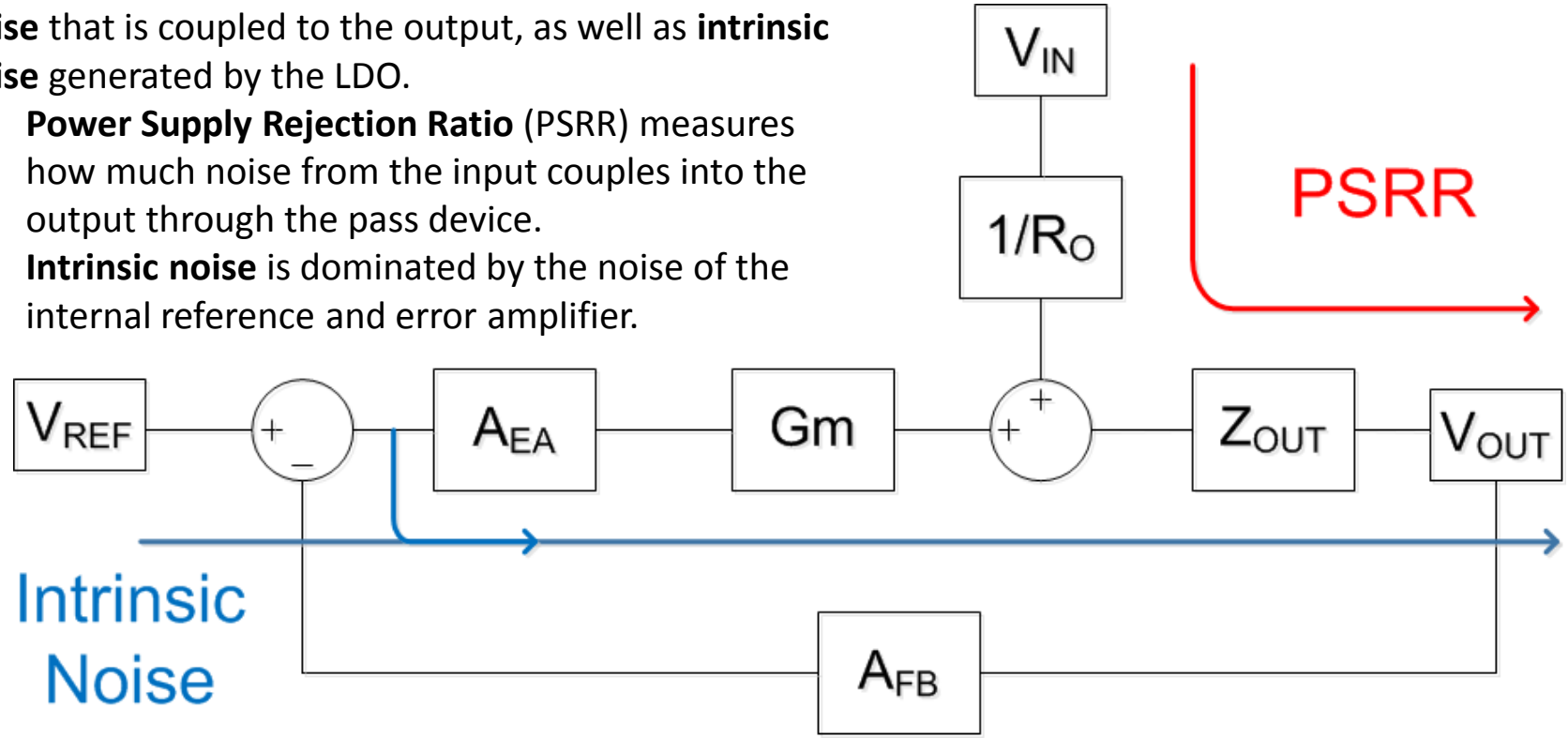
Voltage Reference provides accurate DC voltage.

Topics

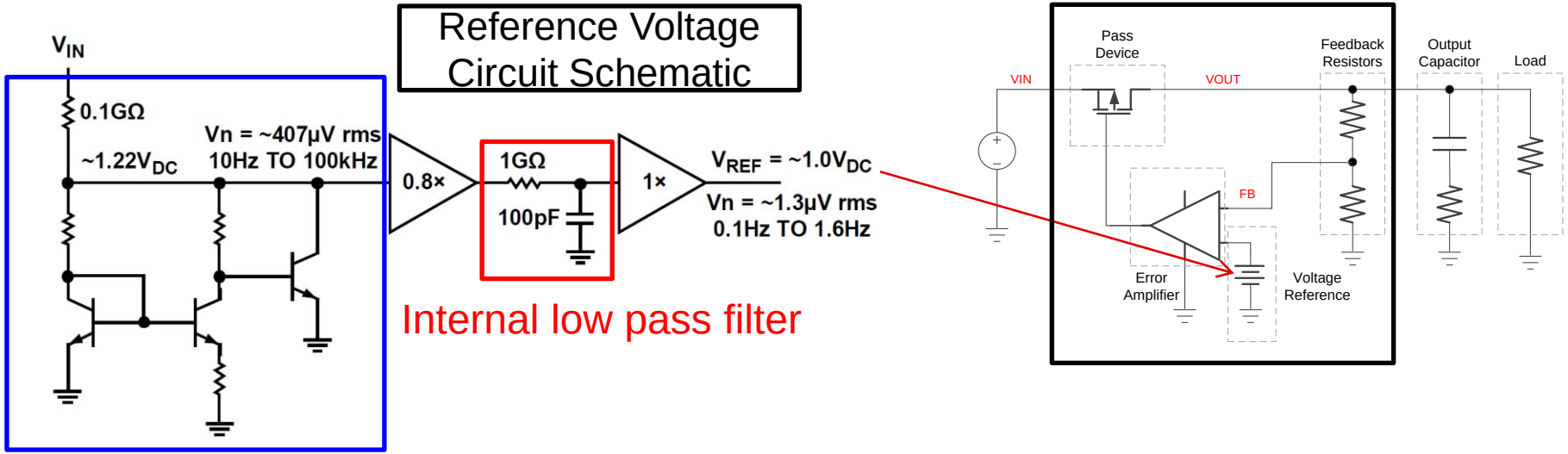
- Noise
- PSRR
- Thermal Performance
- Capacitor vs Capacitance
- Getting Answers to Your LDO Questions ASAP

How PSRR/Noise Relate to the Simplified AC Model

- Total LDO output voltage noise is composed of **Input noise** that is coupled to the output, as well as **intrinsic noise** generated by the LDO.
  - **Power Supply Rejection Ratio** (PSRR) measures how much noise from the input couples into the output through the pass device.
  - **Intrinsic noise** is dominated by the noise of the internal reference and error amplifier.



Noise Reduction with Internal Bandgap RC Filter Ex: LP38798, LP5907

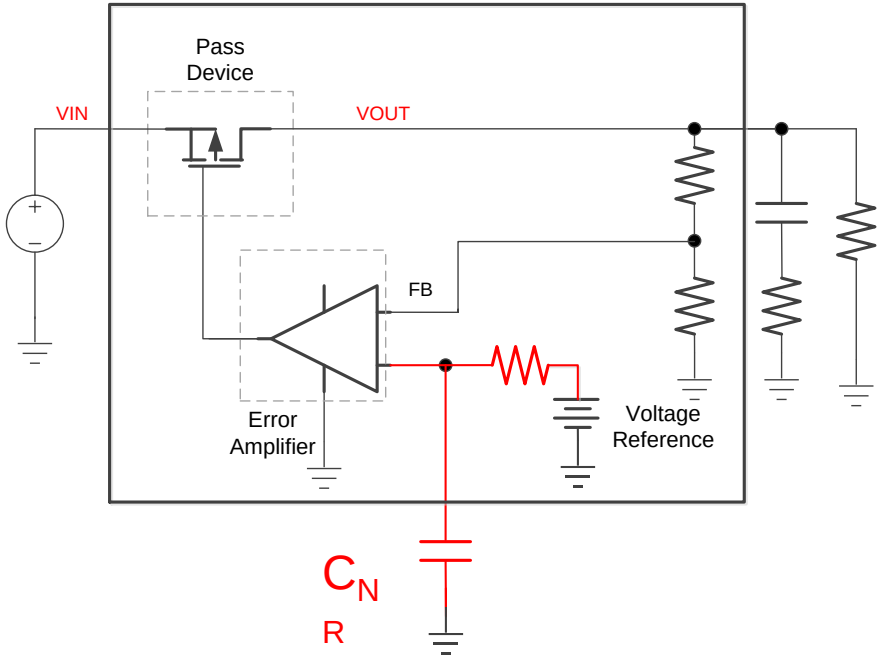


Bandgap Reference Voltage

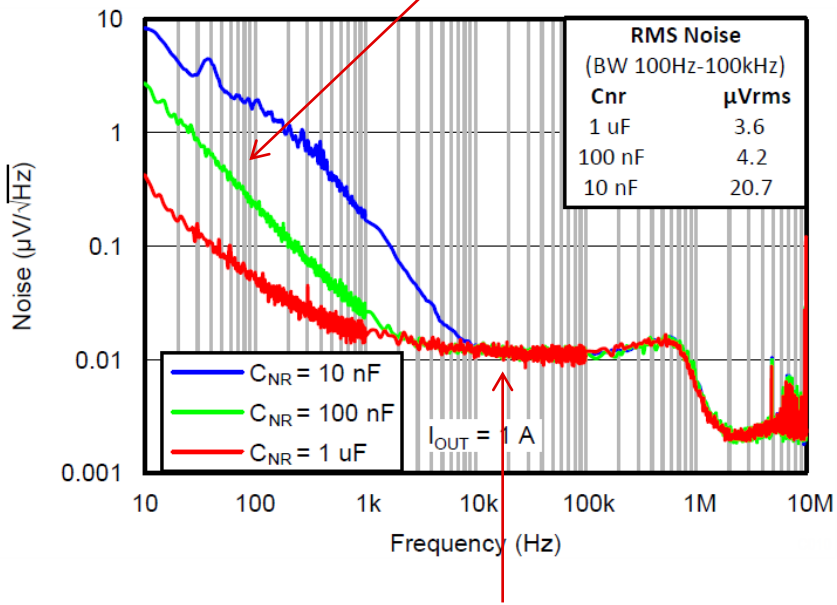
- Noise Reduction filter is integrated using very large filter resistor and small capacitor
  - $f_{cutoff} = \frac{1}{2\pi * R * C} = 1.6Hz$
- No external C_{NR} necessary

Bandgap Filter Using Noise Reduction (NR) Pin Ex: TPS7A83A, TPS7A47

The Reference Voltage noise can be filtered with an RC filter. This can be external or internal. On external devices, add a capacitor to the NR pin.

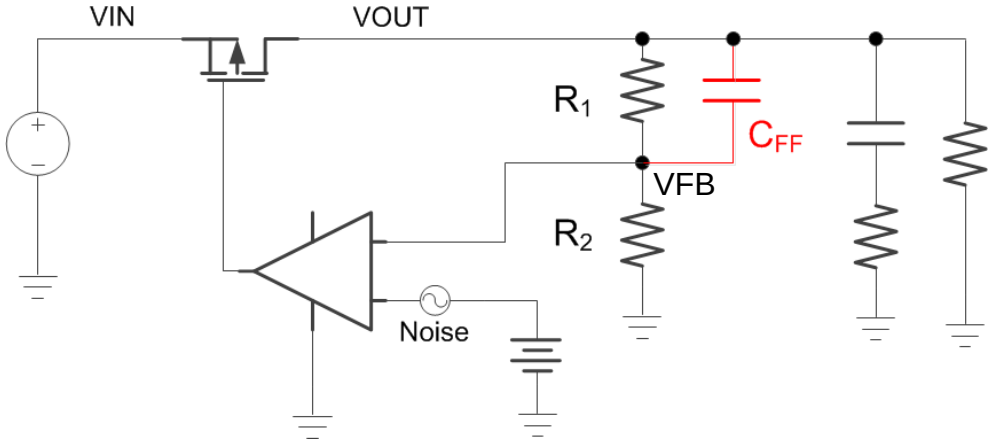


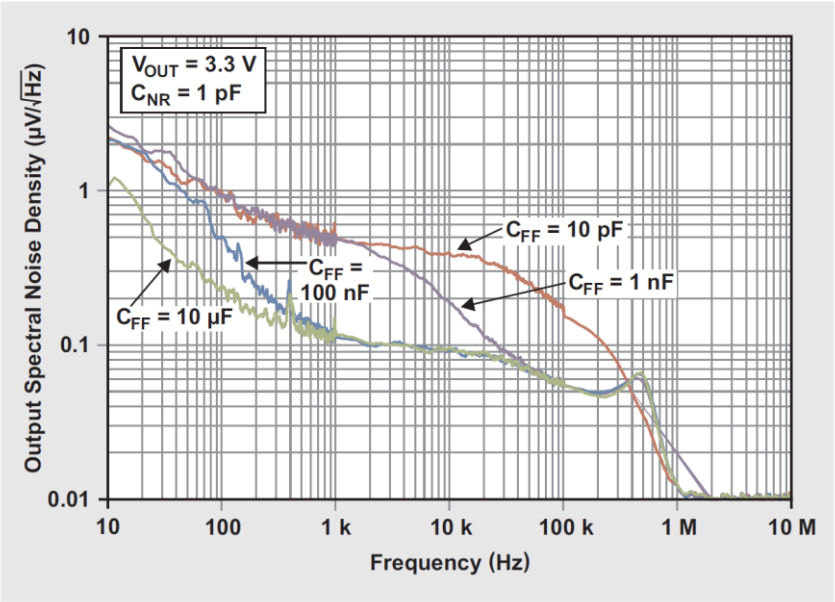
Increasing C_{NR} pushes noise lower.



However, noise in this region is limited by thermal noise from the error amplifier.

Adding feed forward cap reduces high freq. noise





- Error amp keeps Vfb=Vref, so any noise on Vref will also be present on Vfb.
  - Vout is a gained up version of Vfb set by R1 and R2 meaning the noise is gained up as well!
- C_{FF} acts as a short at high frequency which reduces the closed-loop gain amplifying high frequency noise less
- App note on the pros and cons of using a Cff http://www.ti.com/lit/an/sbva042/sbva042.pdf

- Also: Added zero makes LDO more stable ⇒ lower CL Gain peaking.
- Note: C_{FF} only helps when there is gain from Vfb to Vout, C_{FF} is shorted if R1=0

What Conditions Effect Noise

Number one thing that effects noise performance is the output voltage

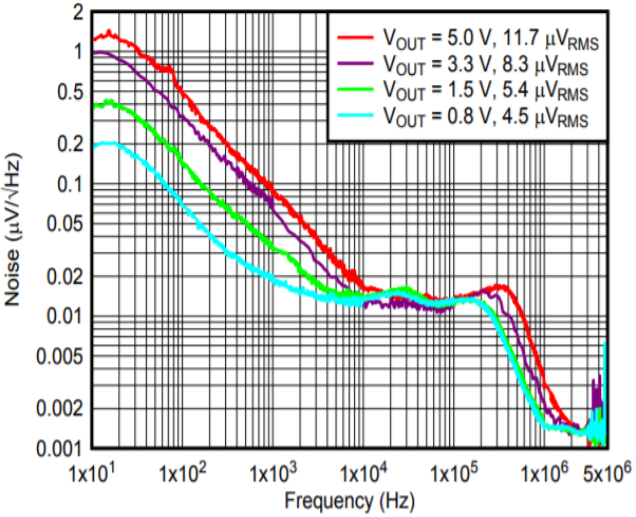


Figure 10. Output Noise vs Frequency and Output Voltage

The next thing that effects noise is the noise reduction capacitor

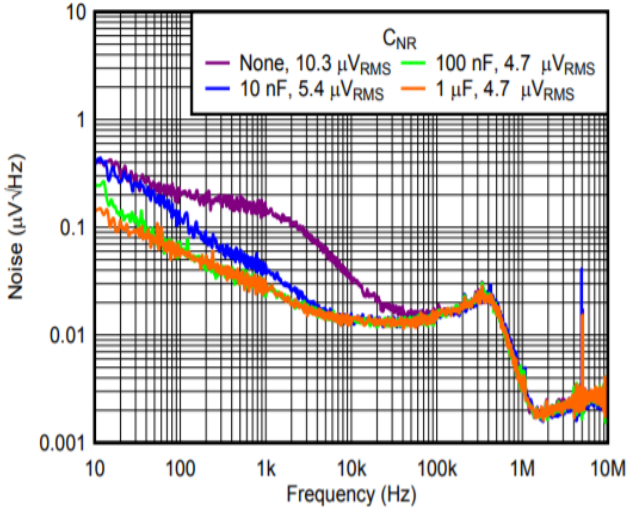


Figure 9. Spectral Noise Density vs Frequency and $C_{NR/SS}$

And the final thing that effects noise to a large degree is the feedforward capacitor

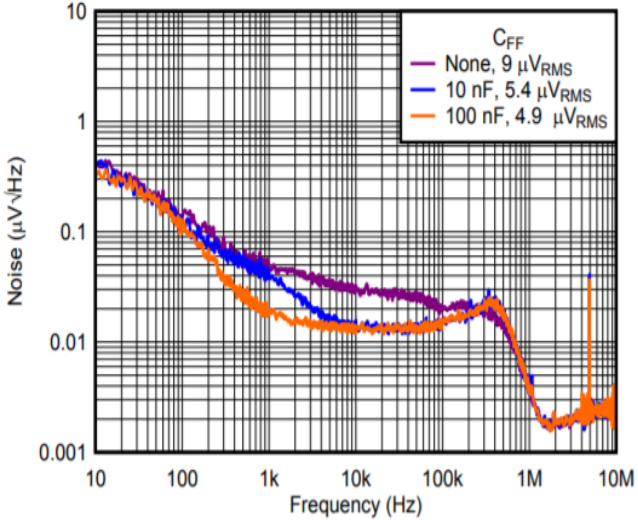


Figure 10. Spectral Noise Density vs Frequency and C_{FF}

What Conditions Do Not Effect Noise

Number one thing that has almost no effect on noise is output current

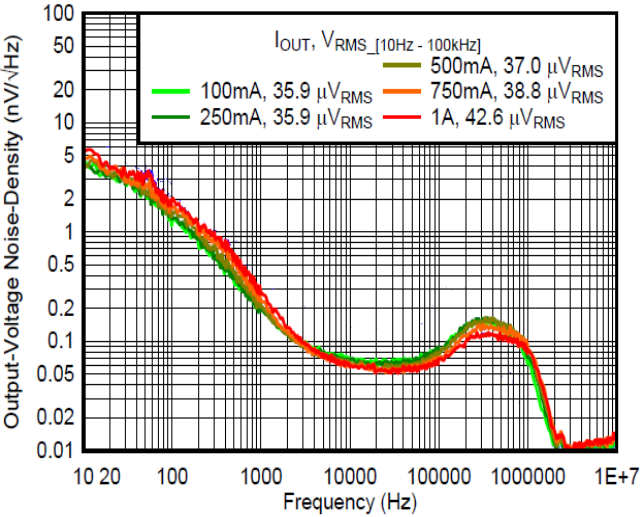


Figure 11. Noise Density vs Frequency and I_{OUT}

The next thing that has very little effect on noise is Vin

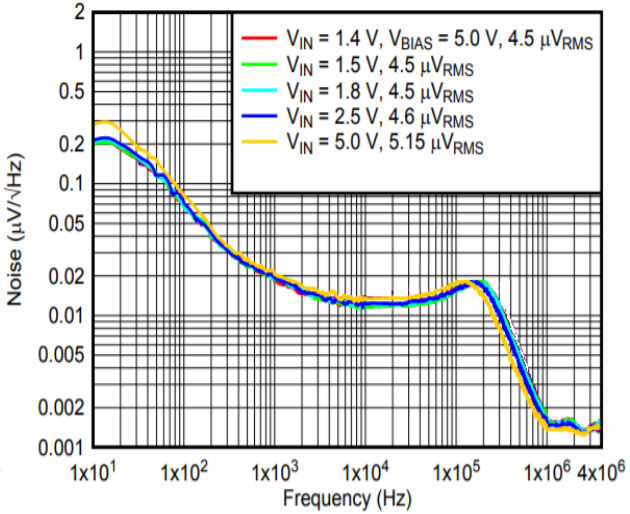


Figure 11. Output Noise vs Frequency and Input Voltage

And the final thing that has a small effect on noise is output capacitor (very large Cout can show some difference)

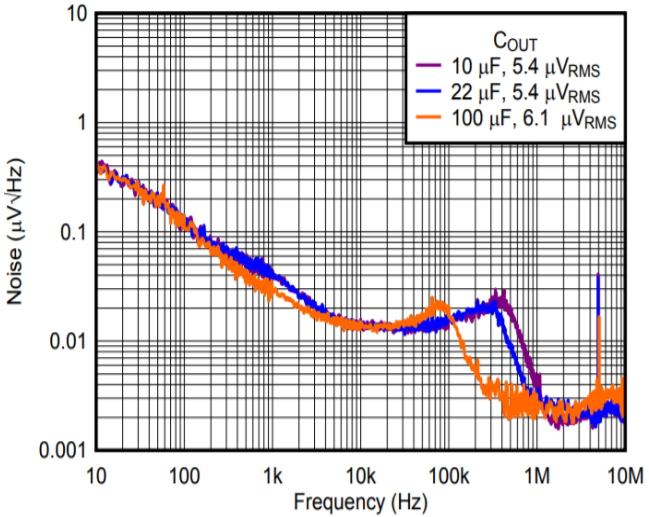


Figure 11. Spectral Noise Density vs Frequency and C_{OUT}

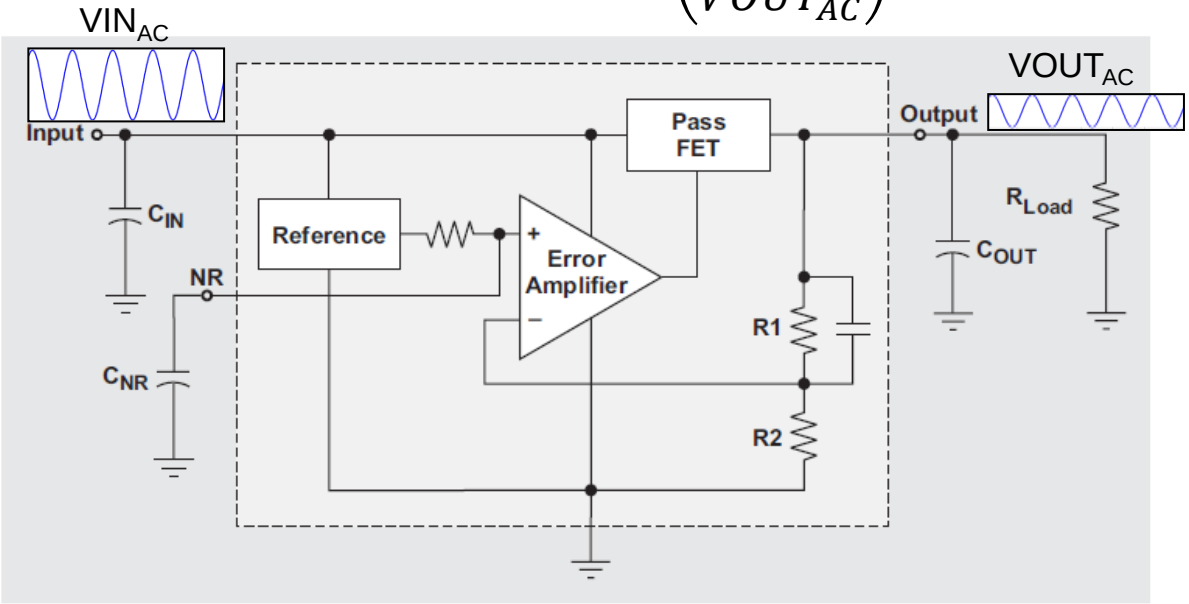
Topics

- Noise
- PSRR
- Thermal Performance
- Capacitor vs Capacitance
- Getting Answers to Your LDO Questions ASAP

PSRR

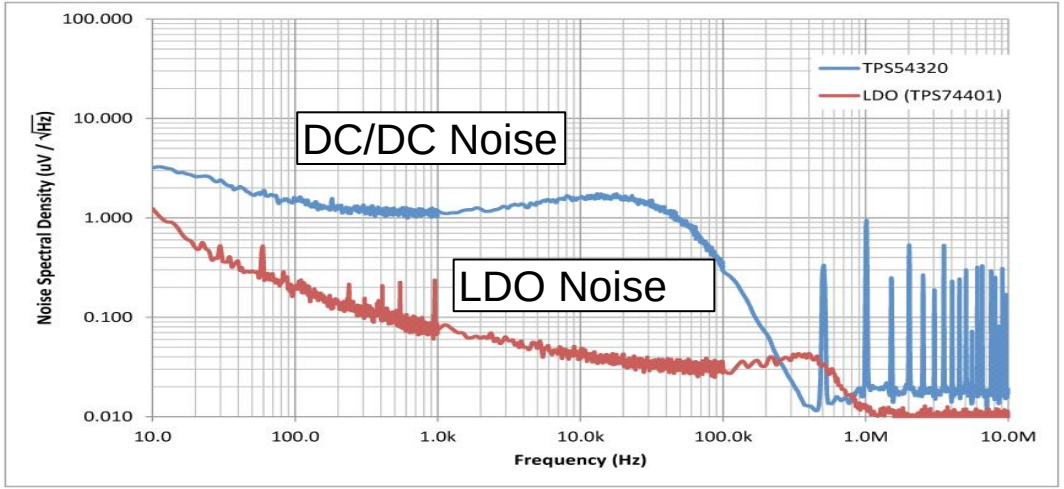
PSRR (Power Supply Rejection Ratio) represents the ability of the LDO to filter input voltage changes. This is critical for low-noise applications.

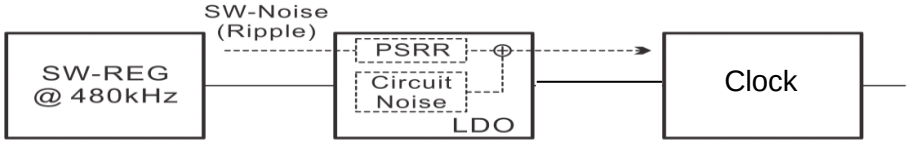
$$PSRR = 20 * \log\left(\frac{VIN_{AC}}{VOUT_{AC}}\right)$$



The Importance of LDO PSRR

- DC/DC (switching) converters are necessary for efficiency, however they are very noisy
  - most clock generators and clocking devices are very sensitive to power supply noise
  - DC/DC converters are commonly followed by an LDO to clean the supply





Texas Instruments

Typical PSRR Curve

Region 1 is determined by:

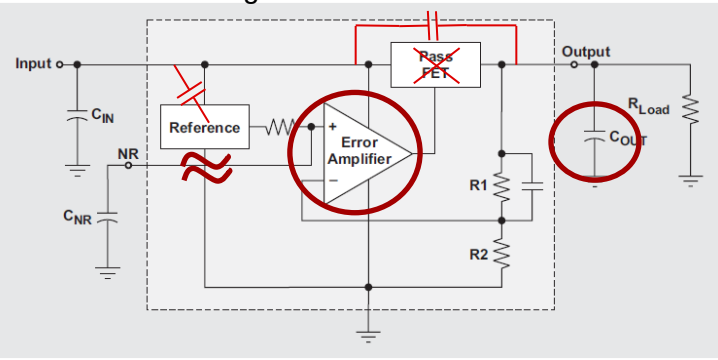
- PSRR of the Reference and the effectiveness of the RC filter

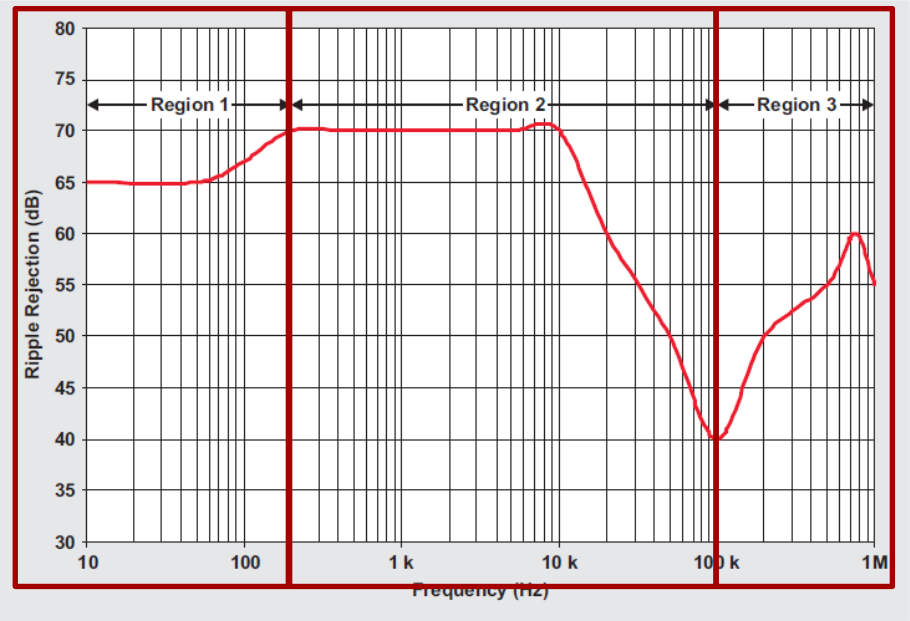
Region 2 is determined by:

- Open-Loop Gain of Error Amplifier

Region 3 is determined by:

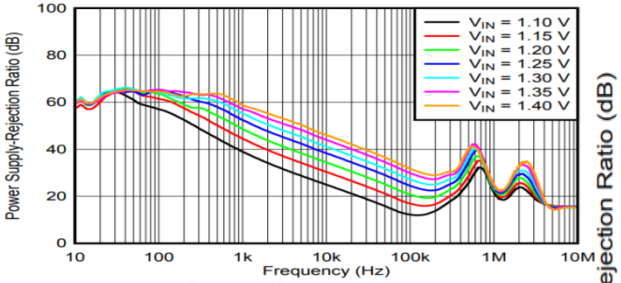
- Parasitic capacitance of the FET and the output capacitor (capacitive divider)
  - The smaller the parasitic cap the less the Vin is AC coupled to Vout
  - The larger Cout the more noise is shunted to GND





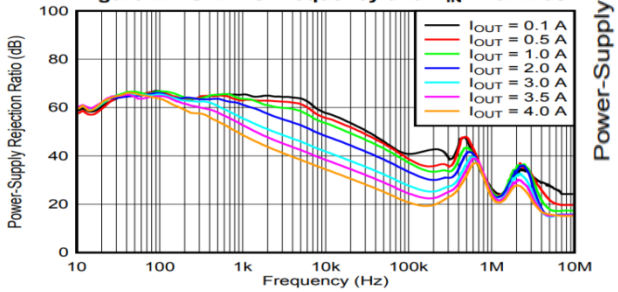
What Conditions Effect PSRR

#1 thing that effects PSRR performance is the Combo of Vin/Iout (Vdo)



I_{OUT} = 4 A, Vout = 0.8V

Figure 2. PSRR vs Frequency and V_{IN} With Bias



V_{IN} = 1.2 V, Vout = 0.8V

Figure 1. PSRR vs Frequency and I_{OUT}

The next thing that effects PSRR is the noise reduction capacitor

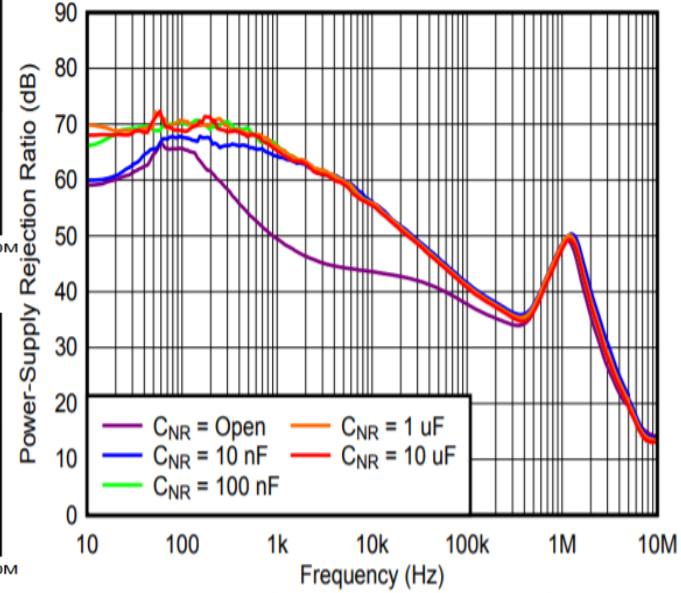


Figure 7. PSRR vs Frequency and $C_{NR/SS}$

And the final thing that effects PSRR is the feedforward capacitor

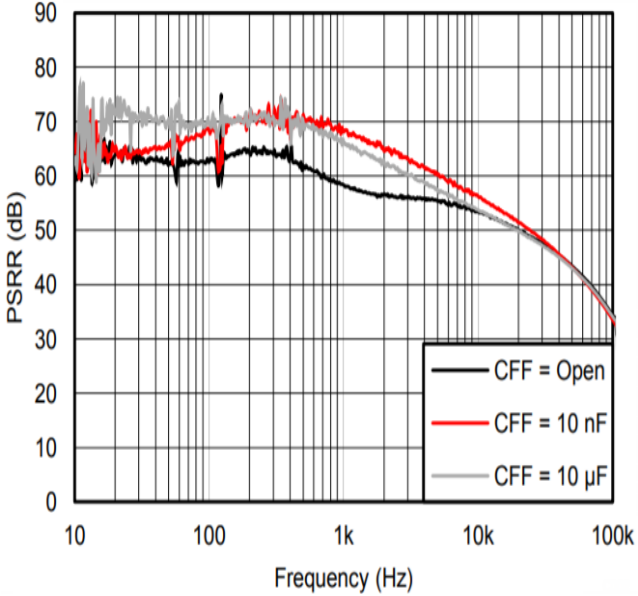


Figure 5. PSRR for Various C_{FF} Values

What Conditions Do Not Effect PSRR

Number one thing that has almost no effect on PSRR is Vbias>min

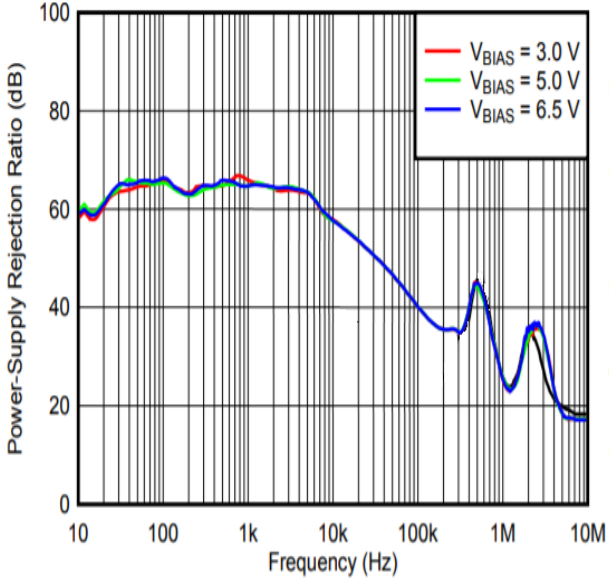


Figure 3. PSRR vs Frequency and V_{BIAS}

The next thing that only has a small effect on PSRR is Vout

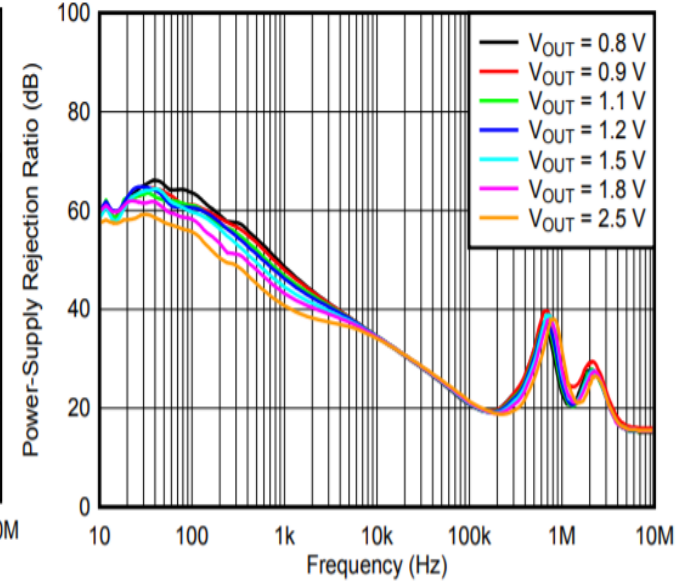


Figure 5. PSRR vs Frequency and V_{OUT} With Bias

And the final thing that has some effect (but only at high freq) is output capacitor

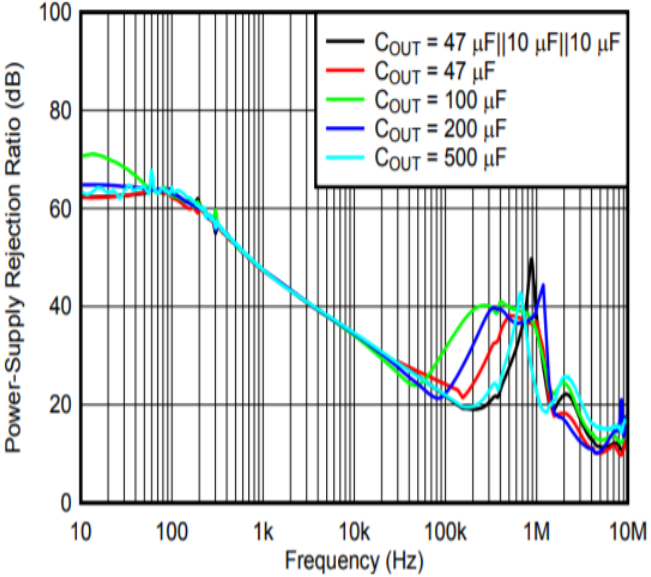


Figure 7. PSRR vs Frequency and C_{OUT}

Topics

- Noise
- PSRR
- Thermal Performance
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JEDEC Thermals

- Because an IC's thermal dissipation is subject to many variables we use the JEDEC standard (JESD51) for all thermal modeling.
- The JEDEC standard is used so that devices can be easily compared on a similar basis.
  - if a competitor is not reporting the JEDEC standard the customer should consider why they don't want to be directly compared to other devices.
- Common thermal metrics: θ_{JA}, θ_{JB}, $\theta_{JC(top)}$, $\theta_{JC(bot)}$

TI Datasheet

6.4 Thermal Information

THERMAL METRIC[1][2]		TPS732[3] DRB [SON] 8 PINS	DCQ [SOT223] 6 PINS	DBV [SOT23] 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.3	53.1	205.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	35.2	119	
$R_{\theta JB}$	Junction-to-board thermal resistance	72.8	7.8	35.4	
ψ_{JT}	Junction-to-top characterization parameter	2.7	2.9	12.7	
ψ_{JB}	Junction-to-board characterization parameter	25	7.7	34.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the *TI PCB Thermal Calculator*.
(3) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3 × 2 thermal via array.

Competitor Datasheet

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Value)		Unit
DPAK 5-PIN PACKAGE			
	Min Pad Board (Note 3)	**1" Pad Board** (Note 4)	
Junction-to-Tab (psi-JLx, ψ_{JLx})	4.2	4.7	C/W
Junction-to-Ambient ($R_{\theta JA}$, θ_{JA})	100.9	46.8	C/W
D²PAK 5-PIN PACKAGE			
	0.4 sq. in. Spreader Board (Note 5)	**1.2 sq. in. Spreader Board** (Note 6)	
Junction-to-Tab (psi-JLx, ψ_{JLx})	3.8	4.0	C/W
Junction-to-Ambient ($R_{\theta JA}$, θ_{JA})	74.8	41.6	C/W

3. 1 oz. copper, 0.26 inch² (168 mm²) copper area, 0.062" thick FR4.
4. 1 oz. copper, 1.14 inch² (736 mm²) copper area, 0.062" thick FR4.
5. 1 oz. copper, 0.373 inch² (241 mm²) copper area, 0.062" thick FR4.
6. 1 oz. copper, 1.222 inch² (788 mm²) copper area, 0.062" thick FR4.

28mm x 28mm area on the top side dedicated to only thermal dissipation?

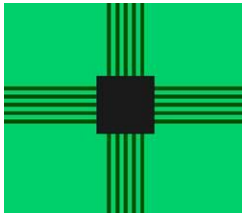
θ_{JA}: Understanding Usage and Limitations

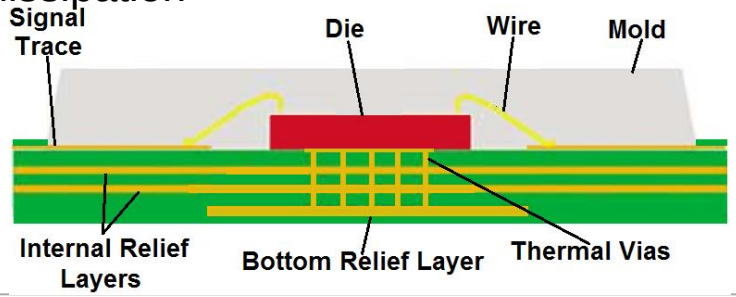
- The junction-to-ambient thermal resistance, θ_{JA}, is the most commonly used thermal metric.
  - θ_{JA} is a measure of the thermal performance of an IC mounted on a PCB.
- θ_{JA} is used since the ambient temperature is one of the few temperatures that designers have accurate data on. $T_J = T_A + (\theta_{JA} * P_D)$
  - The board acts as the main heat sink for any IC attached to it
  - If the actual application board is significantly different from the JEDEC High-K board this can result in an estimate that is unrealistic

Factors Affecting θja	Strength of Influence (rule of thumb)	Relation to θja
PCB design	Very Strong	The more metal connected to the IC the lower θja due to larger thermal mass
Chip or pad size	Strong	The larger the chip and thermal pad the lower θja due to heat spreading
Altitude	Medum	The lower the altitude the lower θja due to increased cooling efficiency of air
External ambient temperature	Weak	The higher the ambient temp the lower θja due to increased radiative heat transfer
Power dissipation	Very Weak	The higher the junction temp the lower θja due to increased heat transfer

JEDEC High-K Board

- TI LDO thermal metrics are modeled using the JEDEC High-K Board (2s2p)
- The JEDEC High-K board has:
  - Two internal layers which have ~5500mm^2 of 1oz copper (1 GND & 1 PWR plane)
  - Bottom layer (opposite the IC) thermal relief layer which has ~1100mm^2 of 2oz copper
  - Internal and bottom layers are connected to the thermal pad using as many thermal vias as can be fit within the power pad dimensions.
  - The top layer only has traces running straight to the pins.
- The JEDEC high-k board is good but not 100% optimized for maximum thermal dissipation





TEST BOARD DESIGN	JEDEC HIGH-K 2s2p	JEDEC LOW-K 1s0p
Trace thickness	0.0028 in	
Trace length	0.98 in	
PCB thickness	0.062 in	
PCB width	4 in	
PCB length	4.5 in	
Power/ground plane thickness	0.0014in (2 planes)	No internal copper planes

Other Thermal Considerations

- Nearby heat sources on the PCB can reduce the ability of the LDO to shed heat to the board
  - This is because those other heat sources increase the local board temperature decreasing the temperature differential between the board to the LDO in question
- Short load pulses will still heat the die significantly if there isn't enough time between high load pulses
  - an increase in power dissipation will cause the die temp to stabilize on the order of tens of milliseconds.
  - So unless the load pulses are less than a few milliseconds, with significantly longer off times, the LDO should reach a similar internal temp as if the load was on constantly.
- Forced convection and board level heatsinks can help significantly, though they are rarely a consideration for many applications which have to rely on passive cooling only
  - The thermal models in our datasheets assume natural convection (no forced air).

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Capacitor & Capacitance Defined

- Capacitor: a **device** used to store an electric charge, consisting of one or more pairs of conductors separated by an insulator.
- Capacitance: the **ability** to store an electric charge.

- In an Ideal world the value written on a capacitor would be exactly the same as the amount of capacitance it provides when inserted into a system.
  - (Un)Fortunately we do not live in a world with ideal components
    - The existence of an ideal components would leave most of us without a job

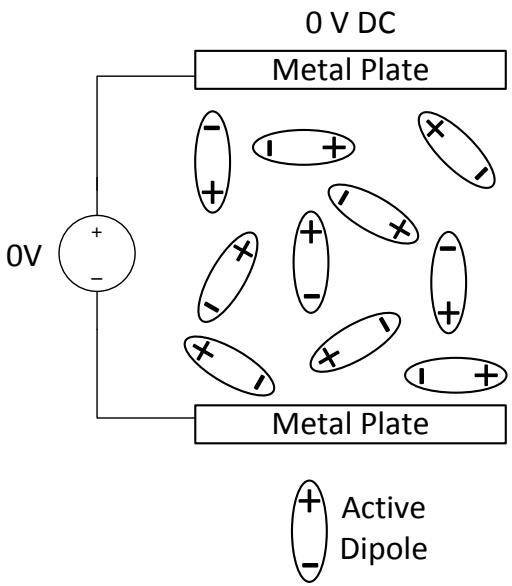
Capacitor vs Capacitance Explained

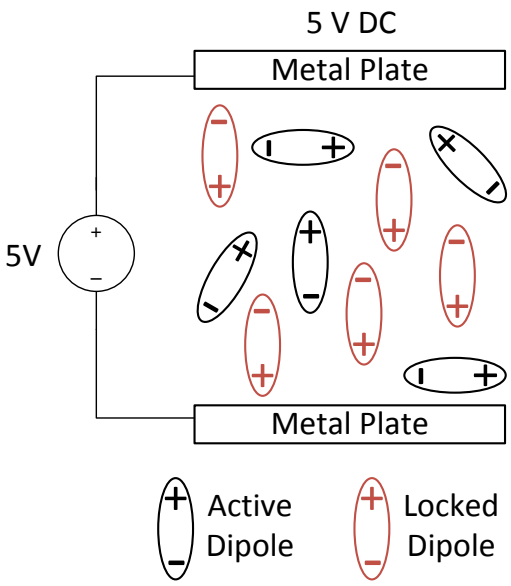
- There are three main reasons why the capacitance of a capacitor isn't always what it says on the label

1. Derating due to being biased with a DC Voltage
2. Derating due to changes in temperature
3. Manufacturing tolerances
    1. This is called out specifically in the specs and is usually ±10% or ±20%

DC Voltage Derating Explained

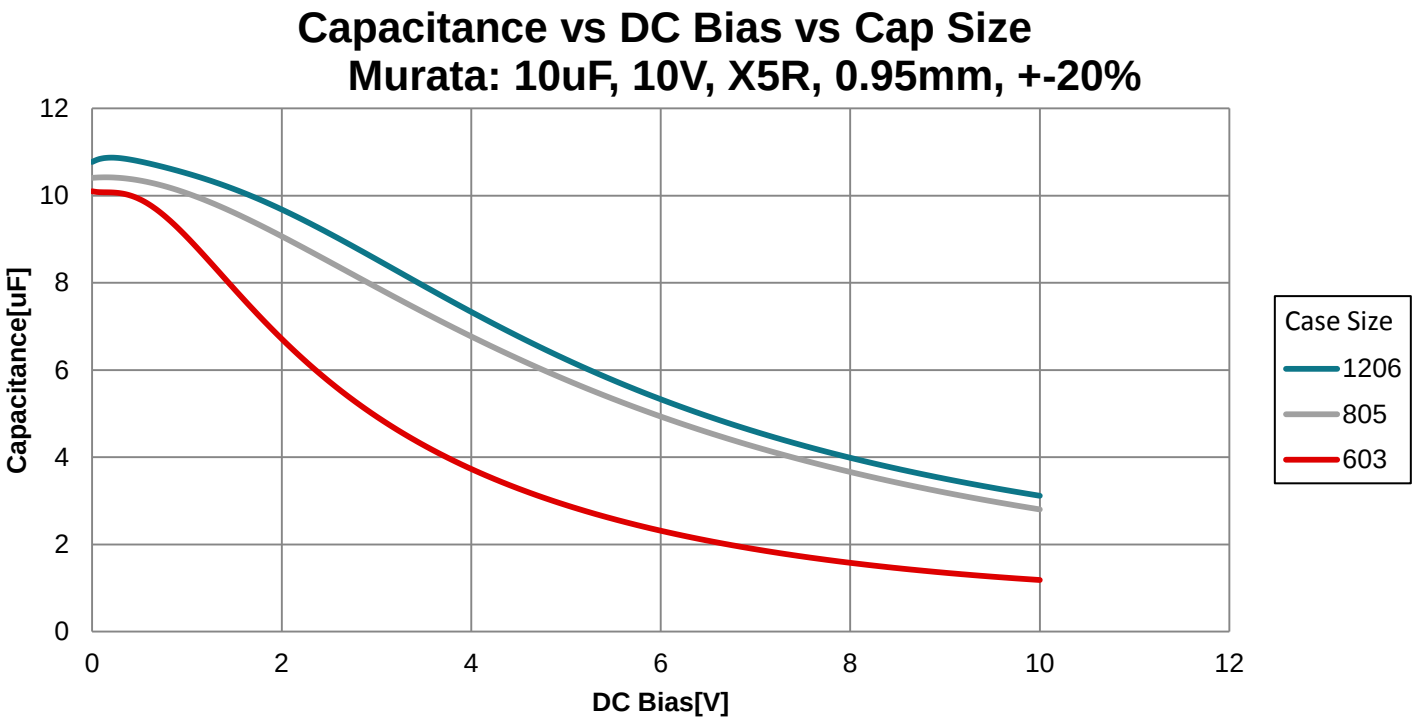
- When a DC Voltage is applied to a capacitor it creates an E-field which “locks” some of the atomic dipoles into place.
  - These “locked” dipoles do not react to AC voltage transients which is why the effective capacitance decreases.





Capacitance vs DC Bias

The same voltage applied across a thicker dielectric will result in lower E-Field which will “lock in” less dipoles



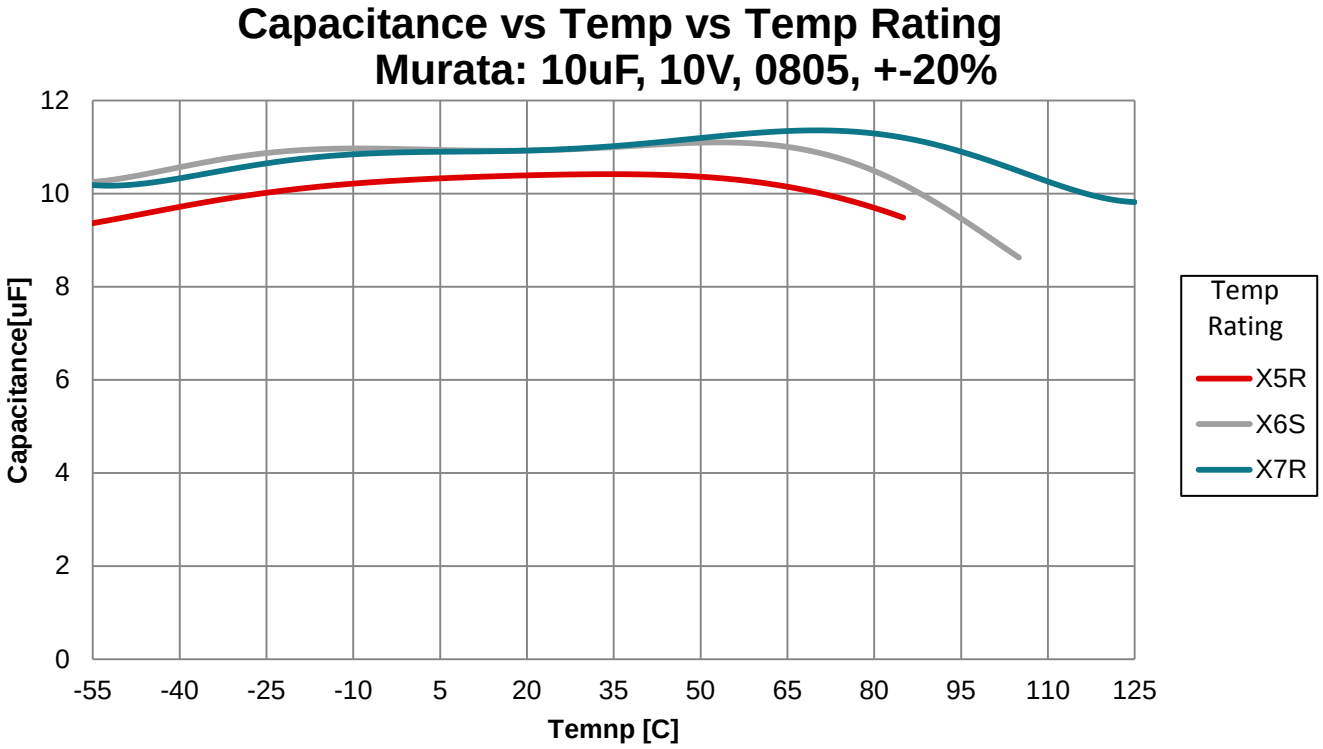
Capacitance vs Temperature Decoder Ring

Like all electronics capacitors have a temperature rating over which their performance is specified

Majority of LDO junction temperatures are usually specified from -40C to 125C.

1st Character: Low Temp		2nd Character: High Temp		3rd Character: Max Change over Temp	
Char	Temp (°C)	Char	Temp (°C)	Char	Change (%)
Z	10	2	45	A	±1.0
Y	-30	4	65	B	±1.5
X	-55	5	85	C	±2.2
		6	105	D	±3.3
		7	125	E	±4.7
		8	150	F	±7.5
		9	200	P	±10
				R	±15
				S	±22
				T	+22, -33
				U	+22, -56
				V	+22, -82

So we usually recommend X5R or X7R caps

Capacitance vs Temperature Graph

Temperature affects the capacitance much less than the DC Bias which can reduce the capacitance by 90%