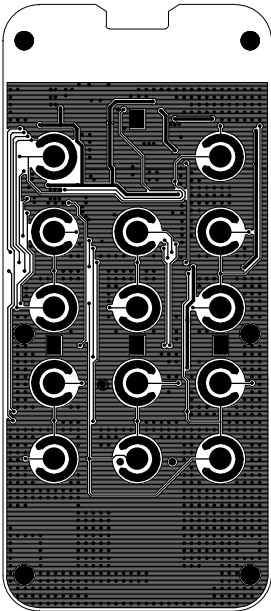


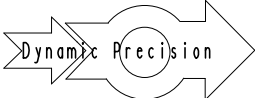
DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
■	0.3	PLATED	776
.	1.0	NON-PLATED	2
▲	1.0	NON-PLATED	1
◎	2.5	NON-PLATED	6
▢	2.3x1.75	NON-PLATED	4

ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>DRM</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI	Latest Revision Prepared By PIOTR PRZYSTUP		Sheet <b>1</b> of 10	Size A4
	First Revesion Checked By ESPEN WIUM	Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013	



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	Title <b>ZLLRC</b>		Layer <b>PA1</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI	Latest Revision Prepared By PIOTR PRZYSTUP		Sheet <b>2</b>	of 10
	First Revesion Checked By ESPEN WIUM	Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013	

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A

A

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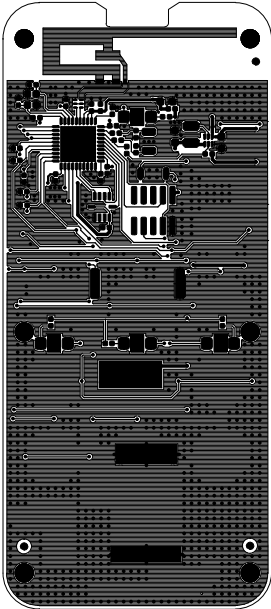
B

C

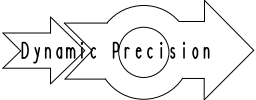
C

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D



ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>PA2</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI	Latest Revision Prepared By PIOTR PRZYSTUP		Sheet <b>3</b>	of 10 Size A4
	First Revesion Checked By ESPEN WIUM	Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013	

A

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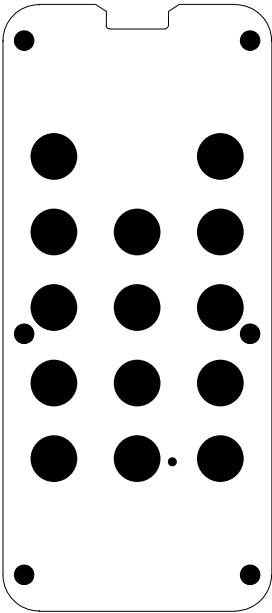
B

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ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>PL1</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI	Latest Revision Prepared By PIOTR PRZYSTUP		Sheet <b>4</b>	of 10 Size A4
	First Revesion Checked By ESPEN WIUM	Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013	

A

A

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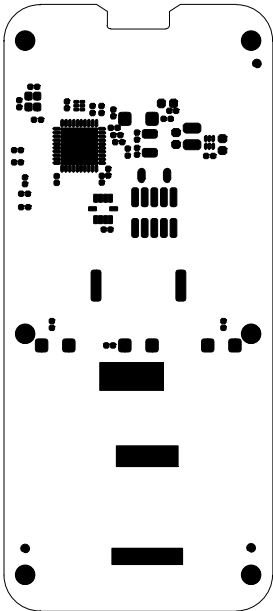
B

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ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>PL2</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI		Latest Revision Prepared By PIOTR PRZYSTUP		Sheet of <b>5</b> 10
	First Revision Checked By ESPEN WIUM		Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013

A

A

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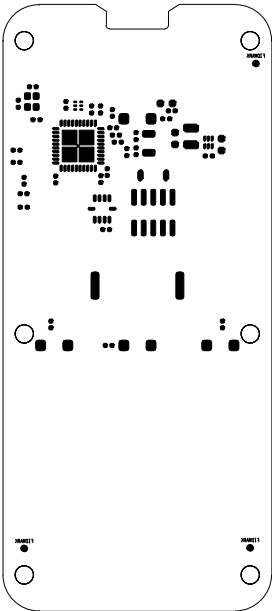
B

C

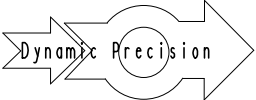
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ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>SP2</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI	Latest Revision Prepared By PIOTR PRZYSTUP		Sheet <b>6</b>	of 10
	First Revision Checked By ESPEN WIUM	Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013	

A

A

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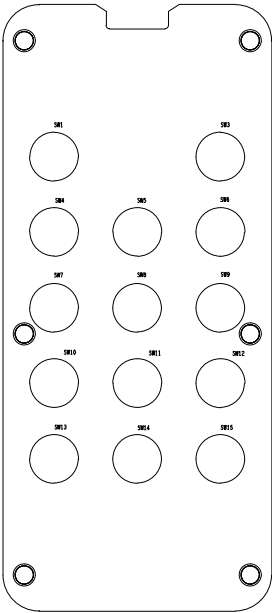
B

C

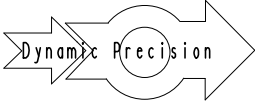
C

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D



ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>SS1</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI	Latest Revision Prepared By PIOTR PRZYSTUP		Sheet <b>7</b>	of 10 Size A4
	First Revesion Checked By ESPEN WIUM	Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013	

A

A

B

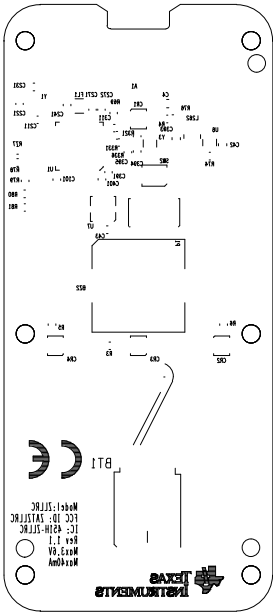
B

C

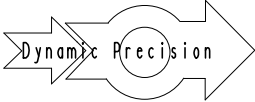
C

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ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>SS2</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI	Latest Revision Prepared By PIOTR PRZYSTUP		Sheet <b>8</b>	of 10
	First Revision Checked By ESPEN WIUM	Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013	



A

A

B

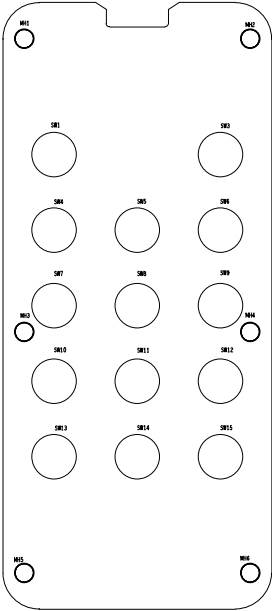
B

C

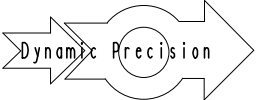
C

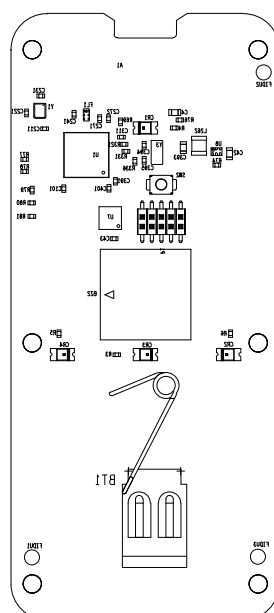
D

D

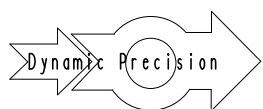


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	Title <b>ZLLRC</b>		Layer <b>AD1</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI	Latest Revision Prepared By PIOTR PRZYSTUP		Sheet <b>9</b> of 10	Size A4
	First Revesion Checked By ESPEN WIUM	Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013	



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Title

**ZLLRC**

Layer

**AD2**

PCB No.

Revision

**1.1**First Revision Prepared By  
ANDRZEJ GRUCHALSKILatest Revision Prepared By  
PIOTR PRZYSTUPSheet of  
**10** 10Size  
A4First Revision Checked By  
ESPEN WIUMLatest Revision Checked By  
ESPEN WIUMLatest modification date  
03 April 2013