Refclk Jitter Analysis for the TLK2521

The jitter on the reference clock (GTXclk) can be a very crucial factor when designing applications with the TLK2521. The TLK2521 has an internal PLL with a certain bandwidth depending on the data rate. Jitter on the Refclk with a frequency below the PLL bandwidth gets transferred into the serial output data stream while high-frequency jitter gets filtered out by the internal PLL. Additional jitter on the serial data stream reduces the data eye opening and increases the probability of generating bit errors.

This document shows what kind and how much jitter can be tolerated by the TLK2521 and still achieve error free data transmission. The clock jitter transfer section investigates the impact of clock jitter on the serial transmitter while the clock jitter tolerance portion focuses on maximum clock jitter for certain applications like transmission over 36 inch of FR4 backplane.

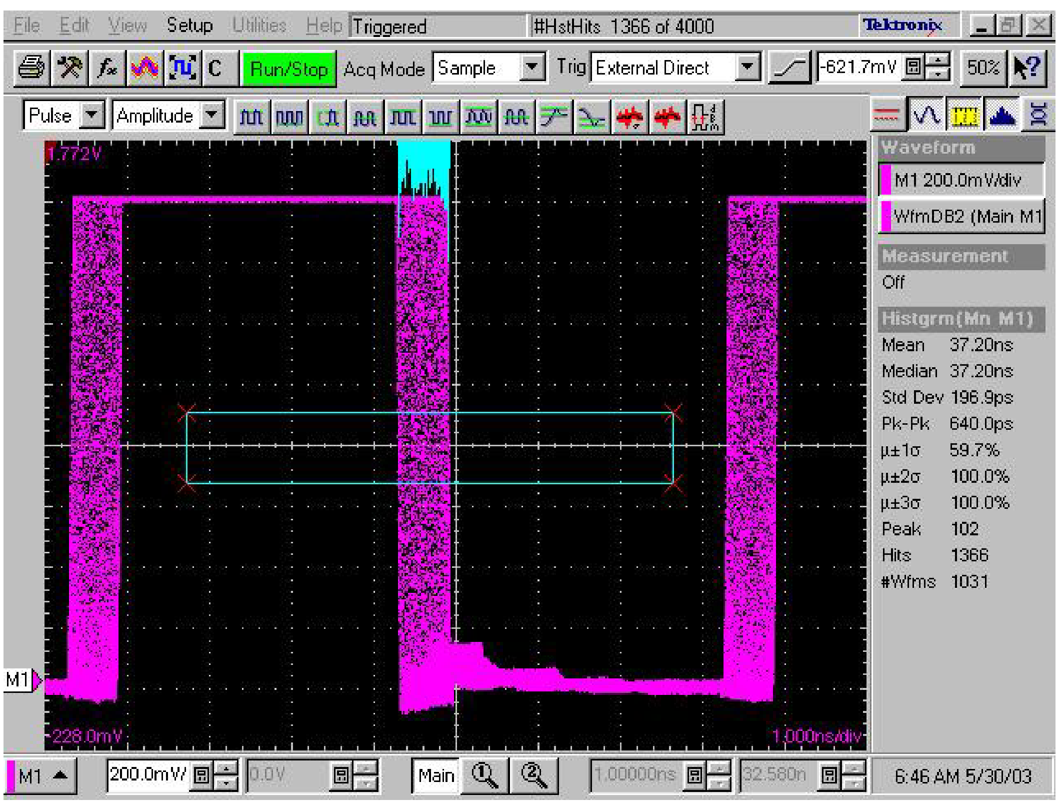

Figure 1: Reference Clock Signal with Large Amount of Jitter

1 Clock Jitter Transfer

First, the transmit characteristic was investigated. The clock jitter transfer plot shows how much jitter gets transferred from the GTXclk into the serial output data stream. The transfer function is highly dependent on the internal PLL, which basically acts like a low-pass filter for jitter on the GTXclk.

For this experiment, the TLK2521 was configured as shown in Figure 2 and set up to transmit the sync-pattern. Since the sync-pattern (10x1, 10x0) has only one fundamental frequency (PRBS pattern has multiple), it makes it easier to measure the jitter content and frequencies. The jitter on the GTXclk as well as the jitter on the serial output data stream was measured with a SIA3000 from Wavecrest.

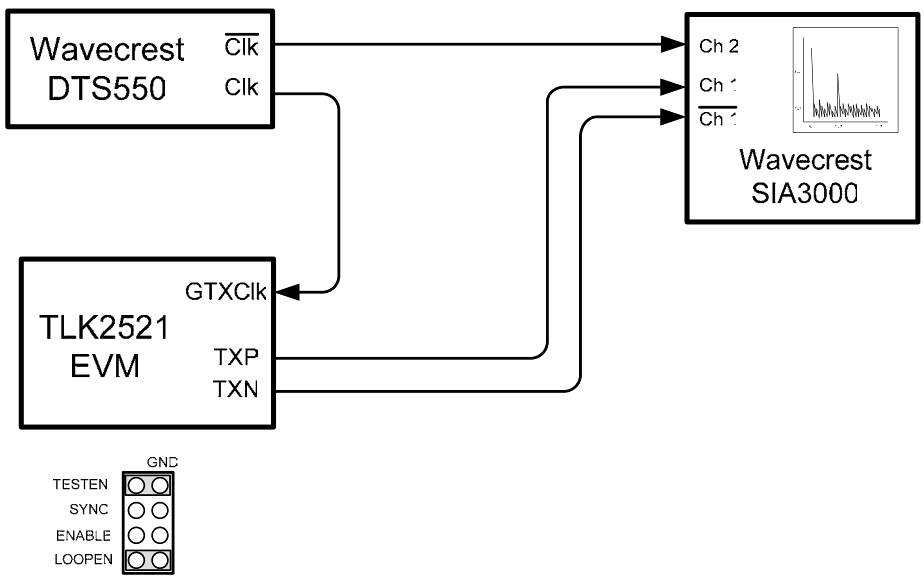

Figure 2: Test Setup for the Clock Jitter Transfer Measurements

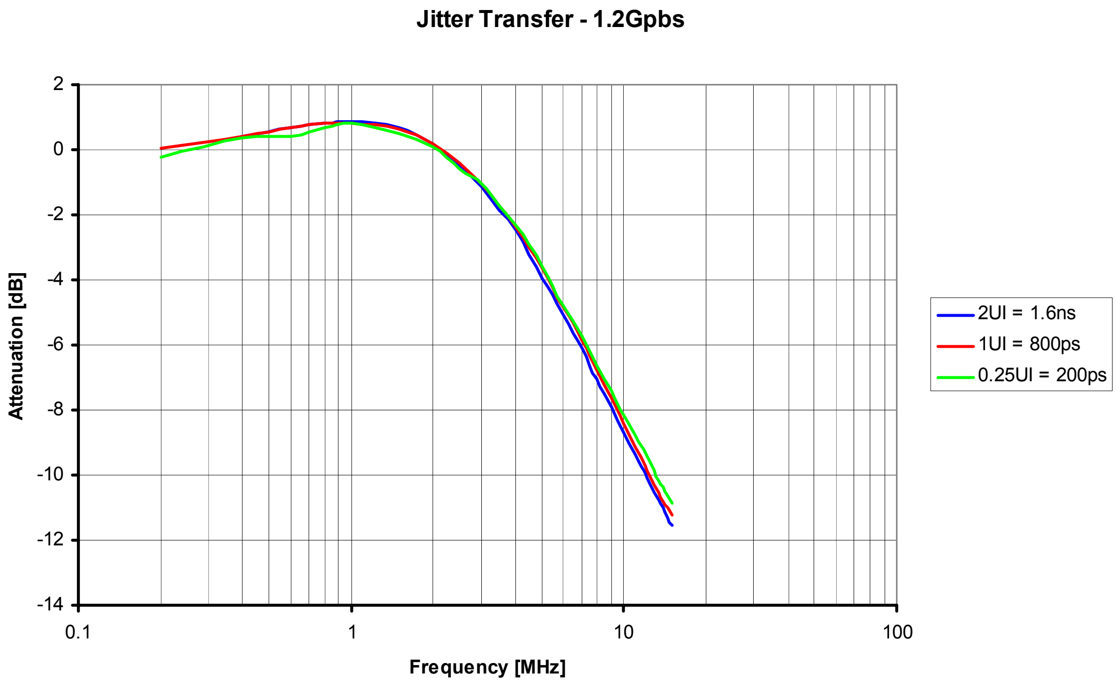

Figure 3: Refclk Jitter Transfer at 1.2 Gbps

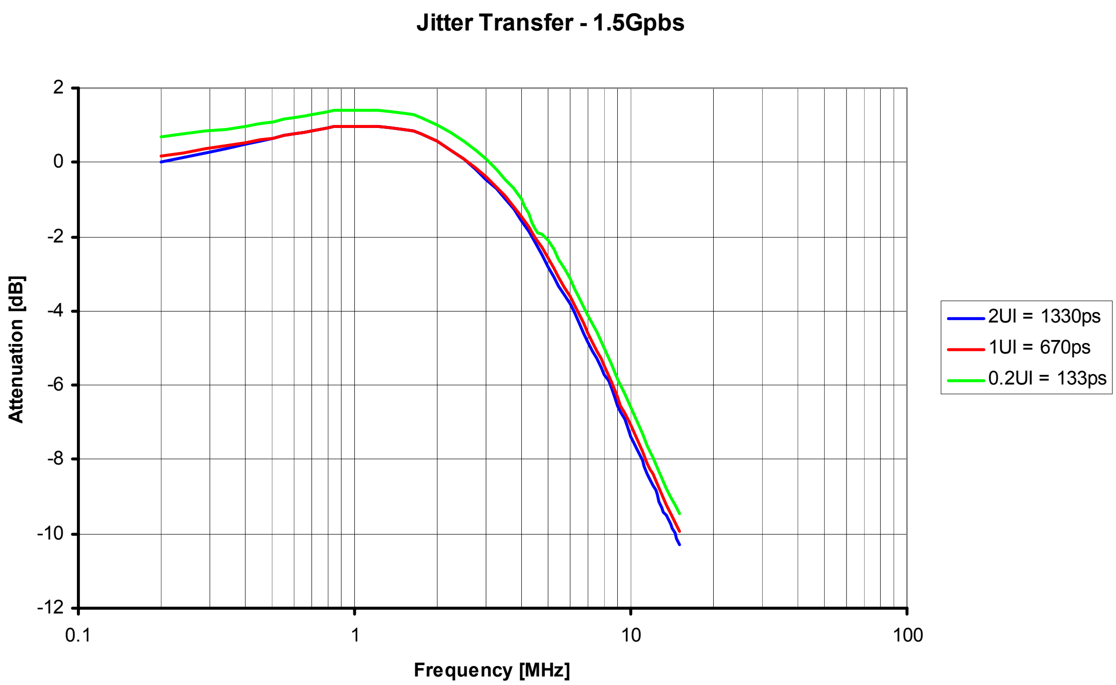

Figure 4: Refclk Jitter Transfer at 1.5 Gbps

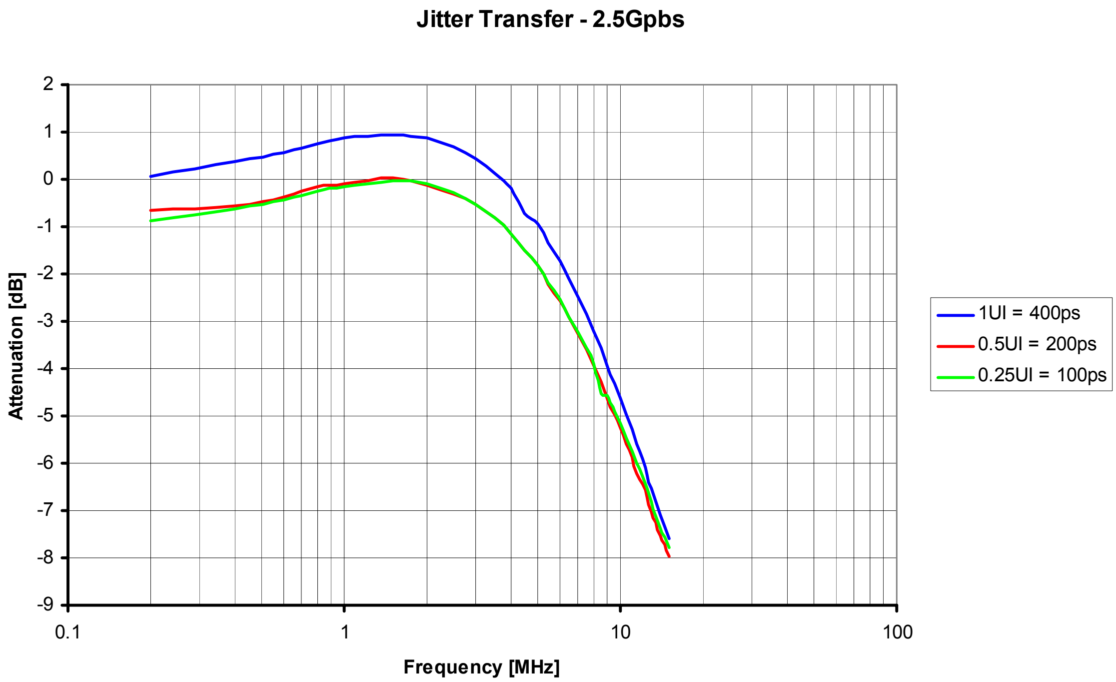

Figure 5: Refclk Jitter Transfer at 2.5 Gbps

Measurement Results

The clock jitter transfer plots at 1.2, 1.5, and 2.5 Gbps clearly show the low-pass filter characteristic of the internal PLL. The plots can be divided in three parts:

- Low frequency: the jitter gets passed straight through the PLL without any amplification or attenuation (0dB).
- Jitter in the PLL bandwidth (~1 MHz for 1.2 and 1.5 Gbps, ~2 MHz for 2.5 Gbps): the jitter gets slightly amplified (1-2 dB).
- High frequency jitter: The PLL attenuates the jitter with -20 dB/dec.

The PLL bandwidth shifts as the data rates vary. For the lower data rates (around 1.25 Gbps), the PLL bandwidth is around 1 MHz while the higher data rates around 2.5 Gbps, the bandwidth is around 2 MHz. This effect can also be observed in the jitter transfer plots.

In order to improve the serial data eye and reduce the transmit output jitter, a very low jitter clock or a clock with low jitter in the PLL bandwidth has to be provided to the GTXclk.

2 Clock Jitter Tolerance

Previous measurements showed that certain jitter frequencies can be filtered out. There are two different kinds of clock jitter, random jitter (RJ) and deterministic jitter (DJ). Random jitter is purely Gaussian. It does not have a frequency associated and therefore can not be filtered out by the internal PLL. Deterministic jitter, on the other hand, always has a certain frequency and therefore can be attenuated by the PLL if it is in the right frequency range.

In order to determine the clock jitter tolerance, typical customer setups (e.g. 36in FR4 backplane or 10m Cat5 cable) were investigated. The TLK2521 was configured to internal PRBS mode (PRBS 2^{23}-1) and the serial output was looped back to itself to mimic a synchronous system with the same clock jitter supplied to every device. In two separate tests, RJ and DJ on the GTXclk were increased until the PRBSpass pin indicated bit errors on the serial receiver.

For the RJ test, the HP noise generator was set up to output white noise (0-15MHz) and the amount of RJ could be adjusted. The sinusoidal frequency modulation of the HP noise generator was used to generate DJ. Frequency and amplitude of the deterministic jitter could be adjusted up to 15 MHz.

The results of these tests should give the system designer an idea of how much Refclk jitter can be tolerated by the TLK2521 in certain setups.

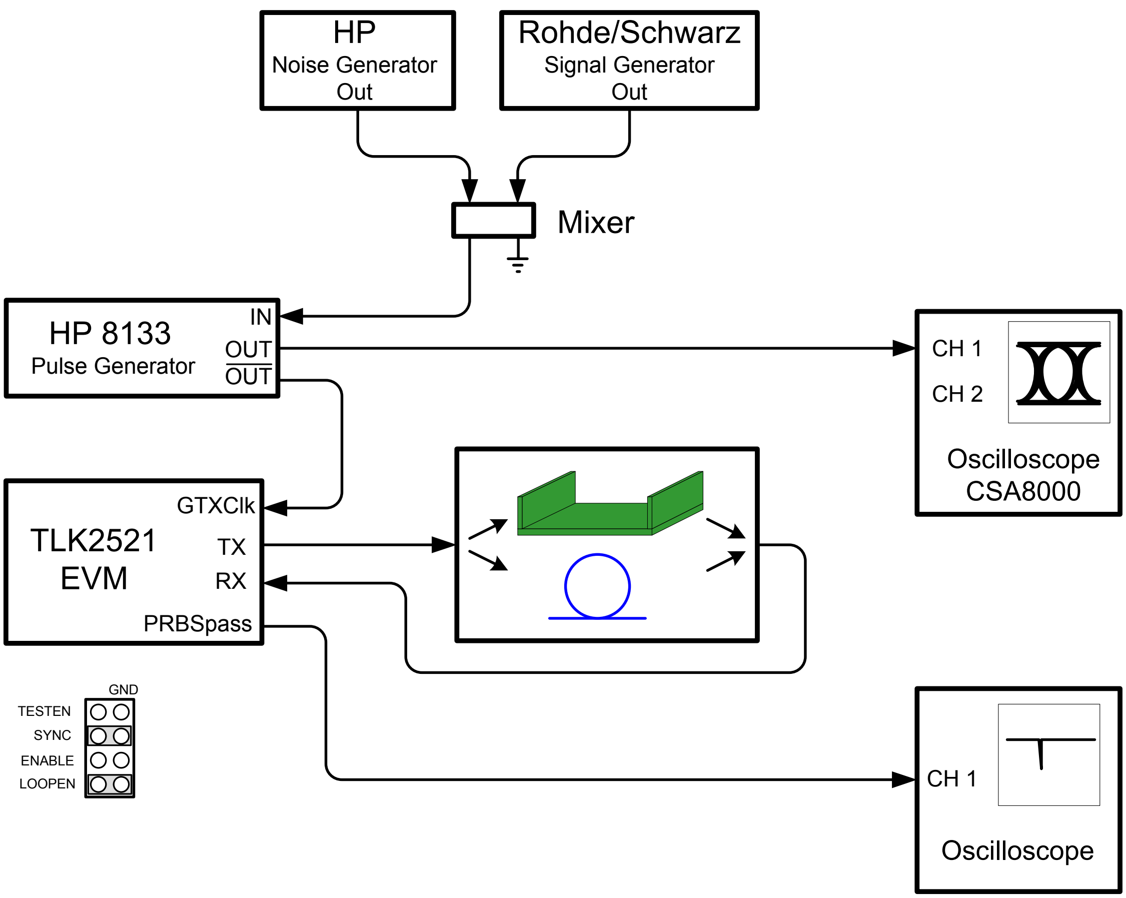

Figure 6: Setup for Refclk Jitter Tolerance Measurements

2.1 Random Jitter - RJ

The first test investigates the RJ and its impact on different applications. The RJ (white noise) from the HP noise generator was increased until the PRBSpass pin of the TLK2521 indicated bit errors.

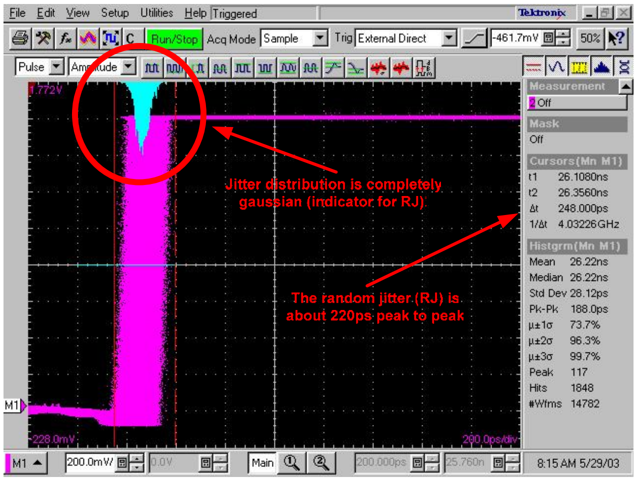

Figure 7: Random Jitter Distribution on the Refclk

Measurement Results

The chart in Figure 8 demonstrates very clearly that the more jitter is on the serial input signal, the less RJ can be tolerated on the GTXclk to still recover the data without bit errors. Transmission media like Cat5 cable have a much higher signal attenuation and jitter generation than the Twinax cable and so allow less jitter on the GTXclk.
Furthermore the graph also shows that at low data rates, the clock jitter tolerance is far bigger than at higher data rates. The signal period is bigger at lower data rates and so more jitter is necessary to *close* the data eye than at higher data rates.

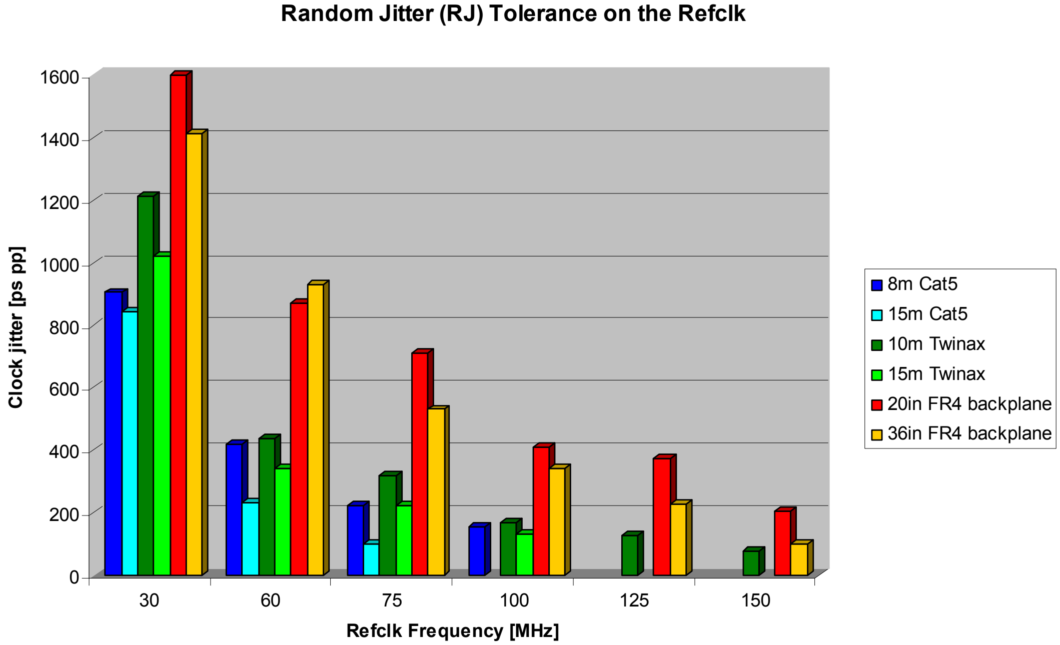

Figure 8: Random Jitter Tolerance on the Refclk for Specific Applications

2.2 Deterministic Jitter - DJ

The next test setup focuses on deterministic jitter (DJ) on the reference clock. In real-life system applications, deterministic jitter appears more often than excessive amounts of jitter. A lot of times, clock oscillators or PLLs create artifacts of the desired frequency (0.5x, 2x, 4x…), which shows up in the reference clock signal.

The maximum amount of deterministic jitter was measured for several typical customer setups. As described previously, the TLK2521 was set up in internal PRBS mode. Then the jitter frequency was swept across the PLL bandwidth and the jitter amplitude was increased until the PRBSpass pin indicated bit errors.

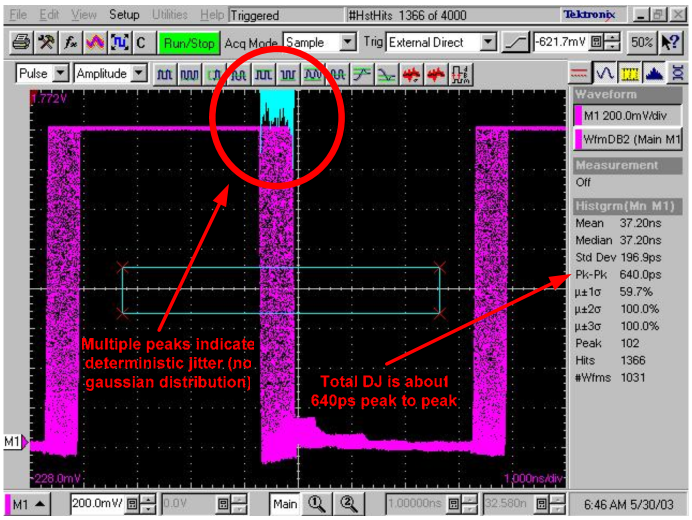

Figure 9:
Deterministic jitter has a non-Gaussian distribution and is clearly visible with the histogram function of the oscilloscope.

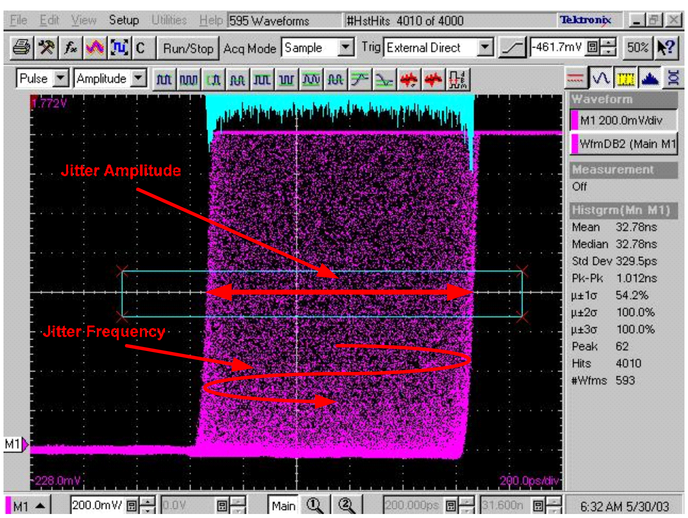

Figure 10:
On the HP noise generator, the amplitude and the frequency were adjusted for the sine wave frequency modulation.
The amplitude determines the total amount of jitter (jitter amplitude) while the modulation frequency sets the *speed* of the moving clock edges.

Measurement Results

The following graphs show the maximum clock jitter tolerance for specific system applications. The application should work if the total jitter of the Refclk source (clock oscillator/FPGA and clock buffer) is less than the values in the charts.

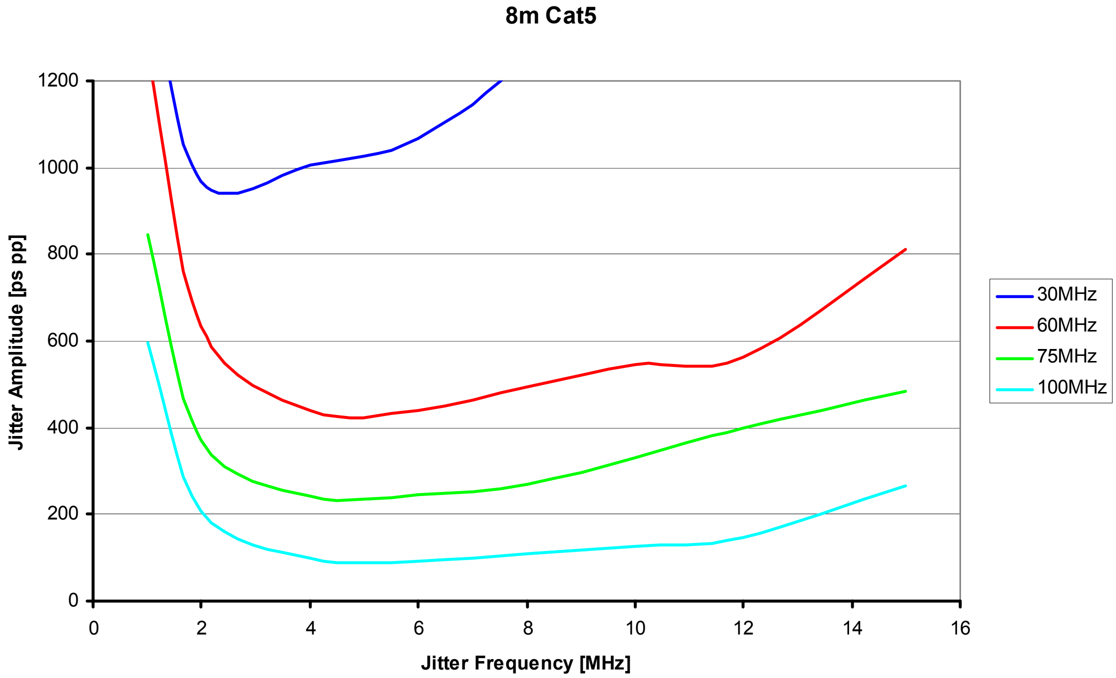

Figure 11: Maximum Amount of Deterministic Jitter on the Refclk Transmitting over 8-m Cat5 Cable

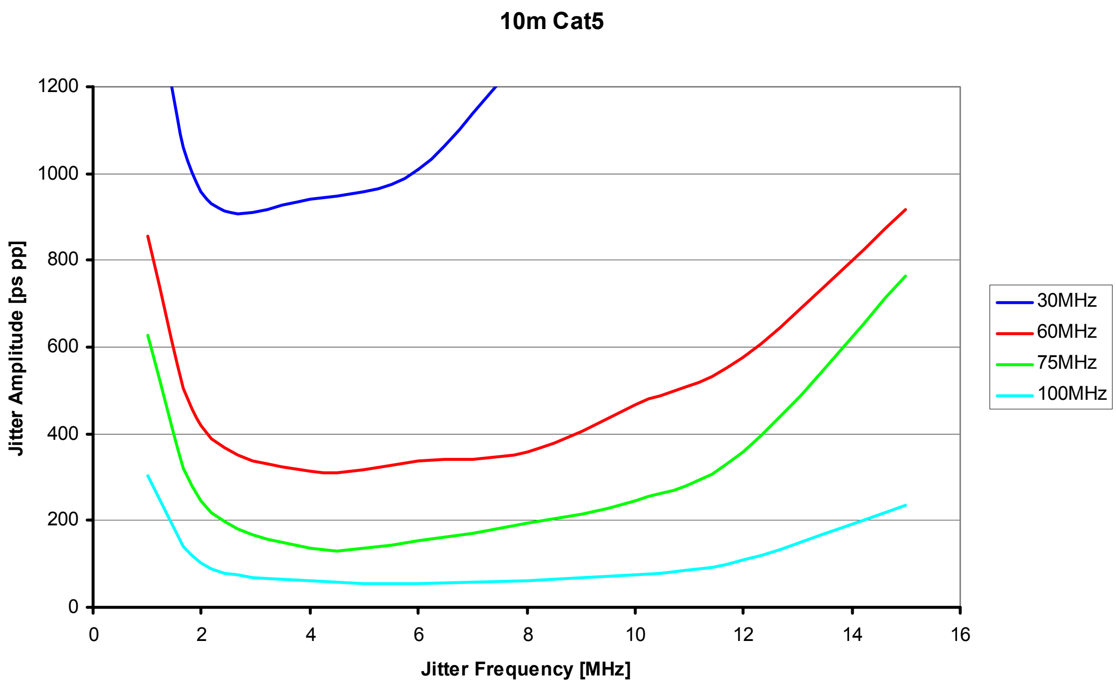

Figure 12: Maximum Amount of Deterministic Jitter on the Refclk Transmitting over 10-m Cat5 Cable

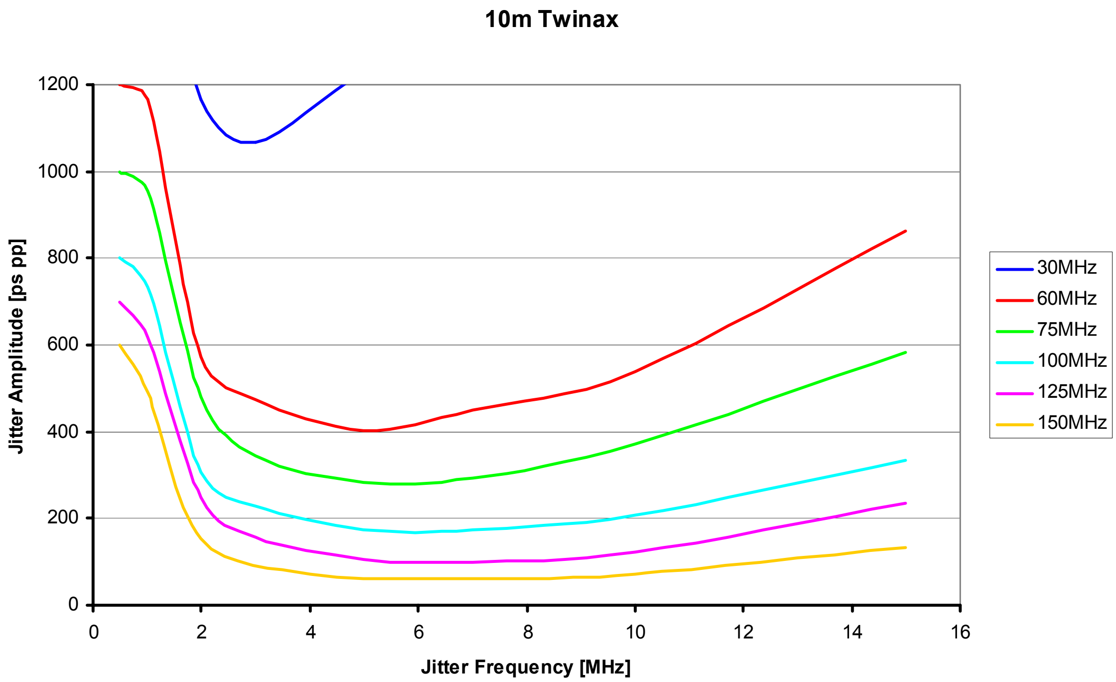

Figure 13: Maximum Amount of Deterministic Jitter on the Refclk Transmitting over 10-m Twinax Cable

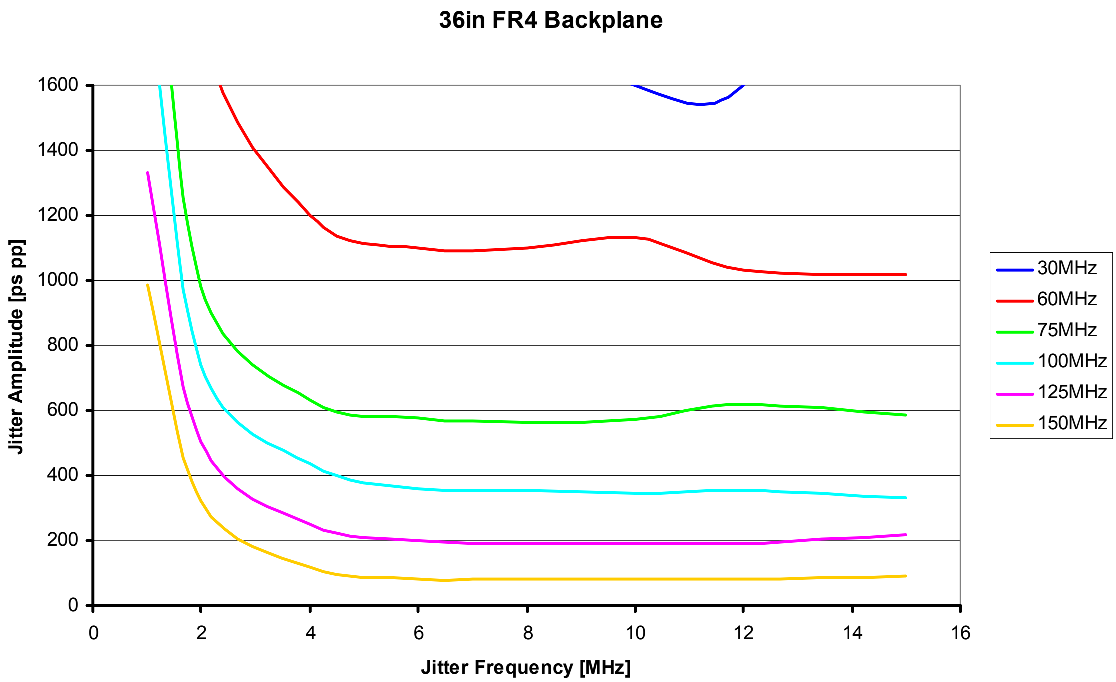

Figure 14: Maximum Amount of Deterministic Jitter on the Refclk Transmitting over 36-inch of FR4

Analysis of Refclk Jitter Tolerance Results

The maximum reference clock jitter is illustrated for four different transmission media. As expected, the minimum for each setup is around the PLL bandwidth of the TLK2521.
As the charts show, a lot of low frequency jitter can be tolerated because receiver is able track that jitter which the transmitter just passes through. High-frequency reference clock jitter on the other hand gets attenuated by the internal PLL.

Summary

The main purpose of this application report is to demonstrate the performance of the TLK2521 in specific system applications when large amounts of jitter are present on reference clock.

It shows the PLL bandwidth at different data rates and the resulting clock jitter transfer function. Furthermore, it gives the system designer an idea of how much clock jitter the TLK2521 can handle in specific setups like a transmission over 36-inch of backplane.

This document also puts the 40 ps, mentioned in the data sheet, in the right perspective. The 40 ps of clock jitter are the limit for high data rates and large amounts of jitter on the serial input data stream. The measurement results show very clearly that for lower data rates and/or a serial input signal with low jitter, the TLK2521 can tolerate a much larger amount of clock jitter (~ 1 ns for 36-inch FR4 at 60 MHz).

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265