

# Programming the UCD9080

Dale Wellborn PMP - Systems Power

#### **ABSTRACT**

The operation of the Texas Instruments UCD9080 is configured by programmable (flash) memory within the device. The memory can be written and read using a command protocol over a standard  $I^2C$  bus interface. This document provides the hardware and software details necessary to program the UCD9080 with the configuration data.

See the UCD9080 data sheet (SLVS692) for a complete description of the device.

#### 1 Hardware

### 1.1 Package

RHB (S-PQFP-N32), 32-pin Plastic Quad Flatpack

# 1.2 Hardware/Device Pinning

Pin Number	Pin Name	Connection/Description	
1	Vss	Ground	
2	NC	Do Not Connect	
3	XIN	Vcc	
4	NC	Vss	
5	RST	Device reset	
6	MON1	Do Not Connect	
7	MON2	Do Not Connect	
8	MON3	Do Not Connect	
9	MON6	Do Not Connect	
10	EN4	Do Not Connect	
11	EN3	Do Not Connect	
12	EN5	Do Not Connect	
13	EN6	Do Not Connect	
14	EN7	Do Not Connect	
15	MON7	Do Not Connect	
16	MON8	Do Not Connect	
17	NC	Vss	
18	MON4	Do Not Connect	
19	MON5	Do Not Connect	
20	NC	Vss	
21	SDA	I <sup>2</sup> C data	
22	SCL	I <sup>2</sup> C clock	



Pin Number	Pin Name	Connection/Description
23	EN1	Do Not Connect
24	EN2	Do Not Connect
25	EN8/ADDR1/GPO1	Vss
26	ADDR2/GPO2	Vss
27	ADDR3/GPO3	Vss
28	ADDR4/GPO4	Vss
29	TEST	Vss
30	Vcc	3.3 V
31	NC	Vss
32	ROSC	100K to Vcc, or 1.75 V

#### 1.3 **Detailed Pin Descriptions**

- RST: Device reset. Input. Active low. Minimum pulse width: 2 µs. The UCD9080 can process commands on the I<sup>2</sup>C bus 15mSec following the negation of RST.
- SDA: I<sup>2</sup>C Serial Data. Input/Output. The SDA complies with the Phillips specification for an I<sup>2</sup>C Slave device. An external pullup resistor is required on this pin. The specification for the Philips I<sup>2</sup>C bus can
  - http://www.semiconductors.philips.com/acrobat download/literature/9398/39340011.pdf
- **SCL:** I<sup>2</sup>C Serial Clock. Input. The SCL complies with the Phillips specification for an I<sup>2</sup>C Slave device. An external pullup resistor is required on this pin. The SCL has a minimum frequency of 10 kHz and a maximum frequency of 100 kHz.
- **ADDRx:** Device Address. Input. The Vss levels on these four pins locate the device at an I<sup>2</sup>C address of 0x60.
- ROSC: Oscillator. Input. This pin controls the device operating speed. Either a 100K pullup to Vcc is required, or 1.75 V can be applied to this pin.

#### 2 Software

Data File Format: The configuration data is supplied in standard Intel hexadecimal format. Beginning at address 0x1080, 128 bytes of data are programmed and beginning at address 0xE000, 512 bytes of data are programmed . Appendix A presents a sample configuration data file.

**I<sup>2</sup>C Transactions:** Programming the device with the configuration data requires I<sup>2</sup>C Write transactions; commands and configuration data are written to the device. Reading the configuration data from the device requires I<sup>2</sup>C Write transactions and I<sup>2</sup>C Read transactions; "read" commands are written, and the configuration data is read. Reading the configuration data can be used to verify the correct programming of the data following a write data operation. Appendix B presents the format of the I<sup>2</sup>C Write and Read transactions. Appendix C presents the set of pseudo I<sup>2</sup>C transactions necessary to write and read the sample configuration data presented in Appendix A.

Note: The I<sup>2</sup>C write and read data transactions presented in Appendix B assume a maximum data transfer block size of 32 bytes. Each block is preceded by the target address. The UCD9080 is capable of supporting blocks sized from 2 bytes to 512 bytes., in multiples of two bytes (i.e., a 16-bit word). When writing data, it is critical that all 128 bytes of the data beginning at address 0x1080 are written, and that all 512 bytes of data beginning at address 0xE000 are written (i.e., it is not permitted to do a partial write of a data area).

Device Identification: An I2C Read transaction can be used to read register 0x27; a value of zero in the second byte read indicates a UCD9080.



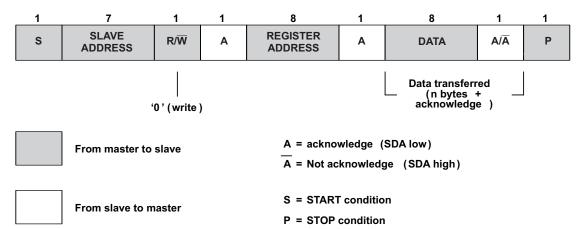
#### Appendix A A Sample Configuration Data File

:20108000546578617320496E737472756D656E7473205543443930383020382D4368616EB3 :2010A0006E656C20506F77657220537570706C792053657175656E63657220616E64204D8C  $: 20 \\ \pm 00 \\$  $: 20 \\ \pm 00 \\$ :20E16000000000C000C000C0042008200418021808181018201810200020202040208020CD :0000001FF

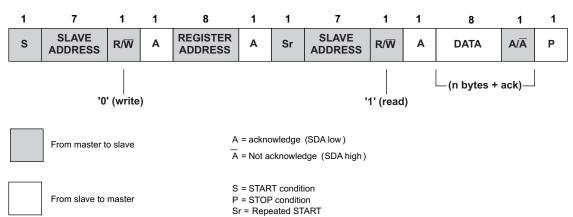


# Appendix B I<sup>2</sup>C Write and Read Transaction Formats

# **B.1** I<sup>2</sup>C Write Transaction



# **B.2** I<sup>2</sup>C Read Transaction





# Appendix C Pseudo I<sup>2</sup>C Write and Read Transactions

A pseudo I<sup>2</sup>C transaction code follows. The user should ensure that data written to the user configuration area of the device (0xE000-0xE1FF) matches that specified in the data sheet except for the user-unique configurable areas.

Note

In the following pseudo  $I^2C$  transactions, a Data Length is specified. This value is not directly part of the  $I^2C$  transaction. Rather, its value is used within the Master to count the data transferred after which a NACK is generated to the slave to stop the transaction.

#### C.1 UCD9080 I<sup>2</sup>C Transactions for Writing User Data and PARAMS

#### C.1.1 I<sup>2</sup>C Write (Open Flash Memory)

Device Address: 0x60 Register Address: 0x2E

Data Length: 1 Data: 0x02

#### C.1.2 $I^2$ C Write (Base Address: 0x1080)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x80 0x10

# C.1.3 I<sup>2</sup>C Write (Unlock and Erase Flash Memory)

Device Address: 0x60 Register Address: 0x32

Data Length: 2 Data: 0xDC 0xBA

#### C.1.4 I<sup>2</sup>C Write (Data Address: 0x1080)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x80 0x10

#### C.1.5 $I^2$ C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

Data: 0x54 0x65 0x78 0x61 0x73 0x20 0x49 0x6E 0x73 0x74 0x72 0x75 0x6D 0x65 0x6E 0x74 0x73 0x20

0x55 0x43 0x44 0x39 0x30 0x38 0x30 0x20 0x38 0x2D 0x43 0x68 0x61 0x6E

### C.1.6 I<sup>2</sup>C Write (Data Address: 0x10A0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xA0 0x10



#### C.1.7 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32 Data Length: 32

Data: 0x6E 0x65 0x6C 0x20 0x50 0x6F 0x77 0x65 0x72 0x20 0x53 0x75 0x70 0x70 0x6C 0x79 0x20 0x53

0x65 0x71 0x75 0x65 0x6E 0x63 0x65 0x72 0x20 0x61 0x6E 0x64 0x20 0x4D

#### C.1.8 I<sup>2</sup>C Write (Data Address: 0x10C0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xC0 0x10

#### C.1.9 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.1.10 $I^2$ C Write (Data Address: 0x10E0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xE0 0x10

#### C.1.11 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.1.12 I<sup>2</sup>C Write (Base Address: 0xE000)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x00 0xE0

#### C.1.13 I<sup>2</sup>C Write (Unlock and Erase the FLASH)

Device Address: 0x60 Register Address: 0x32

Data Length: 2 Data: 0xDC 0xBA

#### C.1.14 I<sup>2</sup>C Write (Data Address: 0xE000)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x00 0xE0



#### C.1.15 *I*<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.1.16 I<sup>2</sup>C Write (Data Address: 0xE020)

Device Address: 0x60 Register Address: 0x30

Length: 2 Data: 0x20 0xE0

## **C.1.17** *I*<sup>2</sup>**C** Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.1.18 $I^2$ C Write (Data address: 0xE040)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x40 0xE0

#### C.1.19 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

0x00 0x00 0x00 0x00 0x00 0x00 0xFF 0x00 0x00 0x00 0x00 0x00 0x00 0x02

#### C.1.20 I<sup>2</sup>C Write (Data Address: 0xE060)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x60 0xE0

#### C.1.21 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.1.22 I<sup>2</sup>C Write (Data Address: 0xE080)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x80 0xE0



#### C.1.23 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

Data: 0x50 0x51 0x52 0x53 0x54 0x55 0x56 0x57 0x00 0x49 0x4A 0x4B 0x01 0x00 0x01 0x04 0x01 0x04

0x05 0x06 0x00 0x00 0x00 0x00 0x05 0xE0 0x05 0xA0 0x32 0xE0 0x33 0xE0

#### C.1.24 I<sup>2</sup>C Write (Data Address: 0xE0A0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xA0 0xE0

## C.1.25 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

0xFF 0x7F 0xFF 0x7F 0xFF 0x7F 0xFF 0x7F 0xFF 0x7F 0xFF 0x7F 0xFF 0x7F

#### C.1.26 I<sup>2</sup>C Write (Data Address: 0xE0C0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xC0 0xE0

#### C.1.27 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.1.28 I<sup>2</sup>C Write (Data Address: 0xE0E0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 : 0xE0 0xE0

#### C.1.29 I<sup>2</sup>C Write (Data

Device Address: 0x60 Register Address: 0x32

Data Length: 32

0x00 0x00

#### C.1.30 I<sup>2</sup>C Write (Data Address: 0xE100)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x00 0xE1



#### **C.1.31** *I*<sup>2</sup>**C** *Write* (*Data*)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

Data: 0x7F 0x00 0x01 0x00 0x02 0x00 0x04 0x00 0x08 0x00 0x10 0x00 0x20 0x00 0x40 0x00 0x00

#### C.1.32 I<sup>2</sup>C Write (Data address: 0xE120)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x20 0xE1

## **C.1.33** *I*<sup>2</sup>**C** Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

Data: 0x00 0x04 0x00

0xA0 0x0F 0xA0 0x0F 0xA0 0x0F 0xA0 0x0F 0xA0 0x0F 0xA0 0x0F 0xA0 0x0F

#### C.1.34 I<sup>2</sup>C Write (Data Address: 0xE140)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x40 0xE1

#### C.1.35 *I*<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

Data: 0x10 0x00 0xFF 0xC0

0xFF 0xC1 0xFF 0xC2 0xFF 0xC3 0xFF 0xC4 0xFF 0xC5 0xFF 0xC6 0xFF 0xC7

#### C.1.36 I<sup>2</sup>C Write (Data Address: 0xE160)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x60 0xE1

#### **C.1.37** *I*<sup>2</sup>**C** Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

Data: 0x00 0x00 0x00 0xC0 0x00 0xC0 0x00 0xC0 0x04 0x20 0x08 0x20 0x04 0x18 0x02 0x18 0x08 0x18

0x10 0x18 0x20 0x18 0x10 0x20 0x00 0x20 0x20 0x20 0x40 0x20 0x80 0x20

# C.1.38 I<sup>2</sup>C Write (Data Address: 0xE180)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x80 0xE1



#### C.1.39 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

Data: 0x00 0x00 0x00 0x04 0x94 0x02 0xF2 0x08 0x10 0x03 0x05 0xC0 0x40 0x00 0xFF 0x08 0x05 0x00

#### C.1.40 I<sup>2</sup>C Write (Data Address: 0xE1A0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xA0 0xE1

## **C.1.41** *I*<sup>2</sup>**C** Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.1.42 I<sup>2</sup>C Write (Data Address: 0xE1C0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xC0 0xE1

#### C.1.43 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.1.44 I<sup>2</sup>C Write (Data Address: 0xE1E0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xE0 0xE1

#### C.1.45 I<sup>2</sup>C Write (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

# C.1.46 I<sup>2</sup>C Write (Lock and Close the FLASH)

Device Address: 0x60 Register Address: 0x2E

Data Length: 1 Data: 0x00



# C.2 UCD9080 I<sup>2</sup>C Transactions for Reading User Data and PARAMS

#### C.2.1 I<sup>2</sup>C Write (Data address: 0x1080

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x80 0x10

### C.2.2 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32 Data Length: 32

#### C.2.3 I<sup>2</sup>C Write (Data Address: 0x10A0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xA0 0x10

#### C.2.4 $I^2$ C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.5 I<sup>2</sup>C Write (Data Address: 0x10C0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xC0 0x10

#### C.2.6 $I^2$ C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.7 I<sup>2</sup>C Write (Data Address: 0x10E0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xE0 0x10

#### C.2.8 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

### C.2.9 I<sup>2</sup>C Write (Data Address: 0xE000)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x00 0xE0



#### C.2.10 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.11 I<sup>2</sup>C Write (Data Address: 0xE020)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x20 0xE0

### 

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.13 I<sup>2</sup>C Write (Data Address: 0xE040)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x40 0xE0

#### C.2.14 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.15 I<sup>2</sup>C Write (Data Address: 0xE060)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x60 0xE0

#### 

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.17 I<sup>2</sup>C Write (Data Address: 0xE080)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x80 0xE0

#### C.2.18 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

### C.2.19 I<sup>2</sup>C Write (Data Address: 0xE0A0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xA0 0xE0



#### C.2.20 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.21 I<sup>2</sup>C Write (Data Address: 0xE0C0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xC0 0xE0

### C.2.22 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

# C.2.23 I<sup>2</sup>C Write (Data Address: 0xE0E0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xE0 0xE0

#### C.2.24 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.25 I<sup>2</sup>C Write (Data Address: 0xE100)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x00 0xE1

#### C.2.26 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.27 I<sup>2</sup>C Write (Data Address: 0xE120)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x20 0xE1

#### 

Device Address: 0x60 Register Address: 0x32

Data Length: 32

### C.2.29 I<sup>2</sup>C Write (Data Address: 0xE140)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x40 0xE1

#### C.2.30 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.31 I<sup>2</sup>C Write (Data Address: 0xE160)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x60 0xE1

# 

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.33 I<sup>2</sup>C Write (Data Address: 0xE180)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0x80 0xE1

#### C.2.34 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.35 I<sup>2</sup>C Write (Data Address: 0xE1A0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xA0 0xE1

#### 

Device Address: 0x60 Register Address: 0x32

Data Length: 32

#### C.2.37 I<sup>2</sup>C Write (Data Address: 0xE1C0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xC0 0xE1

#### C.2.38 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32

Data Length: 32

### C.2.39 I<sup>2</sup>C Write (Data Address: 0xE1E0)

Device Address: 0x60 Register Address: 0x30

Data Length: 2 Data: 0xE0 0xE1



# C.2.40 I<sup>2</sup>C Read (Data)

Device Address: 0x60 Register Address: 0x32 Data Length: 32

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