

5 A Buck Converter Using the TPS6420x Family of Step Down Controllers

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ABSTRACT

This application report describes a circuit to boost the output current of a TPS6420x buck stepdown switching power supply controller. With the addition of a simple driver circuit, the controllers can be configured to provide output currents above the 3-A rating in the datasheet.

In a typical TPS6420x application, the signal SW drives the gate of the PMOS FET. A power FET capable of handling more than 3 A generally has a large gate capacitance. For a high-speed switching circuit such as a switching power supply, a brief, but high-current transition is required to charge and discharge the gate capacitance. The SW gate-drive current is the limiting factor for output current in a TPS6420x-based design. To date, only a few FETs, such as the Si5475, have low enough gate capacitances to enable a TPS6420x circuit to deliver up to 3 A. Higher output currents require higher gate-drive currents.

The current necessary to drive much larger power FETs can be supplied by a drive-boost circuit consisting of two complementary bipolar transistors (Q1), as shown in Figure 1. Because the bipolar transistors in Q1 only supply the transient currents necessary to handle the gate capacitance of Q2, they do not dissipate appreciable heat, and only require a small package. In the implementation shown in Figure 1, the bipolar transistors are in a single SOT23-6 package (ZXTD6717E6).

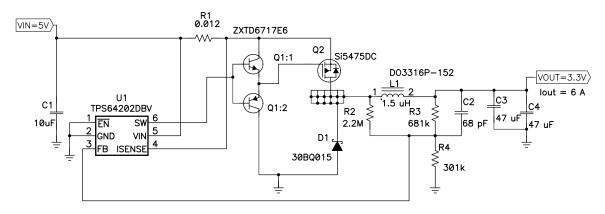


Figure 1. TPS64202 Configured to Provide 3.3 V @ 5 A

The bipolar transistors allow the TPS6420x circuit in the design example to provide up to 5 A of total output current. Higher output current can be achieved with a larger Q2 FET, D1 diode, and/or inductor. See the design example for complete design equations.



In summary, since the control topology for the TPS6420x family relies on output ripple being fed back to the error amplifier, the datasheet design equations recommend a large (> 4.7 μ H) inductor and an output capacitor with an ESR between 50 m Ω and 100 m Ω . However, at higher output currents, the output ripple created by the product of the inductor ripple current and output-capacitor ESR is too large for a practical buck converter. Moreover, since the current rating of an inductor varies inversely to its inductance value, more low-value (< 4.7 μ H) inductors are available with high current ratings. For this application, a 1.5 μ H inductor, ceramic output capacitors, and resistor R2 were used to provide a practical, low output-ripple buck converter.

Figure 2 shows the efficiency of the circuit.

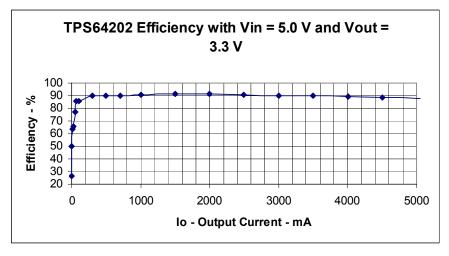


Figure 2. Figure 2 – Efficiency

Figure 3 shows the normalized load regulation.

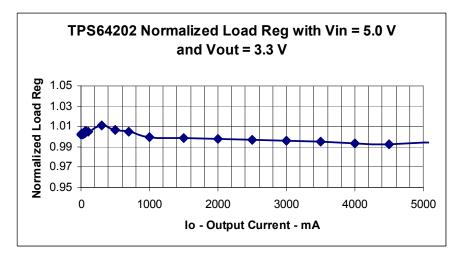


Figure 3. Normalized Load Regulation

Figure 4 shows the output ripple (CH1) at 5 A (CH4)

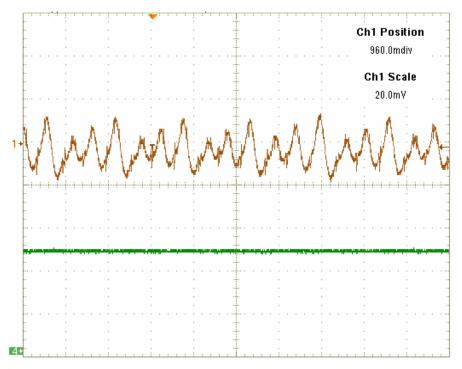


Figure 4. Output Voltage Ripple at I_{OUT} = 5 A

Design Example

This example describes an application with V_{IN} = 5.0V + 5%, T_Amax = 55°C and using ceramic output capacitors to generate 3.3 V and 5 A.

1. Calculate the sense resistor, R1, for the current limit:

$$\mathsf{R}_{(\mathsf{ISENSE})} = \frac{\mathsf{V}_{(\mathsf{ISENSE})\mathsf{MIN}}}{1.3 \times \mathsf{I}_{\mathsf{O}\;\mathsf{MAX}}} = \frac{90 \; \mathsf{mV}}{1.3 \times 5} = 0.014 \; \Omega$$

The next lower standard value (12 m Ω) is selected. If the R_{DS(ON)} of the PMOS FET is used instead of a current sense resistor, then a PMOS with R_{DS(ON)} less than this amount must be selected.

2. Calculate the resistors for the output voltage divider using VFB = 1.21V.

Choose R4 = 301 k Ω , then using datasheet equation 5 below, R2||R3 = 520 k Ω

$$R2 \|R3 = \left(\frac{V_{O} - V_{FB}}{V_{FB}}\right) \times R4 = \frac{(3.3 \text{ V} - 1.21 \text{ V}) \times (301 \text{ k}\Omega)}{1.21 \text{ V}} = 520 \text{ k}\Omega$$

Set R2 = 2.2 M Ω to minimize I $_{Q}$, then use modifications of data sheet equations 28 and 29 to compute R3 = 681 k Ω

$$R3 = \frac{1}{\frac{1}{R2 \| R3} - \frac{1}{R2}} = \frac{1}{\frac{1}{520 \text{ k}\Omega} - \frac{1}{2.2 \text{ M}\Omega}} = 681 \text{ k}\Omega$$

3. Select the external PMOS, Q1.

The minimum input voltage for this application is 5V minus the 5% tolerance, or 4.5V. So, the maximum RMS current through the FET per datasheet equation 11 is

$$I_{(PMOS)RMS} \approx I_{OMAX} \times \sqrt{D_{MAX}} = 5 \text{ A} \times \sqrt{\frac{3.3 \text{ V}}{4.5 \text{ V}}} = 4.3 \text{ A}$$

Per datasheet equation 12, the power dissipation from conduction losses in the FET is

The Si5475, with P_Dmax = 0.7 W at T_A = 85 C, was selected for this application. Otherwise a PMOS with lower $\Gamma_{\text{DS(ON)}}$, and/or a bigger package and therefore lower power dissipation specification, must be used.

4. Select the external diode, D1.

The datasheet assumes that the device only provides currents less than or equal to 3A and uses only the average current through the diode $(I_0 \times 1 - D_{MIN} = 5 \times (1 - \frac{3.3}{5.5}) = 2.0 \text{ A})$ to select the

diode based on its current rating. At higher currents, it is best to also consider the diode's maximum power dissipation. Average thermal-power calculations require the instantaneous voltage drop across the diode at the maximum output current per the diode's datasheet curves. Average thermal power in the diode is computed using this equation:

$$P_{\text{THERMAL}} = I_{\text{OMAX}} \times V_{\text{SCHOTTKY}} \times (1 - D_{\text{MIN}}) = 5 \text{ A} \times 0.4 \text{ V} \times \left(1 - \frac{3.3 \text{ V}}{5.5 \text{ V}}\right) = 0.8 \text{ W}$$

where $V_{(\text{SCHOTTKY})}$ is the voltage drop across the 30BQ015, 3-A Schottky diode in SMC package at I_{O} = 5 A.

5. Select the correct TPS64202 option for U1 using application note SLVA160.

6. Determine the maximum inductor ripple current.

The output-voltage ripple per datasheet equation 14 is

 $\Delta V_{P-P} \approx 1.1 \times \Delta I_L \times ESR_{COUT}$

Solving for ΔI_L , assuming ESR_{COUT} \leq 20 m Ω and with a design goal of $\Delta V_{P-P} \leq$ 20 mV, gives the following:

$$\Delta I_L \approx \frac{\Delta V_{P-P}}{1.1 \times \text{ESR}_{COUT}} = \frac{25 \text{ mV}_{P-P}}{1.1 \times 20 \text{ m}\Omega} = 1.13 \text{ A}$$

7. Calculate the inductor value for L1

Using the TPS64202 running in minimum-off-time mode and using a much larger inductor ripple current than would be allowed with larger ESR, non-ceramic output capacitors yields the smallest inductor value as computed by datasheet equation 10:

$$L = \frac{\left[V_{O} + V_{SCHOTTKY} + \left(R_{RL} + I_{OMAX}\right)\right] \times t_{OFFMIN}}{\Delta I_{I}} = \frac{\left[3.3 \text{ V} + 0.4 \text{ V} + 0.20 \Omega \times 5 \text{ A}\right] \times 0.3 \mu \text{S}}{1.13 \text{ A}} = 1.25 \mu \text{H}$$

where R_{RL} is an estimate of the inductor dc resistance.

The next larger value, 1.5 µH, is selected.

8. Select the output capacitors, C2 and C3.

Assuming that the application requires $\Delta V_0 \le 250$ mV for a $\Delta I_0 = 5$ A, datasheet equation 16 computes the necessary ceramic output capacitance.

$$C_{O} = \frac{L \times \Delta {I_{O}}^{2}}{(V_{I} - V_{O}) \times \Delta V_{O}} = \frac{(1.5 \ \mu h) \times (5 \ A)^{2}}{(5 \ V - 3.3 \ V) \times 250 \ mV} = 90 \ \mu F$$

The next larger value, 100 µF, implemented by two 47 µF capacitors in parallel, is selected.

9. Use a feed-forward capacitor, C4, of approximately 68 pF for designs using ceramic output capacitors.

10. Select the input capacitor, C1.

Assuming that the maximum input-voltage ripple $V_{I(RIPPLE)}$ is 100 mV for this application, datasheet equation 7 gives the minimum value for the input capacitor, CI.

$$C_{I,MIN} = \frac{\frac{1}{2}L(\Delta I_L)^2}{V_{I(RIPPLE)} \times V_I} = \frac{\frac{1}{2} \times 1.5 \ \mu H \times 1.13^2}{250 \ mV \times 5 \ V} = 0.8 \ \mu H$$

The minimum required input capacitance of 10 μ F is used.

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