User's Guide

TPS51218 Buck Controller Evaluation Module User's Guide

ABSTRACT

The TPS51218EVM evaluation module (EVM) is used to evaluate the TPS51218, a small-size, single buck controller with adaptive on-time D-CAP™ mode, providing a fixed 1.2-V output at up to 20 A from a 12-V input bus.

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1 Description

The TPS51218EVM is designed to use a regulated 12-V bus to produce a regulated 1.2-V output at up to 20 A of load current. The TPS51218EVM is designed to demonstrate the TPS51218 in a typical, low-voltage application while providing a number of test points to evaluate the performance of the TPS51218.

1.1 Typical Applications

- High-current system converters for server and desktop power
- Switchers and routers
- Embedded computers
- In-vehicle infotainment PCs
- POS terminals
- Point-of-load modules
- Graphics cards
- Industrial control/factory automation PCs

1.2 Features

The TPS51218EVM features:

- 20-A_{DC} steady-state current
- Support prebias output voltage start-up
- 380-kHz switching frequency
- J4 for enable function
- J3 for auto-skip and forced CCM selection
- Convenient test points for probing critical waveforms

2 Electrical Performance Specifications

Table 2-1. TPS51218EVM Electrical Performance Specifications

Parameter	Test Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS					
Voltage range	V_{IN}	8	12	14	V
Maximum input current	V_{IN} = 8 V, I_O = 20 A			3.55	A
No load input current	V_{DC} = 14 V, I_O = 0 A			50	mA
OUTPUT CHARACTERISTICS					
Output voltage, VOUT			1.2		V
Output voltage regulation	Line regulation (V_{DC} = 10 V–14 V)		1.0%		
	Load regulation (V_{DC} = 12 V, I_O = 0 A–20 A)		1.0%		
Output voltage ripple	V_{IN} = 12 V, I_O = 20 A			40	mVpp
Output load current		0		20	A
Output overcurrent			30		A
SYSTEMS CHARACTERISTICS					
Switching frequency			380		kHz
Peak efficiency	V_{IN} = 12 V, 1.2 V/10 A		90.32%		
Full-load efficiency	V_{IN} = 12 V, 1.2 V/20 A		88.64%		
Operating temperature			25		°C

3 Schematic

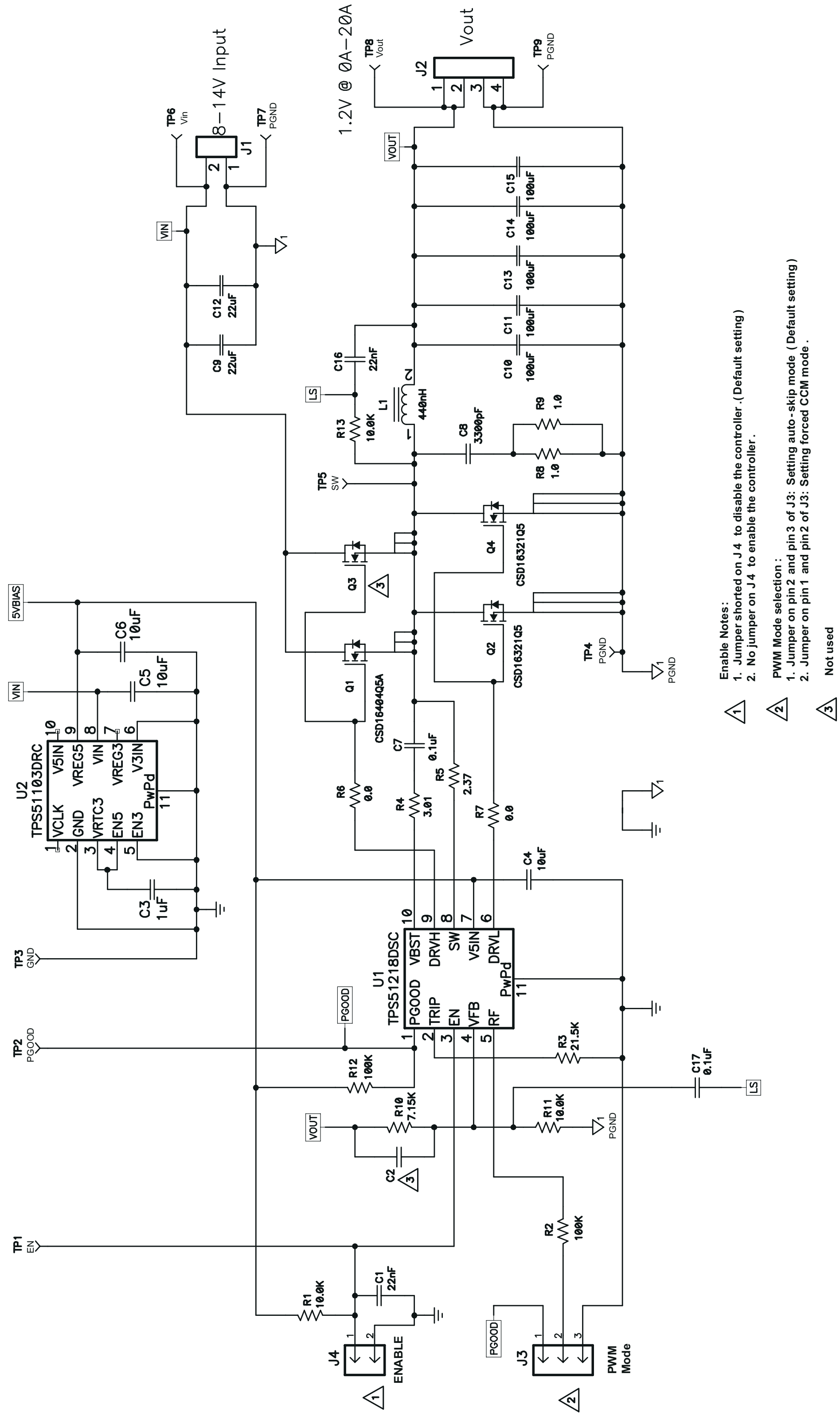

Figure 3-1. TPS51218EVM Schematic

4 Test Setup

4.1 Test Equipment

Voltage Source: The input voltage source, V_{IN}, must be a 0-V to 14-V variable DC source capable of supplying 10 A_{DC}. Connect V_{IN} to J1 as shown in Figure 4-2.

Multimeters: A 0-V to 15-V voltmeter must be used to measure V_{IN} at TP6 (VIN) and TP7 (PGND) and a 0-V to 5-V voltmeter for V_{OUT} measurement at TP8 (VOUT) and TP9 (PGND). A 0-A to 10-A current meter (A1) as shown in Figure 4-2 is used for input current measurements.

Output Load: The output load must be an electronic constant resistance mode load capable of 0 A_{DC} to 30 A_{DC} at 1.2 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope must be set for the following:

- 1-MΩ impedance
- 20-MHz bandwidth
- AC coupling
- 2-µs/division horizontal resolution
- 50-mV/division vertical resolution

Test points TP8 and TP9 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP8 and holding the ground barrel TP9 as shown in Figure 4-1. Using a leaded ground connection can induce additional noise due to the large ground loop.

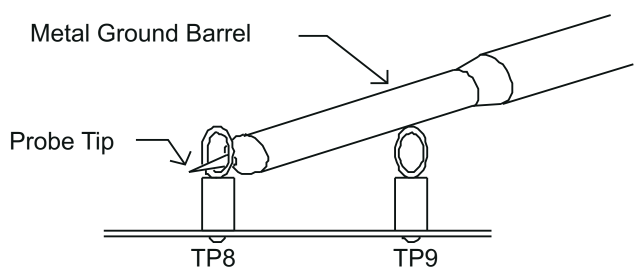

Figure 4-1. Tip and Barrel Measurement for V_{OUT} Ripple

Fan: Some of the components in this EVM can get hot, approaching temperatures up to 60°C during operation. A small fan capable of 200 to 400 LFM is recommended to reduce component temperatures while the EVM is operating. The EVM must not be probed while the fan is not running.

Recommended Wire Gauge: For VIN to J1 (12-V input), the recommended wire size is 1× AWG 14 per input connection, with the total length of wire less than four feet (2-foot input, 2-foot return). For J2 to LOAD, the minimum recommended wire size is 2× AWG 14, with the total length of wire less than four feet (2-foot output, 2-foot return).

4.2 Recommended Test Setup

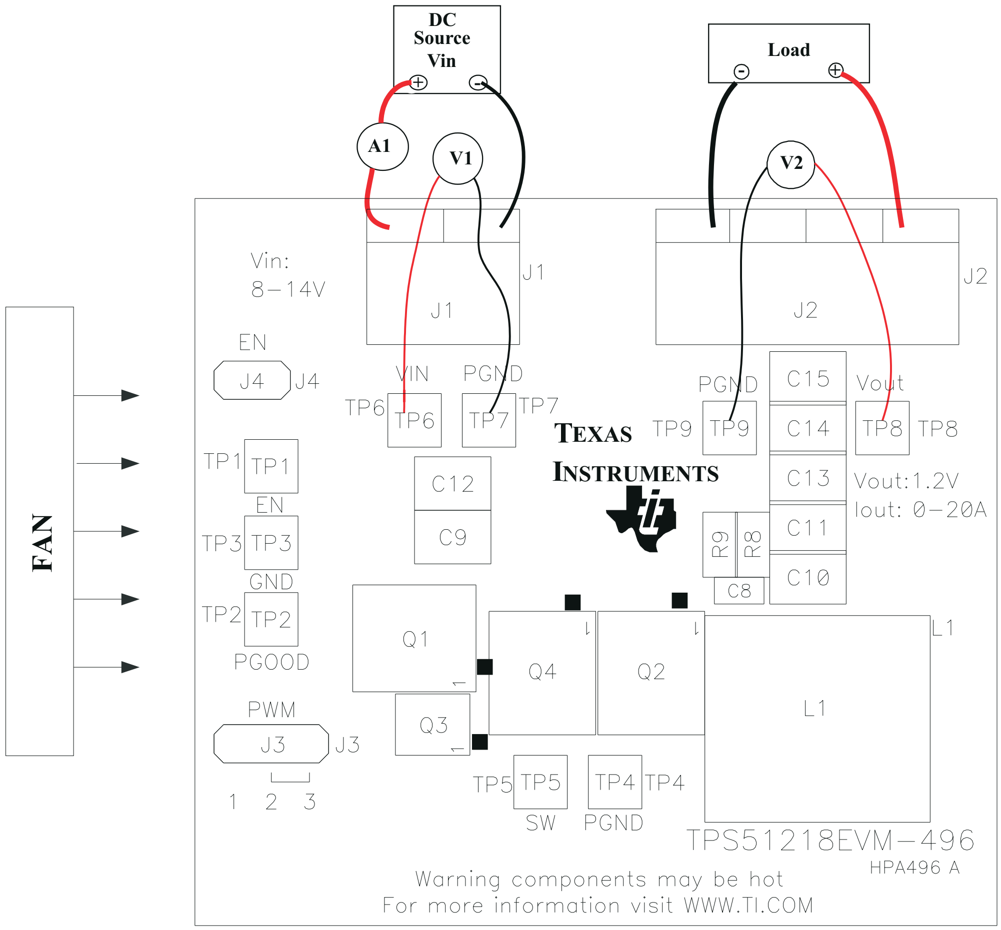

Figure 4-2. TPS51218EVM Recommended Test Setup

Figure 4-2 shows the recommended test setup to evaluate the TPS51218EVM. Working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM.

4.2.1 Configurations

- EN J4 setting
  1. No jumper enables the controller.
  2. A jumper shorted on J4 disables the controller (default setting).
- PWM J3 setting
  1. A jumper on pin 2 and pin 3 of J3 set the auto-skip mode (default setting).
  2. A jumper on pin 1 and pin 2 of J3 sets a forced CCM mode.

4.2.2 Input Connections

1. Prior to connecting the DC input source V_{IN}, it is advisable to limit the source current from V_{IN} to 10 A maximum. Ensure that V_{IN} is initially set to 0 V and connected as shown in Figure 4-2.
2. Connect a voltmeter V1 at TP6 (VIN) and TP7 (PGND) to measure the input voltage.
3. Connect a current meter A1 to measure the input current.

4.2.3 Output Connections

1. Connect the load to J2, and set the load to constant resistance mode to sink 0 A_{DC} before V_{IN} is applied.
2. Connect a voltmeter V2 at TP8 (VOUT) and TP9 (PGND) to measure the output voltage.

4.2.4 Other Connections

Place a fan as shown in Figure 4-2 and turn it on, making sure that air is flowing across the EVM.

5 Test Procedure

5.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Ensure that the load is set to constant resistance mode and to sink 0 A_{DC}.
2. Ensure that the jumper provided in the EVM to short J4 is on before V_{IN} is applied.
3. Ensure that the jumper provided in the EVM to short pin 2 and pin 3 of J3 is on before V_{IN} is applied.
4. Increase V_{IN} from 0 V to 12 V. Use V1 to measure the input voltage.
5. Remove the jumper on J4 to enable the controller.
6. Vary the load from 0 A_{DC} to 20 A_{DC}. V_{OUT} must remain in load regulation.
7. Vary V_{IN} from 8 V to 14 V. V_{OUT} must remain in line regulation.
8. Put the jumper on J4 to disable the controller.
9. Decrease the load to 0 A.
10. Decrease V_{IN} to 0 V.

5.2 List of Test Points

Table 5-1. The Functions of Each Test Points

Test Points	Name	Description
TP1	EN	Enable
TP2	PGOOD	Power Good
TP3	GND	GND
TP4	PGND	PGND
TP5	SW	Switching node
TP6	Vin	Vin
TP7	PGND	GND for Vin
TP8	Vout	Vout
TP9	PGND	PGND

5.3 Equipment Shutdown

1. Shut down the load.
2. Shut down V_{IN}.
3. Shut down the fan.

6 Performance Data and Typical Characteristic Curves

Figure 6-1 through Figure 6-9 present typical performance curves for the TPS51218EVM.

6.1 Efficiency

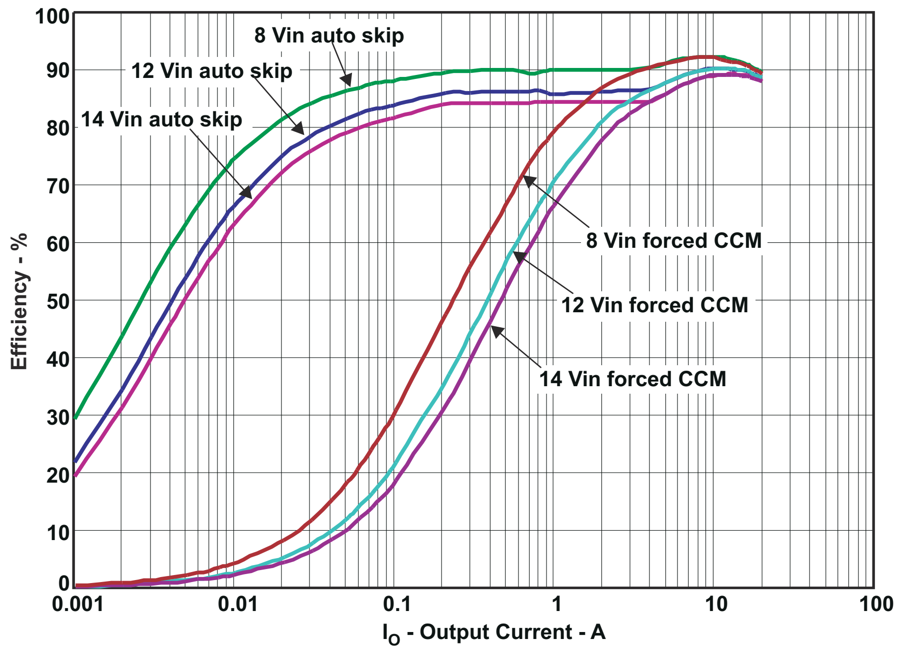

Figure 6-1. TPS51218EVM Efficiency

6.2 Load Regulation

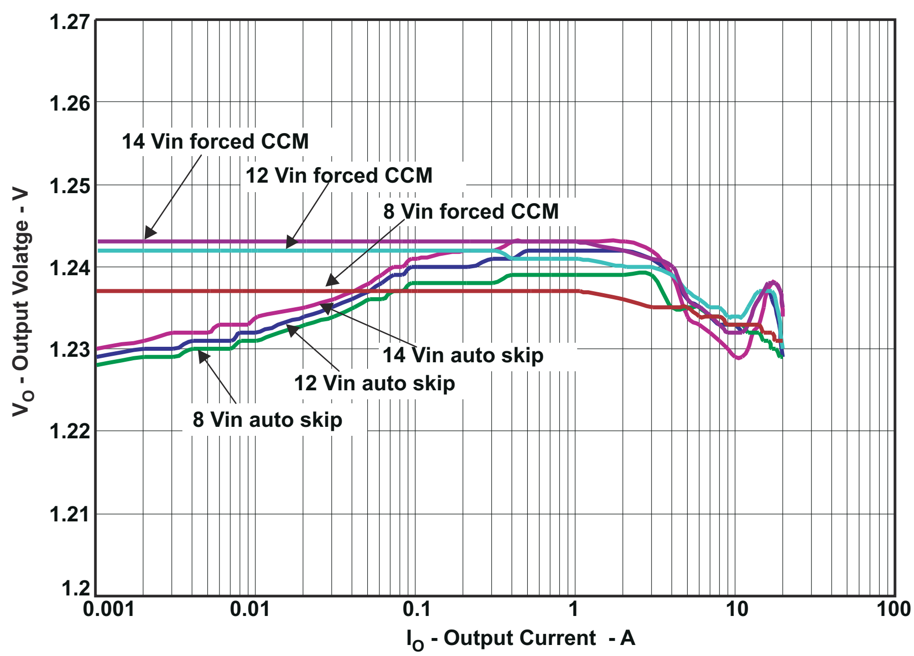

Figure 6-2. TPS51218 Load Regulation

6.3 Transient Response

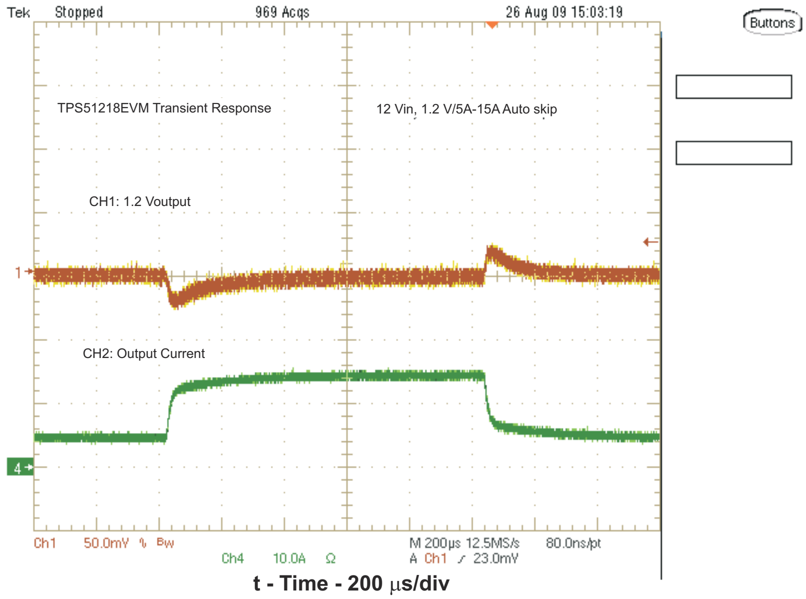

Figure 6-3. TPS51218EVM Load Transient

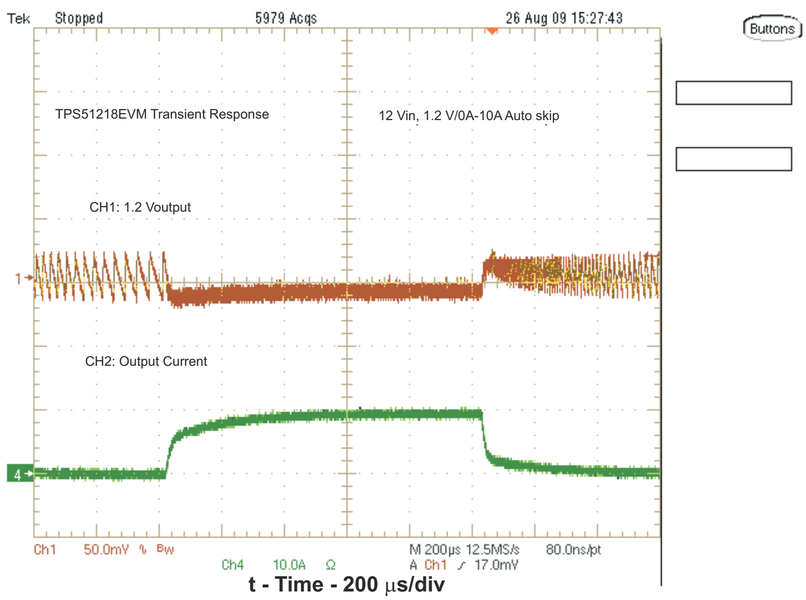

Figure 6-4. TPS51218EVM Load Transient

6.4 Output Ripple

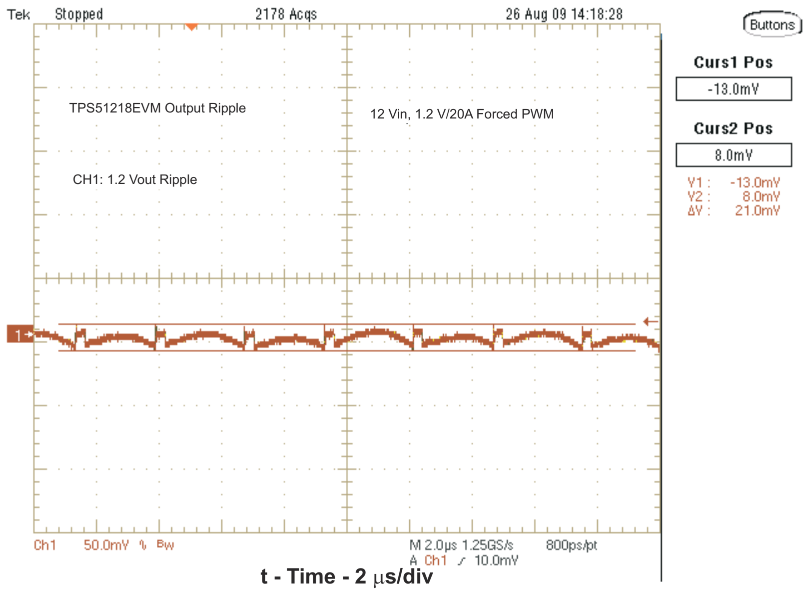

Figure 6-5. Output Ripple

6.5 Switch Node Voltage

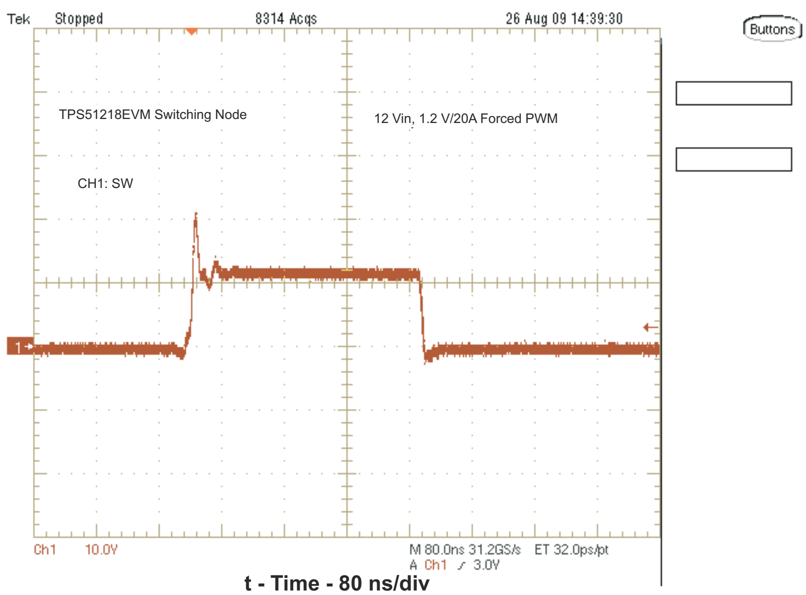

Figure 6-6. Switching Node Waveform

6.6 Turn-On Waveform

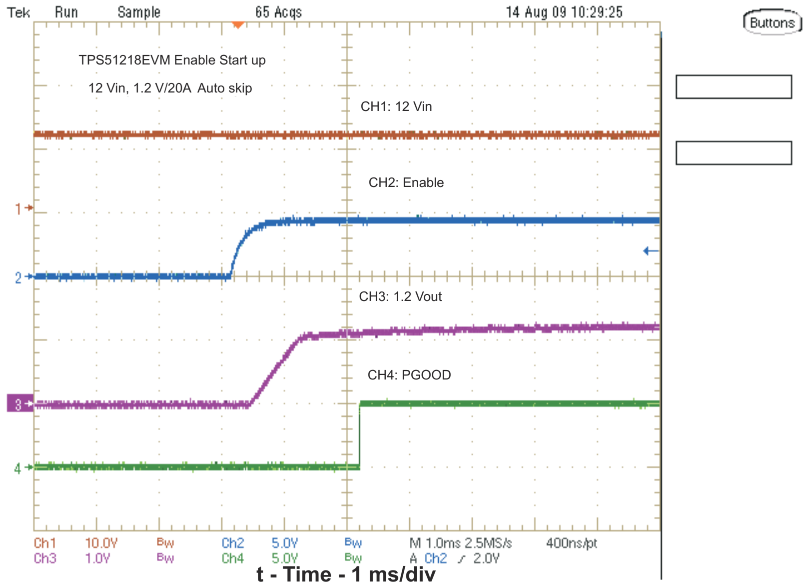

Figure 6-7. Enable Turn-On Waveform

6.7 Turn-Off Waveform

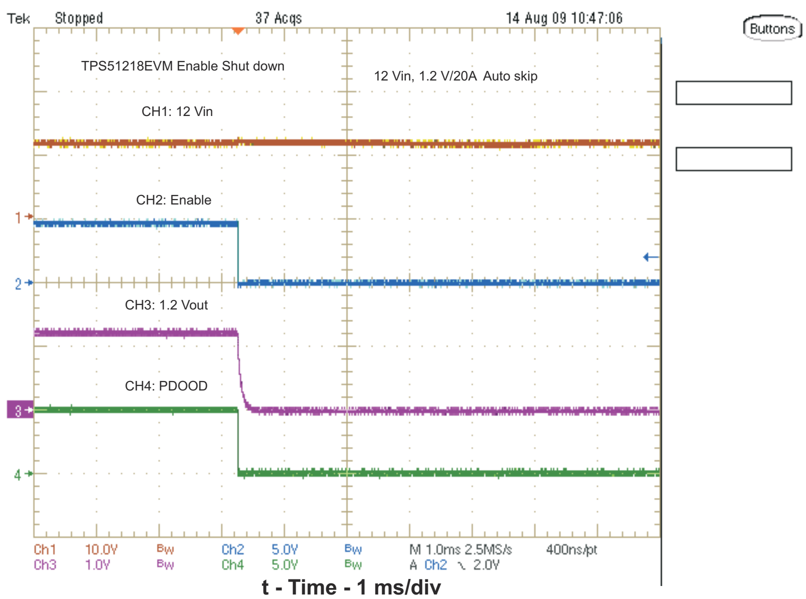

Figure 6-8. Enable Turn-Off Waveform

6.8 Output 1.1-V Prebias Turn-On

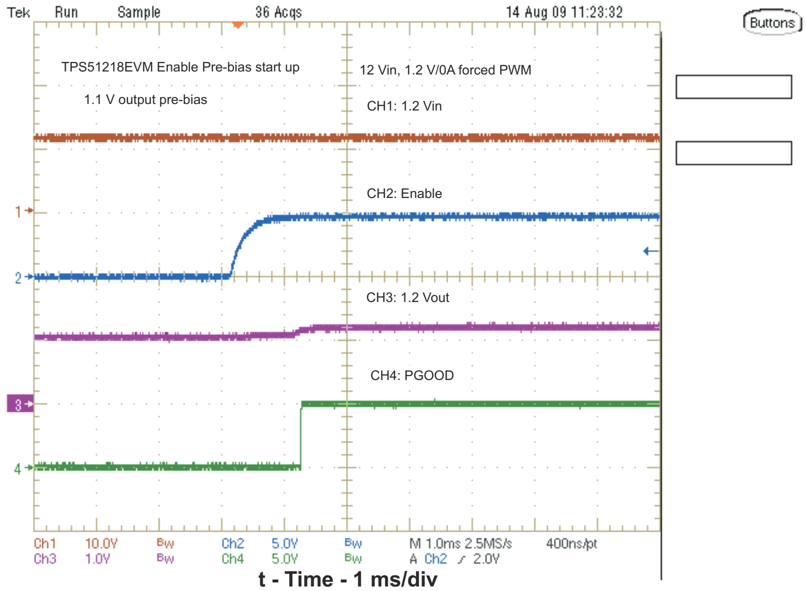

Figure 6-9. Output 1.1-V Prebias TurnOn

7 EVM Assembly Drawing and PCB Layout

Figure 7-1 through Figure 7-6 show the design of the TPS51218EVM printed-circuit board. The EVM has been designed using a four-layer, 2-oz copper circuit board.

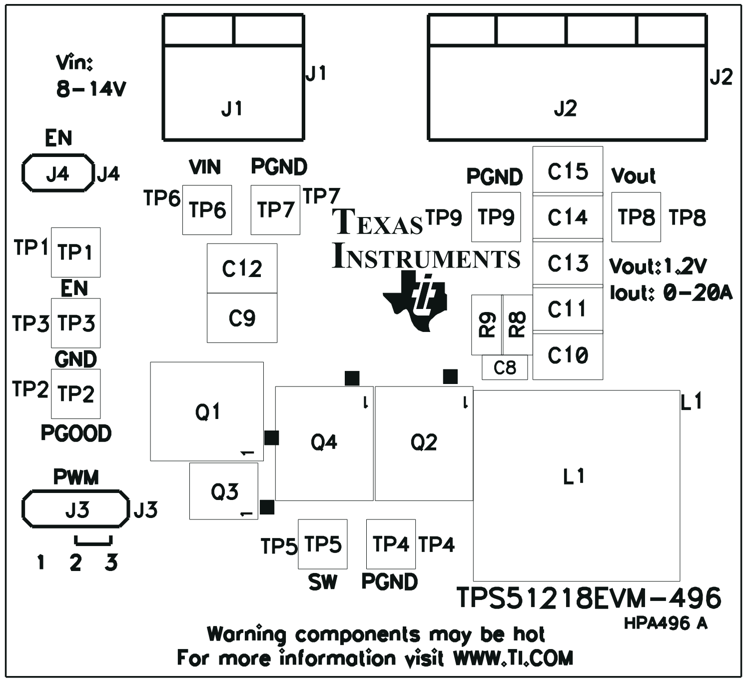

Figure 7-1. TPS51218EVM Top Layer Assembly Drawing, Top View

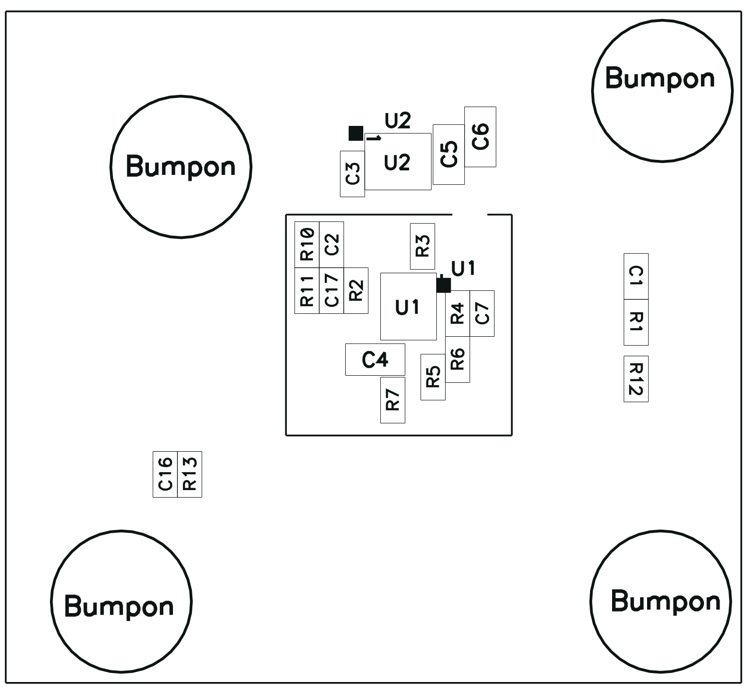

Figure 7-2. TPS51218EVM Bottom Assembly Drawing, Bottom View

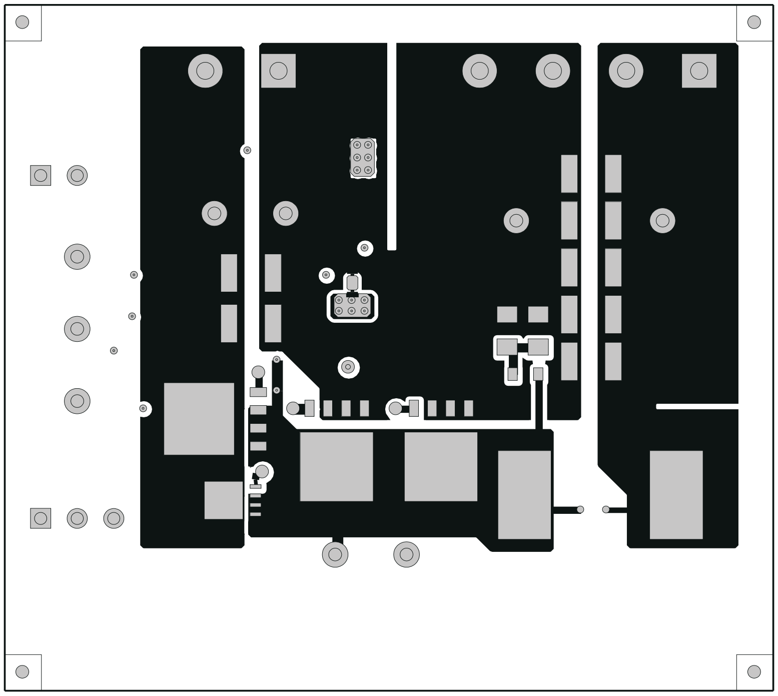

Figure 7-3. TPS51218EVM Top Copper, Top View

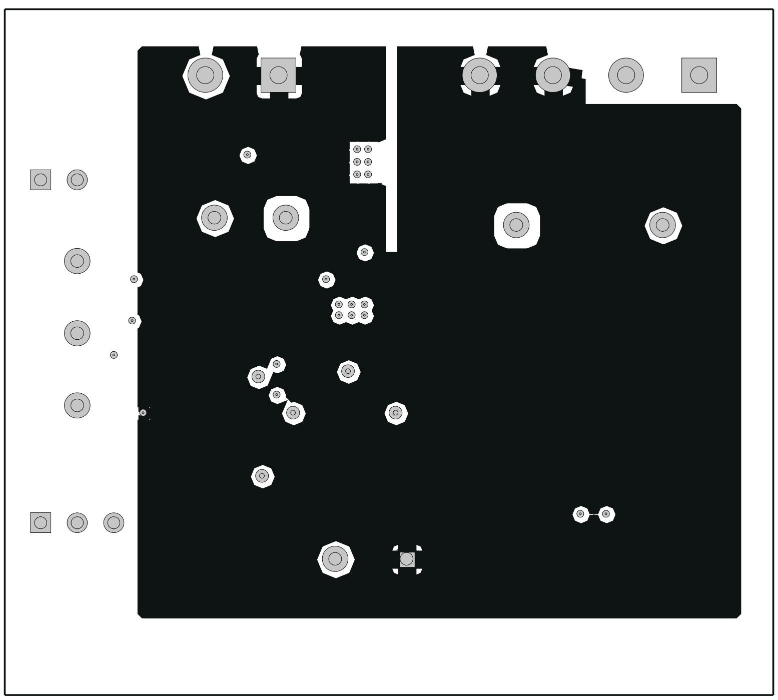

Figure 7-4. TPS51218EVM Internal Layer 1

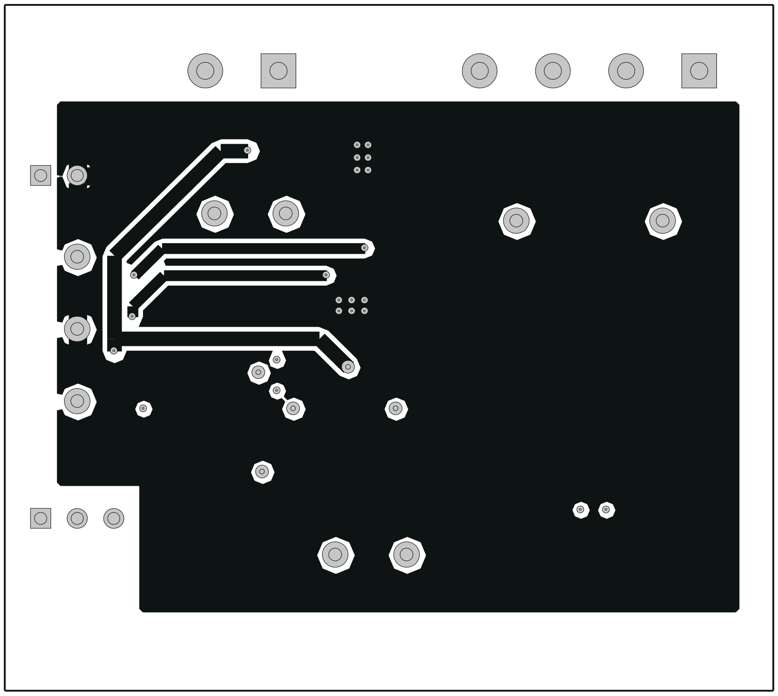

Figure 7-5. TPS51218EVM Internal Layer 2

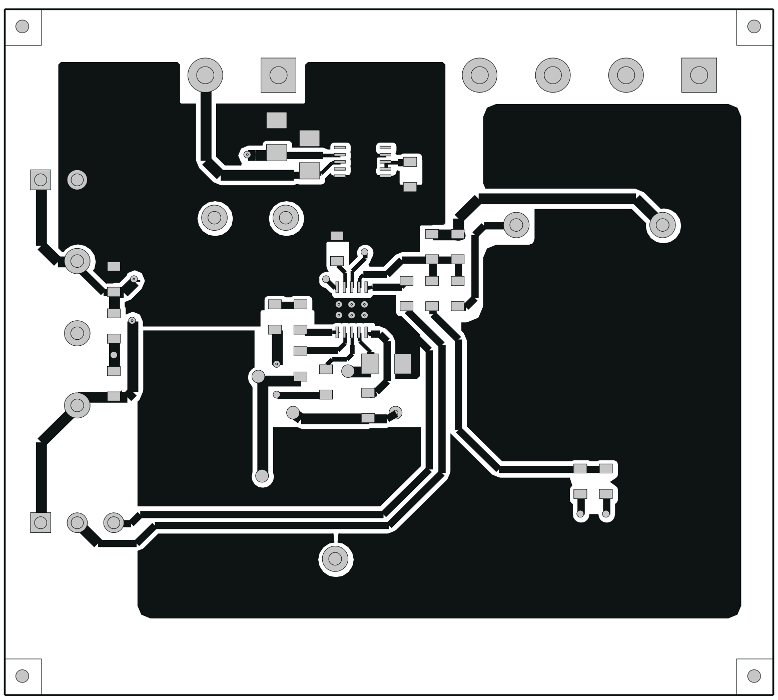

Figure 7-6. TPS51218EVM Bottom Layer

8 Bill of Materials

The EVM components are shown in Table 8-1 according to the schematic shown in Figure 3-1.

Table 8-1. Bill of Materials

QTY	REFDES	Description	MFR	Part Number
2	C9, C12	Capacitor, Ceramic, 22 µF, 16 V, X5R, 10%, 1210	Murata	GRM32ER61C226KE20L
1	C3	Capacitor, Ceramic, 1 µF, 16 V, X7R, 10%, 0603	STD	STD
2	C1, C16	Capacitor, Ceramic, 0.022 µF, 16 V, X7R, 10%, 0603	STD	STD
1	C8	Capacitor, Ceramic, 3300 pF, 25 V, X7R, 10%, 0603	STD	STD
3	C4, C5, C6	Capacitor, Ceramic, 10 µF, 16 V, X5R, 10%, 0805	STD	STD
2	C7, C17	Capacitor, Ceramic, 0.1 µF, 25 V, X7R, 10%, 0603	STD	STD
5	C10, C11, C13, C14, C15	Capacitor, Ceramic, 100 µF, 6.3 V, X5R, 20%, 1210	Murata	GRM32ER60J107ME20L
1	L1	Inductor, SMT, 0.44 µH, 30 A, 0.0032 Ω, 0.530" × 0.510"	Pulse	PA0513.441NLT
			E&E Magnetic	831-02990F
1	Q1	MOSFET, Nchan, 25 V, 21 A, 4.1 mΩ, QFN5X6mm	TI (Ciclon)	CSD16404Q5A
2	Q2, Q4	MOSFET, Nchan, 25 V, 31 A, 2.1 mΩ, QFN5X6mm	TI(Ciclon)	CSD16321Q5
3	R1, R11, R13	Resistor, Chip, 10 k, 1/16W, 1%, 0603	STD	STD
1	R10	Resistor, Chip, 7.15 k, 1/16W, 1%, 0603	STD	STD
1	R3	Resistor, Chip, 19.6 k, 1/16W, 1%, 0603	STD	STD
2	R2, R12	Resistor, Chip, 100 k, 1/16W, 1%, 0603	STD	STD
2	R6, R7	Resistor, Chip, 0, 1/16W, 1%, 0603	STD	STD
1	R4	Resistor, Chip, 3.01, 1/16W, 1%, 0603		
1	R5	Resistor, Chip, 2.37, 1/16W, 1%, 0603	STD	STD
2	R8, R9	Resistor, Chip, 1, 1/16W, 5%, 0805	STD	STD
1	U2	IC, Integrated LDO with switch-over circuit, DGS10	TI	TPS51103DRC
1	U1	IC, Synchronous step-down controller, DSC10	TI	TPS51218DSC

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2010) to Revision A (February 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title.. 2

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