

AN-2195 Driving High Speed ADCs with the LMH6521 DVGA for High IF AC-Coupled Applications

ABSTRACT

This application report discusses driving high speed ADCs with the Texas Instruments LMH6521 DVGA for high IF AC-coupled applications.

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1 Introduction

Sampled data systems can be categorized into two main types. The first and simplest is the baseband system known as the “1st Nyquist-zone” system. The second is a more complex under-sampled system, often referred to as the sub-sampled system or Intermediate frequency (IF)-sampled system. Baseband system applications are generally DC-coupled while the IF-sample systems applications tend to be AC-coupled. In this application report, the LMH6521 is combined with Texas Instruments high-speed analog-to-digital convertor (ADC), the ADC16DV160, that is optimized for an IF frequency of 192 MHz.

The LMH6521 contains two high-performance, digitally controlled variable-gain amplifiers (DVGA) with exceptional gain and phase matching between channels over the entire attenuation range that mates nicely with the dual channels of the ADC16DV160. The ADC16DV160 is a monolithic, dual-channel, high-performance CMOS ADC capable of converting analog input signals into 16-bit digital words at rates up to 160 MSPS. The output noise density of the LMH6521 is typically 33 nV/Hz, which makes the LMH6521 suitable to drive 14-bit to 16-bit ADC’s.

2 Circuit Description

As shown in [Figure 1](#), a low loss 1:4 (impedance ratio) input transformer TC4-1W is used to match the LMH6521’s 200Ω balanced input impedance to a 50Ω unbalanced signal source resulting in a low input insertion loss of 0.8 dB. The LMH6521 provides variable gain, isolation, and source matching to the ADC16DV160. The band-pass filter between the LMH6521 and ADC16DV160 provides attenuation of the amplifier distortion products and noise outside the Nyquist zone helping to preserve the available SNR of the ADC. The filter is a 3rd order 200Ω matched tapped-L anti-aliasing filter designed for an intermediate frequency of 192 MHz and a 20 MHz bandwidth.

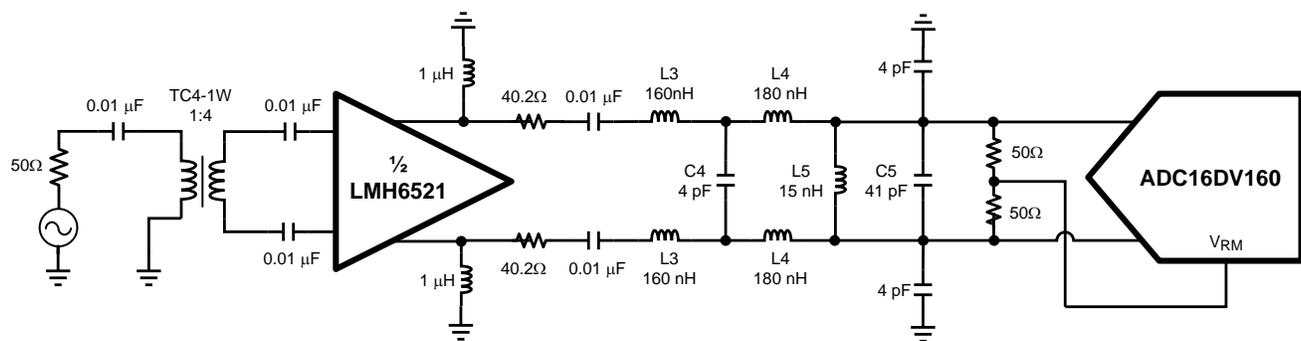


Figure 1. Tapped-L Band-pass Filter For $f_c = 192$ MHz with a 20 MHz Bandwidth Designed for 100Ω Impedance

3 Tapped Inductor Band-pass Filter

The anti-aliasing band-pass filter is called a “Tapped-L” or “Tapped Inductor” filter because it uses series inductors for the T-match impedance transform. [Figure 2](#) shows L1, L2, and the combination of C11 and C12 to make up the T-match structure of the filter. As shown in [Figure 2](#), the filter is broken up into three segments for analysis purposes: down impedance transform, up impedance transform, and band-pass tank. The tank provides a 1st-order band-pass profile while the impedance transform matches the load resistance, R_L , to the source resistance, R_S , at the designated center frequency and increases high frequency roll-off to 4th order.

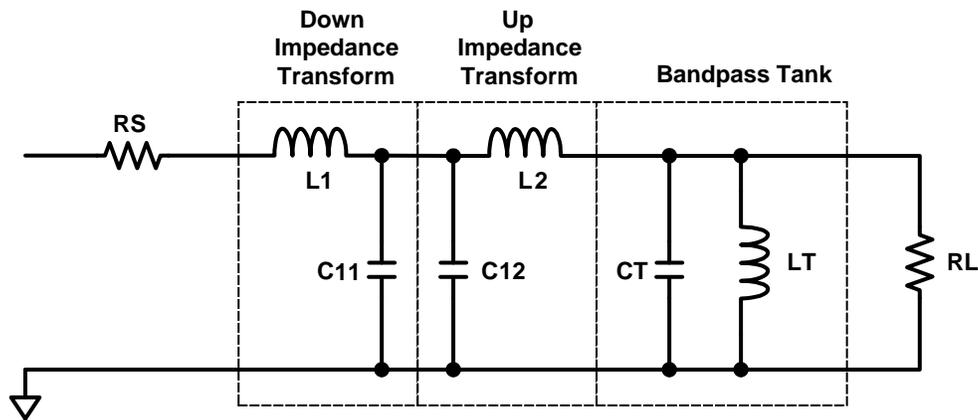


Figure 2. Single-Ended Tapped-L Band-pass Filter Segments

Frequencies above the high frequency corner of 202 MHz have greater than 4th-order roll-off (>24dB/octave) whereas lower frequencies below 182 MHz will have only a 1st order roll-off. At lower frequencies there is less total bandwidth for aliasing. This filter scheme can provide > 40 dB harmonic attenuation with minimal filter complexity and nearly 0 dB insertion loss to allow the LMH6521 to drive the ADC input to full scale without compressing at the supply rails. Ripple in the pass-band is easily kept below 1 dB. The equivalent noise bandwidth (ENBW) of this filter is approximately 44 MHz. Figure 3 shows the filter profile over frequency.

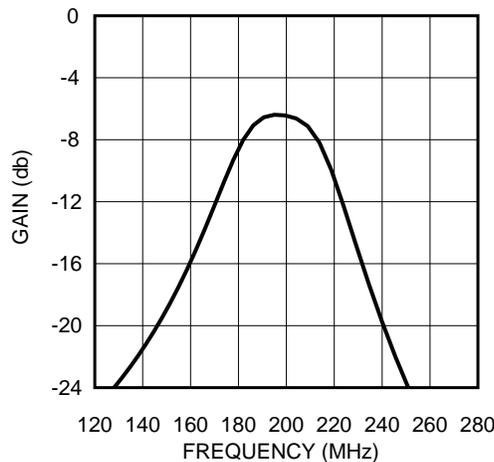


Figure 3. 192 MHz Tapped-L Filter Profile

Inductor L5 (Figure 1) in parallel with the ADC input capacitance and C5 to form a resonant tank to help ensure the ADC input looks like a real resistance at the target IF center frequencies. Inductor L5 shorts the ADC inputs at dc which introduces a zero into the transfer function. The value of C5 should be adjusted with respect to the ADC input capacitance. Since C5 is parallel to $C_{IN(ADC)}$, the equivalent value for C5 is equal to the calculated value ($C5_{calculated}$) minus the ADC input capacitance, $C_{IN(ADC)}$.

4 IF-Sampling Frequency Plan

The ADC16DV160 sub-samples the 192 MHz IF signal with a 153.6 MSPS clock so that the 20MHz signal band aliases to the center of the first Nyquist zone at 38.4 MHz. A large benefit of this plan is the placement of the 2nd order harmonic, H2, completely out of the band of interest when it aliases. HD3 cannot be excluded from the signal band and must be reduced in the system as much as possible. The frequency ranges of the HD2 and HD3 aliases are shown in Figure 4.

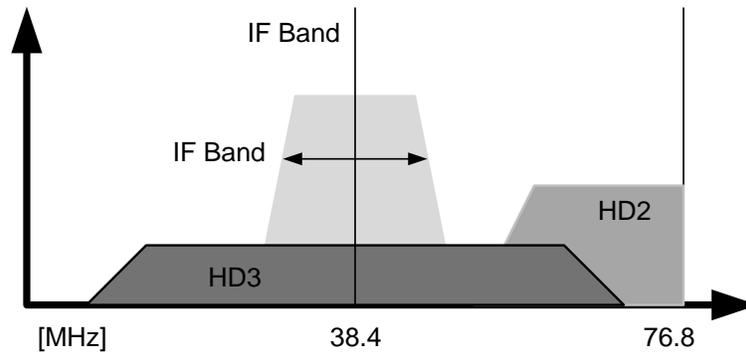


Figure 4. Using Impedance Transform to Realize Voltage Gain

5 System Performance

Figure 5 and Figure 6 show the SFDR and SNR performance over frequency of the circuit shown in Figure 1. The input signal is measured at -1, -3, and -6 dBFS of the ADC.

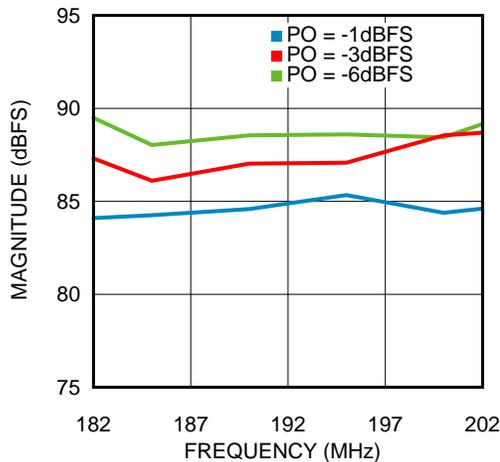


Figure 5. SFDR Performance vs. Input Signal Frequency

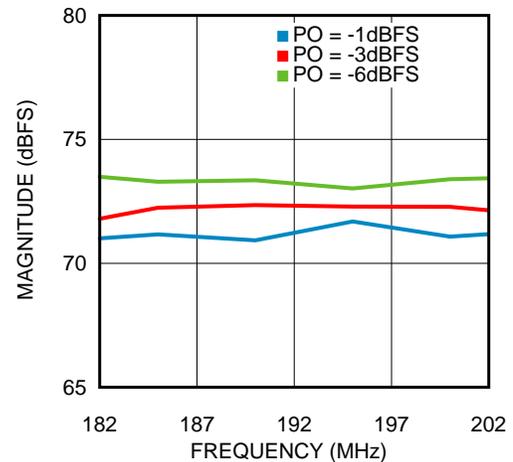


Figure 6. SNR Performance vs. Input Signal Frequency

With a 2-tone large input signal with the LMH6521 set to maximum gain (26dB) to drive an input signal level at the ADC of -1 dBFS, the SNR and SFDR results are shown in [Table 1](#) compared to the stand alone ADC16DV160 specifications.

Table 1. SNR and SFDR Results

Configuration	ADC Input	SNR (dBFS)	SFDR (dBFS)
LMH6521 + BPF + ADC16DV160	-1 dBFS	75.5	82
ADC16DV160 only	-1 dBFS	76	89

6 Optimal Performance

Placement of the LMH6521 relative to the ADC16DV160 is essential for optimal performance. It is recommended that the amplifier be placed as close the ADC as possible and with excellent layout and decoupling techniques to achieve the desired system performance. One way to improve channel isolation is to place the output inductors of each channel of the LMH6521 90 degrees to reduce magnetic coupling as shown in [Figure 7](#). As a minimum, a 4-layer board should be utilized with one ground, one power, and two signal layers. However, by adding more layers, thicker top and bottom metal layers, and additional through vias will improve heat dissipation of the LMH6521 and improve performance.

The LMH6521 DVGA is well suited to drive Texas Instruments family of high speed MSPS data converters: ADC10DV200, ADC12EU050, ADC12C170, ADC16V130, and ADC16DV160. Contact a Texas Instruments representative to obtain documentation on the SP16160CH2RB reference design files.

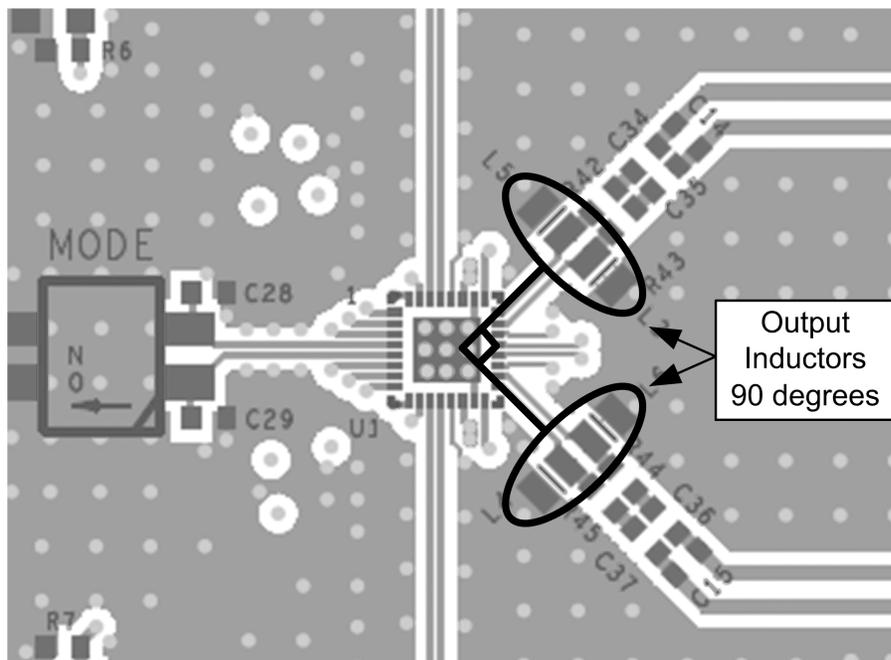


Figure 7. Output Inductors at 90 Degrees

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