

**Test Data
For PMP9362
3/4/2014**



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1. Design Specifications

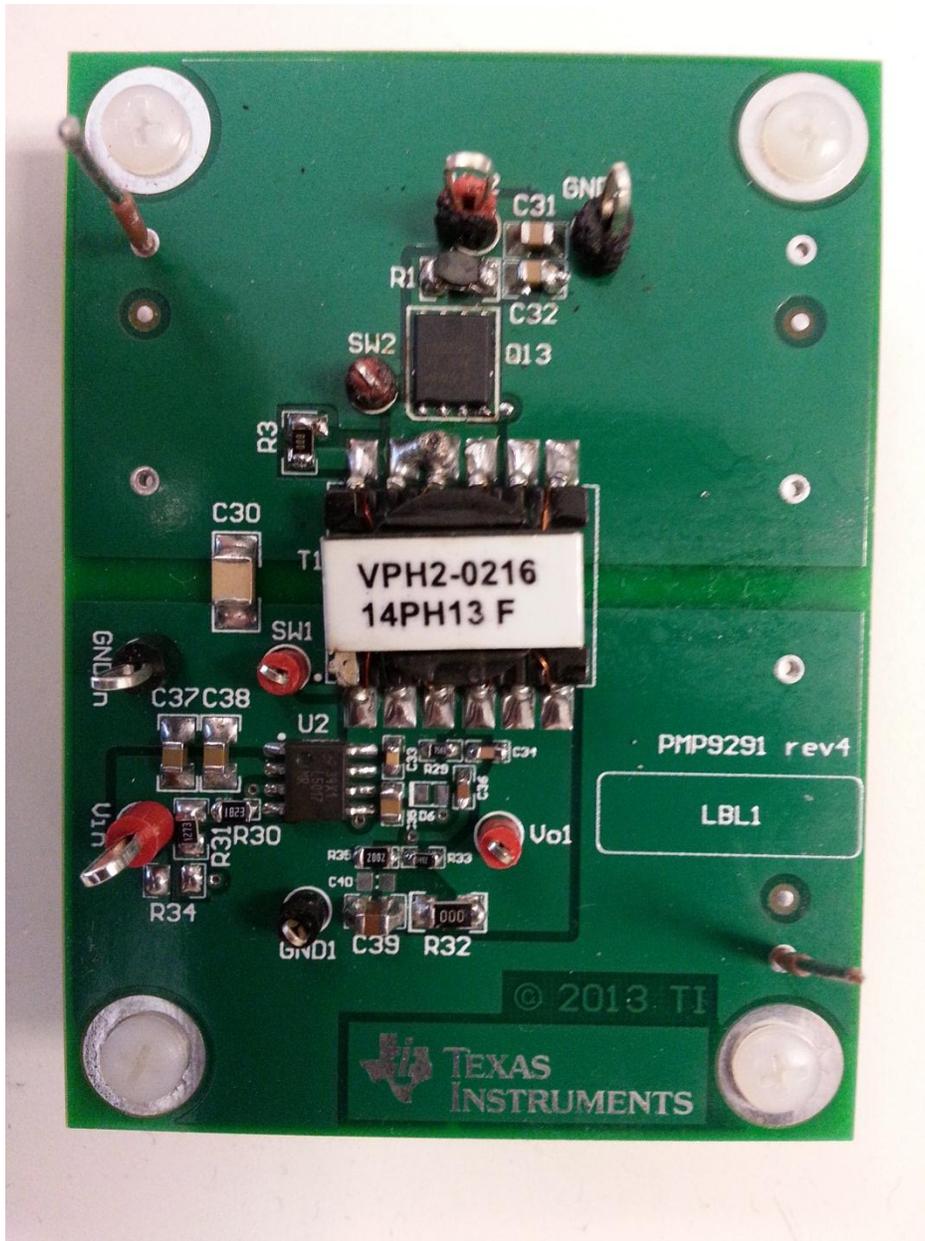
Vin	21.6VDC to 26.4VDC (24VDC Nominal)
Vout	5VDC
Iout	0.3A Max.
Approximate Switching Frequency	≈292KHz

2. Circuit Description

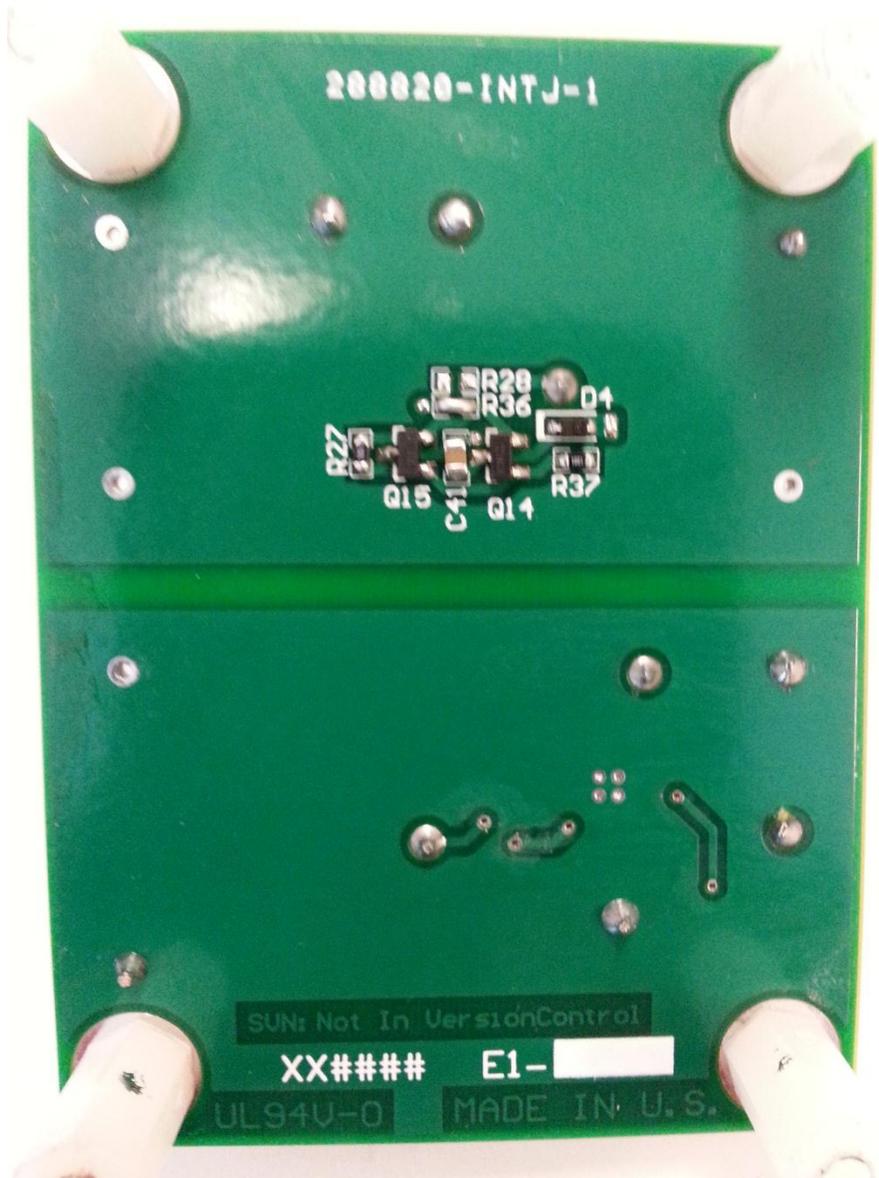
PMP9362 is an Isolated Flyback Converter using a synchronous buck regulator with Self-Driven Synchronous Rectification on the Secondary Side. The design accepts an input voltage of 21.6V_{in} to 26.4V_{in} and provides an isolated output of 5V_{out} capable of supplying a maximum of 0.3A of current to the load. This design was built on a 4-layer PCB. The secondary-side self-driven synchronous rectification offers benefits of no need for pre-load and much lower output voltage tolerances (4.9285V_{out} ± 1.0% over entire line and load range) without the need for opto-coupler and discrete voltage reference. A comparison of output voltage regulation over line and load between this design and an analogous non-synchronous flyback converter (PMP) are given and compared in Sections 5.5 and 5.6. The design uses a readily-available off-the-shelf VERSA-PAC series transformer.

3. PMP9362 Board Photos

Board Dimensions: 2" x 2.7"

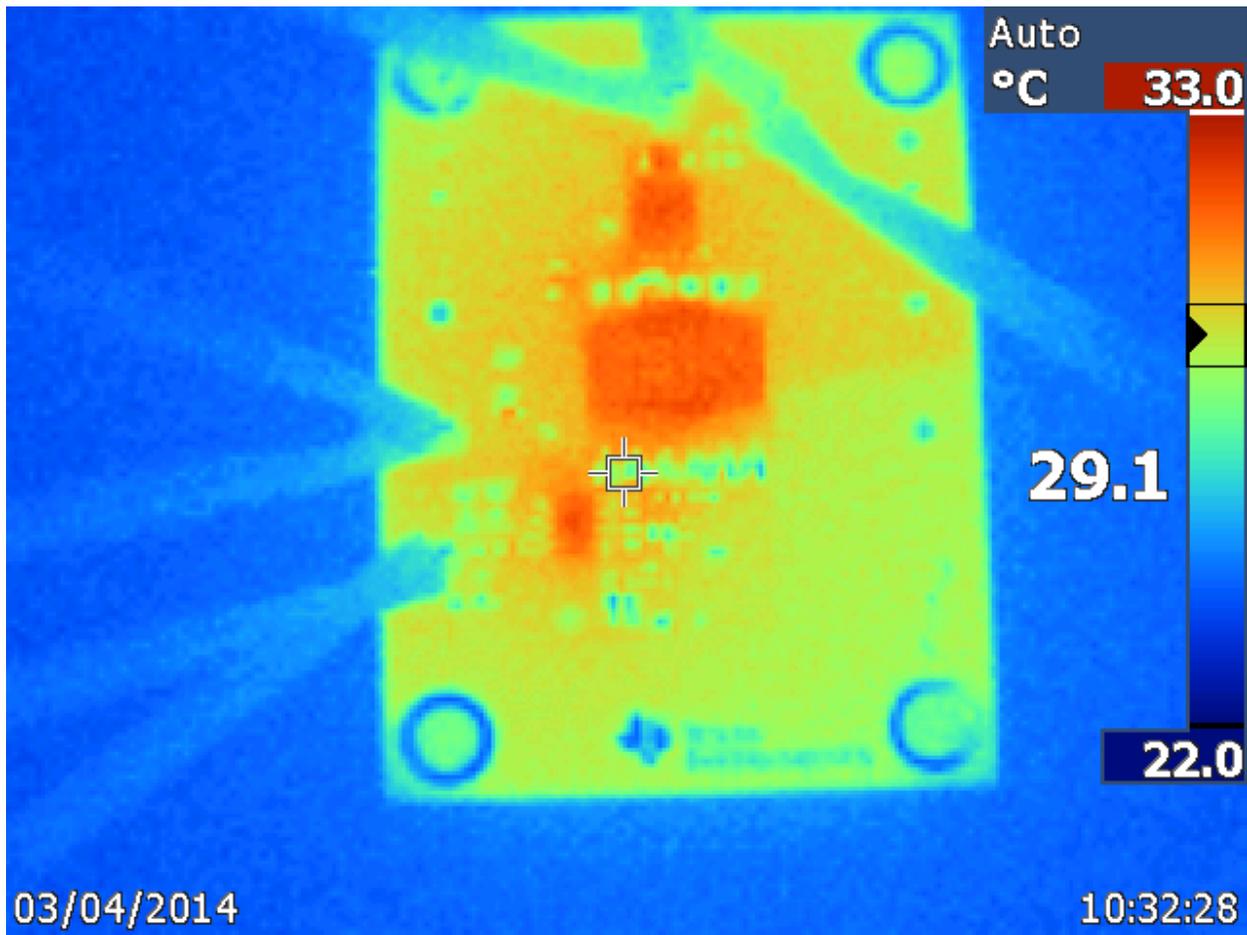


Board Photo (Top)



Board Photo (Bottom)

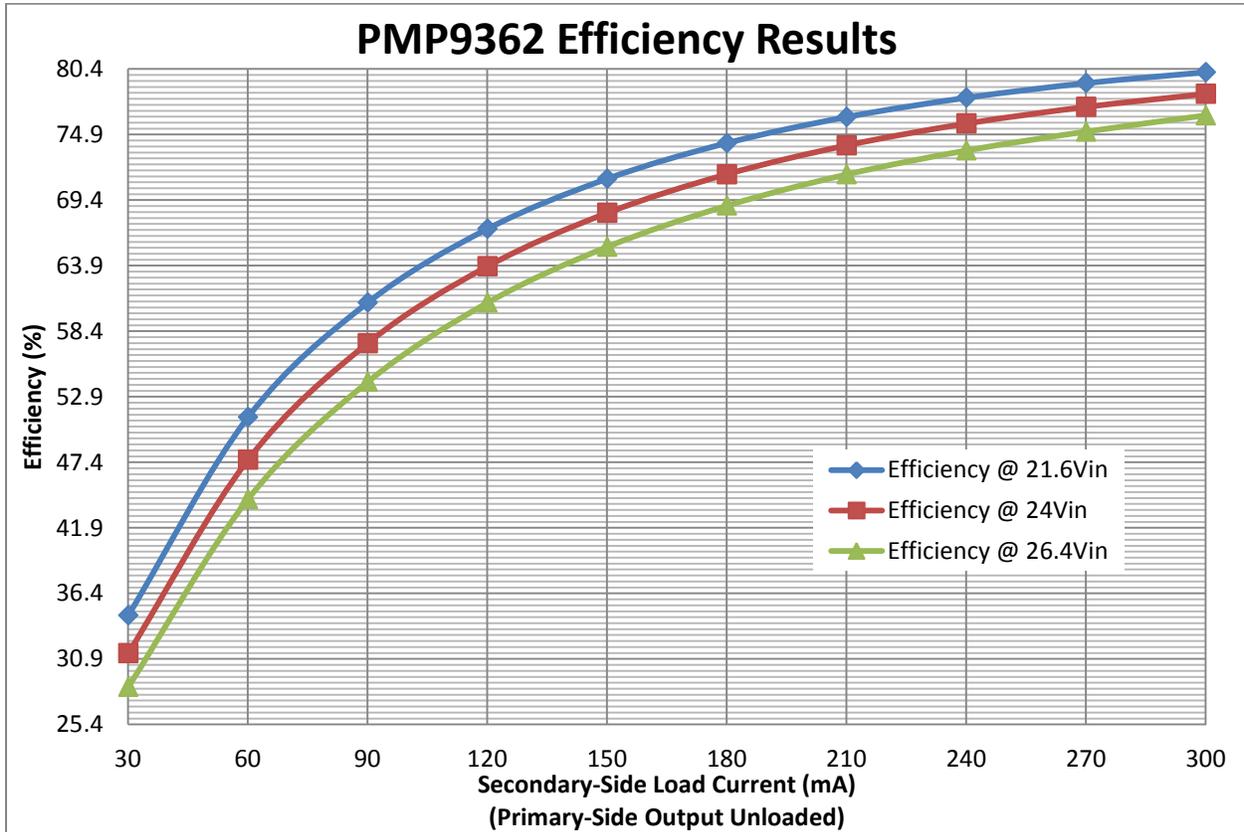
4. Thermal Data



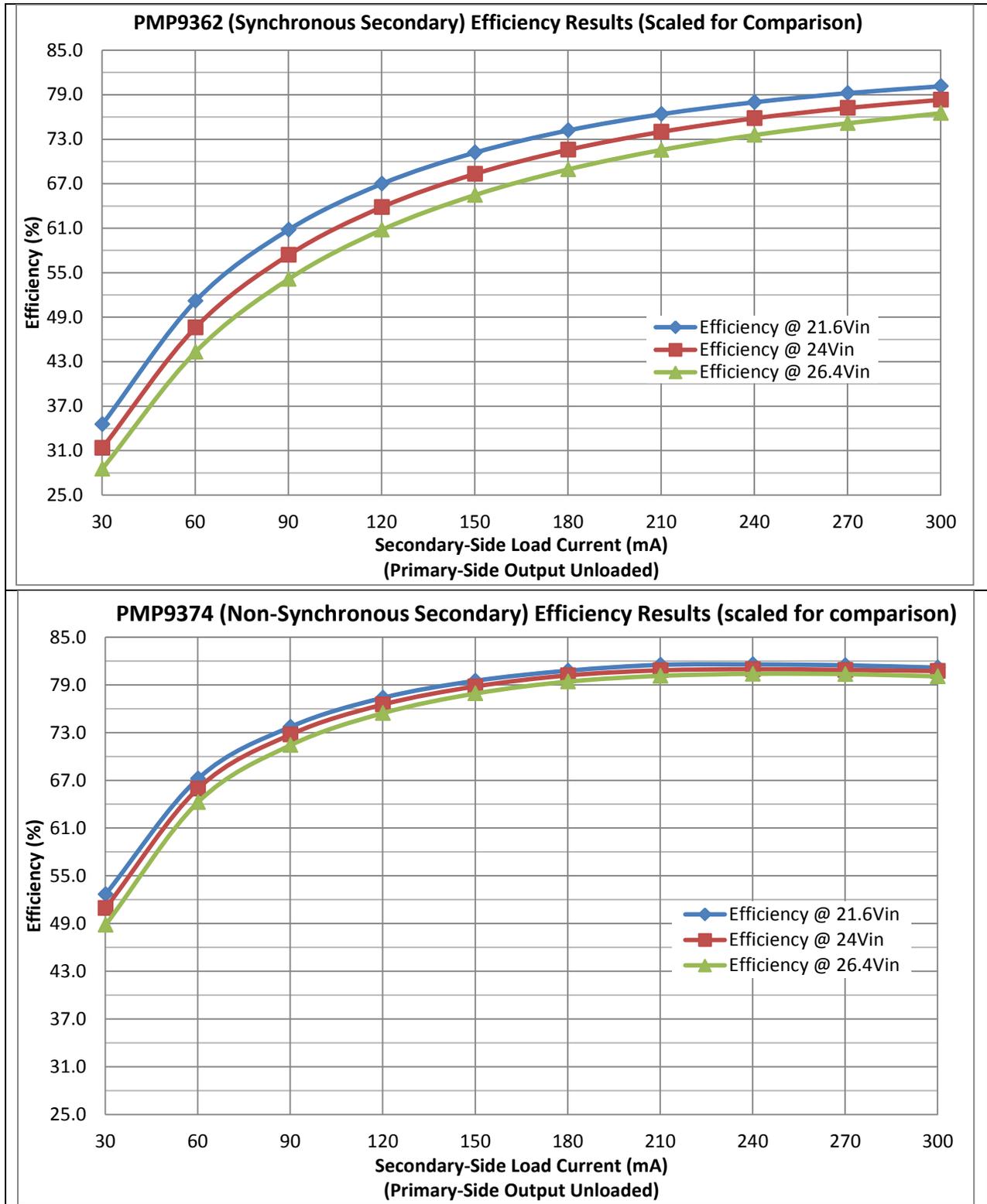
IR thermal image taken at steady state with 24Vin and 0.3A load (no airflow)

5. Efficiency and Line/Load Regulation

5.1 Efficiency Chart



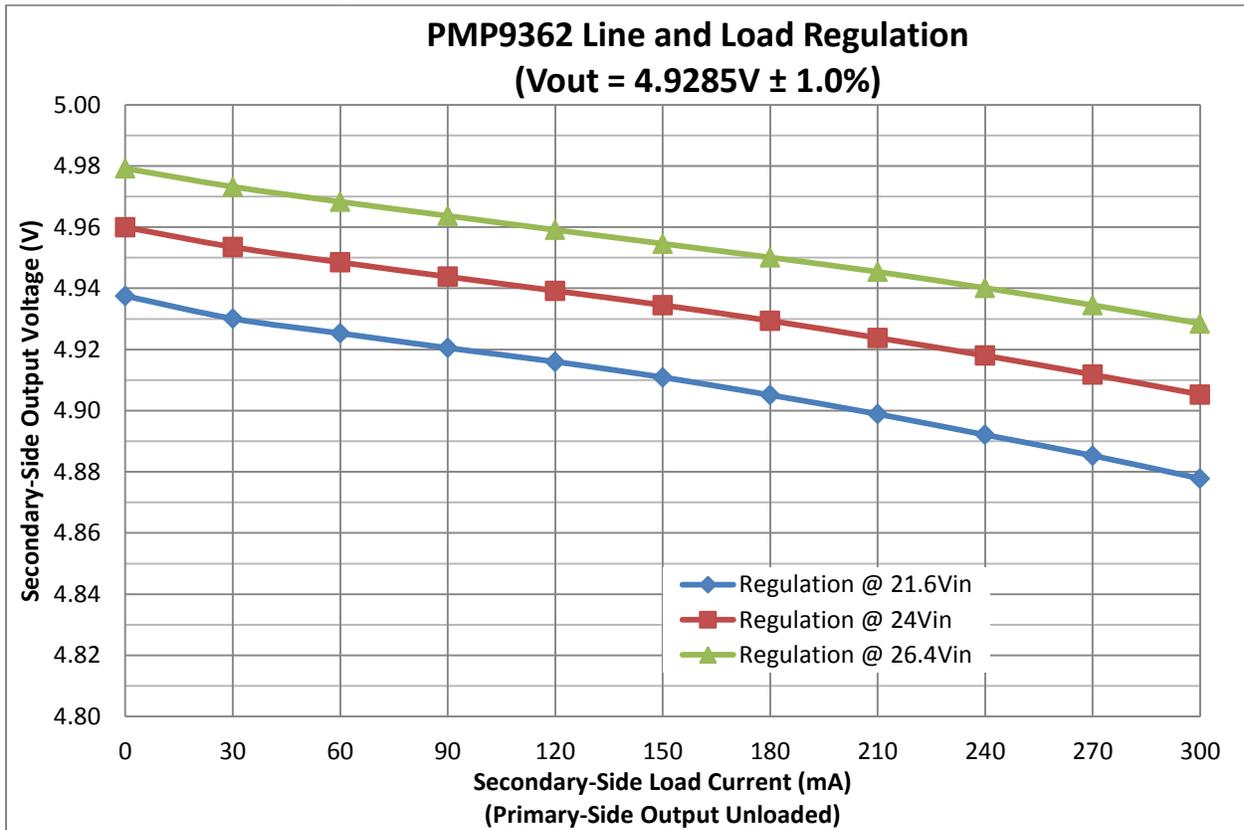
5.2 Efficiency Comparison between PMP9362 (Synchronous Secondary) and PMP9374 (Non-Synchronous Secondary)



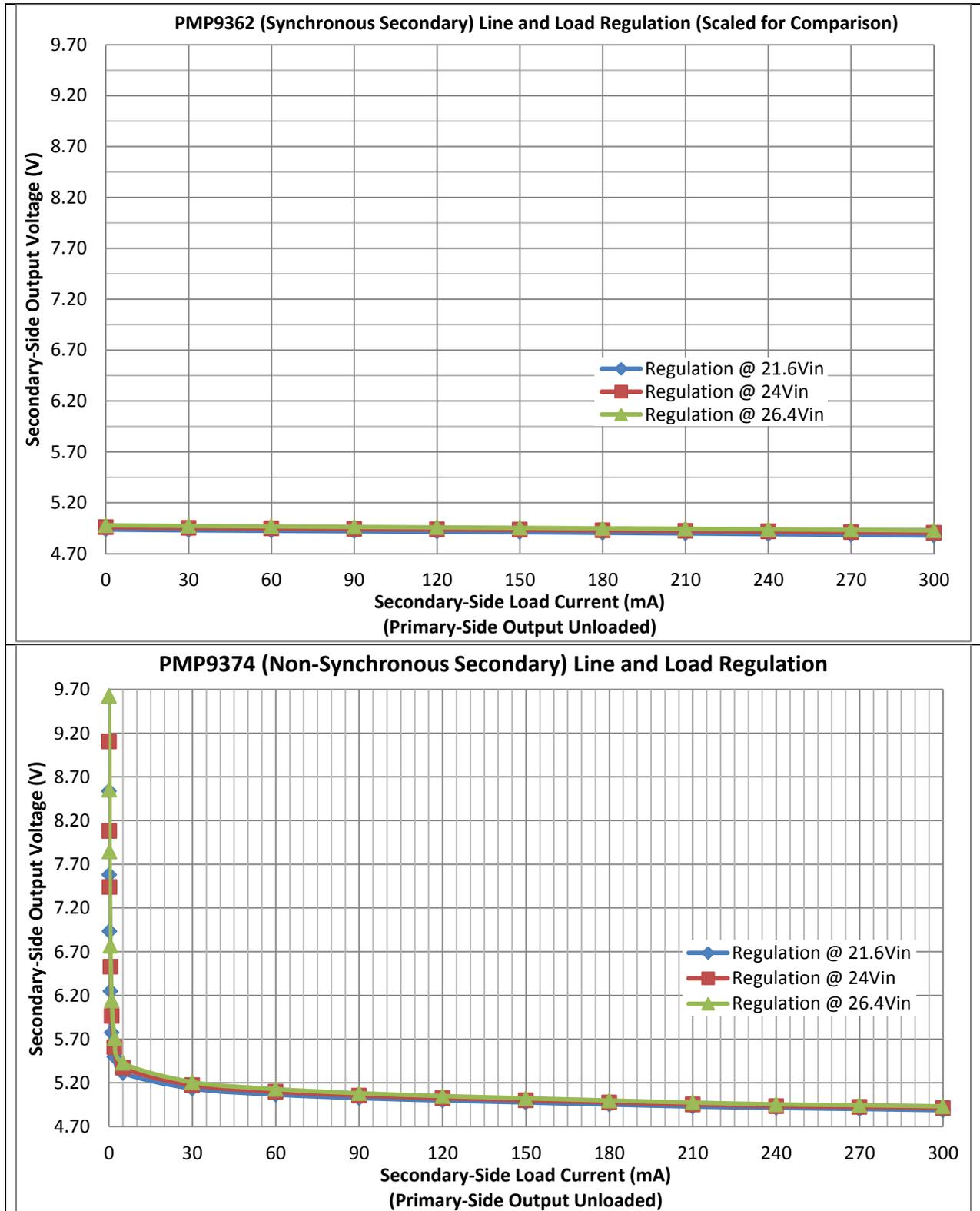
5.3 Efficiency and Line/Load Regulation Data

Vin (V)	Iin (mA)	Vout (V)	Iout (mA)	Pin (W)	Pout (W)	Efficiency (%)
21.6	13.1	4.9375	0	0.2830	0.0000	
21.6	19.815	4.9301	30	0.4280	0.1479	34.6
21.6	26.731	4.9253	60	0.5774	0.2955	51.2
21.6	33.722	4.9205	90	0.7284	0.4428	60.8
21.6	40.77	4.916	120	0.8806	0.5899	67.0
21.6	47.902	4.9109	150	1.0347	0.7366	71.2
21.6	55.098	4.9051	180	1.1901	0.8829	74.2
21.6	62.362	4.8989	210	1.3470	1.0288	76.4
21.6	69.7	4.8921	240	1.5055	1.1741	78.0
21.6	77.089	4.8853	270	1.6651	1.3190	79.2
21.6	84.543	4.8778	300	1.8261	1.4633	80.1
Vin (V)	Iin (mA)	Vout (V)	Iout (mA)	Pin (W)	Pout (W)	Efficiency (%)
24.0	13.693	4.96	0	0.3286	0.0000	
24.0	19.74	4.9535	30	0.4738	0.1486	31.4
24.0	25.983	4.9485	60	0.6236	0.2969	47.6
24.0	32.302	4.9438	90	0.7752	0.4449	57.4
24.0	38.681	4.9392	120	0.9283	0.5927	63.8
24.0	45.14	4.9345	150	1.0834	0.7402	68.3
24.0	51.654	4.9294	180	1.2397	0.8873	71.6
24.0	58.226	4.9238	210	1.3974	1.0340	74.0
24.0	64.862	4.918	240	1.5567	1.1803	75.8
24.0	71.559	4.9118	270	1.7174	1.3262	77.2
24.0	78.296	4.9053	300	1.8791	1.4716	78.3
Vin (V)	Iin (mA)	Vout (V)	Iout (mA)	Pin (W)	Pout (W)	Efficiency (%)
26.4	14.3	4.9792	0	0.3775	0.0000	
26.4	19.798	4.9732	30	0.5227	0.1492	28.5
26.4	25.485	4.9683	60	0.6728	0.2981	44.3
26.4	31.253	4.9637	90	0.8251	0.4467	54.1
26.4	37.08	4.9591	120	0.9789	0.5951	60.8
26.4	42.993	4.9546	150	1.1350	0.7432	65.5
26.4	48.962	4.9501	180	1.2926	0.8910	68.9
26.4	54.977	4.9454	210	1.4514	1.0385	71.6
26.4	61.05	4.9401	240	1.6117	1.1856	73.6
26.4	67.155	4.9345	270	1.7729	1.3323	75.1
26.4	73.2	4.9285	300	1.9325	1.4786	76.5

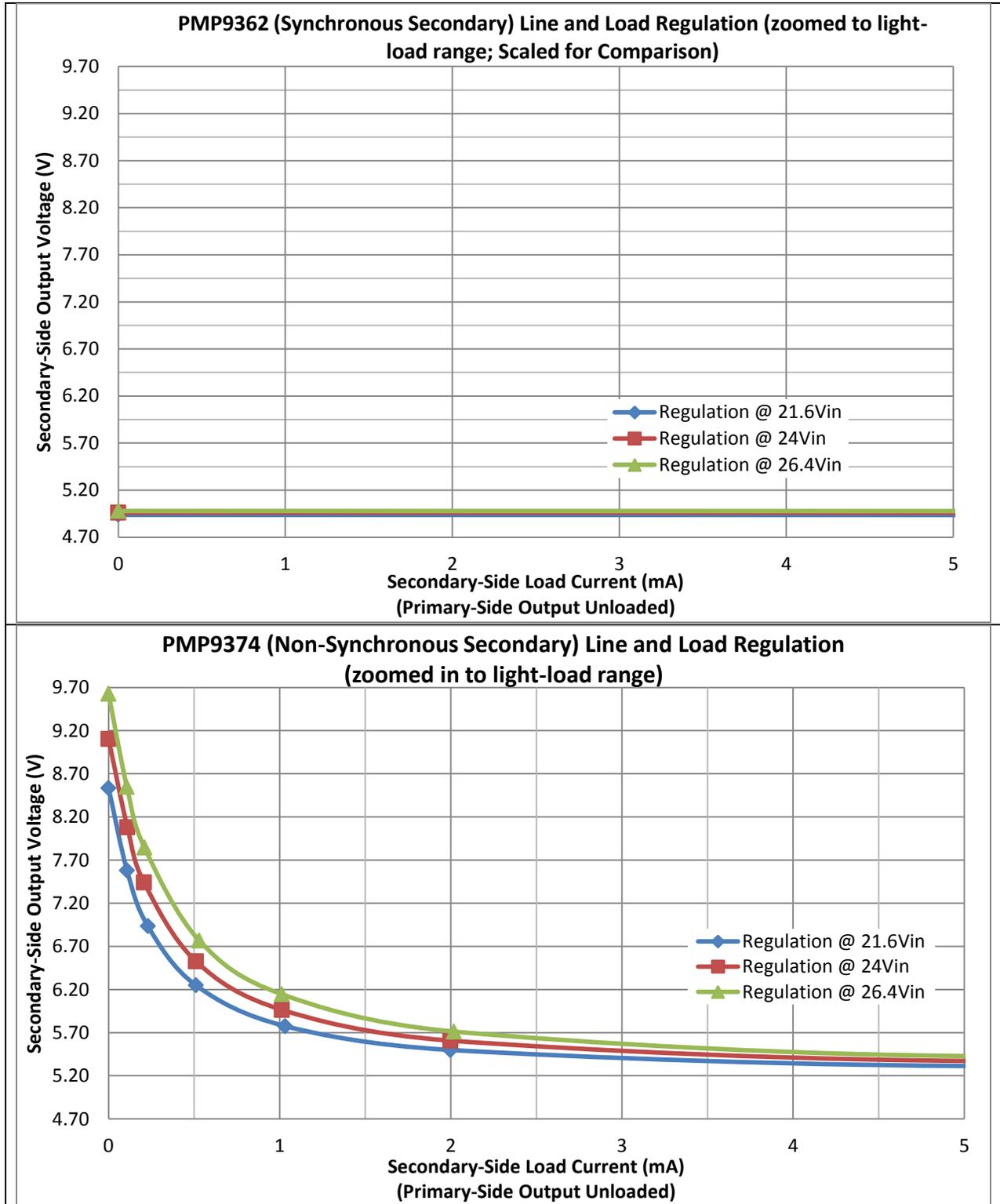
5.4 Line and Load Regulation



5.5 Line and Load Regulation Comparison between Self-Driven Synchronous Rectification and Diode (Non-Synchronous) Rectification

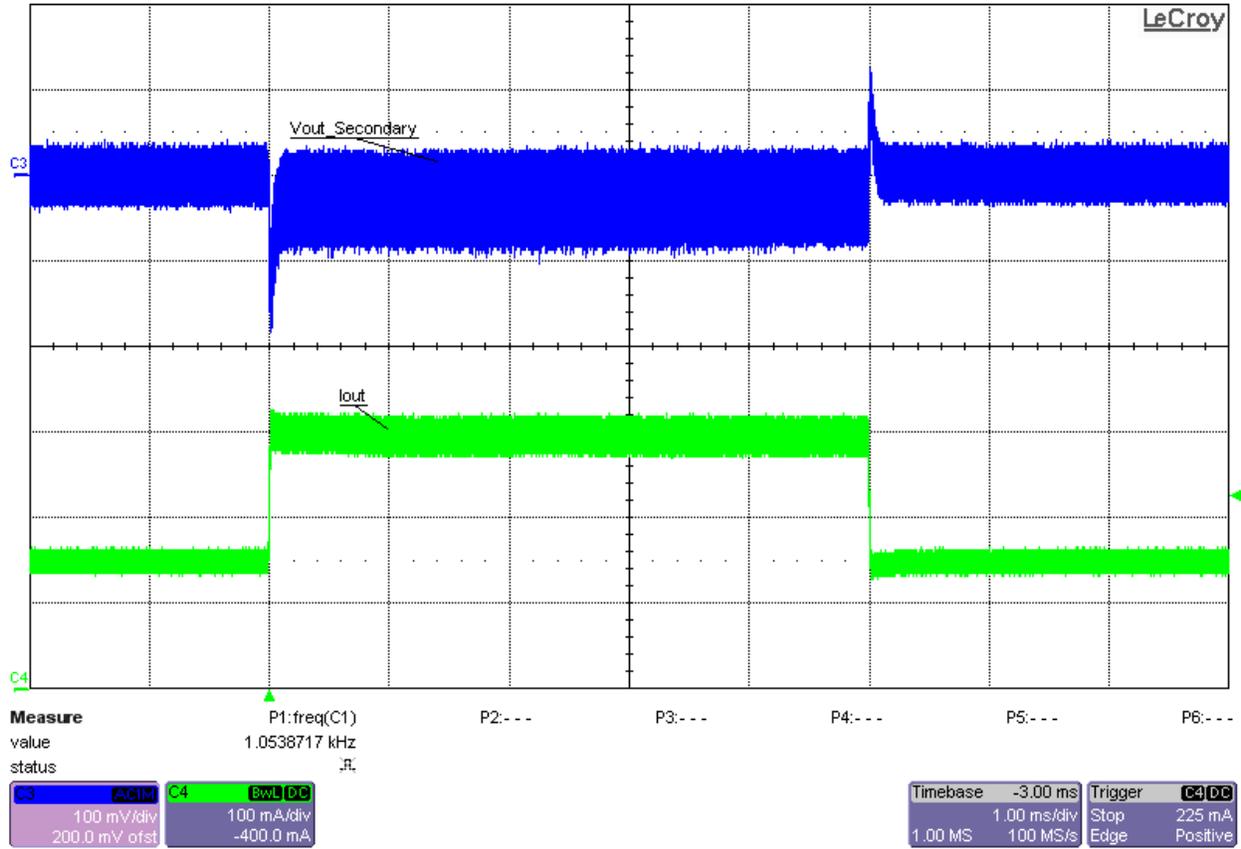


5.6 Line and Load Regulation Comparison between Self-Driven Synchronous Rectification and Diode (Non-Synchronous) Rectification (Zoomed in to light load range)

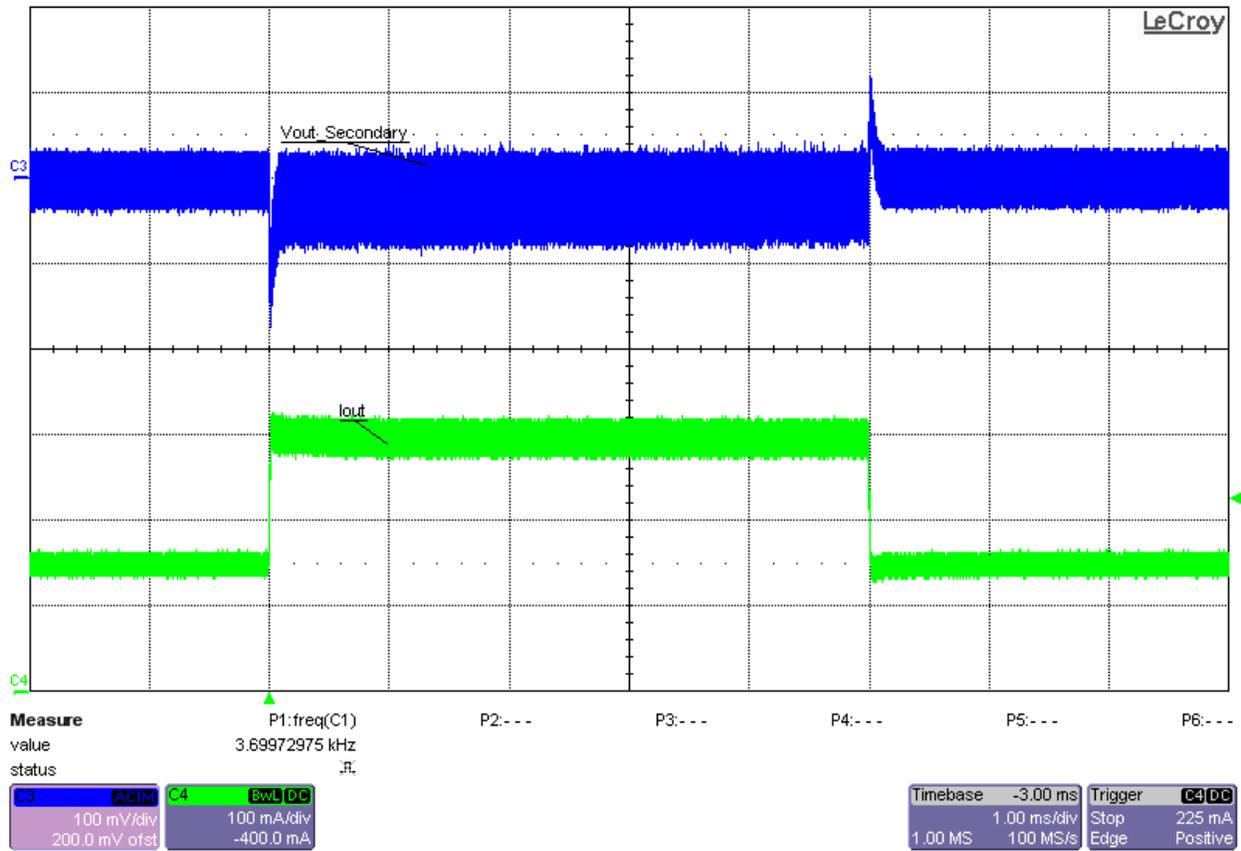


6 Waveforms

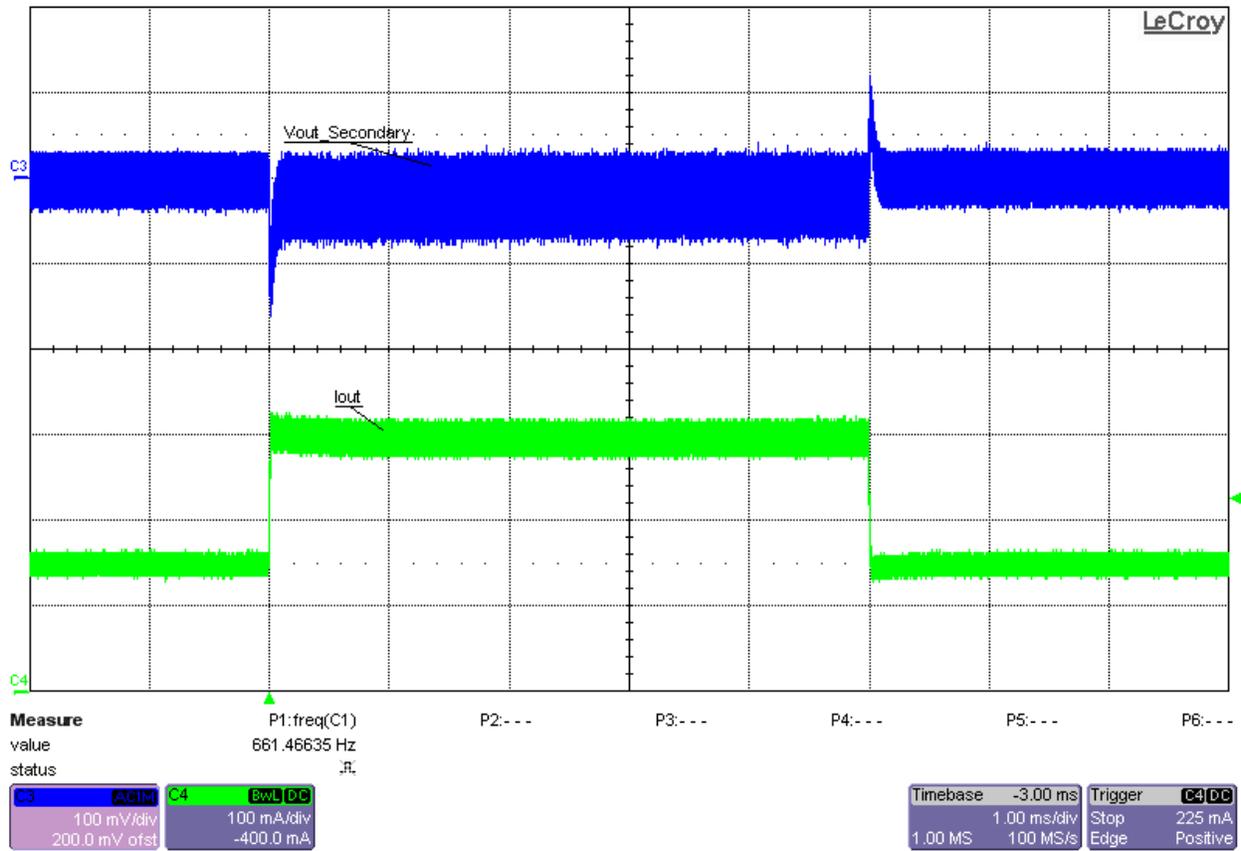
6.1 Load Transient Response



Load Transient Response at 21.6Vin and 50%-to-100% (150mA-to-300mA) Load Step

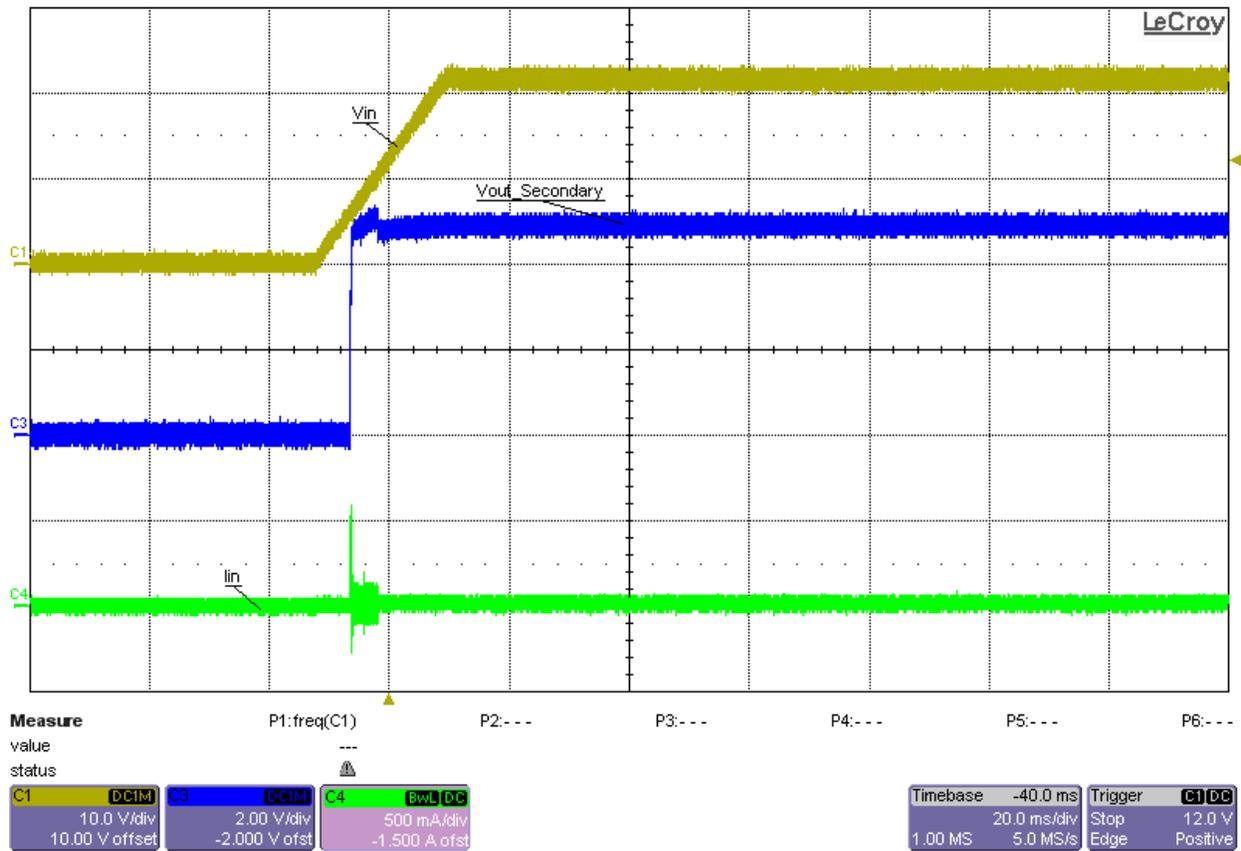


Load Transient Response at 24Vin and 50%-to-100% (150mA-to-300mA) Load Step

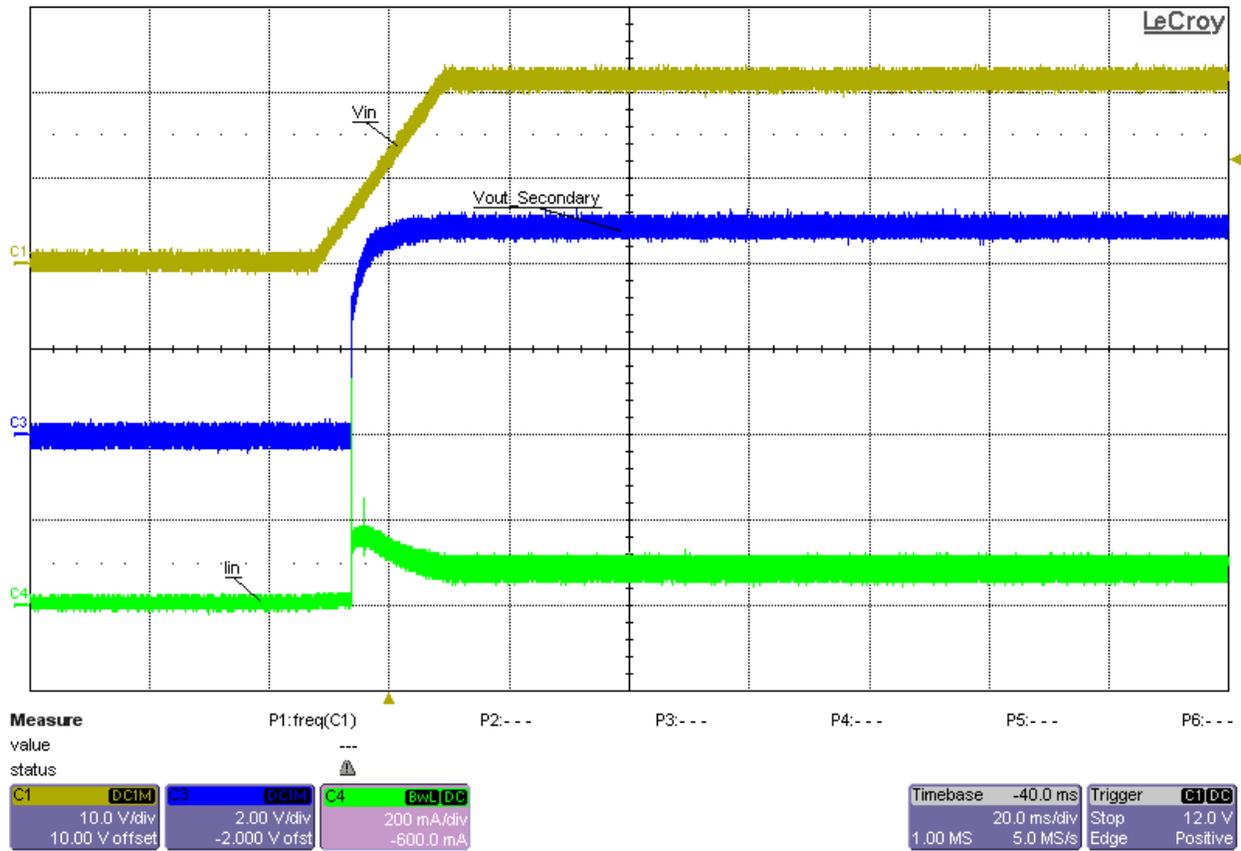


Load Transient Response at 26.4V_{in} and 50%-to-100% (150mA-to-300mA) Load Step

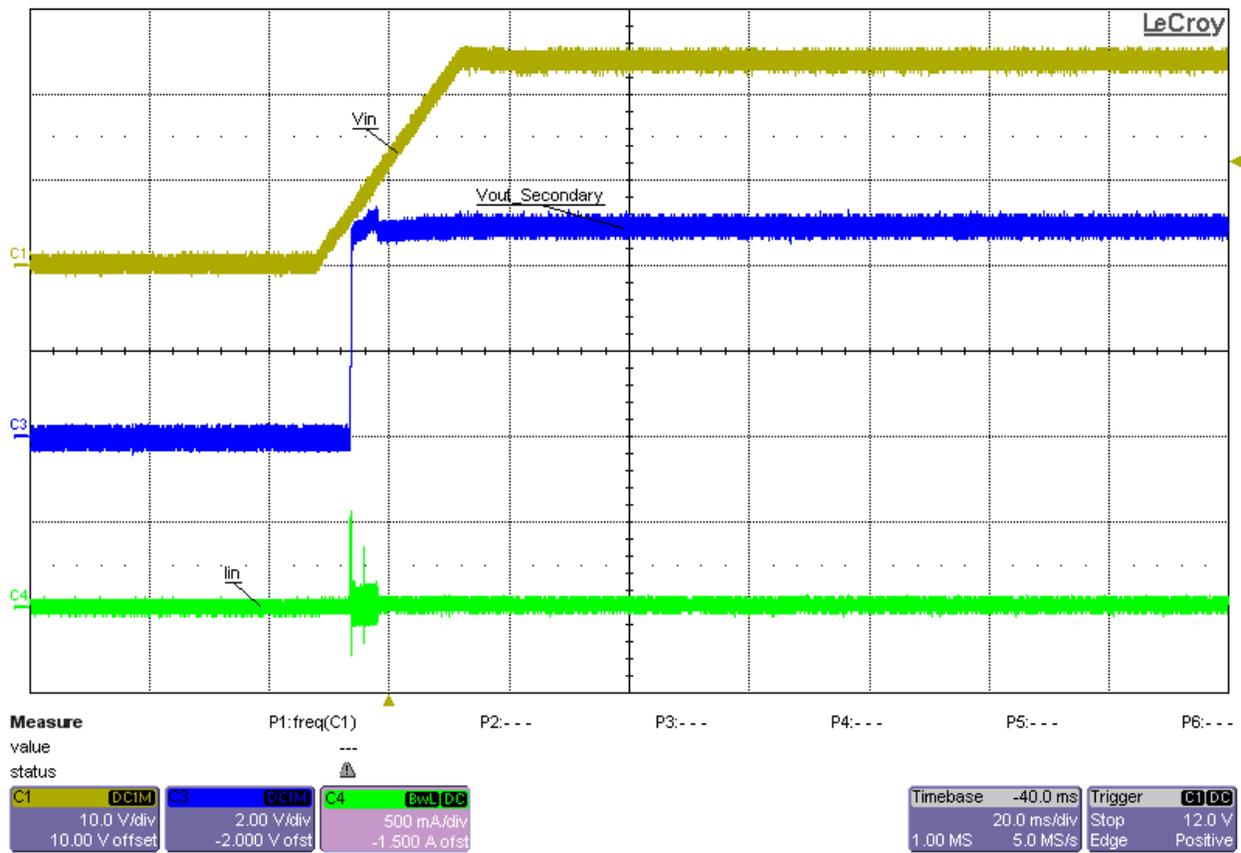
6.2 Startup



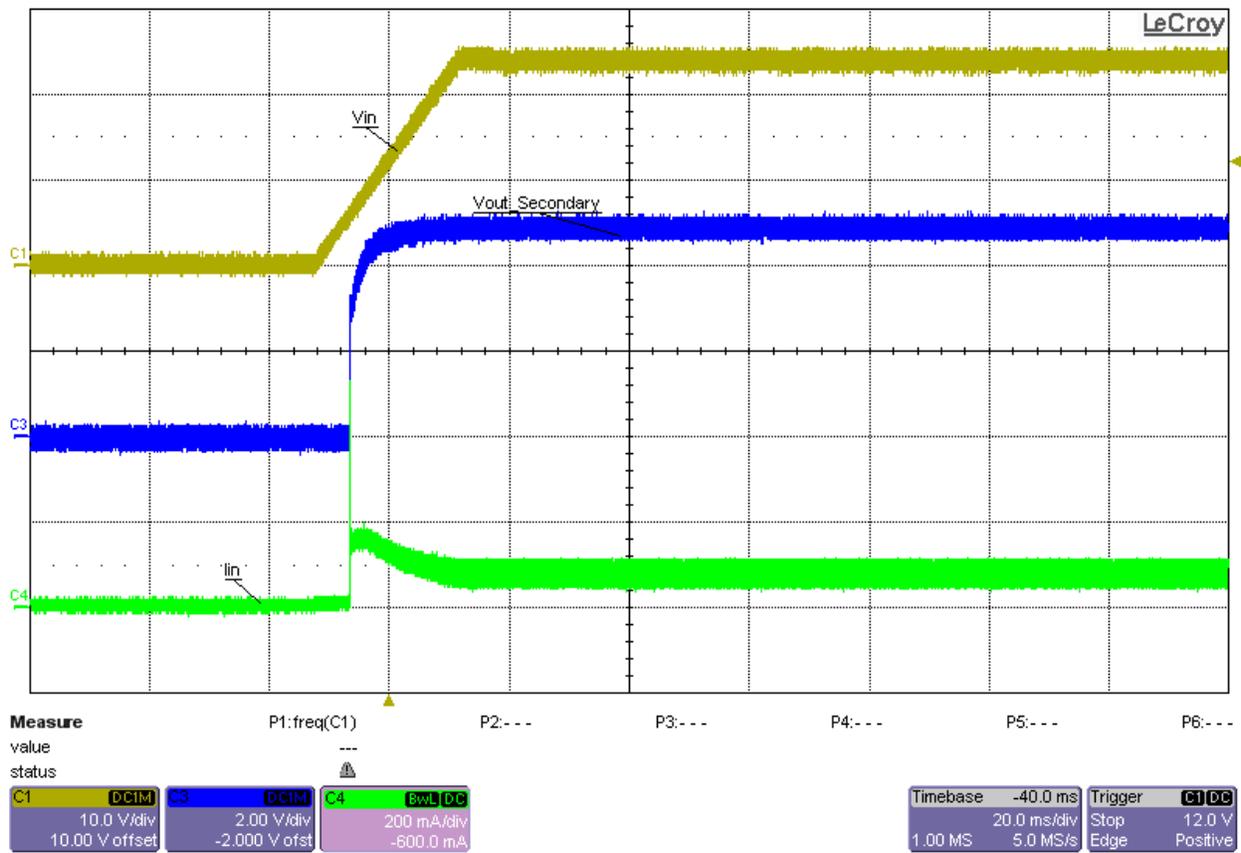
Startup into No Load at 21.6Vin



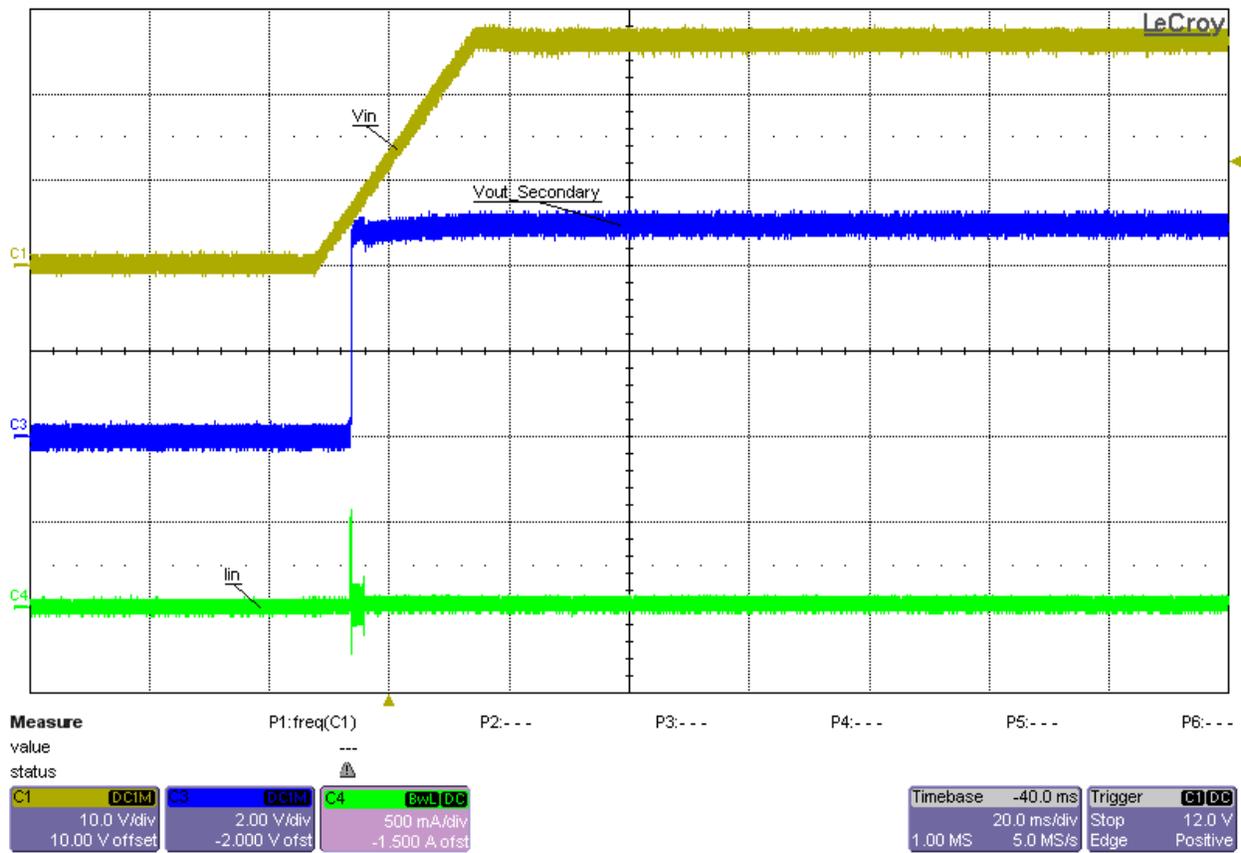
Startup into Full (300mA) Resistive Load at 21.6Vin



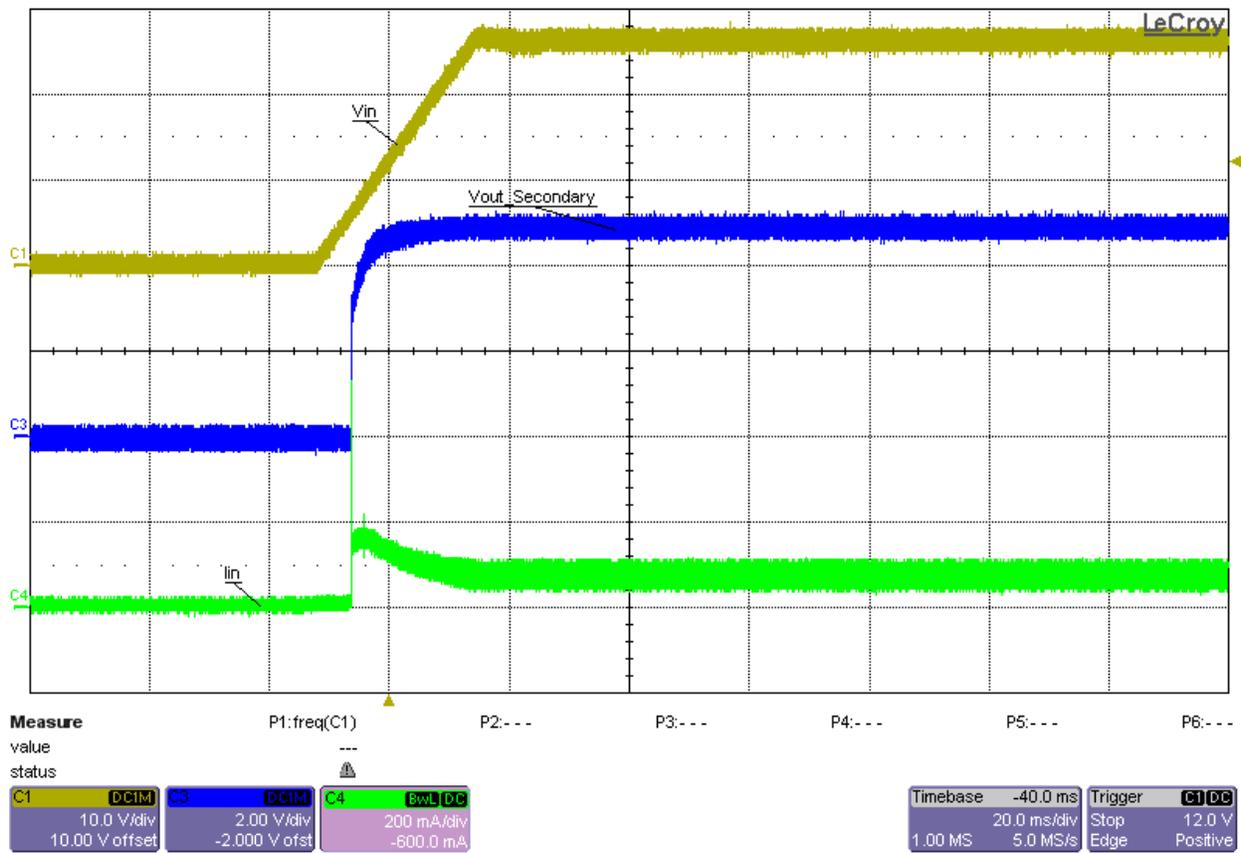
Startup into No Load at 24Vin



Startup into Full (300mA) Resistive Load at 24Vin

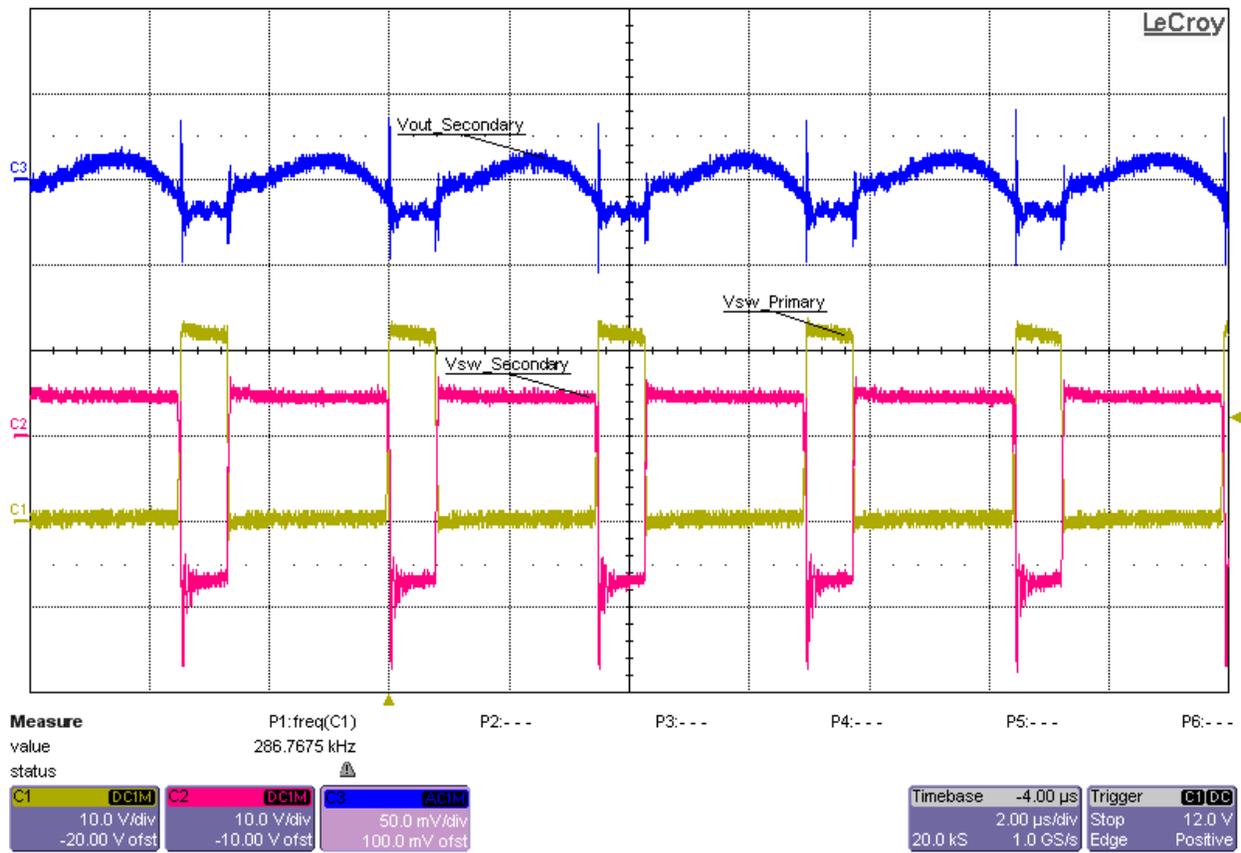


Startup into No Load at 26.4Vin

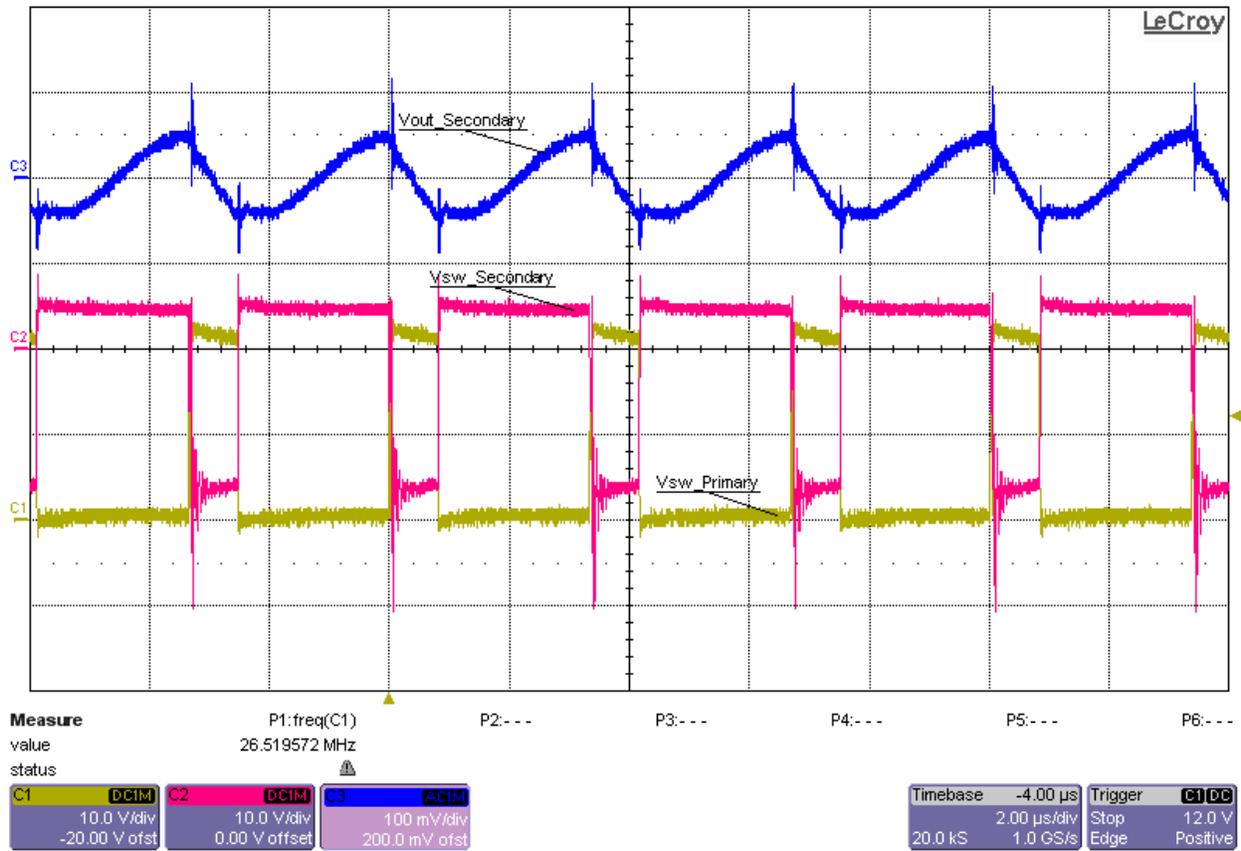


Startup into Full (300mA) Resistive Load at 26.4Vin

6.3 Output Voltage Ripple and Switch Node Voltage

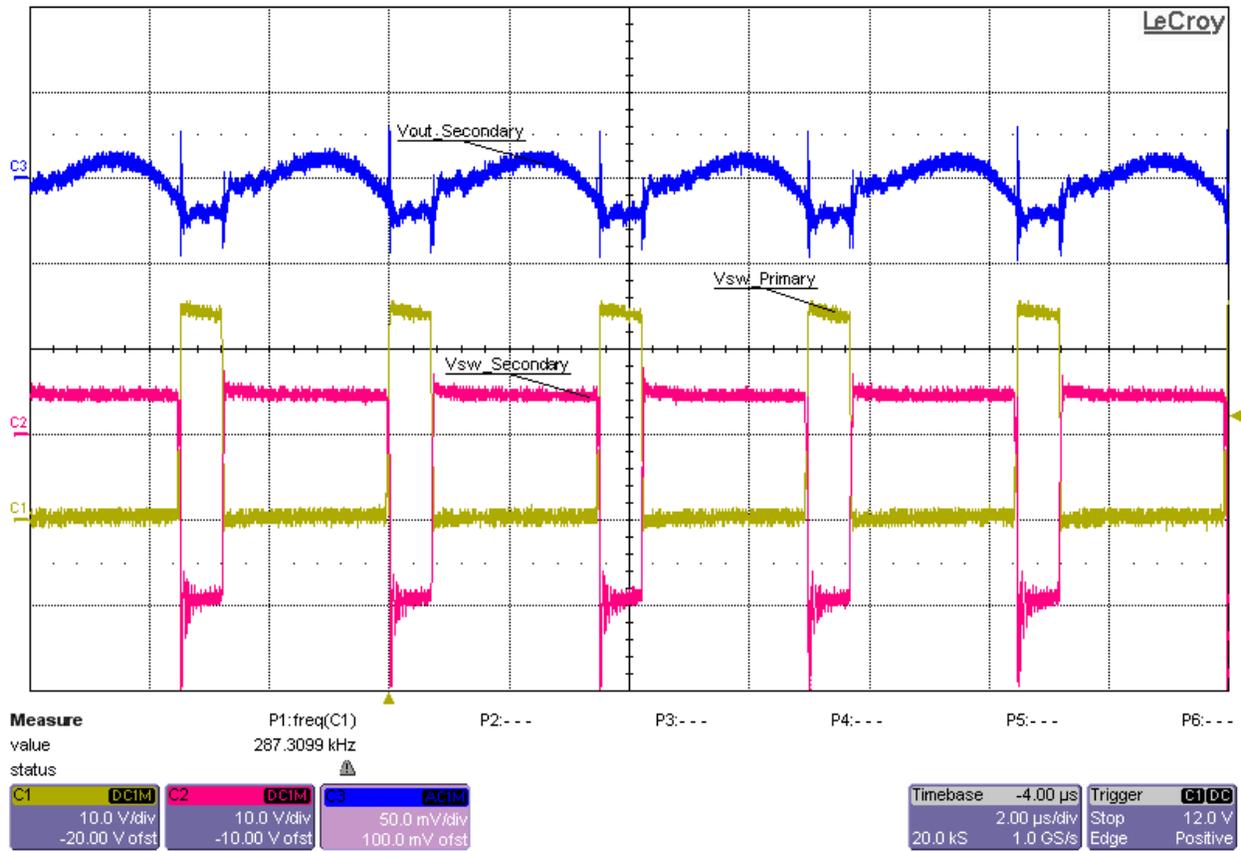


Switch Node and Secondary-Side Output Voltage Ripple at 21.6Vin and No Load (Vripple \approx 30mVp-p)

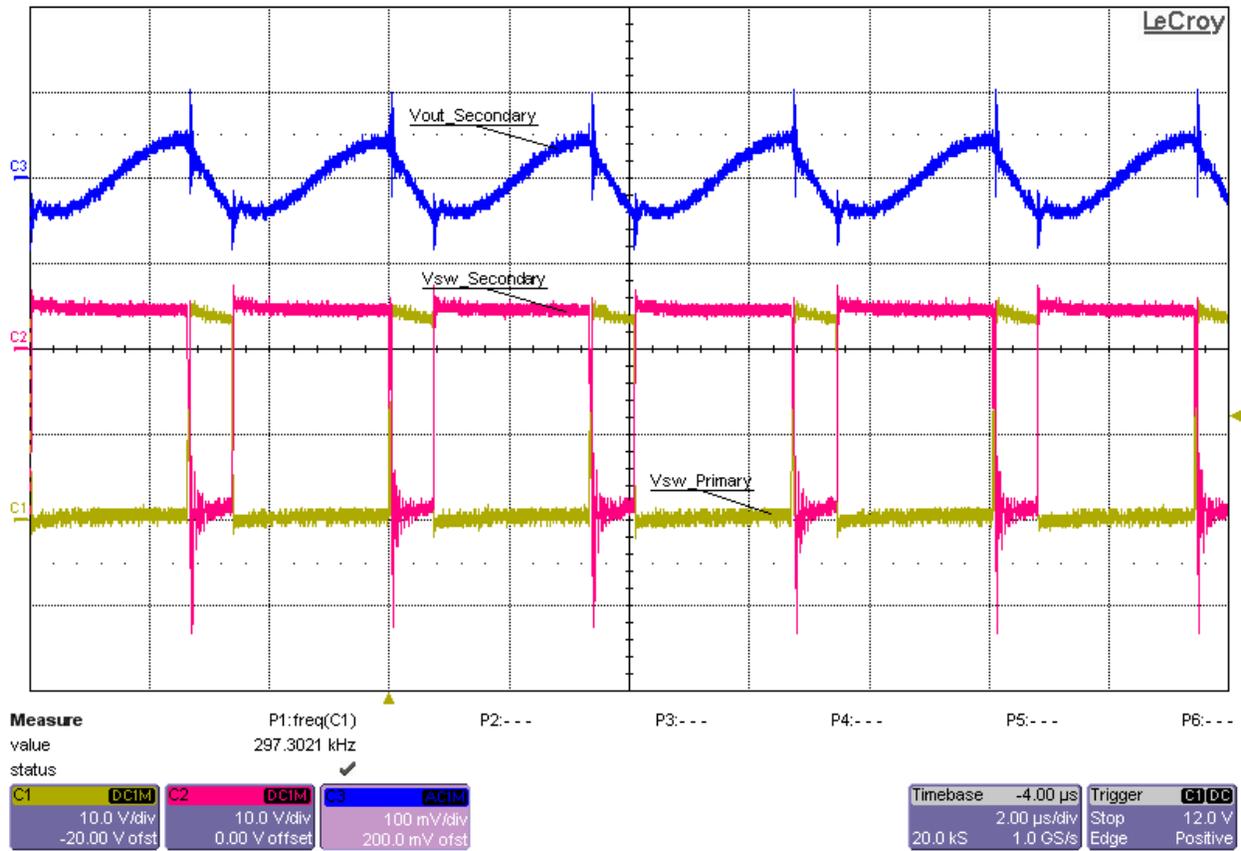


Switch Node and Secondary-Side Output Voltage Ripple at 21.6Vin and Full (300mA) Load

(Vripple \approx 100mVp-p)

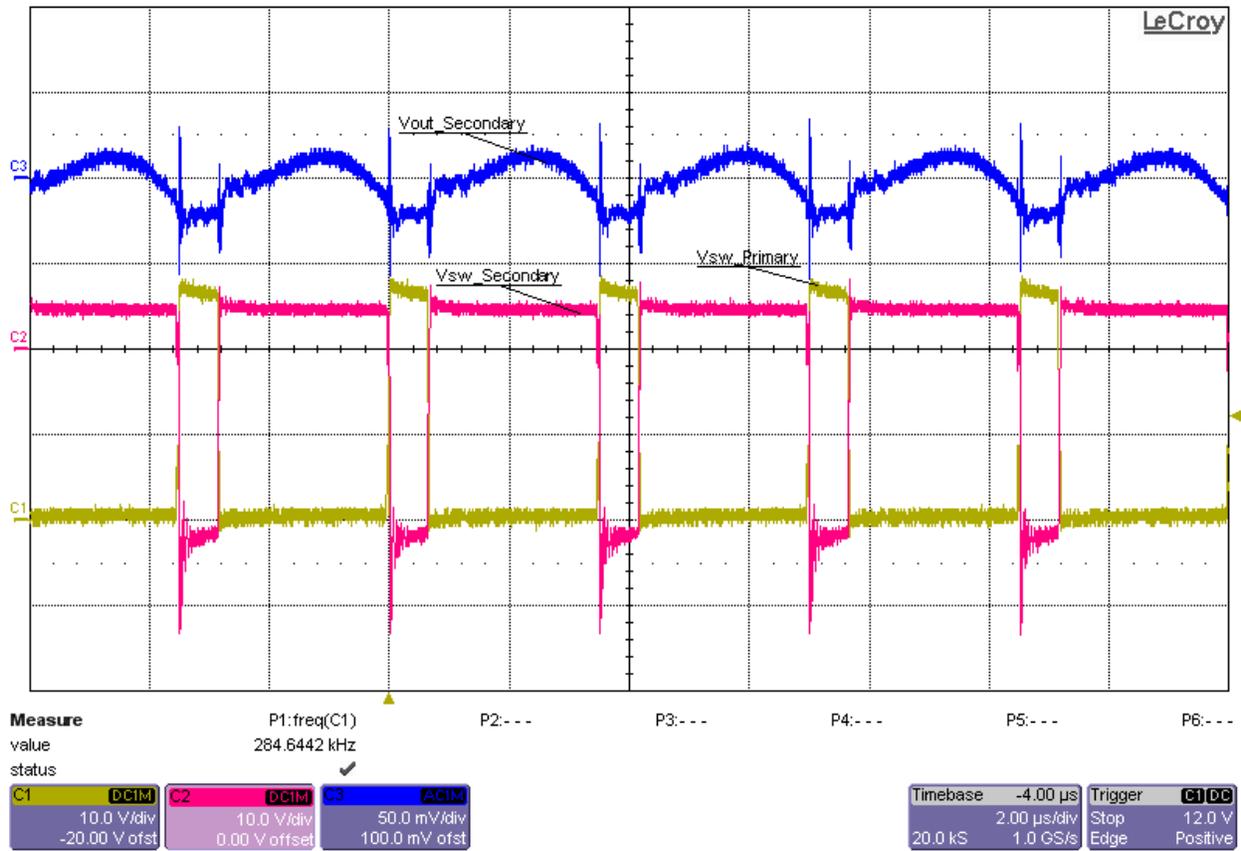


Switch Node and Secondary-Side Output Voltage Ripple at 24Vin and No Load ($V_{ripple} \approx 40mV_{p-p}$)

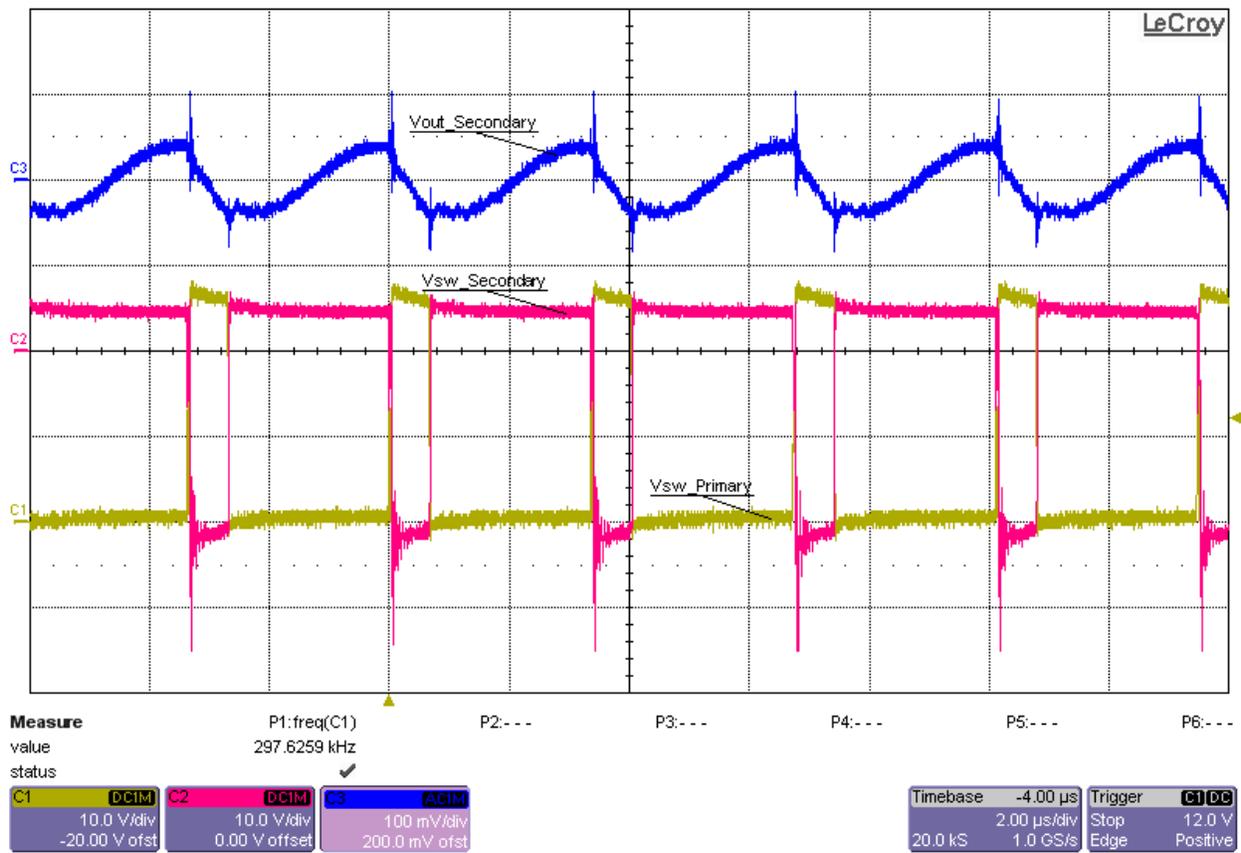


Switch Node and Secondary-Side Output Voltage Ripple at 24Vin and Full (300mA) Load

(Vripple \approx 100mVp-p)



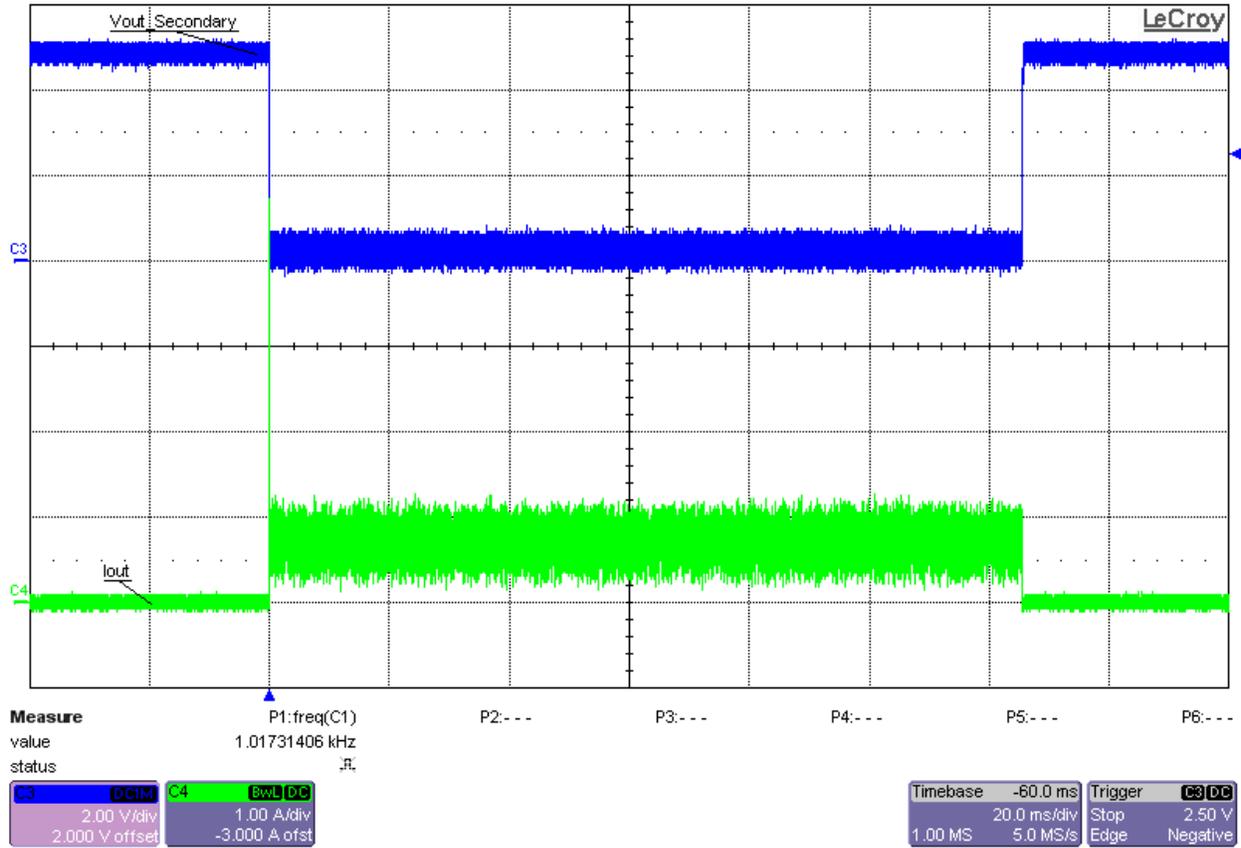
Switch Node and Secondary-Side Output Voltage Ripple at 26.4Vin and No Load ($V_{ripple} \approx 40mVp-p$)



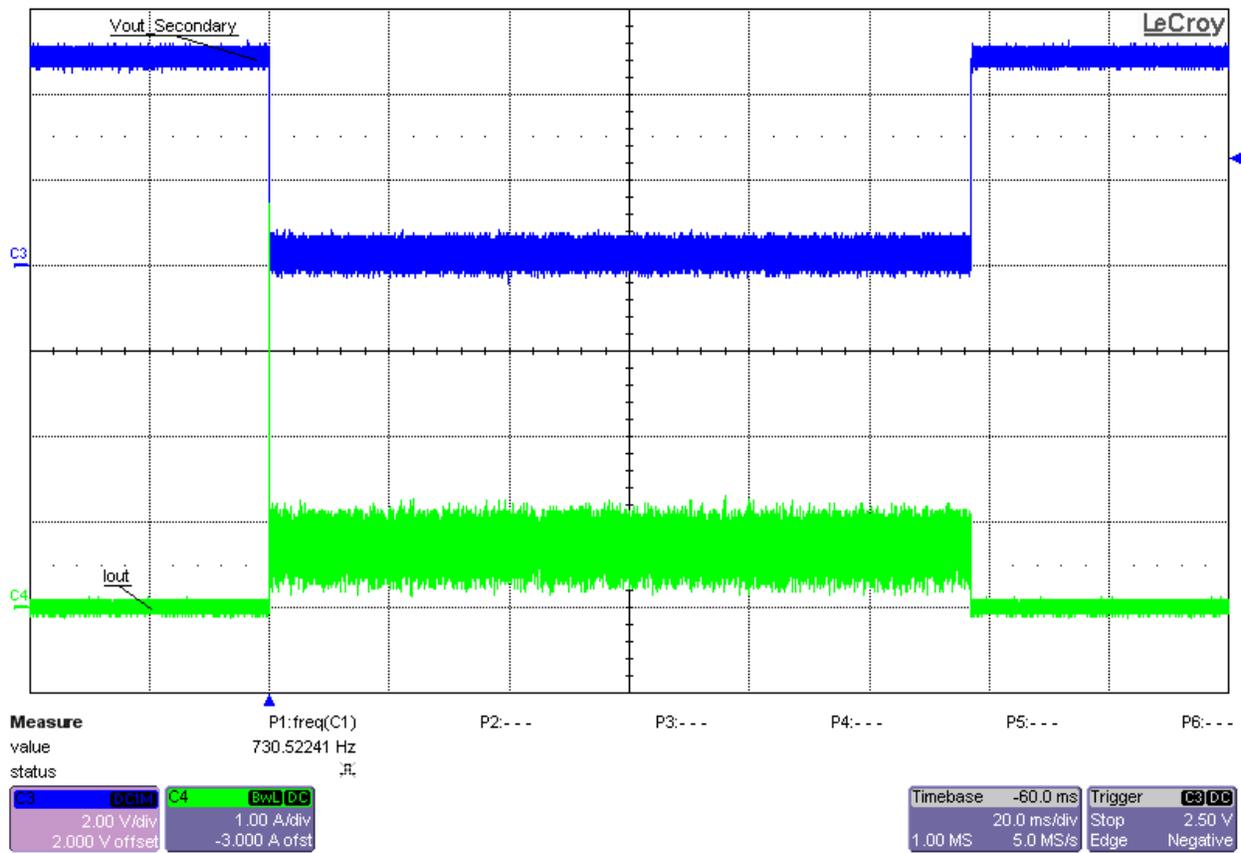
Switch Node and Secondary-Side Output Voltage Ripple at 26.4Vin and Full (300mA) Load

(Vripple \approx 80mVp-p)

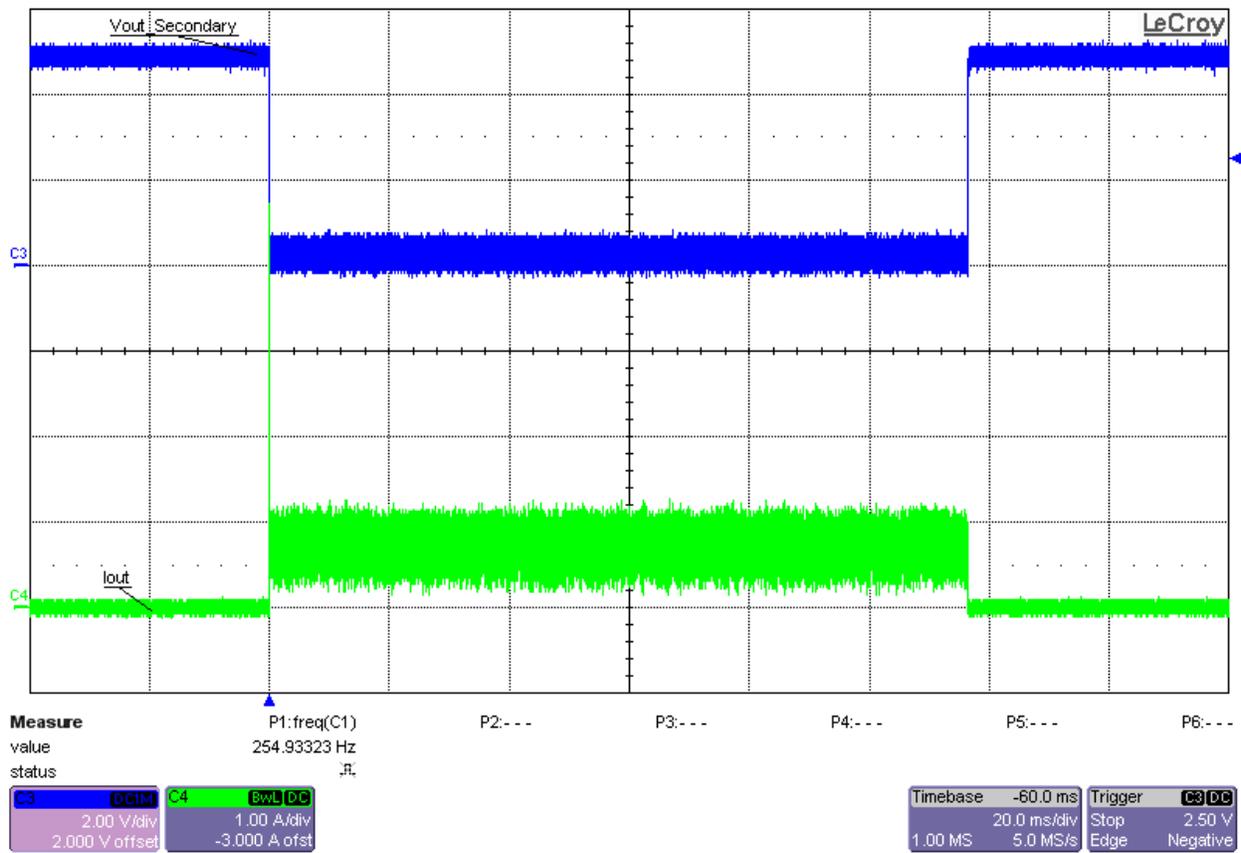
7 Short Circuit Testing



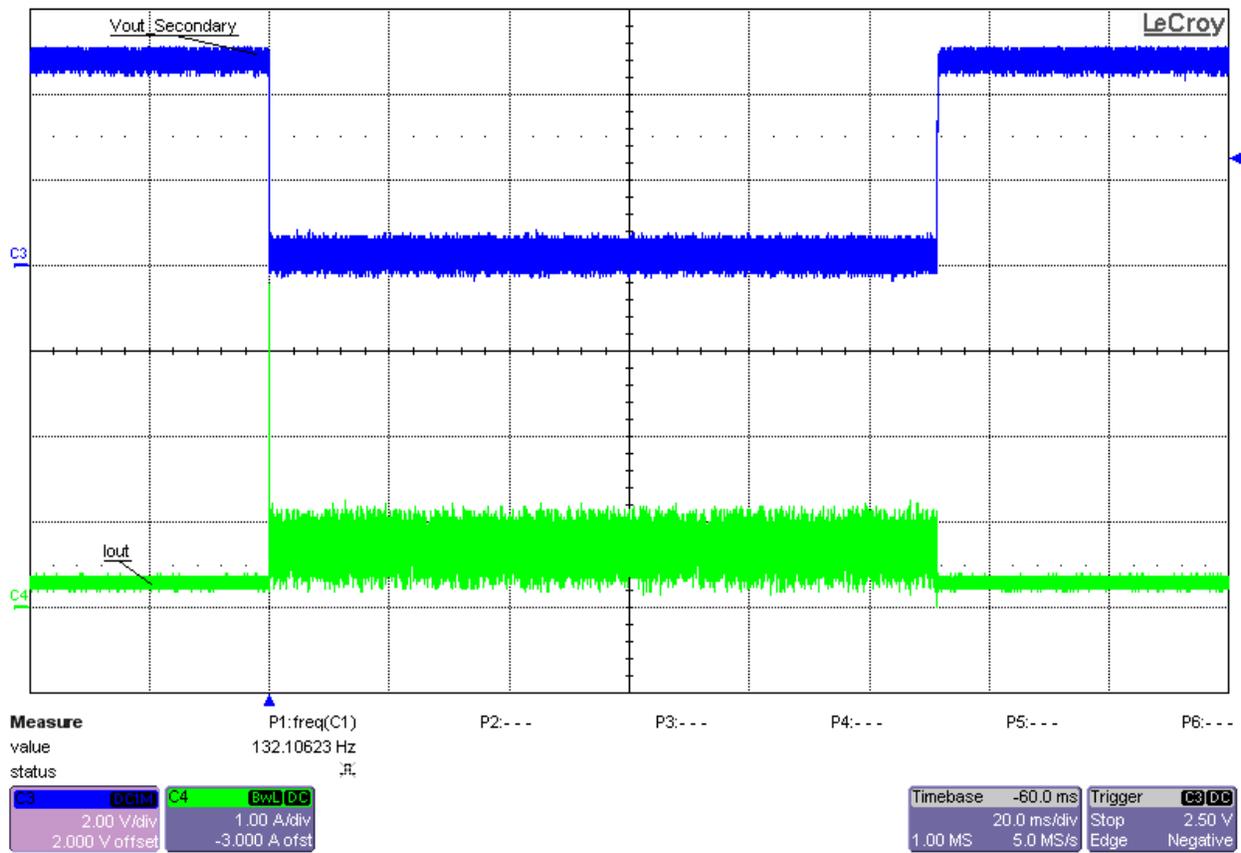
Short Circuit Application and Recovery at 21.6Vin (applied from no load, recovered into no load)



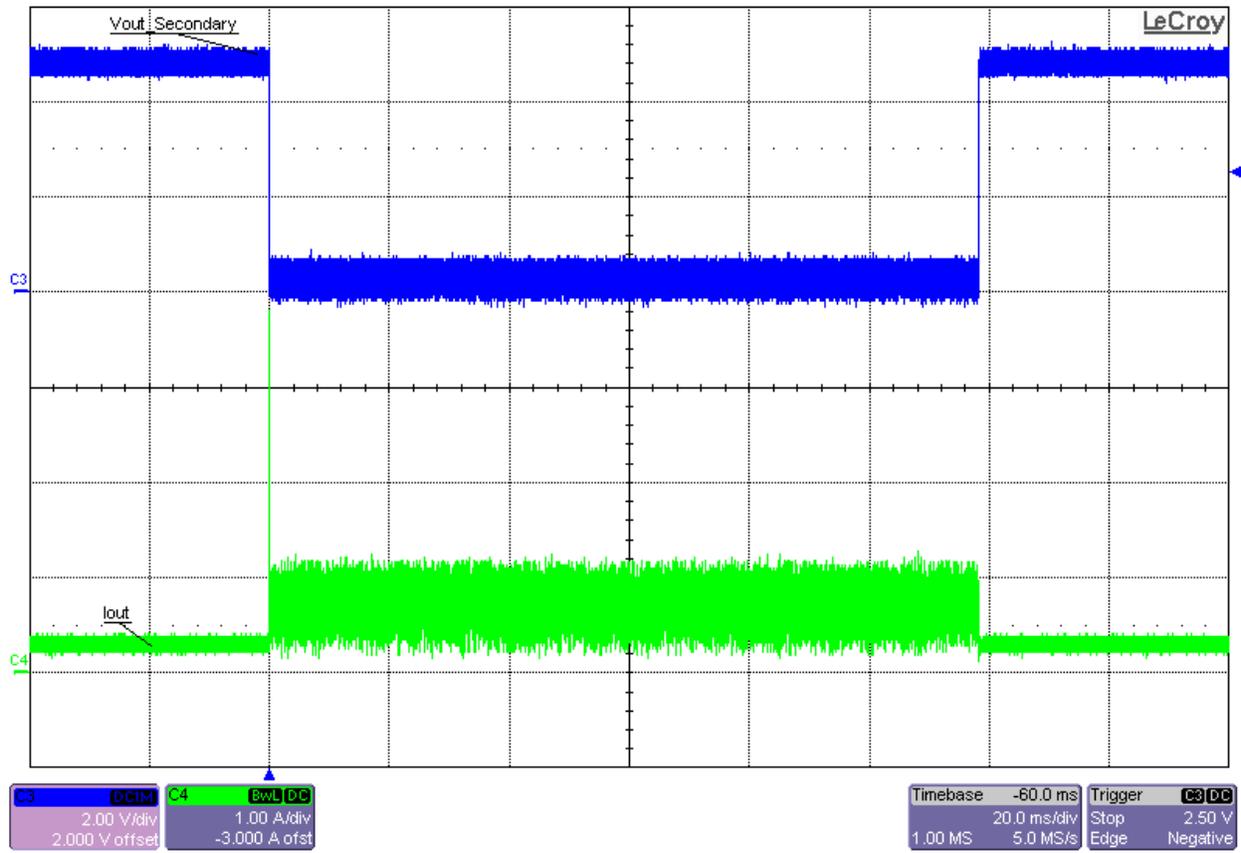
Short Circuit Application and Recovery at 24Vin (applied from no load, recovered into no load)



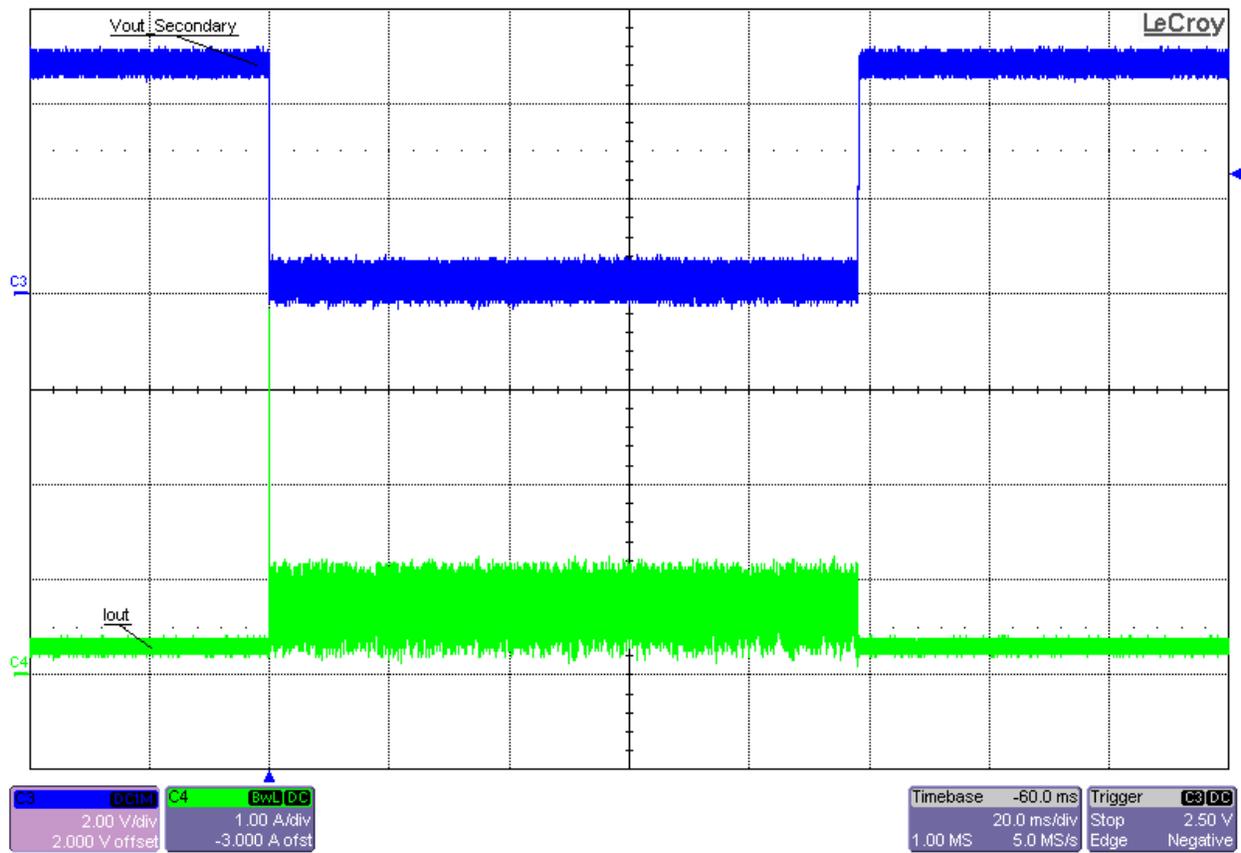
Short Circuit Application and Recovery at 26.4Vin (applied from no load, recovered into no load)



Short Circuit Application and Recovery at 21.6Vin (applied from and recovered into Full 300mA load)



Short Circuit Application and Recovery at 24Vin (applied from and recovered into Full 300mA load)



Short Circuit Application and Recovery at 26.4Vin (applied from and recovered into Full 300mA load)

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