EVM Application #1

Creating a Pulse Width Modulated Signal with a Fixed Duty Cycle Using the TMS320F240 EVM

APPLICATION REPORT: SPRA410

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January 1999

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EVM Application #1

Creating a Pulse Width Modulated Signal with a Fixed Duty Cycle Using the TMS320F240 EVM

Abstract

This document explains how the EVM Application #1 generates a Pulse Width Modulated (PWM) signal and includes the following information.

- ❑ An overview, background and methodology on what the EVM Application #1 is and how it works
- ❑ Listing of the three modules which must be configured
- ❑ Formula for performing period register and compare register value calculations
- ❑ A figure that shows the difference between active high and active low polarity
- ❑ Assembly code for generating a pulse width modulated signal for the target system, the Texas Instruments (TI™) TMS320F240 Evaluation Module (EVM)

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Overview

This application generates a pulse width modulated (PWM) signal asymmetrically (edge-triggered) using C2xx Assembly code. The PWM frequency is 20kHz with a 20% high duty cycle. The algorithm described in this application report was implemented using the TI TMS320F240 EVM.

Module(s) Used

- ❑ Event Manager Module
- ❑ General Purpose Timer 1

Input

None

Output

T1PWM / T1CMP

Background and Methodology

The module used to create the PWM signal is the General Purpose Timer of the Event Manager Module. Although the primary module is the Event Manager Module, other components of the TMS320F240 need to be configured *prior* to creating the PWM signal.

PLL Module

The first module that needs to be configured is the PLL module. The PLL clock module provides all the necessary clock signals for the F240. It is important to know the speed of the CPUCLK in order to create the proper PWM frequency. The PLL receives its CLKIN from the 10MHz crystal oscillator of the EVM. Since the PLL is set up to divide the CLKIN frequency by 2 and then multiply the frequency by 4, the resulting CPUCLK frequency is 20MHz.

Digital I/O Ports

Because the Digital I/O Ports pins are shared with pins of other peripherals of the TMS320F240, the pins necessary to output the PWM signal need to be configured. The PWM output of GP Timer 1 shares its pin with I/O Port B3. If the pin is not configured properly (i.e. the pin is an I/O pin rather than a Timer 1 Output pin), the PWM may be generated internally, but the PWM signal will have no way of being output. As a result, Output Control Register A (OCRA) needs to be configured so that the pin (in this case, pin 105) to be T1PWM/T1CMP instead of IOPB3.

Event Manager Module–General Purpose (GP) Timer

Once the CPUCLK frequency has been determined from the PLL module and the output pin has been configured for the General Purpose Timer 1, the GP Timer 1 in the Event Manager Module can be configured. To create a PWM signal, the registers GPTCON, T1CNT, T1CMPR, T1PR, and T1CON need to be set.

To create an asymmetric PWM signal, the timer is set to the Continuous-Up Count Mode. (If a symmetric PWM signal is desired, then the Timer should be set to the Continuous-Up/Down Count Mode.) Since the CPUCLK is 20MHz, it is easy to obtain a 20kHz signal without pre-scaling the input clock, thus the pre-scale is set to divide by 1. Furthermore, to create a consistent duty cycle for the PWM, the compare register should be loaded when the counter value is 0 or when the counter equals the value in the period register. Since the compare value is constant in this application, the selection of the reload condition for the compare register is not crucial.

In other applications where the compare value will be changed, the reload condition of the compare register becomes important. However, the F240’s compare registers are shadowed, as a result, new compare values can be loaded while a value is present in the compare register without affecting the current value in the register unless the reload condition is to load immediately. The reload condition is determined by bits 3-2 in TxCON.

To create a PWM signal with a specific frequency and duty cycle, the values for the period and the compare registers need to be calculated. In order to calculate the values, the proper CLKIN frequency needs to be known; in this application, the 10MHz crystal that is on the EVM board is used.

Period register value calculation:

$$\text{Period Value} = \frac{\dfrac{\text{CLKIN(OSC)}}{\text{Input Clock Prescaler}} \times \dfrac{\text{PLL Multiplication Ratio}}{\text{PLL Divide by 2}}}{\text{Desired Frequency}}$$

Since the GP Timers start counting from zero, to calculate the value that should be loaded into the period register, 1 should be subtracted from the calculated value obtained to input into register T1PR. Similarly, to find the correct value in the compare register, the duty cycle should be multiplied by the period value and 1 should also be subtracted.

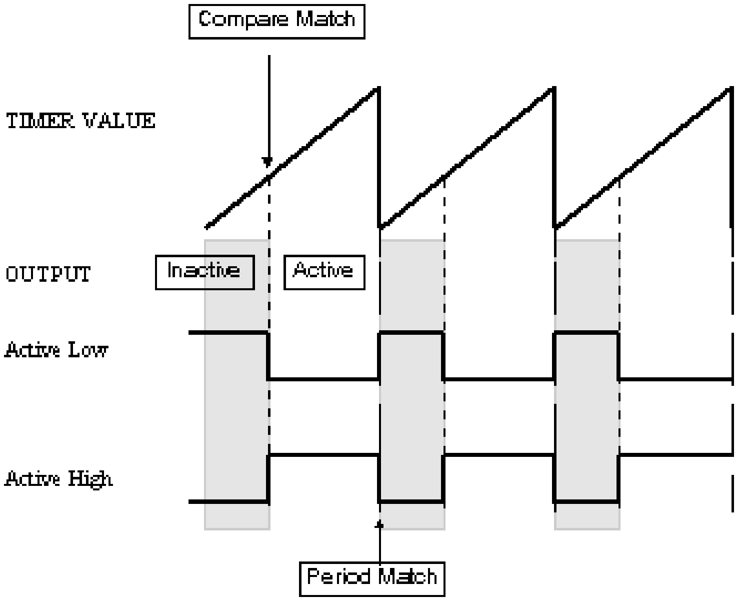
Compare register value calculation:

$$\text{Compare Value} = \text{Period Value} \times \text{Duty Cycle}$$

To determine whether the polarity of the Compare output should be active high or active low, one must understand the difference between the two modes (See Figure 1). If the pin is set to the active low state, during the inactive state, the output will be high and low when active. Setting the output to active high will produce opposite results.

As a result, when the output pin is inactive at the beginning of the period, if set to the active low state, the output will be high, and if it is set to the active high state, the output will be low. When a compare event occurs, the state will switch to active resulting in a low output for the active low state and a high output for the active high state. Depending on the state chosen, the pulse of the PWM signal in the active low state will be at the beginning of the period, and in the active high state, it will be at the end of the period. The point being, if a program is designed with the output pin in the active low state and has a duty cycle of 20%, in the active high state, the same program will have a duty cycle of 80%.

Figure 1. Active High and Active Low Polarity



Once the proper registers have been set to create the PWM signal, the program can be ended (i.e., with an unconditional branch) and the PWM signal will continue to be output until the program stops the signal through software or the program is halted by the user.

```
;*******************************************************************
; File Name:      pwm0.asm
; Originator:     Digital Control Systems Apps group - Houston
; Target System: 'C24x Evaluation Board
;
; Description:    Pulse Width Modulator - Sets up the registers
;                 for an asymmetric PWM output.  The output is a
;                 square wave with a fixed 20% duty cycle.
;                 PWM Period is 0.05ms => 20kHz
;
; Last Updated:    20 June 1997
;
;*******************************************************************
                    .include f240regs.h

;-------------------------------------------------------------------
; Vector address declarations
;-------------------------------------------------------------------
                 .sect ".vectors"

RSVECT           B    START    ; Reset Vector
INT1             B    PHANTOM  ; Interrupt Level 1
INT2             B    PHANTOM  ; Interrupt Level 2
INT3             B    PHANTOM  ; Interrupt Level 3
INT4             B    PHANTOM  ; Interrupt Level 4
INT5             B    PHANTOM  ; Interrupt Level 5
INT6             B    PHANTOM  ; Interrupt Level 6
RESERVED         B    PHANTOM  ; Reserved
SW_INT8          B    PHANTOM  ; User S/W Interrupt
SW_INT9          B    PHANTOM  ; User S/W Interrupt
SW_INT10         B    PHANTOM  ; User S/W Interrupt
SW_INT11         B    PHANTOM  ; User S/W Interrupt
SW_INT12         B    PHANTOM  ; User S/W Interrupt
SW_INT13         B    PHANTOM  ; User S/W Interrupt
SW_INT14         B    PHANTOM  ; User S/W Interrupt
SW_INT15         B    PHANTOM  ; User S/W Interrupt
SW_INT16         B    PHANTOM  ; User S/W Interrupt
TRAP             B    PHANTOM  ; Trap vector
NMINT            B    PHANTOM  ; Non-maskable Interrupt
EMU_TRAP         B    PHANTOM  ; Emulator Trap
SW_INT20         B    PHANTOM  ; User S/W Interrupt
SW_INT21         B    PHANTOM  ; User S/W Interrupt
SW_INT22         B    PHANTOM  ; User S/W Interrupt
SW_INT23         B    PHANTOM  ; User S/W Interrupt


;===================================================================
; M A I N   C O D E  - starts here
;===================================================================
                 .text
                 NOP
START:    SETC   INTM          ;Disable interrupts
```

```
                 SPLK  #0000h,IMR    ;Mask all core interrupts
                 LACC  IFR           ;Read Interrupt flags
                 SACL  IFR           ;Clear all interrupt flags

                 CLRC  SXM           ;Clear Sign Extension Mode
                 CLRC  OVM           ;Reset Overflow Mode
                 CLRC  CNF           ;Config Block B0 to Data mem

;-----------------------------------
; Set up PLL Module
;-----------------------------------
                 LDP   #00E0h

;The following line is necessary if a previous program set the PLL
;to a different setting than the settings which the application;
;uses. By disabling the PLL, the CKCR1 register can be modified so
;that the PLL can run at the new settings when it is re-enabled.

SPLK             #0000000001000001b,CKCR0 ;CLKMD=PLL
Disable,SYSCLK=CPUCLK/2


;                       5432109876543210
                 SPLK  #0000000010111011b,CKCR1
;CLKIN(OSC)=10MHz,CPUCLK=20MHz

;CKCR1 - Clock Control Register 1
;Bits 7-4  (1011)CKINF(3)-CKINF(0) - Crystal or Clock-In Frequency
;                 Frequency = 10MHz
;Bit  3    (1)    PLLDIV(2) - PLL divide by 2 bit
;                 Divide PLL input by 2
;Bits 2-0  (011) PLLFB(2)-PLLFB(0) - PLL multiplication ratio
;                 PLL Multiplication Ration = 4


;                       5432109876543210
                 SPLK  #0000000011000011b,CKCR0 ;CLKMD=PLL ENable,
                                                    SYSCLK=CPUCLK/2

;CKCR0 - Clock Control Register 0
;Bits 7-6  (11)   CLKMD(1),CLKMD(0) - Operational mode of Clock
;                 Module PLL Enabled; Run on CLKIN on exiting low
;                 power mode
;Bits 5-4  (00)   PLLOCK(1),PLLOCK(0) - PLL Status. READ ONLY
;Bits 3-2  (00)   PLLPM(1),PLLPM(0) - Low Power Mode
;                 LPM0
;Bit 1     (0)    ACLKENA - 1MHz ACLK Enable
;                 ACLK Enabled
;Bit 0     (1)    PLLPS - System Clock Prescale Value
;                 f(sysclk)=f(cpuclk)/2
;                       5432109876543210
                 SPLK  #0100000011000000b,SYSCR ;CLKOUT=CPUCLK

;SYSCR - System Control Register
;Bit 15-14 (01)     RESET1,RESET0 - Software Reset Bits
;                   No Action
;Bits 13-8 (000000) Reserved
;Bit 7-6   (11)     CLKSRC1,CLKSRC0 - CLKOUT-Pin Source Select
;                   CPUCLK: CPU clock output mode
;Bit 5-0   (000000) Reserved


  SPLK  #006Fh, WDCR      ;Disable WD if VCCP=5V (JP5 in pos. 2-3)
  KICK_DOG                ;Reset Watchdog


;-----------------------------------
; Set up Digital I/O Port
;-----------------------------------
                 LDP   #225  ;DP=225, Data Page to Configure OCRA
;                       5432109876543210
                 SPLK  #0011100000000000b,OCRA

;OCRA  - Output Control Register A
;Bit 15    (0)   CRA.15 - IOPB7
;Bit 14    (0)   CRA.14 - IOPB6
;Bit 13    (1)   CRA.13 - T3PWM/T3CMP
;Bit 12    (1)   CRA.12 - T2PWM/T2CMP
;Bit 11    (1)   CRA.11 - T1PWM/T1CMP
;Bit 10    (0)   CRA.10 - IOPB2
;Bit 9     (0)   CRA.9 - IOPB1
;Bit 8     (0)   CRA.8 - IOPB0
;Bits 7-4  (0000)Reserved
;Bit 3     (0)   CRA.3 - IOPA3
;Bit 2     (0)   CRA.2 - IOPA2
;Bit 1     (0)   CRA.1 - IOPA1
;Bit 0     (0)   CRA.0 - IOPA0


;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
;- Event Manager Module Reset
;*
;-This section resets all of the Event Manager Module Registers.
;*This is necessary for silicon revsion 1.1; however, for
;-silicon revisions 2.0 and later, this is not necessary
;*
;-
;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*

LDP              #232          ;DP=232 Data Page for the Event
                               ;Manager
SPLK             #0000h,GPTCON ;Clear General Purpose Timer Control
SPLK             #0000h,T1CON  ;Clear GP Timer 1 Control
SPLK             #0000h,T2CON  ;Clear GP Timer 2 Control
SPLK             #0000h,T3CON  ;Clear GP Timer 3 Control

SPLK             #0000h,COMCON ;Clear Compare Control
SPLK             #0000h,ACTR   ;Clear Full Compare Action Control
                               ;Register
SPLK             #0000h,SACTR  ;Clear Simple Compare Action Control
                               ;Register
SPLK             #0000h,DBTCON ;Clear Dead-Band Timer Control
                               ;Register

SPLK             #0000h,CAPCON ;Clear Capture Control

SPLK             #0FFFFh,EVIFRA;Clear Interrupt Flag Register A
SPLK             #0FFFFh,EVIFRB;Clear Interrupt Flag Register B
SPLK             #0FFFFh,EVIFRC;Clear Interrupt Flag Register C

SPLK             #0000h,EVIMRA ;Clear Event Manager Mask Register A
SPLK             #0000h,EVIMRB ;Clear Event Manager Mask Register B
SPLK             #0000h,EVIMRC ;Clear Event Manager Mask Register C

;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
;-               End of RESET section for silicon revision 1.1
;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*

;-----------------------------------
; Set up Event Manager Module
;-----------------------------------
T1COMPARE        .set  200        ;T1Compare 20% of T1Period
T1PERIOD         .set  1000       ;T1Period value = 20kHz signal


                 LDP   #232       ;DP=232, Data Page for Event
                                  ;Manager Addresses
                 SPLK  #T1COMPARE,T1CMPR   ;Compare value for
                                           ; 20% duty cycle

;                       2109876543210
                 SPLK  #0000001010101b,GPTCON

;GPTCON - GP Timer Control Register
;Bit 15    (0)   T3STAT - GP Timer 3 Status.  READ ONLY
;Bit 14    (0)   T2STAT - GP Timer 2 Status.  READ ONLY
;Bit 13    (0)   T1STAT - GP Timer 1 Status.  READ ONLY
;Bits 12-11(00)  T3TOADC - ADC start by event of GP Timer 3
;                No event starts ADC
;Bits 10-9 (00)  T2TOADC - ADC start by event of GP Timer 2
;                No event starts ADC
;Bits 8-7  (00)  T1TOADC - ADC start by event of GP Timer 1
;                No event starts ADC
;Bit 6     (1)   TCOMPOE - Compare output enable
```

```
;                Enable all three GP timer compare outputs
;Bits 5-4  (01)  T3PIN - Polarity of GP Timer 3 compare output
;                Active Low
;Bits 3-2  (01)  T2PIN - Polarity of GP Timer 2 compare output
;                Active Low
;Bits 1-0  (01)  T1PIN - Polarity of GP Timer 1 compare output
;                Active Low

                 SPLK  #T1PERIOD,T1PR ;Period value for 20kHz signal
                 SPLK  #0000h,T1CNT   ;Clear GP Timer 1 Counter
                 SPLK  #0000h,T2CNT   ;Clear GP Timer 2 Counter
                 SPLK  #0000h,T3CNT   ;Clera GP Timer 3 Counter


;                       5432109876543210
                 SPLK  #0001000000000010b,T1CON

;T1CON - GP Timer 1 Control Register
;Bits 15-14(00)  FREE,SOFT - Emulation Control Bits
;                Stop immediately on emulation suspend
;Bits 13-11(010) TMODE2-TMODE0 - Count Mode Selection
;                Continuous-Up Count Mode
;Bits 10-8 (000) TPS2-TPS0 - Input Clock Prescaler
;                Divide by 1
;Bit 7     (0)   Reserved
;Bit 6     (0)   TENABLE - Timer Enable
;                Disable timer operations
;Bits 5-4  (00)  TCLKS1,TCLKS0 - Clock Source Select
;                Internal Clock Source
;Bits 3-2  (00)  TCLD1,TCLD0 - Timer Compare Register Reload
;                Condition When counter is 0
;Bit 1     (1)   TECMPR - Timer compare enable
;                Enable timer compare operation
;Bit 0     (0)   Reserved

;                      5432109876543210
                 SPLK #0000000000000000b,T2CON  ;GP Timer 2-Not Used

;T2CON - GP Timer 2 Control Register
;Bits 15-14(00)  FREE,SOFT - Emulation Control Bits
;                   Stop immediately on emulation suspend
;Bits 13-11(000) TMODE2-TMODE0 - Count Mode Selection
;                   Stop/Hold
;Bits 10-8 (000) TPS2-TPS0 - Input Clock Prescaler
;                   Divide by 1
;Bit 7     (0)   TSWT1 - GP Timer 1 timer enable bit
;                   Use own TENABLE bit
;Bit 6     (0)   TENABLE - Timer Enable
;                   Disable timer operations
;Bits 5-4  (00)  TCLKS1,TCLKS0 - Clock Source Select
;                   Internal Clock Source
;Bits 3-2  (00)  TCLD1,TCLD0 - Timer Compare Register Reload
```

```
;                   Condition When counter is 0
;Bit 1     (0)   TECMPR - Timer compare enable
;                   Disable timer compare operation
;Bit 0     (0)   SELT1PR - Period Register select
;                   Use own period register

;                       5432109876543210
                 SPLK  #0000000000000000b,T3CON  ;GP Timer 3-Not Used

;T3CON - GP Timer 3 Control Register
;Bits 15-14(00)  FREE,SOFT - Emulation Control Bits
;                   Stop immediately on emulation suspend
;Bits 13-11(000) TMODE2-TMODE0 - Count Mode Selection
;                   Stop/Hold
;Bits 10-8 (000) TPS2-TPS0 - Input Clock Prescaler
;                   Divide by 1
;Bit 7     (0)   TSWT1 - GP Timer 1 timer enable bit
;                   Use own TENABLE bit
;Bit 6     (0)   TENABLE - Timer Enable
;                      Disable timer operations
;Bits 5-4  (00)  TCLKS1,TCLKS0 - Clock Source Select
;                   Internal Clock Source
;Bits 3-2  (00)  TCLD1,TCLD0 - Timer Compare Register Reload
;                   Condition When counter is 0
;Bit 1     (0)   TECMPR - Timer compare enable
;                   Disable timer compare operation
;Bit 0     (0)   SELT1PR - Period Register select
;                   Use own period register

SBIT1            T1CON,B6_MSK     ;Sets Bit 6 of T1CON

;T1CON - GP Timer 1 Control Register
;Bit 6     (1)   TENABLE - Timer Enable
;                   Enable Timer Operations

END              B  END

;===================================================================
; I S R  -  PHANTOM
;
; Description:   Dummy ISR, used to trap spurious interrupts.
;
; Modifies:      Nothing
;
; Last Update:   16 June 95
;===================================================================
PHANTOM          KICK_DOG         ;Resets WD counter
                 B  PHANTOM
```