



Application Report SPRA883 – December 2002

OMAP System DMA Throughput Analysis

Bill Winderweedle

DSP Catalog and EEE, Device Applications

ABSTRACT

The OMAP[™] architecture devices contain a nine-channel system DMA, useable for block transfers of data without intervention by the TIARM925T MPU or the TMSC55x DSP. This application report describes optimization techniques for improving throughput. Examples are given for using external memories such as SDRAM and SRAM for transferring data to and from internal memory. Internal memory transfers are also discussed.

Contents

1	Introduction	۱	3
2	System Set	q	3
	2.1 Periphe	ral Registers Setup	4
3	Throughput	Analysis Examples	6
	3.1 SDMA	Fransfers with EMIFS Destination	7
	3.1.1	_ogic Analyzer Images of EMIFS to EMIFS System DMA Transfers	8
	3.2 SDMA	Fransfers with EMIFF Destination	11
	3.2.1	_ogic Analyzer Images of EMIFF to EMIFF System DMA Transfers	12
	3.3 SDMA	Fransfers with IMIF Destination	15
	3.4 SDMA	Transfers with MPUI Destination	17
4	Conclusion	5	18
5	References		18
Арр	endix A ON	IAP Block Diagram	19
Арр	endix B MF	PU Memory Map	20
Арр	endix C EN	IIFS Behavior	21
Арр	endix D EN	IIFF Behavior	22

List of Figures

Figure 1	Code Segment for Logic Analyzer Trigger, DMA Enable, and
-	Transfer End Polling Loop
Figure 2	System DMA EMIFS Reads and Writes (No Burst, 16-bit)
Figure 3	System DMA EMIFS Reads and Writes (No Burst, 32-bit)
Figure 4	System DMA EMIFS Read (Burst of 4 by 16-bit)10
Figure 5	System DMA EMIFS Write (Burst of 4 by 16-bit)10
Figure 6	System DMA EMIFS Read (Burst of 4 by 32-bit)10
Figure 7	System DMA EMIFS Write (Burst of 4 by 32-bit)1

Trademarks are the property of their respective owners.

SPRA883

Figure 8	System DMA EMIFF Reads and Write (No Burst, 16-bit)	13
Figure 9	System DMA EMIFF Reads (No Burst, 32-bit)	13
Figure 10	System DMA EMIFF Writes (No Burst, 32-bit)	14
Figure 11	System DMA EMIFF Read (Burst of 4 x 16-bit)	14
Figure 12	System DMA EMIFF Write (Burst of 4 x 16-bit)	14
Figure 13	System DMA EMIFF Read (Burst of 4 x 32-bit)	15
Figure 14	System DMA EMIFF Write (Burst of 4 x 32-bit)	15
Figure A–1	OMAP Block Diagram	19

TEXAS INSTRUMENTS

List of Tables

Table 1	Clock Setup	3
Table 2	Transfer Sources, Destinations, Types, ARM Addresses	6
Table 3	IMIF Transfers to EMIFS: Latency, Throughput	7
Table 4	EMIFS Transfers to EMIFS: Latency, Throughput	7
Table 5	EMIFF Transfers to EMIFS: Latency, Throughput	8
Table 6	MPUI Transfers to EMIFS: Latency, Throughput	8
Table 7	IMIF Transfers to EMIFF: Latency, Throughput	11
Table 8	EMIFS Transfers to EMIFF: Latency, Throughput	11
Table 9	EMIFF Transfers to EMIFF: Latency, Throughput	12
Table 10	MPUI Transfers to EMIFF: Latency, Throughput	12
Table 11	IMIF Transfers to IMIF: Latency, Throughput	15
Table 12	EMIFS Transfers to IMIF: Latency, Throughput	16
Table 13	EMIFF Transfers to IMIF: Latency, Throughput	16
Table 14	MPUI Transfers to IMIF: Latency, Throughput	16
Table 15	IMIF Transfers to MPUI: Latency, Throughput	17
Table 16	EMIFS Transfers to MPUI: Latency, Throughput	17
Table 17	EMIFF Transfers to MPUI: Latency, Throughput	17
Table 18	MPUI Transfers to MPUI: Latency, Throughput	18
Table B–1	MPU Memory Map	20
Table C–1	EMIFS Cycle Behavior with ARM I/D-Caches Disabled,	
	EMIFS_PRIO = 0x00000000, and EMIFS_CS3_CONFIG.FCLKDIV=TC/2	21
Table C–2	EMIFS /CS Active Widths for Asynchronous Reads/Writes	21
Table D–1	EMIFF Behavior for Single and Burst Reads/Writes (TC Cycles)	22



1 Introduction

The OMAP architecture devices contain a nine-channel system DMA, useable for block transfers of data without intervention by the ARM9TDMI MPU or the C55x DSP. This application report analyzes the throughput between some of the possible sources and destinations using the SDMA. Optimization techniques for improving throughput are discussed.

2 System Setup

The following were used in the course of creating this applications report:

- A test board with external Samsung K4S561632C-TL75 256M-bit SDRAM and 512KB Samsung K6T4016U3C-TB70 SRAM
- OMAP Code Composer Studio v2.0 for TIARM925 MPU and C55X DSP
- Tektronix TLA714 Logic Analyzer
- POMAP5910CGZG

The OMAP5910 MPU and DSP clocks were set up for 150MHz operation. The OMAP5910 Traffic Controller (TC) clock was set up for 75MHz operation. The system DMA (SDMA) and internal SRAM (IMIF) run at the same speed as the TC. The slow external memory interface (EMIFS) connected to asynchronous SRAM was clocked at 37.5MHz, with 3 waitstates (WS) for reads and 1 WS for writes, with a write enable length (WELEN) of 1. The fast external memory interface (EMIFF) connected to SDRAM was clocked at 75MHz with a CAS latency of 2. The MPUI division factor (DIVF) for APIF_HNSTROBE was set to 2. All clock domains, peripherals, and SDMA channels unnecessary for performing the throughput analysis were disabled. The clock related settings are summarized in Table 1.

Table 1. Clock Set	up
--------------------	----

DSP	MPU	MPUI	TC/IMIF/SDMA	EMIFF		EMIFS				
150MHz	150MHz	DIVF 2	75MHz	75MHz	CAS 2	37.5MHz	WELEN 1	3WS Rd	1WS Wr	

A combination of ARM assembly and unoptimized C code was used for performing the system DMA transfers on a single channel. The ARM code executed from EMIFS SRAM. Test setup and results tables were stored in internal IMIF. The MPUI port was configured for shared access mode. The DSP executed in a polling loop within SARAM0, located at DSP starting address 0x10000. Iterations of tests were run both with and without ARM I-cache enabled.

The external latency time was measured using a GPIO pin as a logic analyzer trigger. After the GPIO pin was driven high in the test code, the dma channel was directly enabled. No internal or external sync events were used. Latency was not measured where both the source and destination for the transfer were contained within IMIF or DSP internal memory accessed through MPUI. The EMIFS addresses and data busses were observed on the logic analyzer for the cycle of the code fetch where the DMACCR register was set. The latency was derived in TC cycles from the EMIFS code fetch cycle. Therefore, some overhead is included.

Average throughput was measured using an ARM timer peripheral running at 6 MHz. The timer was enabled in code before the logic analyzer was enabled and disabled, after a polling loop detected the end of the transfer. The timer values were scaled to derive the TC cycle count. A code segment used to enable and measure the throughput is shown in Figure 1.

SPRA883

```
// Enable ARM timers
RunTimersOneTwoThree();
// Set MPUIO 3 high, use this for logic analyzer trigger
ARMIO_SET_GPIO_BIT(ARMIO_HIGH,3);
// Enable DMA channel 0
DMA_EnableChannel(DMA_CHANNEL_0);
// Polling Channel 0 Status registers bit 'FrameEnd'
while((DMA_ACC(NO_GLOB_REG,
DMA_CHANNEL_0,DMA_CSR)&(0x0001<<SYSDMA_DMA_CSR_CHX_FRAME_POS))==0);
// Disable ARM timers
StopTimersOneTwoThree();</pre>
```

Figure 1. Code Segment for Logic Analyzer Trigger, DMA Enable, and Transfer End Polling Loop

2.1 Peripheral Registers Setup

TC was configured as follows:

- EMIFS_PRIO, EMIFF_PRIO, and IMIF_PRIO settings
 - 31:16 reserved
 - 15:12 LB host set to 000b for single transfers, not used in this analysis
 - 11:8 System DMA set to 0000b and 1111b for 1 and 16 consecutive transfers while other ports are waiting. The larger number provides optimal throughput at the expense of the other ports.
 - 7 reserved
 - 6:4 DSP (CPU or DMA) set to 000b for single transfers, not used in this analysis
 - 3 reserved
 - 2:0 ARM set to 000b for single transfers, ARM EMIFS code fetch (EMIFS_PRIO) affected the transfers in this analysis. IMIF result table writes were not factored into this analysis because this occurred at the end of the test, after the system DMA transfer was completed.
- EMIFS_CONFIG_REG = 0x00000012
 - Boot mode was set for CS3 space at 0x0000000
- EMIFS_CS3_CONFIG = 0x00001139
 - WELEN=1, WRWST=1, RDWST=3, FLCLKDIV=TC/2
- EMIFF_SDRAM_CONFIG = 0x101D4F4
 - SDF1 frequency range, auto-refresh enabled and calculated from SDRAM data sheet for minimum, 16-bit bus, 256 M bits, 4 banks



- EMIFF_MRS = 0x0000027
 - CAS latency 2, full-page burst length
- TIMEOUT1 = TIMEOUT2 = TIMEOUT3 = 0x0000000
- ENDIANISM = 0x0000000
 - Little-endian

SDMA was configured for channel 0 operation as follows:

- DMA_GCR = 0x000000C
 - Clock autogating on, free
- DMA_CSDP = various
 - No burst and 16-bit, no burst and 32-bit, source and destination burst 4 and 16/32-bit
- DMA_CCR = 0xA060
 - Source and destination single index, entire frame is transferred
- DMA_CICR = 0x0009
 - Frame and timeout interrupts enabled
- DMA_CSSA_L = various
- DMA_CSSA_U = various
- DMA_CDSA_L = various
- DMA_CDSA_U = various
- DMA_CEN = 0x4e20 and 0x2710
 - 20,000 and 10,000 elements
- DMA_CFN = 1
 - Single frame
- DMA_CFI = 1
 - Single frame index
- DMA_CEI = 1
 - Single element index

3 Throughput Analysis Examples

Throughput examples were generated for transfers between all combinations of EMIFF, EMIFS, IMIF, and MPUI. Transfers of 10Kx32-bits and 20Kx16-bits were done *without* burst; transfers of 10Kx32-bits and 20Kx16-bits were done *with* burst. MPUI burst is not supported, but transfers with a different type of source or destination were examined. Table 2 summarizes the types of transfers and the ARM memory map source and destination addresses.

		Transfe	Destination			
Transfer Source	IMIF	EMIFS	EMIFF	MPUI		
IMIF	Src:0x20002000	Src:0x20002000	Src:0x20002000	Src:0x20002000		
	Dest:0x20007000	Dest:0x00040000	Dest:0x10002000	Dest:0xE0014000		
	20Kx16 no burst	20Kx16 no burst	20Kx16 no burst	20Kx16 no burst		
	10Kx32 no burst	10Kx32 no burst	10Kx32 no burst	10Kx32 no burst		
	20Kx16 burst 4	20Kx16 burst 4	20Kx16 burst 4	20Kx16 burst 4		
	10Kx32 burst 4	10Kx32 burst 4	10Kx32 burst 4	10Kx32 burst 4		
EMIFS	Src:0x00000000	Src:0x00000000	Src:0x00000000	Src:0x0000000		
	Dest:0x20002000	Dest:0x00040000	Dest:0x1000C000	Dest:0xE0014000		
	20Kx16 no burst	20Kx16 no burst	20Kx16 no burst	20Kx16 no burst		
	10Kx32 no burst	10Kx32 no burst	10Kx32 no burst	10Kx32 no burst		
	20Kx16 burst 4	20Kx16 burst 4	20Kx16 burst 4	20Kx16 burst 4		
	10Kx32 burst 4	10Kx32 burst 4	10Kx32 burst 4	10Kx32 burst 4		
EMIFF	Src:0x10002000	Src:0x10002000	Src:0x10002000	Src:0x10002000		
	Dest:0x20002000	Dest:0x00040000	Dest:0x1000C000	Dest:0xE0014000		
	20Kx16 no burst	20Kx16 no burst	20Kx16 no burst	20Kx16 no burst		
	10Kx32 no burst	10Kx32 no burst	10Kx32 no burst	10Kx32 no burst		
	20Kx16 burst 4	20Kx16 burst 4	20Kx16 burst 4	20Kx16 burst 4		
MPUI	Src:0xE0000000	Src:0xE0000000	Src:0xE0000000	Src:0xE0000000		
	Dest:0x20002000	Dest:0x00040000	Dest:0x10002000	Dest:0xE0015000		
	20Kx16 no burst	20Kx16 no burst	20Kx16 no burst	20Kx16 no burst		
	10Kx32 no burst	10Kx32 no burst	10Kx32 no burst	10Kx32 no burst		
	20Kx16 burst 4	20Kx16 burst 4	20Kx16 burst 4	Burst not supported		
	10Kx32 burst 4	10Kx32 burst 4	10Kx32 burst 4			

Table 2. Transfer Sources, Destinations, Types, ARM Addresses

NOTE: MPUI burst is not supported. All other memories used in this analysis are supported by System DMA bursts.

Logic analyzer data was captured to detect the latency for the first read of an external dma transfer source and the first write of an external dma destination. Latency was not measured for internal memory sources and destinations. Throughput data was derived for the average number of 16-bit words per TC cycle. A transfer of a single element was measured and subtracted from the large block transfers to remove overhead. Throughput was measured with ARM I-cache enabled/disabled and the priority for dma at a minimum 0 and maximum 15.

In the following sections, examples are given for the various transfers between external and internal memories.

3.1 SDMA Transfers with EMIFS Destination

System DMA transfers with EMIFS as the destination and various sources are shown in Table 3, through Table 6.

		Latency (1	C cycles)	Average Throughput (TC cycles per 16-bit wo				
IMIF Source	Src:0x20002000	First read		I-cache	I-cache enabled			
EMIFS Destination	Dest:0x20007000		First write	DMA Priority 0	DMA Priority 15	DMA priority 15		
	20Kx16 no burst	Internal	121.4	35.0	14.0	14.0		
	10Kx32 no burst	Internal	121.4	22.5	12.0	12.0		
	20Kx16 burst 4	Internal	121.4	13.1	10.5	10.5		
	10Kx32 burst 4	Internal	121.4	13.1	10.5	10.5		

Table 3. IMIF Transfers to EMIFS: Latency, Throughput

Since code is being fetched from EMIFS by the MPU, this negatively impacts the system DMA writes. Use of dma priority 15, while keeping the MPU at dma priority 0, results in greater than 2x of improvement in average throughput. However, the cache does not provide improvement in this case, because the code segment used for the transfer is relatively small. Bursting improves throughput for all cases of I-cache enabled/disabled or priority settings.

Table 4. EMIFS Transfers to EMIFS: Latency, Throughput

		Latency (1	C cycles)	Average Throughput (TC cycles per 16-bit word				
EMIFS Source	Src:0x00000000	First read		I-cache	I-cache enabled			
EMIFS Destination	Dest:0x20002000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15		
	20Kx16 no burst	114.9	167.1	72.0	30.0	30.0		
	10Kx32 no burst	114.9	212.1	46.0	25.0	25.0		
	20Kx16 burst 4	114.9	227.9	26.5	24.2	24.2		
	10Kx32 burst 4	114.9	227.9	26.5	24.2	24.2		

Similar improvements for priority, and bursting hold true for EMIFS to EMIFS.

		Latency (T	C cycles)	Average Throughput (TC cycles per 16-bit word)			
EMIFF Source	Src:0x10002000	First read		I-cache	I-cache enabled		
EMIFS Destination	Dest:0x20002000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15	
	20Kx16 no burst	96.9	121.4	35.0	14.0	14.0	
	10Kx32 no burst	96.9	121.4	22.5	12.0	12.0	
	20Kx16 burst 4	96.9	121.4	13.1	10.6	10.6	
	10Kx32 burst 4	96.9	121.4	13.1	10.6	10.6	

Table 5. EMIFF Transfers to EMIFS: Latency, Throughput

The throughput data for EMIFF to EMIFS transfers is nearly identical to IMIF to EMIFS transfers. The EMIFS writes are the dominating factor of the transfer.

Table 6. MPUI Transfers to EMIFS: Latency, Throughput

		Latency (1	FC cycles)	Average Throu	ghput (TC cycles	per 16-bit word)
MPUI Source	Src:0xE0000000	First read		I-cache	I-cache enabled	
EMIFS Destination	Dest:0x20002000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15
	20Kx16 no burst	Internal	121.4	35.0	14.0	14.0
	10Kx32 no burst	Internal	147.6	22.5	13.0	13.0
	20Kx16 burst 4	Internal	224.9	13.1	13.1	13.1
	10Kx32 burst 4	Internal	224.9	13.6	13.6	13.6

NOTE: MPUI bursts are not supported. Bursting is used on destination EMIFS only.

MPUI transfers to EMIFS continue the trend of the others. MPUI reads are the limiting factor in this example. Burst reads of the MPUI are not supported. This is reflected in the slightly worse throughput, with bursting set for the destination EMIFS.

3.1.1 Logic Analyzer Images of EMIFS to EMIFS System DMA Transfers

Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 7 are images captured using a logic analyzer with the system DMA configured for EMIFS to EMIFS transfers in various modes.

For the capture image figure from a logic analyzer in Figure 2, and others to follow, the sample ticks are at the same rate as the TC clock (75 MHz). Beginning at cursor 1, four consecutive SDMA non-burst 16-bit reads of external asynchronous SRAM are followed by a 32-bit CPU fetch. At cursor 2, a SDMA write follows the CPU fetch and the captured sequence ends with another SDMA read. As configured in this example, the SDMA EMIFS read cycles are 10 TC clocks and the SDMA EMIFS write cycles are 10 TC clocks. The CPU EMIFS 32-bit fetch cycle shown is 20 TC cycles long. The EMIFS memory space select signal NFCS_3 is inactive for 3 TC clocks after a SDMA read, 1 TC clock after a SDMA write, and 4 TC clocks after a CPU fetch. For more details on the EMIFS cycle behavior, see Table C–1 and Table C–2 in Appendix C.

NSTR	UMENTS	ENS INSTRUMENTS BOTTO	UNCT						SPR.	A883
Matasafe										
<u>></u> [₽.		🗲 🕅 🕈 Time/Div: 🕅	ion 💌 👥	3 <u>0</u>						
C1: 14.973	tes 🗄 🗠 🛙	15.996us 🗐 Dell	a Firm: 1.014us 🗧	3						
NFCS_3	G1: 1	C2 1	Delta: D							
	1							· · · · · · · · · · · · · · · · · · ·		
Sample NFCS_3 NFOE NFWE	04-920-000 vs									
ADDRESS DATA	ES 20 X 2	0000002 227C X EAOG	X 8000004 X X 8994	0000006 X EAF	CODECCE X	X FFFE X	0040000 X 0 X 2375 (1999)	2300 X	040002 X 000000A EADD X2300X EADD	

Texas

Figure 2. System DMA EMIFS Reads and Writes (No Burst, 16-bit)

Similar to the 32-bit CPU fetch seen in Figure 2, for 32-bit reads and writes shown in Figure 3, the throughput is improved by the removal of the inactive TC cycles penalty between the consecutive 16-bit accesses which make up the complete 32-bits. The inactive TC clocks after SDMA EMIFS 32-bit reads and writes are the same for as for 16-bit mode.

Wavelorm 1
팀타 <u>X</u> 학교 화 관 · · · · · · · · · · · · · · · · · · ·
11: 14.9721us 🚖 C2: 16.1992us 🕂 Delta Time: 1.22705us 🔆
JFCS_3 C1: 1 C2: 1 Delta: 0
Į
ample 14.920.c00 us
ATA ESEO X 237C X EAOD X FFFE X EAFF X 2380 X EAOD X FFFE X EAFF X 237C X EAOD WINC FFFE X EAFF # X .
T_[1]

Figure 3. System DMA EMIFS Reads and Writes (No Burst, 32-bit)

At cursor 1, 2 consecutive System DMA EMIFS read bursts of 4 by 16-bit are shown in Figure 4. The EMIFS interface combines these into a single 8 by 16-bit burst read to the external SRAM. Thus, avoiding the wasted cycles between the single 16-bit or 32-reads in the previous examples. The entire set of bursts completes in 10 TC cycles per 16-bit word (80 TC cycles total) with a following inactive /CS for 3 TC cycles, seen previously. A MPU fetch occurs after the burst read. Following the fetch and its trailing inactive /CS for 4 TC cycles, at cursor 2, a System DMA EMIFS burst write begins writing the data from the read.

SPRA883

wavefor	rm 1																- C ×
~티민.	시 또 🖬 🖬 🚠	e 🛉	M 🔶 Tim	c/Dix: 100n	•	뗖다	C.										
01: 14.972	2.0 🛨 (22: 16.3395	W .	Deta Tir	ne: 1.4275us	ž											
NFCS_3	C1: 1		C2 0	1	Dał	a: -1											
							1							2			
Sample NECS 3	C1.909,900 C2	<u>10010</u>	0.000	0.00	uuuu	10101	0,0,00	0.000	11111	1000	10101	0.000	<u></u>	01010	10100	nu nuți	
NFOE								1111	1111		1000				0.000		
NPWE ADDRESS		a V asass	2 2 0000	1000							0006020				Victor		Vacada
DATA	E580 (2392	EACO X	FFFE	ENF	53 03	EAOD	X FFF		EAFF	DBC	6 X	FFFE	2392	X EADO	XX FFFE	EAFF
•														• • • • • •			1
1																	<u> </u>

V Texas

INSTRUMENTS

OMAP)

Figure 4. System DMA EMIFS Read (Burst of 4 by 16-bit)

Two consecutive system DMA EMIFS burst writes of 4 by 16-bit are shown in Figure 5. Similar to the burst read of the same mode, the EMIFS implements this as a single 8 by 16 bit burst. Another set of 2 burst reads begins at the completion of the burst writes.



Figure 5. System DMA EMIFS Write (Burst of 4 by 16-bit)

Figure 6 shows a single System DMA EMIFS burst read of 4 by 32-bit implemented as a single 8 by 16-bit burst read by the EMIFS. Externally, the behavior is the same as for the 2 consecutive 4 by 16-bit bursts. However, internally throughput is improved by the wider bus usage. A MPU fetch and the beginning of a burst write follow the burst read.

🚟 Wayelo	m 1																_	ΠX
<u>></u> [₹.	が住民	<u>क</u> 🕻	9 🔺	h 🔶 Tin	o/Div: 10	6.7n2 👱] 🖽	R Q										
C1: 14.97	21uo 🚊	C 2	16.3390.	o 🚊	D alta 1	ins. 1.4270	i5ui 🚊	3										
NFCS_3	C	3: 1		C2 1	1		0 elta: 0											
		1							 	 		-0						
Sample NFCS_3 NFCE	14.000,70	1111							 			0.1.1	0000			uuui i	7619159	188
NFWE ADDRESS DATA	00040EE) E590	(00000) X	00×0000	002 X 00 EA00	00004)(0 (FFFE		000000)(X 2303	000000A) X EAO		6030)(0806	0006072 X FFFE	Хоон ЭК 2		040002) EADO X	(0040004 X FFFE))(00400 X EAFF		203
	1																	



A single System DMA EMIFS burst write of 4 by 32-bit is shown in Figure 7. This is implemented as a single 8 by 16-bit burst write by the EMIFS. Again, the behavior is similar to the 2 consecutive 4 by 16-bit variety, but takes advantage of the internal 32-bit bus width.

Wavelo	m 1																					-	
~[8.	お際層	an C	r 🔸 M	1 🔶 Tine	s/Div: 1	06.7ns	Υ.	理	<u>Q;</u>														
C1: 16.05	191/2 🚊	5 02	17.1318u	*	Delta	n line: 🚺	0798us	-															
NFCS_3		C1: 1		C2 1			Deita	D															
												2											
Sample	h h h h h h	ពីដោយ	0000			000	0.000	000	hinii	In in	U UU	00 E	mini	nuun	TUUT.	000	0.010	0000	0.000		1000	inin ini	181
NFCS_3		3.62	den here.	10000		130000	10.000	1.000	Sector 2	1000	2010		15637		0.000	-15922	0.000	0.00	05932	3 25-52	3.0303	100010	
NFOE		22/2020	3377	1005	24.02	12172	12223	2/2022	19725	1 2221	12 1/4								102.130				
NPWE					_				1000	ш.			1000	1000	1000	1000	1.57/244	1000	1.10.00	1000	1 1 1 1 1 1	10000	
ADDRESS	X	0040000	X004000	2)(00400	04X00	KODOG)	0040000	K 00400	04×00	400DC)	00400	u Xe	0000010	X00000	L2 X 000	0014X	000016	000001	8×000	0017)(0	00001CX	0000010	
DATA	EIDC 8	2392	CEA00	XXX 7777		AFF X	X 2303	EA00		TTTE X	EAFF		X 26	A2 X 1	(A00)	(FFFE	X EAL	1002	558 X	EA00	2694	X EAC	00
	1																						•
_ ?																							ê

Figure 7. System DMA EMIFS Write (Burst of 4 by 32-bit)

3.2 SDMA Transfers with EMIFF Destination

System DMA transfers with EMIFF SDRAM as the destination and various sources are shown in Table 7, Table 8, Table 9, and Table 10.

		Latency (T	C cycles)	Average Throu	ghput (TC cycles	per 16-bit word)
IMIF Source	Src:0x20002000	First read		I-cache	disabled	I-cache enabled
EMIFF Destination	Dest:0x10002000		First write	DMA Priority 0	DMA Priority 15	DMA priority 15
	20Kx16 no burst	Internal	101.9	4.1	4.1	4.1
	10Kx32 no burst	Internal	101.9	2.0	2.0	2.0
	20Kx16 burst 4	Internal	104.9	2.0	2.0	2.0
	10Kx32 burst 4	Internal	104.9	2.0	2.0	2.0

Table 7. IMIF Transfers to EMIFF: Latency, Throughput

The use of 32-bit and/or bursting for IMIF to EMIFF transfers shows at least 2X improvement over non-burst 16-bit transfers. The initial latency for the first write increases slightly with the word size and the use of bursting.

Table 8. EMIFS Transfers to EMIFF: Latency, Throughput

		Latency (1	C cycles)	Average Throu	ghput (TC cycles	per 16-bit word)
EMIFS Source	Src:0x00000000	First read		I-cache	disabled	I-cache enabled
EMIFF Destination	Dest:0x1000C000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15
	20Kx16 no burst	114.9	131.1	37.0	16.0	16.0
	10Kx32 no burst	114.9	140.9	23.5	13.0	13.0
	20Kx16 burst 4	114.9	200.9	13.4	13.4	13.4
	10Kx32 burst 4	114.9	200.9	13.4	13.4	13.4

SPRA883

The latency improvement trend continues for 32-bit, bursting, and dma priority. The initial write increases more significantly with word size and bursting for an EMIFS source than for an IMIF source.

		Latency (1	C cycles)	Average Throu	ghput (TC cycles	per 16-bit word)
EMIFF Source	Src:0x10002000	First read		I-cache	disabled	I-cache enabled
EMIFF Destination	Dest:0x1000C000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15
	20Kx16 no burst	96.9	125.1	17.1	17.1	17.1
	10Kx32 no burst	96.9	129.6	9.5	9.5	9.6
	20Kx16 burst 4	96.9	116.9	4.3	4.3	4.3
	10Kx32 burst 4	96.9	116.9	4.3	4.3	4.3

Table 9. EMIFF Transfers to EMIFF: Latency, Throughput

A 4X improvement is seen with the use of bursting. The first write is worse for a larger word size, but improves with bursting enabled.

		Latency (1	C cycles)	Average Throu	ghput (TC cycles	per 16-bit word)
MPUI Source	Src:0xE0000000	First read		I-cache	disabled	I-cache enabled
EMIFF Destination	Dest:0x10002000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15
	20Kx16 no burst	Internal	112.4	13.0	13.0	13.0
	10Kx32 no burst	Internal	125.1	13.0	13.0	13.0
	20Kx16 burst 4	Internal	203.1	13.0	13.0	13.0
	10Kx32 burst 4	Internal	203.1	13.6	13.6	13.6

Table 10. MPUI Transfers to EMIFF: Latency, Throughput

NOTE: MPUI bursts are not supported. Bursting is used on destination EMIFF only.

The MPUI reads are the limiting factor in this example. As in the MPUI to EMIFS example, the lack of bursting support on MPUI results in slightly worse throughput for bursting mode set on the EMIFF port.

3.2.1 Logic Analyzer Images of EMIFF to EMIFF System DMA Transfers

Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, and Figure 14 are images captured using a logic analyzer with the system DMA configured for EMIFF to EMIFF transfers in various modes.

The EMIFF is clocked at the same rate as the TC (75 MHz). Beginning at cursor 1, in Figure 8, 4 consecutive SDMA EMIFF 16-bit non-burst reads are shown. These 4 reads occur on the same row of the SDRAM. The row is opened by the active NSRAS and the closing of the row is done with a precharge, NSRAS and NSWE active on the same TC cycle. Each read is initiated by the active NSCAS. Since only a single read is done on each access, this is considered as a non-burst. However, the EMIFF performs this as a SDRAM burst of 1 with a burst terminate or burst stop, NSWE active, on the TC cycle following the active NSCAS. In this example, the CAS latency is 2. This is shown with the data valid at 2 TC clocks after the NSCAS active.

At cursor 2, in Figure 8, a SDMA EMIFF 16-bit non-burst write follows the closing of the row on the previous reads. Similar to the 16-bit non-burst SDMA EMIFF reads, the EMIFF implements the non-burst as a SDRAM single burst with a burst terminate on the cycle immediately following the write. For more details on EMIFF cycle behavior, refer to Table D–1 in Appendix D.



Figure 8. System DMA EMIFF Reads and Write (No Burst, 16-bit)

Figure 9 shows 3 consecutive SDMA EMIFF 32-bit non-burst reads. These reads are implemented by the EMIFF as SDRAM dual burst 16-bit reads. Thus, throughput is improved by the elimination of TC cycles between the 2 consecutive 16-bit reads, which make up the 32-bit read.

🔛 Wavele	tem 1																								
~[6.	8 B	10	하며	9 🔸	M 🔶 Ti	ne/Dix 🛛	3.35ns	٠	m Lin	0,															
C1: 1273	87us	÷	62	13213	• ±] Delta	s Tine 🛛	8ni	3																
NSPIAS		. C	1:0		C2	1		Del	le: 1																
		-	ļ																						
Sample	12.17	0,9	1.62	1225	10000	1000	23233	1201	21,7223	1000	S 1030	10780	1202.0	19030	1281255	7822	1000	1.200		1,233,26	0.00		. 1	11-000,51	0 MS
NSFAS			100	1	10000	10000	1.000	2.50	10.00	0.000	1 - 2 - 2	100.00	125.520	1.525		10000	1.1.1	1 2 2 2 2	1000	5 00.54		2000	1 2 2 2 2 2	290.0	
NSCAS			V-1657	10000	1	1	2.53	1.52.2	1.1 133.01	1	8 3555	1	1	28555	145.533	143,532	1000	12255	1		153206	12012		5.52.22	1522
NSWE			1.1.1.1	222501	0100	05.02	1		C 205	1	S 312/22	0.000	1222132	1	-	22:5275			12.01%	4 9 2 9 9	1	1	1000000	12/22/05	
SADO			0008	0.000	X 1000	0005	X 0001	Χ	100	0003	17 1940 A.M.	K 8002	X 0006	0007	X	00	68	2	X 0014	X 0008	X 8005	X	000	9	1.1
SDATA		-		70	et.		2012/02/02		7330			OGF		6307	X _ ^	902			TO GF	1.1.1.1.1.1.1	EF15		id de	704	<u> </u>
A	phone:																								ार्ग
a a																									6 1
<u> </u>	1 2 2 1 2			Care = 2.0	112110		interes est	0.120		100.00.000		- 171 mar 14			2 1 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2		11 - 2 61	1.1.2.1.1.2.14				a		Cr + 2 + + 10	

Figure 9. System DMA EMIFF Reads (No Burst, 32-bit)

At cursor 2, 2 consecutive SDMA EMIFF 32-bit non-burst writes are shown in Figure 10, followed by a single read. Similar to the 32-bit non-burst reads, the writes of the same mode are implemented by the EMIFF as SDRAM dual burst 16-bit writes. Thus, throughput is improved by the elimination of TC cycles between the 2 consecutive 16-bit reads, which make up each 32-bit write.

Image: Second	Wavefer 🖬	m 1																						
Ct: 12:787-us Ct: 13:2787-us Ct: 13:587-us Ct: 13:596-5 INSRVS D:: Ct: Defa: 1		8 PB B	<u> :::</u> 2	9 🔸	ðð 📥 Til	na/Die 🔢	33511	•	m Ln	ୟ														
NSRVS D1:1 C2:1 Delx:1 3	01: 12.787	ს ქ	- cs	13.2133	ж <u>ж</u>	Delta	Tine 🖪	26.236ns	÷															
Sanole \$3,300,300 us ,	NSFUS	l	n: a		C2:	1		Delta:	1															
NSP/6		13,200,51	2																				13.9	6,510 us-
	NSBAS	·	• • • •										.		·····									
NSWE	NSCAS	2000	1.000	1.000	10000				1					-				1000	1.1.1		1000			277 .038
	NSWE	1	20072-0	1.22(49)		and the	L	1.000	1		1	-	122200	10000	12-0-12	201265	2000	7.75-0	1	1.000	1714710	10000		10
5000 0001 X 0110 X 0010 X 0001 X 1020 X 1002 X 0000 X 0010 X 0000 X 00000 X 00000 X 0000 X 00	54D0	1000	0031		X 0330	0030	X 0003	X 1030	X 1002	X 0030	K 0113	X		10000	8000	1.1.1.1.1		-	(0009)	<u> </u>	0008	X	0.03	0
SDATA 2027 X 7225 X 8307 X 8307 X 8307 X 8307 X 8307 X 8307	SDATA,		70	SF		7346	X T	065	× 6307	XARE	\sim		2.5.25	6	07		1000		COTEC	50	47		63.07	

V Texas

INSTRUMENTS

DWVD)

Figure 10. System DMA EMIFF Writes (No Burst, 32-bit)

In Figure 11, 2 consecutive SDMA EMIFF bursts of 4 by 16-bit are shown. The EMIFF is configured for SDRAM bursts of 8 by 16-bit. This significantly improves the throughput over the previous non-burst examples.

🖀 Wovefo	nm 1																					_ [ЗX
<u>∍</u> [₹.	影响	a 👬 🛛	e 🔸	00 🔷 Tin	e/Div 🛙	3.35no	•	W C	Q,														
C1: 12.79	64un j	- C2	13.0529	uo 🗄	Delta	Time: 25	6.466na																
NSRAS		C1: 1		C2: 1	1		Delta:	0															
							·				6. N.C.					det e die.	- Artica		det en stanne	- ALA AN		0	
Sample	12.206	500 US 1	1	100		200		10.5	1200	1.1						1	1	1000			17-0	53,000	12-
NSBAS				0.000	1002202											1000			1000	100			ΤŤ
NECAS		0.000			1993	207430	1940	14.5	1.44	1 12 12	1.1.1			2.2.2	25.255			122007	10.192	1000	3030	· · · ·	T
NSWE	<u> </u>				591919S								-		0.000					<u>.</u>			Ŧ
SDATA		doos	6307	0000 X	X	706F X	23A. X	6307 ×	4952	EF15 X	DBGE	67B	άŶ.	COSB		0008			6307		0010		=
1	1																						<u>ت</u> ،
+ †																						, i	

Figure 11. System DMA EMIFF Read (Burst of 4 x 16-bit)

Beginning at cursor 2, 2 consecutive SDMA EMIFF 4 by 16-bit write bursts are shown in Figure 12. As in the previous example for the SDRAM reads in the same mode, the EMIFF performs this as a single 8 by 16-bit burst. Again, the throughput is much improved over the non-burst mode.

🔛 Wavefo	ran 1															
⇒ E ₹.	8 40 B 5	1 🗗 🔺 🕅	Time/Div	13.3540	•	ui 🖓	Q,									
C1: 12.78	56ua 🛃	C2 13.0528u	De E	ella Time: 🛛	7.267na											
NSRAS	C1: 1		C2: 1		Delta:	0										
			ļ													
Sample	13.013,0p0 us									100					13.	92,500 us
NSRAS						0.000	200200	1111		100000	200100	2020	 J		20000	
NSCAS						1000	101015	12101		076752	02000	0.5755	100000	1000		
NSWE				<u> 1000000</u>		40.00	0.255.00	1000	10110	259.00	12000	2004430		1400 2005		2012/00/01
SADD	K.	0010		0000	×		C	0010		1.1.1.1.1.1.1.1		0007		0006		
SDATA		6307	1962	706F	7345	63.07	(APG2)	(EF35)	DBGE)	6784	C058		6784			
THE OWNER OF	1															التي.
													 			<u> </u>

Figure 12. System DMA EMIFF Write (Burst of 4 x 16-bit)

A single SDMA EMIFF read burst of 4 by 32-bit is displayed in Figure 13. This is implemented as a SDRAM read burst of 8 by 16-bit. Since the external EMIFF bus is 16 bits, the single 4 by 32-bit burst read is performed in the same number of TC cycles as for the 2 consecutive 4 by 16-bit burst reads.

👑 Wavef	om 1																					
2년 년.	[1] 최태國 해입 · 第·1 me/Dec 13 35ms · 照당 C																					
01: 12.7	n: 12.7658us 🚖 t.2 13.0528us 🚖 Deta Time 267ns 🚖																					
NSRAS		C1:1		C	2: 1		Delta	0														
	-0	<u> </u>																				
Sample	163	.186,000 .	is I	1.2	1	1	1	1.00	1.52	1.0	1.00	1	1000	1	46.52	1		1.1		1.1	3,053,00	0.11
NSR4S				1		1222	152014		15.24	10000	7.22	33524	5.043	1233	101214	1200		N 992				
NSCAS		2010 5.0		_	10000	12/04/2	52/2502.	32-8-53	376454	2010034	20555	1/64294		0.45552	10-12-1	2002	4453	1 9.00	2012/02/	14 555	20. 2.20	244
NSWE		1.11				100000	1.1.1.1.1.1	100	10000	1000	1		1000		1000							
SADD		0008	X 00	20 X		100000	0008	1.1.0.0.0.0	2000	100000	X 0007	х	1000000		0008	1 200000	1 20120	- X -	1 100	0030	C	
SDATA		200221 202	6784	0	X 7061	D(73A)	X 6307	X ASC	C EF15	X OB6E	X 6784		COSE	Þ.	0.00000	1 4051500	2 2 2 2 2 2	6784	24 46252	201 01572	941 (1 90)	
•	-																					2
†																						÷ 1

Figure 13. System DMA EMIFF Read (Burst of 4 x 32-bit)

At cursor 2, a SDMA EMIFF write burst of 4 by 32-bit is shown in Figure 14, followed by the start of a read cycle. The EMIFF implements this as a SDRAM write burst of 8 by 16-bit.

🖀 Wayefo	an 1									
-25+	<u> 몸목 美麗尼 高智 수정</u> + Trac/Diz 1325ng 도 <u>발</u> 异 <u>이</u>									
C1: 12.78	58us 🚊 C2:	13.0528ue 🚊 Del	ta l'ine: 🔤							
NSRAS	C1.1	C2: 1	Delta D							
Sample	23.053,000 us					13,319,500				
NSR/AS										
NSCA5										
NSWE										
SADO	0030	X 0000 X	0020	X 60.07 X	0008					
SDATA	6784	X 706F X 73AC)	6307 A9C2 X EF15 X DB6E X	6784 X C058 X	6784	X GTEE X SA47 X				
•	•									
<u></u>										

Figure 14. System DMA EMIFF Write (Burst of 4 x 32-bit)

3.3 SDMA Transfers with IMIF Destination

System DMA transfers with IMIF internal SRAM as the destination and various sources are shown in Table 11, Table 12, Table 13, and Table 14.

		Latency (1	C cycles)	Average Throughput (TC cycles per 16-bit word)				
IMIF Source	Src:0x20002000	First read		I-cache	disabled	I-cache enabled		
IMIF Destination	Dest:0x20007000		First write	DMA Priority 0	DMA Priority 15	DMA priority 15		
	20Kx16 no burst	Internal	Internal	4.0	4.0	4.0		
	10Kx32 no burst	Internal	Internal	2.0	2.0	2.0		
	20Kx16 burst 4	Internal	Internal	1.7	1.7	1.7		
	10Kx32 burst 4	Internal	Internal	1.7	1.7	1.7		

Table 11. IMIF Transfers to IMIF: Latency, Throughput

Usage of bursting and/or 32-bits for IMIF to IMIF transfers shows at least 2X improvement over non-burst 16-bit mode.

		Latency (T	C cycles)	Average Throughput (TC cycles per 16-bit word)				
EMIFS Source	Src:0x00000000	First read		I-cache disabled		I-cache enabled		
IMIF Destination	Dest:0x20002000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15		
	20Kx16 no burst	114.9	Internal	37.0	16.0	16.0		
	10Kx32 no burst	114.9	Internal	23.5	23.5	13.0		
	20Kx16 burst 4	114.9	Internal	13.4	13.4	13.4		
	10Kx32 burst 4	114.9	Internal	13.4	13.4	13.4		

Table 12. EMIFS Transfers to IMIF: Latency, Throughput

A nearly 3X latency improvement is given by the use of bursting. The initial reads are independent of word size and bursts for an EMIFS source to IMIF destination.

Table 13. EMIFF Transfers to IMIF: Latency, Throughput

		Latency (1	FC cycles)	Average Throughput (TC cycles per 16-bit word)				
EMIFF Source	Src:0x10002000	First read		I-cache	disabled	I-cache enabled		
IMIF Destination	Dest:0x20002000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15		
	20Kx16 no burst	96.9	Internal	6.1	6.1	6.1		
	10Kx32 no burst	96.9	Internal	3.5	3.5	3.5		
	20Kx16 burst 4	96.9	Internal	2.8	2.8	2.8		
	10Kx32 burst 4	96.9	Internal	2.8	2.8	2.8		

A greater than 2X improvement is seen with the use of bursting. Again, the initial read latency is independent of word size and bursting.

Table 14. MPUI Transfers to IMIF: Latency, Throughput

		Latency (1	FC cycles)	Average Throughput (TC cycles per 16-bit word)				
MPUI Source	Src:0xE0000000	First read		I-cache disabled		I-cache enabled		
IMIF Destination	Dest:0x10002000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15		
	20Kx16 no burst	Internal	Internal	13.0	13.0	13.0		
	10Kx32 no burst	Internal	Internal	13.0	13.0	13.0		
	20Kx16 burst 4	Internal	Internal	13.0	13.0	13.0		
	10Kx32 burst 4	Internal	Internal	13.6	13.6	13.6		

NOTE: MPUI bursts are not supported. Bursting is used on destination IMIF only.

The transfers are dominated by the relatively slow MPUI source. Again, bursting with 32 bits is slightly worse than the other modes, when the source is MPUI.

3.4 SDMA Transfers with MPUI Destination

System DMA transfers with a destination of DSP SARAM through the MPUI and various sources are shown in Table 15, Table 16, Table 17, and Table 18.

Table 15. IMIF Transfers to MPUI: Latency, Throughput

		Latency (T	C cycles)	Average Throughput (TC cycles per 16-bit word)				
IMIF Source	Src:0x20002000	First read		I-cache disabled		I-cache enabled		
MPUI Destination			First write	DMA Priority 0	DMA Priority 15	DMA priority 15		
	20Kx16 no burst	Internal	Internal	13.0	13.0	13.0		
	10Kx32 no burst	Internal	Internal	13.0	13.0	13.0		
	20Kx16 burst 4	Internal	Internal	13.0	13.0	13.0		
	10Kx32 burst 4	Internal	Internal	13.0	13.0	13.0		

NOTE: MPUI bursts are not supported. Bursting is used on the source IMIF only.

IMIF to MPUI transfers are dominated by the MPUI writes.

Table 16. EMIFS Transfers to MPUI: Latency, Throughput

		Latency (1	FC cycles)	Average Throughput (TC cycles per 16-bit word)				
EMIFS Source	Src:0x00000000	First read		I-cache	I-cache disabled			
MPUI Destination	Dest:0xE0014000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15		
	20Kx16 no burst	114.9	Internal	37.0	16.0	16.0		
	10Kx32 no burst	114.9	Internal	23.5	13.0	13.0		
	20Kx16 burst 4	114.9	Internal	13.4	13.4	13.4		
	10Kx32 burst 4	114.9	Internal	13.5	13.5	13.5		

NOTE: MPUI bursts are not supported. Bursting is used on the source EMIFS only.

The initial reads are independent of word size and bursts for an EMIFS source to MPUI destination. A nearly 3X latency improvement is given by the use of bursting. Average EMIFS throughput for bursting in 32-bit mode is slightly worse than for 16-bit burst mode.

Table 17. EMIFF Transfers to MPUI: Latency, Throughput

		Latency (1	FC cycles)	Average Throughput (TC cycles per 16-bit word)				
EMIFF Source	Src:0x10002000	First read		I-cache	I-cache enabled			
MPUI Destination	Dest:0xE0014000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15		
	20Kx16 no burst	96.9	Internal	13.0	13.0	13.0		
	10Kx32 no burst	96.9	Internal	13.0	13.0	13.0		
	20Kx16 burst 4	96.9	Internal	13.0	13.0	13.0		
	10Kx32 burst 4	96.9	Internal	13.0	13.0	13.0		

NOTE: MPUI bursts are not supported. Bursting is used on the source EMIFF only.



The MPUI writes dominate the transfer throughput. The initial EMIFF read latency is independent of word size and bursting.

		Latency (1	C cycles)	Average Throughput (TC cycles per 16-bit word)				
MPUI Source	Src:0xE0000000	First read		I-cache disabled		I-cache enabled		
MPUI Destination	Dest:0xE0015000		First write	DMA Priority 0	DMA Priority 15	DMA Priority 15		
	20Kx16 no burst	Internal	Internal	26.0	26.0	26.0		
	10Kx32 no burst	Internal	Internal	26.0	26.0	26.0		
	Bursting	N/A	N/A	N/A	N/A	N/A		

Table 18. MPUI Transfers to MPUI: Latency, Throughput

NOTE: MPUI bursts are not supported.

System DMA transfers through MPUI have the same average throughput in either direction. The transfer latency is double that seen for transfers with MPUI as the limiting factor.

4 Conclusions

In general, for the greatest system DMA throughput, bursting should be used whenever possible. Use of I-cache is beneficial for tight code loops running within the same memory as other activity. Increasing the priority levels for a requestor of a particular TC memory can provide better throughput at the expense of other ports accessing the same memory. Furthermore, the choice of a particular memory type will have a major impact to throughput. In order from fastest memory to slowest memory, these are: IMIF, EMIFF, EMIFS, and MPUI (DSP memory).

5 References

- 1. OMAP5910 Dual-Core Processor Data Manual (SPRS197)
- 2. OMAP5910 Dual-Core Processor Technical Reference Manual (SPRU602)
- 3. Samsung Electronics <u>http://www.samsungelectronics.com</u>







Figure A–1. OMAP Block Diagram

Appendix B MPU Memory Map

Table B-1.	MPU	Memory	Мар
------------	-----	--------	-----

Address Range	On-Chip	External Interface
0x0000 0000 0x01FF FFFF		FLASH CS0 32 Mbytes
0x0200 0000 0x03FF FFFF	reserved	
0x0400 0000 0x05FF FFFF		FLASH CS1 32 Mbytes
0x0600 0000 0x07FF FFFF	reserved	
0x0800 0000 0x09FF FFFF		FLASH CS2 32 Mbytes
0x0A00 0000 0x0BFF FFFF	reserved	
0x0C00 0000 0x0DFF FFFF		FLASH CS3 32 Mbytes
0x0E00 0000 0x0FFF FFFF	reserved	
0x1000 0000 0x13FF FFFF		SDRAM 64Mbytes
0x1400 0000 0x1FFF FFFF	reserved	
0x2000 0000 0x2002 FFFF	Internal SRAM 192Kbytes	
0x2003 0000 0x2FFF FFFF	reserved	
0x3000 0000 0x7FFF FFFF		Local bus space for USB host
0x8000 0000 0xDFFF FFFF	reserved	
0xE000 0000 0xE0FF FFFF	DSP public memory space (accessible by MPUI) 16Mbytes	
0xE100 0000 0xEFFF FFFF	DSP public peripherals (accessible by MPUI)	
0xFFFB 0000 0xFFFC FFFF	MPU public, MPU/DSP shared peripherals	
0xFFFD 0000 0xFFFE FFFF	MPU private peripherals	
0xFFFF 0000 0xFFFF FFFF	reserved	

Appendix C EMIFS Behavior

Table C-1. EMIFS Cycle Behavior with ARM I/D-Caches Disabled, EMIFS_PRIO = 0x00000000, and EMIFS_CS3_CONFIG.FCLKDIV=TC/2

	EMIFS Cycle Behavior	
Consecutiv	Minimum TC Cycles	
1st	2nd	Between CS Active
System DMA Read (16-bit, 32-bit, or burst)	System DMA Write (16-bit, 32-bit, or burst)	3
System DMA Read (16-bit, 32-bit, or burst)	ARM Program Fetch or Data Read (32-bit)	3
System DMA Write (16-bit, 32-bit or burst)	System DMA Read (16-bit, 32-bit, or burst)	1
System DMA Write (32-bit or burst)	ARM Program Fetch or Data Read (32-bit)	1
System DMA Read (32-bit or burst)	Consecutive 16-bit words within first operation	0
System DMA Write (32-bit or burst)	Consecutive 16-bit words within first operation	0
ARM Program Fetch or Data Read (32-bit)	System DMA Read (16-bit, 32-bit, or burst)	4
ARM Program Fetch or Data Read (32-bit)	System DMA Write (16-bit, 32-bit, or burst)	4

Table C-2. EMIFS /CS Active Widths for Asynchronous Reads/Writes

FCLKDIV	CS Active Width Read (TC Cycles)	CS Active Width Write (TC Cycles)
divide by 1	1*(RDWST+1)+1	1*(WRWST+WELEN+1)+2
divide by 2	2*(RDWST+1)+2	2*(WRWST+WELEN+1)+4
divide by 4	4*(RDWST+1)+4	4*(WRWST+WELEN+1)+8
divide by 6	6*(RDWST+1)+6	6*(WRWST+WELEN+1)+12

For this application report, the following apply:

- FCLKDIV = /2, RDWST = 3, WRWST = 1, WELEN = 1
- CS Active Width Read = 2*(RDWST+1)+2 = 2*(3+1)+2 = 10 TC cycles
- $\overline{\text{CS}}$ Active Width Write = 2*(WRWST+WELEN+1)+4 = 2*(1+1+1)+4 = 10 TC cycles

Appendix D EMIFF Behavior

Table D–1. EMIFF Behavior for Single and Burst Reads/Writes (TC Cycles)

	t _{RCD}	t _{RAS} -t _{RCD}	Burst	t _{RP}	t _{RRD}	_		
System DMA Data Type	RAS to CAS	CAS to Burst Terminate	Terminate to Precharge	Precharge to Next RAS	Total TC Cycles	TC Cycles per 16-bit Word	Precharge to Auto-Refresh	Auto-Refresh to RAS
16-bit read	2	1	5	2	10	10	4	5
32-bit read	2	2	5	2	11	5.5	4	5
16-bit read burst of 4	2	8 (EMIFF bursts 8x16)	8	2	20	2.5 (for transfers in multiples of 8x16)	4	5
32-bit read burst of 4	2	8 (EMIFF bursts 8x16)	8	2	20	2.5	4	5
16-bit write	2	1	5	2	10	10	4	5
32-bit write	2	2	5	2	11	5.5	4	5
16-bit write burst of 4	2	8 (EMIFF bursts 8x16)	2	2	14	1.75 <i>(</i> for transfers in multiples of 8x16)	4	5
32-bit write burst of 4	2	8 (EMIFF bursts 8x16)	2	2	14	1.75	4	5

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments Post Office Box 655303 Dallas, Texas 75265

Copyright © 2002, Texas Instruments Incorporated