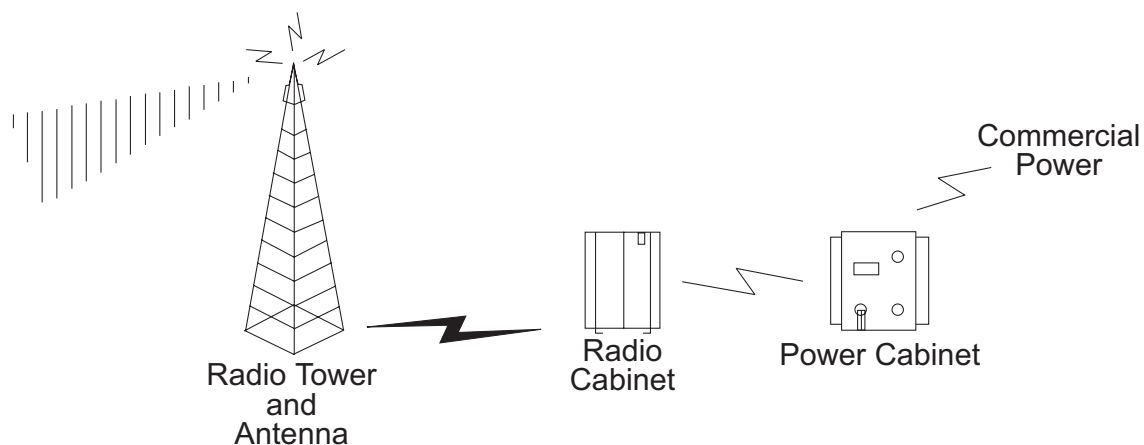


## Introduction

The purpose of this paper is to describe the beneficial effects on the economics of 3G channel card design brought about by the introduction of TI's high-density TMS320TC11x UMTS Infrastructure Chipset. It will consider the current needs of the changing wireless landscape. It will break down the costs facing 3G basestation OEMs. And it will enumerate the various architectures from which manufacturers can choose to design their solutions.

The paper also will go into detail describing the design and function of the new chipset, which includes the TMS320TC100 digital signal processor (DSP), the TMS320TC110 application-specific standard processor (ASSP) and the TMS320TC120 ASSP. By coupling an industry-leading, wireless-infrastructure tailored, programmable DSP with customizable ASSPs, TI has eliminated the need for OEMs to develop custom ASICs. This leads to substantial cost reductions. Meanwhile, flexible resource pooling and efficient interfaces tremendously improve channel density over today's solutions. And manufacturers can still easily customize their products through the flexible hardware and modular software of TI's chipset.

When examined vis-à-vis the demands of the ever-changing 3G landscape and the exorbitant costs OEMs face today, it becomes clear that these new chips have revolutionized 3G channel card design.



**Figure 1: Typical Basestation Deployment**

## **The Wireless Landscape and a Breakdown of Design Costs**

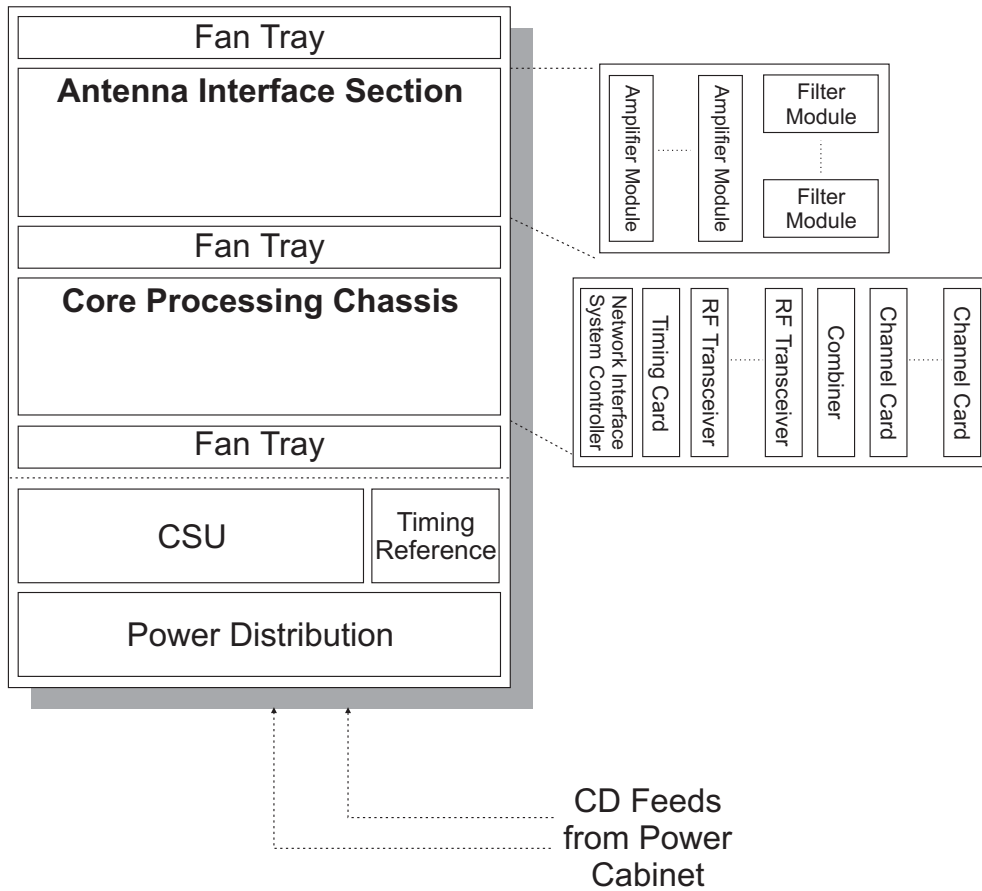
The wireless landscape is changing. While the number of subscribers is increasing and the average number of voice minutes used is up, the average revenue per subscriber is down. Carriers are faced with the challenge of finding new revenue-generating services. The voice market is ultra-competitive so carriers are looking for new data-oriented services such as web surfing, gaming, and video and picture exchange to help them achieve their goals.

At the same time carriers want to reduce capital and operating expenditures. But building out and maintaining a widespread network that includes data as well as voice is not cheap. So these carriers need new and better equipment and they need more of it in order to minimize dead spots.

This puts added pressure on manufacturers to quickly create and deliver highly flexible, differentiated solutions. But manufacturers have pressures of their own. This differentiation must happen without incurring an excessive amount of R&D expenditures. Manufacturers would rather use that time and money on other areas that help them win in this changing marketplace. As a result, they are turning around and demanding a lot of their silicon solution providers to help cut costs.

Rising base station design costs are due to three drivers: the RF transceiver, the power amp and the channel card. Of these, OEMs spend the most time and money attempting to optimize channel card design. Within the channel card itself, the modem dominates cost, accounting for approximately 70 percent of the cost.

So it becomes apparent that in the changing 3G landscape, the silicon provider who can address both cost and flexibility (i.e., differentiation) concerns will be the winner.



**Figure 2: UMTS Node-B Block Diagram with Breakout View of Core Processing Chassis**

### Architecture Options for Wireless OEMs

OEMs have been presented with several options to meet their needs. None of these options have quite fit the bill. Each approach has benefits, but also has drawbacks that ultimately leave manufacturers wanting more.

For example, a DSP plus FPGA approach to channel card design delivers a good level of flexibility but also a fairly steep bill of materials. Conversely, an all ASIC approach has a low bill of materials (BOM) cost but poor flexibility.

When reconfigurable processors have been tried, OEMs have seen additional problems. Not only is the bill of materials high, but there is a significant software development cost. This is due in most part to immature tools.

An all DSP solution has also been discussed. However, OEMs seem to be rejecting this approach despite its inherent flexibility. At this time, there is not a single base station that uses an all-DSP solution. For the most part, OEMs have turned to a DSP plus custom ASIC approach. Until now, this has delivered the best combination of low-cost design and high flexibility.

But the new programmable UMTS Infrastructure Chipset offers a single platform that maintains the same flexibility as the popular DSP-plus-custom-ASIC solution but at a substantially lower cost. The cost savings come in two forms: First, OEMs don't incur the development expense of creating their own custom ASIC – typically millions of dollars; and, second, they get a substantial savings on BOM cost because the TI solution actually increases channel density by a factor of two to 64 channels.

Of equal importance to cellular infrastructure OEMs is the fact that the cost savings are delivered without sacrificing the ability to customize and differentiate their solution. In TI's chipset, the receive and transmit chip-rate ASSPs consist of flexible hardware configured via registers and commands under DSP software control, making differentiation not only possible, but simple.

### **The High-Density TMS320TC11x UMTS Chipset from TI**

It is instructive to take an in-depth look at the new chipset. The TC1110 ASSP supports the intensive uplink chip-rate processing function and works in concert with a TC1100 DSP performing uplink chip-rate assist and symbol-rate functions. The TC1120 ASSP supports the downlink chip-rate functions with a TC1100 DSP performing the downlink symbol rate functions. These are the critical functions of the uplink and downlink base-band processors that OEMs need to create next-generation solutions for 3G wireless.

Putting functionality in the DSP also allows OEMs to differentiate their solutions with their own intellectual property. Functionality requiring very high MIPS was migrated into the ASSPs where there is more return on investment in terms of MIPS to silicon die area. This hardware/software partitioning optimizes both flexibility and channel density. These are the keys towards a low-cost solution during both development and operation.

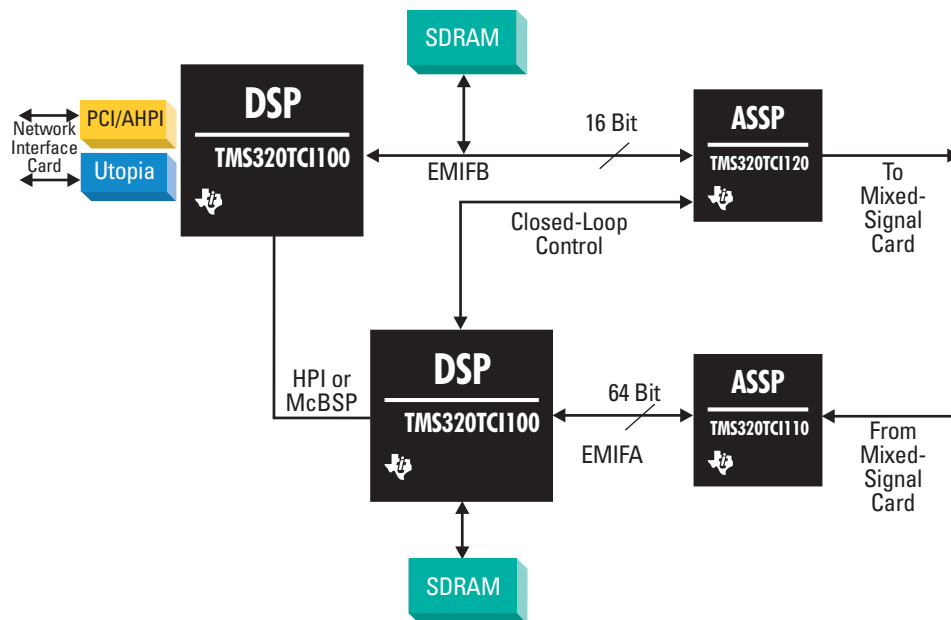


Figure 3: The UMTS Infrastructure Chipset from TI in a System Configuration

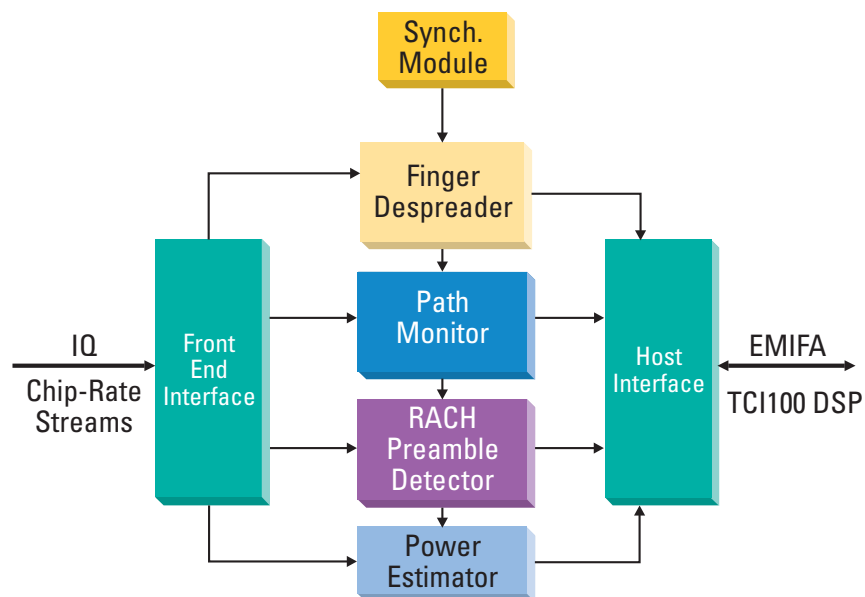
### Wireless-Infrastructure-Tailored TCI100 DSP

The high-performance TCI100 DSP is optimized for wireless infrastructure applications and operates at a clock speed of 720 MHz. It has two multipliers that support four 16 × 16-bit multiplies per cycle. The enhanced direct memory access (DMA) controller has 64 independent channels and can be operated in slave mode. The embedded Viterbi coprocessor can support 350 voice (12.2-kbps AMR) channels and the Turbo coprocessor can support 28 high-data-rate (384-kbps) users. The TCI100 DSP supports a 64-bit external memory interface (EMIF) bus (EMIFA), a 16-bit EMIF bus (EMIFB) and other common interfaces such as Utopia and multi-channel buffered serial port (McBSP).

### The High-Performance TCI110 ASSP

A closer look at the high-performance coprocessor, the TCI110 ASSP, reveals several correlation modules and two interface blocks. These correlation modules are built around a high-performance correlation engine and are programmable and therefore are very flexible. Examples of some of the programmable features are the coherent and non-coherent accumulation length, pilot mask and activity factor. These correlation modules each have a pool of resources on a single chip from which OEMs can pull as needed. For example, manufacturers can draw more resources for each high-bandwidth data call and less for each voice call leading to a highly efficient use of silicon. The correlation modules included in the TCI110 ASSP are:

- The **finger de-spreader** module de-spreads symbols on the dedicated and common channels. In addition, it performs early, on-time and late (EOL) correlations on the control channels.
- The **path monitor** module performs correlations over a configurable search window on the control channel.
- The **preamble detector** module performs correlations over a configurable search window on a common channel preamble such as the random access channel (RACH).



**Figure 4: The TCI110 ASSP**

The TCI110 ASSP also features a front-end interface and a host interface. The front-end interface supports many different antenna configurations. The 48-bit front-end bus operates at a clock rate of up to 92.16 MHz and supports up to 24 streams from up to 12 sources (antennae). Three over-sampling rates are supported: two, four or eight samples per chip. The front-end interface also distributes samples to the correlation processors at a sample rate that matches the specific requirements of each.

The host interface is highly optimized to make the most efficient use of the total bandwidth. It transfers correlation results to the TCI100 DSP over a 64-bit bus using an Enhanced Direct Memory Access Controller (EDMA). This allows data to be transferred without CPU interaction thus reducing the overall transfer overhead by about an order of magnitude.

## The HSDPA-Ready TCI120 ASSP

TI's UMTS chipset also includes a second coprocessor, the TCI120 ASSP. This component of TI's offering supports highly flexible chip-rate processing of 3GPP Node B downlink physical layer. This ASSP works with the TCI100 DSP in implementing the complete downlink physical layer functionality. This includes the newest high-speed downlink standard feature known as high-speed downlink packet access or HSDPA. This new feature allows OEMs to increase downlink capacity enabling faster Internet downloads and improved video conferencing.

The flexibility supported by the TCI120 ASSP allows the selection of a combination of variable-rate voice and data users on up to 288 channels. It also allows a choice of one to three sectors, and a selection of open- or closed-loop transmit diversity. Real-time closed-loop control is ensured via six dedicated serial links to the TCI100 DSP.

The architecture of the TCI120 ASSP is centered around nine channel blocks, which can be configured to support up to 32 dedicated or common channels (see Figure 5). Each channel block supports both QPSK and 16-QAM modulation for HSDPA.

The TCI100 DSP performs downlink symbol-rate functions and sends control, configuration and user data to the TCI120 ASSP for each downlink slot over a high-bandwidth parallel interface. Separate closed-loop interfaces for power control, transmit diversity, and acquisition indicator channel are supported by six multi-channel buffered serial ports connecting the DSP to the TCI120 ASSP.

Separate outputs for the primary and diversity antennas in each sector are formed by summing the data from the channel blocks assigned to that sector. The output of the TCI120 ASSP interfaces seamlessly to TI's GC5016 digital up/downconverter. The GC5016 device supports pulse-shaping, interpolation, and digital up-conversion for three sectors.

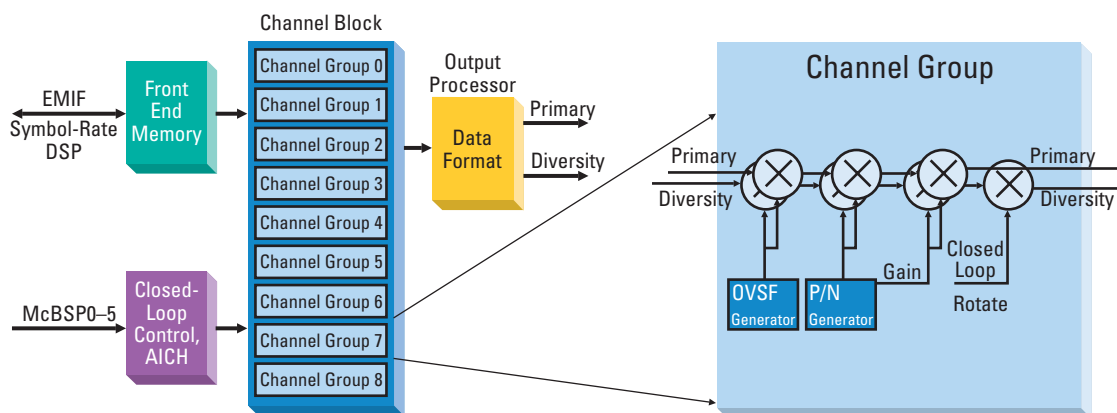


Figure 5: The TCI120 ASSP

**Software**

Both the TCI110 and TCI120 ASSPs are supported with device-control software and plug-ins for Code Composer Studio™ from TI. These provide APIs for communication of control and data to each ASSP, as well as visibility into the device in real-time for ease of debugging. In addition, there is a resource manager available for the TCI110 ASSP, which abstracts the implementation details and monitors the resources for that device.

**Conclusion**

Clearly, TI's high-density UMTS Infrastructure Chipset is an innovative solution to the challenges facing manufacturers in the ever-changing 3G market. By offering a single platform that maintains the same flexibility as the popular DSP-plus-custom-ASIC solution but at a substantially lower cost, TI is giving 3G wireless OEMs what they have been asking for.

Manufacturers will enjoy cost savings coming in two forms: First, by not incurring the development expense of creating their own custom ASIC – typically millions of dollars; and, second, by BOM savings. Meanwhile, flexible resource pooling and efficient interfaces tremendously improve channel density over today's solutions. And manufacturers can still easily customize their products through the flexible hardware and modular software of TI's chipset.

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