

Manual Update Sheet

DATE: July 9, 2002

Document Being Updated: *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals*

Literature Number Being Updated: SPRU357B

This Manual Update Sheet (literature number SPRZ015C) ships with the *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357B).

Page: **Change or Add:**

2–5 **Section 2.2.1, System Control and Status Registers 1 and 2 (SCSR1, SCSR2)**

Replace the current description of Bit 0 of SCSR1 *with* the following:

Bit 0 **ILLADR.** Illegal Address detect bit

If an illegal address has occurred this bit will be set. It is up to software to clear this bit following an illegal address detect. This bit is cleared by writing a 1 to it and should be cleared as part of the initialization sequence. Note: An illegal address access will cause an NMI.

Page: **Change or Add:**

2–6 **Section 2.2.1, System Control and Status Registers 1 and 2 (SCSR1, SCSR2)**

Replace the current description of Bit 5 of SCSR2 *with* the following:

Bit 5 **Watchdog Override.** (WD protect bit)

After RESET, this bit gives the user the ability to protect the WD function from being disabled through software (by setting the WDDIS bit = 1 in the WDCR). This bit is a clear-only bit and defaults to a 1 after reset, *Note: this bit is cleared by writing a 1 to it.*

- 0 Protects the WD from being disabled by software. This bit cannot be set to 1 by software. It is a clear-only bit, cleared by writing a 1. Clearing this bit would enable the WD if it is currently disabled.
- 1 This is the default reset value and allows the user to disable the WD through the WDDIS bit in the WDCR. Once cleared however, this bit can no longer be set to 1 by software, thereby protecting the integrity of the WD timer

Section 2.5.3, Nonmaskable Interrupt (NMI)

Append the following to Section 2.5.3:

The following caution should be observed while using the SARAM on 240xA devices that lack an external memory interface (XMIF): The last 2 words in SARAM cannot be used to store a RET or Branch instruction. This is because, when a RET or Branch instruction reaches the execute phase of the pipeline, the next two instruction words have already been fetched. Since addresses 8800h and above is illegal in 240xA devices that lack XMIF, this asserts an NMI. As an example, the following code snippet will work fine:

```
87FB    xxxxx
87FC    xxxxx
87FD    RET
87FE    xxxxx
87FF    xxxxx
```

However, if the RET instruction is pushed down to 87FE or 87FF, an NMI will be asserted.

The following code snippet illustrates the behavior of unconditional branch:

```
87FB    NOP
87FC    B    "address"
87FE    xxxxx
87FF    xxxxx
```

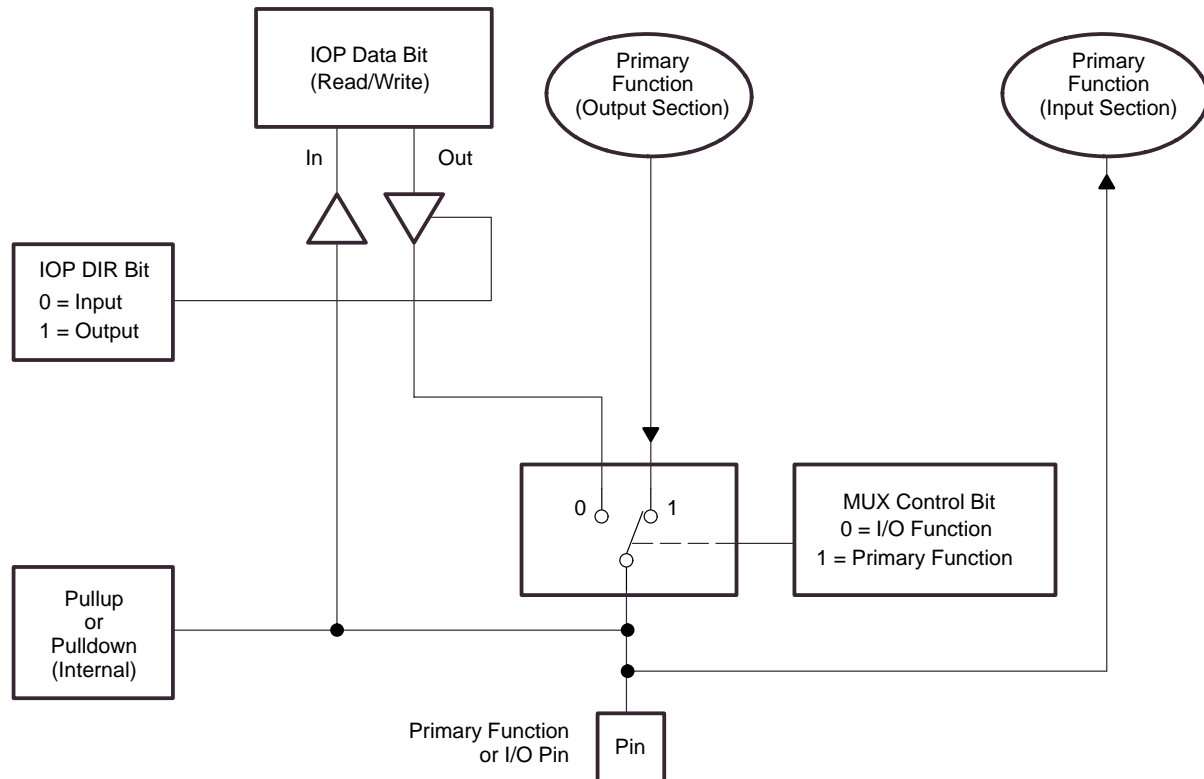
This will work fine. However, if the B occupies 87FD or above , then NMI will be asserted. TBLR and TBLW instructions can operate on data at locations 87FE or 87FF without any issue.

Page: Change or Add:

5-2

Figure 5-1, Shared Pin Configuration

Replace the current drawing with the following:



Page: Change or Add:

5-7

Table 5-4, I/O Mux Control Register C (MCRC) Configuration

Replace the secondary pin function of Bit 14, **IOPF6**, with **Reserved**

Page: Change or Add:

5-7

Table 5-4, I/O Mux Control Register C (MCRC) Configuration

Add the following to the table:

Note: IOPF6 is not multiplexed with any other function. Independent of the value of MCRC.14, this pin always works as a GPIO pin.

Page: Change or Add:

6-38

Section 6.4, Compare Units, first paragraph

Replace the sentence "The time base for the compare units is provided by GP timer 1 (for EVA) and by GP timer 2 (for EVB)." with "The time base for the compare units is provided by GP timer 1 (for EVA) and by GP timer 3 (for EVB)."

Page: Change or Add:

6-38

Figure 6-12, Compare Unit Block Diagram

Replace "(For EVA: x = 1, 2, 3; y = 1, 3, 5; z = 1. For EVB: x = 4, 5, 6; y = 7, 9, 11; z = 2.)" with "(For EVA: x = 1, 2, 3; y = 1, 3, 5; z = 1. For EVB: x = 4, 5, 6; y = 7, 9, 11; z = 3.)"

Page: Change or Add:

6–39 **Section 6.4, Compare Units, top paragraph**

Replace the sentence “The time base for the compare units and the associated PWM circuits is provided by GP timer 1 (for EVA) or GP timer 2 (for EVB), which can be in any of its counting modes when the compare operation is enabled.” *with* “The time base for the compare units and the associated PWM circuits is provided by GP timer 1 (for EVA) or GP timer 3 (for EVB), which can be in any of its counting modes when the compare operation is enabled.”

Page: Change or Add:

6–42 **Description of Bit 8 of Compare Control Register A (COMCONA)**

Replace the current description with the following:

Bit 8 **$\overline{\text{PDPINTA}}$ STATUS.** This bit reflects the current status of the $\overline{\text{PDPINTA}}$ pin. Application could poll this bit to determine whether the fault that activated this pin has disappeared. (This bit is applicable to 240xA devices only — it is reserved on 240x devices and returns a zero when read.)

Page: Change or Add:

6–43 **Description of Bit 8 of Compare Control Register B (COMCONB)**

Replace the current description with the following:

Bit 8 **$\overline{\text{PDPINTB}}$ STATUS.** This bit reflects the current status of the $\overline{\text{PDPINTB}}$ pin. Application could poll this bit to determine whether the fault that activated this pin has disappeared. (This bit is applicable to 240xA devices only — it is reserved on 240x devices and returns a zero when read.)

Page: Change or Add:

6–60 **Section 6.6.5, Double Update PWM Mode**

Add Section 6.6.5, Double Update PWM Mode:

The '240xA Event Manager supports “Double Update PWM Mode.” This mode refers to a PWM operation mode in which the position of the leading edge and the position of the trailing edge of a PWM pulse are independently modifiable in each PWM period. To support this mode, the compare register that determines the position of the edges of a PWM pulse must allow (buffered) compare value update once at the beginning of a PWM period and another time in the middle of a PWM period.

The compare registers in 240xA Event Managers are all buffered and support three compare value reload/update (value in buffer becoming active) modes. These modes have earlier been documented as compare value reload conditions. The reload condition that supports double update PWM mode is reloaded on Underflow (beginning of PWM period) OR Period (middle of PWM period). Double update PWM mode can be achieved by using this condition for compare value reload.

Page: Change or Add:

6–69 **Figure 6–28, Capture Units Block Diagram (EVB)**

Replace “T2CNT GP timer 4 counter” *with* “T4CNT GP timer 4 counter”
Replace “T1CNT GP timer 3 counter” *with* “T3CNT GP timer 3 counter”

Page: **Change or Add:**
6–70 **Section 6.8.1, Capture Unit Features**, second bullet from top
Insert the sentence “In the case of 240xA devices, the input must be held for a duration mandated by the input qualifier circuitry.” *before* the last sentence “Input pins CAP1 and CAP2 (CAP4 and CAP5 in case of EVB) can also be used as QEP inputs to QEP circuit.”

Page: **Change or Add:**
6–70 **Section 6.8.2, Operation of Capture Units**
Append the following sentence to the first paragraph: “In the case of 240xA devices, additional latency due to the input qualifier circuitry must be taken into account.”

Page: **Change or Add:**
6–71 **Section 6.8.3, Capture Unit Registers**
Delete the following sentence from the paragraph: “Additionally, CAPCONA/B is also used to control the operation of the QEP circuit.”

Page: **Change or Add:**
6–71 **Figure 6–29, Capture Control Register A (CAPCONA) — Address 7420h**
Bit 15, CAPRES: *replace* “RW–0” with “W–0”

Page: **Change or Add:**
6–71 **Description of Bit 15 of Capture Control Register A (CAPCONA)**
Replace the description of Bit 15 with the following:

Bit 15 **CAPRES.** Capture reset. Always reads zero.

Writing a 0 clears the capture registers.
0 Clears all registers of capture units to 0
1 No action

Page: **Change or Add:**
6–73 **Figure 6–30, Capture Control Register B (CAPCONB) — Address 7520h**
Bit 15, CAPRES: *replace* “RW–0” with “W–0”

Page: **Change or Add:**
6–73 **Description of Bit 15 of Capture Control Register B (CAPCONB)**
Replace the description of Bit 15 with the following:

Bit 15 **CAPRES.** Capture reset. Always reads zero.

Writing a 0 clears the capture registers.
0 Clears all registers of capture units to 0
1 No action

Page: **Change or Add:**

6-73

Description of Bits 14-13 of Capture Control Register B (CAPCONB)

Replace the description of Bits 14-13 with the following:

Bits 14-13 CAPQEPN. Capture Units 4 and 5 control.

- 00 Disables Capture Units 4 and 5. FIFO stacks retain their contents.
- 01 Enables Capture Units 4 and 5
- 10 Reserved
- 11 Reserved

Page: **Change or Add:**

6-79

Section 6.9.1, QEP Pins

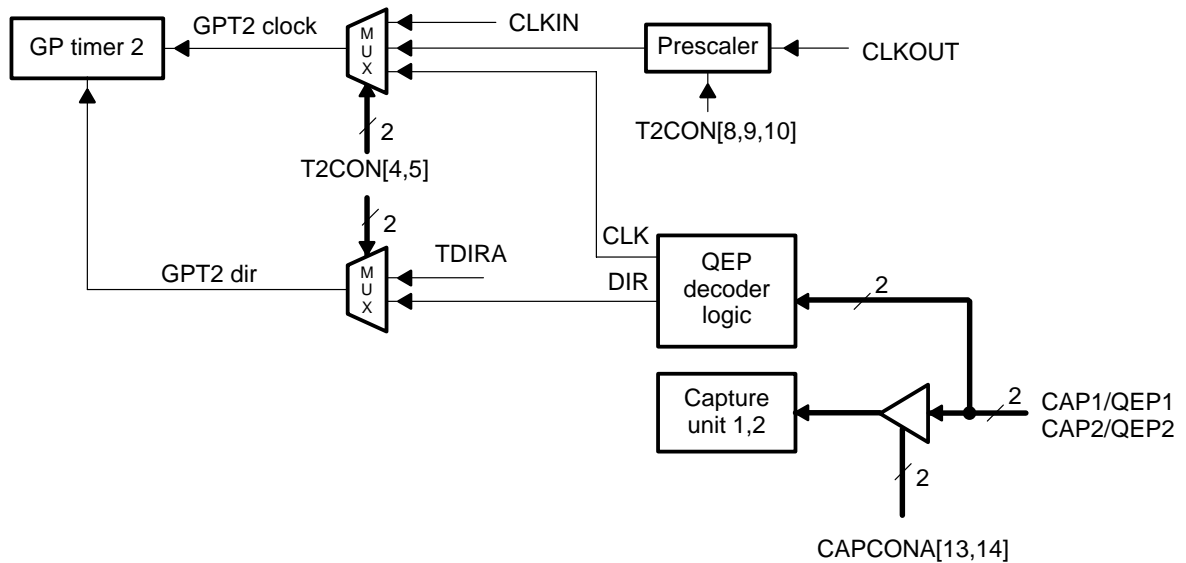
Delete the following sentence from the paragraph: "Proper configuration of CAPCONx bits is required to enable the QEP circuit and disable capture units, thus assigning the associated input pins for use by the QEP circuit."

Page: **Change or Add:**

6-79

Figure 6-33, Quadrature Encoder Pulse (QEP) Circuit Block Diagram for EVA

Replace the existing figure with the following:

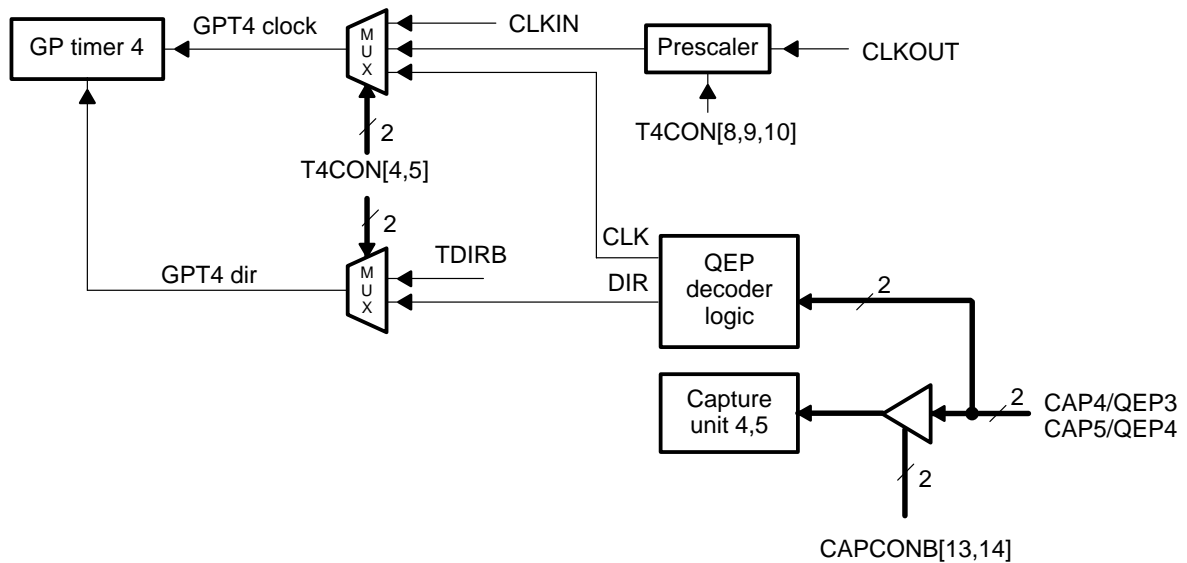


Page: Change or Add:

6-80

Figure 6-34, Quadrature Encoder Pulse (QEP) Circuit Block Diagram for EVB

Replace the existing figure with the following:



Page: Change or Add:

6-81

Section 6.9.5, Register Setup for the QEP Circuit

Delete the following:

3) Configure CAPCONA to enable the QEP circuit

Page: Change or Add:

6-82

Section 6.9.5, Register Setup for the QEP Circuit

Delete the following:

3) Configure CAPCONB to enable the QEP circuit

Page: Change or Add:

7-2

Section 7.1, Features

Replace the second bulleted item:

Fast conversion time (S/H + Conversion) of 375 ns (425 ns in LC2402A)

with

Fast conversion time (S/H + Conversion): 375 ns for LC2406A/LC2404A, 425 ns for LC2402A, and 500 ns for LF240xA

Page: Change or Add:

7-5

Figure 7-1, Block Diagram of Autosequenced ADC in Cascaded Mode

Replace "10-bit, 375-ns[†] S/H + A/D converter" with "10-bit S/H + A/D converter[†]"

Replace the footnote "[†]425-ns for LC2402A" with "[†]375-ns for LC2406A/LC2404A, 425-ns for LC2402A, and 500-ns for LF240xA"

- Page:** **Change or Add:**
- 7–6 **Figure 7–2, Block Diagram of Autosequenced ADC With Dual Sequencers**
Replace “10-bit, 375-ns† S/H + A/D converter” with “10-bit S/H + A/D converter†”
Replace the footnote “†425-ns for LC2402A” with “†375-ns for LC2406A/LC2404A, 425-ns for LC2402A, and 500-ns for LF240xA”
- Page:** **Change or Add:**
- 7–33 **Section 7.5.4, Autosequence Status Register (AUTO_SEQ_SR)**
Add the following Note:
Note: The AUTO_SEQ_SR register and the RESULTn registers of the 240xA ADC module are “Read-only”. Any attempt to write to these registers will cause an NMI.
- Page:** **Change or Add:**
- 7–37 **Section 7.5.6, ADC Conversion Result Buffer Registers (RESULTn)**
Add the following Note:
Note: The AUTO_SEQ_SR register and the RESULTn registers of the 240xA ADC module are “Read-only”. Any attempt to write to these registers will cause an NMI.
- Page:** **Change or Add:**
- 8–23 **Bit 6 RX ERR INT ENA**
*Replace “SCI receive **enable** interrupt enable” with “SCI receive **error** interrupt enable”*
- Page:** **Change or Add:**
- 8–28 **Section 8.7.5, Receiver Status Register (SCIRXST)**
Delete from the first paragraph: “Each time the buffers are read, the flags are cleared.”
- Page:** **Change or Add:**
- 10–17 **Figure 10–9, Local Acceptance Mask Register n (0, 1) High Word (LAMn_H) – Addresses 710Bh, 710Dh**
Append the following to the description of Bit 15, LAMI:
- When LAMI = 1:
1. The IDE bit of the receive mailbox is a “don’t care”. The IDE bit of the receive mailbox is overwritten by the IDE bit of the transmitted message.
 2. The filtering criterion must be satisfied in order to receive a message.
 3. The number of bits to be compared is a function of the value of the IDE bit of the transmitted message.
- When LAMI = 0:
1. The IDE bit of the receive mailbox determines the number of bits to be compared.
- NOTE:** The definition for the IDE bit changes depending on the value of the LAMI bit:
When LAMI = 1:
IDE = 1: The RECEIVED message had an extended identifier
IDE = 0: The RECEIVED message had a standard identifier
When LAMI = 0:
IDE = 1: The TO BE RECEIVED message must have an extended identifier
IDE = 0: The TO BE RECEIVED message must have a standard identifier

Page: Change or Add:

10–26

Description of Bit 10 of BCR1

Replace the current description of Bit 10 with the following:

Bit 10	SBG. Synchronization edge.
0	The CAN module resynchronizes on the falling edge only.
1	Reserved.

Page: Change or Add:

10–26

Description of Bits 9–8 of BCR1

Replace the current description of Bits 9–8 with the following:

Bits 9–8 **SJW.** Synchronization jump width.

SJW indicates by how many units of TQ a bit is allowed to be lengthened or shortened when resynchronizing with the receive data stream on the CAN bus. The synchronization is performed with the falling edge (SBG = 0) of the bus signal. SJW is programmable from 1 to 4 TQ.

Note: Since the SJW[1:0] value is enhanced by one by the CAN module, the value that is written in bits [1:0] is actually (SJW – 1), where SJW is the timing segment referred to in Figure 10–17, CAN Bit Timing.

Page: Change or Add:

10–26

Description of Bits 6–3 of BCR1

Replace the current description of Bits 6–3 with the following:

Bits 6–3 **TSEG1[3:0].** Time segment 1.

This parameter specifies the length of the TSEG1 segment in TQ units.

TSEG1 combines PROP SEG and PHASE SEG1 segments (CAN protocol).

$$\text{TSEG1} = \text{PROP SEG} + \text{PHASE SEG1}.$$

The value of TSEG1 is programmable from 3 to 16 TQ and must be greater than or equal to TSEG2.

Note: Since the TSEG1[3:0] value is enhanced by one by the CAN module, the value that is written in bits [3:0] is actually (TSEG1 – 1), where TSEG1 is the timing segment referred to in Figure 10–17, CAN Bit Timing.

Page:

Change or Add:

10–27

Description of Bits 2–0 of BCR1

Replace the current description of Bits 2–0 with the following:

Bits 2–0 TSEG2[2:0]. Time segment 2.

TSEG2 defines the length of PHASE SEG2 in TQ units.

The value of TSEG2 is programmable from 2 to 8 TQ in compliance with the formula:

$$(SJW + 1) \leq TSEG2 \leq 8.$$

Note: Since the TSEG2[2:0] value is enhanced by one by the CAN module, the value that is written in bits [2:0] is actually (TSEG2 – 1), where TSEG2 is the timing segment referred to in Figure 10–17, CAN Bit Timing.

Note:

The user-defined values for the SJW, TSEG1, and TSEG2 parameters are enhanced by one (by the internal logic) when the CAN module accesses these parameters.

Page:

Change or Add:

10–28

Table 10–4, CAN Bit Timing Examples for I_{CLK} = 40 MHz

Replace the current table with the following:

TSEG1	TSEG2	Bit Time	BRP	Sampling Point	Baud Rate
4	3	10	3	60%	1 Mbit/s
10	7	20	3	60%	500 Kbit/s
9	4	16	9	68.8%	250 Kbit/s
14	8	25	15	64%	100 Kbit/s
11	6	20	39	65%	50 Kbit/s

Page:

Change or Add:

11–10

Section 11.3.3, WD Timer Control Register

Replace the current description of Bit 6 of WDCR with the following:

Bit 6 WDDIS. Watchdog Disable. This bit can be written only when the WD OVER-RIDE bit in the SCSR2 register is 1.

0 Watchdog is enabled.

1 Watchdog is disabled.

Note: Clearing the WD OVERRRIDE bit in the SCSR2 register after disabling the WD would re-enable the WD.

Page: **Change or Add:**
12–2 **Section 12.1, General**
Add the following before the first paragraph: “The 240 is a 5-V part, whereas the 240xA devices operate at 3.3 V.

Page: **Change or Add:**
12–3 **Section 12.2, Event Manager**
Append the following to the current list:

- Some pins in the EV have an “input qualification” circuitry. Refer to the *TMS320LF2407A*, *TMS320LF2406A*, *TMS320LF2403A*, *TMS320LF2402A*, *TMS320LC2406A*, *TMS320LC2404A*, *TMS320LC2402A DSP Controllers* data sheet (literature number SPRS145) for more details.

Page: **Change or Add:**
13–9 **Section 13.4.3.2, Fast \overline{RD} Strobe Operation**
Replace “The W/\overline{R} signal will remain all the time from reset and will go high during external write cycles. Refer to the memory interface timings in the *TMS320LF2407*, *TMS320LF2406*, *TMS320LF2402 DSP Controllers Data Sheet* (literature number SPRS094) for additional timing details.” *with* the following:

In the LF2407A device, the W/\overline{R} signal will remain low all the time after reset and will go high during external write cycles. In other LF240xA devices, the W/\overline{R} signal will remain low all the time after reset until the application configures it as a GPIO pin and drives it to the desired level. During reset, this pin floats and gets pulled up by the internal pullup circuitry. If an application needs this pin to be low even during reset, then an external pulldown resistor may be added.

In LC240xA devices, the W/\overline{R} signal will remain “pulled up” all the time from reset until the application configures it as a GPIO pin and drives it to the desired level.

Refer to the External Memory Interface timings in the *TMS320LF2407A*, *TMS320LF2406A*, *TMS320LF2403A*, *TMS320LF2402A*, *TMS320LC2406A*, *TMS320LC2404A*, *TMS320LC2402A DSP Controllers* data sheet (literature number SPRS145).

Page: **Change or Add:**
13–13 *Add* the following section:
Section 13.6.1 Input Qualification Circuitry
Some pins in the EV have an “input qualification” circuitry. Refer to the *TMS320LF2407A*, *TMS320LF2406A*, *TMS320LF2403A*, *TMS320LF2402A*, *TMS320LC2406A*, *TMS320LC2404A*, *TMS320LC2402A DSP Controllers* data sheet (literature number SPRS145) for more details.

Page:

Change or Add:

v to vi

Related Documentation From Texas Instruments section

Replace the current version *with* the following:

Related Documentation From Texas Instruments

The following books describe the C24x and related support tools. To inquire about any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924. When inquiring, please identify the book by its title and literature number. Many of these documents are located on the Internet at <http://www.ti.com>.

TMS320F/C24x DSP Controllers Reference Guide: CPU and Instruction Set (literature number SPRU160) describes the TMS320C24x 16-bit fixed-point digital signal processor controller. Covered are its architecture, internal register structure, data and program addressing, and instruction set. Also includes instruction set comparisons and design considerations for using the XDS510 emulator.

TMS320LF2407, TMS320LF2406, TMS320LF2402 DSP Controllers (literature number SPRS094) data sheet contains the electrical and timing specifications for these devices, as well as signal descriptions and pinouts for all of the available packages.

TMS320LF2407A, TMS320LF2406A, TMS320LF2403A, TMS320LF2402A, TMS320LC2406A, TMS320LC2404A, TMS320LC2402A DSP Controllers (literature number SPRS145) data sheet contains the electrical and timing specifications for these devices, as well as signal descriptions and pinouts for all of the available packages.

TMS320LF2401A, TMS320LC2401A DSP Controllers (literature number SPRS161) data sheet contains the electrical and timing specifications for these devices, as well as signal descriptions and pinouts for available packages.

TMS320C1x/C2x/C2xx/C5x Code Generation Tools Release 6.60 Getting Started Guide (literature number SPRU121) describes how to install the TMS320C1x, TMS320C2x, TMS320C2xx, and TMS320C5x assembly language tools and the C compiler for the C1x, C2x, C2xx, and C5x devices. The installations for MS-DOS™, OS/2™, SunOS™, and Solaris™ systems are covered.

TMS320C1x/C2x/C2xx/C5x Assembly Language Tools User's Guide (literature number SPRU018) describes the assembly language tools (assembler, linker, and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the C1x, C2x, C2xx, and C5x generations of devices.

TMS320C2x/C2xx/C5x Optimizing C Compiler User's Guide (literature number SPRU024) describes the C2x/C2xx/C5x C compiler. This C compiler accepts ANSI standard C source code and produces TMS320™ assembly language source code for the C2x, C2xx, and C5x generations of devices.

XDS51x Emulator Installation Guide (literature number SPNU070) describes the installation of the XDS510™, XDS510PP™, and XDS510WS™ emulator controllers. The installation of the XDS511™ emulator is also described.

JTAG/MPSD Emulation Technical Reference (literature number SPDU079) provides the design requirements of the XDS510™ emulator controller, discusses JTAG designs (based on the IEEE 1149.1 standard), and modular port scan device (MPSD) designs.

Code Composer Studio User's Guide (literature number SPRU328) explains how to use the Code Composer Studio™ Integrated Development Environment to build and debug embedded real-time DSP applications.

Page: **Change or Add:**

vii **Trademarks** section
 Replace the current version *with* the following:

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