

Manual Update Sheet

DATE: February 19, 2003

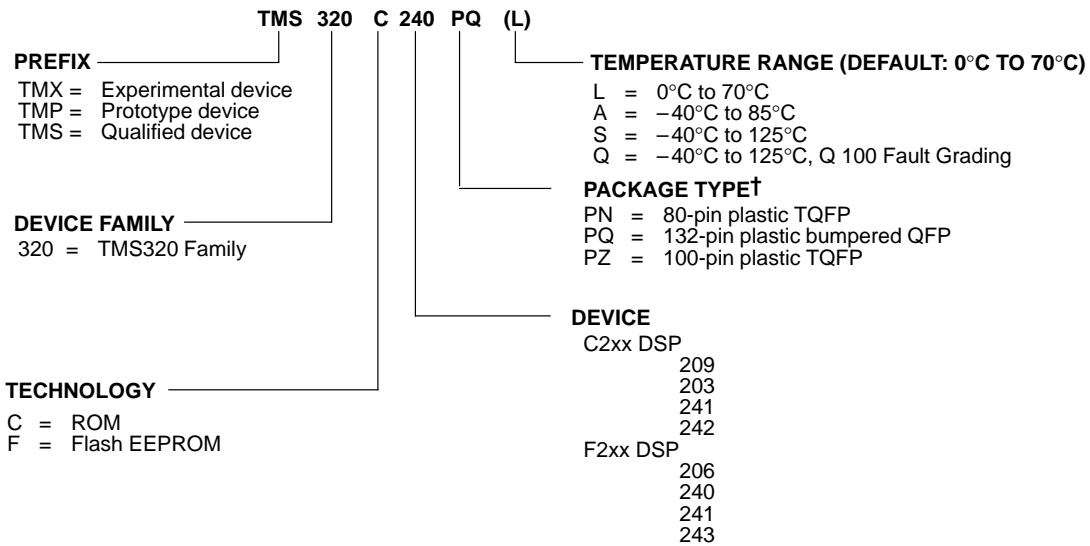
Document Being Updated: *TMS320F/C240 DSP Controllers Reference Guide: Peripheral Library and Specific Devices*

Literature Number Being Updated: SPRU161C

This Manual Update Sheet (literature number SPRZ195) ships with the *TMS320F/C240 DSP Controllers Reference Guide: Peripheral Library and Specific Devices* (literature number SPRU161C).

Page: **Change or Add:**

1-4 **Figure 1-2, TMS320 Device Nomenclature**
 Replace the current drawing with the following:



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Table 2-2, TMS320F/C240 Pin Functions

Updated the descriptions of TCK, TDI, TDO, TMS, and $\overline{\text{TRST}}$ to the following:

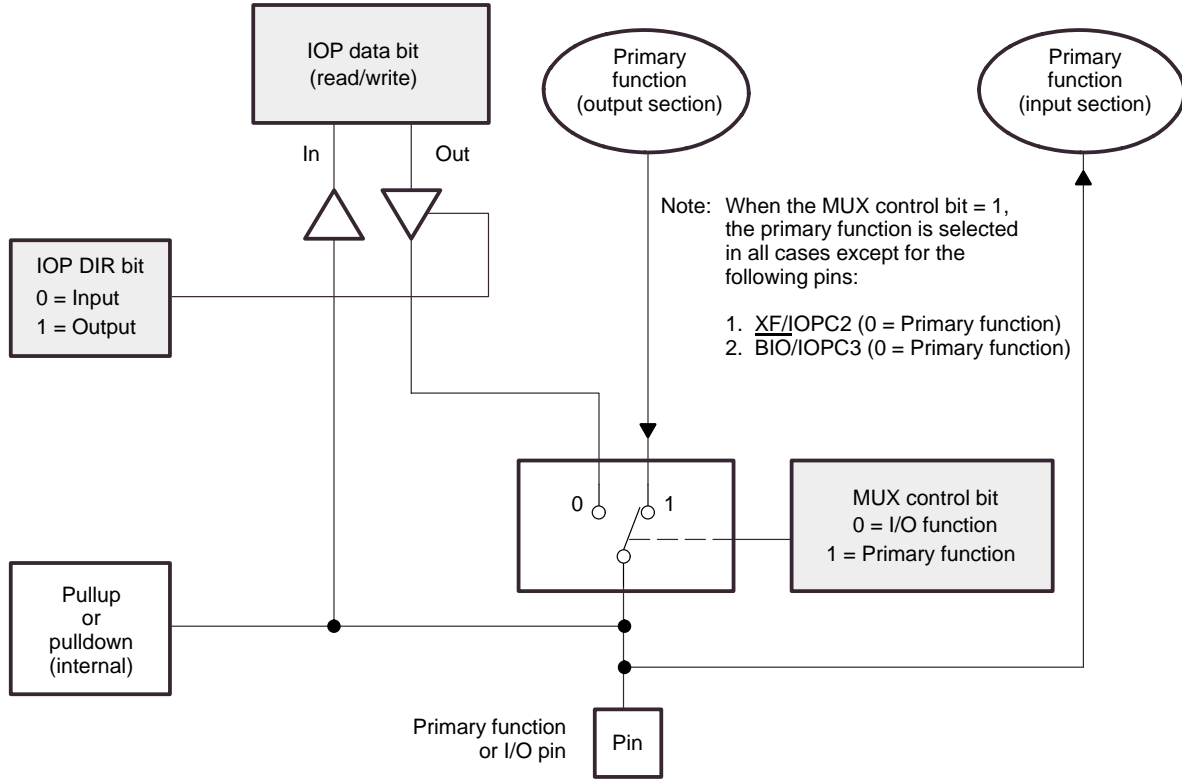
Pin			
Name	No.	Type†	Description
TCK	30	I	JTAG test clock. This is normally a free-running clock signal with a 50% duty cycle. The changes on test-access port (TAP) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test data register of the 'C2xx core on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	31	I	JTAG test data input (TDI). TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	34	O/Z	JTAG test data output (TDO). The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state when $\overline{\text{OFF}}$ is active low.
TMS	33	I	JTAG test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$	32	I	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored.

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Figure 2-6, Shared Pin Configuration

Replace the current drawing with the following:



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Section 2.5.1, Resets

Replace the paragraph about checking flags with the following:

Your program can check the power-on reset flag (PORST flag, SYSSR, IS), the illegal address flag (ILL ADDR flag, SYSSR.12), the software reset flag (SWRST flag, SYSSR.10), and the watchdog reset flag (WDRST flag, SYSSR.9) to determine the source of the reset. A reset does not clear these flags.

Page:

2-34

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Section 2.5.1, Resets

Replace the CAUTION note with the following:

After $\overline{\text{PORESET}}$ goes high and clocks have stabilized (see data sheet for crystal and external oscillator cases), all I/O pins assume a high-impedance state, and PLL/CLK register bits are set to reset values. The $\overline{\text{PORESET}}$ signal decides the reset state of the I/O pins and PLL/CLK bits, irrespective of the $\overline{\text{RS}}$ signal. $\overline{\text{PORESET}}$ should go high before the $\overline{\text{RS}}$ signal goes inactive to ensure that reset conditions are well defined.

The I/O pins and PLL/CLK bits are in their previous state on $\overline{\text{PORESET}}$ low (or undefined on power-up) until $\overline{\text{PORESET}}$ is driven high.

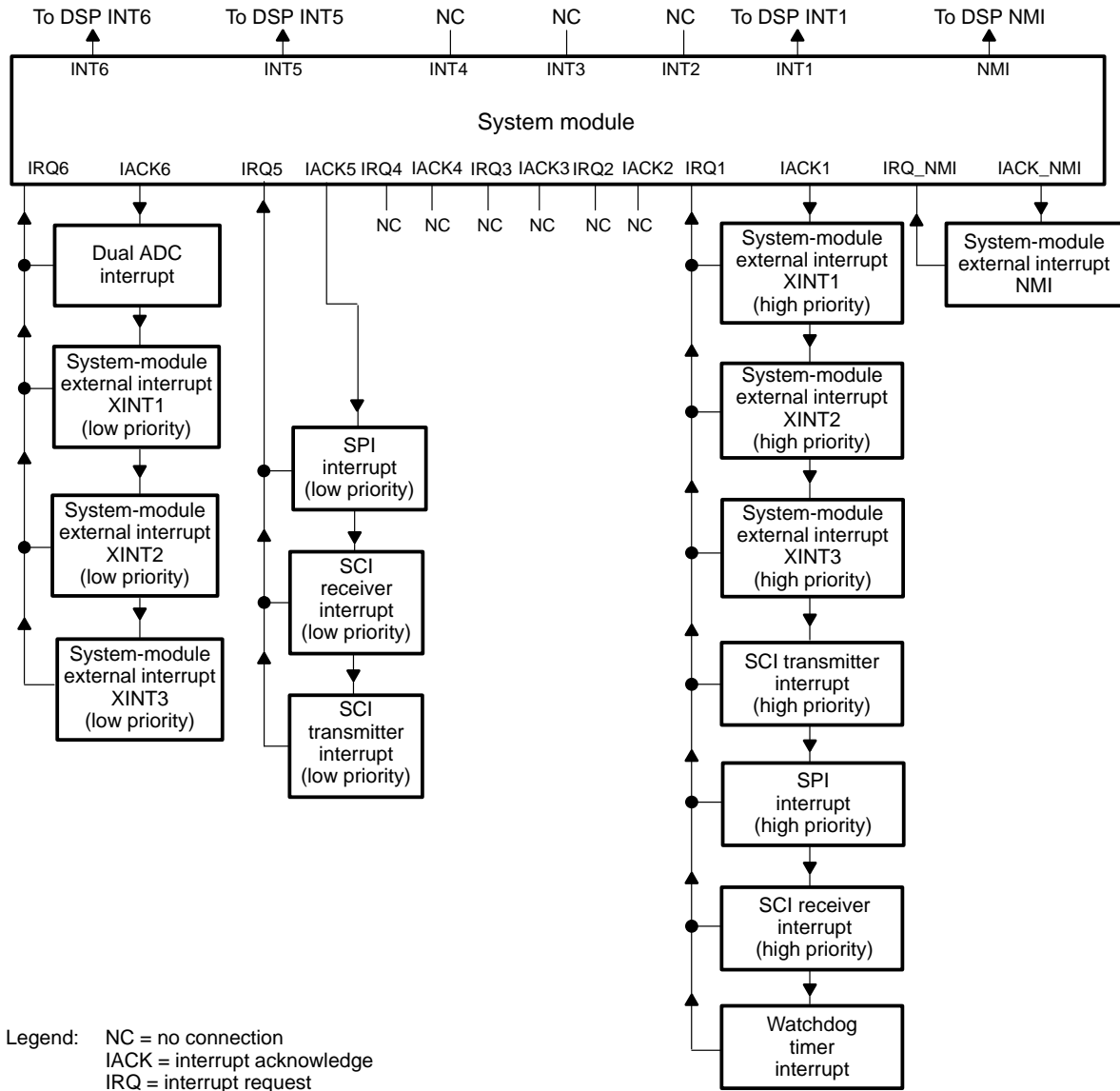
$\overline{\text{RS}}$ is an I/O pin, unlike $\overline{\text{PORESET}}$, which is an input only. After reset, the $\overline{\text{RS}}$ pin functions as an output to internal reset signals such as watchdog.

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Figure 2-15, System-Module Interrupt Structure

Replace the current drawing with the following:



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10-2

Section 10.1, Flash EEPROM Overview

Replace the first paragraph with the following:

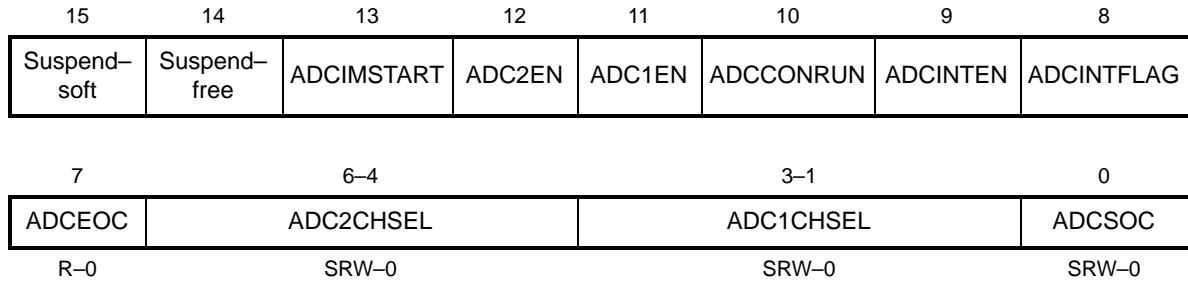
The flash EEPROM module provides an attractive alternative to masked ROM program memory. Like ROM, flash EEPROM is nonvolatile; however, it has the advantage of *in-target* reprogrammability, both on the production floor and in the field.

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A-12

Figure A-16, ADC Control Register 1 (ADCTRL1) — Address 7032h

Replace the current drawing with the following:



Note: R = read access, W = write, S = shadowed, -0 = value after reset

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v to vii

Related Documentation From Texas Instruments section

Replace the current version with the following:

Related Documentation from Texas Instruments

The following books describe the 'F/C240 and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924. When ordering, please identify the book by its title and literature number. Many of these documents are located on the internet at <http://www.ti.com>.

TMS320F/C24x DSP Controllers CPU and Instruction Set Reference Guide (literature number SPRU160) describes the TMS320F/C24x 16-bit fixed-point digital signal processor controller. Covered are its architecture, internal register structure, data and program addressing, and instruction set. Also includes instruction set comparisons and design considerations for using the XDS510 emulator.

TMS320F243/F241/C242 DSP Controllers System and Peripherals Reference Guide (literature number SPRU276) describes the architecture, system hardware, peripherals, and general operation of the TMS320F243, 'F241, and 'C242 digital signal processor (DSP) controllers.

TMS320F240 DSP Controller (literature number SPRS042) data sheet contains the electrical and timing specifications for the TMS320F240 device, as well as signal descriptions and pinouts for all of the available packages.

TMS320F20x/F24x DSP Embedded Flash Memory Technical Reference (literature number SPRU282) describes the operation of the embedded flash EEPROM module on the TMS320F20x/F24x digital signal processor (DSP) and provides sample code that you can use to develop your own software.

TMS320C1x/C2x/C2xx/C5x Code Generation Tools Getting Started Guide (literature number SPRU121) describes how to install the TMS320C1x, TMS320C2x, TMS320C2xx, and TMS320C5x assembly language tools and the C compiler for the 'C1x, 'C2x, 'C2xx, and 'C5x devices. The installations for MS-DOS™, OS/2™, SunOS™, and Solaris™ systems are covered.

TMS320C1x/C2x/C2xx/C5x Assembly Language Tools User's Guide (literature number SPRU018) describes the assembly language tools (assembler, linker, and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C1x™, TMS320C2x™, TMS320C2xx™, and TMS320C5x™ generations of devices.

TMS320C2x/C2xx/C5x Optimizing C Compiler User's Guide (literature number SPRU024) describes the TMS320C2x™, TMS320C2xx™, and TMS320C5x™ C compiler. This C compiler accepts ANSI standard C source code and produces TMS320 assembly language source code for the TMS320C2x, TMS320C2xx, and TMS320C5x generations of devices.

XDS51x Emulator Installation Guide (literature number SPNU070) describes the installation of the XDS510™, XDS510PP™, and XDS510WS™ emulator controllers. The installation of the XDS511™ emulator is also described.

XDS522/XDS522A Emulation System Installation Guide (literature number SPRU171) describes the installation of the emulation system. Instructions include how to install the hardware and software for the XDS522™ and XDS522A™.

XDS522A Emulation System User's Guide (literature number SPRU169) tells you how to use the XDS522A™ emulation system. This book describes the operation of the breakpoint, tracing, and timing functionality in the XDS522A emulation system. This book also discusses BTT software interface and includes a tutorial that uses step-by-step instructions to demonstrate how to use the XDS522A emulation system.

XDS522A Emulation System Online Help (literature number SPRC002) is an online help file that provides descriptions of the BTT software user interface, menus, and dialog boxes.

JTAG/MPSD Emulation Technical Reference (literature number SPDU079) provides the design requirements of the XDS510™ emulator controller, discusses JTAG designs (based on the IEEE 1149.1 standard), and modular port scan device (MPSD) designs.

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