

**Test Data
For PMP9478
8/20/2014**



Power Specification

Vin range: 20V – 32V

Nominal Vin = 24V

Quad Isolated Outputs: $\pm 15\text{V}@50\text{mA}$, $\pm 5\text{V}@50\text{mA}$

Fsw = 350kHz

Board Photos

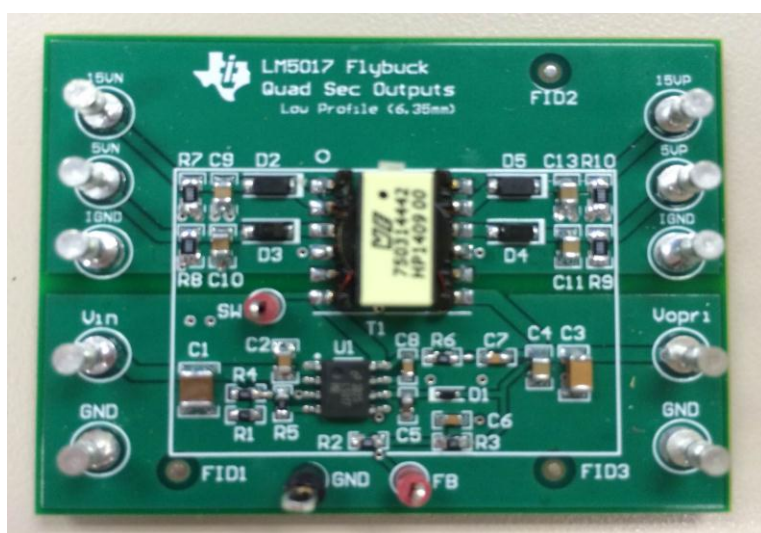


Figure 1. Board Front



Figure 2. Board Back

Size: 36x20mm

5VP: +5V output, 5VN: -5V output

15VP: +15V output, 15VN: -15V output

Efficiency

The efficiency is calculated for all outputs; the load current is incremented at 10mA interval.

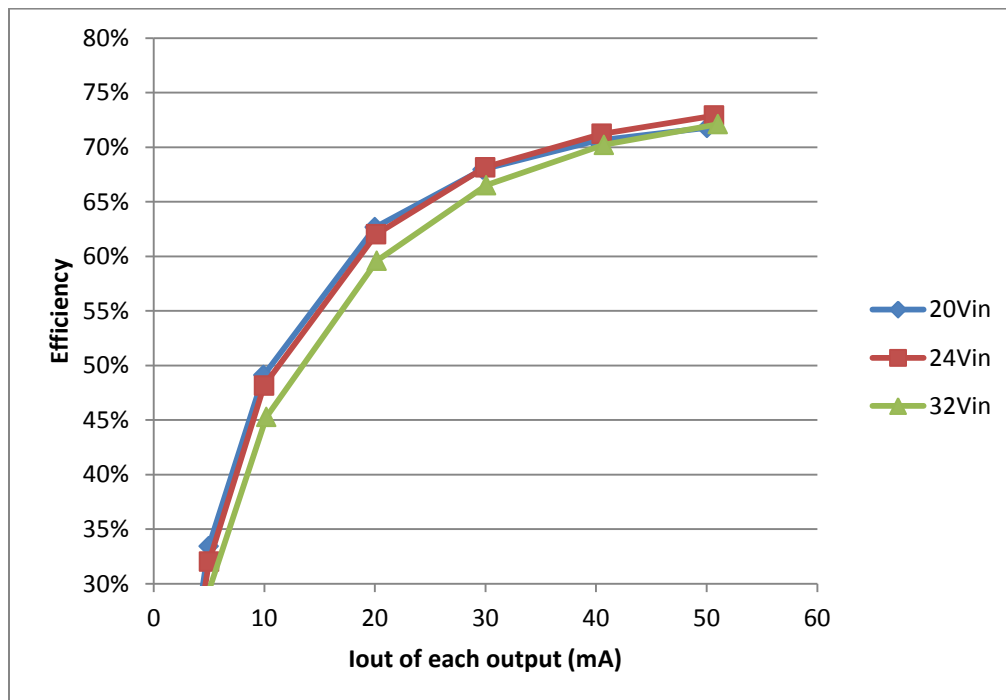
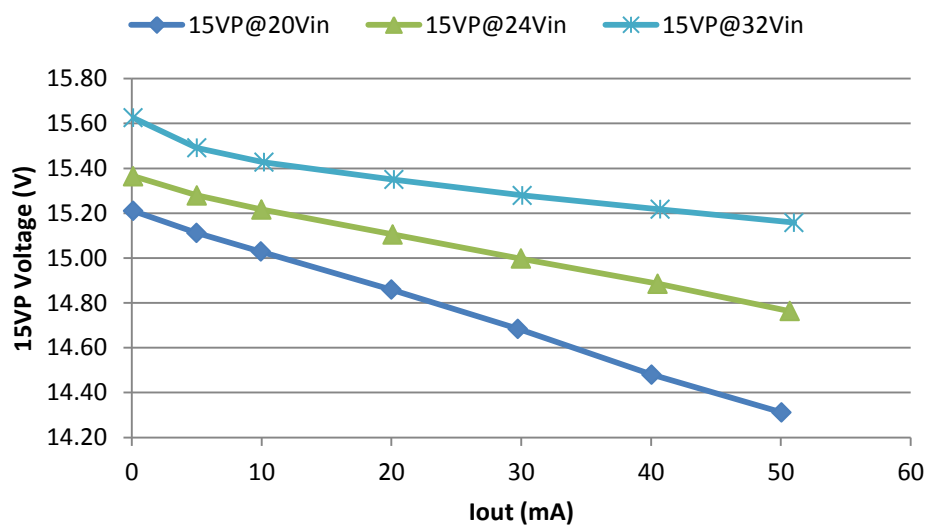
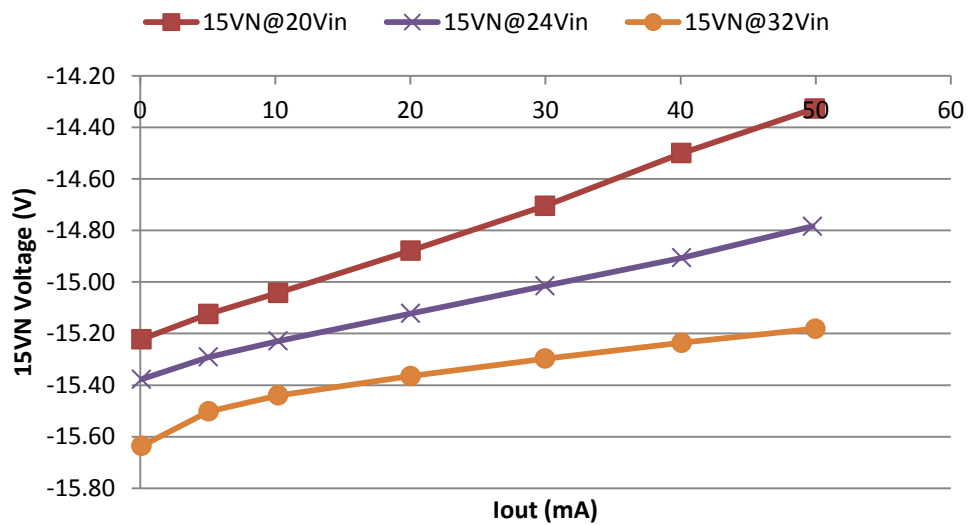


Figure 3. Quad Output Efficiency

Cross Regulation

The cross regulation was tested by sweeping different load condition on 15VP, 15VN, 5VP, and 5VN at various input voltage.

**Figure 4. Positive 15V Vout at Different Load****Figure 5. Negative 15V Vout at Different Load**

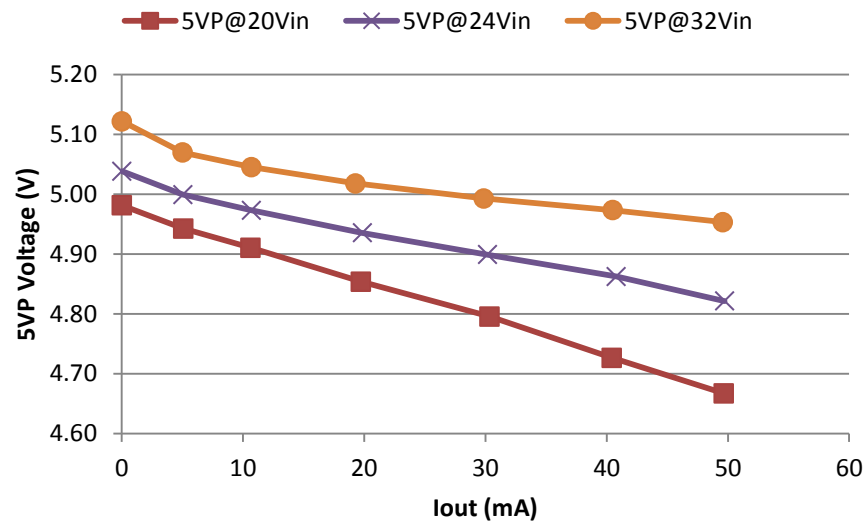


Figure 6. Positive 5V Vout at Different Load

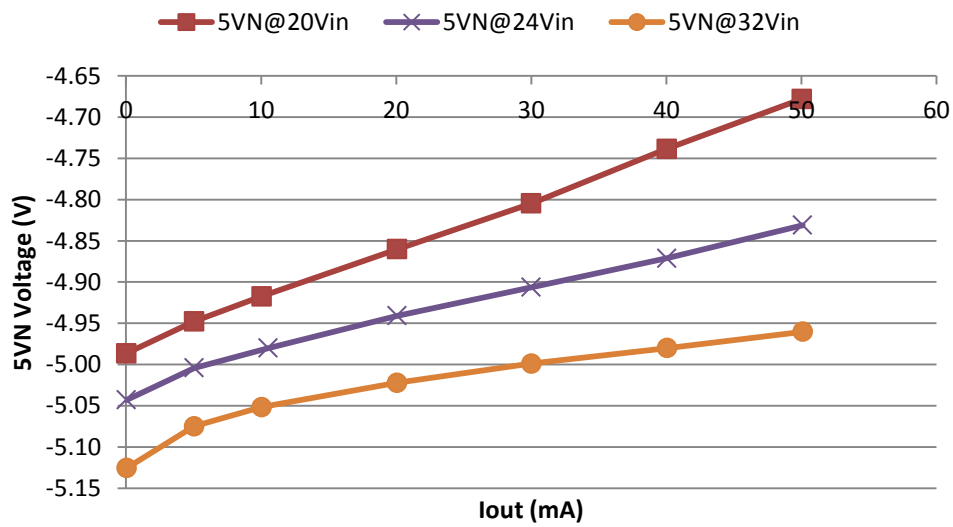


Figure 7. Negative 5V Vout at Different Load

For more data at different Vin, see the Appendix.

Start Up

Test condition 1: The input voltage was set at 24V, and all four outputs were set at full load.
Ch1 - Vin, Ch2 – 5VP (5V), Ch3 – 5VN (-5V)

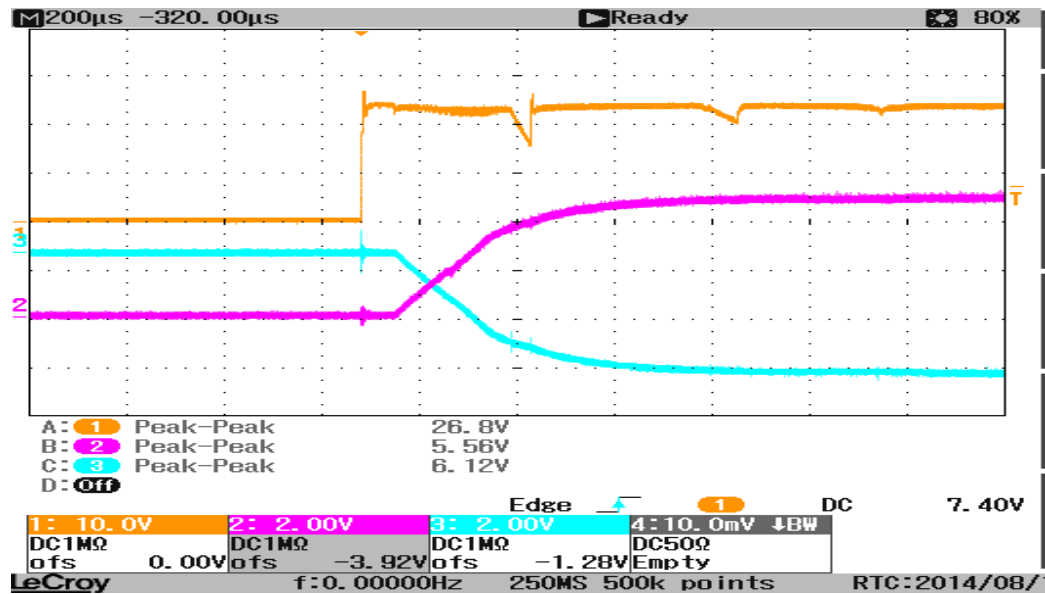


Figure 8. ±5V Start Up at Full Load

Test condition 2: The input voltage was set at 24V, and all four outputs were set at full load.
Ch1 - Vin, Ch2 – 15VP (+15V), Ch3 – 15VN (-15V)

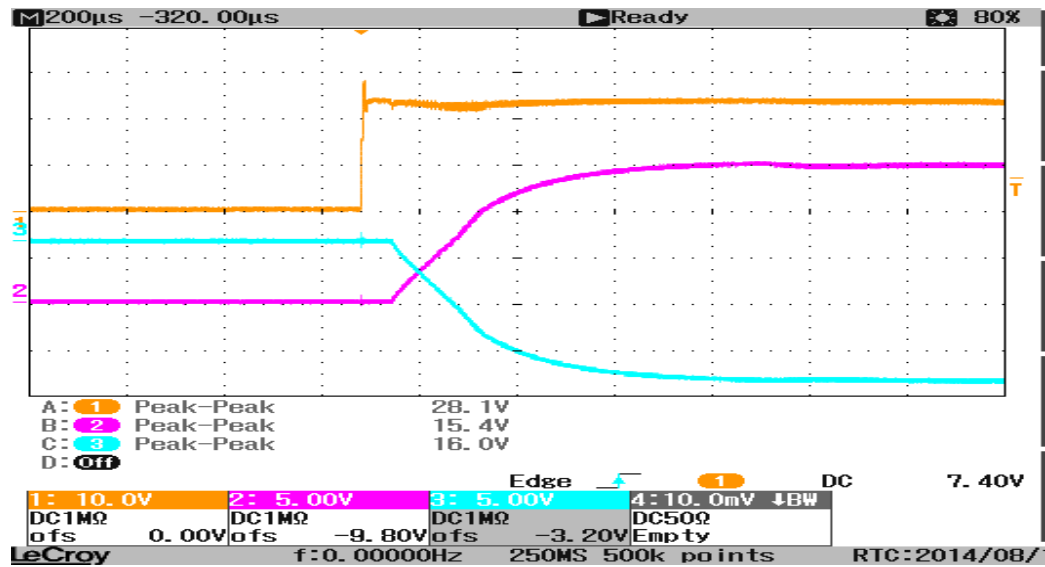


Figure 9. ±15V Start Up at Full Load

Switching Waveforms

- Test condition: The input voltage was set at 24V, and all four outputs were set at full load.
Ch1 – V_{sw} (switch node voltage)

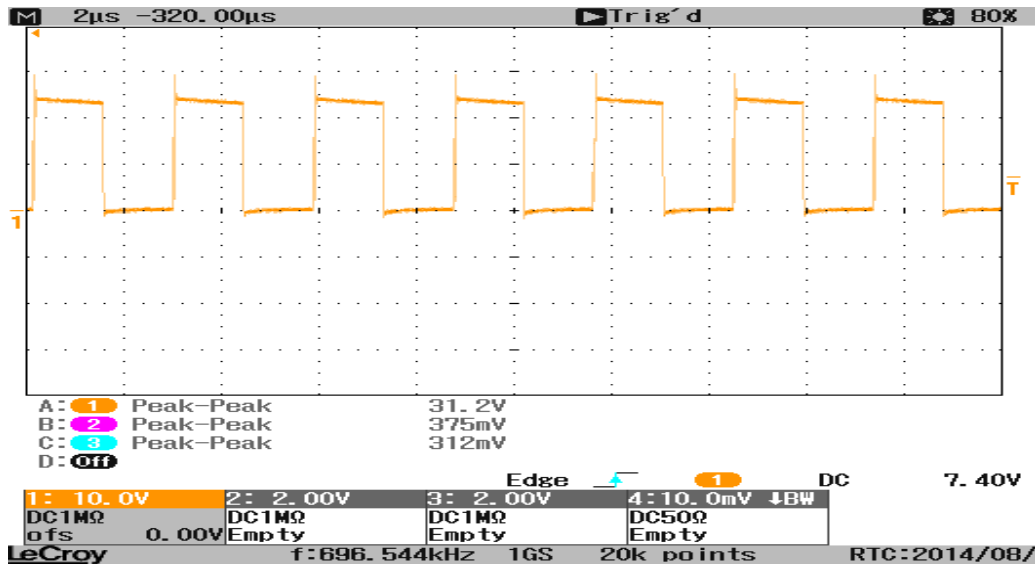


Figure 10. Switch Node Waveform at Full Load

- Test condition: The input voltage was set at 24V, and all four outputs were set at no load.
Ch1 – V_{sw} (switch node voltage)

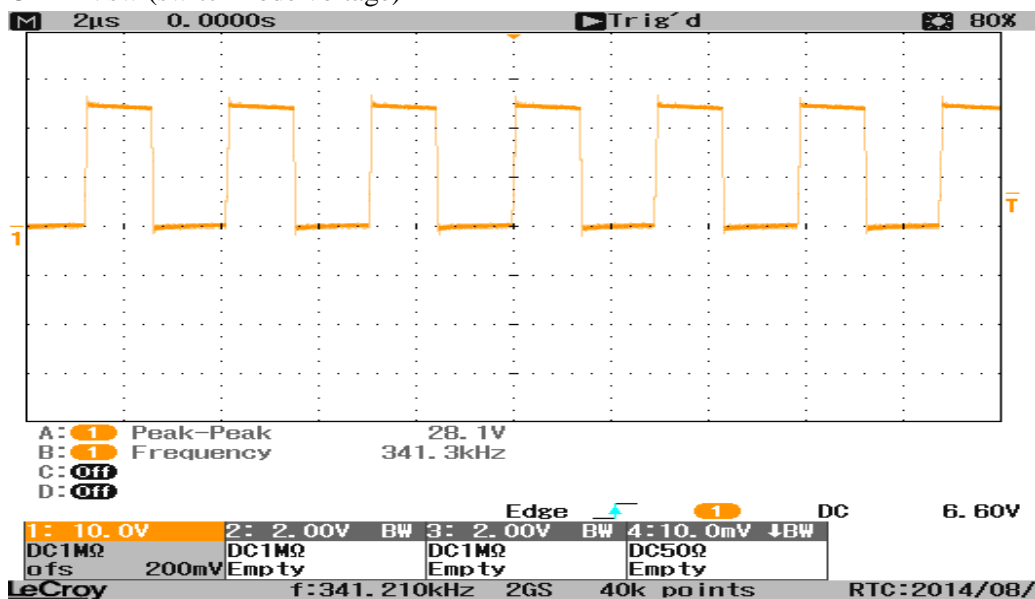


Figure 11. Switch Node Waveform at No Load

3. Test condition: The input voltage was set at 32V, and all four outputs were set at full load. Ch1 – Vd5 (+5V output diode voltage stress from cathode (-) to anode (+))

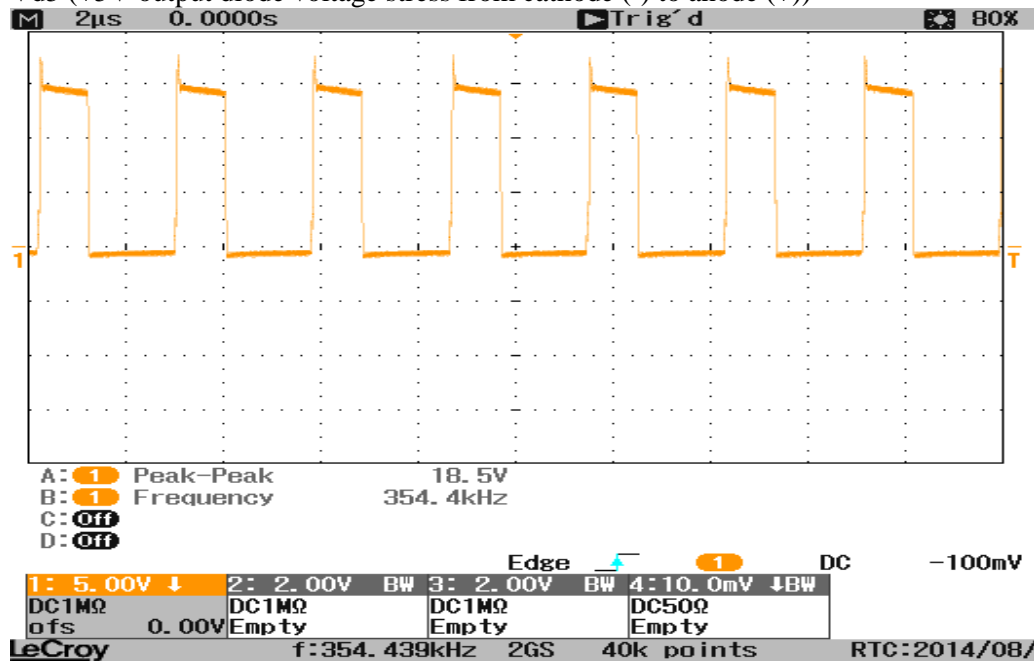


Figure 12. +5V Diode Voltage Stress Waveform at Full Load

4. Test condition: The input voltage was set at 32V, and all four outputs were set at full load. Ch1 – Vd5 (-5V output diode voltage stress from cathode (-) to anode (+))

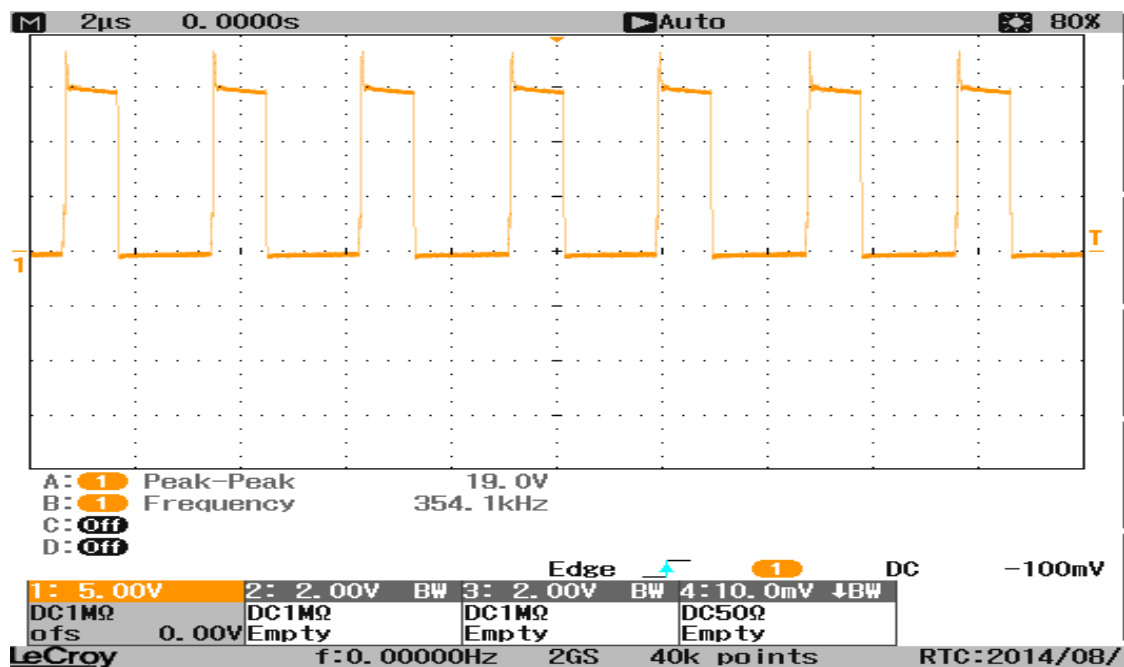


Figure 13. -5V Diode Voltage Stress Waveform at Full Load

5. Test condition: The input voltage was set at 32V, and all four outputs were set at full load. Ch1 – Vd15 (+15V output diode voltage stress from cathode (-) to anode (+))

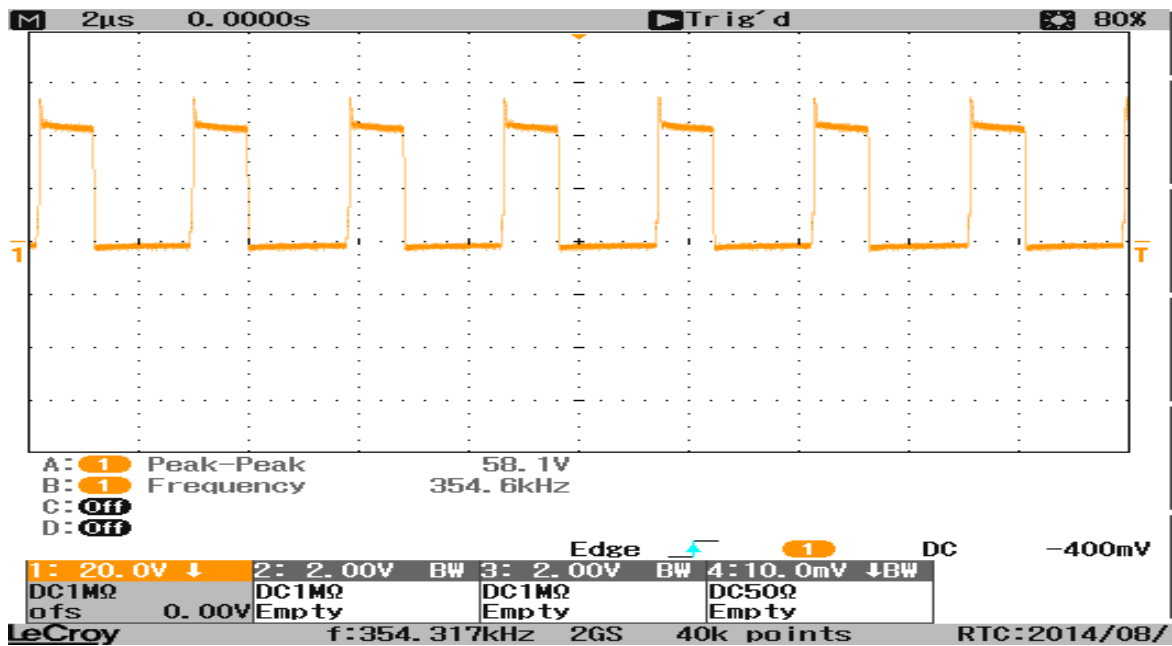


Figure 14. +15V Diode Voltage Stress Waveform at Full Load

6. Test condition: The input voltage was set at 32V, and all four outputs were set at full load. Ch1 – Vd15 (-15V output diode voltage stress from cathode (-) to anode (+))

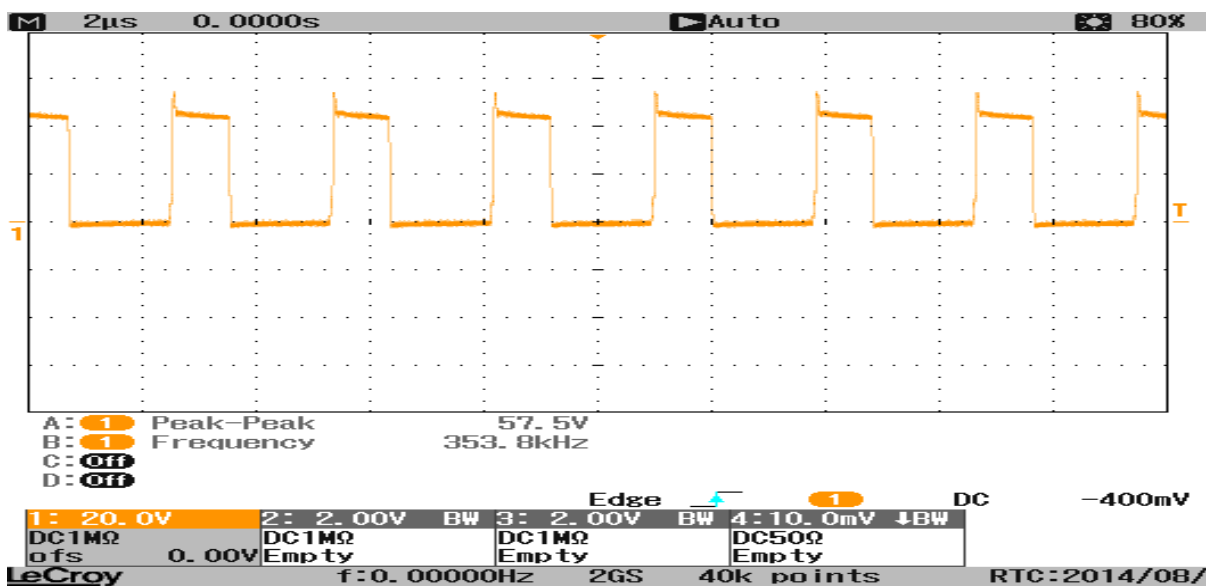


Figure 15. -15V Diode Voltage Stress Waveform at Full Load

Load Transients

+5V Output Load Step

Test condition: $V_{in} = 24V$, 5VP (+5V) load from 0A to 50mA, no load the other outputs.

Ch1- 5VP (+5V) (AC mode), Ch2- 5VN (-5V) (AC mode), Ch4- I_o (+5V output current)

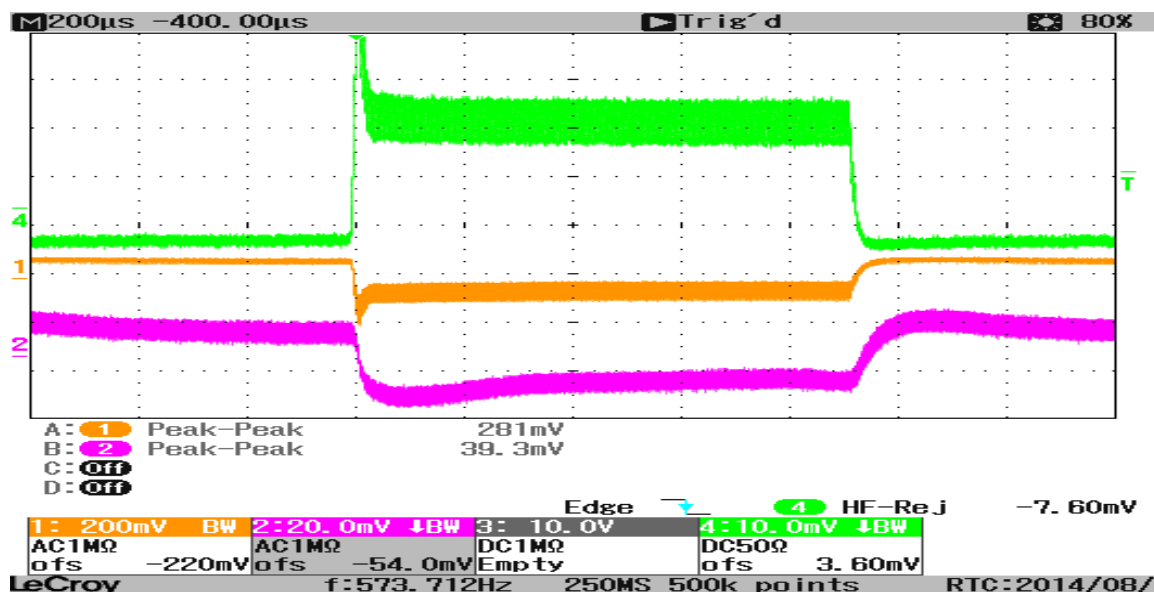


Figure 16. +5V Load Transients

+15V Output Load Step

Test condition: $V_{in} = 24V$, 15VP (+15V) load from 0A to 50mA, no load the other outputs.

Ch1- 15VP (+15V) (AC mode), Ch2- 15VN (-15V) (AC mode), Ch4- I_o (+15V output current)

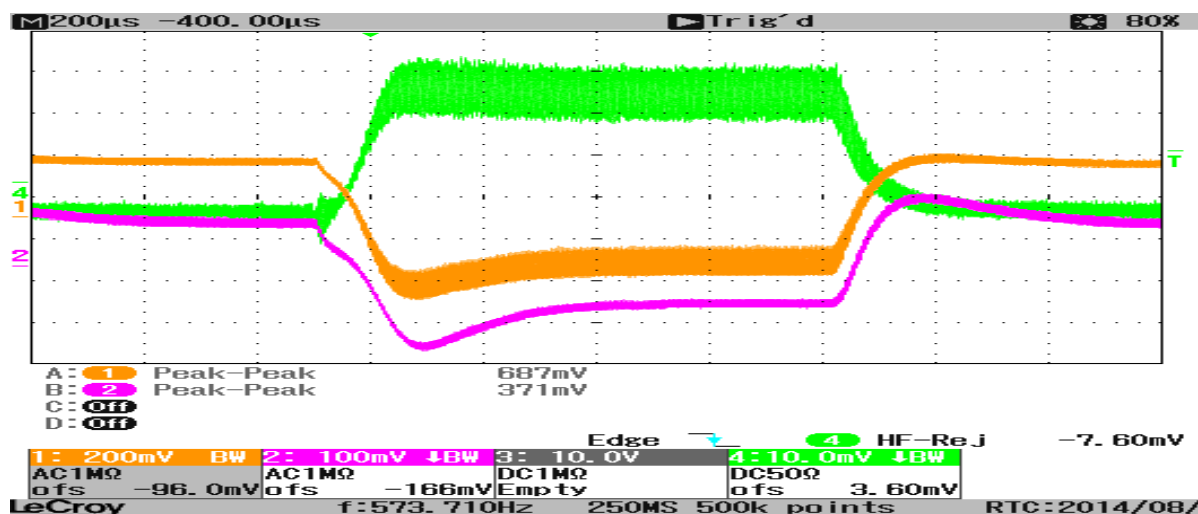


Figure 17. +15V Load Transients

Output Voltage Ripples

Test condition: The input voltage was set at 24V, and all four outputs were set at full load.

Ch2 – 5VP (+5V) (AC coupled)

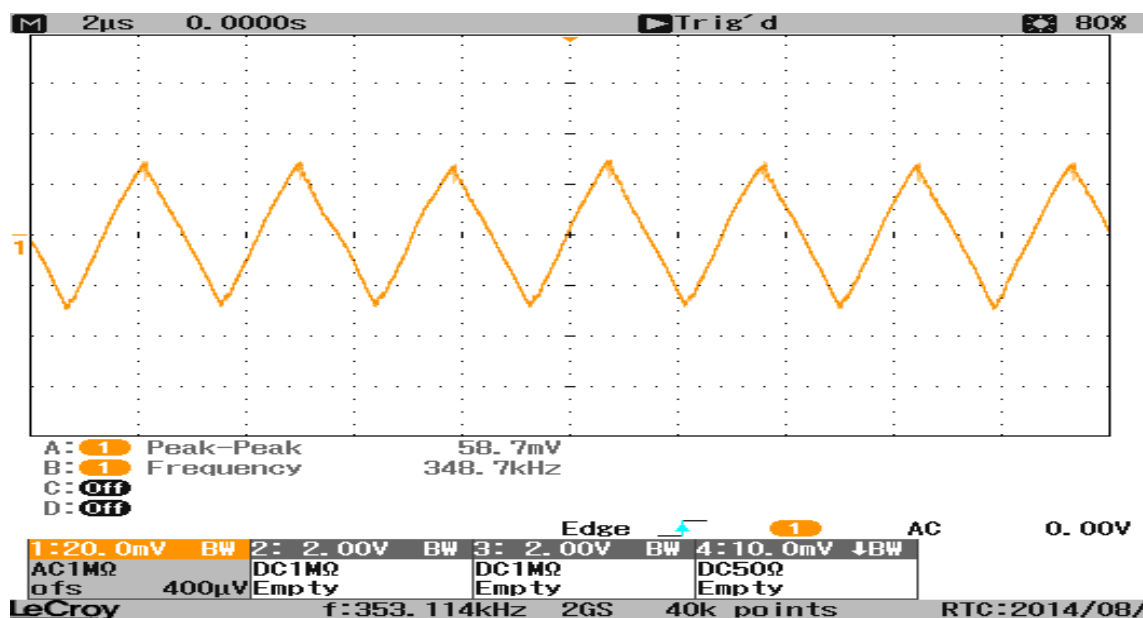


Figure 18. +5V AC Output Ripple at Full Load

Test condition: The input voltage was set at 24V, and all four outputs were set at full load.

Ch2 – 5VN (-5V) (AC coupled)

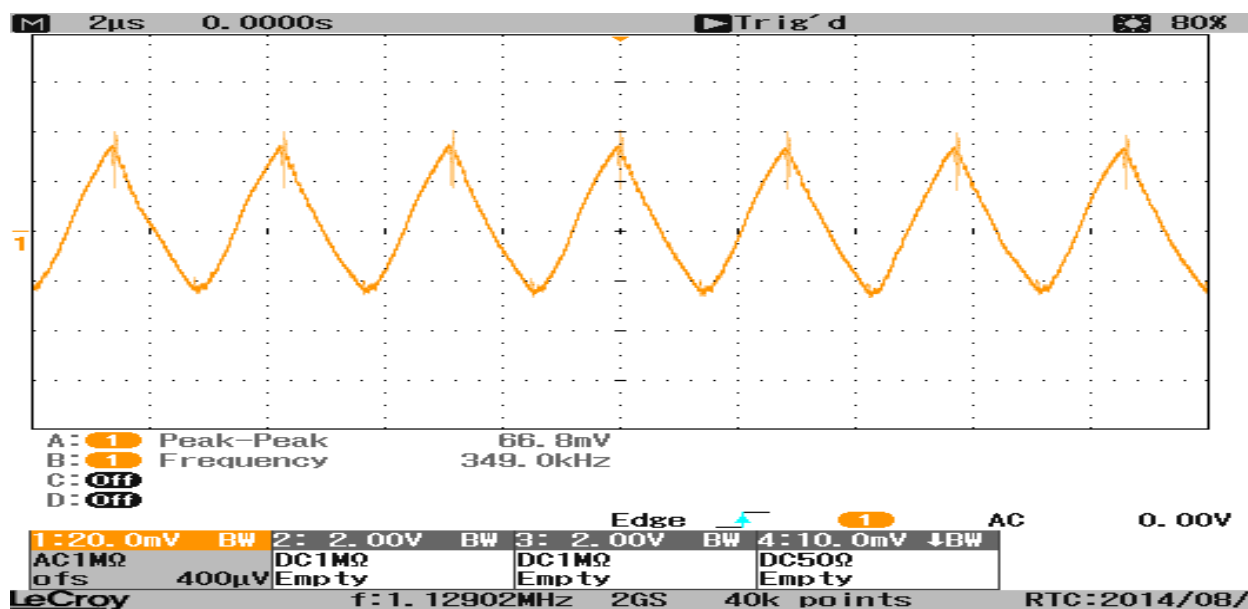


Figure 19. -5V AC Output Ripple at Full Load

Test condition: The input voltage was set at 24V, and all four outputs were set at full load.

Ch2 – 15VN (-15V) (AC coupled)

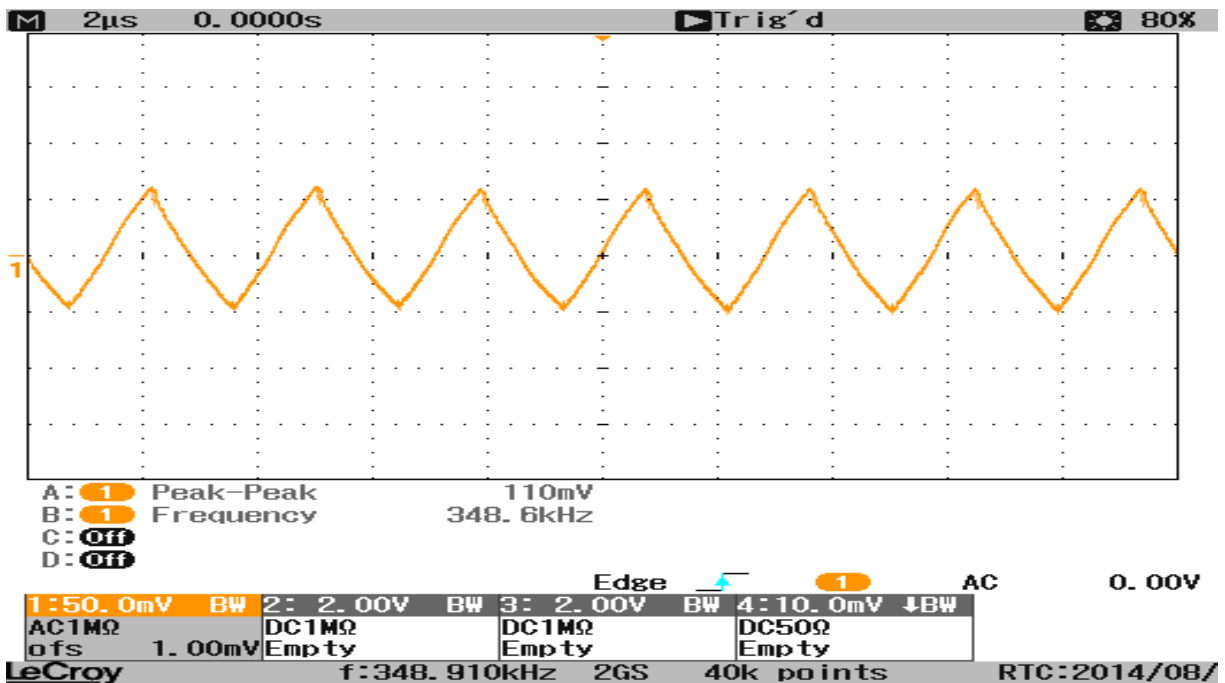


Figure 20. -15V AC Output Ripple at Full Load

Test condition: The input voltage was set at 24V, and all four outputs were set at full load.

Ch2 – 15VP (+15V) (AC coupled)

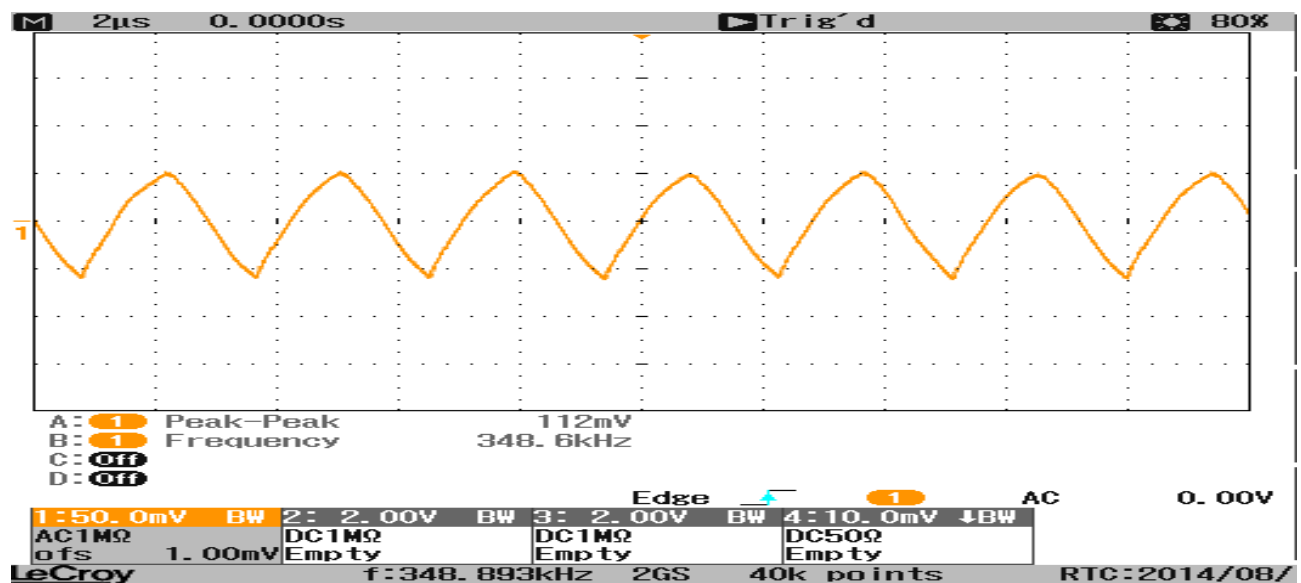


Figure 21. +15V AC Output Ripple at Full Load

Appendix – Test Data

V_{in}=20V

V _{in}	I _{in}	15VP	I _{o15vp}	5VP	I _{o5vp}	15VN	I _{o15vn}	5VN	I _{o5vn}	Efficiency
20.02	19.70	15.21	0.11	4.98	0.02	-15.22	0.10	-4.99	0.04	0.89%
20.05	30.14	15.11	4.98	4.94	5.07	-15.12	5.07	-4.95	5.05	33.43%
20.07	41.04	15.03	9.94	4.91	10.63	-15.04	10.22	-4.92	10.05	49.13%
20.03	62.84	14.86	20.01	4.85	19.73	-14.88	20.03	-4.86	20.07	62.66%
20.05	85.67	14.68	29.75	4.80	30.35	-14.70	29.99	-4.80	30.00	67.96%
19.92	109.67	14.48	40.05	4.73	40.43	-14.50	40.08	-4.74	40.04	70.59%
20.05	131.87	14.31	50.05	4.67	49.65	-14.33	49.94	-4.68	50.05	71.77%

V_{in}=24V

V _{in}	I _{in}	15VP	I _{o15vp}	5VP	I _{o5vp}	15VN	I _{o15vn}	5VN	I _{o5vn}	Efficiency
24.04	17.76	15.37	0.11	5.04	0.02	-15.38	0.11	-5.04	0.04	0.86%
24.01	26.60	15.28	5.01	5.00	5.05	-15.29	5.07	-5.00	5.05	32.05%
23.98	35.77	15.22	9.98	4.97	10.70	-15.23	10.22	-4.98	10.53	48.17%
23.94	54.15	15.11	20.11	4.94	19.85	-15.12	20.03	-4.94	20.07	62.02%
23.96	73.18	15.00	29.98	4.90	30.17	-15.02	29.99	-4.91	30.00	68.16%
23.99	93.30	14.89	40.52	4.86	40.80	-14.91	40.08	-4.87	40.04	71.23%
24.02	112.30	14.76	50.69	4.82	49.73	-14.78	49.78	-4.83	50.09	72.90%

V_{in}=32V

V _{in}	I _{in}	15VP	I _{o15vp}	5VP	I _{o5vp}	15VN	I _{o15vn}	5VN	I _{o5vn}	Efficiency
32.04	15.48	15.63	0.11	5.12	0.02	-15.64	0.11	-5.13	0.04	0.77%
32.05	21.97	15.49	5.02	5.07	5.03	-15.50	5.08	-5.08	5.04	29.49%
32.01	28.96	15.43	10.19	5.05	10.69	-15.44	10.22	-5.05	10.04	45.28%
32.00	42.76	15.35	20.19	5.02	19.29	-15.37	20.04	-5.02	20.08	59.60%
31.97	57.25	15.28	30.09	4.99	29.87	-15.30	29.99	-5.00	30.02	66.53%
31.98	72.65	15.22	40.72	4.97	40.51	-15.24	40.09	-4.98	40.07	70.22%
32.08	87.62	15.16	51.02	4.95	49.59	-15.18	49.98	-4.96	50.11	72.10%

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