

INA122

Single Supply, *MicroPower* INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 60 μ A
- WIDE POWER SUPPLY RANGE
Single Supply: 2.2V to 36V
Dual Supply: -0.9/+1.3V to \pm 18V
- COMMON-MODE RANGE TO (V-) - 0.1V
- RAIL-TO-RAIL OUTPUT SWING
- LOW OFFSET VOLTAGE: 250 μ V max
- LOW OFFSET DRIFT: 3 μ V/ $^{\circ}$ C max
- LOW NOISE: 60nV/ $\sqrt{\text{Hz}}$
- LOW INPUT BIAS CURRENT: 25nA max
- 8-PIN DIP AND SO-8 SURFACE-MOUNT

APPLICATIONS

- PORTABLE, BATTERY OPERATED SYSTEMS
- INDUSTRIAL SENSOR AMPLIFIER:
Bridge, RTD, Thermocouple
- PHYSIOLOGICAL AMPLIFIER:
ECG, EEG, EMG
- MULTI-CHANNEL DATA ACQUISITION

DESCRIPTION

The INA122 is a precision instrumentation amplifier for accurate, low noise differential signal acquisition. Its two-op-amp design provides excellent performance with very low quiescent current, and is ideal for portable instrumentation and data acquisition systems.

The INA122 can be operated with single power supplies from 2.2V to 36V and quiescent current is a mere 60 μ A. It can also be operated from dual supplies. By utilizing an input level-shift network, input common-mode range extends to 0.1V below negative rail (single supply ground).

A single external resistor sets gain from 5V/V to 10000V/V. Laser trimming provides very low offset voltage (250 μ V max), offset voltage drift (3 μ V/ $^{\circ}$ C max) and excellent common-mode rejection.

Package options include 8-pin plastic DIP and SO-8 surface-mount packages. Both are specified for the -40 $^{\circ}$ C to +85 $^{\circ}$ C extended industrial temperature range.



SPECIFICATIONS

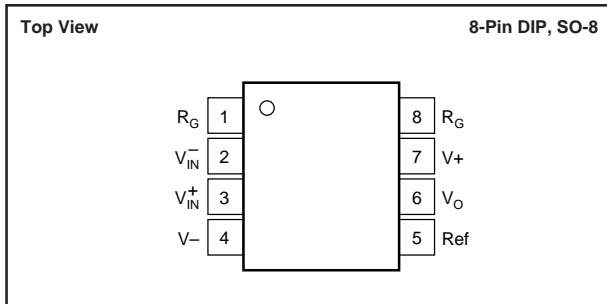
At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 20\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.

PARAMETER	CONDITIONS	INA122P, U			INA122PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI vs Temperature	$V_S = +2.2\text{V to } +36\text{V}$		± 100	± 250		± 150	± 500	μV
vs Power Supply (PSRR)			± 1	± 3		*	± 5	$\mu\text{V}/^\circ\text{C}$
Input Impedance				10	30		*	100
Safe Input Voltage	$R_S = 0$	$(V^-) - 0.3$		$(V^+) + 0.3$	*		*	$\Omega \parallel \text{pF}$
	$R_S = 10\text{k}\Omega$	$(V^-) - 40$		$(V^+) + 40$	*		*	V
Common-Mode Voltage Range		0		3.4	*		*	V
Common-Mode Rejection	$V_{CM} = 0\text{V to } 3.4\text{V}$	83	96		76	90		dB
INPUT BIAS CURRENT								
vs Temperature			-10	-25		*	-50	nA
Offset Current			± 40			*		$\text{pA}/^\circ\text{C}$
vs Temperature			± 1	± 2		*	± 5	nA
			± 40			*		$\text{pA}/^\circ\text{C}$
GAIN			G = 5 to 10k			*		V/V
Gain Equation			G = 5 + 200k Ω /R _G			*		V/V
Gain Error	G = 5		± 0.05	± 0.1		*	± 0.15	%
vs Temperature	G = 5		5	10		*	*	$\text{ppm}/^\circ\text{C}$
Gain Error	G = 100		± 0.3	± 0.5		*	± 1	%
vs Temperature	G = 100		± 25	± 100		*	*	$\text{ppm}/^\circ\text{C}$
Nonlinearity	G = 100, $V_O = -14.85\text{V to } +14.9\text{V}$		± 0.005	± 0.012		*	± 0.024	%
NOISE (RTI)								
Voltage Noise, f = 1kHz			60			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 100Hz			100			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 10Hz			110			*		$\text{nV}/\sqrt{\text{Hz}}$
f _B = 0.1Hz to 10Hz			2			*		$\mu\text{Vp-p}$
Current Noise, f = 1kHz			80			*		$\text{fA}/\sqrt{\text{Hz}}$
f _B = 0.1Hz to 10Hz			2			*		pAp-p
OUTPUT								
Voltage, Positive	$V_S = \pm 15\text{V}$	$(V^+) - 0.1$	$(V^+) - 0.05$		*	*		V
Negative	$V_S = \pm 15\text{V}$	$(V^-) + 0.15$	$(V^-) + 0.1$		*	*		V
Short-Circuit Current	Short-Circuit to Ground		+3/-30			*		mA
Capacitive Load Drive			1			*		nF
FREQUENCY RESPONSE								
Bandwidth, -3dB	G = 5		120			*		kHz
	G = 100		5			*		kHz
	G = 500		0.9			*		kHz
Slew Rate			+0.08/-0.16			*		V/ μs
Settling Time, 0.01%	G = 5		350			*		μs
	G = 100		450			*		μs
	G = 500		1.8			*		ms
Overload Recovery	50% Input Overload		3			*		μs
POWER SUPPLY								
Voltage Range, Single Supply		+2.2	+5	+36	*	*	*	V
Dual Supplies		-0.9/+1.3		± 18	*	*	*	V
Current	$I_O = 0$		60	85		*	*	μA
TEMPERATURE RANGE								
Specification		-40		+85	*		*	$^\circ\text{C}$
Operation		-55		+85	*		*	$^\circ\text{C}$
Storage		-55		+125	*		*	$^\circ\text{C}$
Thermal Resistance, θ_{JA}								
8-Pin DIP			150			*		$^\circ\text{C}/\text{W}$
SO-8 Surface-Mount			150			*		$^\circ\text{C}/\text{W}$

* Specification same as INA122P, INA122U.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V-	36V
Signal Input Terminals, Voltage ⁽²⁾	(V-)-0.3V to (V+)+0.3V
Current ⁽²⁾	5mA
Output Short Circuit	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage.
 (2) Input terminals are internally diode-clamped to the power supply rails. Input signals that can exceed the supply rails by more than 0.3V should be current-limited to 5mA or less.

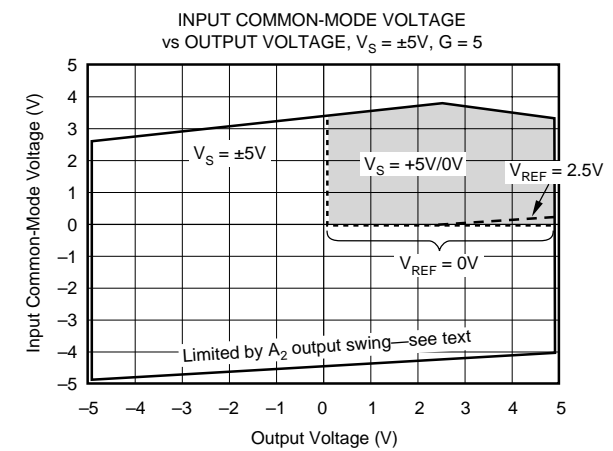
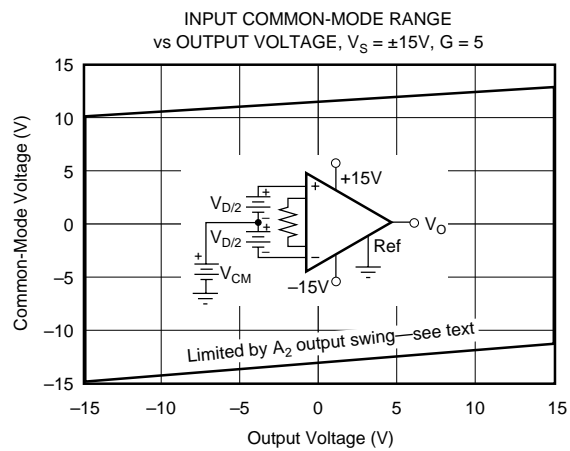
PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
INA122PA	8-Pin DIP	006
INA122P	8-Pin DIP	006
INA122UA	SO-8 Surface Mount	182
INA122U	SO-8 Surface Mount	182

NOTE: (1) For detailed drawing and dimension table, see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

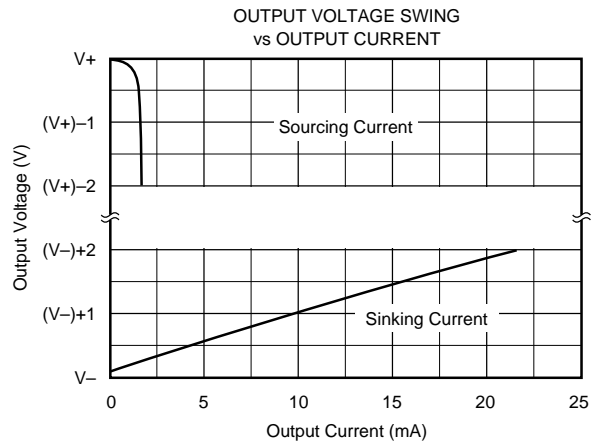
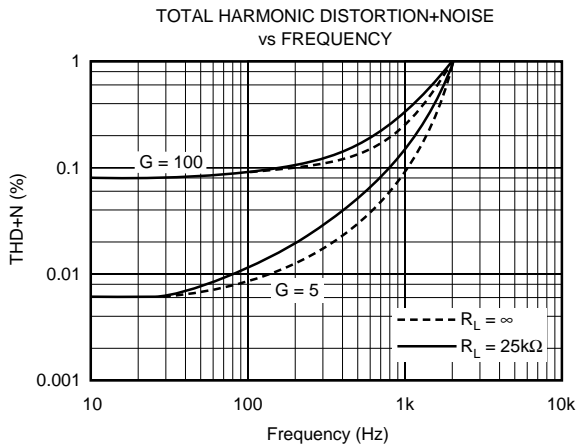
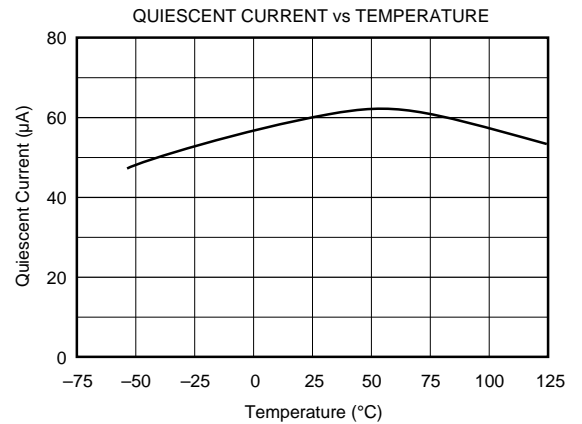
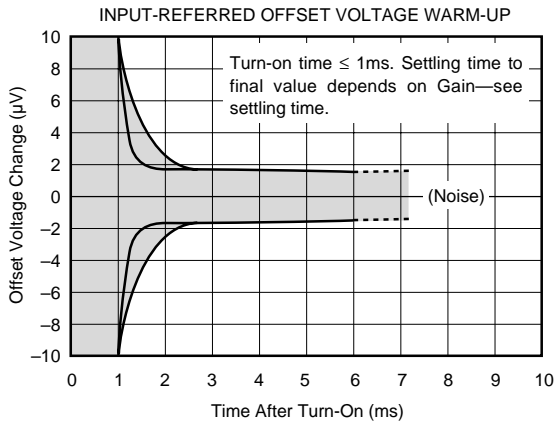
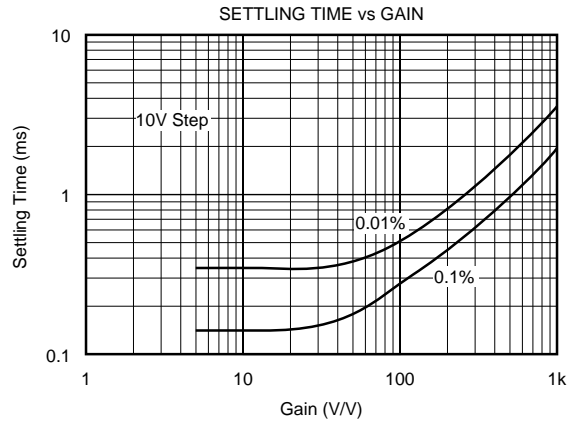
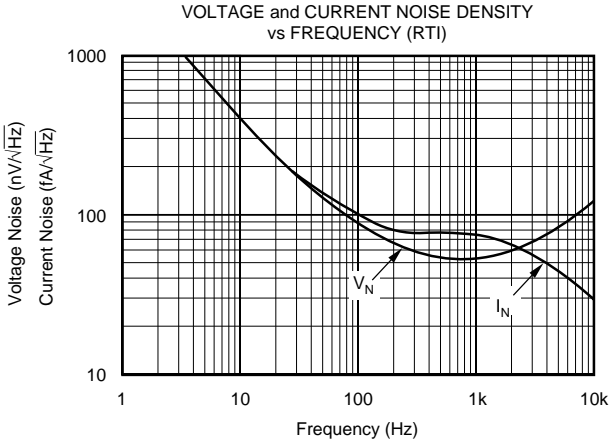
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 5\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

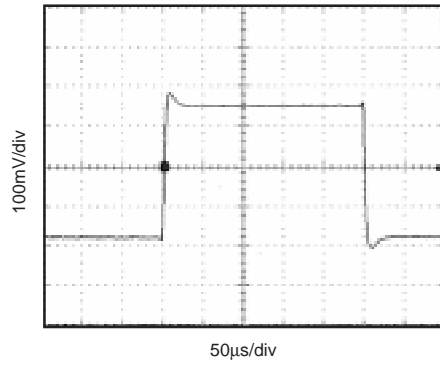
At $T_A = +25^\circ\text{C}$ and $V_S = \pm 5\text{V}$, unless otherwise noted.



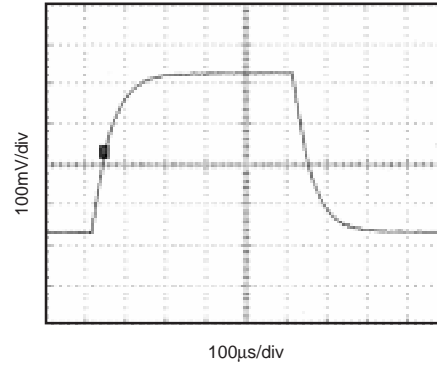
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 5\text{V}$, unless otherwise noted.

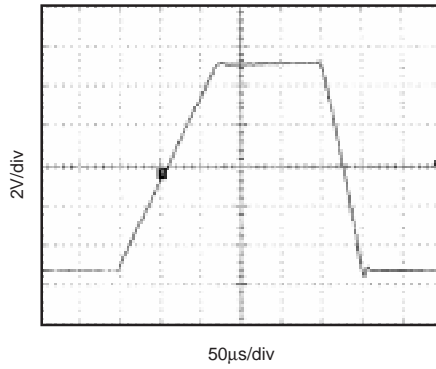
SMALL-SIGNAL STEP RESPONSE
 $G = 5$



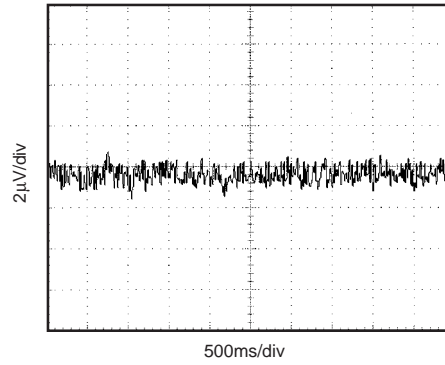
SMALL-SIGNAL STEP RESPONSE
 $G = 100$



LARGE-SIGNAL STEP RESPONSE
 $G = 5$



INPUT-REFERRED NOISE VOLTAGE
0.1Hz to 10Hz



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA122. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to ensure good common-mode rejection. A resistance of 10Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR.

SETTING THE GAIN

Gain of the INA122 is set by connecting a single external resistor, R_G , as shown:

$$G = 5 + \frac{200\text{k}\Omega}{R_G} \quad (1)$$

Commonly used gains and R_G resistor values are shown in Figure 1.

The 200kΩ term in equation 1 comes from the internal metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA122.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1).

OFFSET TRIMMING

The INA122 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external

offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is added to the output signal. An op amp buffer is used to provide low impedance at the Ref terminal to preserve good common-mode rejection.

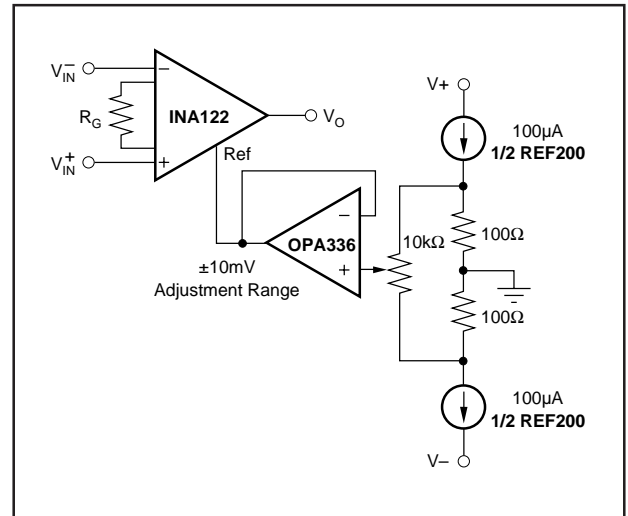


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA122 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately -10nA (current flows out of the input terminals). High input impedance means that this input bias current changes very little with varying input voltage.

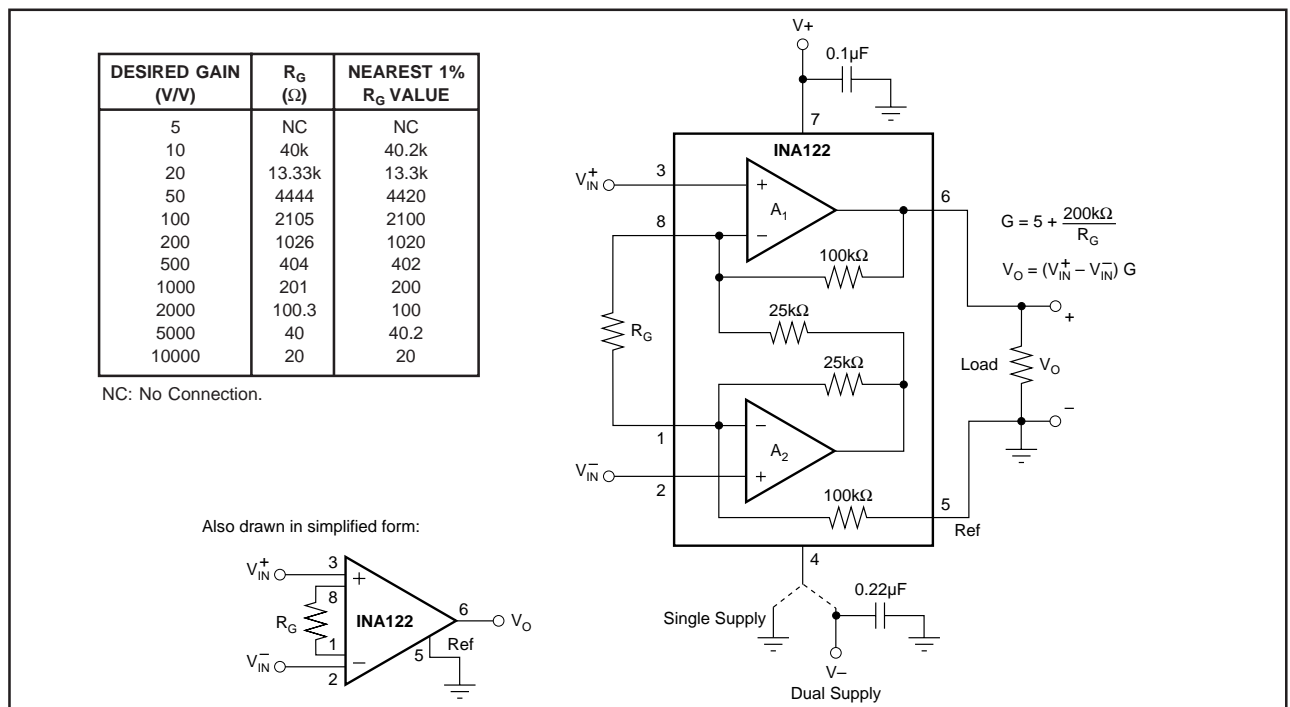


FIGURE 1. Basic Connections.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA122 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

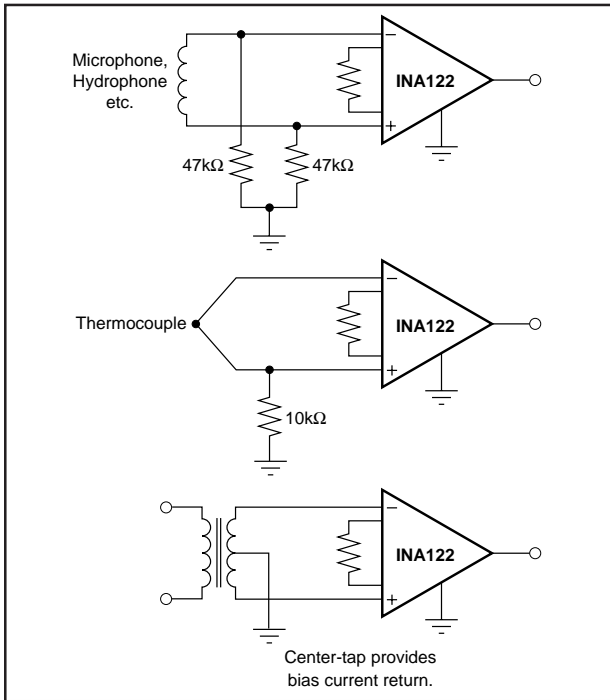


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT PROTECTION

The inputs of the INA122 are protected with internal diodes connected to the power supply rails (Figure 4). These diodes will clamp the applied signal to prevent it from damaging the input circuitry. If the input signal voltage can exceed the power supplies by more than 0.3V, the input signal current should be limited to less than 5mA to protect the internal clamp diodes. This can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

INPUT COMMON-MODE RANGE

The common-mode range for some common operating conditions is shown in the typical performance curves. The INA122 can operate over a wide range of power supply and V_{REF} configurations, making it impractical to provide a comprehensive guide to common-mode range limits for all possible conditions. The most commonly overlooked overload condition occurs by attempting to exceed the output swing of A_2 , an internal circuit node that cannot be measured. Calculating the expected voltages at A_2 's output (see equation in Figure 4) provides a check for the most common overload conditions.

The design of A_1 and A_2 are identical and their outputs can swing to within approximately 100mV of the power supply rails, depending on load conditions. When A_2 's output is saturated, A_1 can still be in linear operation, responding to changes in the non-inverting input voltage. This may give the appearance of linear operation but the output voltage is invalid.

A single supply instrumentation amplifier has special design considerations. Using commonly available single-supply op amps to implement the two-op amp topology will not yield equivalent performance. For example, consider the condition where both inputs of common single-supply op amps are



FIGURE 4. INA122 Simplified Circuit Diagram.

equal to 0V. The outputs of both A_1 and A_2 must be 0V. But any small positive voltage applied to V_{IN}^+ requires that A_2 's output must swing below 0V, which is clearly impossible without a negative power supply.

To achieve common-mode range that extends to single-supply ground, the INA122 uses precision level-shifting buffers on its inputs. This shifts both inputs by approximately +0.5V, and through the feedback network, shifts A_2 's output by approximately +0.6V. With both inputs and V_{REF} at single-supply, A_2 's output is well within its linear range. A positive V_{IN}^+ causes A_2 's output to swing below 0.6V.

As a result of this input level-shifting, the voltages at pin 1 and pin 8 are not equal to their respective input terminal voltages (pins 2 and 3). For most applications, this is not important since only the gain-setting resistor connects to these pins.

LOW VOLTAGE OPERATION

The INA122 can be operated on a single power supply as low as +2.2V (or a total of +2.2V on dual supplies). Performance remains excellent throughout the power supply range up to +36V (or $\pm 18V$). Most parameters vary only slightly throughout this supply voltage range—see typical performance curves.

Operation at very low supply voltage requires careful attention to ensure that the common-mode voltage remains within its linear range.

LOW QUIESCENT CURRENT OPERATION

The INA122 maintains its low quiescent current ($60\mu A$) while the output is within linear operation (up to 200mV from the supply rails). When the input creates a condition that overdrives the output into saturation, quiescent current increases. With V_O overdriven into the positive rail, the quiescent current increases to approximately $400\mu A$. Likewise, with V_O overdriven into the negative rail (single supply ground) the quiescent current increases to approximately $200\mu A$.

OUTPUT CURRENT RANGE

Output sourcing and sinking current values versus the output voltage ranges are shown in the typical performance curves. The positive and negative current limits are not equal. Positive output current sourcing will drive moderate to high load impedances. Battery operation normally requires the careful management of power consumption to keep load impedances very high throughout the design.



FIGURE 5. Micropower Single Supply Bridge Amplifier.



FIGURE 6. Single-Supply Current Shunt Measurement.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA122P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	INA122P	Samples
INA122PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA122P A	Samples
INA122PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA122P A	Samples
INA122U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI		INA 122U	
INA122U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 122U	Samples
INA122UA	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI		INA 122U A	
INA122UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 122U A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA122U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA122UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA122U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA122UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA122P	P	PDIP	8	50	506	13.97	11230	4.32
INA122PA	P	PDIP	8	50	506	13.97	11230	4.32
INA122PAG4	P	PDIP	8	50	506	13.97	11230	4.32
INA122U	D	SOIC	8	75	506.6	8	3940	4.32
INA122UA	D	SOIC	8	75	506.6	8	3940	4.32

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated