TCA4311 Hot Swappable 2-Wire Bus Buffers

Not Recommended for New Designs

1 Features

- Operating Power-Supply Voltage Range of 2.7-V to 5.5-V
- Supports Bidirectional Data Transfer of I^2C Bus Signals
- SDA and SCL Lines Are Buffered Which Increases Fanout
- 1-V Precharge on All SDA and SCL Lines Prevents Corruption During Live Board Insertion and Removal From Backplane
- SDA and SCL Input Lines Are Isolated From Outputs
- Accommodates Standard Mode and Fast Mode I^2C Devices
- Applications Include Hot Board Insertion and Bus Extension
- Low I_{CC} Chip Disable of <1 µA
- READY Open-Drain Output
- Supports Clock Stretching, Arbitration, and Synchronization
- Powered-Off High-Impedance I^2C Pins
- Open-Drain I^2C Pins
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Description

The TCA4311 is a hot swappable I^2C bus buffer that supports I/O card insertion into a live backplane without corruption of the data and clock busses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, this device provides bidirectional buffering, keeping the backplane and card capacitances isolated. During insertion, the SDA and SCL lines are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

When the I^2C bus is idle, the TCA4311 can be put into shutdown mode by setting the EN pin low. When EN is high, the TCA4311 resumes normal operation. It also includes an open drain READY output pin, which indicates that the backplane and card sides are connected together. When READY is high, the SDAIN and SCLIN are connected to SDAOUT and SCLOUT. When the two sides are disconnected, READY is low.

Both the backplane and card may be powered with supply voltages ranging from 2.7 V to 5.5 V, with no restrictions on which supply voltage is higher.

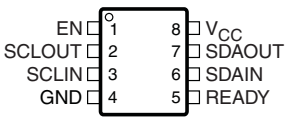
The TCA4311 has standard open-drain I/Os. The size of the pullup resistors to the I/Os depends on the system, but each side of this buffer must have a pullup resistor. The device is designed to work with Standard Mode and Fast Mode I^2C devices in addition to SMBus devices. Standard Mode I^2C devices only specify 3 mA in a generic I^2C system where Standard Mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA4311	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

D OR DGK PACKAGES
(TOP VIEW)



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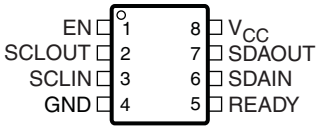
3 Revision History

Changes from Original (December 2008) to Revision A	Page
• Added Missing ACK Errata section.	10

4 Pin Configuration and Functions

D OR DGK PACKAGES
(TOP VIEW)



Pin Functions

SOIC (D) OR MSOP (DGK) PACKAGE		DESCRIPTION
PIN NUMBER	NAME	
1	EN	Active-high chip enable pin. If EN is low, the TCA4311 is in a low current (<1 μA) mode. It also disables the rise-time accelerators, disables the bus precharge circuitry, drives READY low, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT. EN should be high (at V_{CC}) for normal operation. Connect EN to V_{CC} if this feature is not being used.
2	SCLOUT	Serial clock output. Connect this pin to the SCL bus on the card.
3	SCLIN	Serial clock input. Connect this pin to the SCL bus on the backplane.
4	GND	Supply ground
5	READY	Connection flag/rise-time accelerator control. READY is low when either EN is low or the start-up sequence described in the operation section has not been completed. READY goes high when EN is high and start-up is complete. Connect a 10-kΩ resistor from this pin to V_{CC} to provide the pull up.
6	SDAIN	Serial data input. Connect this pin to the SDA bus on the backplane.
7	SDAOUT	Serial data output. Connect this pin to the SDA bus on the card.
8	V_{CC}	Supply power. Main input power supply from backplane. This is the supply voltage for the devices on the backplane I^2C busses. Connect pullup resistors from SDAIN and SCLIN (and also from SDAOUT and SCLOUT) to this pin. Place a bypass capacitor of at least 0.01 μF close to this pin for best results.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range(2)	SDAIN, SCLIN, SDAOUT, SCLOUT	–0.3	7	V
V_I	Input voltage range(2)	EN	–0.3	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
I_{CC}	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(3)	D package		97	°C/W
		DGK package		172	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	5.5	V
V_{IH}	High-level input voltage	SDA and SCL inputs	0.7 × V_{CC}	5.5	V
		EN input	2	5.5	
V_{IL}	Low-level input voltage	SDA and SCL inputs	–0.5	0.3 × V_{CC}	V
		EN input	–0.5	0.8	
I_{OL}	Low-level output current	V_{CC} = 3 V		3	mA
		V_{CC} = 4.5 V		3	
T_A	Operating free-air temperature		–40	85	°C

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{CC}	Positive supply voltage		2.7		5.5	V
I_{CC}	Supply current	V_{CC} = 5.5 V, V_{SDAIN} = V_{SCLIN} = 0 V		5.1	7	mA
I_{SD}	Supply current in shutdown mode	V_{EN} = 0 V		0.1		µA
Start-Up Circuitry						
V_{PRE}	Precharge voltage	SDA, SCL floating	0.8	1	1.2	V
t_{IDLE}	Bus idle time		50	95	150	µs
V_{EN}	EN threshold voltage			0.5 × V_{CC}	0.9 × V_{CC}	V
V_{DIS}	Disable threshold voltage	EN Pin	0.1 × V_{CC}	0.5 × V_{CC}		V
I_{EN}	EN input current	EN from 0 V to V_{CC}		±0.1	±1	µA
t_{EN}	Enable time			95		µs
t_{DIS}	Disable time (EN to READY)			30		ns
t_{STOP}	SDAIN to READY delay after STOP			1.2		µs
t_{READY}	SCLOUT/SDAOUT to READY			0.8		µs
I_{OFF}	READY OFF state leakage current			±0.1		µA
V_{OL}	READY output low voltage	I_{PULLUP} = 3 mA			0.4	V
Rise-Time Accelerators						
$I_{PULLUPAC}$	Transient boosted pull-up current	Positive transition on SDA, SCL, V_{CC} = 2.7 V,	1	2		mA
Input-Output Connection						
V_{OS}	Input-output offset voltage	10 kΩ to V_{CC} on SDA, SCL, V_{CC} = 3.3 V,(1)	0	100	175	mV
C_{IN}	Digital input capacitance				10	pF
V_{OL}	Output low voltage, input = 0 V	SDA, SCL pins, I_{SINK} = 3 mA,	0		0.4	V
I_I	Input leakage current	SDA, SCL pins = V_{CC} = 5.5 V			±5	µA

(1) The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pullup resistor and V_{CC} voltage is shown in the *Typical Characteristics* section.

5.5 Typical Characteristics

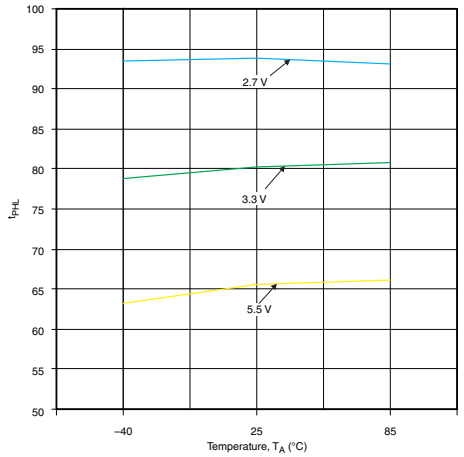


Figure 1. Input/Output t_{PLH} vs Temperature

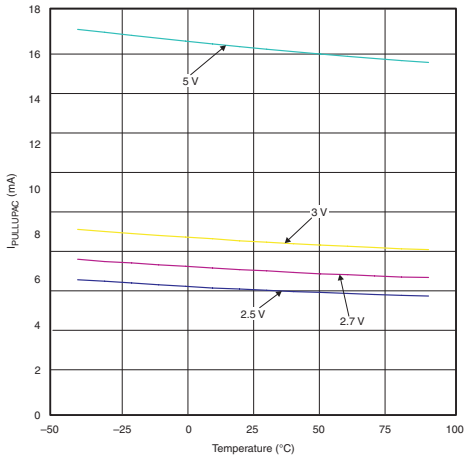


Figure 2. $I_{PULLUPAC}$ vs Temperature

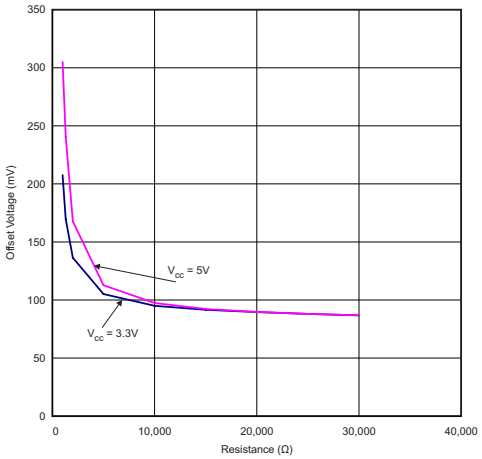
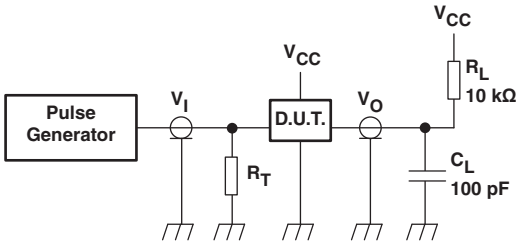


Figure 3. Input-Output Offset Voltage vs Pull-up Resister

6 Parameter Measurement Information



R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generators.

Figure 4. Test Circuitry for Switching Times

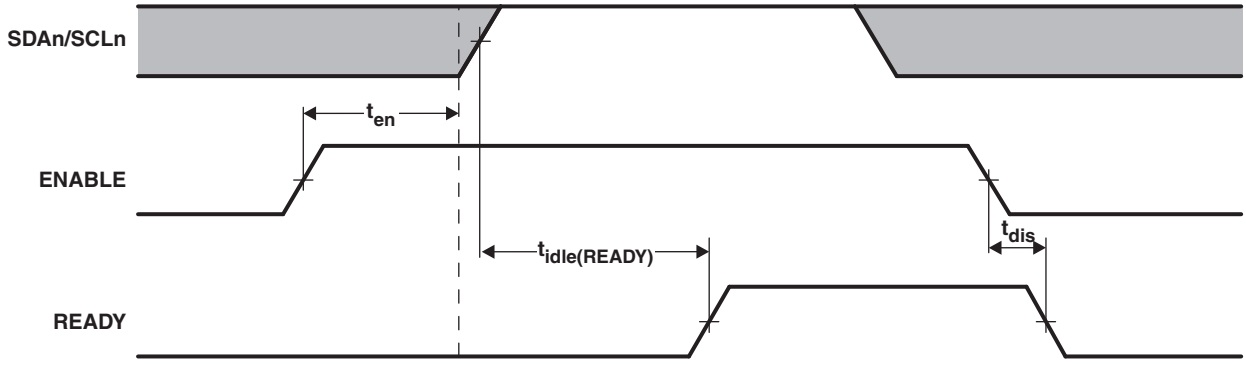


Figure 5. Timing for t_{en}, $t_{idle(READY)}$, and t_{dis}

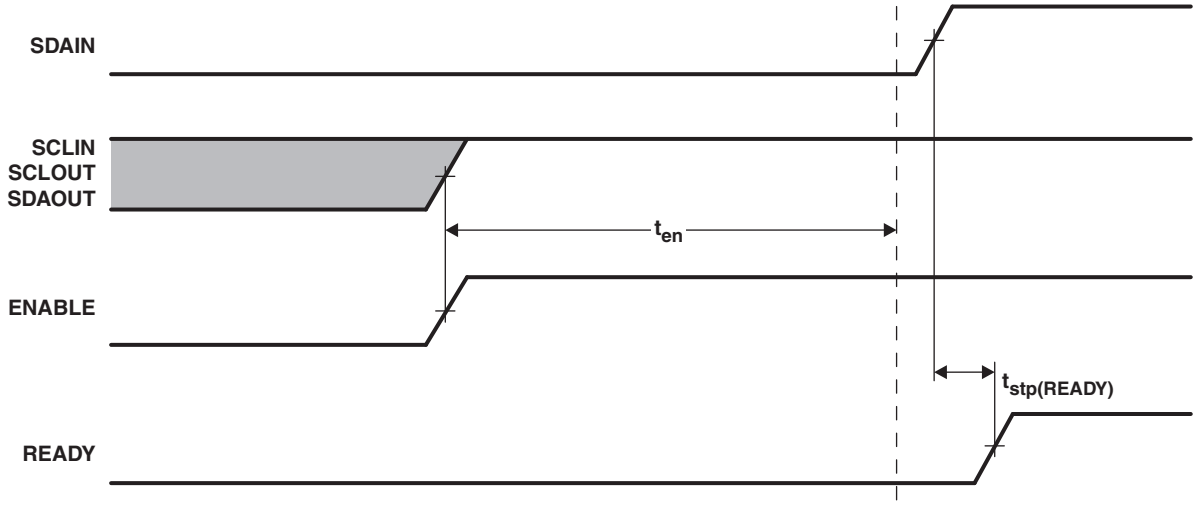


Figure 6. $t_{stp(READY)}$ That Can Occur After t_{en}

Parameter Measurement Information (continued)

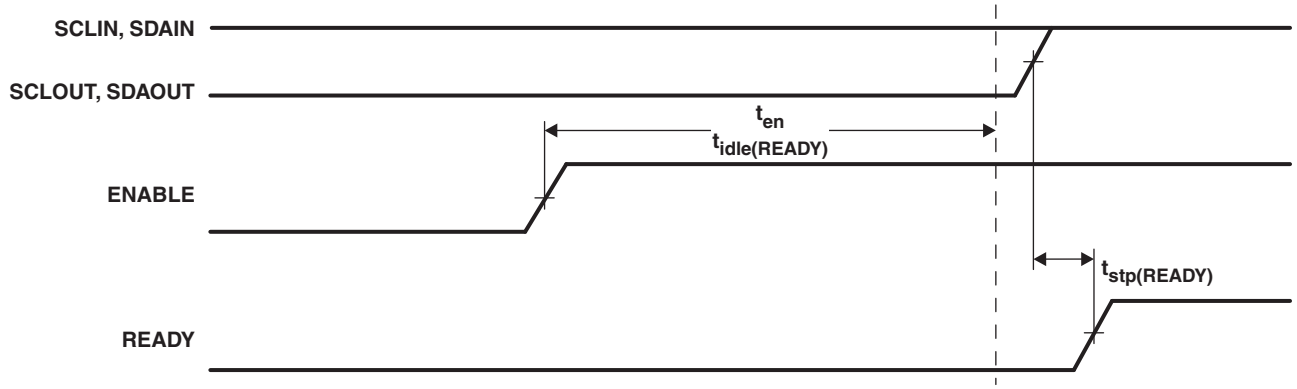
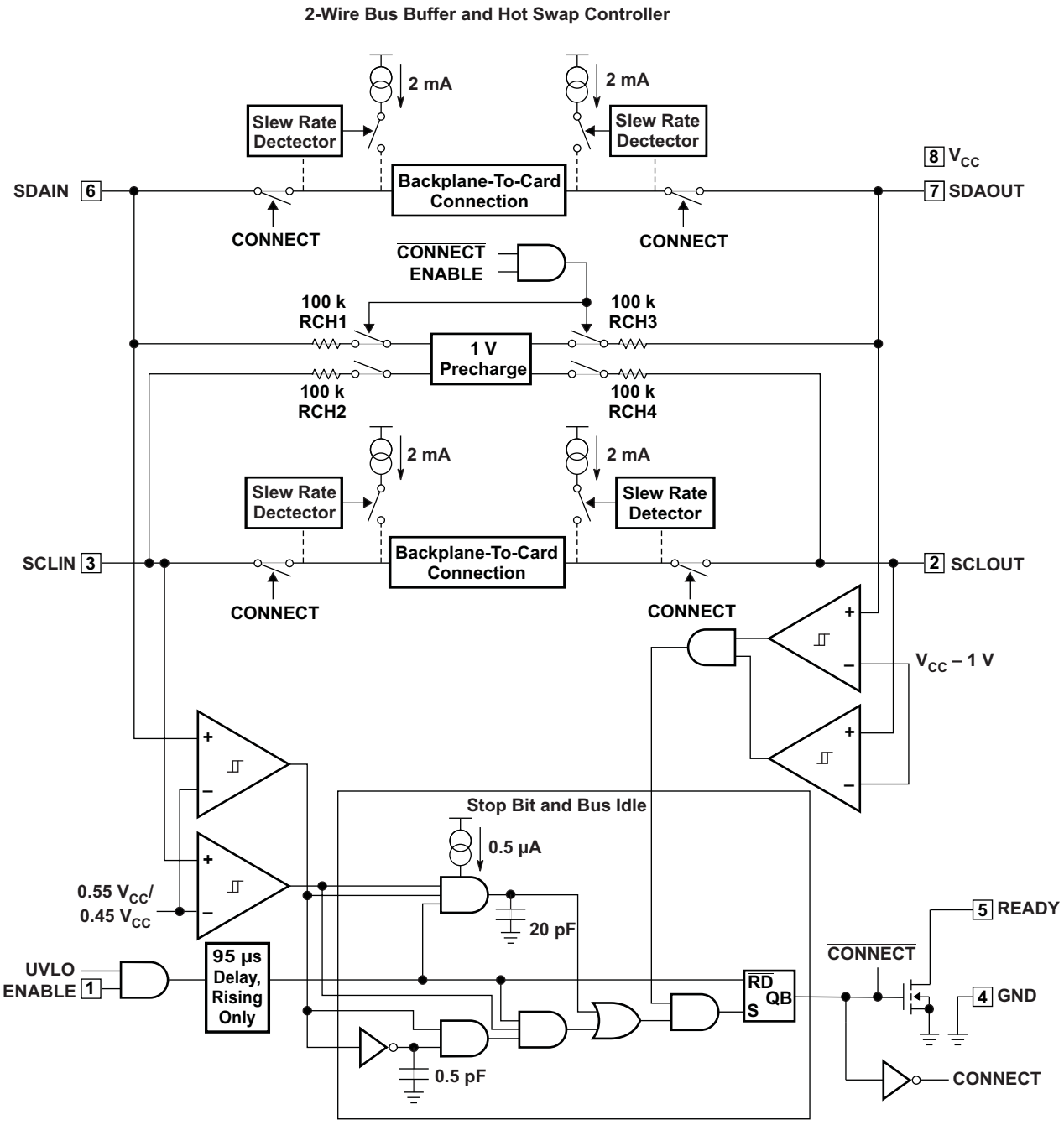


Figure 7. $t_{stp(READY)}$ That Can Occur After t_{en} and $t_{idle(READY)}$

7 Detailed Description

7.1 Functional Block Diagram



7.2 Feature Description

7.2.1 Rise-Time Accelerators

Once connection has been established, rise-time accelerator circuits on all four SDA and SCL pins are activated. These allow the user to choose weaker DC pullup currents on the bus, reducing power consumption while still meeting system rise-time requirements. During positive bus transitions, the TCA4311 switches in 2 mA (typical) of current to quickly slew the SDA and SCL lines once their DC voltages exceed 0.6 V. Using a general rule of 20 pF of capacitance for every device on the bus (10 pF for the device and 10 pF for interconnect), choose a pullup current so that the bus will rise on its own at a rate of at least 1.25 V/µs to guarantee activation of the accelerators.

For example, assume an SMBus system with V_{CC} = 3 V, a 10-kΩ pullup resistor and equivalent bus capacitance of 200 pF. The rise-time of an SMBus system is calculated from ($V_{IL(MAX)}$ – 0.15 V) to ($V_{IH(MIN)}$ + 0.15 V), or 0.65 V to 2.25 V. It takes an RC circuit 0.92 time constants to traverse this voltage for a 3 V supply; in this case, 0.92 × (10 kΩ × 200 pF) = 1.84 µs. Thus, the system exceeds the maximum allowed rise-time of 1 µs by 84%. However, using the rise-time accelerators, which are activated at a DC threshold of below 0.65 V, the worst-case rise-time is: (2.25 V – 0.65 V) × 200 pF/1 mA = 320 ns, which meets the 1 µs rise-time requirement.

7.2.2 READY Digital Output

This pin provides a digital flag which is low when either EN is low or the start-up sequence described earlier in this section has not been completed. READY goes high when EN is high and start-up is complete. The pin is driven by an open drain pull-down capable of sinking 3 mA while holding 0.4 V on the pin. Connect a resistor of 10 kΩ to V_{CC} to provide the pullup.

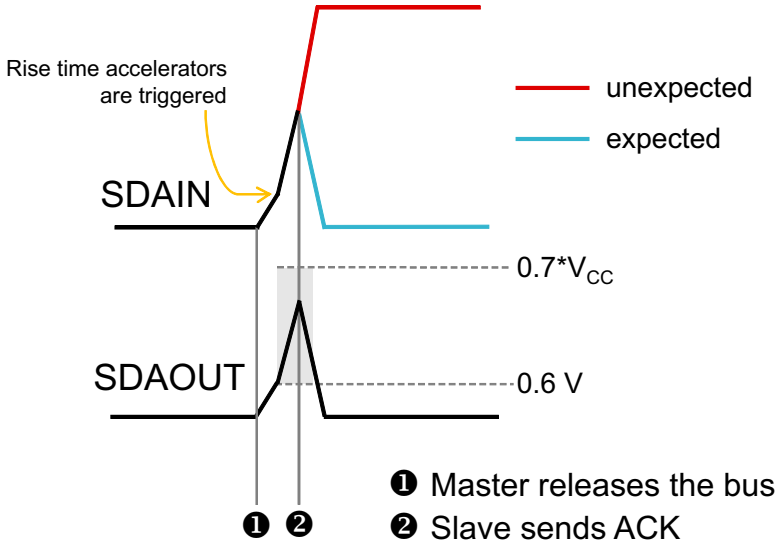
7.2.3 EN Low Current Disable

Grounding the EN pin disconnects the backplane side from the card side, disables the rise-time accelerators, drives READY low, disables the bus precharge circuitry and puts the part in a near-zero current state. When the pin voltage is driven all the way to V_{CC}, the part waits for data transactions on both the backplane and card sides to be complete (as described in the Start-Up section) before reconnecting the two sides.

7.2.4 Missing ACK Errata

Description

- When the slave (or master) device sends an ACK bit, a logic low on SDA during the 9th clock cycle, the slave (or master) may pull the SDA line low while the rise time accelerators are engaged, and the master (or slave) side will stay high.
- The rise time accelerators will be engaged when the voltage is above 0.6 V (typical), and below V_{IH}, 0.7*VCC
- In the example described below, SDAOUT is a slave attempting to send an ACK bit. SDAOUT pulls to a logic low but the ACK is not transferred to the other side and SDAIN will remain high unexpectedly.



Feature Description (continued)

System Impact

The ACK bit will not be transferred through the TCA4311, and the slave or master device will interpret the result as a NACK.

System Workaround

Usage of the TCA4311A is recommended.

7.3 Device Functional Modes

7.3.1 Start-Up

When the TCA4311 first receives power on its V_{CC} pin, either during power-up or during live insertion, it starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until V_{CC} rises above 2.5 V.

During this time, the 1 V precharge circuitry is also active and forces 1 V through 100-kΩ nominal resistors to the SDA and SCL pins. Because the I/O card is being plugged into a live backplane, the voltage on the backplane SDA and SCL busses may be anywhere between 0 V and V_{CC}. Precharging the SCL and SDA pins to 1 V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing the amount of disturbance caused by the I/O card.

Once the TCA4311 comes out of UVLO, it assumes that SDAIN and SCLIN have been inserted into a live system and that SDAOUT and SCLOUT are being powered up at the same time as itself. Therefore, it looks for either a stop bit or bus idle condition on the backplane side to indicate the completion of a data transaction. When either one occurs, the part also verifies that both the SDAOUT and SCLOUT voltages are high. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane, and the rise time accelerators are enabled.

7.3.2 Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. For proper operation, logic low input voltages should be no higher than 0.4 V with respect to the ground pin voltage of the TCA4311. SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT release high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock synchronization, arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the TCA4311.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and card capacitances isolated. Because of this isolation, the waveforms on the backplane busses look slightly different than the corresponding card bus waveforms, as described here.

8 Application and Implementation

8.1 Typical Application

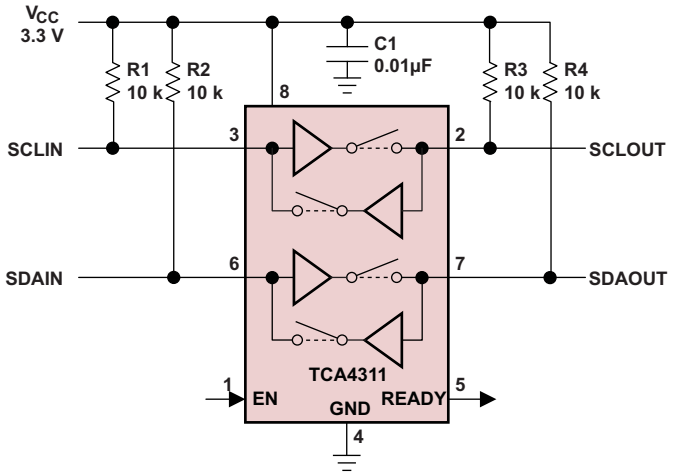


Figure 8. TCA4311 Typical Application

8.1.1 Live Insertion and Capacitance Buffering Application

Figure 9 through Figure 10 illustrate the usage of the TCA4311 in applications that take advantage of both its hot swap controlling and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing a TCA4311 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the TCA4311 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the TCA4311, which is less than 10 pF.

Figure 9 shows the TCA4311 in a CompactPCI™ configuration. Connect V_{CC} and EN to the output of one of the CompactPCI power supply Hot Swap circuits. Use a pullup resistor to EN for a card side enable/disable.

V_{CC} is monitored by a filtered UVLO circuit. With the V_{CC} voltage powering up after all other pins have established connection, the UVLO circuit ensures that the backplane and card data and clock busses are not connected until the transients associated with live insertion have settled. Owing to their small capacitance, the SDAIN and SCLIN pins cause minimal disturbance on the backplane busses when they make contact with the connector.

Figure 10 shows the TCA4311 in a PCI application, where all of the pins have the same length. In this case, connect an RC series circuit on the I/O card between V_{CC} and EN. An RC product of 10 ms provides a filter to prevent the TCA4311 from becoming activated until the transients associated with live insertion have settled.

Typical Application (continued)

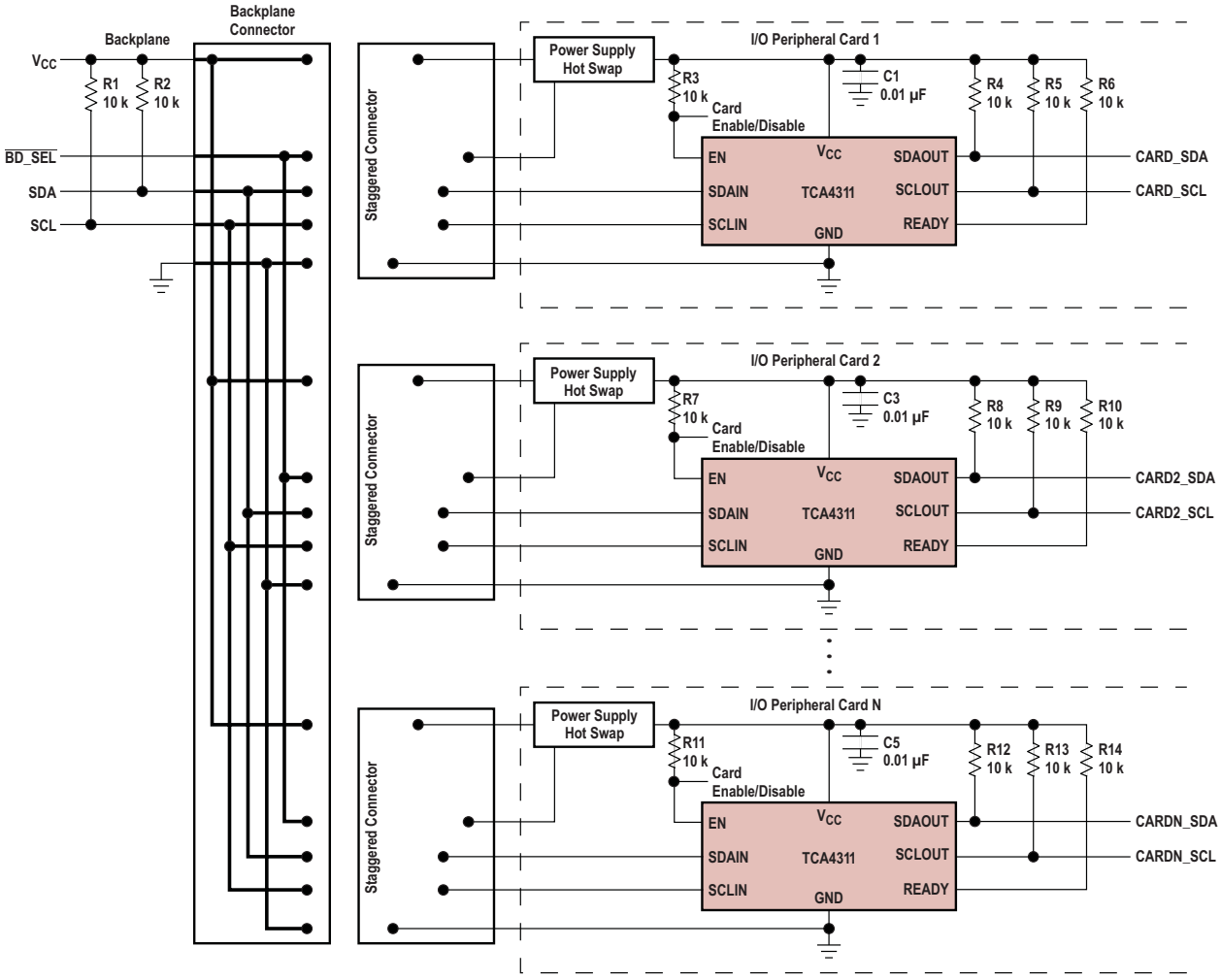


Figure 9. Inserting Multiple I/O Cards into a Live Backplane Using the TCA4311 in a CompactPCI System

Typical Application (continued)

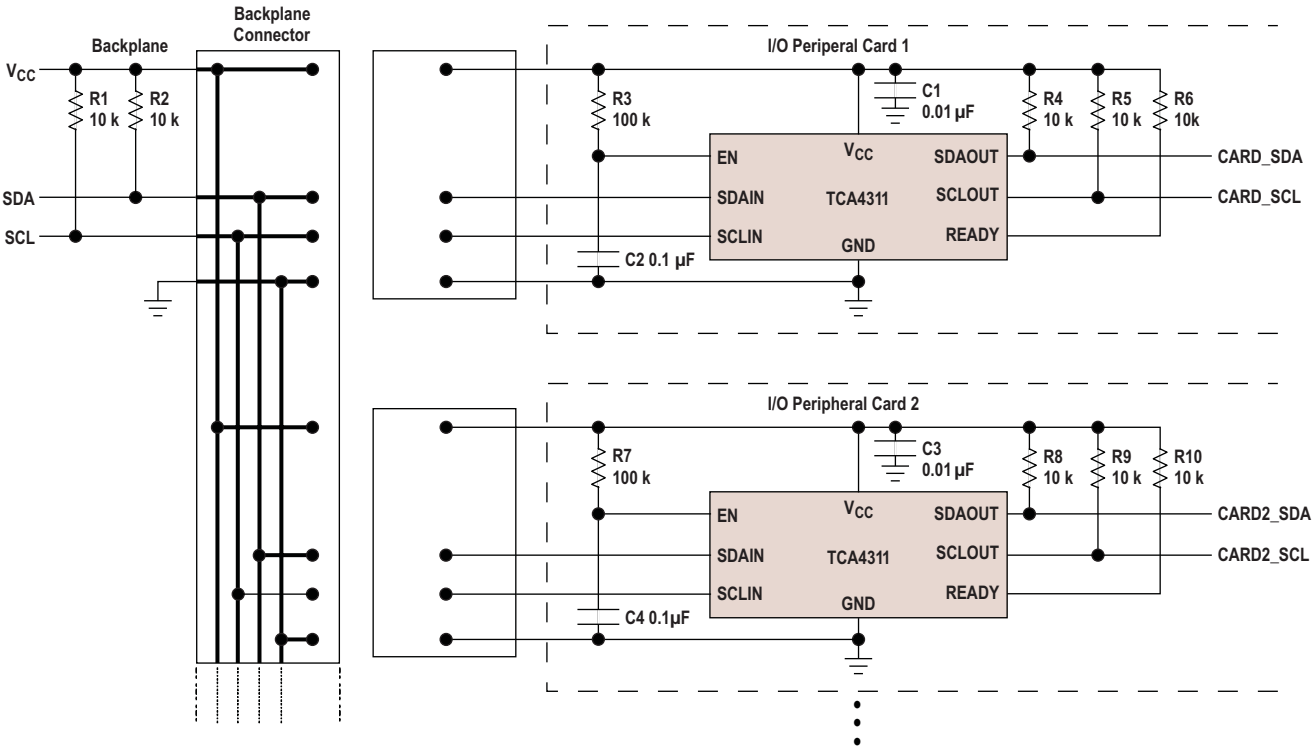


Figure 10. Inserting Multiple I/O Cards into a Live Backplane Using the TCA4311 in a PCI System

8.1.2 Repeater/Bus Extender Application

Users who wish to connect two 2-wire systems separated by a distance can do so by connecting two TCA4311 back-to-back, as shown in Figure 11. The I^2C specification allows for 400 pF maximum bus capacitance, severely limiting the length of the bus. The SMBus specification places no restriction on bus capacitance, but the limited impedances of devices connected to the bus require systems to remain small if rise- and fall-time specifications are to be met. The strong pullup and pulldown impedances of the TCA4311 are capable of meeting rise- and fall-time specifications for one nanofarad of capacitance, thus allowing much more interconnect distance. In this situation, the differential ground voltage between the two systems may limit the allowed distance, because a valid logic low voltage with respect to the ground at one end of the system may violate the allowed V_{OL} specification with respect to the ground at the other end. In addition, the connection circuitry offset voltages of the back-to-back TCA4311 add together, directly contributing to the same problem.

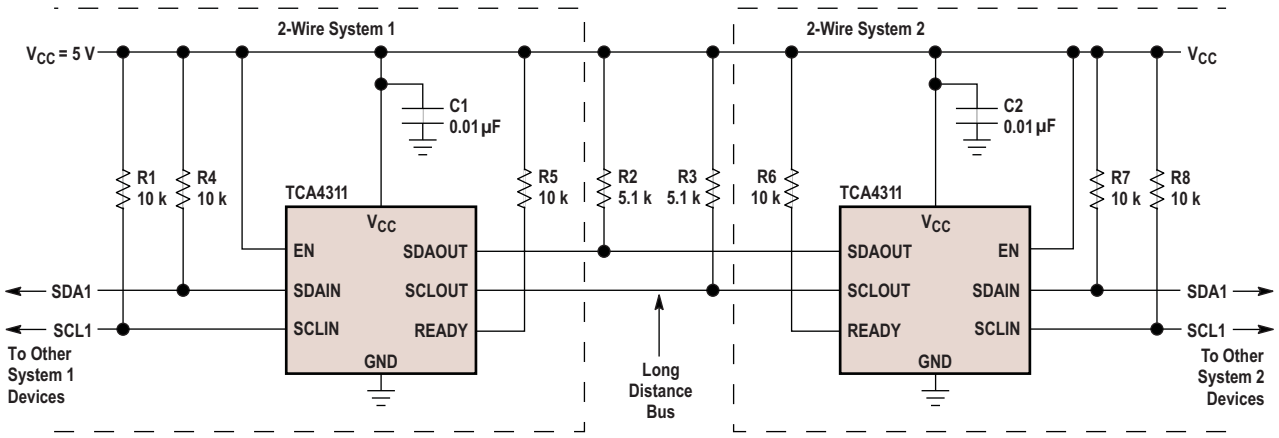


Figure 11. Repeater/Bus Extender Application

Typical Application (continued)

8.1.3 Systems With Disparate Supply Voltages

In large 2-wire systems, the V_{CC} voltages seen by devices at various points in the system can differ by a few hundred millivolts or more. This situation is well modeled by a series resistor in the V_{CC} line, as shown in Figure 12. For proper operation of the TCA4311, make sure that $V_{CC(BUS)} \geq V_{CC(TCA4311)} - 0.5$ V.

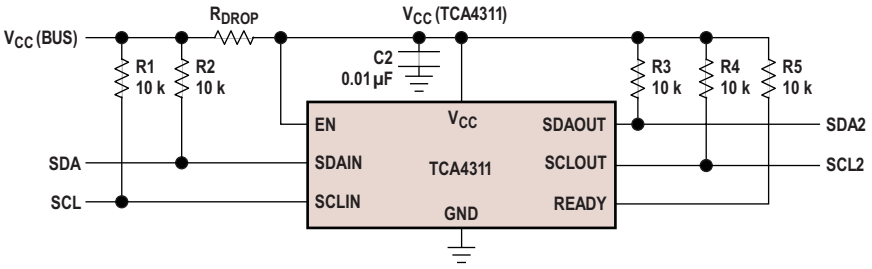


Figure 12. System With Disparate V_{CC} Voltages

8.1.4 Design Requirements

8.1.4.1 Input to Output Offset Voltage

When a logic low voltage, V_{LOW1}, is driven on any of the TCA4311's data or clock pins, the TCA4311 regulates the voltage on the other side of the chip (call it V_{LOW2}) to a slightly higher voltage, as directed by the following equation:

$$V_{LOW2} = V_{LOW1} + 75\ mV + (V_{CC}/R) \times 100$$

where R is the bus pullup resistance in ohms (Ω). For example, if a device is forcing SDAOUT to 10 mV where V_{CC} = 3.3 V and the pullup resistor R on SDAIN is 10 kΩ, then the voltage on SDAIN = 10 + 75 + (3.3/10000) × 100 = 118 mV. See the *Typical Characteristics* section for curves showing the offset voltage as a function of V_{CC} and R.

8.1.4.2 Propagation Delays

During a rising edge, the rise-time on each side is determined by the combined pullup current of the TCA4311 boost current and the bus resistor and the equivalent capacitance on the line. If the pullup currents are the same, a difference in rise-time occurs which is directly proportional to the difference in capacitance between the two sides. This effect is displayed in Figure 13 for V_{CC} = 3.3 V and a 10-kΩ pullup resistor on each side (50 pF on one side and 150 pF on the other). Since the output side has less capacitance than the input, it rises faster and the effective t_{PLH} is negative.

There is a finite propagation delay, t_{PHL}, through the connection circuitry for falling waveforms. Figure 14 shows the falling edge waveforms for the same V_{CC}, pullup resistors and equivalent capacitance conditions as used in Figure 13. An external NMOS device pulls down the voltage on the side with 150 pF capacitance; the TCA4311 pulls down the voltage on the opposite side, with a delay of 55 ns. This delay is always positive and is a function of supply voltage, temperature and the pullup resistors and equivalent bus capacitances on both sides of the bus. The *Typical Characteristics* section shows t_{PHL} as a function of temperature and voltage for 10-kΩ pullup resistors and 100 pF equivalent capacitance on both sides of the part. By comparison with Figure 14, the V_{CC} = 3.3 V curve shows that increasing the capacitance from 50 pF to 100 pF results in a t_{PHL} increase from 55 ns to 75 ns. Larger output capacitances translate to longer delays (up to 150 ns). Users must quantify the difference in propagation times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.

Typical Application (continued)

8.1.5 Detailed Design Procedure

8.1.5.1 Resistor Pull-Up Value Selection

The system pullup resistors must be strong enough to provide a positive slew rate of 1.25 V/µs on the SDA and SCL pins, in order to activate the boost pullup currents during rising edges. Choose maximum resistor value R using the formula:

$R \leq (V_{CC(MIN)} - 0.6)\ (800{,}000) / C$

where R is the pullup resistor value in ohms, $V_{CC(MIN)}$ is the minimum V_{CC} voltage and C is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose R ≤ 16 kΩ for V_{CC} = 5.5 V maximum, R ≤ 24 kΩ for V_{CC} = 3.6 V maximum. The start-up circuitry requires logic high voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pullup values are needed to overcome the precharge voltage.

8.1.6 Application Curves

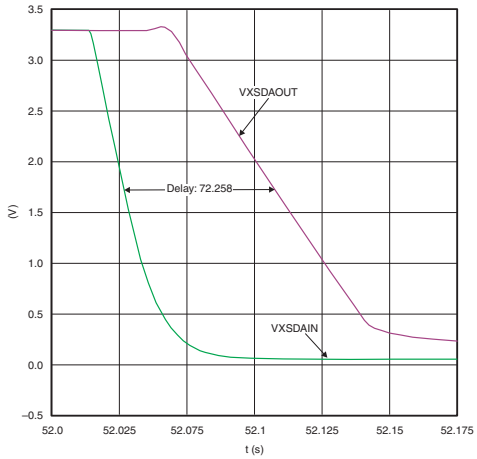


Figure 13. Input-Output Connection t_{PLH}

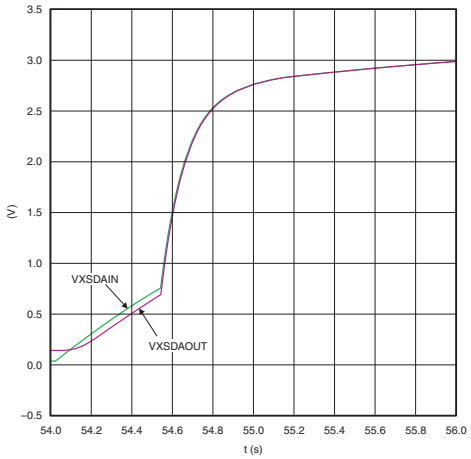


Figure 14. Input-Output Connection t_{PHL}

9 Device and Documentation Support

9.1 Trademarks

CompactPCI is a trademark of PCI Industrial Computer Manufacturers Group.
All other trademarks are the property of their respective owners.

9.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA4311DGKR	NRND	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3JS	
TCA4311DR	NRND	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PR311	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

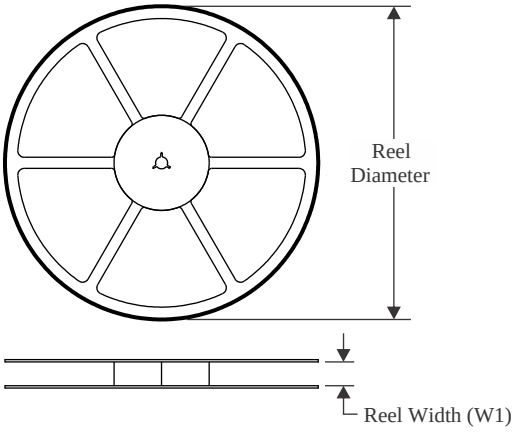
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

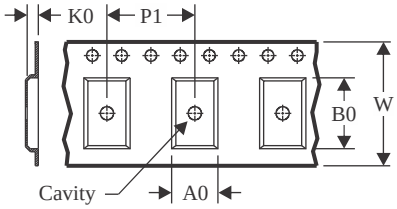
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

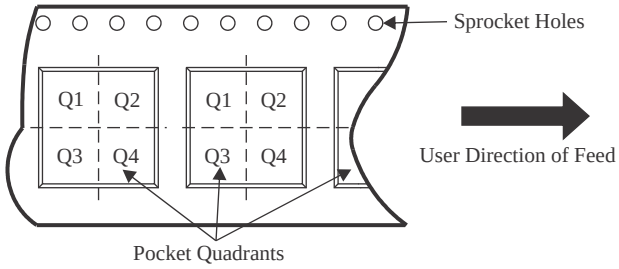


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

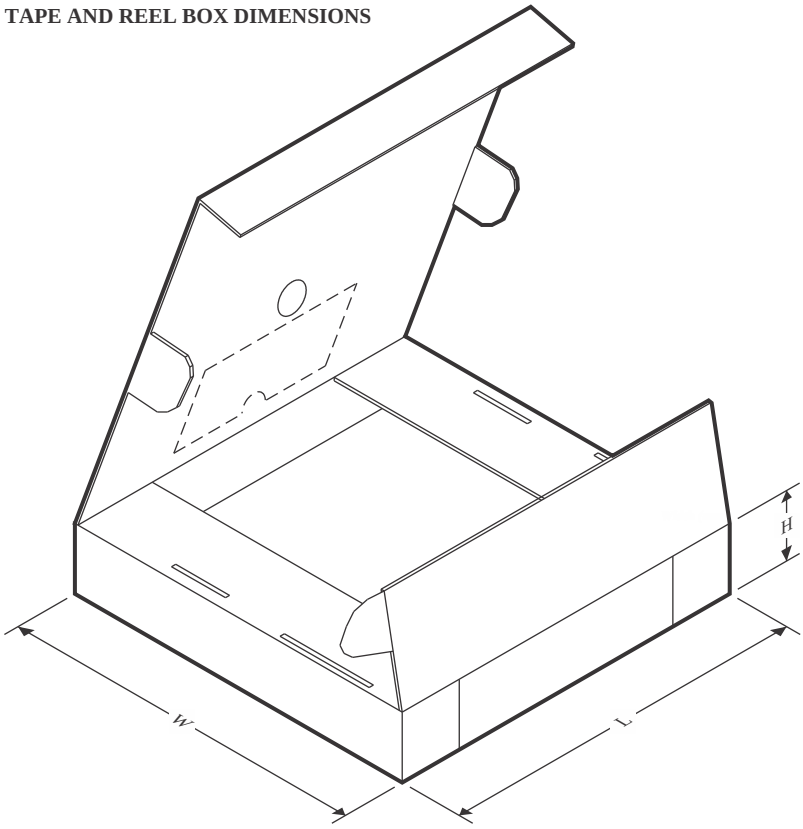
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

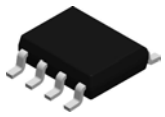
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA4311DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TCA4311DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA4311DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TCA4311DR	SOIC	D	8	2500	356.0	356.0	35.0

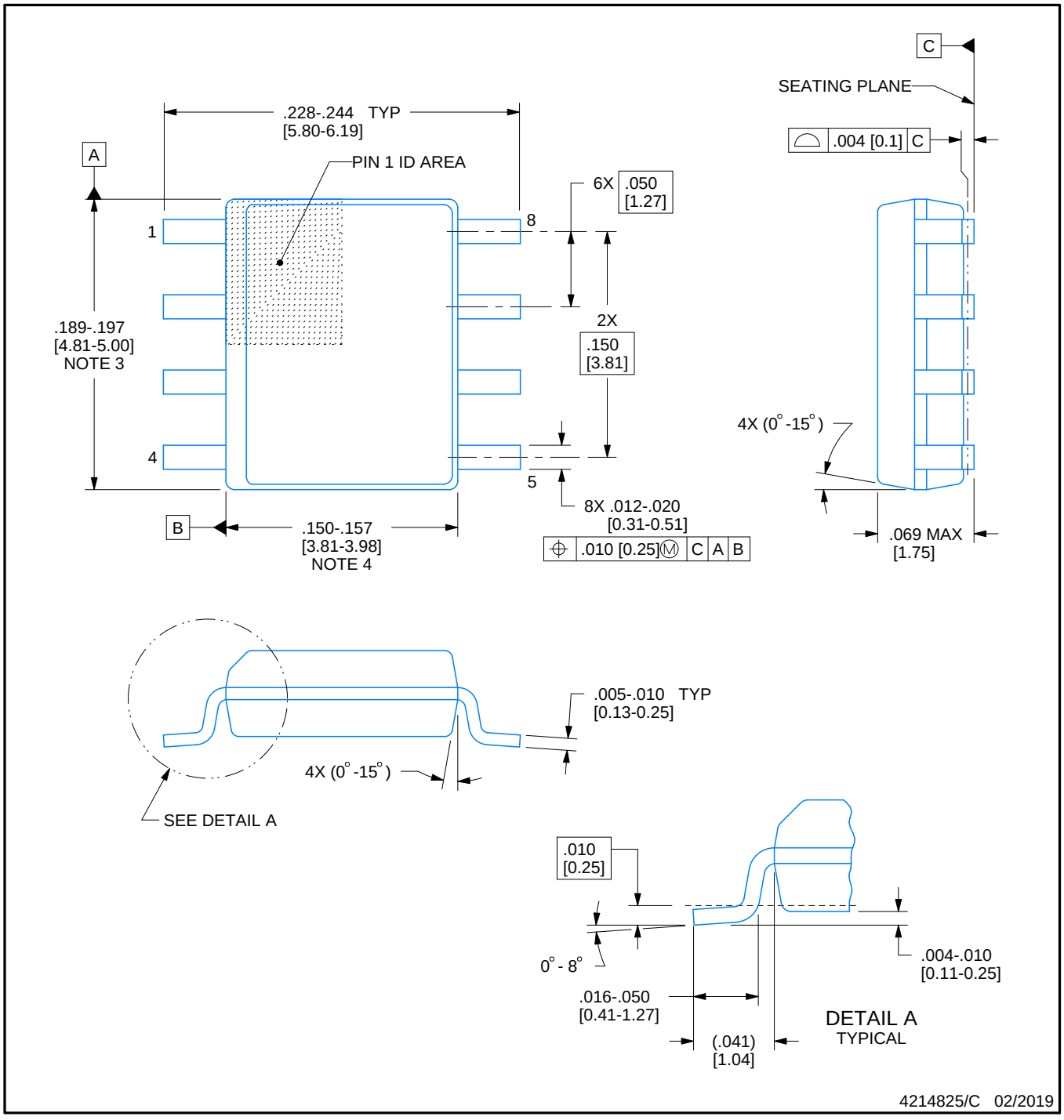


PACKAGE OUTLINE

D0008A

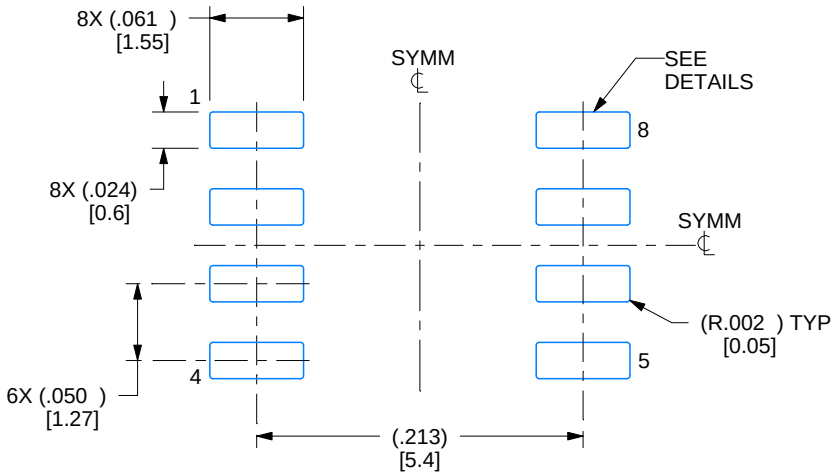
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

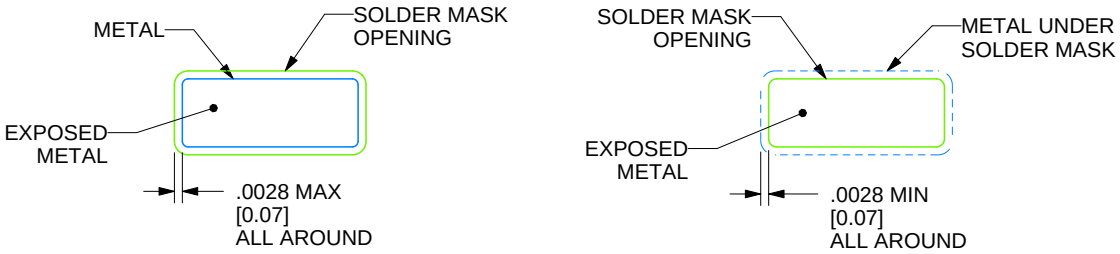


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

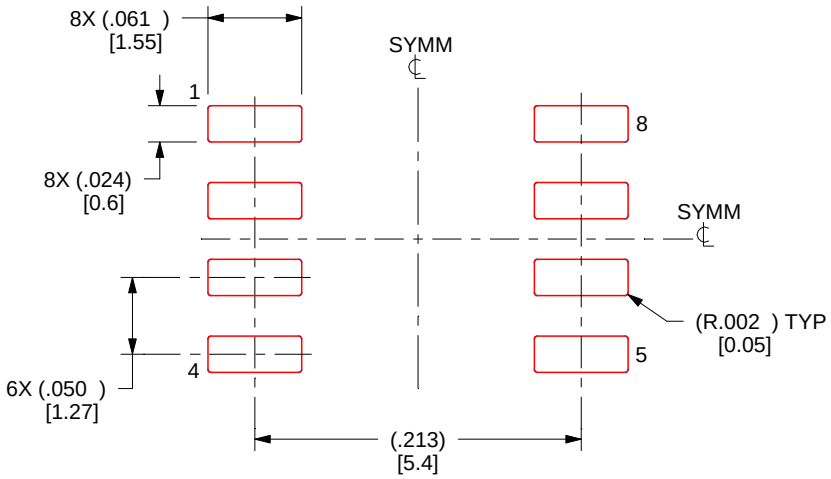
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



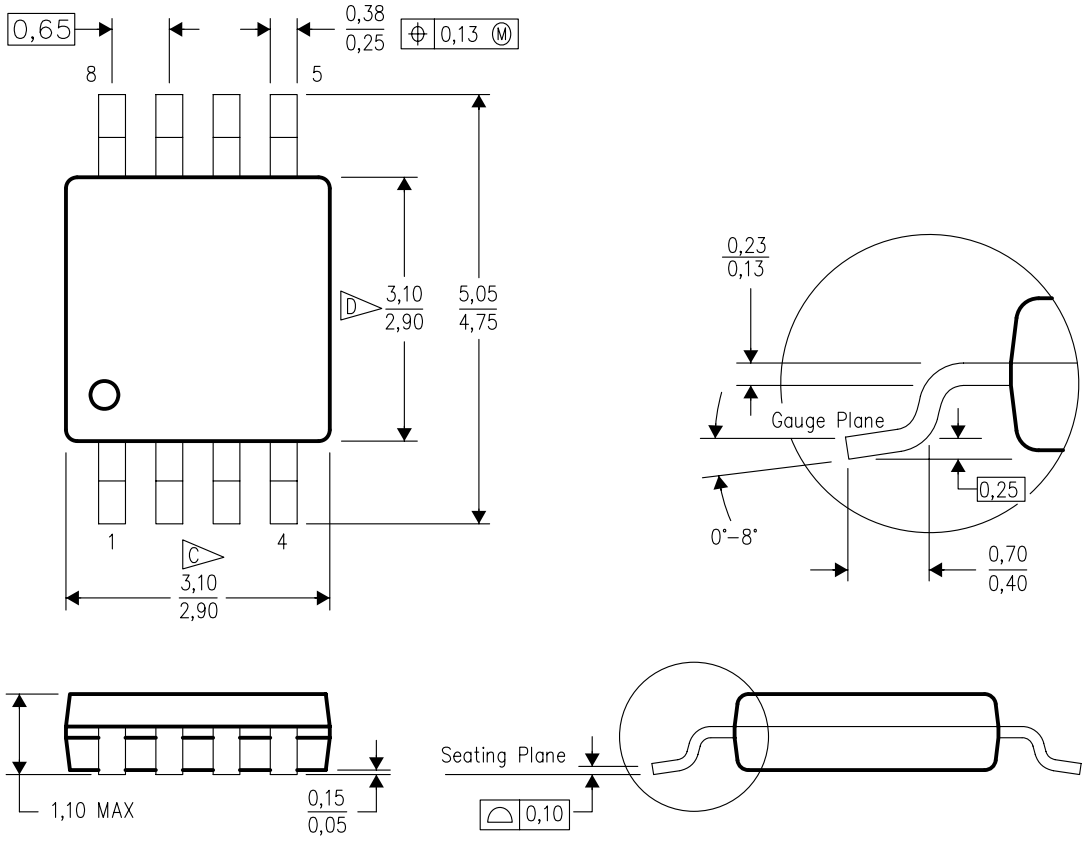
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

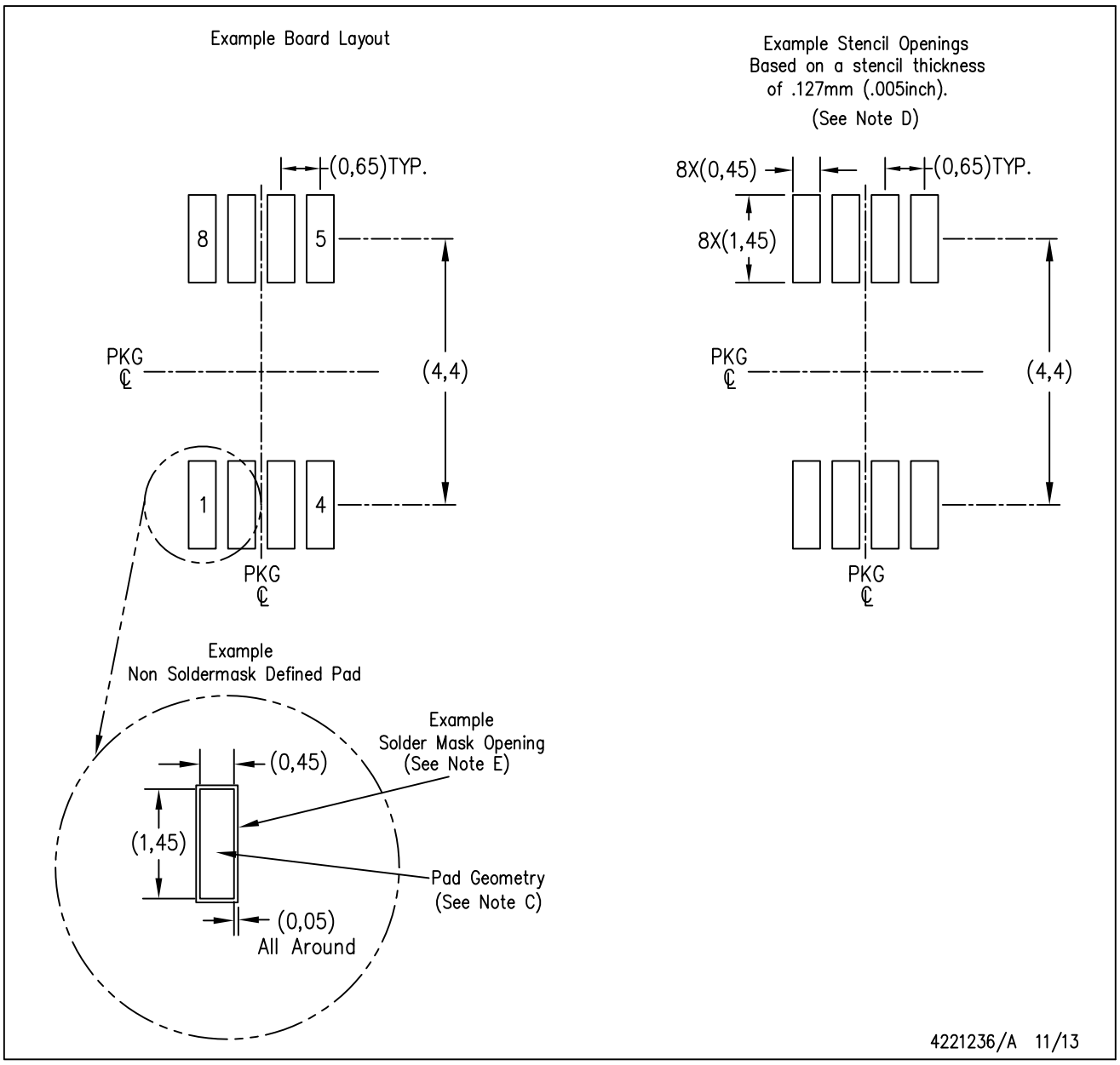
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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