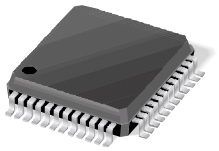


12-BIT, 80 MSPS CommsADC™ ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 80-MSPS Maximum Sample Rate
- 12-Bit Resolution
- No Missing Codes
- 360-mW Power Dissipation
- CMOS Technology
- On-Chip S/H
- 75 dB Spurious Free Dynamic Range at 100 MHz IF
- 1-GHz Bandwidth Differential Analog Input
- On-Chip References
- 2s Complement Digital Output
- 3.3-V Analog, 1.8-V Digital Supply
- 1.8 V–3.3 V I/O

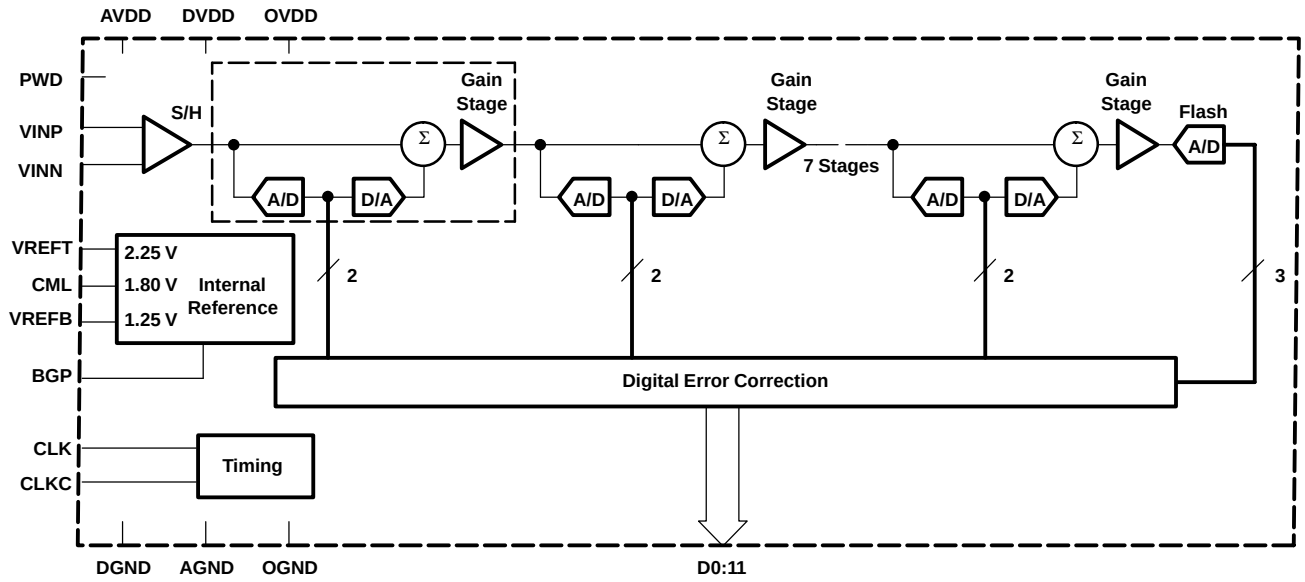
APPLICATIONS

- Cellular Base Transceiver Station Receive Channel
  - IF Sampling Applications
  - TDMA: GSM, IS-136, EDGE/UWC-136
  - CDMA: IS-95, UMTS, CDMA2000
  - Wireless Local Loop
  - LMDS, MMDS
  - Wideband Baseband Receivers
- Medical Imaging:
  - Ultrasound
  - Magnetic Resonant Imaging
- Portable Instrumentation

DESCRIPTION

The ADS5410 is a high-speed, high-performance pipelined analog-to-digital converter with exceptionally low-noise and high spurious-free dynamic range. The ADS5410 high input bandwidth makes it ideal for IF subsampling solutions where digital I/Q demodulators are used. Its high dynamic range makes it well suited for GSM, IS-95, UMTS, and IS-136 digital receivers. Its linearity and low DNL make it ideal for medical imaging applications. Low power consumption makes the ADS5410 ideal for applications in compact pico- and micro-base stations and in portable designs.

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

CommsADC is a trademark of Texas Instruments.

AVAILABLE OPTIONS

T_A	PACKAGE
	48–TQFP
–40°C to 85°C	ADS5410IPFB

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		ADS 5410
Supply voltage range	AVDD	–0.3 V to 4 V
	DVDD	–0.3 V to 2.3 V
	OVDD	–0.3 V to 3.6 V
Voltage between	AGND and DGND	–0.3 to 0.3 V
	AVDD to DVDD	–3.3 V to 3.3 V
Digital input (2)		–0.3 V to AVDD + 0.3 V
Digital data output		–0.3 V to OVDD + 0.3 V
Clamp current for digital input or output		±20 mA
Operating free-air temperature range, T_A		–40°C to 85°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Measured with respect to AGND.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
SUPPLIES AND REFERENCES				
Operating free-air temperature, T_A	–40		85	°C
Analog supply voltage, $V_{(AVDD)}$	3	3.3	3.6	V
Digital supply voltage, $V_{(DVDD)}$	1.6	1.8	2	V
ANALOG INPUTS				
Output driver supply voltage, $V_{(OVDD)}$	1.6		3.6	V
Input common-mode voltage		CML(1)		V
Differential input voltage range		2		Vpp
CLOCK INPUTS CLK AND CLKC				
Sample rate, $f_{(S)}$	5		80	MHz
Differential input mode voltage input swing	0.4		3.3	V
Differential input common mode voltage		1.65		V
Single-ended mode high-level input voltage, $V_{IH(S)}$	2			V
Single-ended mode low-level input voltage, $V_{IL(S)}$			0.8	V
Clock pulse width high, $t_{W(H)}$	5.625	6.25		ns
Clock pulse width low, $t_{W(L)}$	5.625	6.25		ns

(1) See references section in DC ELECTRICAL CHARACTERISTICS table.

DC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, clock frequency = 80 MSPS, 50% clock duty cycle (AVDD = 3.3 V, DVDD = 1.8 V, OVDD = 1.8 V) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Accuracy(1)						
	No missing codes	Fs = 88 MSPS(2)		Assured		
DNL	Differential nonlinearity		–0.9	±0.5	1	LSB
INL	Integral nonlinearity		–2	±1.5	2	LSB
E_O	Offset error			3		mV
E_G	Gain error			0.5		%FS
Power Supply						
$I_{(AVDD)}$	Analog supply current	Fs = 80 MSPS, A_I = FS, f_i = 2 MHz		105		mA
$I_{(DVDD)}$	Digital supply current			1		
$I_{(OVDD)}$	Digital output driver supply current			3.5		
	Power dissipation			360	450	mW
	Power down dissipation	PWDN = high		30	45	mW
PSRR	Power supply rejection ratio			±0.3		mV/V
References						
$V_{ref(VREFB)}$	Reference bottom		1.1	1.25	1.4	V
$V_{ref(VREFT)}$	Reference top		2.1	2.25	2.4	V
	$V_{REFT} – V_{REFB}$			1.06		V
	$V_{REFT} – V_{REFB}$ variation (6σ)			0.06		V
$V_{OC(CML)}$	Common mode output voltage			1.8		V
Digital Inputs (PWD)						
I_{IH}	High-level input current	V_i = 1.6 V	–10		10	µA
I_{IL}	Low-level input current	V_i = 0.3 V	–10		10	µA
V_{IH}	High-level input voltage		1.8			V
V_{IL}	Low-level input voltage				0.8	V
Digital Outputs						
V_{OH}	High-level output voltage	I_{OH} = –50 µA	1.4			V
V_{OL}	Low-level output voltage	I_{OL} = 50 µA			0.4	V

(1) Fs = 80 MSPS, sinewave input, f_i = 2 MHz
(2) Speed margin test

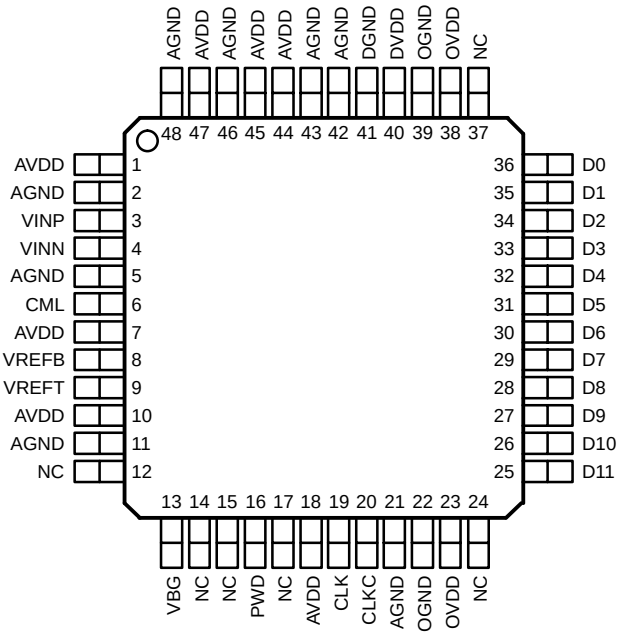
AC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, clock frequency = 80 MSPS, 50% clock duty cycle (AVDD = 3.3 V, DVDD = 1.8 V, OVDD = 1.8 V) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious free dynamic range, A_i = –1 dBFS (no exceptions)	f_i = 2.2 MHz		76		dBc
		f_i = 17.4 MHz	72	76		
		f_i = 31 MHz		76		
		f_i = 70 MHz		72		
		f_i = 150 MHz		70		
HD3	Third order harmonic, A_i = –1 dBFS	f_i = 2.2 MHz		84		dBc
		f_i = 17.4 MHz		84		
		f_i = 31 MHz		86		
		f_i = 70 MHz		79		
		f_i = 150 MHz		70		
HD2	Second order harmonic, A_i = –1 dBFS	f_i = 2.2 MHz		81		dBc
		f_i = 17 MHz		80		
		f_i = 31 MHz		90		
		f_i = 70 MHz		88		
		f_i = 150 MHz		75		
SNR	Signal-to-noise ratio, A_i = –1 dBFS	f_i = 2.2 MHz		67		dB
		f_i = 17.4 MHz	63	66		
		f_i = 31 MHz		65		
		f_i = 70 MHz		62		
		f_i = 150 MHz		57		
SINAD	Signal-to-noise and distortion, A_i = –1 dBFS	f_i = 2.2 MHz		66		dB
		f_i = 17.4 MHz	62.5	65		
		f_i = 31 MHz		64		
		f_i = 70 MHz		61		
		f_i = 150 MHz		56		
	Two tone IMD rejection, $A_{1,2}$ = –7 dBFS	f_1 = 15.2 MHz, f_2 = 15.9 MHz		77		dBc
	Track mode bandwidth	–3 dB BW with –3dBFS input at low frequency		1		GHz

PIN ASSIGNMENTS

PFB PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AVDD	1, 7, 10, 18, 44, 45, 47	I	Analog power supply
AGND	2, 5, 11, 21, 42, 43, 46, 48	I	Analog ground
CLK	19	I	Clock input
CLKC	20	I	Complementary clock input
CML	6	O	Common-mode output voltage
D11–D0	25–36	O	Digital outputs, D11 is most significant data bit, D0 is least significant data bit.
DGND	41	I	Digital ground
DVDD	40	I	Digital power supply
NC	12, 14, 15, 17, 24, 37		No connection
OGND	22, 39	I	Digital driver ground
OVDD	23, 38	I	Digital driver power
PWD	16	I	Power down, active high
VBG	13	O	Bandgap voltage output
VINN	4	I	Complementary analog input
VINP	3	I	Analog input
VREFB	8	O	Reference bottom
VREFT	9	O	Reference top

TIMING DIAGRAMS

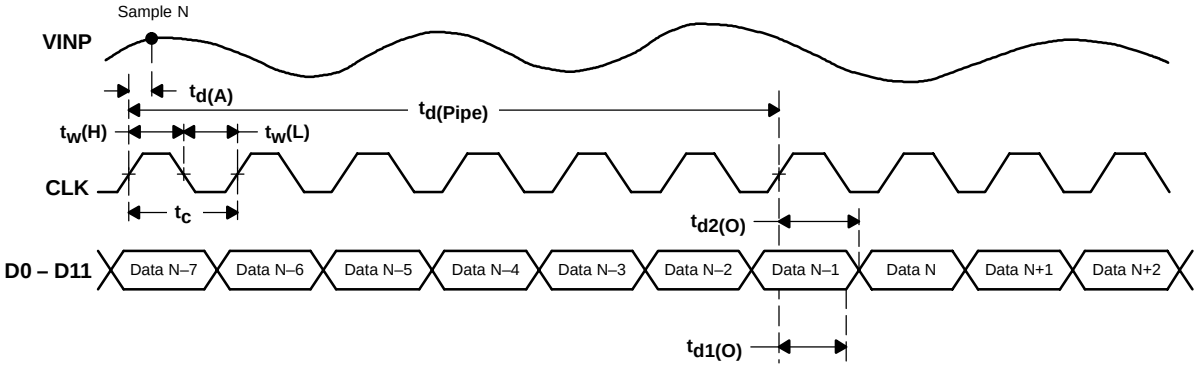


Figure 1. ADS5410 Timing Diagram

TIMING CHARACTERISTICS

		MIN	TYP	MAX	UNIT
$t_{d(A)}$	Aperture delay		2		ns
	Aperture jitter		1.5		ps
$t_{d1(O)}$	Output propagation delay (beginning of transition)		6		ns
$t_{d2(O)}$	Output propagation delay (data stable)		10		ns
$t_{d(Pipe)}$	Latency		6		Clock cycles

TYPICAL CHARACTERISTICS†

SPECTRAL PERFORMANCE

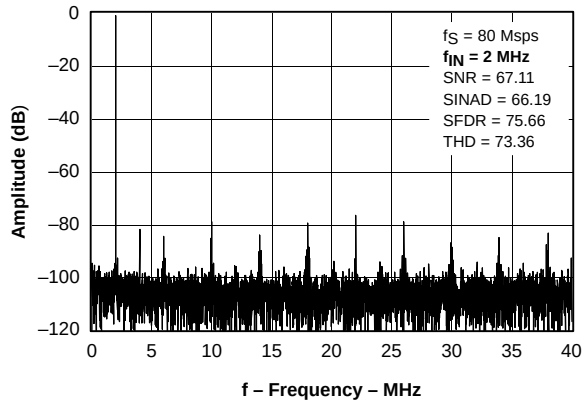


Figure 2

SPECTRAL PERFORMANCE

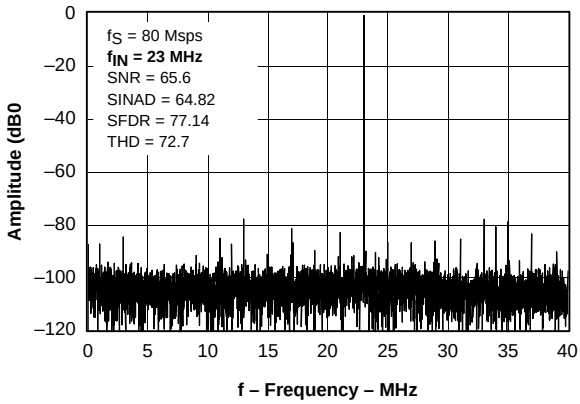


Figure 3

SPECTRAL PERFORMANCE

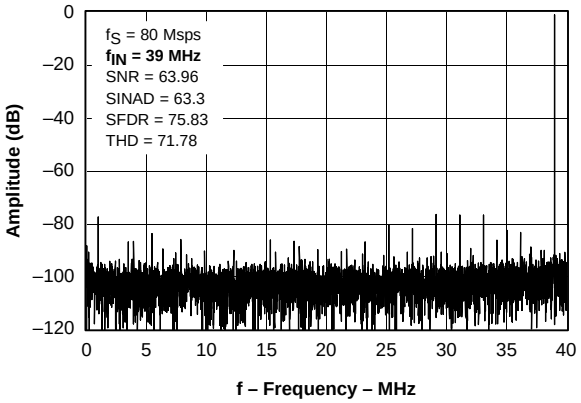


Figure 4

SPECTRAL PERFORMANCE

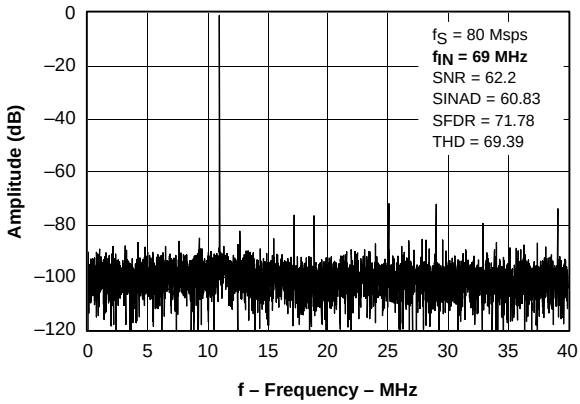


Figure 5

SPECTRAL PERFORMANCE

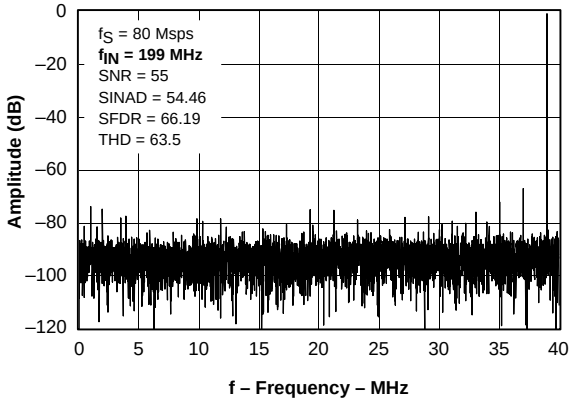


Figure 6

SPECTRAL PERFORMANCE

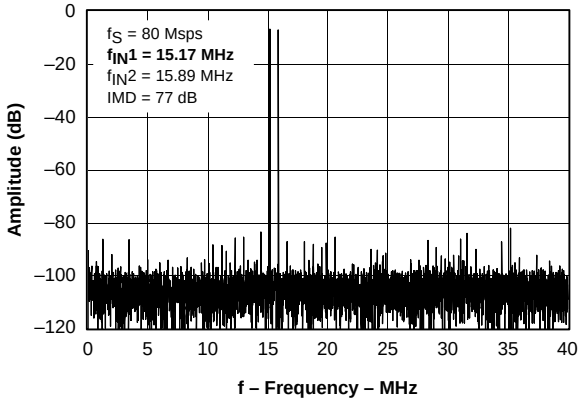


Figure 7

†50% duty cycle. AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, DV_{DD} = 1.8 V

TYPICAL CHARACTERISTICS†

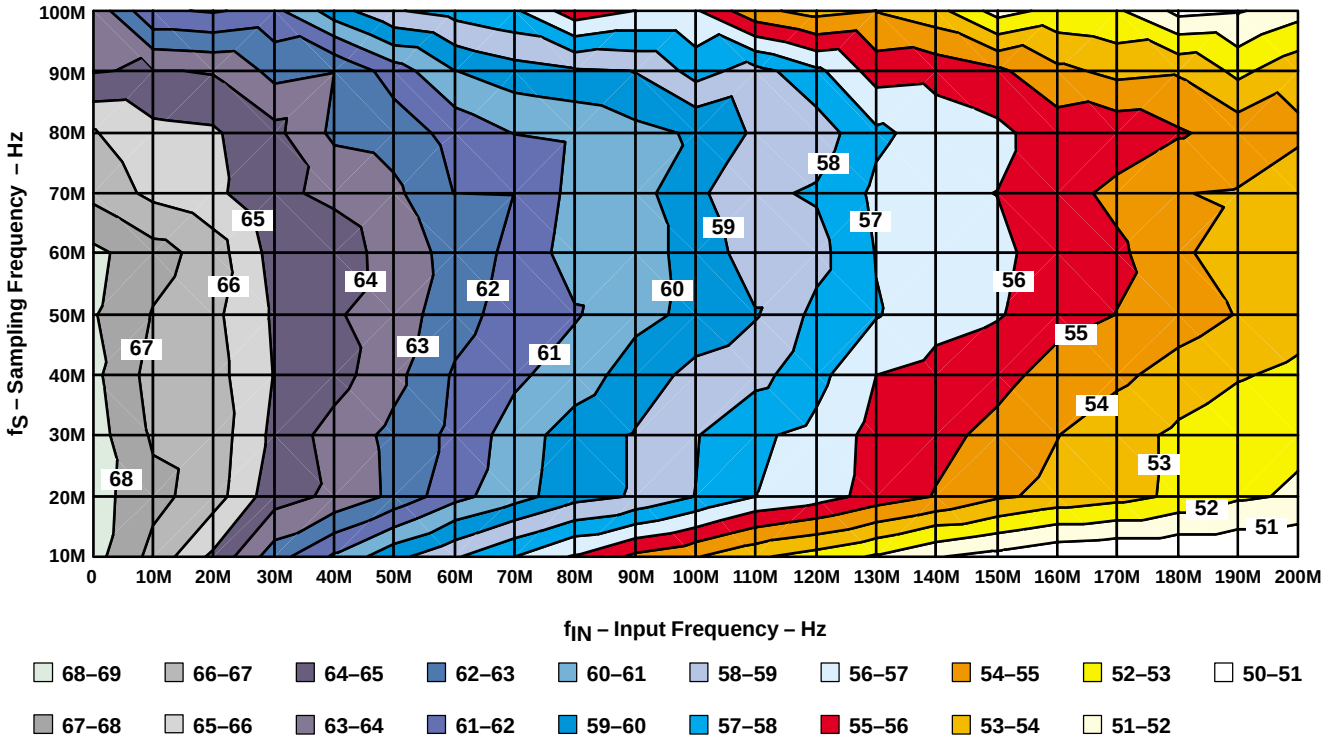


Figure 8. SINAD [dBFS]

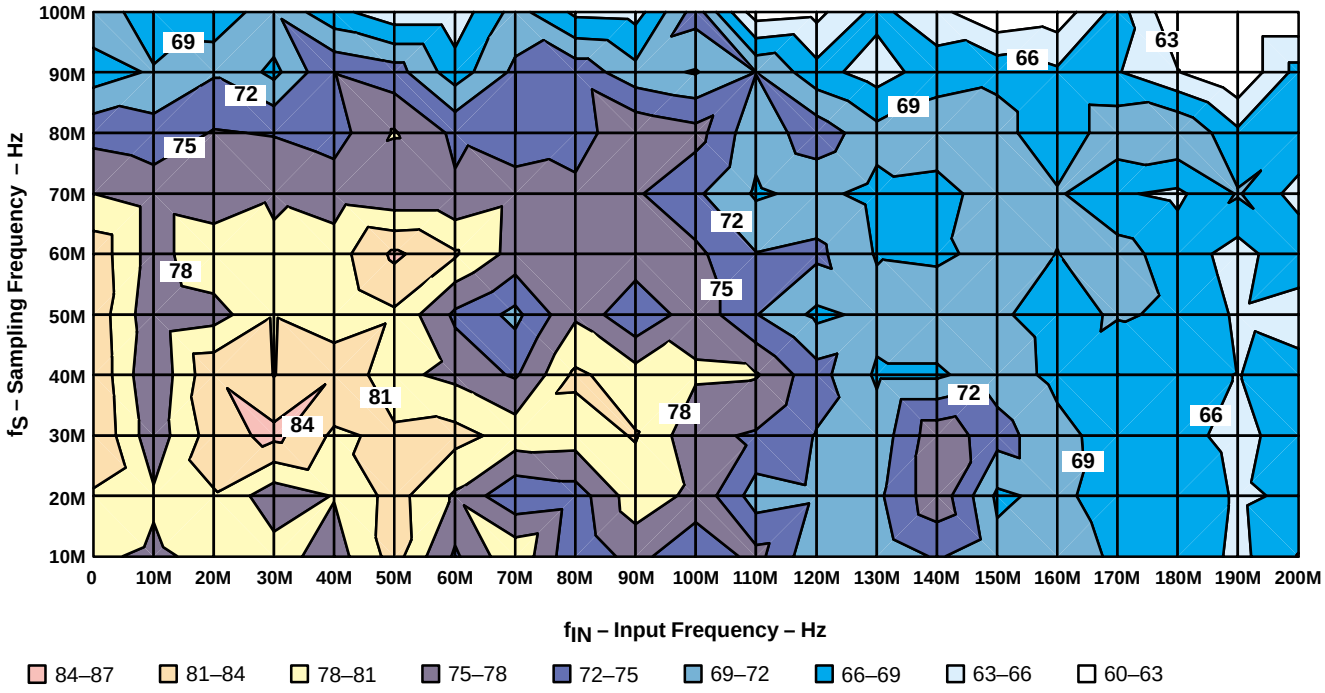


Figure 9. SFDR [dBc]

†50% duty cycle. AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, DV_{DD} = 1.8 V

TYPICAL CHARACTERISTICS†

AC PERFORMANCE vs INPUT POWER

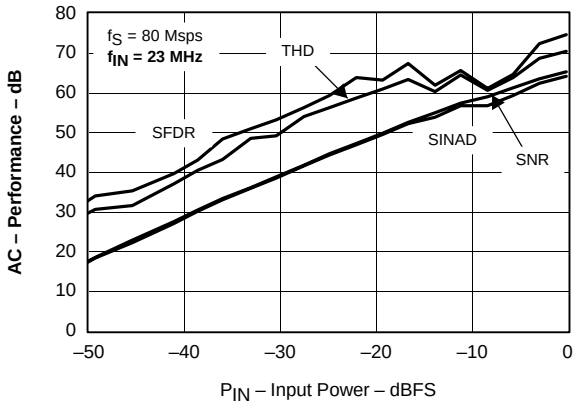


Figure 10

AC PERFORMANCE vs DUTY CYCLE

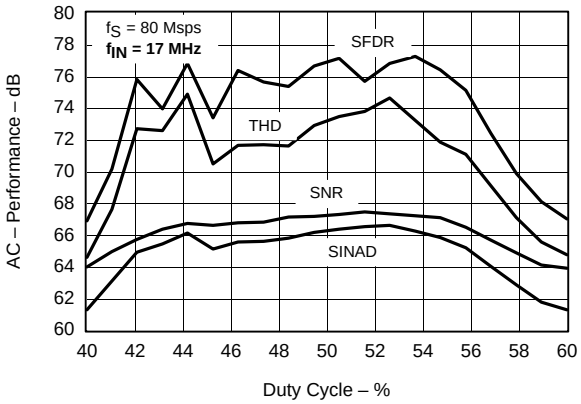
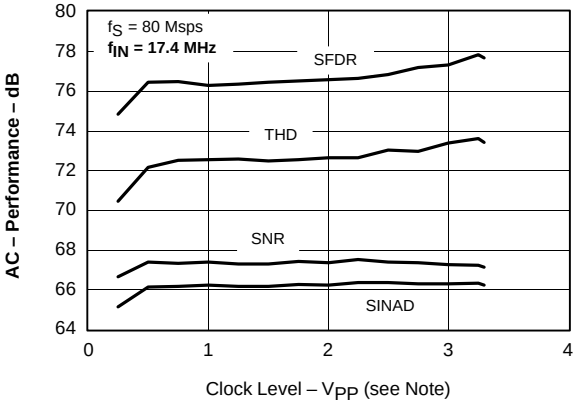


Figure 11

AC PERFORMANCE vs CLOCK LEVEL



NOTE: Voltage peak to peak in pin 19 or 20. Multiply by 2 to obtain differential peak to peak.

Figure 12

AC PERFORMANCE vs ANALOG SUPPLY VOLTAGE

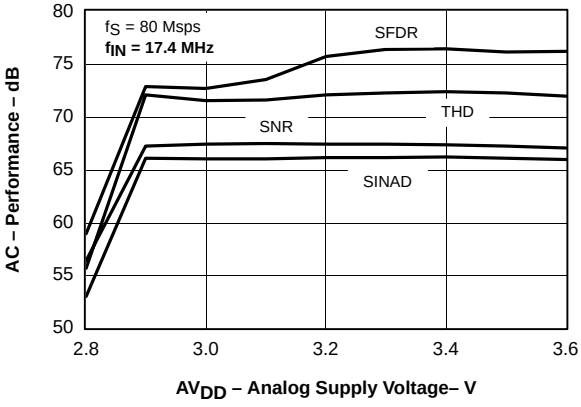


Figure 13

WCDMA SINGLE CARRIER MEASUREMENT

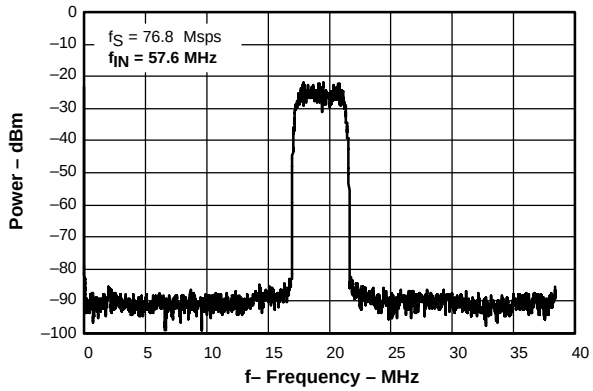


Figure 14

INPUT BANDWIDTH

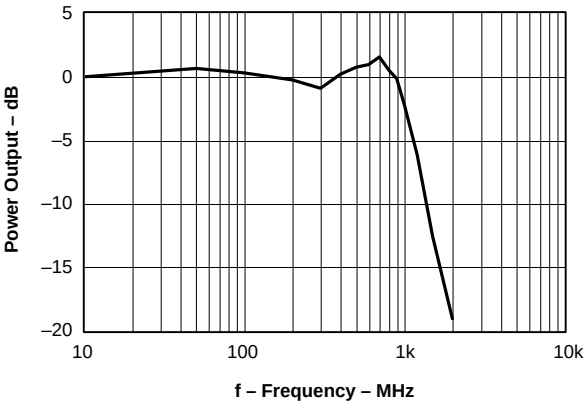


Figure 15

†50% duty cycle. AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, DV_{DD} = 1.8 V

TYPICAL CHARACTERISTICS†

DIFFERENTIAL NONLINEARITY

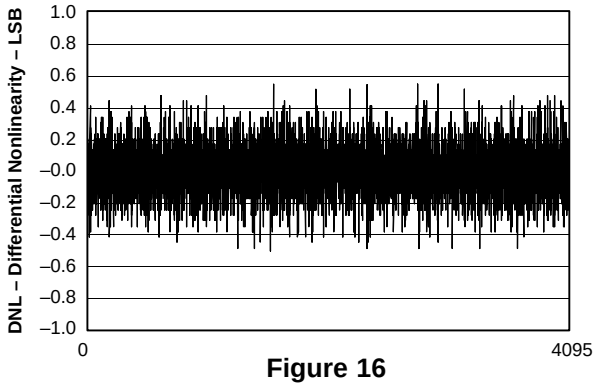


Figure 16

INTEGRAL NONLINEARITY

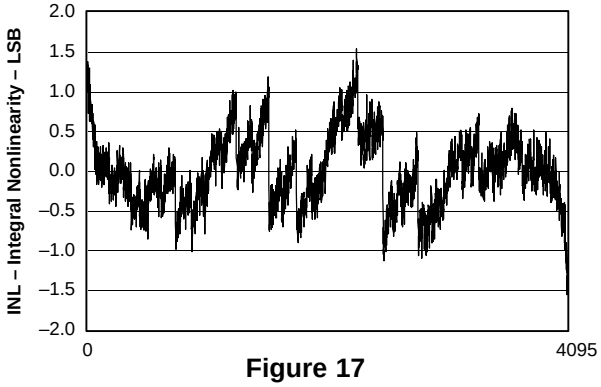


Figure 17

†50% duty cycle. AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, DV_{DD} = 1.8 V

EQUIVALENT CIRCUITS

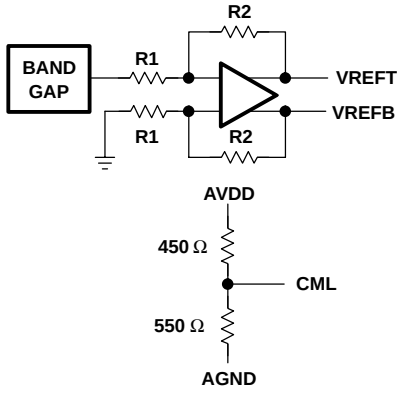


Figure 18. References

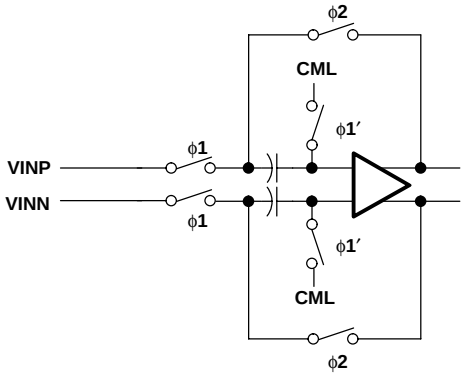


Figure 19. Analog Input Stage

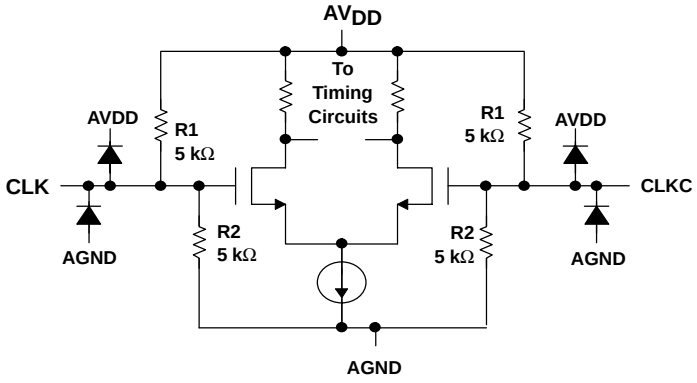


Figure 20. Clock Inputs

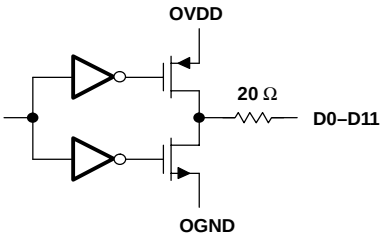


Figure 21. Digital Outputs

APPLICATION INFORMATION

CONVERTER OPERATION

The ADS5410 is a 12 bit ADC. Its low power (360 mW) at 80 Msps and high sampling rate is achieved using a state-of-the-art switched capacitor pipeline architecture built on an advanced low-voltage CMOS process. The ADS5410 analog core primarily operates from a 3.3-V supply consuming most of the power. The digital core operates from 1.8-V supply. A TPS76318 can be used to obtain the 1.8 V from the 3.3-V AVDD supply, if 1.8 V is not a supply already available in the design. For additional interfacing flexibility, the digital output supply (OV_{DD}) can be set from 1.6 V to 3.6 V. The ADC core consists of 10 pipeline stages and one flash ADC. Each of the stages produces 1.5 bits per stage. Both the rising and the falling clock edges are utilized to propagate the sample through the pipeline every half clock, for a total of six clock cycles.

ANALOG INPUTS

The analog input for the ADS5410 consists of a differential track-and-hold amplifier implemented using a switched capacitor technique, shown in Figure 19. This differential input topology, along with closely matched capacitors, produces a high level of ac-performance up to high sampling rates.

The ADS5410 requires each of the analog inputs (AIN+, AIN–) to be externally biased around the common mode level of the internal circuitry (CML, pin 6). After the connection of CML to the inputs, as shown in the diagrams below, the common mode level of the signal is between 1.6 V and 1.9 V depending on several factors, but this variation does not affect performance. For a full scale differential input, each of the differential lines of the input signal (pins 3 and 4) swings symmetrically between CML+0.5 V and CML–0.5 V. The maximum swing is determined by the two reference voltages, the top reference (REFT), and the bottom reference (REFB).

Although the inputs can be driven in single-ended configuration, the ADS5410 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 22 shows one possible configuration. The single ended signal is fed to the primary of an RF transformer. Since the input signal must be biased around the common mode voltage of the internal circuitry, the common mode (CML) reference from the ADS5410 is connected to the center-tap of the secondary. To ensure a steady low noise CML reference, the best performance is obtained when the CML output is connected to ground with a 0.1-μF and 0.01-μF low inductance capacitor.

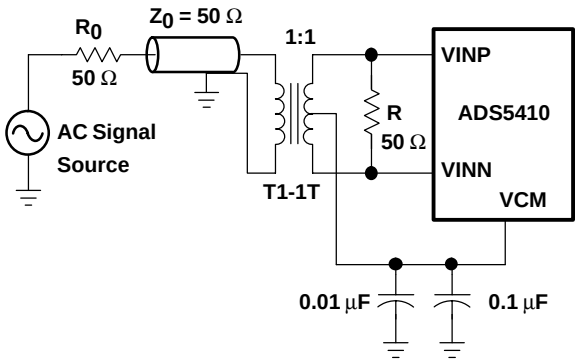


Figure 22. Driving the ADS5410 Analog Input With Impedance Matched Transmission Line

If it is necessary to buffer or apply a gain to the incoming analog signal, it is possible to combine a single-ended amplifier with an RF transformer as shown in Figure 23. TI offers a wide selection of operational amplifiers, as the THS3001, the OPA687, or the OPA690 that can be selected depending on the application. R_{in} and C_{in} can be placed to isolate the source from the switching inputs of the ADC and to implement a low pass RC filter to limit the input noise in the ADC. Although not needed, it is recommended to lay out the circuit with placement for those 3 components, which allows fine tune of the prototype if necessary. Nevertheless, any mismatch between the differential lines of the input produces a degradation in performance at high input frequencies, mainly characterized by an increase in the even harmonics. In this case, special care should be taken keeping as much electrical symmetry as possible between both inputs. This includes shorting R_{in} and leaving C_{in} unpopulated.

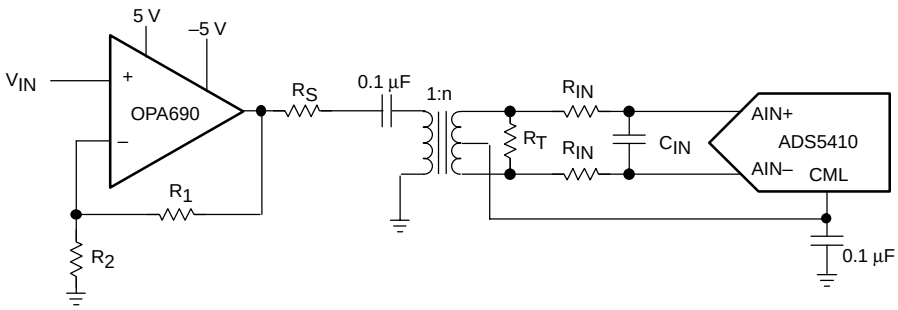


Figure 23. Converting a Single-Ended Input Signal Into a Differential Signal Using an RF Transformer

Another possibility is the use of differential input/output amplifiers that can simplify the driver circuit for applications requiring input dc coupling. Flexible in their configurations (Figure 24), such amplifiers can be used for single ended to differential conversion, for signal amplification, and also for filtering prior to the ADC.

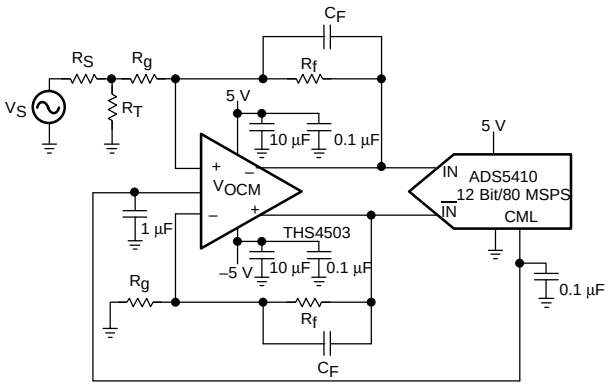


Figure 24. Using the THS4503 With the ADS5410

REFERENCE CIRCUIT

The ADS5410 has its own internal reference generation saving external circuitry in the design. For optimum performance, it is best to connect both VREFB and VREFT to ground with a 1-µF and 0.1-µF decoupling capacitors in parallel, and a 0.1-µF capacitor between both pins (Figure 25). The band-gap voltage output is not a voltage source, and is used internally by the ADS5410. However, it should be decoupled to ground with a 1-µF and 0.01-µF capacitor, in parallel.

CLOCK INPUTS

The ADS5410 clock input can be driven with either a differential clock signal or a single ended clock input with little or no difference in performance between the single-ended and differential-input configurations. The common mode of the clock inputs is set internally to $AV_{DD}/2$ using 5-kΩ resistors (Figure 20). The clock input should be either a sine wave or a square wave having a 50% duty cycle.

When driven with a single-ended CMOS clock input, it is best to connect the CLK input to ground with a 0.01-µF capacitor (see Figure 26) while CLK is ac couple with 0.01 µF to the clock source.

The ADS5410 clock input can also be driven differentially, reducing susceptibility to common mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.01-µF capacitors (see Figure 27). The differential input swing can vary between 1 V and 6 V with little or no performance degradation (see Figure 12).

POWER DOWN

When power down (pin 16) is tight to AVDD, the device reduces its power consumption until a typical value of 30 mW. Connecting this pin to GND enables the device operation.

DIGITAL OUTPUTS

The ADS5410 output format is 2s complement. The voltage level of the outputs can be adjusted by setting the OVDD voltage between 1.65 V and 3.6 V, allowing for direct interface to several digital families. For better performance, customers should select the smaller output swing required in the application. To improve the performance, mainly on the higher output voltage swing configurations, the addition of a series resistor at the outputs, limiting peak currents, is recommended. The maximum value of this resistor is limited by the maximum data rate of the application. Values between 0 Ω and 200 Ω are usual. Also, limiting the length of the external traces is a good practice.

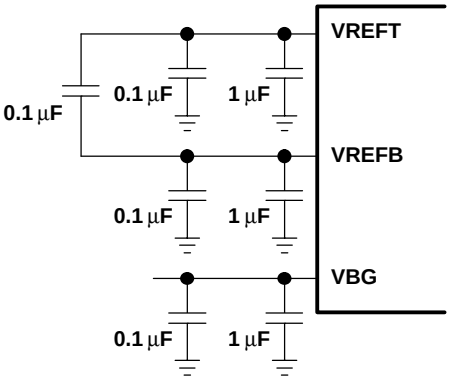


Figure 25. Internal Reference Usage

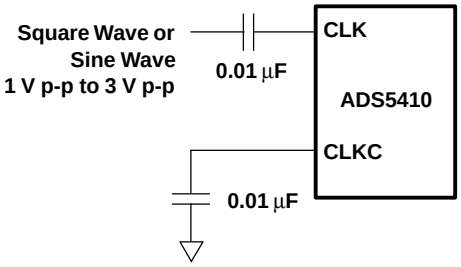


Figure 26. AC-Coupled Single-Ended Clock Input

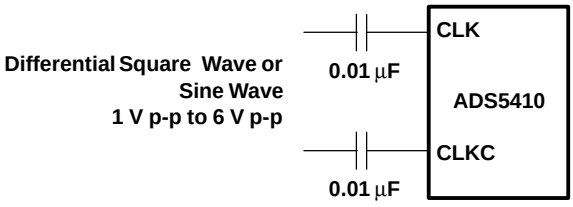


Figure 27. AC-Coupled Differential Clock Input

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point of the rising edge of the CLK command and the instant at which the analog input is sampled.

Aperture Uncertainity (Jitter)

The sample-to-sample variation in aperture delay.

Differential Nonlinearity

The average deviation of any single LSB transition at the digital output from an ideal 1 LSB step at the analog input.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a *best straight line* determined by a least square curve fit.

Clock Pulse Width/Duty Cycle

Pulse width high is the minimum amount of time that the CLK pulse should be left in logic 1 state to achieve rated performance; pulse width low is the minimum time CLK pulse should be left in low state. At a given clock rate, these specs define an acceptable clock duty cycles.

Maximum Conversion Rate

The clock rate at which parametric testing is performed.

Offset Error

The difference between the voltage at which the digital output transitions from midscale to one LSB above midscale, and the ideal voltage at which this transition should occur

Output Propagation Delay ($t_{d2(O)}$)

The delay between the 50% point of the rising edge of CLK command and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio

The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic and it is reported in dBc.

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product reported in dBc

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCE72010RGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CDCE72010	Samples
CDCE72010RGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CDCE72010	Samples
CDCE72010RGCTG4	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CDCE72010	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

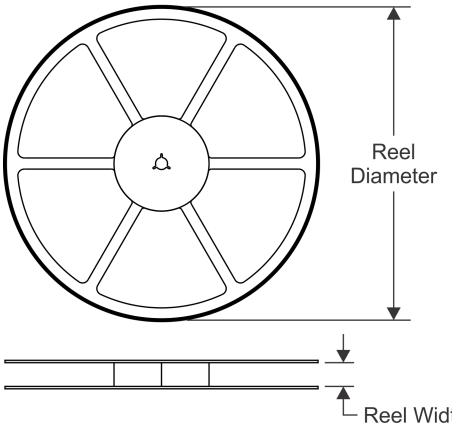
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

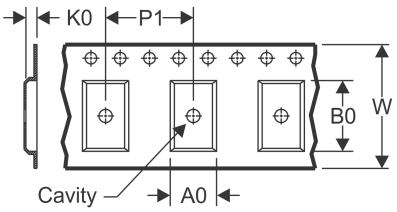
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

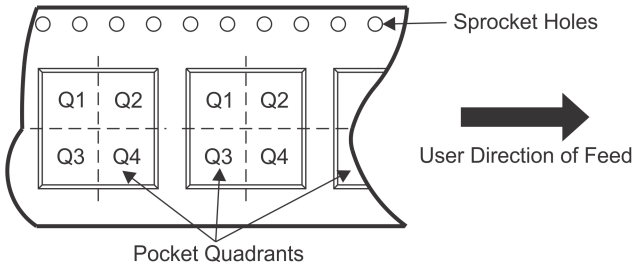


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

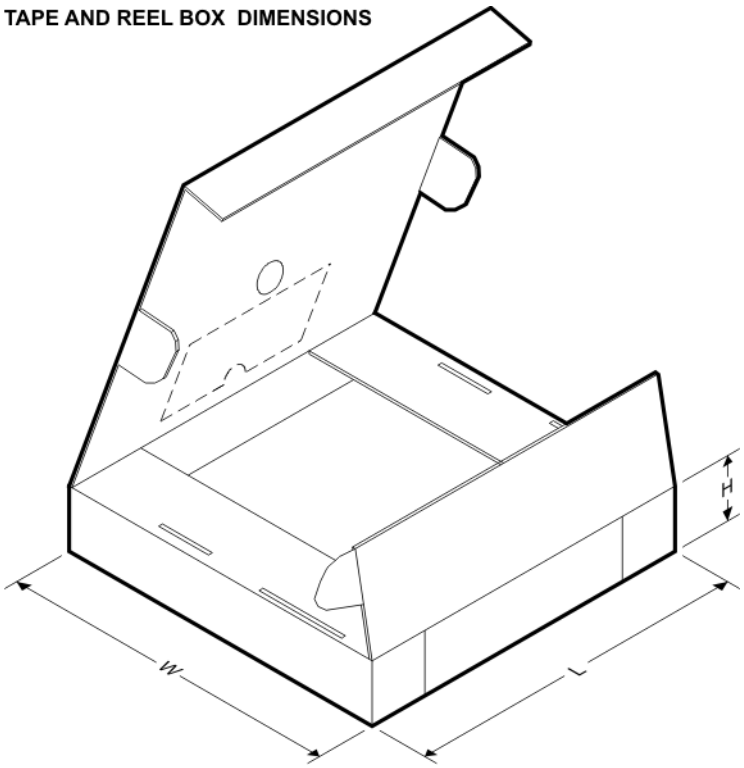
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE72010RGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
CDCE72010RGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE72010RGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
CDCE72010RGCT	VQFN	RGC	64	250	367.0	367.0	38.0

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