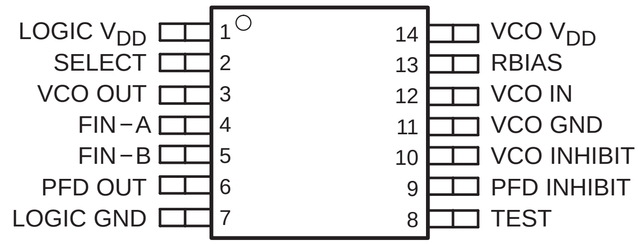
- **VCO (Voltage-Controlled Oscillator):**
  - **Complete Oscillator Using Only One External Bias Resistor (RBIAS)**
  - **Lock Frequency:**
    30 MHz to 55 MHz (VDD = 3 V ±5%, T_A = –20°C to 75°C, x1 Output)
    30 MHz to 60 MHz (VDD = 3.3 V ±5%, T_A = –20°C to 75°C, x1 Output)
    43 MHz to 110 MHz (VDD = 5 V ±5%, T_A = –20°C to 75°C, x1 Output)
  - **Selectable Output Frequency**
- **PFD (Phase Frequency Detector): High Speed, Edge-Triggered Detector with Internal Charge Pump**
- **Independent VCO, PFD Power-Down Mode**
- **Thin Small-Outline Package (14 Terminal)**
- **CMOS Technology**
- **Pin Compatible TLC2933IPW**

14-PIN TSOP (PW PACKAGE)
(TOP VIEW)



description

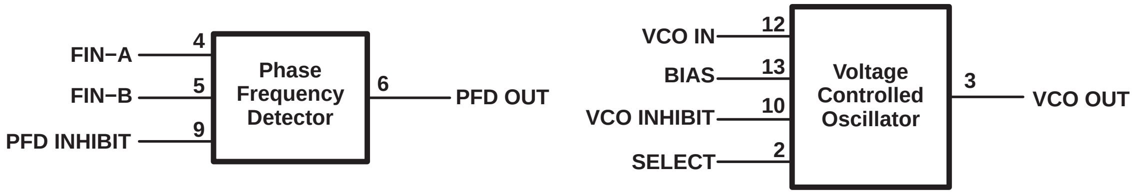
The TLC2933A is designed for phase-locked loop (PLL) systems and is composed of a voltage-controlled oscillator (VCO) and an edge-triggered type phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external bias resistor (R_{BIAS}). The VCO has a 1/2 frequency divider at the output stage. The high speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions, which can be used as power-down mode. Due to the TLC2933A high speed and stable oscillation capability, the TLC2933A is suitable for use as a high-performance PLL.

AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (PW)
–20°C to 75°C	TLC2933AIPW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
LOGIC VDD	1		Power supply for the internal logic. This power supply should be separated from VCO V_{DD} to reduce cross-coupling between supplies.
SELECT	2	I	VCO output frequency select. When SELECT is high, the VCO output frequency is ×1/2 and when low. The output frequency is ×1.
VCO OUT	3	O	VCO output. When the VCO INHIBIT is high, VCO output is low.
FIN−A	4	I	Input reference frequency $f_{(REF\ IN)}$ is applied to FIN−A.
FIN−B	5	I	Input for VCO external counter output frequency $f_{(FIN-B)}$. FIN−B is nominally provided from the external counter.
PFD OUT	6	O	PFD output. When the PFD INHIBIT is high, PFD output is in the high-impedance state.
LOGIC GND	7		GND for the internal logic.
TEST	8		Connect to GND.
PFD INHIBIT	9	I	PFD inhibit control. When PFD INHIBIT is high, PFD output is in the high-impedance state.
VCO INHIBIT	10	I	VCO inhibit control. When VCO INHIBIT is high, VCO output is low.
VCO GND	11		GND for VCO.
VCO IN	12	I	VCO control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.
RBIAS	13	I	Bias supply. An external resistor (R_{BIAS}) between VCO V_{DD} and R_{BIAS} supplies bias for adjusting the oscillation frequency range.
VCO V_{DD}	14		Power supply for VCO. This power supply should be separated from LOGIC V_{DD} to reduce cross-coupling between supplies.

detailed description

VCO oscillation frequency

The VCO oscillation frequency is determined by an external register (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depends on this Resistor value. For the lock frequency range, refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

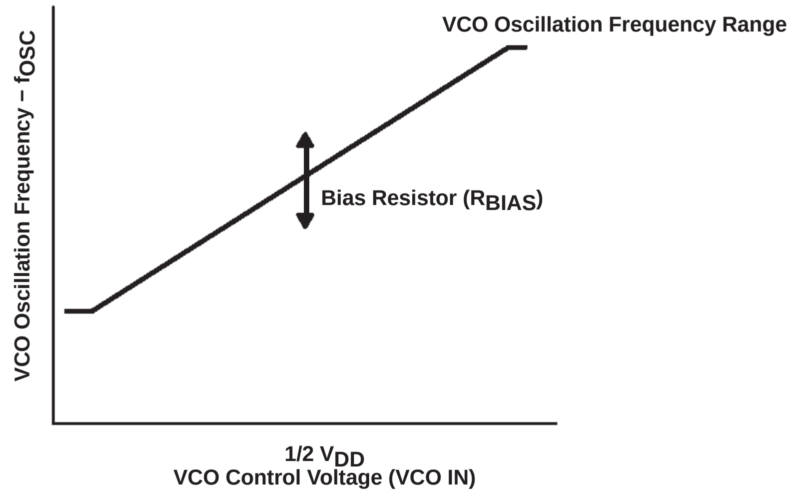


Figure 1. Oscillation Frequency

VCO output frequency 1/2 divider

The TLC2933A SELECT terminal sets the f_{OSC} VCO output frequency as shown in Table 1. The 1/2 f_{OSC} output should be used for minimum VCO output jitter.

Table 1. VCO Output 1/2 Divider Function

SELLECT	VCO OUTPUT
Low	f_{OSC}
High	1/2 f_{OSC}

VCO inhibit function

The VCO has an externally controlled inhibit function which inhibit the VCO output. A high level on the VCO INHIBIT terminal stops the VCO oscillation and powers down the VCO. The output maintains a low level during the power−down mode as shown in Table 2.

Table 2. VCO Inhibit Function

VCO INHIBIT	VCO OSCILLATOR	VCO OUT	$I_{DD(VCO)}$
Low	Active	Active	Normal
High	Stopped	Low level	Power Down

PFD operation

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to FIN−A and FIN−B as shown in Figure 2. Normally the reference is supplied to FIN−A and the frequency from the external counter output is fed to FIN−B. For clock recovery PLL system, other types of phase detectors should be used.

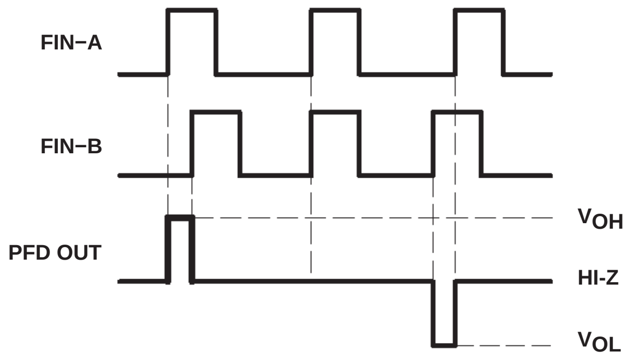


Figure 2. PFD Function Timing Chart

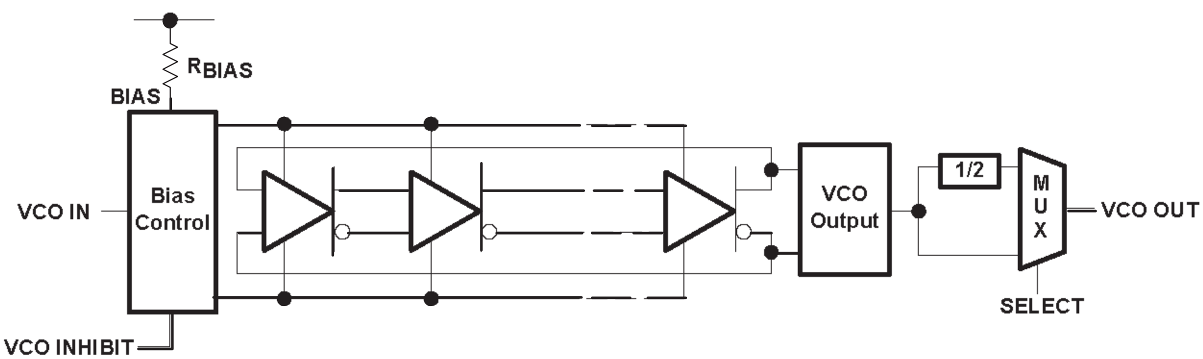
PFD inhibit control

A high level on the PFD INHIBIT terminal places PFD OUT in the high-impedance state and the PFD stops phase detection as shown in Table 3. A high level on the PFD INHIBIT terminal can also be used as the power-down mode for the PFD.

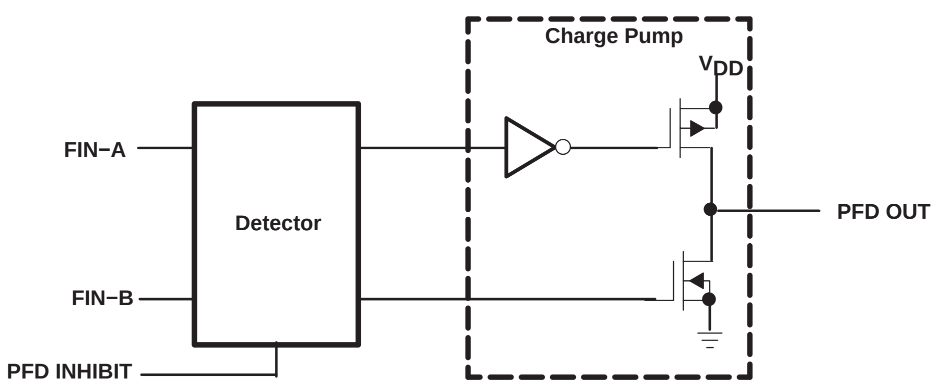
Table 3. VCO Output Control Function

PFD INHIBIT	DETECTION	PFD OUT	$I_{DD(PFD)}$
Low	Active	Active	Normal
High	Stopped	Hi−Z	Power Down

VCO block schematic



PFD block schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (each supply), V_{DD} (see Note 1) . . . . 7 V
Input voltage range (each input), V_{IN} (see Note 1) . . . . −0.5 V to V_{DD} + 0.5 V
Input current (each input), I_{IN} . . . . ±20 mA
Output current (each output), I_O . . . . ±20 mA
Operating free-air temperature range, T_A . . . . –20°C to 75°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 5.6 mW/°C.

recommended operating conditions

PARAMETERS		MIN	TYP	MAX	UNIT
Supply voltage (each supply, see Note 3)	V_{DD} = 3 V	2.85	3	3.15	V
	V_{DD} = 3.3 V	3.135	3.3	3.465	
	V_{DD} = 5 V	4.75	5	5.25	
Input voltage, (inputs except VCO IN)		0		V_{DD}	V
Output current, (each output)		0		±2	mA
VCO control voltage at VCO IN		0.9		V_{DD}	V
Lock frequency	V_{DD} = 3 V	30		55	MHz
	V_{DD} = 3.3 V	30		60	
	V_{DD} = 5 V	43		110	
Bias resisitor	V_{DD} = 3 V	2.2		5.1	kΩ
	V_{DD} = 3.3 V	2.2		5.1	
	V_{DD} = 5 V	2.2		5.1	

NOTE 3: It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) should be at the same voltage and separated from each other.

electrical characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.3	V
V_{TH}	Input threshold voltage at select, VCO inhibit		0.9	1.5	2.1	V
I_I	Input current at Select, VCO inhibit	V_I = V_{DD} or GND			±1	µA
$Z_{I(VCOIN)}$	VCO IN input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.41	1	µA
$I_{DD(VCO)}$	VCO supply current	See Note 5		11.7	23	mA

NOTES: 4. Current into VCO V_{DD}, when VCO INHIBIT = high, PFD is inhibited.
5. Current into VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCOOUT = 15-pF Load, VCO INHIBIT = GND, and PFD INHIBIT = GND.

electrical characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted) (continued)

PFD section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.3	V
I_{OZ}	High impedance state output current	PFD inhibit = high, V_O = V_{DD} or GND			±1	µA
V_{IH}	High level input voltage at Fin−A, Fin−B		2.1			V
V_{IL}	Low level input voltage at Fin−A, Fin−B				0.5	V
V_{TH}	Input threshold voltage at PFD inhibit		0.9	1.5	2.1	
C_{IN}	Input capacitance at Fin−A, Fin−B			5.6		pF
Z_{IN}	Input impedance at Fin−A, Fin−B			10		MΩ
$I_{DD(Z)}$	High impedance state PFD supply current	See Note 6			1	µA
$I_{DD(PFD)}$	PFD supply current	See Note 7			3	mA

NOTES: 6. The current into LOGIC V_{DD} when FIN−A and FIN−B = ground, PFD INHIBIT = V_{DD}, PFD OUT open, and VCO OUT is inhibited.
7. The current into LOGIC V_{DD} when FIN−A = 1 MHz and FIN−B = 1 MHz ($V_{I(PP)}$ = 3 V, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.

operation characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

VCO section

	Parameter	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Operation oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}	32	47	63	MHz
f_{STB}	Time to stable oscillation (see Note 8)				10	µs
t_r	Rise time	C_L = 15 pF		8.6	14	ns
t_f	Fall time	C_L = 15 pF		7.1	12	ns
	Duty cycle at VCO OUT	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}	45%	50%	55%	
α (f_{OSC})	Temperature coefficient of oscillation frequency	VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		–0.21		%/°C
k_{SVS} (fosc)	Supply voltage coefficient of oscillation frequency	VCO IN = 1/2 V_{DD}, V_{DD} = 4.75 V to 5.25 V		0.002		%/mV
	Jitter absolute (see Note 9)	PLL jitter, N = 128		262		ps

NOTES: 8. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully deigned PCB with no device socket.

PFD section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operation frequency		32			MH
t_{PLZ}	PFD output disable time from low level			22	50	ns
t_{PHZ}	PFD output disable time from high level			21	50	ns
t_{PZL}	PFD output enable time to low level			6.5	30	ns
t_{PZH}	PFD output enable time to high level			7	30	ns
t_r	Rise time	C_L = 15 pF		3.4	10	ns
t_f	Fall time	C_L = 15 pF		1.9	10	ns

electrical characteristics, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

VCO section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –2 mA	2.64			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.33	V
V_{TH}	Input threshold voltage at select, VCO inhibit		1.05	1.65	2.25	V
I_I	Input current at Select, VCO inhibit	V_I = V_{DD} or GND			±1	µA
$Z_{I(VCOIN)}$	VCO IN input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 10		0.44	1	µA
$I_{DD(VCO)}$	VCO supply current	See Note 11		14.7	28	mA

NOTES: 10. Current into VCO V_{DD}, when VCO INHIBIT = high, PFD is inhibited.
11. Current into VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCOOUT = 15-pF Load, VCO INHIBIT = GND, and PFD INHIBIT = GND.

PFD section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –2 mA	2.97			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High impedance state output current	PFD inhibit = high, V_O = V_{DD} or GND			±1	µA
V_{IH}	High level input voltage at Fin−A, Fin−B		2.1			V
V_{IL}	Low level input voltage at Fin−A, Fin−B				0.5	V
V_{TH}	Input threshold voltage at PFD inhibit		1.05	1.65	2.25	
C_{IN}	Input capacitance at Fin−A, Fin−B			5.6		pF
Z_{IN}	Input impedance at Fin−A, Fin−B			10		MΩ
$I_{DD(Z)}$	High impedance state PFD supply current	See Note 12			1	µA
$I_{DD(PFD)}$	PFD supply current	See Note 13			3	mA

NOTES: 12. The current into LOGIC V_{DD} when FIN−A and FIN−B = ground, PFD INHIBIT = V_{DD}, PFD OUT open, and VCO OUT is inhibited.
13. The current into LOGIC V_{DD} when FIN−A = 1 MHz and FIN−B = 1 MHz ($V_{I(PP)}$ = 3.3 V, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.

operation characteristics, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

VCO section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Operation oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 VDD	35	55	80	MHz
fstb	Time to stable oscillation (see Note 14)				10	µs
tr	Rise time	C_L = 15 pF		8.3	14	ns
t_f	Fall time	C_L = 15 pF		6.7	12	ns
f_{DUTY}	Duty cycle at VCO OUT	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 VDD	45%	50%	55%	
α (f_{OSC})	Temperature coefficient of oscillation frequency	VCO IN = 1/2 VDD, T_A = –20°C to 75°C		–0.232		%/°C
$k_{SVS}(f_{OSC})$	Supply voltage coefficient of oscillation frequency	VCO IN = 1/2 V_{DD}, V_{DD} = 4.75 V to 5.25 V		0.002		%/mV
	Jitter absolute (see Note 15)	PLL jitter, N = 128		211		ps

NOTES: 14. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
15. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully deigned PCB with no device socket.

operation characteristics, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted) (continued)

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operation frequency		40			MHz
t_{PLZ}	PFD output disable time from low level			21	50	ns
t_{PHZ}	PFD output disable time from high level			21	50	ns
t_{PZL}	PFD output enable time to low level			5.8	30	ns
t_{PZH}	PFD output enable time to high level			6.2	30	ns
t_r	Rise time	C_L = 15 pF		3	10	ns
t_f	Fall time	C_L = 15 pF		1.7	10	ns

electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –2 mA	4			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.5	V
V_{TH}	Input threshold voltage at select, VCO inhibit		1.5	2.5	3.5	V
I_I	Input current at select, VCO inhibit	V_I = V_{DD} or GND			±1	µA
$Z_{I(VCOIN)}$	VCO IN input impedance	VCO IN = 1/2 V_{DD}		10		M(
IDD(inh)	VCO supply current (inhibit)	See Note 16		0.61	1	µA
IDD(vco)	VCO supply current	See Note 17		35.5	55	mA

NOTES: 16. Current into VCO V_{DD}, when VCO INHIBIT = high, PFD is inhibited.
17. Current into VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCOOUT = 15-pF Load, VCO INHIBIT = GND, and PFD INHIBIT = GND.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –2 mA	4.5			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High impedance state output current	PFD inhibit = high, V_o = V_{DD} or GND			±1	µA
V_{IH}	High level input voltage at Fin−A, Fin−B		4.5			V
V_{IL}	Low level input voltage at Fin−A, Fin−B				1	V
V_{TH}	Input threshold voltage at PFD inhibit		1.5	2.5	3.5	
C_{IN}	Input capacitance at Fin−A, Fin−B			5.6		pF
Z_{IN}	Input impedance at Fin−A, Fin−B			10		MΩ
$I_{DD(Z)}$	High impedance state PFD supply current	See Note 18			1	µA
$I_{DD(PFD)}$	PFD supply current	See Note 19		0.48	3	mA

NOTES: 18. The current into LOGIC V_{DD} when FIN−A and FIN−B = ground, PFD INHIBIT = V_{DD}, PFD OUT open, and VCO OUT is inhibited.
19. The current into LOGIC V_{DD} when FIN−A = 1 MHz and FIN−B = 1 MHz ($V_{I(PP)}$ = 5 V, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited

operation characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

VCO section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Operation oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}	70	99	130	MHz
f_{STB}	Time to stable oscillation (see Note 20)				10	us
t_r	Rise time	C_L = 15 pF		5.4	10	ns
t_f	Fall time	C_L = 15 pF		5	10	ns
f_{DUTY}	Duty cycle at VCO OUT	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}	45%	50%	55%	
α (f_{OSC})	Temperature coefficient of oscillation frequency	VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		–0.309		%/°C
k_{SVS}(f_{OSC})	Supply voltage coefficient of oscillation frequency	VCO IN = 1/2 V_{DD}, V_{DD} = 4.75 V to 5.25 V		0.001		%/mV
	Jitter absolute (see Note 21)	PLL jitter, N = 128		140		ps

NOTES: 20. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
21. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully deigned PCB with no device socket.

PFD section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operation frequency		65			MHz
t_{PLZ}	PFD output disable time from low level			20	40	ns
t_{PHZ}	PFD output disable time from high level			20	40	ns
t_{PZL}	PFD output enable time to low level			4	20	ns
t_{PZH}	PFD output enable time to high level			4.3	20	ns
t_r	Rise time	C_L = 15 pF		2.1	10	ns
t_f	Fall time	C_L = 15 pF		1.3	10	ns

PARAMETER MEASUREMENT INFORMATION

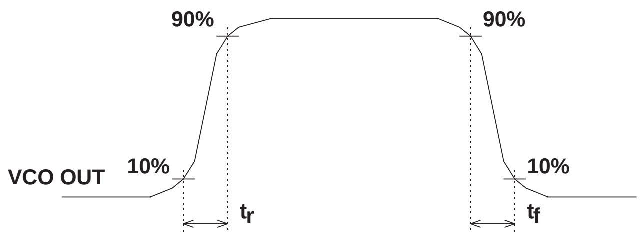


Figure 3. VCO Output Voltage Waveform

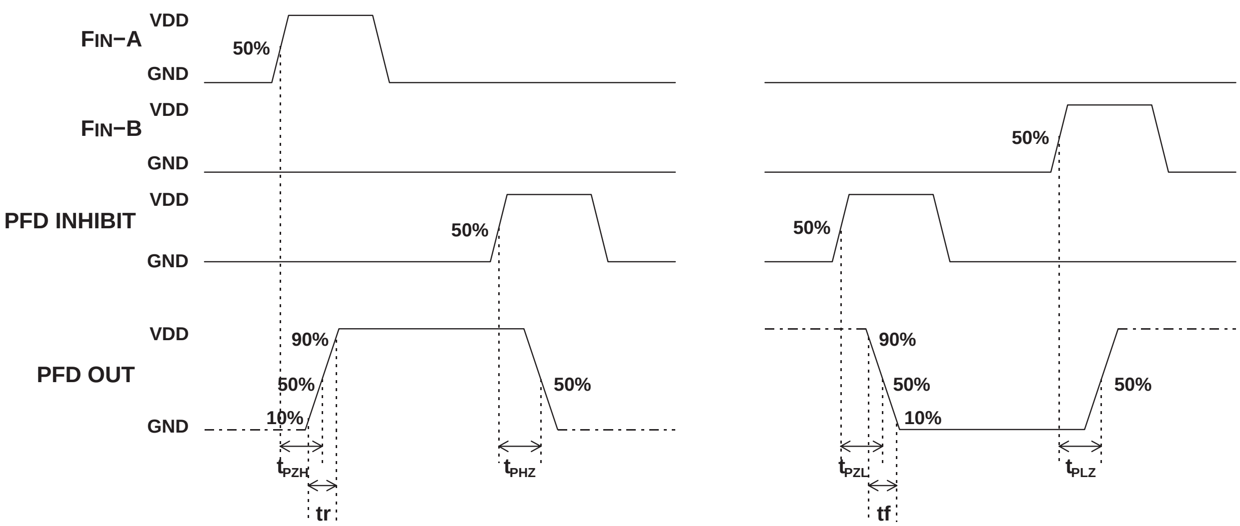


Figure 4. PFD Output Voltage Waveform

Table 4. PFD Output Test Conditions

PARAMETER	R_L	C_L	S1	S2
t_{PZH}	1 kΩ	15 pF	OPEN	CLOSE
t_{PHZ}				
t_r				
t_{PZL}			CLOSE	OPEN
t_{PLZ}				
t_f				

PARAMETER MEASUREMENT INFORMATION

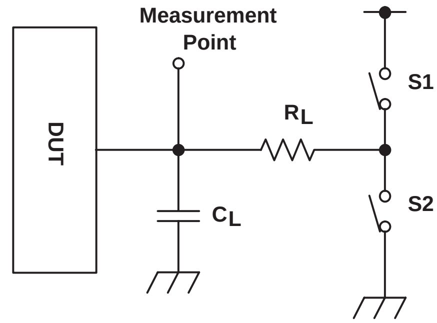


Figure 5. PFD Output Test Conditions

TYPICAL CHARACTERISTICS

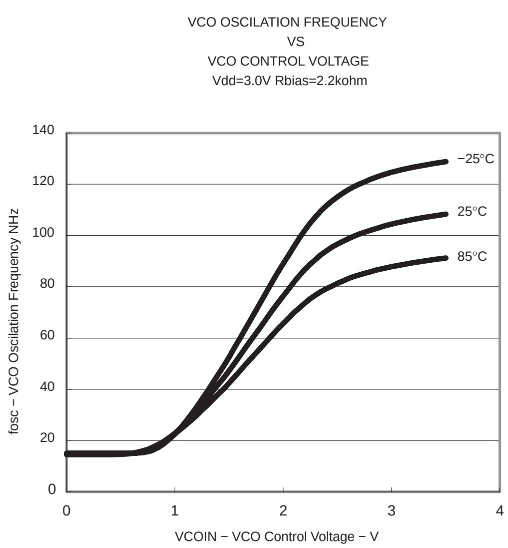


Figure 6.

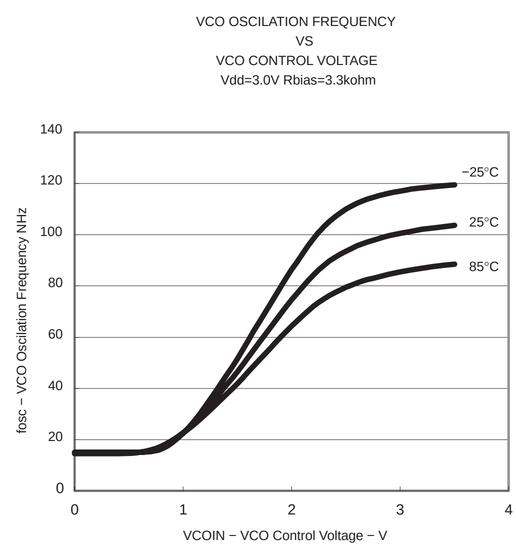


Figure 7.

TYPICAL CHARACTERISTICS

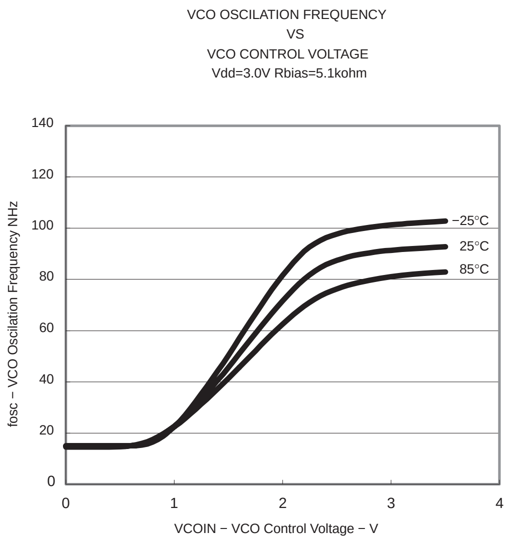


Figure 8.

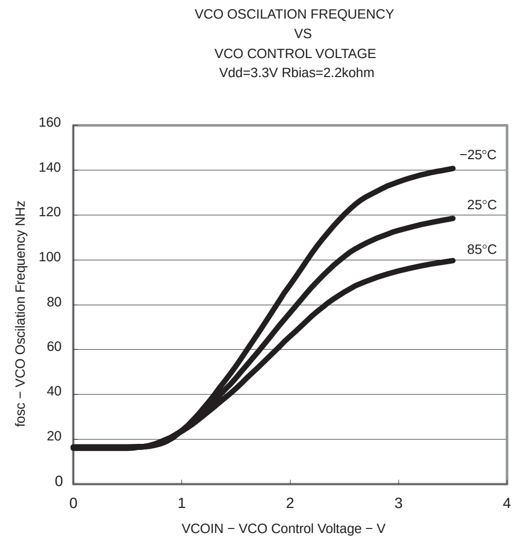


Figure 9.

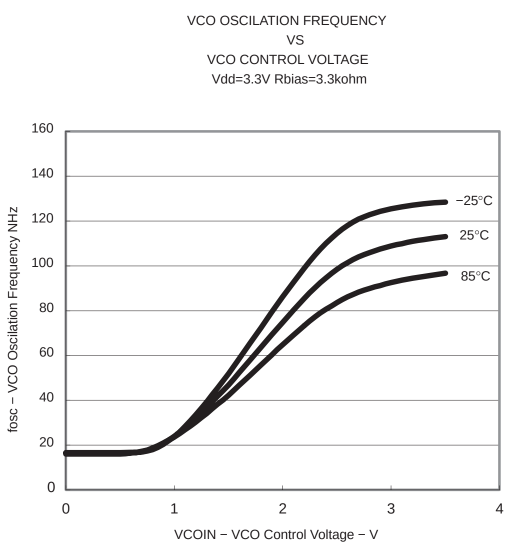


Figure 10.

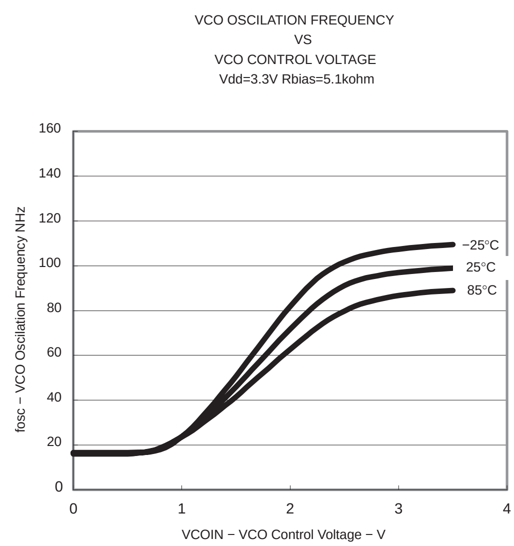


Figure 11.

TYPICAL CHARACTERISTICS

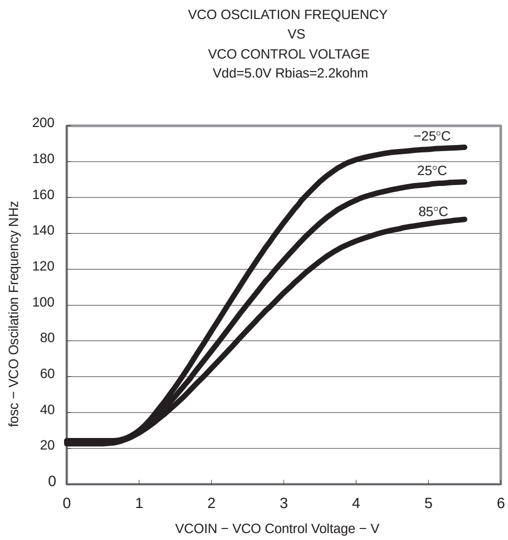


Figure 12.

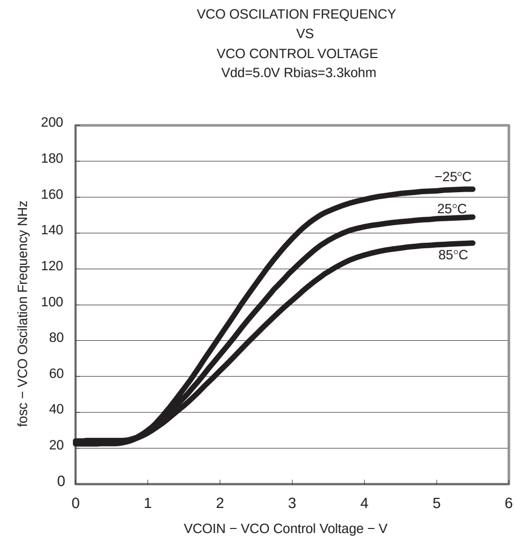
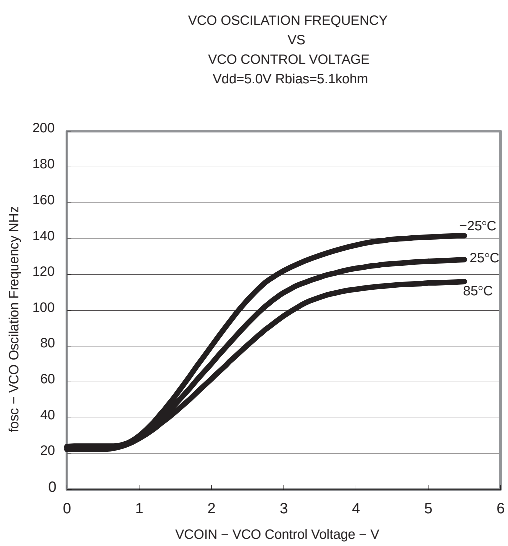


Figure 13.



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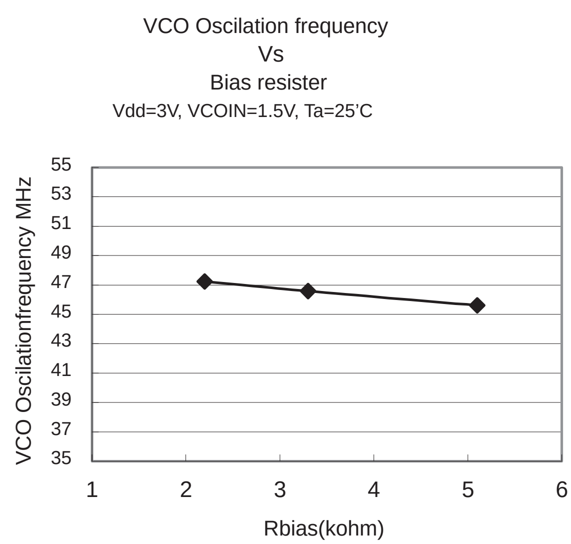
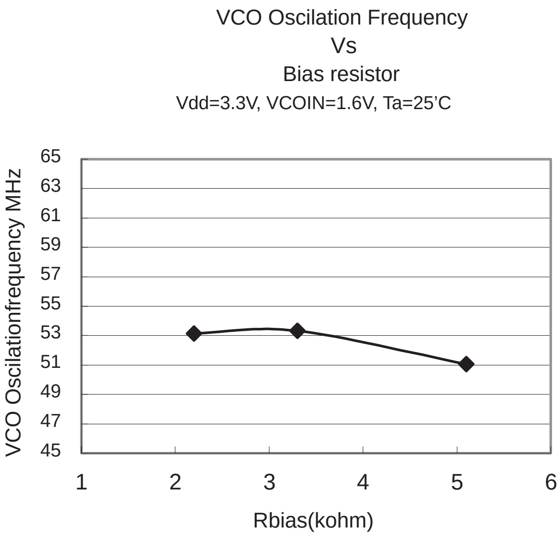


Figure 15.

TYPICAL CHARACTERISTICS



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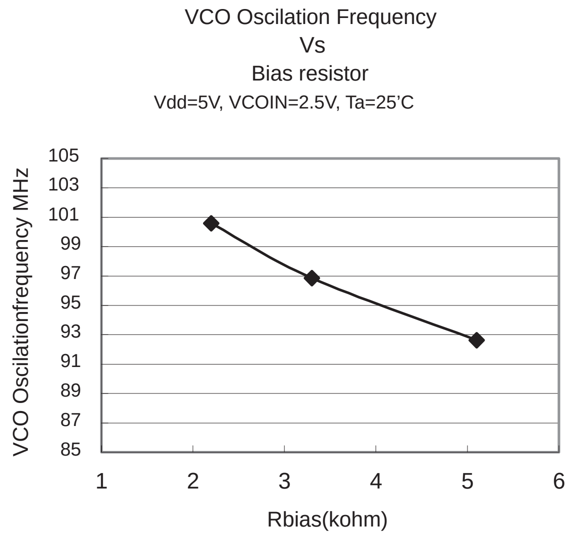


Figure 17.

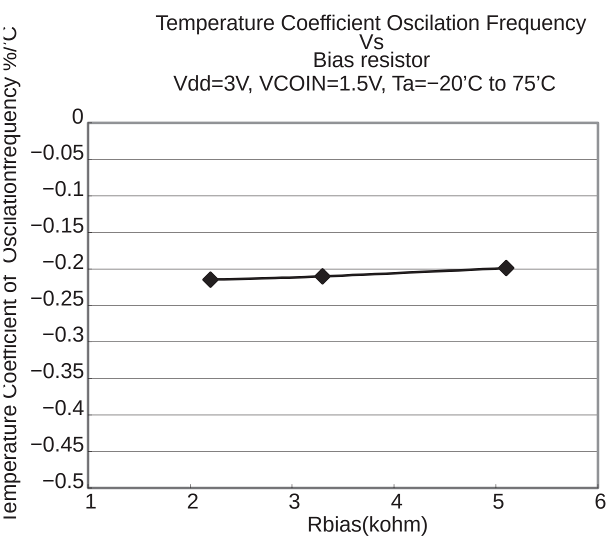


Figure 18.

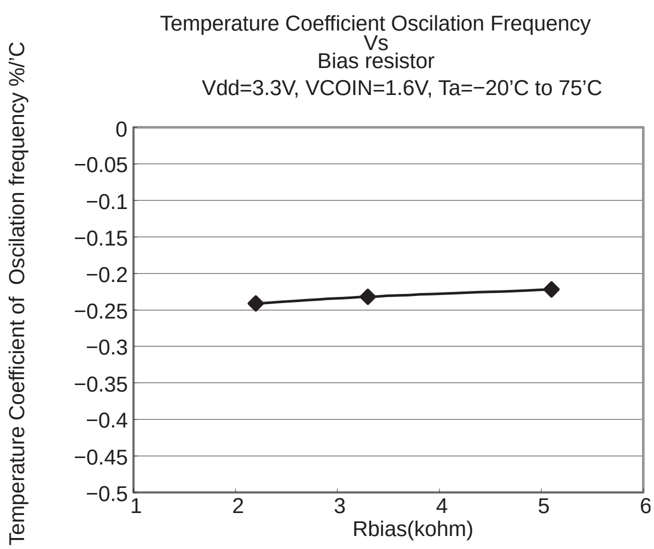


Figure 19.

TYPICAL CHARACTERISTICS

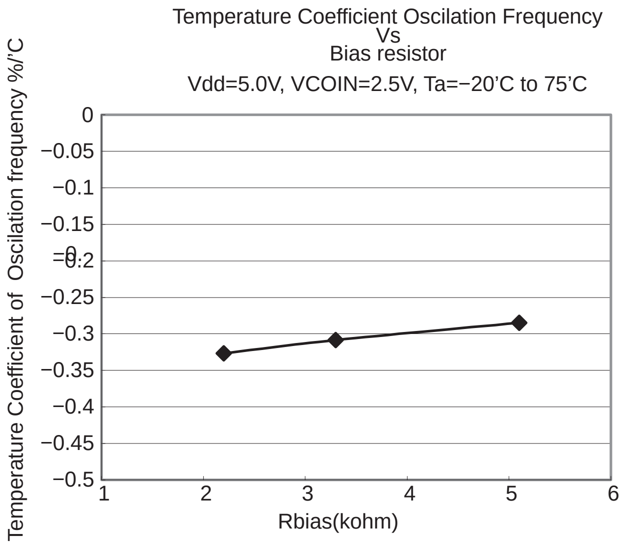
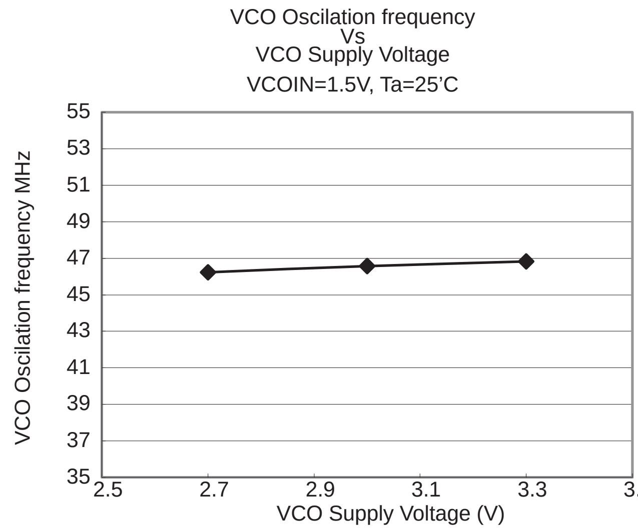


Figure 20.



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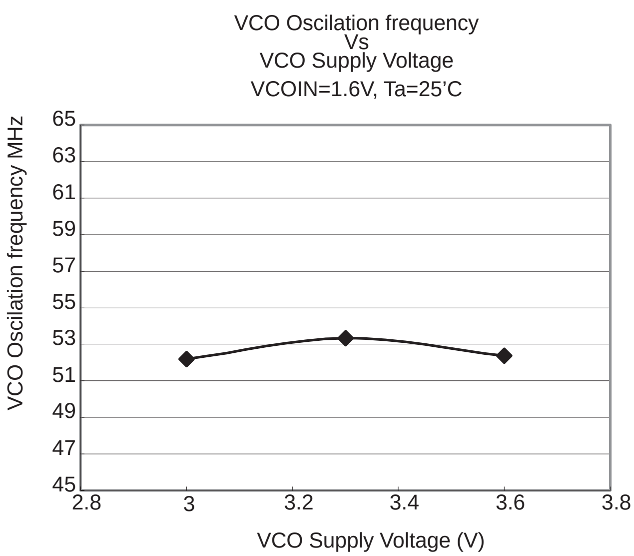

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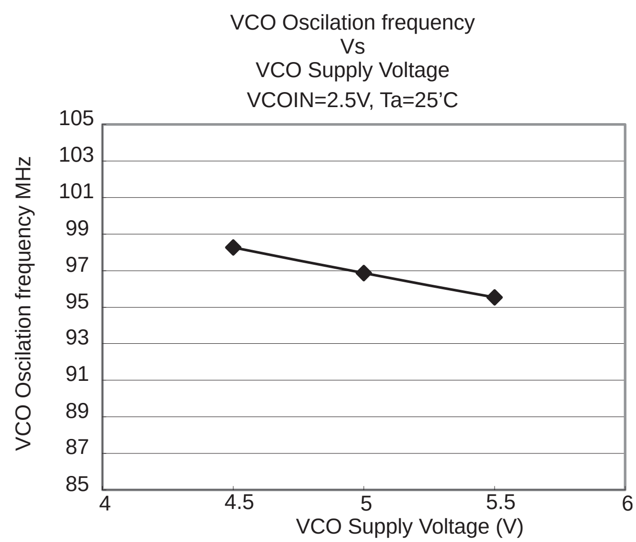


Figure 23.

TYPICAL CHARACTERISTICS

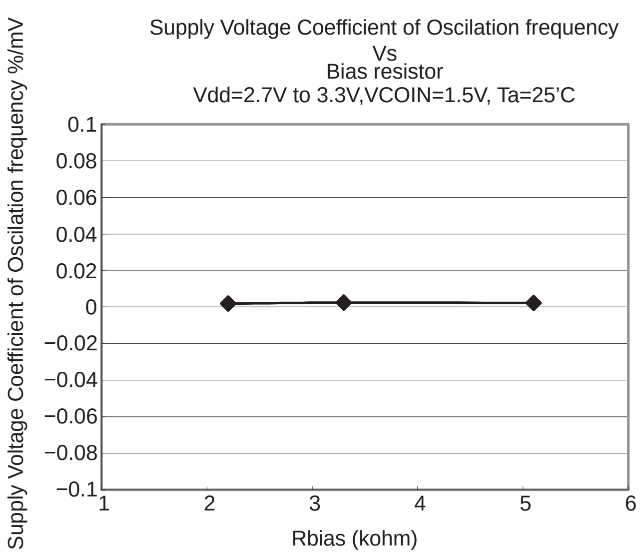
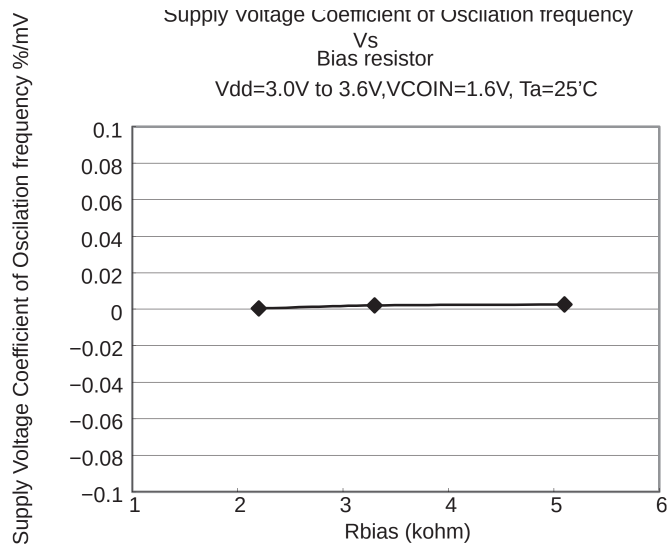


Figure 24.



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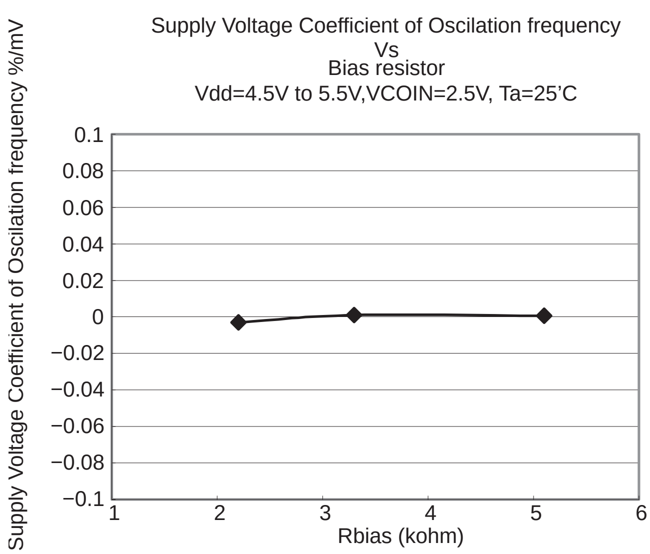


Figure 26.

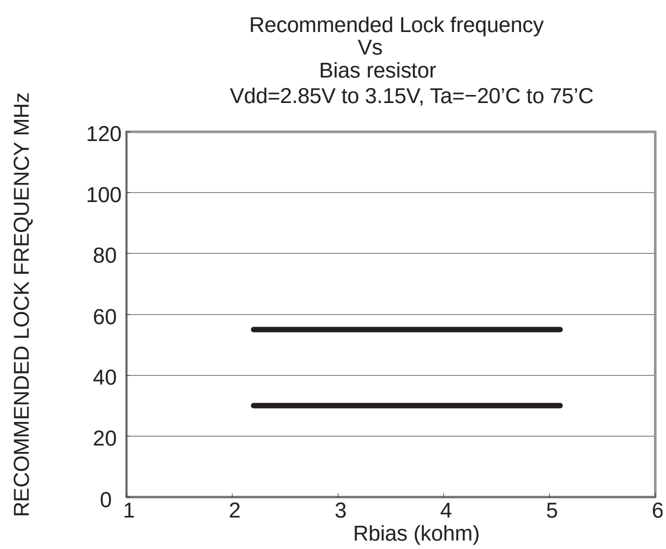


Figure 27.

TYPICAL CHARACTERISTICS

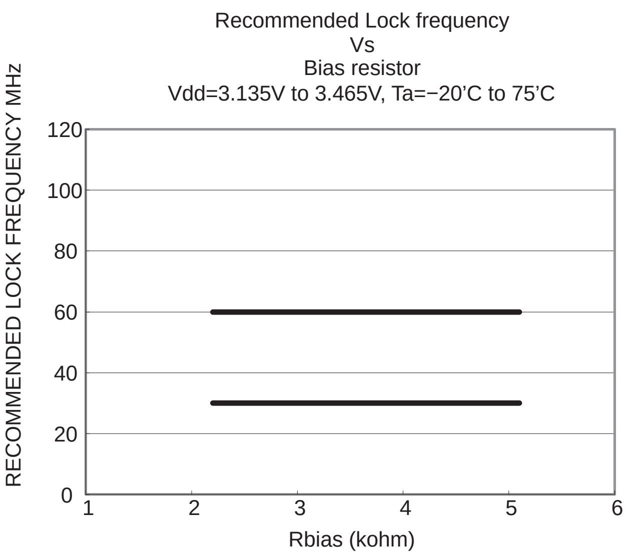


Figure 28.

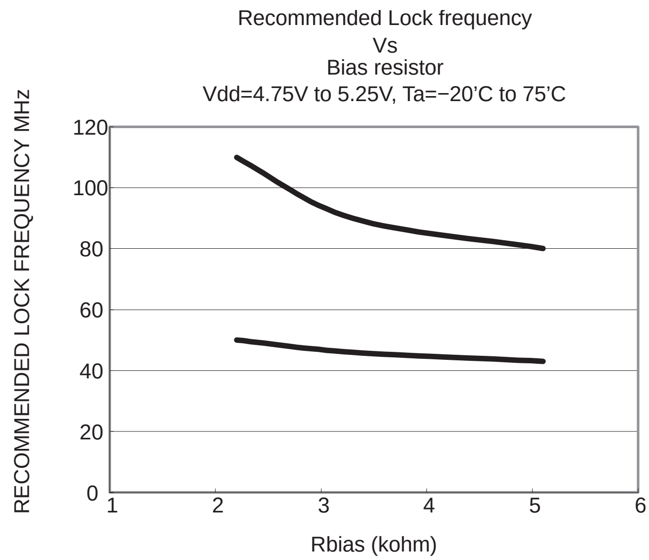


Figure 29.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2933AIPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2933A
TLC2933AIPW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2933A
TLC2933AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2933A
TLC2933AIPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2933A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

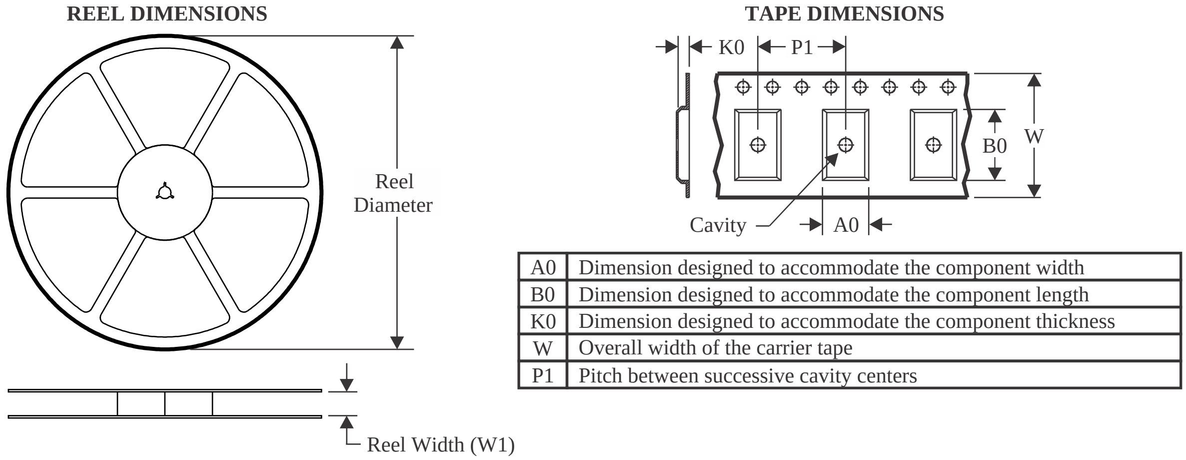
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

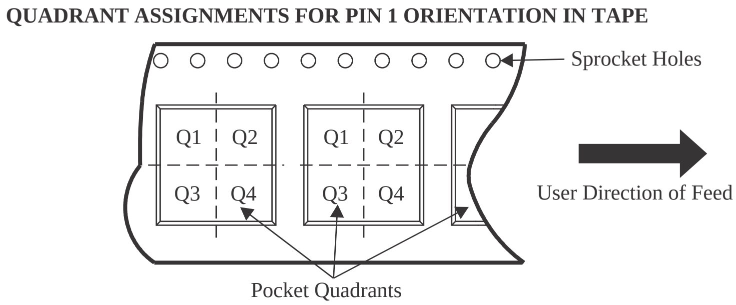
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



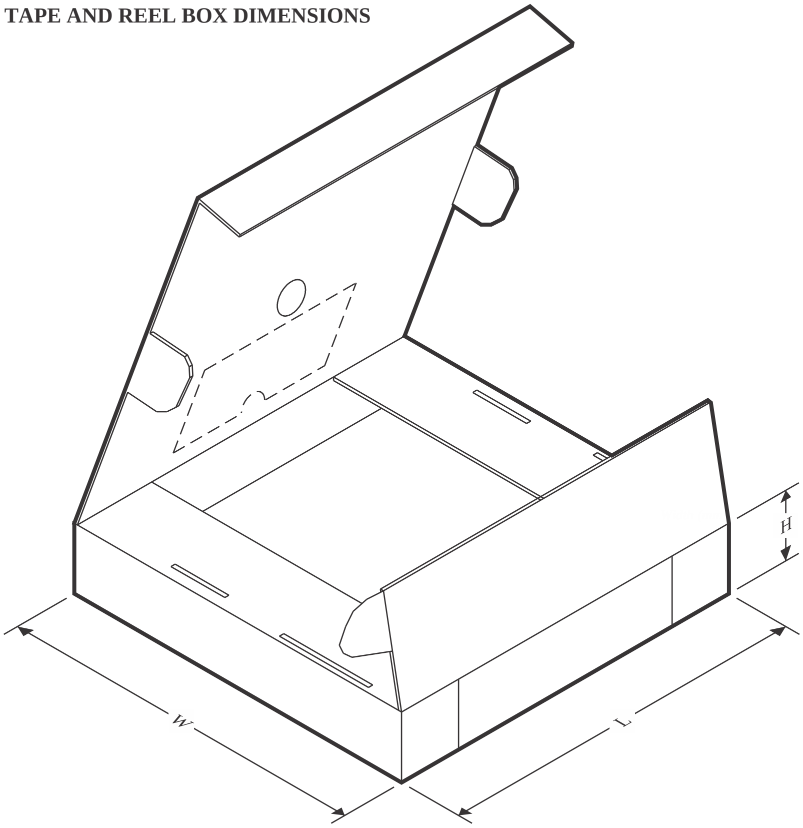
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2933AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

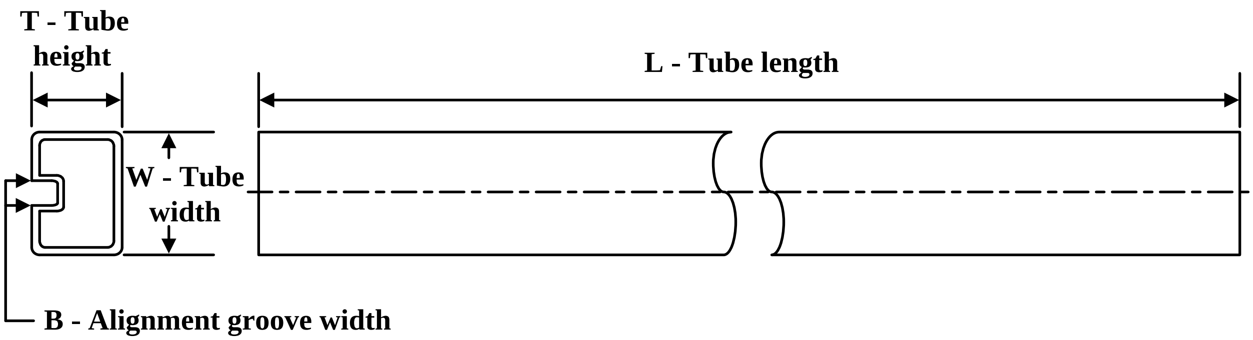
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

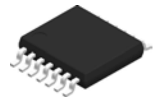
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2933AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE

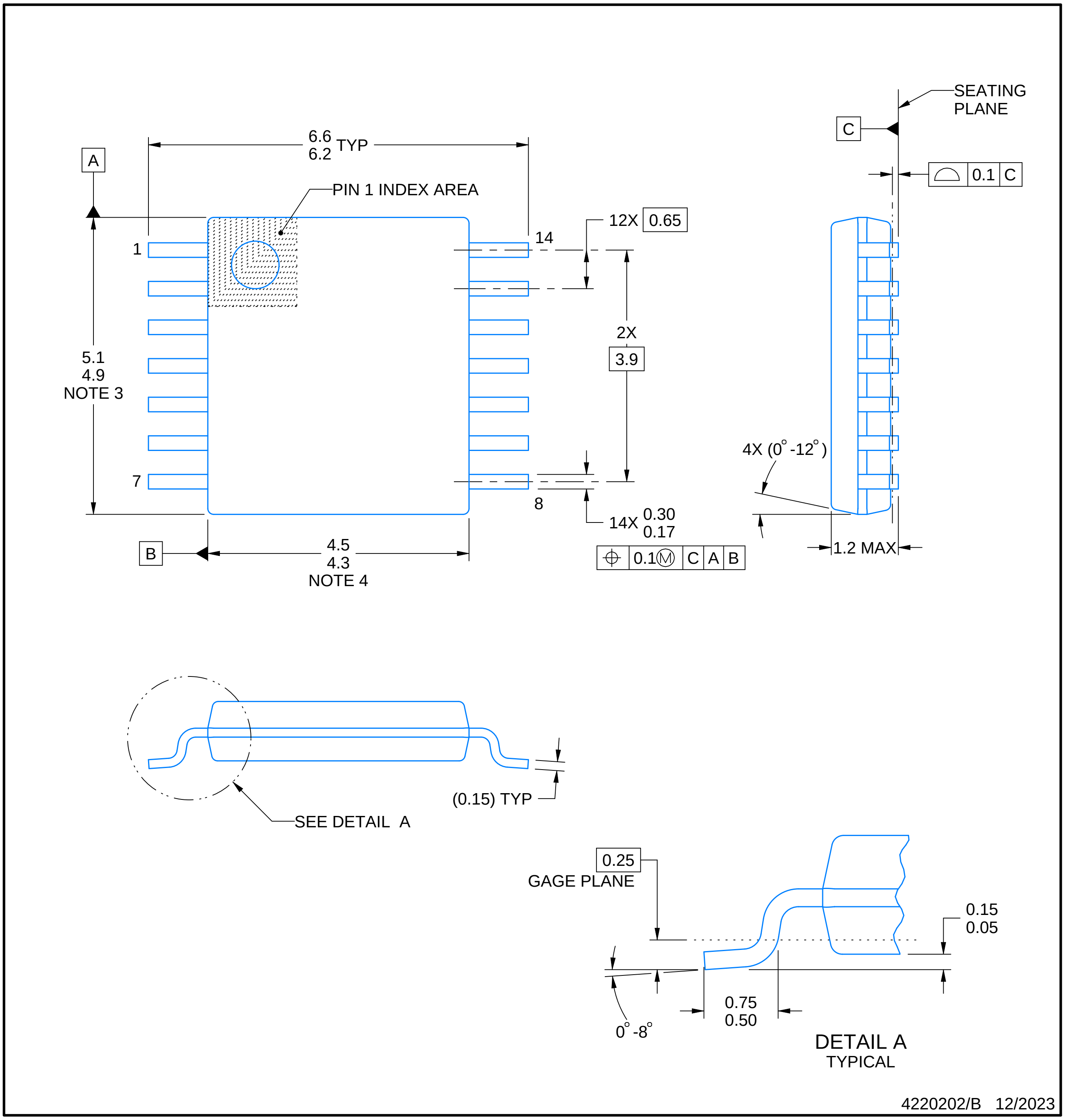


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC2933AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC2933AIPW.B	PW	TSSOP	14	90	530	10.2	3600	3.5

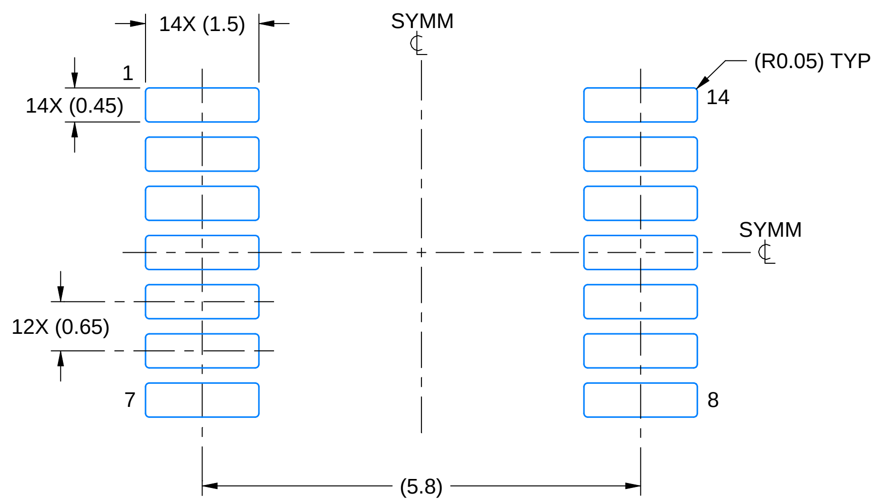


SMALL OUTLINE PACKAGE

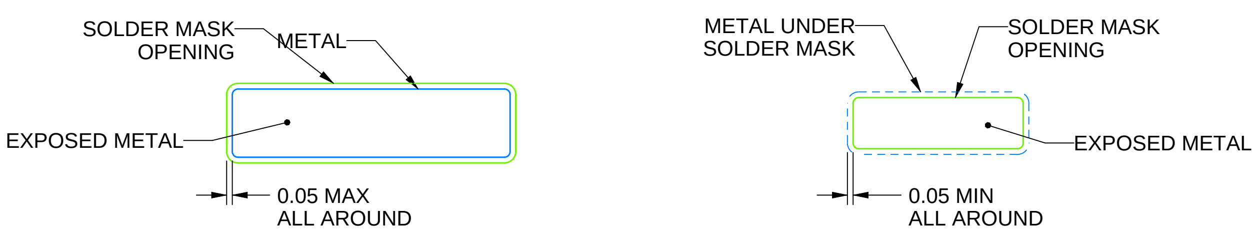


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)

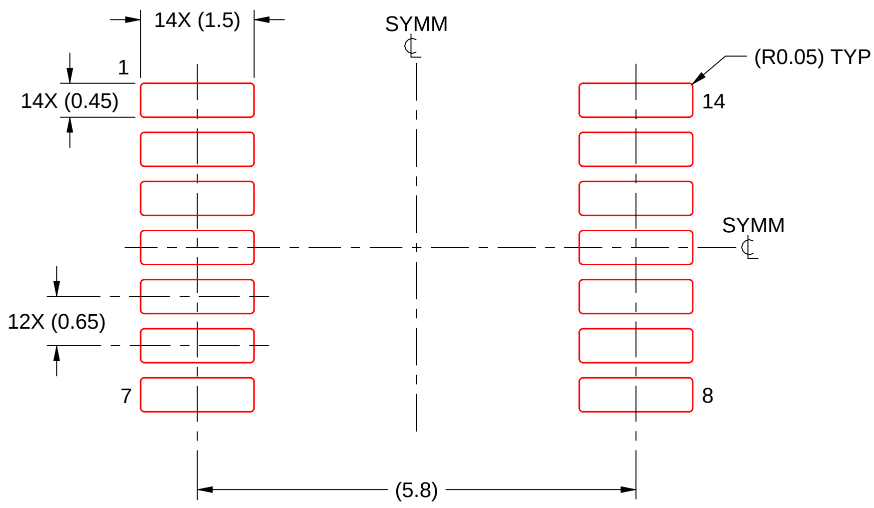
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.