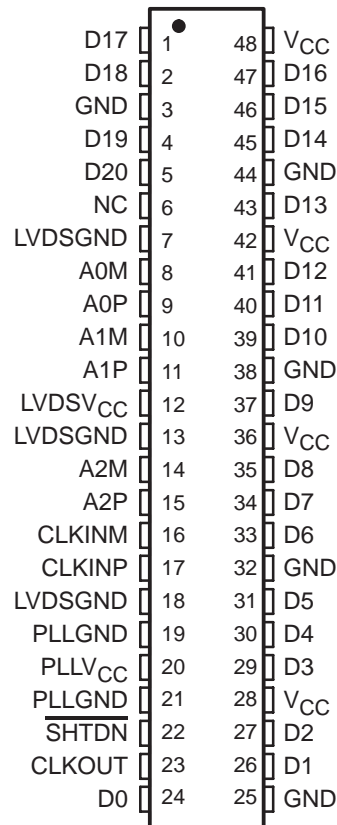- **3:21 Data Channel Expansion at up to 178.5 Mbytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **Three Data Channels and Clock Low-Voltage Differential Channels In and 21 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply**
- **Tolerates 4-kV HBM ESD**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range of 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Inputs Meet or Exceed the Standard Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the DS90C364 and SN75LVDS86**
- **Improved Jitter Tolerance**
- **See SN65LVDS86A-Q1 Data Sheet for Information About the Automotive Qualified Version**

DGG PACKAGE
(TOP VIEW)

D17	1	48	V_{CC}
D18	2	47	D16
GND	3	46	D15
D19	4	45	D14
D20	5	44	GND
NC	6	43	D13
LVDSGND	7	42	V_{CC}
A0M	8	41	D12
A0P	9	40	D11
A1M	10	39	D10
A1P	11	38	GND
LVDSV$_{CC}$	12	37	D9
LVDSGND	13	36	V_{CC}
A2M	14	35	D8
A2P	15	34	D7
CLKINM	16	33	D6
CLKINP	17	32	GND
LVDSGND	18	31	D5
PLLGND	19	30	D4
PLLV$_{CC}$	20	29	D3
PLLGND	21	28	V_{CC}
$\overline{SHTDN}$	22	27	D2
CLKOUT	23	26	D1
D0	24	25	GND

NC – Not connected

description

The SN65LVDS86A/SN75LVDS86A FlatLink™ receiver contains three serial-in 7-bit parallel-out shift registers and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, '83, '84, or '85, over four balanced-pair conductors and expansion to 21 bits of single-ended low-voltage LVTTL synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at seven times the LVDS input clock (CLKIN) rate. The data is then unloaded to a 21-bit-wide LVTTL parallel bus at the CLKIN rate. The 'LVDS86A presents valid data on the falling edge of the output clock (CLKOUT).

The 'LVDS86A requires only four line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear ($\overline{SHTDN}$) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN75LVDS86A is characterized for operation over ambient free-air temperatures of 0°C to 70°C. The SN65LVDS86A is characterized for operation over the full Automotive temperature range of −40°C to 125°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TEXAS INSTRUMENTS

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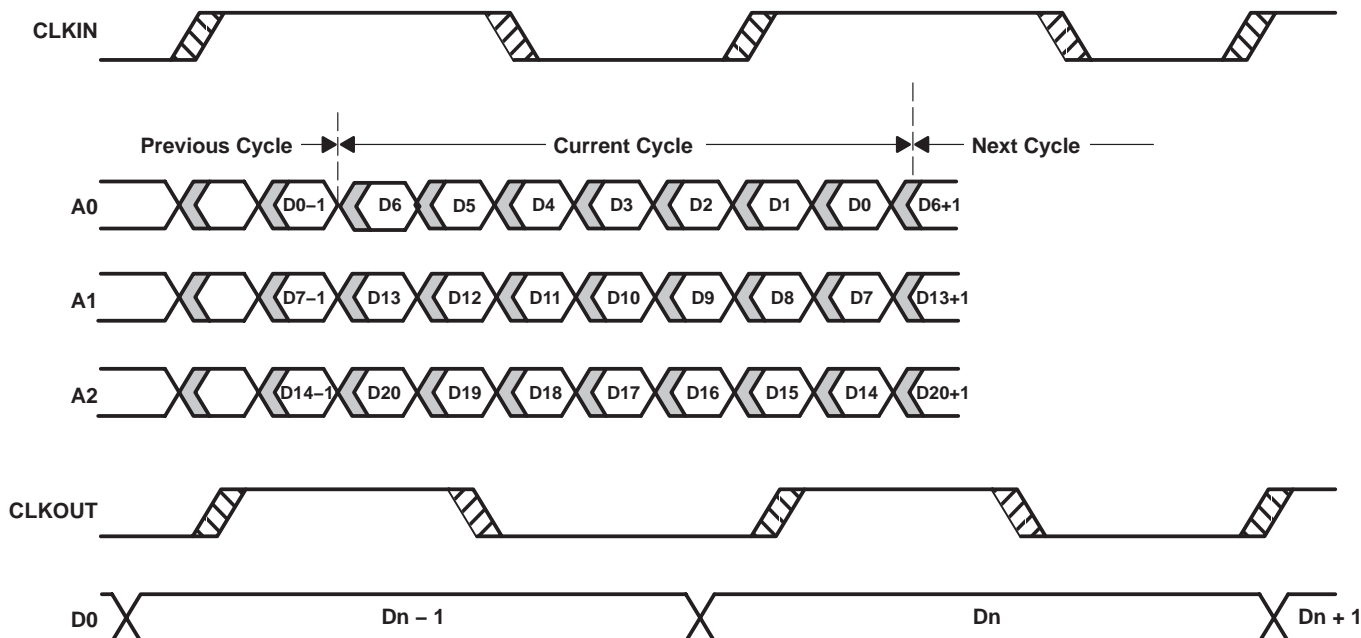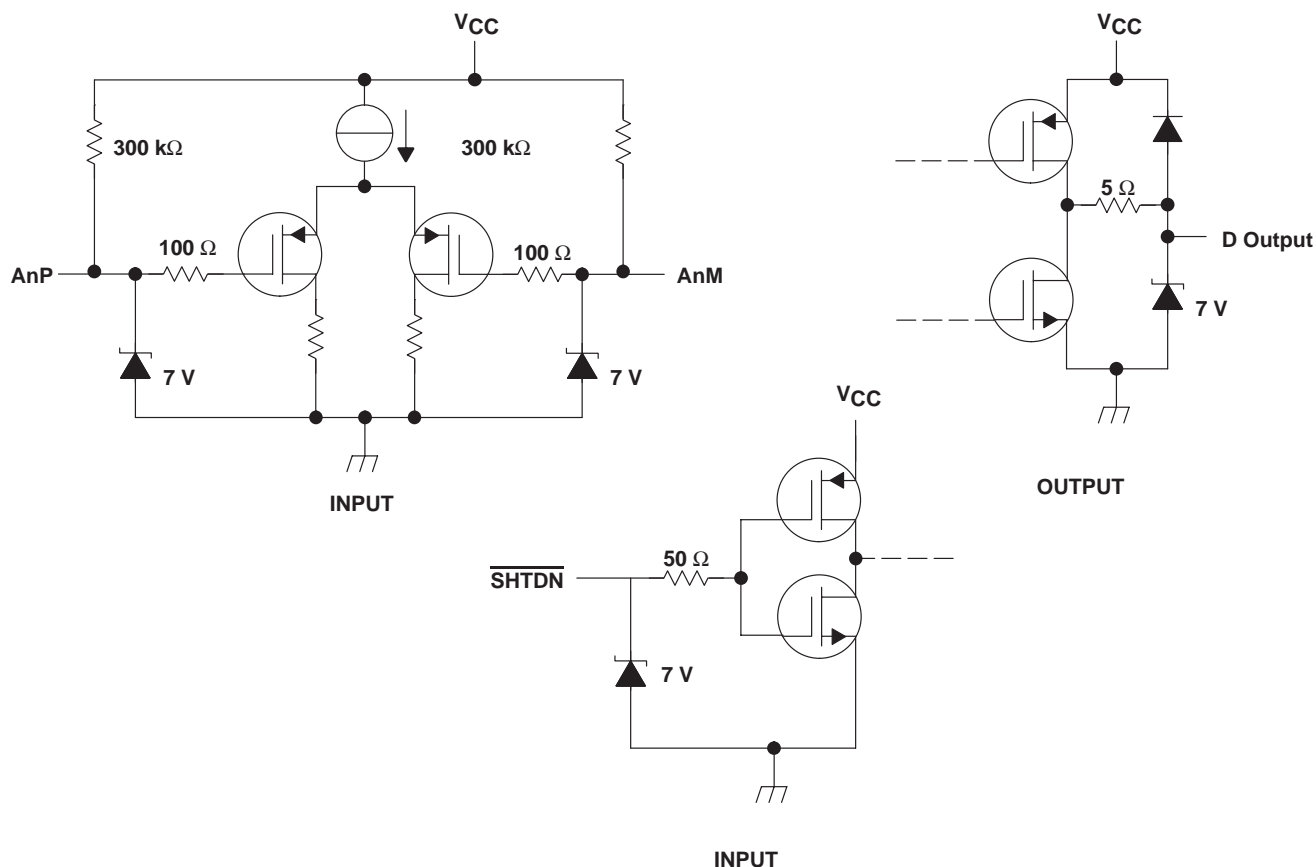
functional block diagram
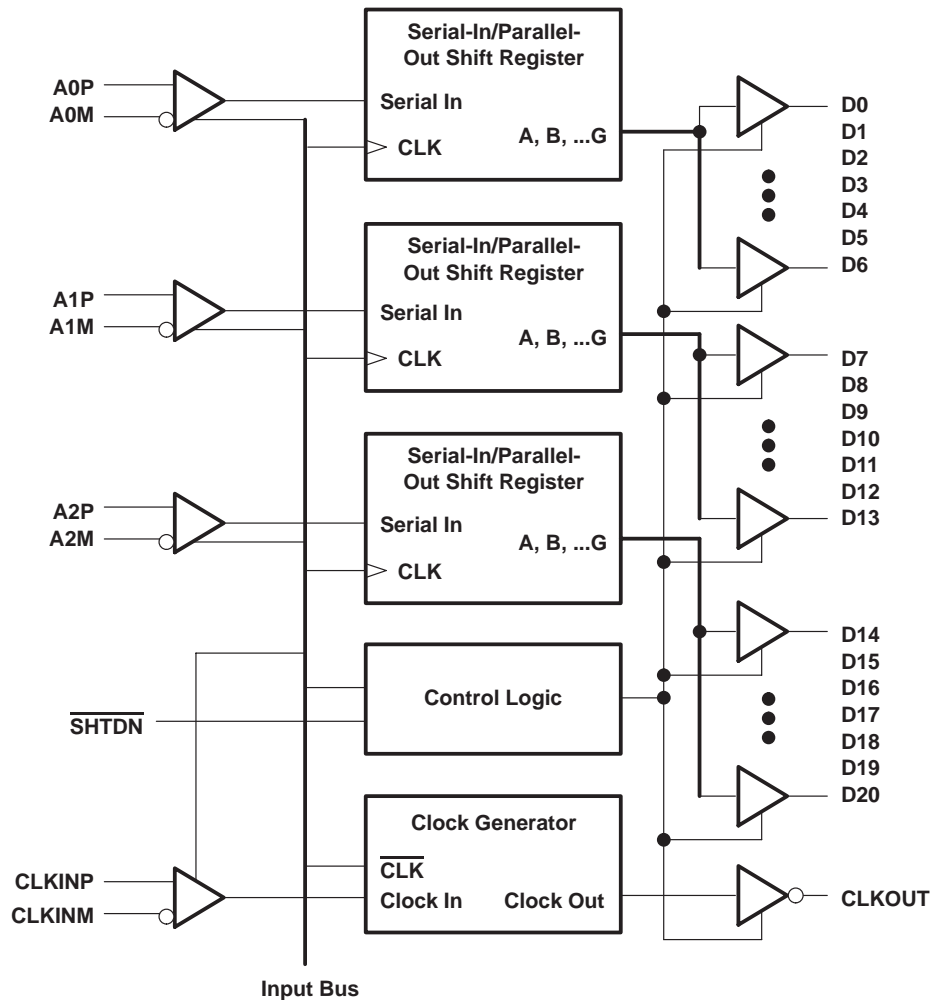
Figure 1. SN65LVDS86A/SN75LVDS86A Load and Shift Timing Sequences

equivalent input and output schematic diagrams

SN65LVDS86A, SN75LVDS86A
FlatLink™ RECEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) .... −0.5 V to 4 V
Voltage range at any terminal .... −0.5 V to V_{CC} + 0.5 V
Electrostatic discharge (see Note 2): All pins (Class 3A) .... 4 KV
                                                          All pins (Class 2B) .... 200 V
Continuous total power dissipation .... See Dissipation Rating Table
Operating virtual junction temperature range, T_J .... −40°C to 150°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1.   All voltage values are with respect to the GND terminals unless otherwise noted.
         2.   This rating is measured using MIL-STD-883C Method, 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DGG	1637 mW	13.1 mW/°C	1048 mW	327 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

recommended operating conditions (see Figure 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH} ($\overline{SHTDN}$)		2			V
Low-level input voltage, V_{IL} ($\overline{SHTDN}$)				0.8	V
Magnitude differential input voltage, $|V_{ID}|$		0.1		0.6	V
Common-mode input voltage, V_{IC}		$\dfrac{|V_{ID}|}{2}$		$2.4 - \dfrac{|V_{ID}|}{2}$	V
Operating free-air temperature, T_A	SN75LVDS86A	0		70	°C
	SN65LVDS86A	−40		125	

timing requirements

	MIN	NOM	MAX	UNIT
Cycle time, input clock, t_c§	14.7	t_c	32.4	ns

§ Parameter t_c is defined as the mean duration of a minimum of 32 000 clock cycles.

electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage					100	mV
V_{IT-}	Negative-going differential input threshold voltage‡			−100			mV
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA		2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA				0.4	V
I_{CC}	Quiescent current (average)	Disabled, All inputs to GND				280	µA
		Enabled, AnP = 1 V, AnM = 1.4 V, t_c = 15.38 ns			33	40	mA
		Enabled, C_L = 8 pF, Grayscale pattern (see Figure 3), t_c = 15.38 ns			43		
		Enabled, C_L = 8 pF, Worst-case pattern (see Figure 4) t_c = 15.38 ns			68		
I_{IH}	High-level input current ($\overline{SHTDN}$)	$V_{IH} = V_{CC}$				±20	µA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	$V_{IL} = 0$	SN75LVDS86A			±20	µA
			SN65LVDS86A			±25	
I_I	Input current A inputs	$0 \le V_I \le 2.4$ V				±20	µA
I_{OZ}	High-impedance output current	$V_O = 0$ or V_{CC}				±10	µA

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{su}	Setup time, D0–D20 to CLKOUT↓	C_L = 8 pF, See Figure 5	5			ns
t_h	Data hold time, CLKOUT↓ to D0–D20		5			ns
$t_{(RSKM)}$	Receiver input skew margin§ (see Figure 7)	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps¶,	550	700		ps
t_d	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	V_{CC} = 3.3 V, t_c = 15.38 ns (±0.2%), T_A = 25°C	3	5	7	ns
t_{en}	Enable time, $\overline{SHTDN}$ to phase lock	See Figure 7		1		ms
t_{dis}	Disable time, $\overline{SHTDN}$ to off state	See Figure 8		400		ns
t_t	Transition time, output (10% to 90% t_r or t_f) (data only)	C_L = 8 pF		3		ns
t_t	Transition time, output (10% to 90% t_r or t_f) (clock only)	C_L = 8 pF		1.5		ns
t_w	Pulse duration, output clock			0.50 t_c		ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ The parameter $t_{(RSKM)}$ is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. The value of this parameter at clock periods other than 15.38 ns can be calculated from $t_{RSKM} = t_c/14 - 550$ ps.
¶ \|Input clock jitter\| is the magnitude of the change in input clock period.
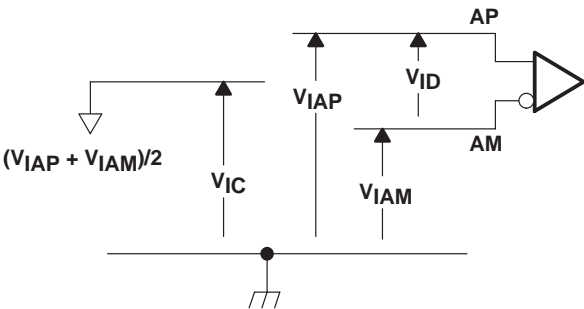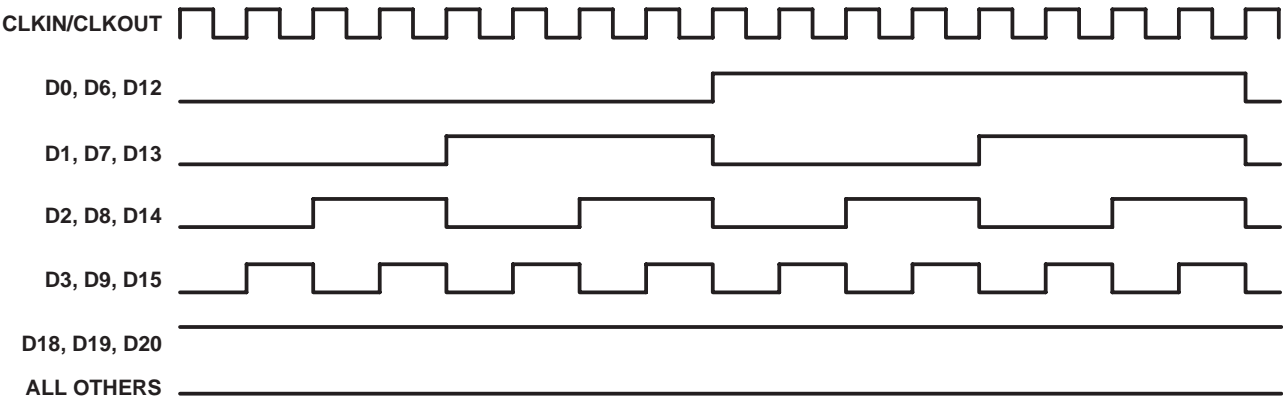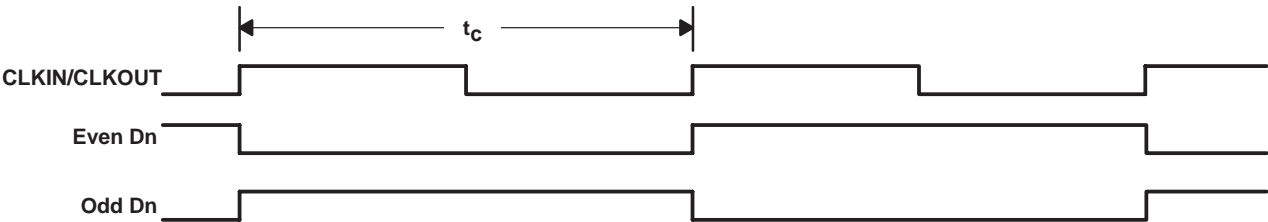
PARAMETER MEASUREMENT INFORMATION

Figure 2. Voltage Definitions

NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern.

Figure 3. 16-Grayscale Test-Pattern Waveforms

NOTE A: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVTTL outputs.

Figure 4. Worst-Case Test-Pattern Waveforms
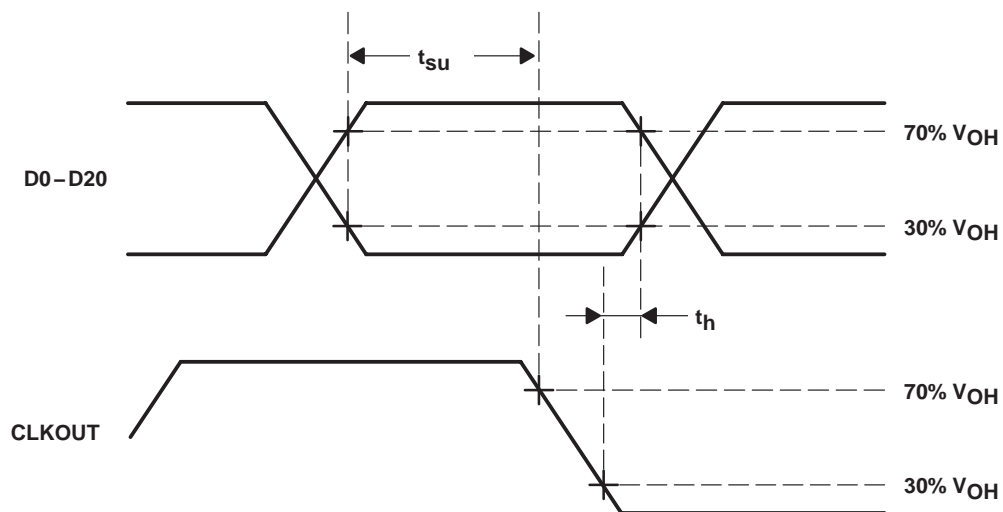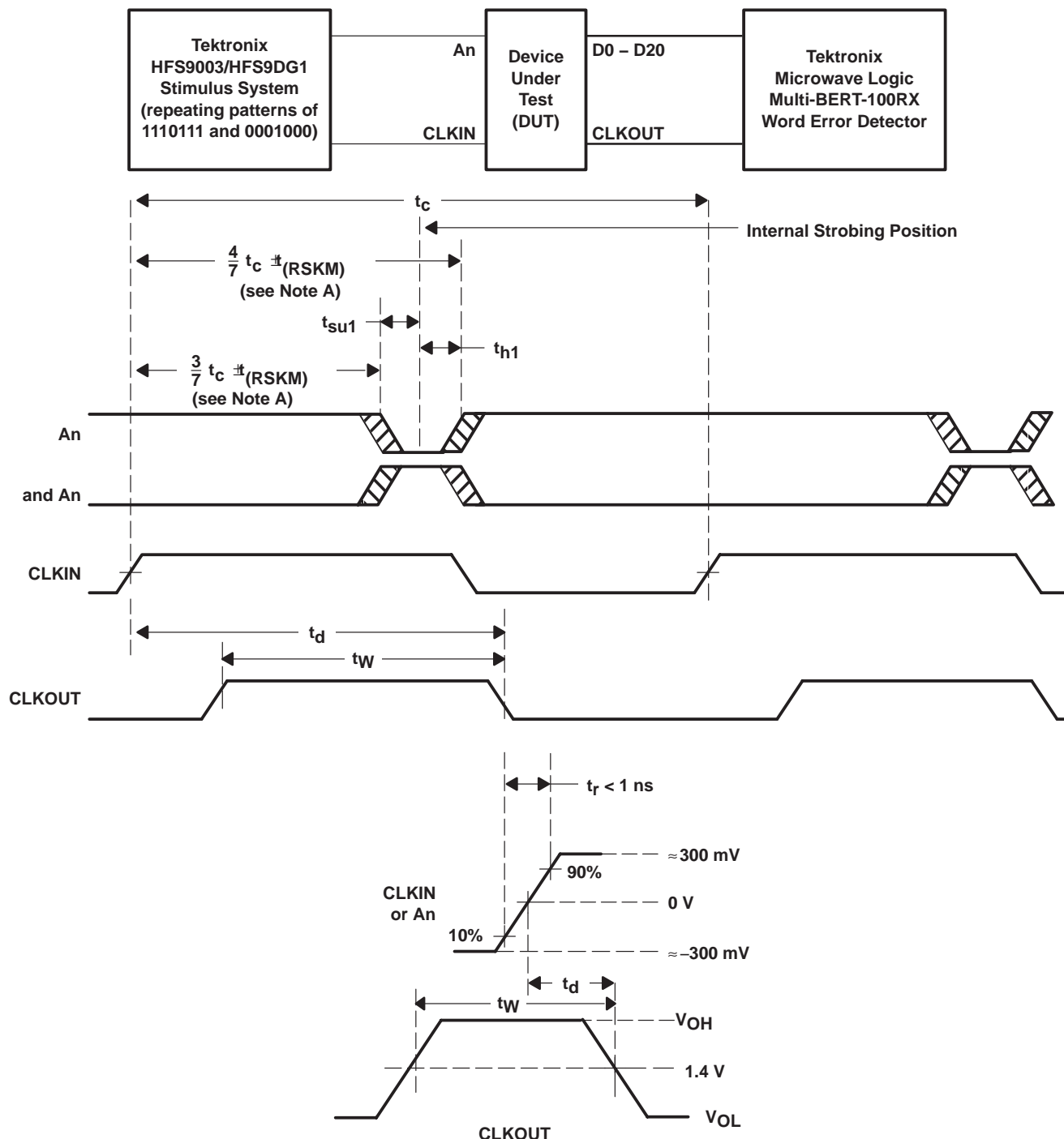
PARAMETER MEASUREMENT INFORMATION

Figure 5. Setup and Hold Time Waveforms

PARAMETER MEASUREMENT INFORMATION

NOTE A: CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is $t_{(RSKM)}$.

Figure 6. Receiver Input Skew Margin, Setup/Hold Time, and Delay Time Definitions
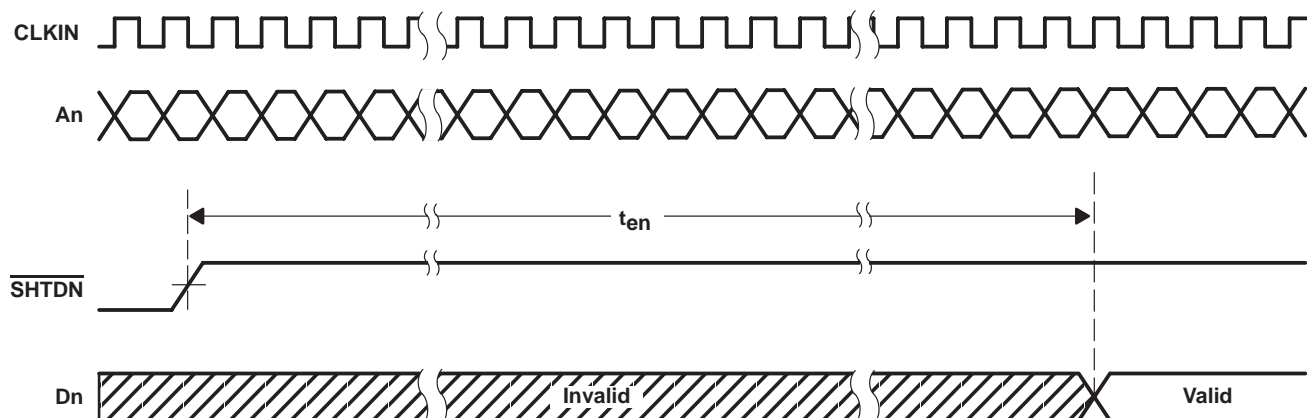
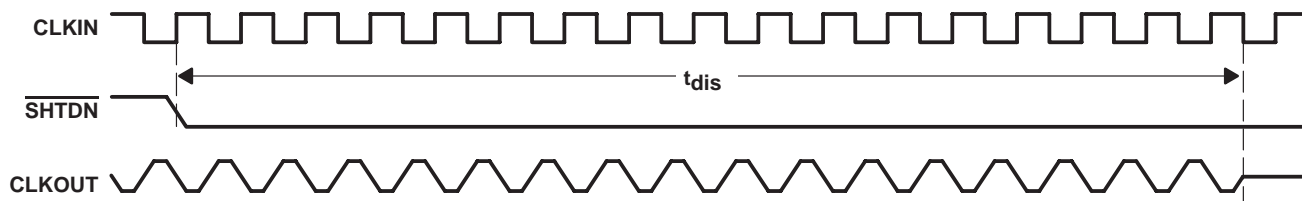## PARAMETER MEASUREMENT INFORMATION

Figure 7. Enable Time Waveforms

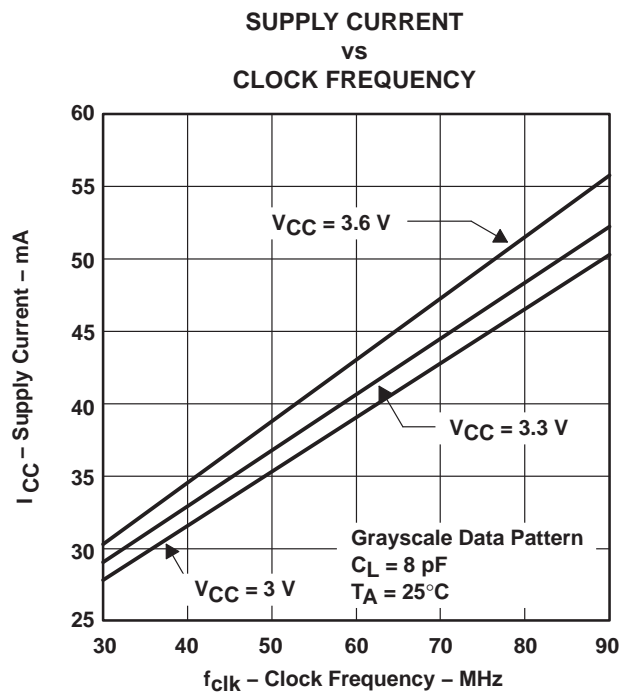**Figure 8. Disable Time Waveforms**

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

Figure 9. RMS Grayscale I$_{CC}$ vs Clock Frequency
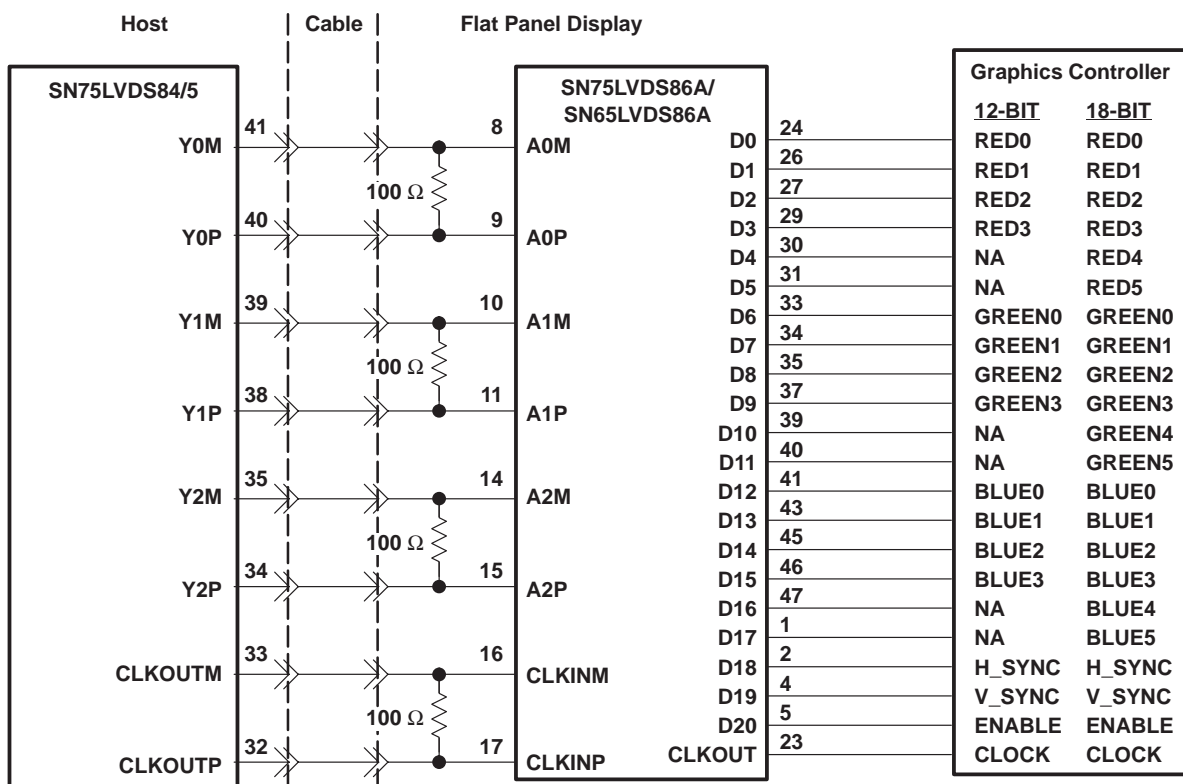
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APPLICATION INFORMATION

Figure 10. 18-Bit Color Host to Flat Panel Display Application

NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
B. NA - not applicable, these unused inputs should be left open.
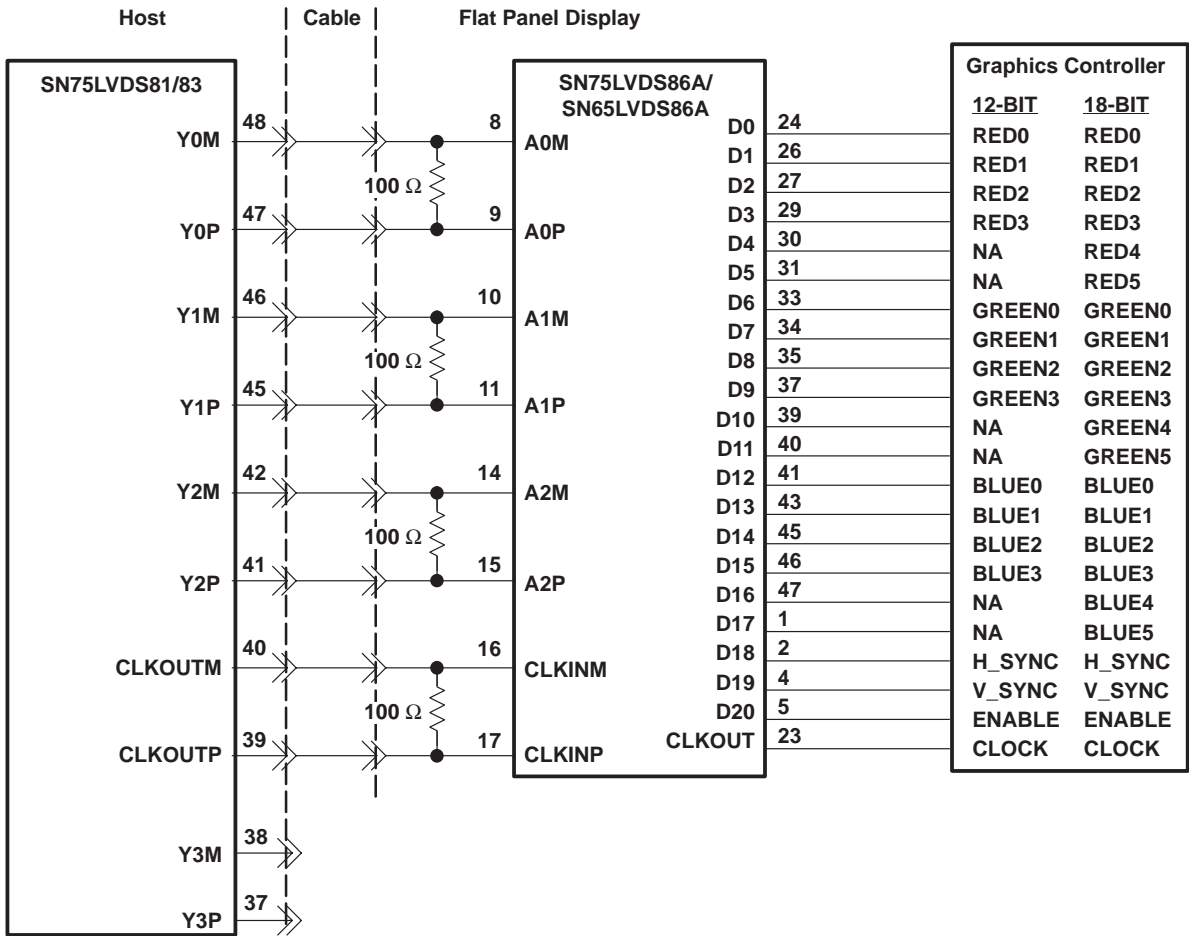
APPLICATION INFORMATION

NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
B. NA - not applicable, these unused inputs should be left open.

Figure 11. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

See the *FlatLink™ Designer's Guide* (SLLA012) for more application information.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS86AQDGG	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ
SN65LVDS86AQDGG.A	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ
SN65LVDS86AQDGGR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ
SN65LVDS86AQDGGR.A	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ
SN75LVDS86ADGG	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS86A
SN75LVDS86ADGG.A	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS86A
SN75LVDS86ADGGR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	SN75LVDS86A
SN75LVDS86ADGGR.A	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS86A
SN75LVDS86ADGGRG4	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	SN75LVDS86A
SN75LVDS86ADGGRG4.A	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS86A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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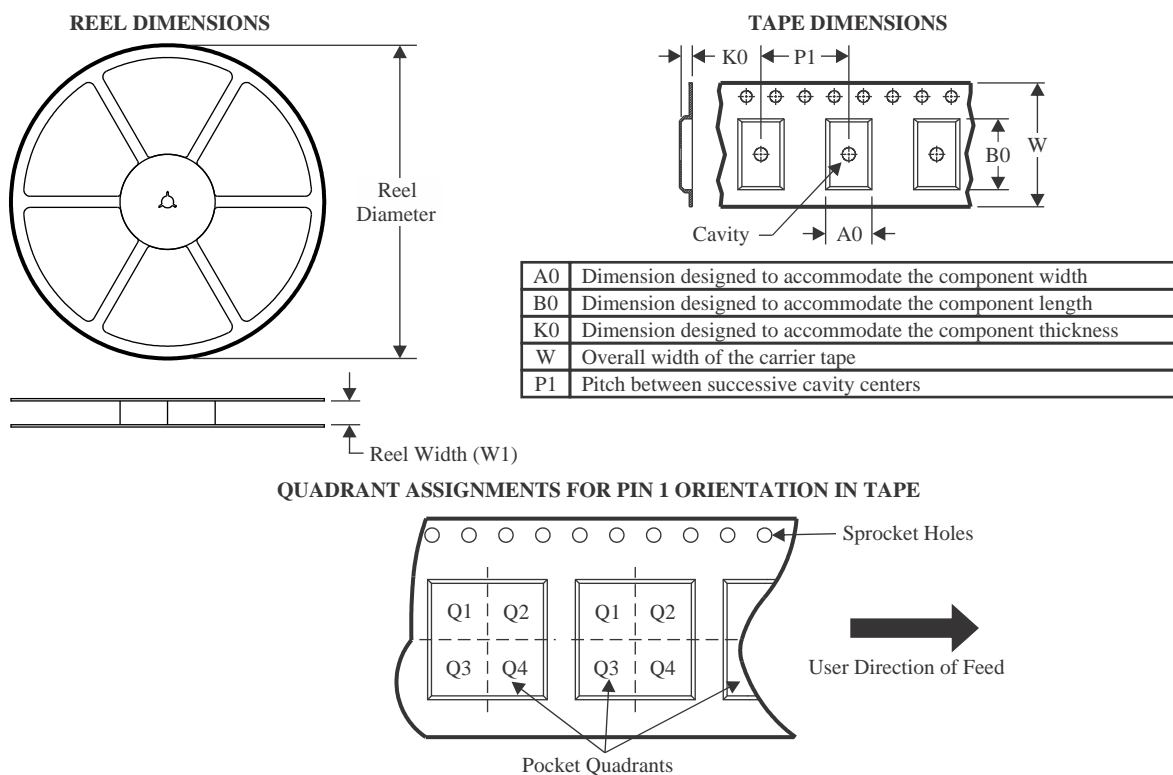
OTHER QUALIFIED VERSIONS OF SN65LVDS86A :

• Automotive : SN65LVDS86A-Q1

NOTE: Qualified Version Definitions:

   • Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS86AQDGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN75LVDS86ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN75LVDS86ADGGRG4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS
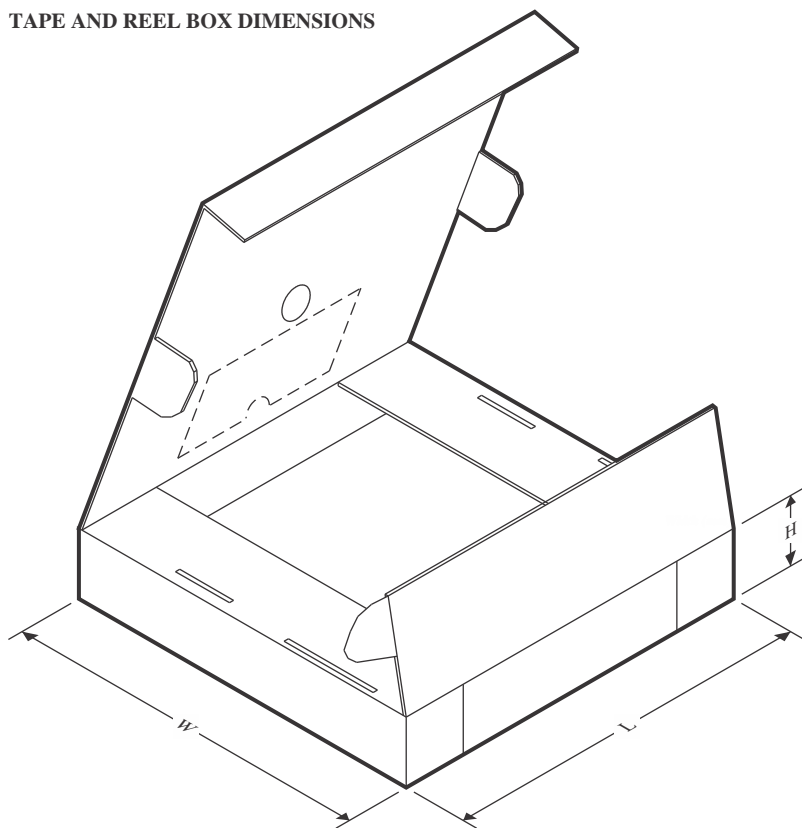
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS86AQDGGR	TSSOP	DGG	48	2000	350.0	350.0	43.0
SN75LVDS86ADGGR	TSSOP	DGG	48	2000	350.0	350.0	43.0
SN75LVDS86ADGGRG4	TSSOP	DGG	48	2000	350.0	350.0	43.0

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS86AQDGG	DGG	TSSOP	48	40	530	11.89	3600	4.9
SN65LVDS86AQDGG.A	DGG	TSSOP	48	40	530	11.89	3600	4.9
SN75LVDS86ADGG	DGG	TSSOP	48	40	530	11.89	3600	4.9
SN75LVDS86ADGG.A	DGG	TSSOP	48	40	530	11.89	3600	4.9

8.3
7.9 TYP

A

PIN 1 ID
AREA

1

46X 0.5

48

12.6
12.4
NOTE 3

2X
11.5

24

25

B

6.2
6.0

48X 0.27
0.17

⊕ 0.08 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

1.2
1.0

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
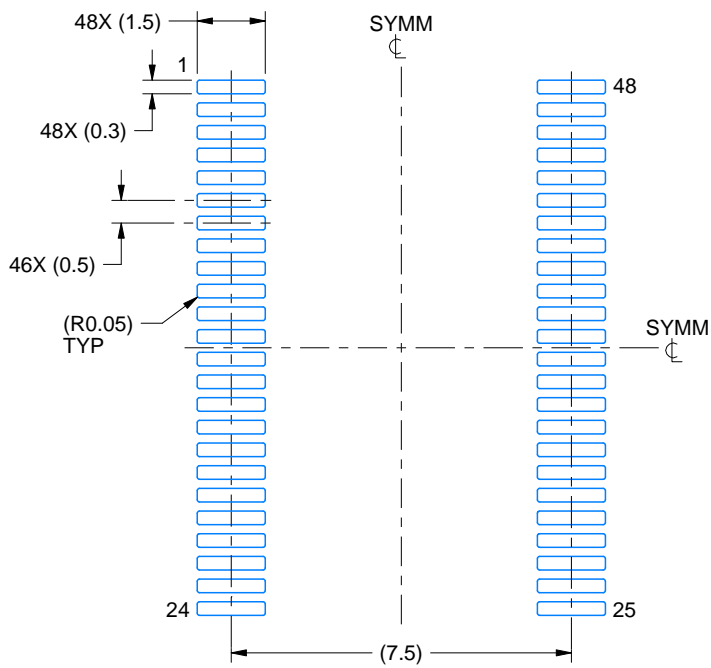TYPICAL
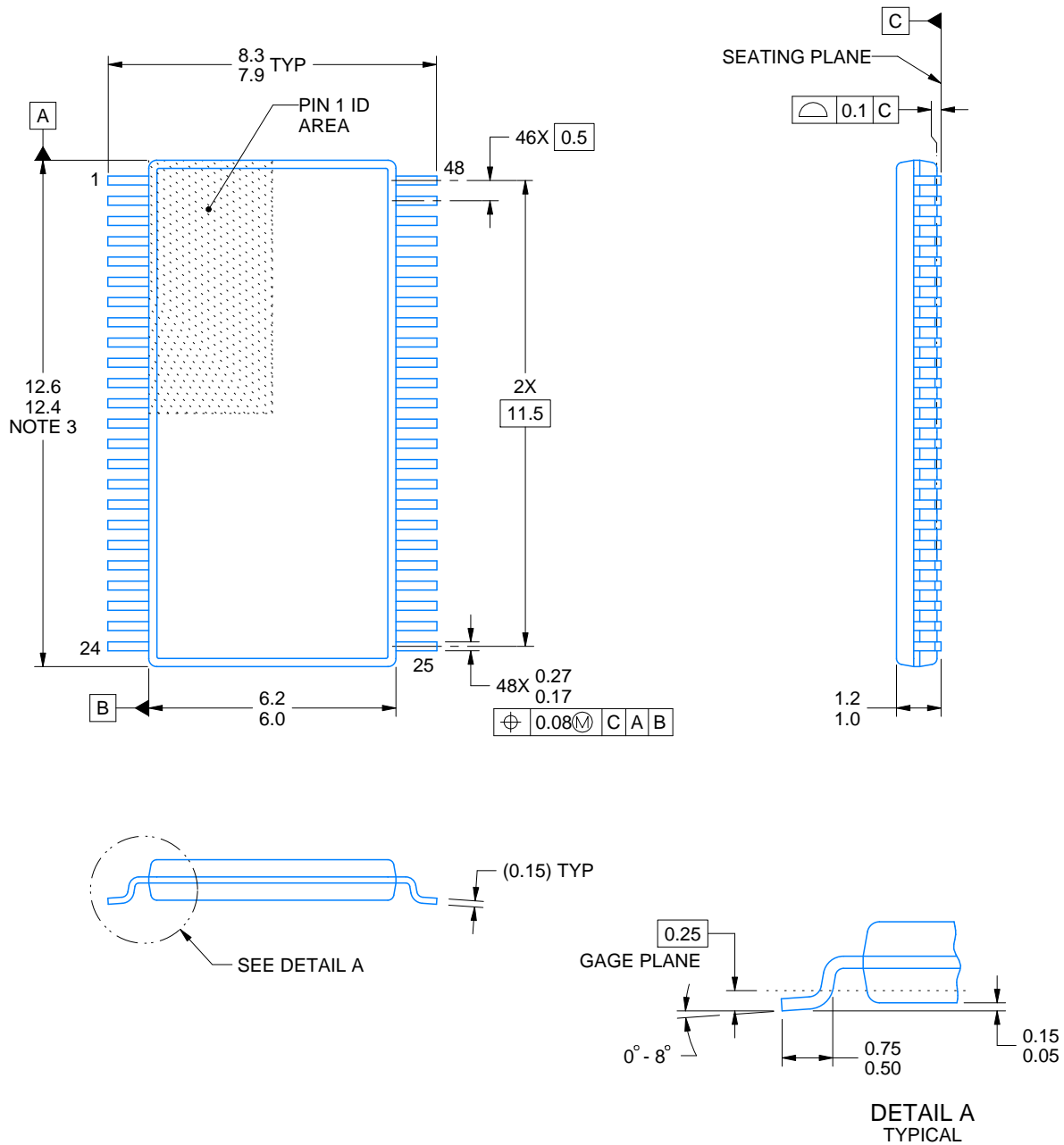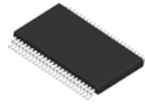
4214859/B   11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
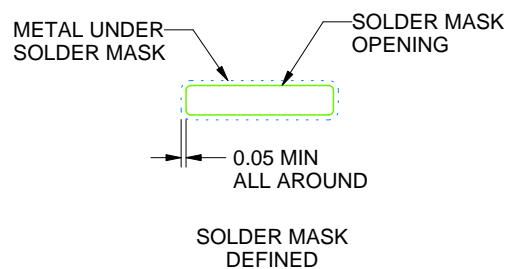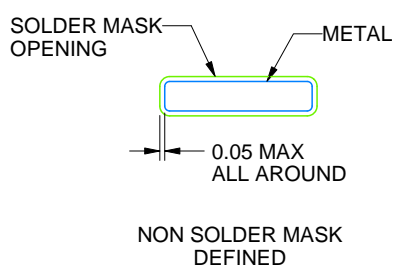4. Reference JEDEC registration MO-153.

DGG0048A

TSSOP - 1.2 mm max height

48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05)
TYP

SYMM

48

SYMM

24

25

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

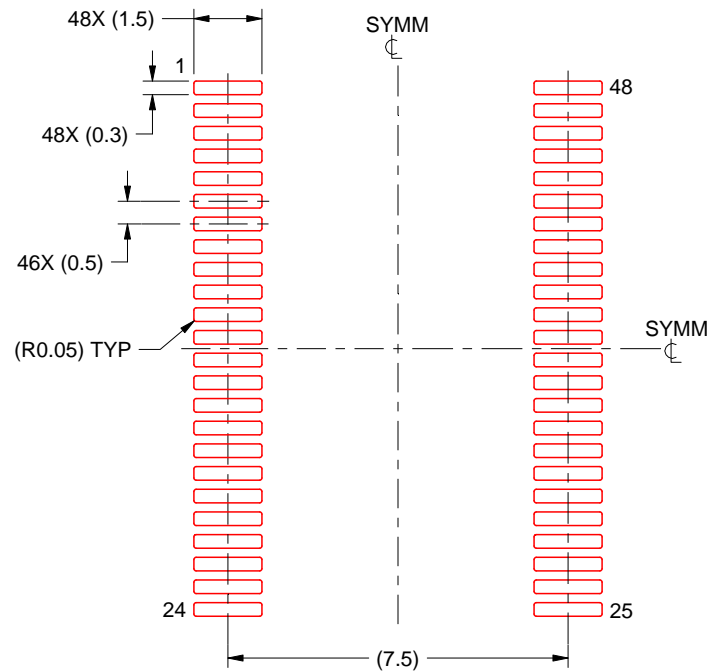4214859/B   11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

48X (1.5)

1

48

48X (0.3)

46X (0.5)

SYMM

SYMM

(R0.05) TYP

24

25

(7.5)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B   11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97
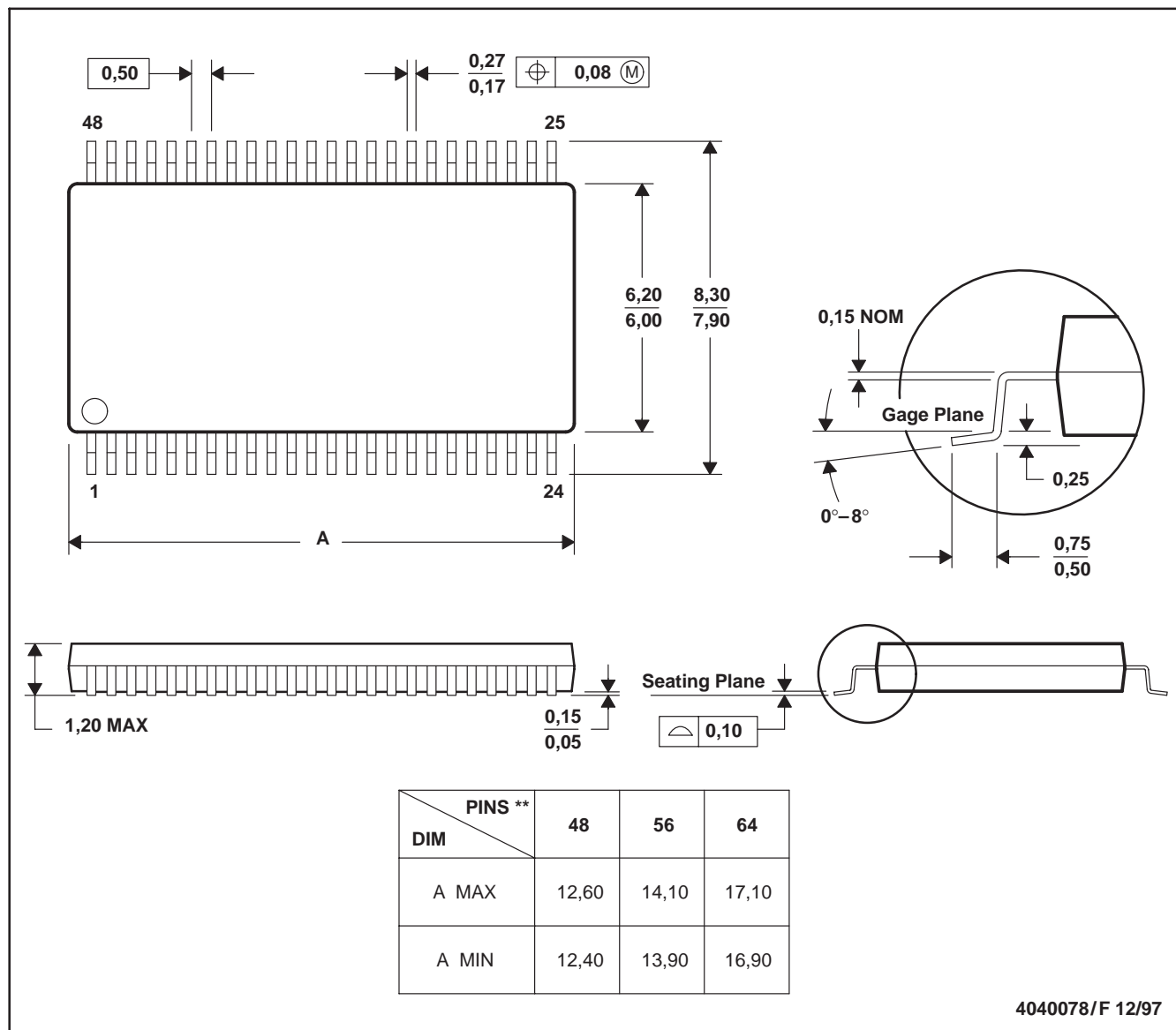
NOTES: A. All linear dimensions are in millimeters.
    B. This drawing is subject to change without notice.
    C. Body dimensions do not include mold protrusion not to exceed 0,15.
    D. Falls within JEDEC MO-153

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