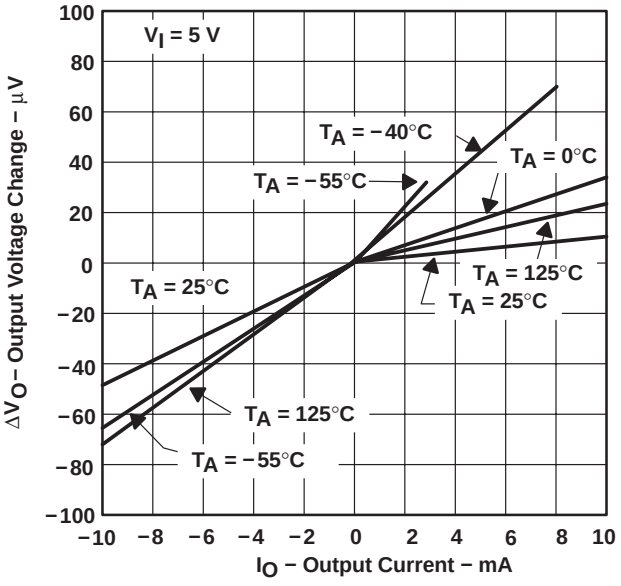
- **2.5-V Virtual Ground for 5-V/GND Analog Systems**
- **High Output-Current Capability Sink or Source . . . 20 mA Typ**
- **Micropower Operation . . . 170 μA Typ**
- **Excellent Regulation Characteristics**
  - **Output Regulation**
    - **−45 μV Typ at I_O = 0 to −10 mA**
    - **+15 μV Typ at I_O = 0 to +10 mA**
  - **Input Regulation = 1.5 μV/V Typ**
- **Low-Impedance Output . . . 0.0075 Ω Typ**
- **Macromodel Included**

description

In signal-conditioning applications using a single power source, a reference voltage is required for termination of all signal grounds. To accomplish this, engineers have typically used solutions consisting of resistors, capacitors, operational amplifiers, and voltage references. Texas Instruments has eliminated all of those components with one easy-to-use 3-terminal device. That device is the TLE2425 precision virtual ground.

Use of the TLE2425 over other typical circuit solutions gives the designer increased dynamic signal range, improved signal-to-noise ratio, lower distortion, improved signal accuracy, and easier interfacing to ADCs and DACs. These benefits are the result of combining a precision micropower voltage reference and a high-performance precision operational amplifier in a single silicon chip. It is the precision and performance of these two circuit functions together that yield such dramatic system-level performance.

OUTPUT REGULATION



The TLE2425 improves input regulation as well as output regulation and, in addition, reduces output impedance and power dissipation in a majority of virtual-ground-generation circuits. Both input regulation and load regulation exceed 12 bits of accuracy on a single 5-V system. Signal-conditioning front ends of data acquisition systems that push 12 bits and beyond can use the TLE2425 to eliminate a major source of system error.

AVAILABLE OPTIONS

T_A	SMALL OUTLINE (D)	PLASTIC TO-226AA (LP)
0°C to 70°C	TLE2425CD	TLE2425CD
−40°C to 85°C	TLE2425ID	TLE2425ID
−55°C to 125°C	TLE2425MD	—

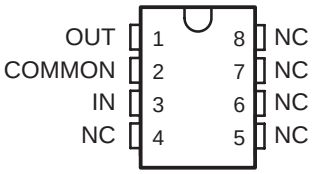
† The D package is available taped and reeled. Add R suffix to the device type (e.g., TLE2425CDR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

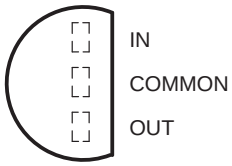
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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D, OR JG PACKAGE
(TOP VIEW)



LP PACKAGE
(TOP VIEW)



NC − No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Continuous input voltage, V_I . . . . . 40 V
Output current, I_O . . . . . ±80 mA
Duration of short-circuit current at (or below) 25°C (see Note 1) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . −40°C to 85°C
M-suffix . . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or LP package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mV	5.8 mW/°C	464 mW	377 mW	145 mW
JG	1050 mV	8.4 mW/°C	672 mW	546 mW	210 mW
LP	775 mV	6.2 mW/°C	496 mW	403 mW	155 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	4	40	4	40	4	40	V
Operating free-air temperature, T_A	0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2425C			UNIT
				MIN	TYP	MAX	
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	I_O = 0		25°C		170	250	µA
			Full range			250	
Input voltage regulation	V_I = 4.5 V to 5.5 V		25°C		1.5	20	µV
			Full range			25	
	V_I = 4 V to 40 V		25°C		1.5	20	µV/V
			Full range			25	
Ripple rejection	f = 120 Hz,	$\Delta V_{I(PP)}$ = 1 V	25°C		80		dB
Output voltage regulation (source current)‡	I_O = 0 to −10 mA		25°C	−160	−45	160	µV
			Full range	−250		250	
	I_O = 0 to −20 mA		25°C	−450	−150	450	
Output voltage regulation (sink current)‡	I_O = 0 to 10 mA		25°C	−160	15	160	µV
			Full range	−250		250	
	I_O = 0 to 20 mA		25°C	−235	65	235	
Long-term drift of output voltage	Δt = 1000 h,	Noncumulative	25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current (sink current)	V_O = 5 V		25°C	30	55		mA
Short-circuit output current (source current)	V_O = 0			−30	−50		
Output noise voltage, rms	f = 10 Hz to 10 kHz		25°C		100		µV
Output voltage response to output current step	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		110		µs
		C_L = 100 pF			115		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0			180		
		C_L = 100 pF			180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V,	V_O to 0.1%	25°C		12		µs
	V_I = 4.5 to 5.5 V,	V_O to 0.01%			30		
Output voltage turn-on response	V_I = 0 to 5 V,	V_O to 0.1%	25°C		125		µs
	V_I = 0 to 5 V,	V_O to 0.01%			210		

† Full range is 0°C to 70°C.
‡ The listed values are not production tested.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2425I			UNIT
				MIN	TYP	MAX	
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	I_O = 0		25°C		170	250	µA
			Full range			250	
Input voltage regulation	V_I = 4.5 V to 5.5 V		25°C		1.5	20	µV
			Full range			75	
	V_I = 4 V to 40 V		25°C		1.5	20	µV/V
			Full range			75	
Ripple rejection	f = 120 Hz,	$\Delta V_{I(PP)}$ = 1 V	25°C		80		dB
Output voltage regulation (source current)‡	I_O = 0 to −10 mA		25°C	−160	−45	160	µV
			Full range	−250		250	
	I_O = 0 to −20 mA		25°C	−450	−150	450	
Output voltage regulation (sink current)‡	I_O = 0 to 8 mA		25°C	−160	15	160	µV
			Full range	−250		250	
	I_O = 0 to 20 mA		25°C	−235	65	235	
Long-term drift of output voltage	Δt = 1000 h,	Noncumulative	25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current (sink current)	V_O = 5 V		25°C	30	55		mA
Short-circuit output current (source current)	V_O = 0			−30	−50		
Output noise voltage, rms	f = 10 Hz to 10 kHz		25°C		100		µV
Output voltage response to output current step	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		110		µs
		C_L = 100 pF			115		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0			180		
		C_L = 100 pF			180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V,	V_O to 0.1%	25°C		12		µs
	V_I = 4.5 to 5.5 V,	V_O to 0.01%			30		
Output voltage turn-on response	V_I = 0 to 5 V,	V_O to 0.1%	25°C		125		µs
	V_I = 0 to 5 V,	V_O to 0.01%			210		

† Full range is −40°C to 85°C.
‡ The listed values are not production tested.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2425M			UNIT
				MIN	TYP	MAX	
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	I_O = 0		25°C		170	250	µA
			Full range			250	
Input voltage regulation	V_I = 4.5 V to 5.5 V		25°C		1.5	20	µV
			Full range			100	
	V_I = 4.5 V to 40 V		25°C		1.5	20	µV/V
			Full range			100	
Ripple rejection	f = 120 Hz,	$\Delta V_{I(PP)}$ = 1 V	25°C		80		dB
Output voltage regulation (source current)‡	I_O = 0 to −10 mA		25°C	−160	−45	160	µV
			Full range	−250		250	
	I_O = 0 to −20 mA		25°C	−450	−150	450	
Output voltage regulation (sink current)‡	I_O = 0 to 3 mA		25°C	−160	15	160	µV
			Full range	−250		250	
	I_O = 0 to 20 mA		25°C	−235	65	235	
Long-term drift of output voltage	Δt = 1000 h,	Noncumulative	25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current (sink current)	V_O = 5 V		25°C	30	55		mA
Short-circuit output current (source current)	V_O = 0			−30	−50		
Output noise voltage, rms	f = 10 Hz to 10 kHz		25°C		100		µV
Output voltage response to output current step	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		110		µs
		C_L = 100 pF			115		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0			180		
		C_L = 100 pF			180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V,	V_O to 0.1%	25°C		12		µs
	V_I = 4.5 to 5.5 V,	V_O to 0.01%			30		
Output voltage turn-on response	V_I = 0 to 5 V,	V_O to 0.1%	25°C		125		µs
	V_I = 0 to 5 V,	V_O to 0.01%			210		

† Full range is −55°C to 125°C.
‡ The listed values are not production tested.

TYPICAL CHARACTERISTICS

Table Of Graphs

		FIGURE
Output voltage	Distribution	1
	vs Free-air temperature	2
Output voltage hysteresis	vs Free-air temperature	3
Input bias current	vs Input voltage	4
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Input voltage regulation		6
Ripple rejection	vs Frequency	7
Output voltage regulation		8
Output impedance	vs Frequency	9
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Spectral noise voltage density	vs Frequency	11
Wide-band noise voltage	vs Frequency	12
Output voltage change with current step	vs Time	13
Output voltage change with voltage step	vs Time	14
Output voltage power-up response	vs Time	15
Output current	vs Load capacitance	16

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF OUTPUT VOLTAGE

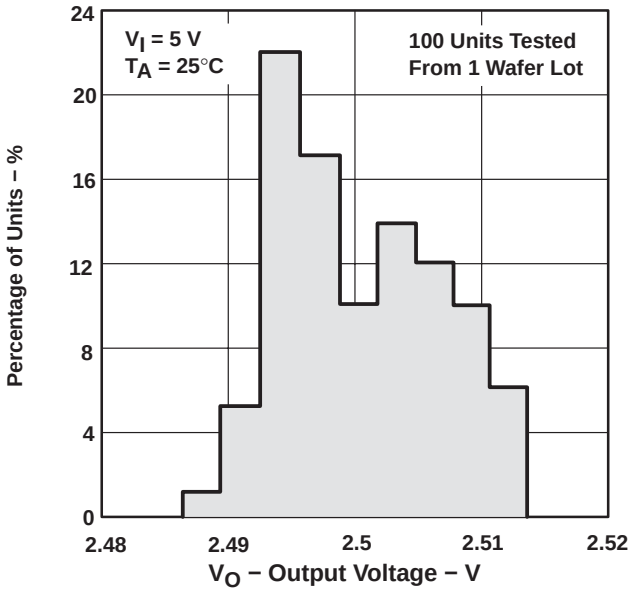


Figure 1

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

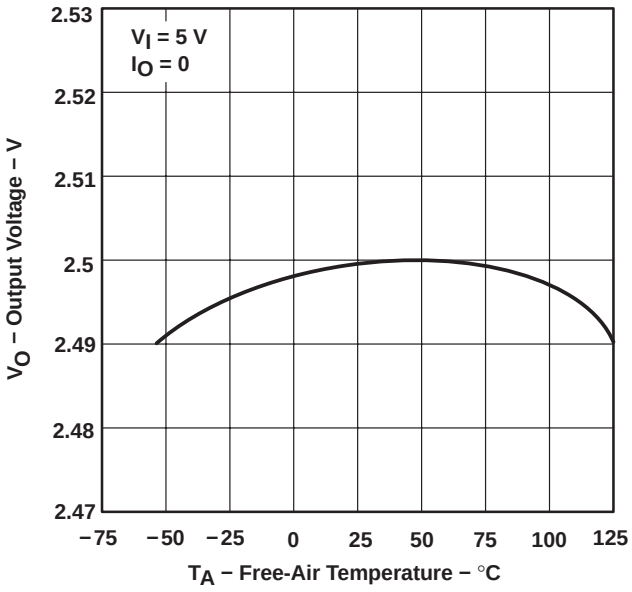


Figure 2

OUTPUT VOLTAGE HYSTERESIS vs FREE-AIR TEMPERATURE

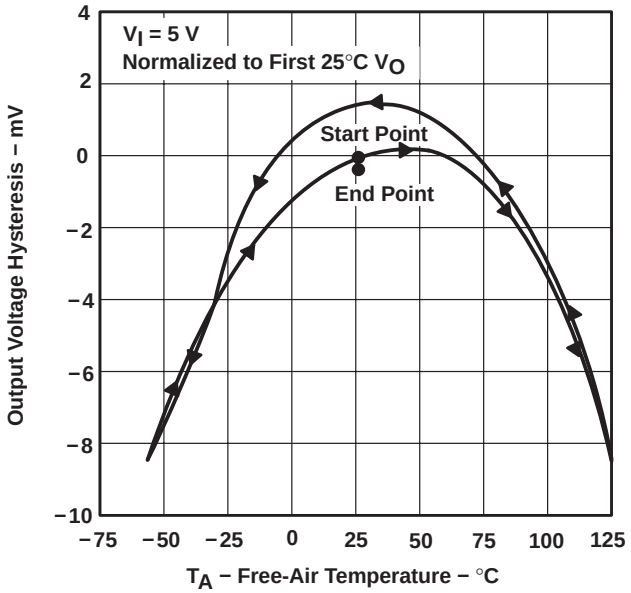


Figure 3

INPUT BIAS CURRENT vs INPUT VOLTAGE

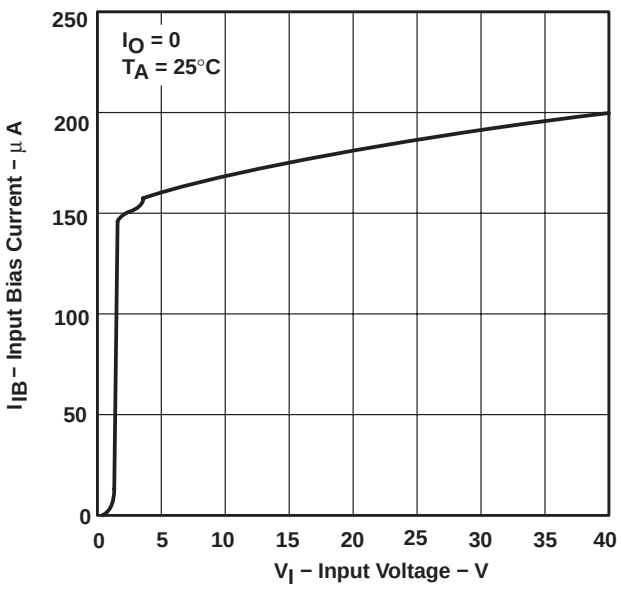


Figure 4

† Data at high and low temperatures are applicable within rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

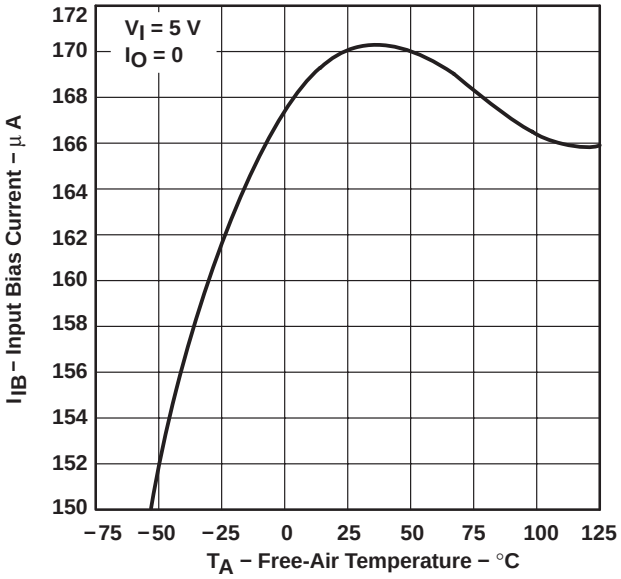


Figure 5

INPUT VOLTAGE REGULATION

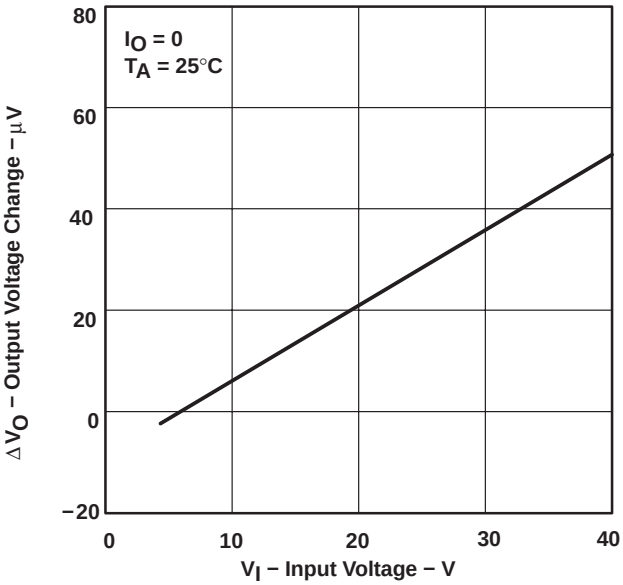


Figure 6

RIPPLE REJECTION vs FREQUENCY

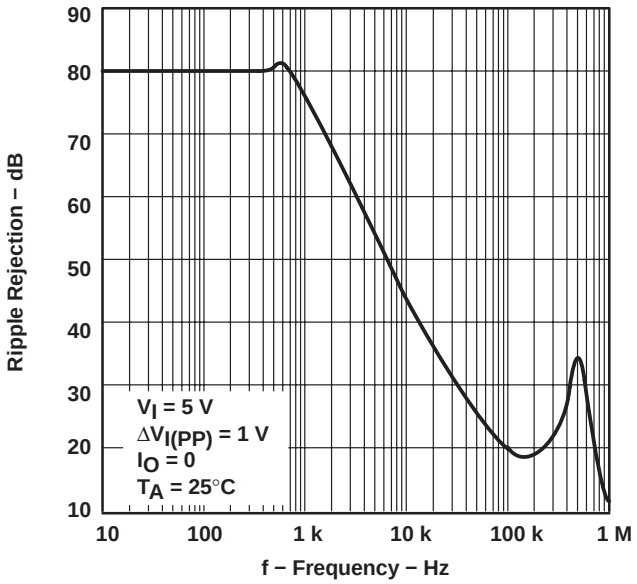


Figure 7

OUTPUT VOLTAGE REGULATION

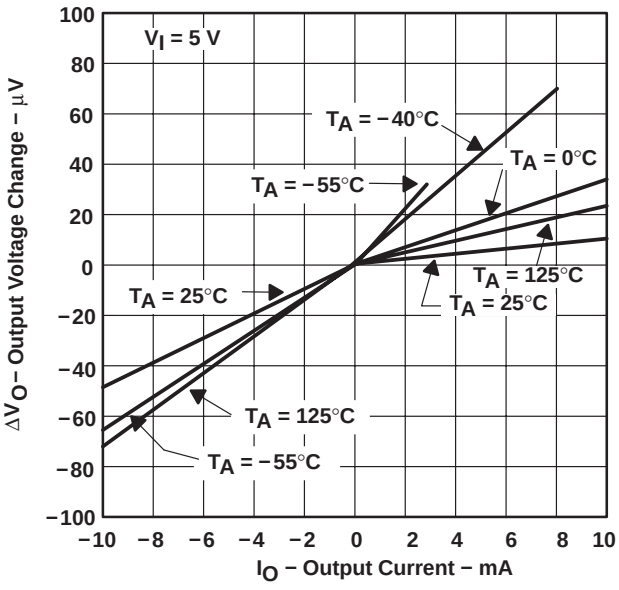


Figure 8

† Data at high and low temperatures are applicable within rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

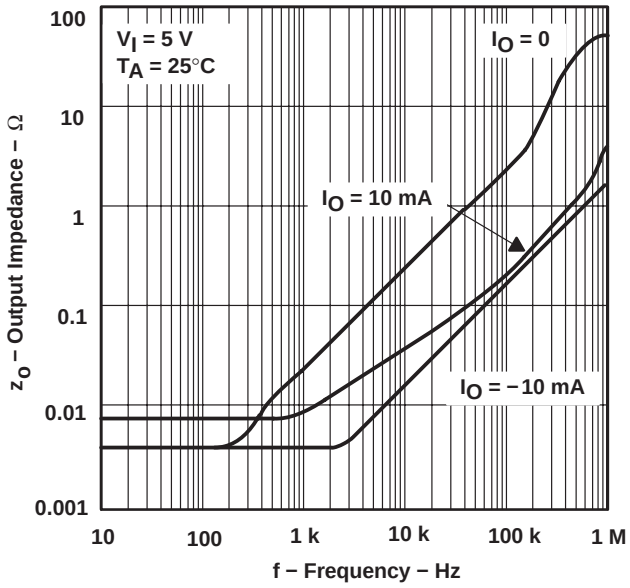


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

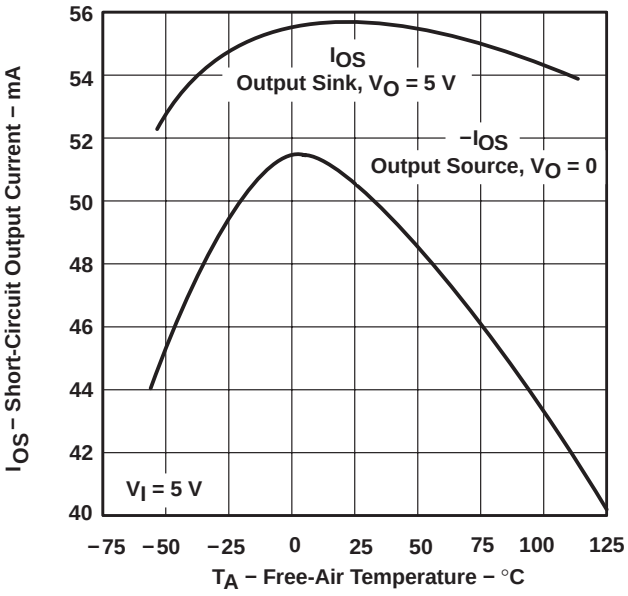


Figure 10

SPECTRAL NOISE VOLTAGE DENSITY vs FREQUENCY

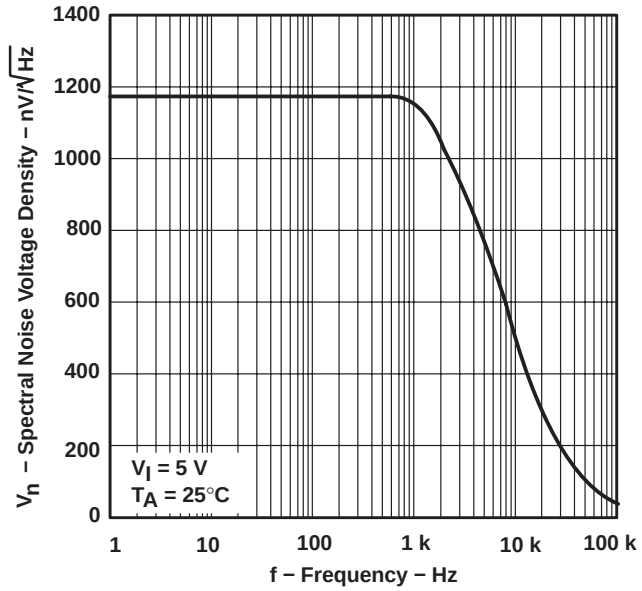


Figure 11

WIDE-BAND NOISE VOLTAGE vs FREQUENCY

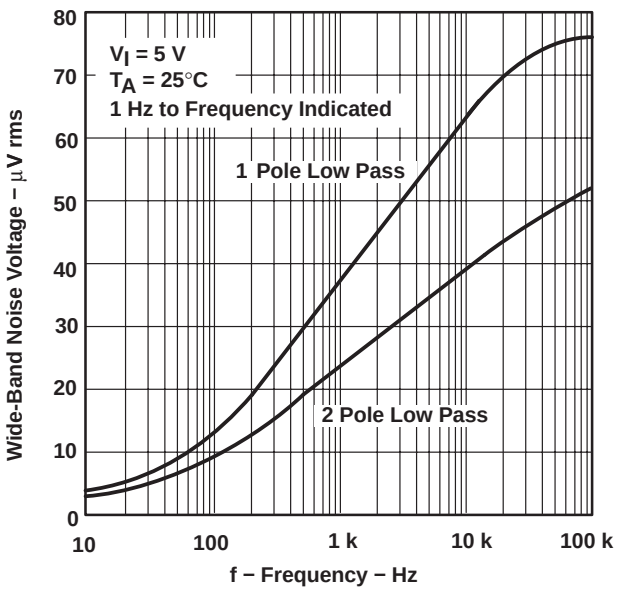


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE TO OUTPUT CURRENT STEP vs TIME

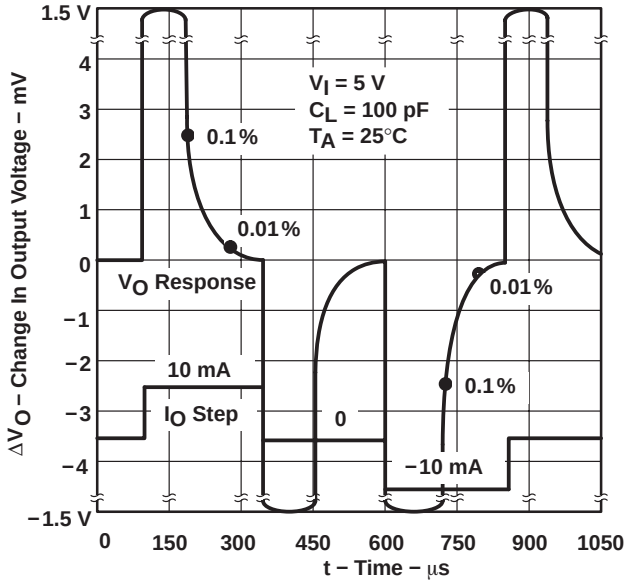


Figure 13

OUTPUT VOLTAGE RESPONSE TO INPUT VOLTAGE STEP vs TIME

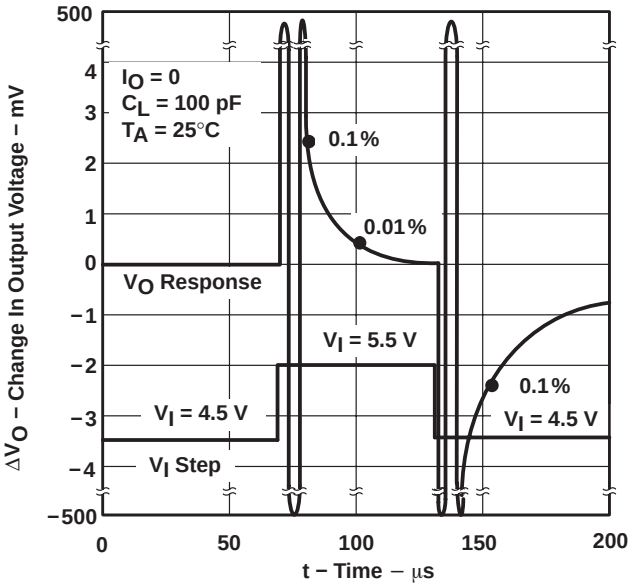


Figure 14

OUTPUT VOLTAGE POWER-UP RESPONSE vs TIME

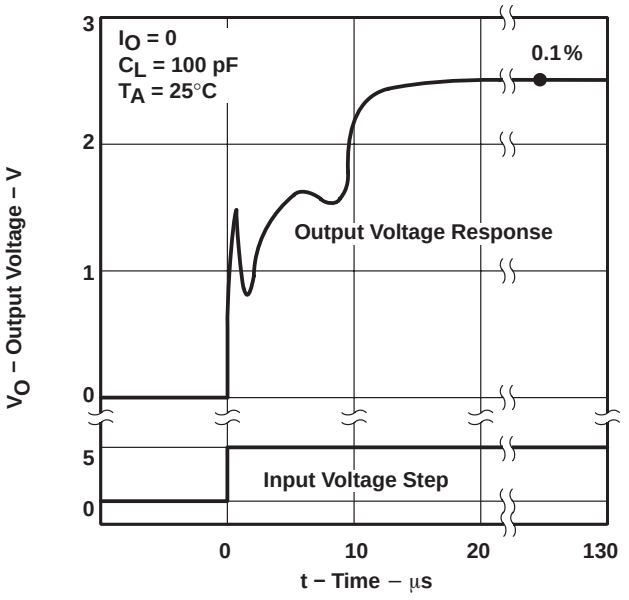


Figure 15

STABILITY RANGE OUTPUT CURRENT vs LOAD CAPACITANCE

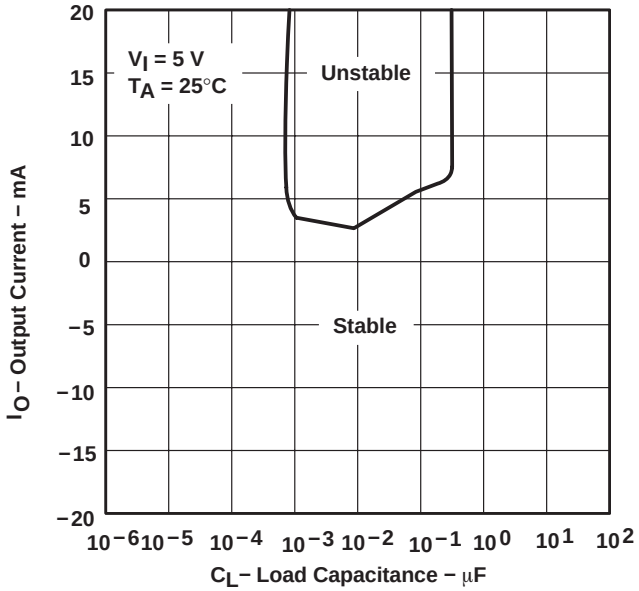


Figure 16

macromodel information

```
*   TLE2425 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
*   CREATED USING PARTS RELEASE 4.03 ON 08/21/90 AT 13:51
*   REV (N/A)     SUPPLY VOLTAGE: 5 V
*   CONNECTIONS:  INPUT
*                 |   COMMON
*                 |   |   OUTPUT
*                 |   |   |
.SUBCKT TLE2425   3   4   5
*
```

```
*   OPAMP SECTION
    C1     11  12  21.66E-12
    C2      6  7   30.00E-12
    C3     87  0   10.64E-9
    CPSR   85  86  15.9E-9
    DCM+   81  82  DX
    DCM-   83  81  DX
    DC      5  53  DX
    DE     54  5   DX
    DLN    92  90  DX
    DLP    90  91  DX
    DP      4  3   DX
    ECMR   84  99  (2,99) 1
    EGND   99  0   POLY(2)   (3,0)  (4,0)  0   .5 .5
    EPSR   85  0   POLY(1)   (3,4)  -16.22E-6 3.24E-6
    ENSE   89  2   POLY(1)   (88,0) 120E-6 1
    FB      7  99  POLY(6)   VB  VC  VE  VLP VLN VPSR   0   74.8E6 -10E6  10E6   10E6
+   -10E6  74E6
    GA      6  0   11  12  320.4E-6
    GCM     0  6   10  99  1.013E-9
    GPSR   85  86  (85,86)   100E-6
    GRC1   4   11  (4,11) 3.204E-4
    GRC2   4   12  (4,12) 3.204E-4
    GRE1   13  10  (13,10)   1.038E-3
    GRE2   14  10  (14,10)   1.038E-3
    HLIM   90  0   VLIM   1K
    HCMR   80  1   POLY(2)   VCM+   VCM-   0   1E2 1E2
    IRP     3  4   146E-6
    IEE     3  10  DC  24.05E-6
    IIO     2  0   .2E-9
    I1     88  0   1E-21
    Q1     11  89  13  QX
    Q2     12  80  14  QX
    R2      6  9   100.0E3
    RCM    84  81  1K
    REE    10  99  8.316E6
    RN1    87  0   2.55E8
    RN2    87  88  11.67E3
```

macromodel information (continued)

```
        RO1     8  5   63
        RO2     7  99  62
        VCM+   82  99  1.0
        VCM-   83  99  -2.3
        VB      9  0   DC  0
        VC      3  53  DC  1.400
        VE     54  4   DC  1.400
        VLIM    7  8   DC  0
        VLP    91  0   DC  30
        VLN     0  92  DC  30
        VPSR    0  86  DC  0
        RFB     5  2   1K
        RIN    30  1   1K
        RCOM   34  4   .1
    *REGULATOR SECTION
        RG1    30  0   20MEG
        RG2    30  31  .2
        RG3    31  35  400K
        RG4    35  34  411K
        RG5    31  36  25MEG
        HREG   31  32  POLY(2)   VPSET  VNSET  0   1E2 1E2
        VREG   32  33  DC  0V
        EREG   33  34  POLY(1)   (36,34)   1.23 1
        VADJ   36  34  1.27V
        HPSET  37  0   VREG   1.030E3
        VPSET  38  0   DC  20V
        HNSET  39  0   VREG   6.11E5
        VNSET  40  0   DC  -20V
        DSUB    4  34  DX
        DPOS   37  38  DX
        DNNEG  40  39  DX
    .MODEL DX  D(IS=800.0E-18)
    .MODEL QX  PNP(IS=800.0E-18 BF=480)
    .ENDS
```

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2425CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2425C	
TLE2425CDR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2425C	
TLE2425CLP	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type		2425C	
TLE2425CPS	LIFEBUY	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		Q2425	
TLE2425CPSR	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		Q2425	
TLE2425ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2425I	
TLE2425IDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2425I	
TLE2425IDR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2425I	
TLE2425ILP	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type		2425I	
TLE2425MD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2425M	
TLE2425MDRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2425M	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

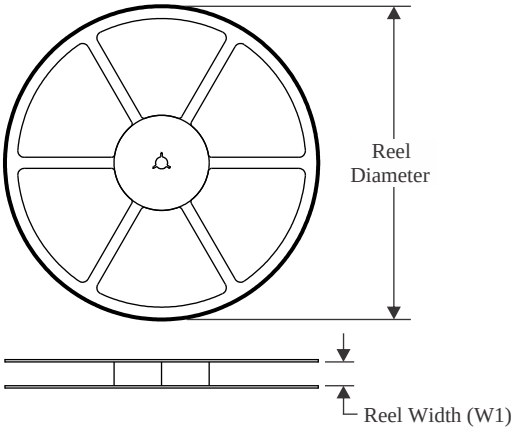
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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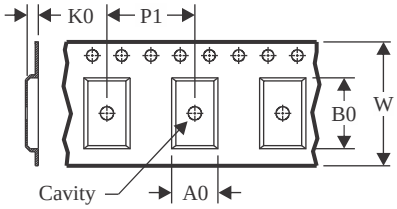
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

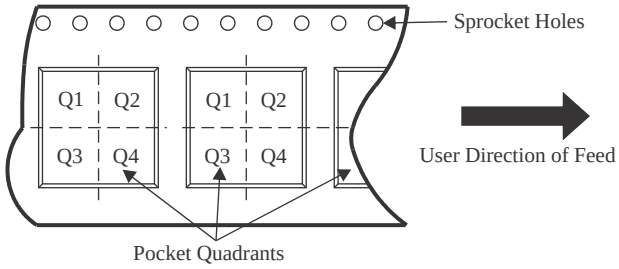


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

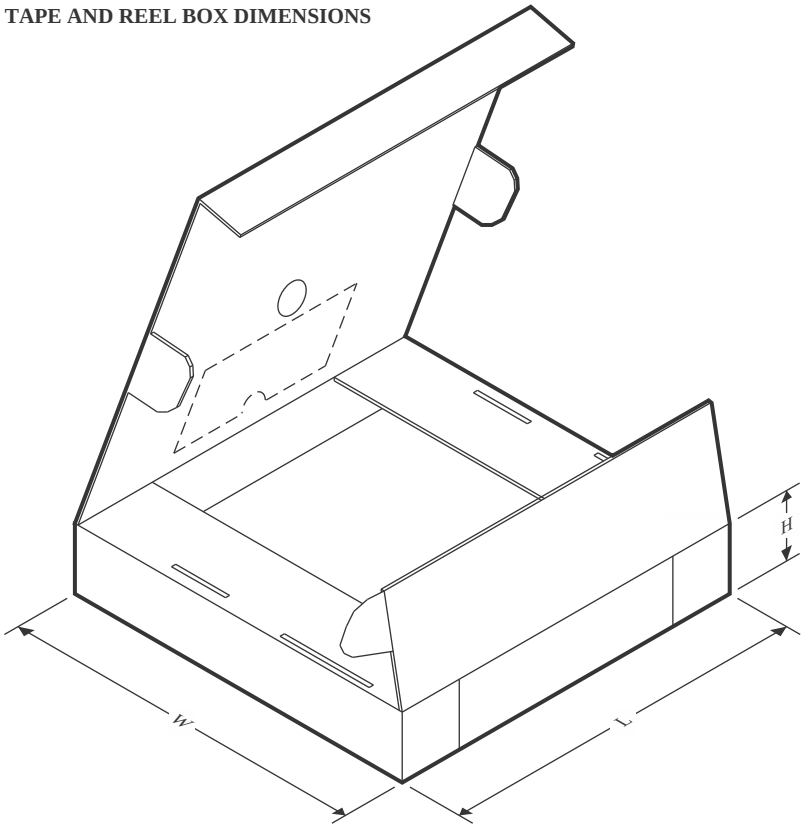
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2425CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2425CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLE2425IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

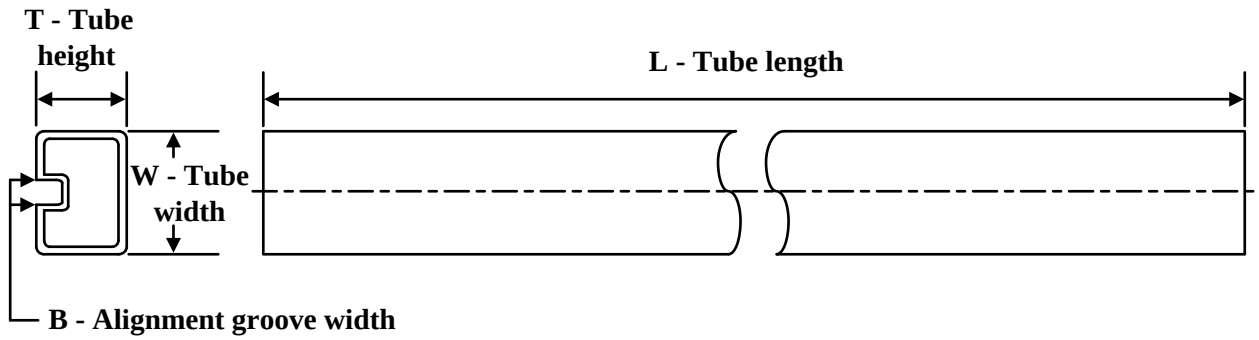
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

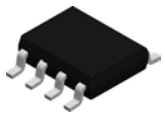
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2425CDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2425CPSR	SO	PS	8	2000	356.0	356.0	35.0
TLE2425IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLE2425CD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2425CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLE2425ID	D	SOIC	8	75	505.46	6.76	3810	4
TLE2425IDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2425MD	D	SOIC	8	75	505.46	6.76	3810	4

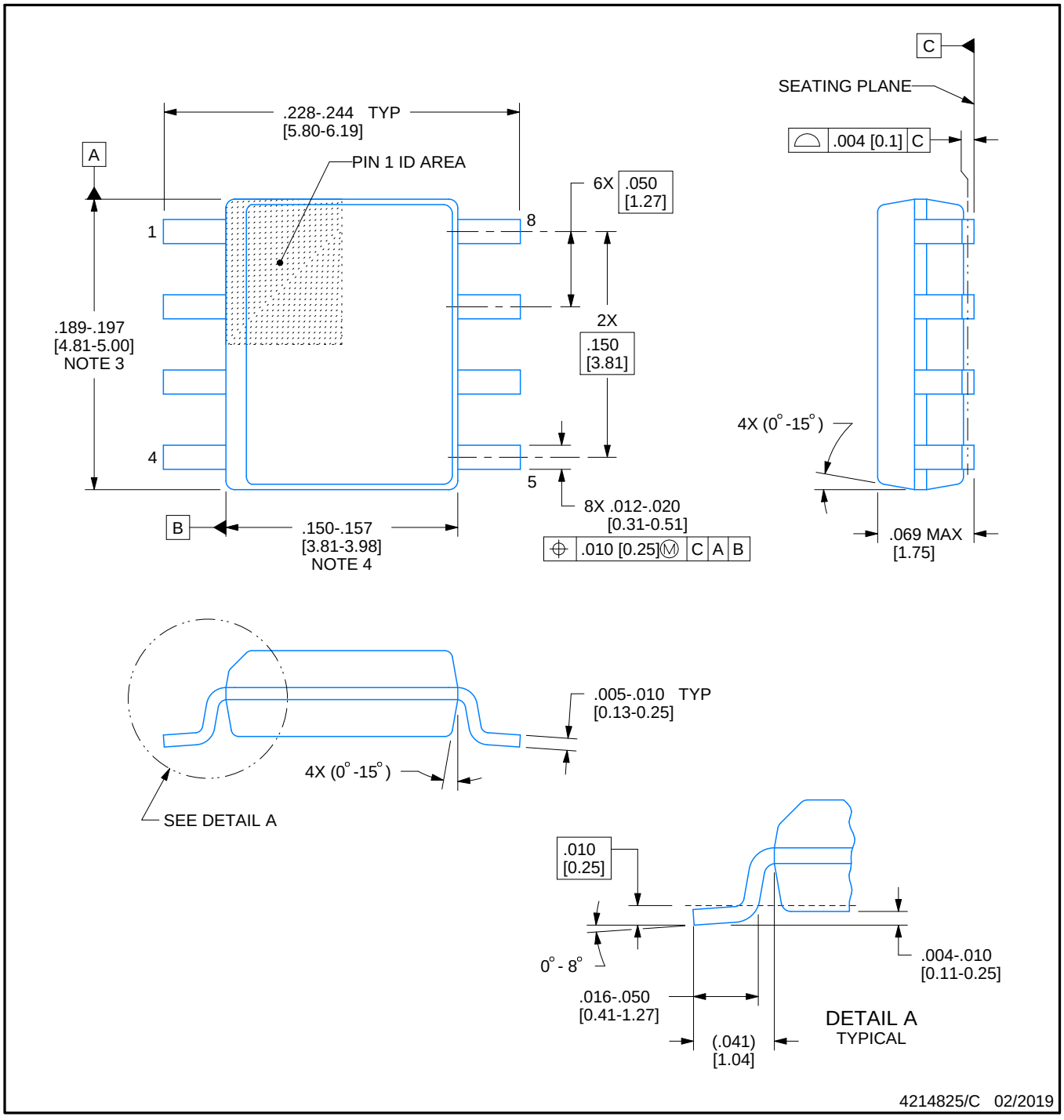


PACKAGE OUTLINE

D0008A

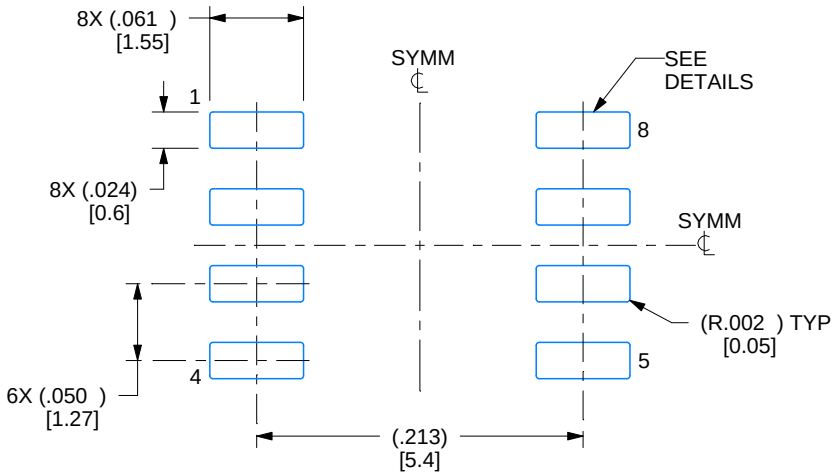
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

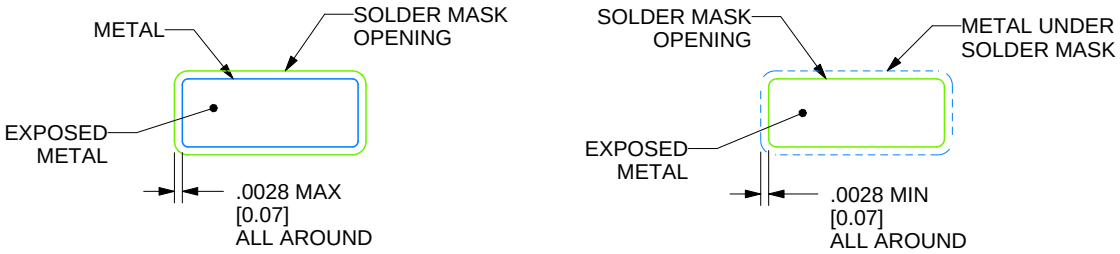


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

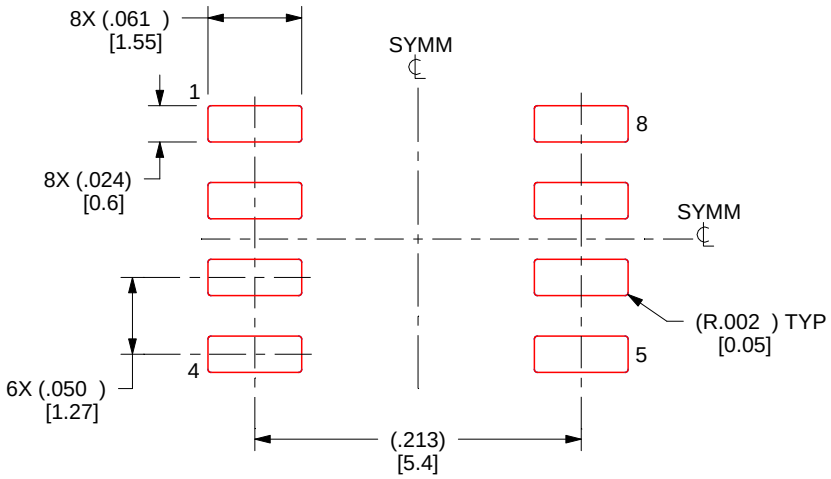
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

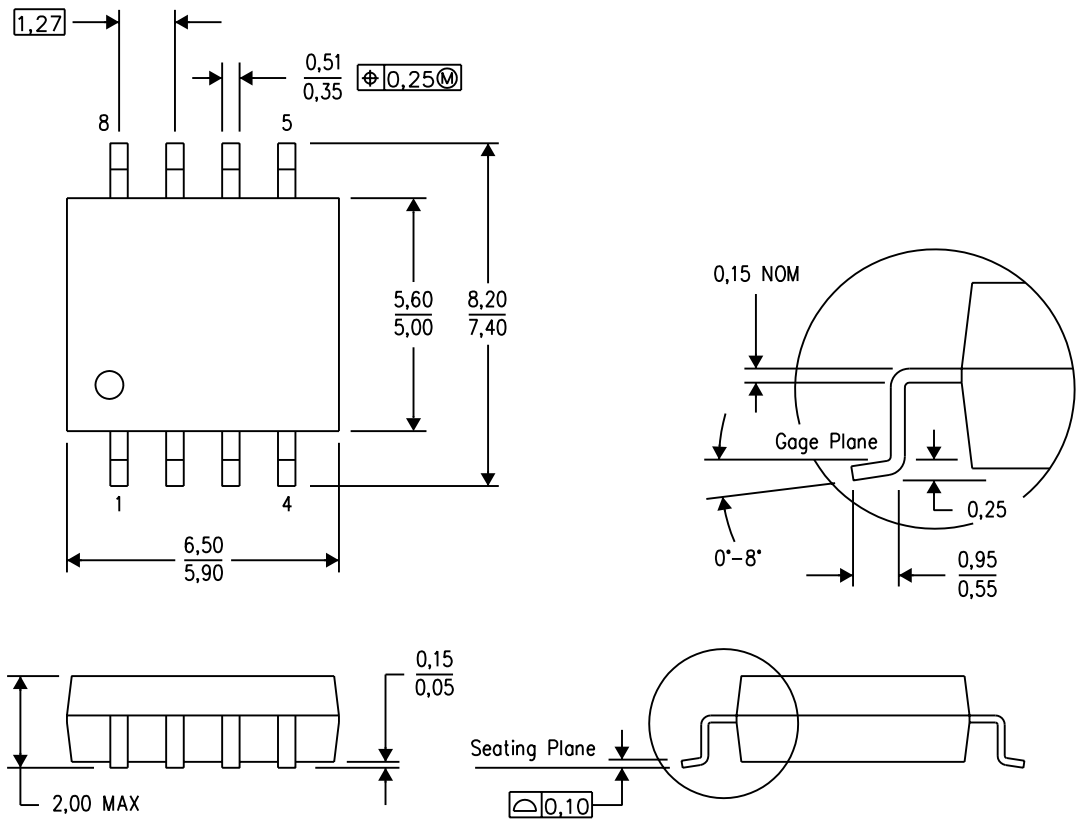
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

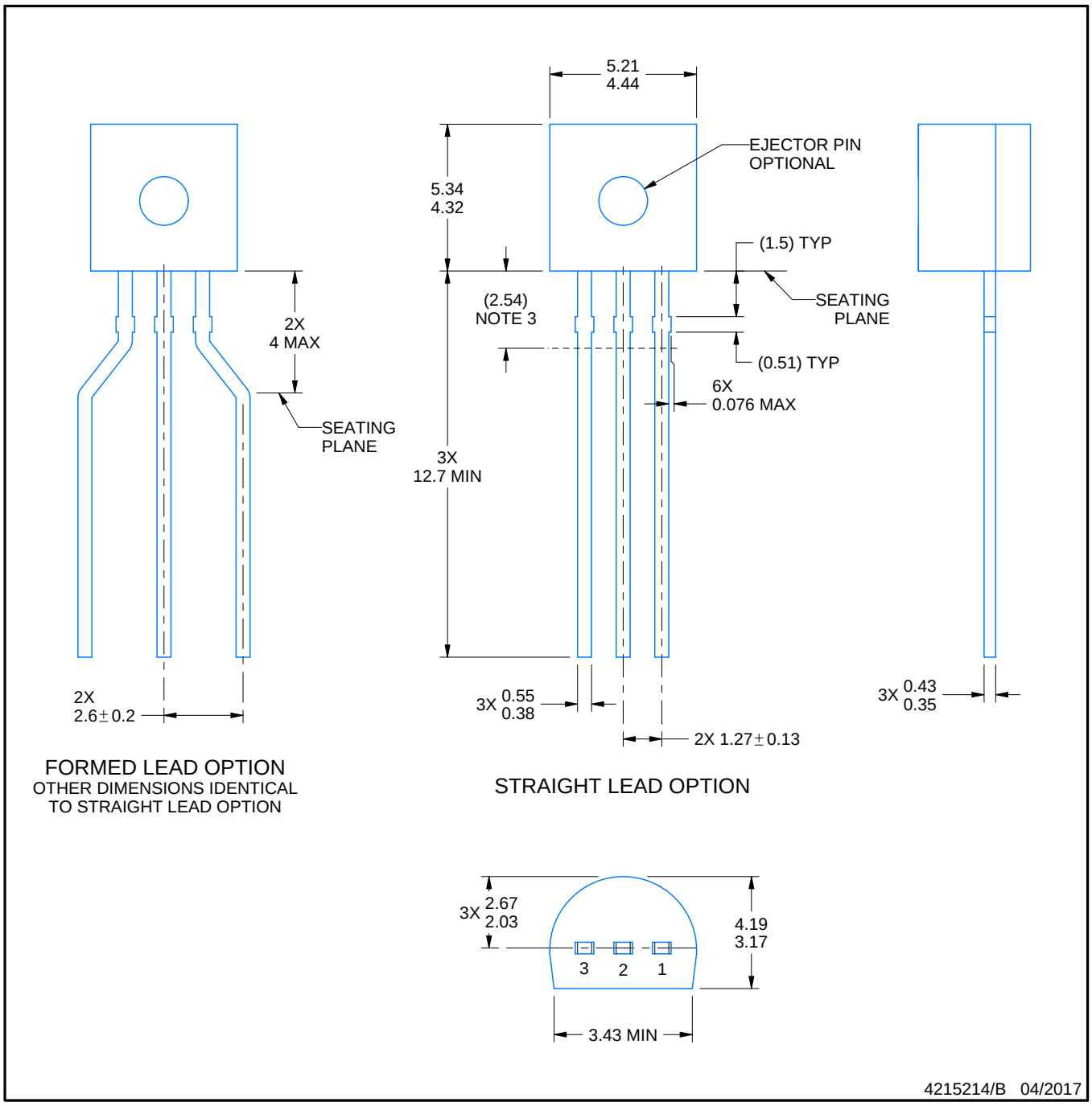




PACKAGE OUTLINE

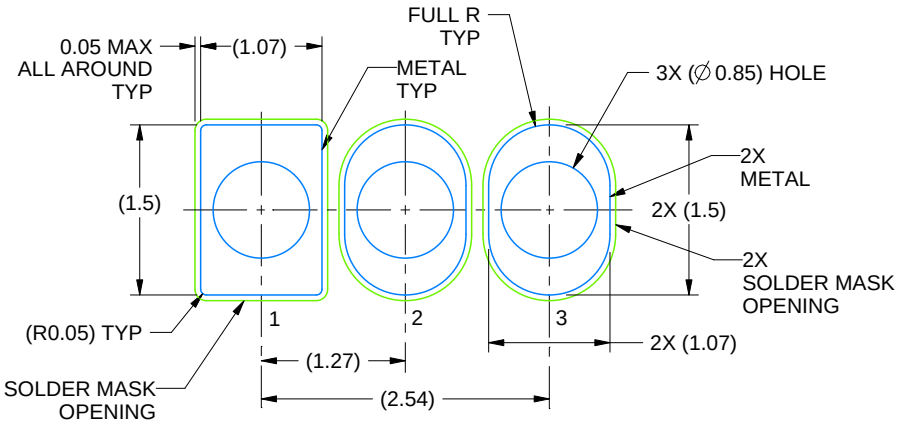
TO-92 - 5.34 mm max height

TO-92

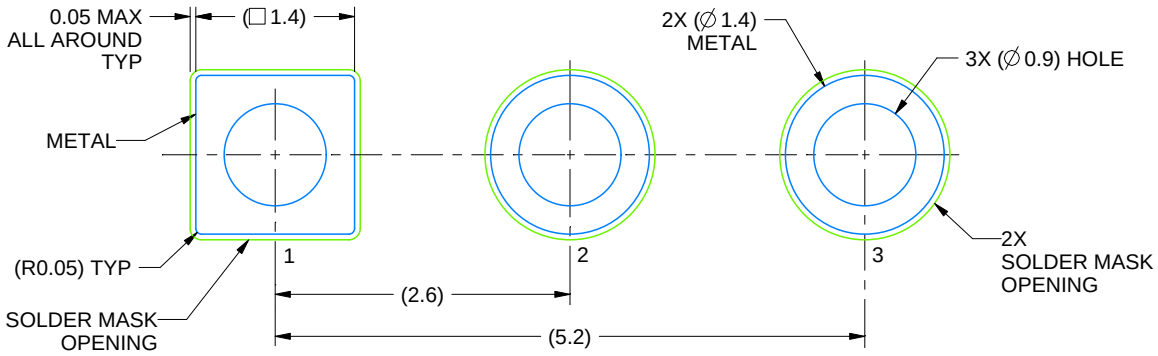


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



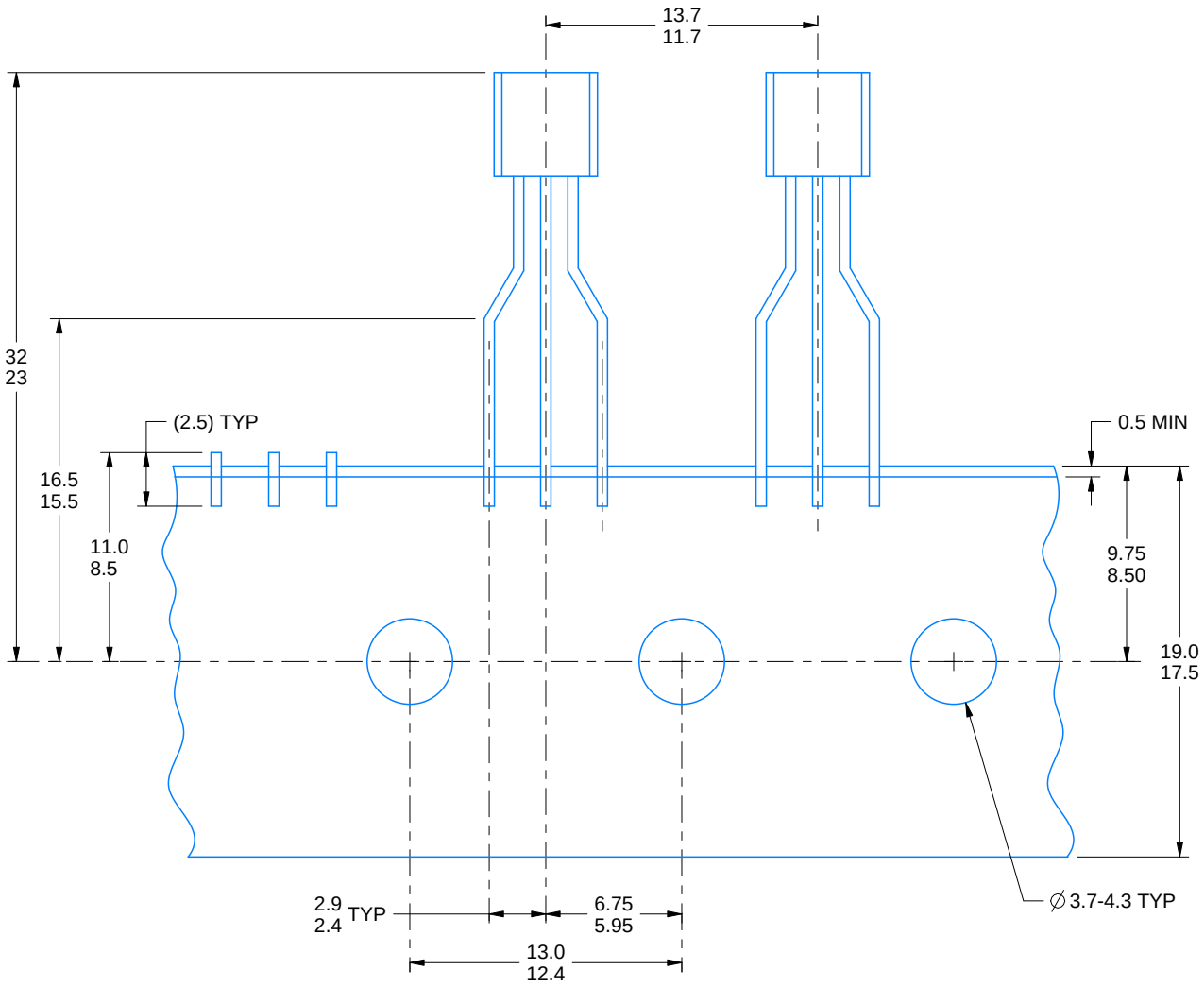
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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