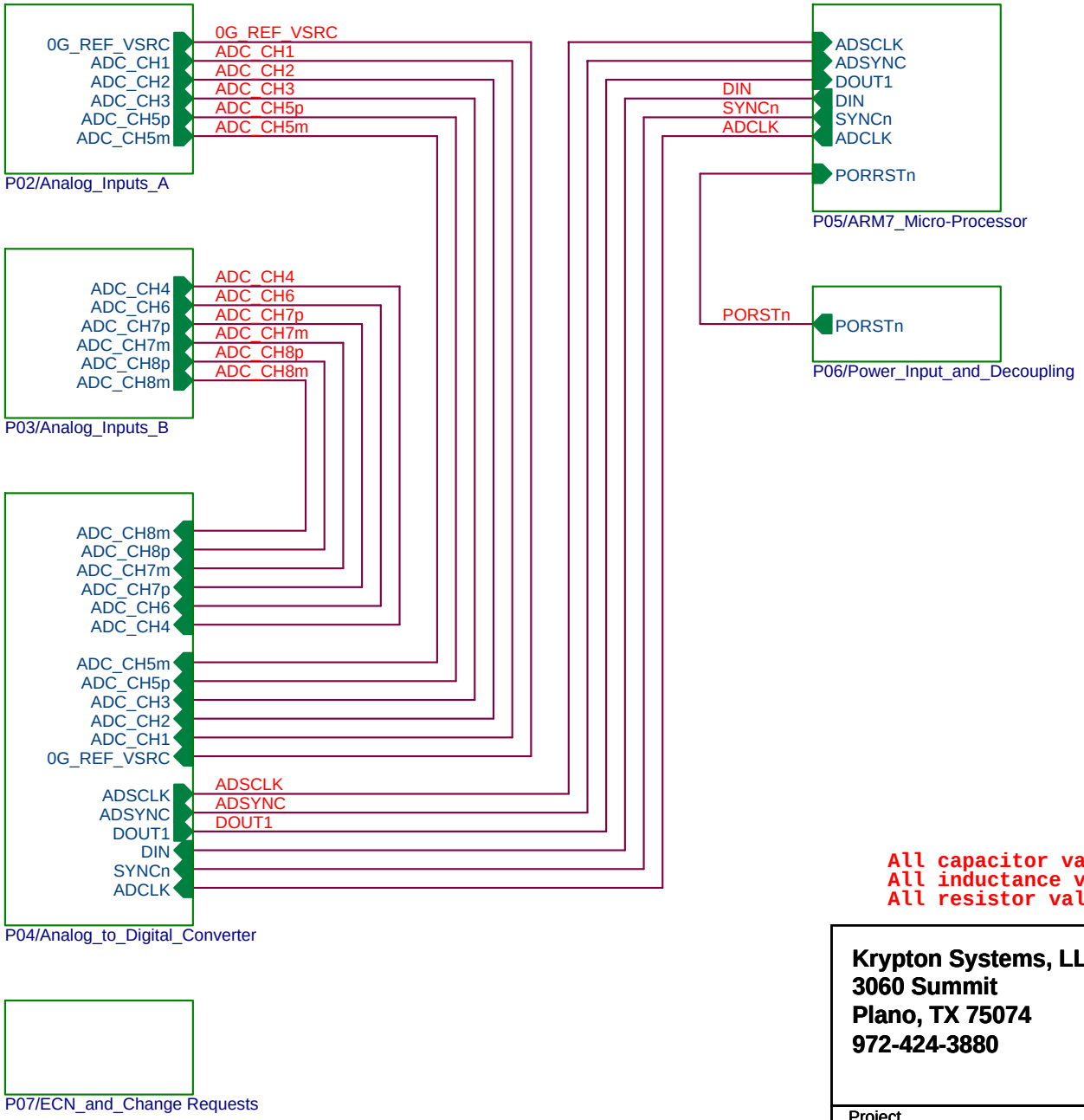

All capacitor values are shown as farads.
All inductance values are shown as henries.
All resistor values are shown as ohms.

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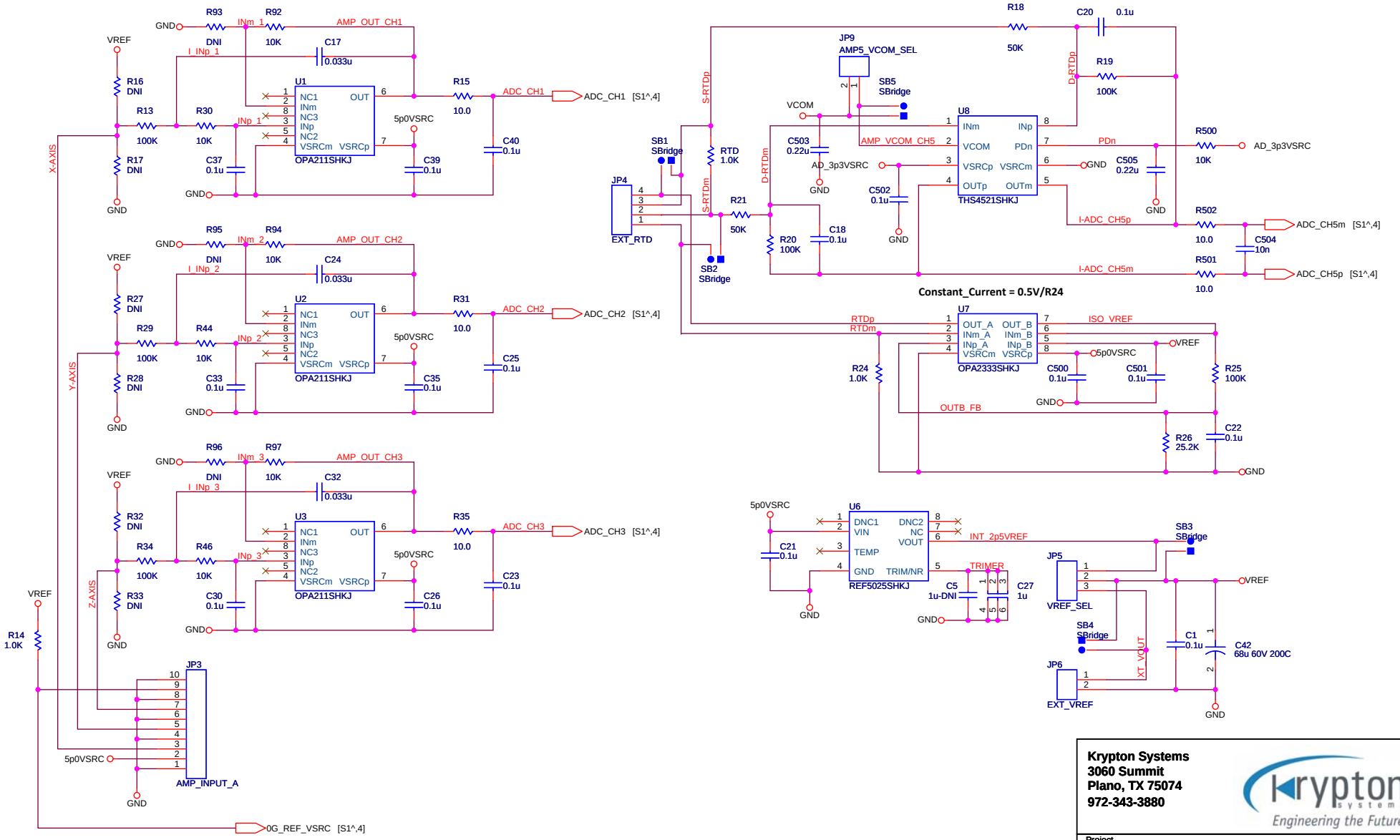
Project: **TI HEAT EVM Rev-B**			
Size: **A**	Eng: KWH	Drawing File Name: **Hiearchical_Block_Diagram**	Rev: **B**
Date: **Friday, May 18, 2012**	Sheet **1** of **7**		



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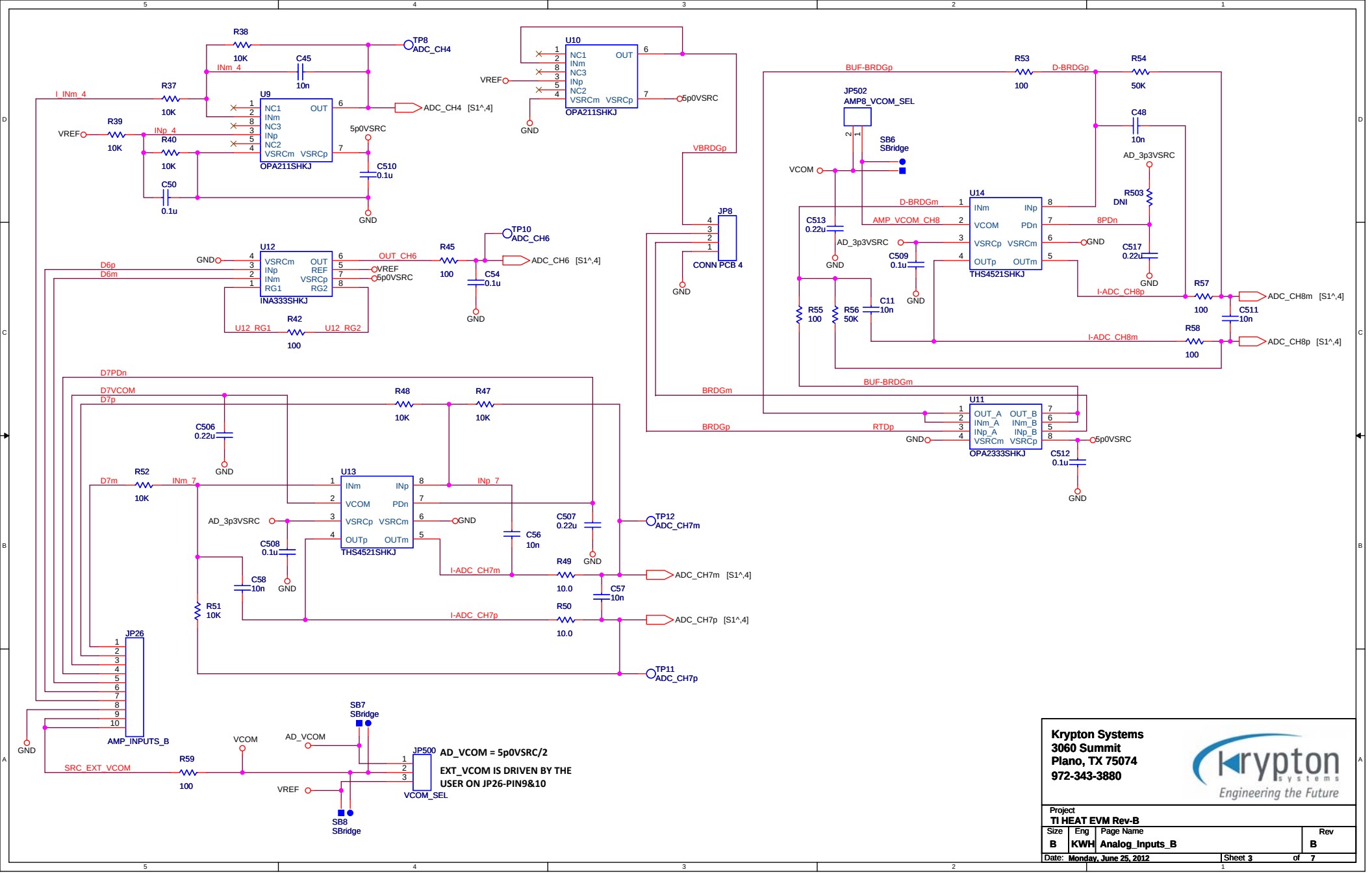
Project: **TI HEAT EVM Rev-B**			
Size: **B**	Eng: **KWH**	Page Name: **Analog_Inputs_A**	Rev: **B**
Date: **Monday, June 25, 2012**	Sheet **2** of **7**		



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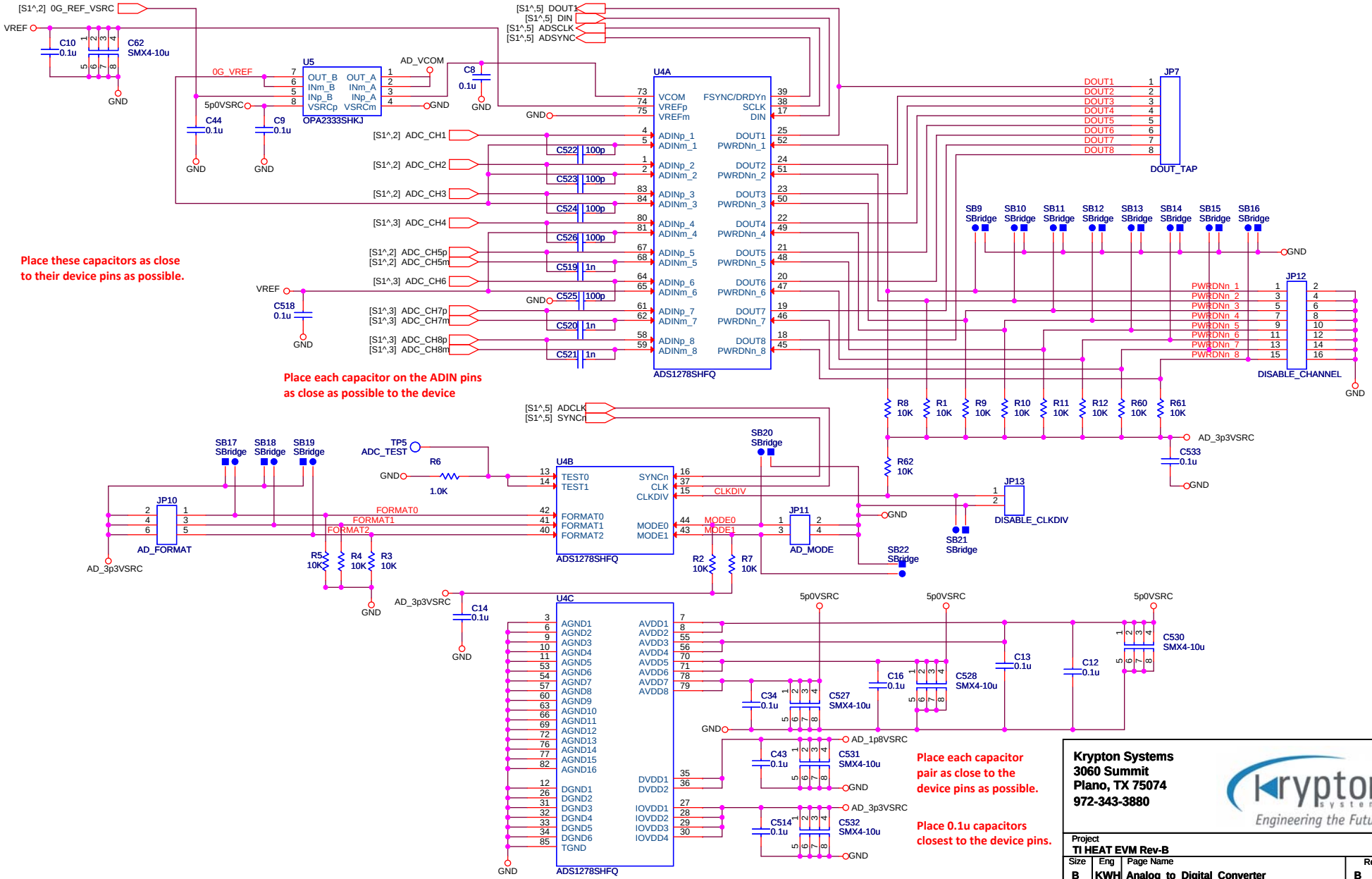
Project	TI HEAT EVM Rev-B		
Size	Eng	Page Name	Rev
B	KWH	Analog_Inputs_B	B
Date: Monday, June 25, 2012		Sheet 3 of 7	


[S1^,2] 0G_REF_VSRC
VREF
C10 0.1u
C62 SMX4-10u
GND
0G_VREF
5p0VSRC
C44 0.1u
C9 0.1u
U5
OUT_B OUT_A
INm_B INm_A
INp_B INp_A
VSRCp VSRCm
OPA2333SHKJ
AD_VCOM
C8 0.1u
[S1^,5] DOUT1
[S1^,5] DIN
[S1^,5] ADSCLK
[S1^,5] ADSYNC
U4A
VCOM
VREFp
VREFm
FSYNC/DRDYn
SCLK
DIN
ADINp_1
ADINm_1
DOUT1
PWRDNn_1
ADINp_2
ADINm_2
DOUT2
PWRDNn_2
ADINp_3
ADINm_3
DOUT3
PWRDNn_3
ADINp_4
ADINm_4
DOUT4
PWRDNn_4
ADINp_5
ADINm_5
DOUT5
PWRDNn_5
ADINp_6
ADINm_6
DOUT6
PWRDNn_6
ADINp_7
ADINm_7
DOUT7
PWRDNn_7
ADINp_8
ADINm_8
DOUT8
PWRDNn_8
ADS1278SHFQ
[S1^,2] ADC_CH1
[S1^,2] ADC_CH2
[S1^,2] ADC_CH3
[S1^,3] ADC_CH4
[S1^,2] ADC_CH5p
[S1^,2] ADC_CH5m
[S1^,3] ADC_CH6
[S1^,3] ADC_CH7p
[S1^,3] ADC_CH7m
[S1^,3] ADC_CH8p
[S1^,3] ADC_CH8m
C522 100p
C523 100p
C524 100p
C526 100p
C519 1n
C525 100p
C520 1n
C521 1n
C518 0.1u
Place these capacitors as close to their device pins as possible.
Place each capacitor on the ADIN pins as close as possible to the device
JP7
DOUT_TAP
SB9 SBridge
SB10 SBridge
SB11 SBridge
SB12 SBridge
SB13 SBridge
SB14 SBridge
SB15 SBridge
SB16 SBridge
JP12
DISABLE_CHANNEL
R8 10K
R1 10K
R9 10K
R10 10K
R11 10K
R12 10K
R60 10K
R61 10K
AD_3p3VSRC
C533 0.1u
[S1^,5] ADCLK
[S1^,5] SYNCn
SB20 SBridge
R62 10K
JP13
DISABLE_CLKDIV
SB21 SBridge
SB17 SBridge
SB18 SBridge
SB19 SBridge
TP5 ADC_TEST
R6 1.0K
U4B
TEST0
TEST1
SYNCn
CLK
CLKDIV
FORMAT0
FORMAT1
FORMAT2
MODE0
MODE1
ADS1278SHFQ
JP10
AD_FORMAT
JP11
AD_MODE
SB22 SBridge
R5 10K
R4 10K
R3 10K
R2 10K
R7 10K
U4C
AGND1
AGND2
AGND3
AGND4
AGND5
AGND6
AGND7
AGND8
AGND9
AGND10
AGND11
AGND12
AGND13
AGND14
AGND15
AGND16
DGND1
DGND2
DGND3
DGND4
DGND5
DGND6
TGND
AVDD1
AVDD2
AVDD3
AVDD4
AVDD5
AVDD6
AVDD7
AVDD8
DVDD1
DVDD2
IOVDD1
IOVDD2
IOVDD3
IOVDD4
ADS1278SHFQ
C14 0.1u
5p0VSRC
C34 0.1u
C527 SMX4-10u
C16 0.1u
C528 SMX4-10u
C13 0.1u
C12 0.1u
C530 SMX4-10u
C43 0.1u
C531 SMX4-10u
AD_1p8VSRC
C514 0.1u
C532 SMX4-10u
Place each capacitor pair as close to the device pins as possible.
Place 0.1u capacitors closest to the device pins.
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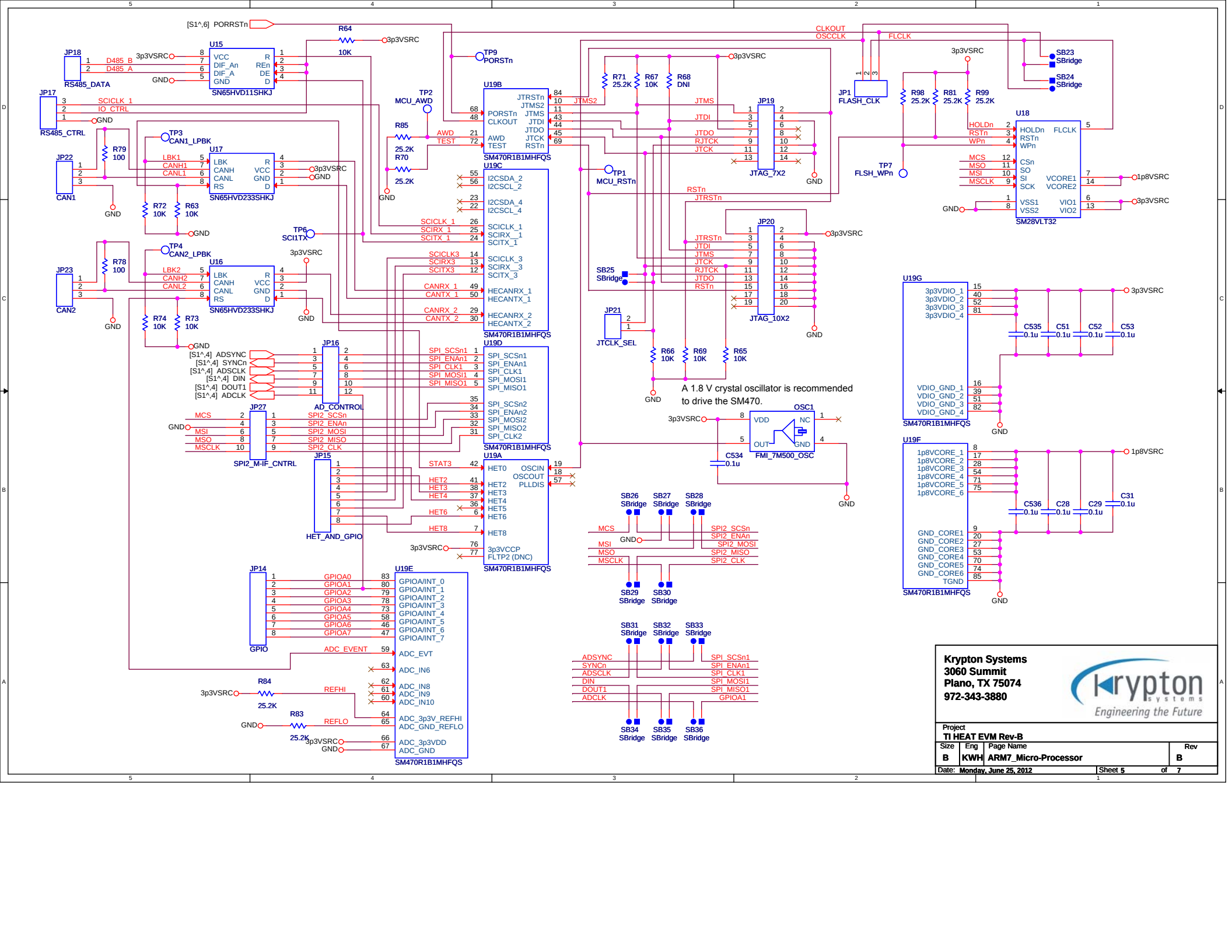
Project
TI HEAT EVM Rev-B
Size B
Eng KWH
Page Name Analog_to_Digital_Converter
Rev B
Date: Monday, June 25, 2012
Sheet 4 of 7



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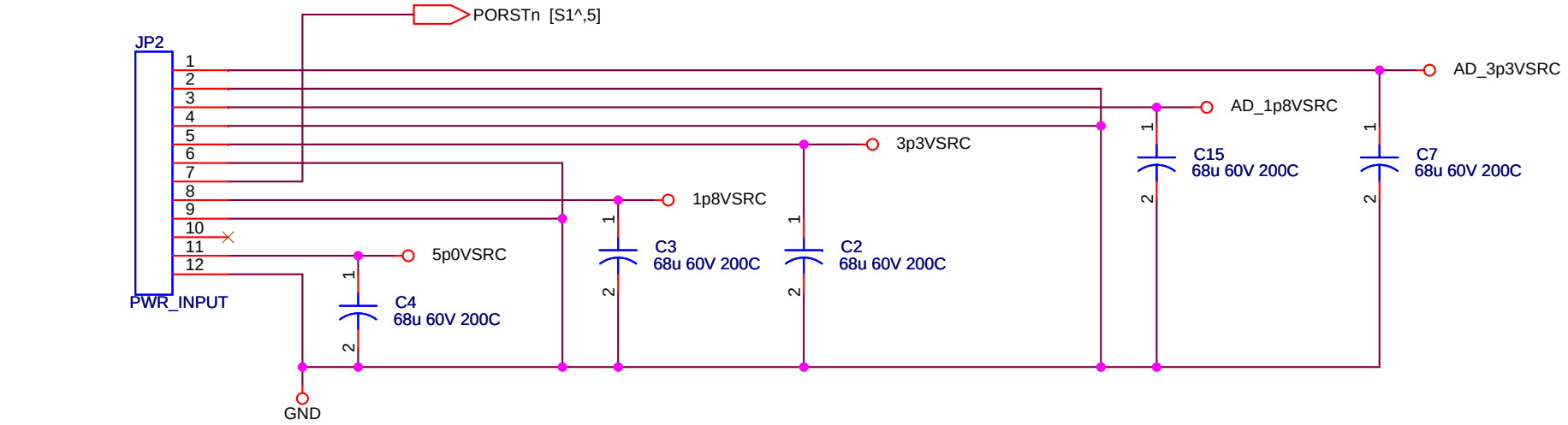
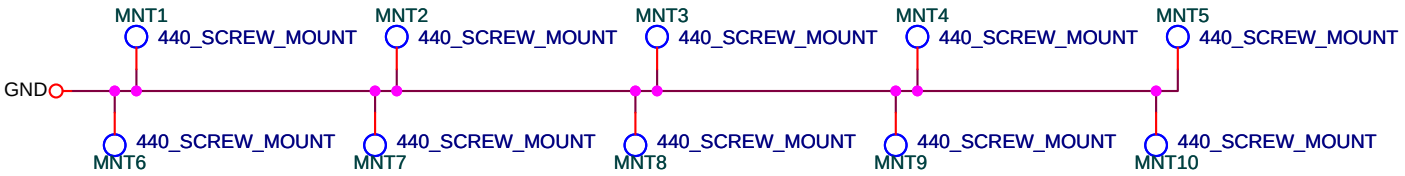
Project			
TI HEAT EVM Rev-B			
Size	Eng	Page Name	Rev
B	KWH	ARM7_Micro-Processor	B
Date: Monday, June 25, 2012		Sheet 5 of 7	





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Project			
TI HEAT EVM Rev-B			
Size	Eng	Page Name	Rev
A	**KWH**	**Power_Input_and_Decoupling**	**B**
Date: **Friday, May 18, 2012**		Sheet **6** of **7**	

TI_HEATEVM_REV-M_010312.DSN	FOLLOWING SCHEMATIC AND LAYER PLACEMENT REVIEW WE MODIFIED THE POWER INPUT STRUCTURES, CHANGED Y-AXIS AND Z-AXIS FILTERS SO THAT THEY EQUAL THE X-AXIS FILTERS. THE ITEMS IN REV-H, REV-J, AND REV-K WERE APPROVED. BOARD WAS RELEASED TO LAYOUT. LAYOUT REVIEW WILL BE HELD WHEN PLACEMENT IS FINALIZED.	KWH	01/18/12
TI_HEATEVM_REV-N_010312.DSN	MODIFIED SCHEMATIC TO REFLECT THE ERRORS NOTED DURING LAYOUT 1) SB27 HAS AN OPEN PIN 2) SB7 AND SB8 ARE CONNECTED TO THE SAME NET. SB8 WAS MOVED TO CORRECT NET 3) BOARD GREW 0.4 INCH LONGER AND NEEDED TWO MORE MOUNTING HOLES 4) ADDED C535 AND C536 TO ARM7 SO THAT EACH SIDE OF THE DEVICE HAS A DECOUPLING CAP ON BOTH POWER NETS	KWH	01/23/12
TI_HEATEVM_REV-P_010312.DSN	ADDED FOOTPRINT TO JP2	KWH	01/23/12
TI_HEATEVM_REV-S_010312.DSN	THE REFHI NET WAS BROKEN, IT WAS CONNECTED AT R84.	KWH	01/27/12
TI_HEATEVM_REV-T_010312.DSN	SOME COMPONENT VALUES WERE UPDATED PER THE NEW DESIGN RULES FROM TI. SOME PART NUMBERS AND/OR FOOTPRINTS WERE UPDATED TO BRING BOM IN STEP WITH THE OLD BOM>	KWH	02/01/12
TI_HEATEVM_REV_A1_030912.DSN	REVIEW WITH HECTOR TORRES. SCHEMATIC EDITED BASED ON HECTORS FEEDBACK. A/D CONNECTIONS TO 0G NET, VCOM AND VREF NETS WERE MODIFIED	NIMA	03/09/12

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Project: TI HEAT EVM Rev-B			
Size: A	Eng: KWH	Page Name: ECN_and_Change Requests	Rev: B
Date: Friday, May 18, 2012	Sheet 7 of 7		