

## VERY LOW POWER, NEGATIVE RAIL INPUT, RAIL-TO-RAIL OUTPUT, FULLY DIFFERENTIAL AMPLIFIER

Check for Samples: [THS4521-HT](#)

### FEATURES

- Fully Differential Architecture
- Bandwidth: 40.7 MHz (210°C)
- Slew Rate: 353.5 V/μs (210°C)
- HD<sub>2</sub>: –96 dBc at 1 kHz (1 V<sub>RMS</sub>, R<sub>L</sub> = 1 kΩ) (210°C)
- HD<sub>3</sub>: –91.5 dBc at 1 kHz (1 V<sub>RMS</sub>, R<sub>L</sub> = 1 kΩ) (210°C)
- Input Voltage Noise: 19.95 nV/√Hz (f = 100 kHz)
- Open-Loop Gain: 90 dB (typ) (210°C)
- NRI—Negative Rail Input
- RRO—Rail-to-Rail Output
- Output Common-Mode Control (with Low Offset and Drift)
- Power Supply:
  - Voltage: 2.5 V (±1.25 V) to 3.3 V (±1.65 V)
  - Current: 1.4 mA/ch (3.3 V)
- Power-Down Capability: 10 μA (typ) (210°C)

### APPLICATIONS

- Down-Hole Drilling
- High Temperature Environments

### SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Extreme (–55°C/210°C) Temperature Range<sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.

(1) Custom temperature ranges available

### DESCRIPTION

The THS4521 is a very low-power, fully differential op amp with rail-to-rail output and an input common-mode range that includes the negative rail. This amplifier is designed for low-power data acquisition systems and high-density applications where power dissipation is a critical parameter, and provides exceptional performance in audio applications.

The THS4521 features accurate output common-mode control that allows for dc-coupling when driving analog-to-digital converters (ADCs). This control, coupled with an input common-mode range below the negative rail as well as rail-to-rail output, allows for easy interfacing between single-ended, ground-referenced signal sources. Additionally, this device is ideally suited for driving both successive-approximation register (SAR) and delta-sigma (ΔΣ) ADCs using only a single 2.5-V to 3.3-V and ground power supply.

The THS4521 is characterized for operation from –55°C to 210°C.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	KGD (bare die)	THS4521SKGD1	NA
	HKJ	THS4521SHKJ	THS4521SHKJ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
11 mils.	Silicon with backgrind	Floating	Al-Cu (0.5%)	1380 nm

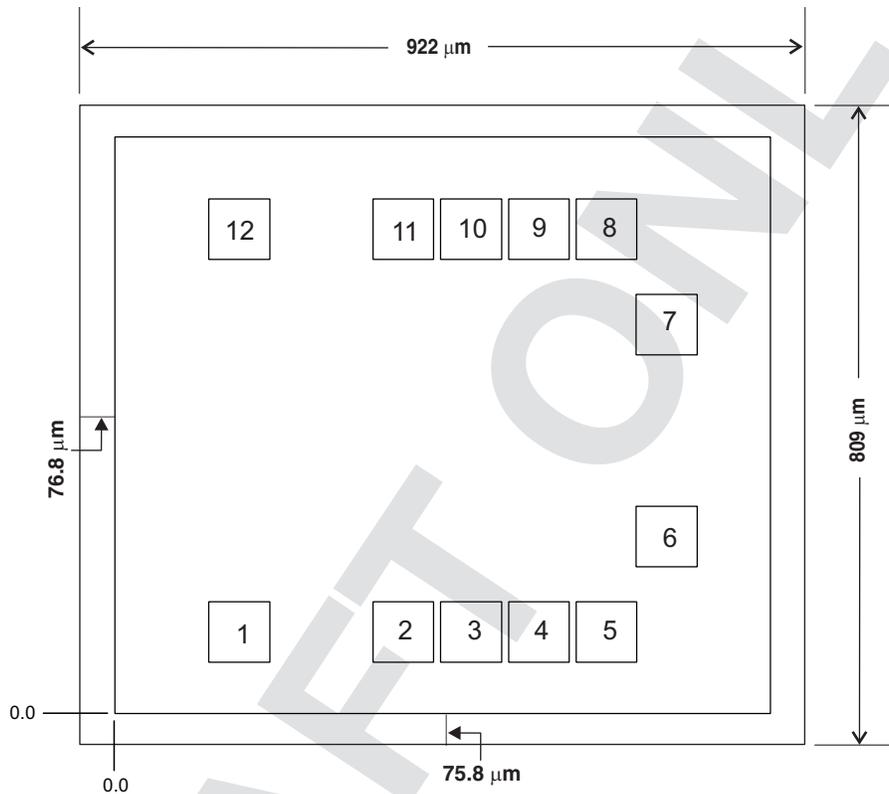


Table 1. Bond Pad Coordinates in Microns

DISCRIPTION	PAD NUMBER	X min	Y min	X max	Y max
V <sub>IN-</sub>	1	80.7	3.7	165.7	88.7
V <sub>OCM</sub>	2	310.6	3.7	395.6	88.7
V <sub>S+</sub>	3	405.6	3.7	490.6	88.7
V <sub>S+</sub>	4	500.6	3.7	585.6	88.7
V <sub>S+</sub>	5	595.6	3.7	680.6	88.7
V <sub>OUT+</sub>	6	679.6	137.55	764.6	222.55
V <sub>OUT-</sub>	7	679.6	434.7	764.6	519.7
V <sub>S-</sub>	8	595.6	568.6	680.6	653.6
V <sub>S-</sub>	9	500.6	568.6	585.6	653.6
V <sub>S-</sub>	10	405.6	568.6	490.6	653.6
PD	11	310.6	568.6	395.6	653.6
V <sub>IN+</sub>	12	80.7	568.6	165.7	653.6

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Over operating free-air temperature range (unless otherwise noted).

			UNIT
Supply Voltage, $V_{S-}$ to $V_{S+}$		3.6	V
Input/Output Voltage, $V_I$ ( $V_{IN\pm}$ , $V_{OUT\pm}$ , $V_{OCM}$ pins)		$(V_{S-}) - 0.7$ to $(V_{S+}) + 0.7V$	V
Differential Input Voltage, $V_{ID}$		1	V
Output Current, $I_O$		100	mA
Input Current, $I_I$ ( $V_{IN\pm}$ , $V_{OCM}$ pins)		10	mA
Continuous Power Dissipation		See Thermal Characteristic Specifications	
Maximum Junction Temperature, $T_J$ (continuous operation, long-term reliability) <sup>(2)</sup>		217	°C
Operating Free-air Temperature Range, $T_A$		-55 to 210	°C
Storage Temperature Range, $T_{STG}$		-65 to 210	°C
ESD Rating:	Human Body Model (HBM)	1300	V
	Charge Device Model (CDM)	1000	V
	Machine Model (MM)	50	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Refer to [Figure 1](#) for expected life time.

**THERMAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$\theta_{JC}$	Junction-to-case thermal resistance (to bottom of case)			5.7	°C/W
	Junction-to-case thermal resistance (to top of case lid - as if formed dead bug)			13.7	

**ELECTRICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3.3\text{ V}$** 

At  $V_{S+} = 3.3\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$  (differential),  $R_L = 1\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	-55°C to 125°C			-55°C to 210°C			UNIT	TEST LEVEL <sup>(1)</sup>
		MIN	TYP	MAX	MIN	TYP	MAX		
<b>AC PERFORMANCE</b>									
Small-Signal Bandwidth	$V_{OUT} = 100\text{ mV}_{PP}$ , $G = 1$		104.3			40.7		MHz	C
	$V_{OUT} = 100\text{ mV}_{PP}$ , $G = 2$		42			12.5		MHz	C
	$V_{OUT} = 100\text{ mV}_{PP}$ , $G = 5$		12.2			3.15		MHz	C
	$V_{OUT} = 100\text{ mV}_{PP}$ , $G = 10$		8.1			2.2		MHz	C
Gain Bandwidth Product	$V_{OUT} = 100\text{ mV}_{PP}$ , $G = 10$		81			22		MHz	C
Large-Signal Bandwidth	$V_{OUT} = 2\text{ V}_{PP}$ , $G = 1$		84			22		MHz	C
Bandwidth for 0.1-dB Flatness	$V_{OUT} = 2\text{ V}_{PP}$ , $G = 1$		18.1			5.4		MHz	C
Rising Slew Rate (Differential)	$V_{OUT} = 2\text{-V Step}$ , $G = 1$ , $R_L = 200\ \Omega$		377.5			353.5		V/ $\mu\text{s}$	C
Falling Slew Rate (Differential)	$V_{OUT} = 2\text{-V Step}$ , $G = 1$ , $R_L = 200\ \Omega$		422.5			392.5		V/ $\mu\text{s}$	C
Overshoot	$V_{OUT} = 2\text{-V Step}$ , $G = 1$ , $R_L = 200\ \Omega$		6.75			8.85		%	C
Undershoot	$V_{OUT} = 2\text{-V Step}$ , $G = 1$ , $R_L = 200\ \Omega$		7.85			11.45		%	C
Rise Time	$V_{OUT} = 2\text{-V Step}$ , $G = 1$ , $R_L = 200\ \Omega$		13.5			15.9		ns	C
Fall Time	$V_{OUT} = 2\text{-V Step}$ , $G = 1$ , $R_L = 200\ \Omega$		11.4			14.6		ns	C
Settling Time to 1%	$V_{OUT} = 2\text{-V Step}$ , $G = 1$ , $R_L = 200\ \Omega$		18.5			23.5		ns	C
Harmonic Distortion									
2nd harmonic	$f = 1\text{ kHz}$ , $V_{OUT} = 1\text{ V}_{RMS}$ , $G = 1^{(2)}$ , differential input		-115			-96		dBc	C
	$f = 1\text{ MHz}$ , $V_{OUT} = 2\text{ V}_{PP}$ , $G = 1$		-77			-68.5		dBc	C
3rd harmonic	$f = 1\text{ kHz}$ , $V_{OUT} = 1\text{ V}_{RMS}$ , $G = 1^{(2)}$ , differential input		-116			-91.5		dBc	C
	$f = 1\text{ MHz}$ , $V_{OUT} = 2\text{ V}_{PP}$ , $G = 1$		-80.5			-68.5		dBc	C
Second-Order Intermodulation Distortion	Two-tone, $f_1 = 2\text{ kHz}$ , $f_2 = 500\text{ Hz}$ , $V_{OUT} = 1\text{ V}_{RMS}$ envelope		-91.5			-79.5		dBc	C
Third-Order Intermodulation Distortion	Two-tone, $f_1 = 2\text{ kHz}$ , $f_2 = 500\text{ Hz}$ , $V_{OUT} = 1\text{ V}_{RMS}$ envelope		-95.5			-79.5		dBc	C
Input Voltage Noise	$f > 10\text{ kHz}$		9.05			19.95		nV/ $\sqrt{\text{Hz}}$	C
Input Current Noise	$f > 100\text{ kHz}$		1.8			2.45		pA/ $\sqrt{\text{Hz}}$	C
Overdrive Recovery Time	Overdrive = $\pm 0.5\text{ V}$		116.5			126		ns	C
Output Balance Error	$V_{OUT} = 100\text{ mV}$ , $f \leq 2\text{ MHz}$ (differential input)		-51.5			-45.5		dB	C
Closed-Loop Output Impedance	$f = 1\text{ MHz}$ (differential)		0.3					$\Omega$	C
<b>DC PERFORMANCE</b>									
Open-Loop Voltage Gain ( $A_{OL}$ )			102			90		dB	A
Input-Referred Offset Voltage			$\pm 0.1$	$\pm 5$		$\pm 0.43$	$\pm 11.5$	mV	A
Input offset voltage drift <sup>(3)</sup>			$\pm 1$	$\pm 28$		$\pm 2$	$\pm 50$	$\mu\text{V}/^\circ\text{C}$	B
Input Bias Current			$\pm 0.75$	$\pm 3.3$		$\pm 0.78$	$\pm 4.5$	$\mu\text{A}$	A
Input bias current drift <sup>(3)</sup>			$\pm 3.3$	$\pm 14$		$\pm 4.8$	$\pm 17$	nA/ $^\circ\text{C}$	B
Input Offset Current			$\pm 0.3$	$\pm 1.7$		$\pm 0.5$	$\pm 3.5$	$\mu\text{A}$	A
Input offset current drift <sup>(3)</sup>			$\pm 1.1$	$\pm 8$		$\pm 1.26$	$\pm 9$	nA/ $^\circ\text{C}$	B

(1) Test levels: **(A)** 100% tested. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.

(2) Not directly measurable; calculated using noise gain of 101.

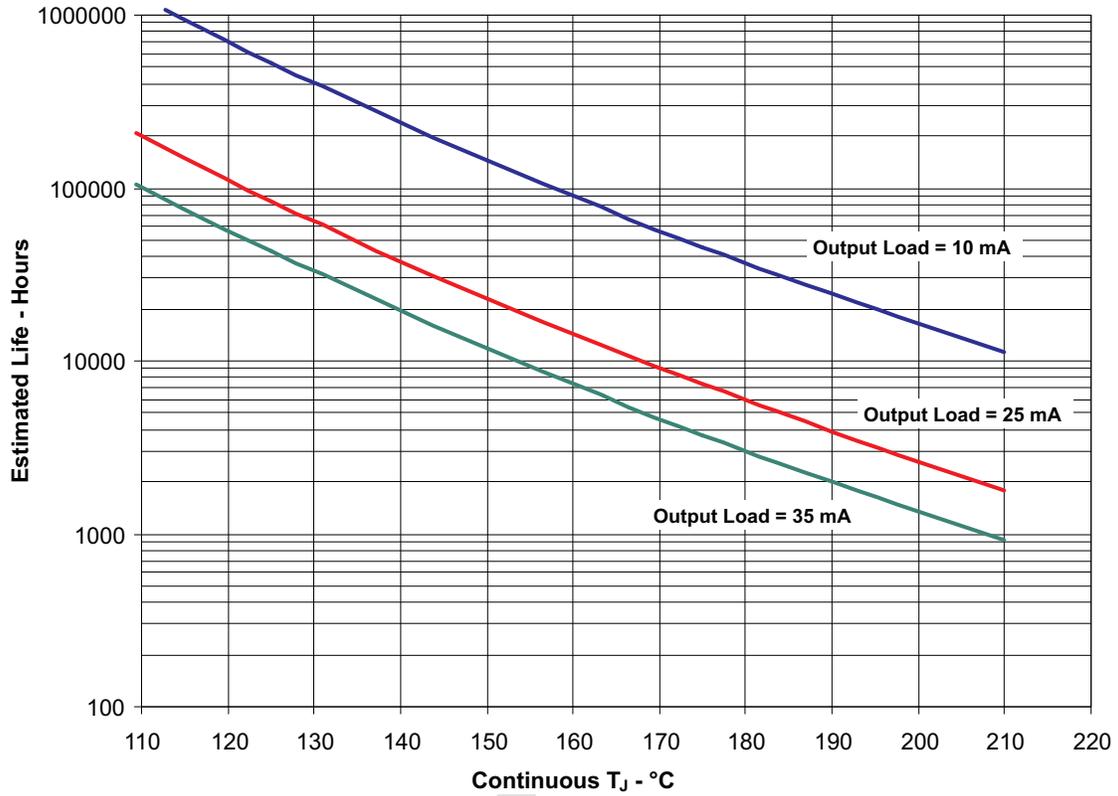
(3) Input Offset Voltage Drift, Input Bias Current Drift and Input Offset Current Drift are average values calculated by taking data at -55°C and 125°C, computing the difference and dividing by 180. High temperature drift data is an average value calculated by taking data at -55°C and 210°C, computing the difference and dividing by 265.

**ELECTRICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3.3\text{ V}$  (continued)**

At  $V_{S+} = 3.3\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$  (differential),  $R_L = 1\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	-55°C to 125°C			-55°C to 210°C			UNIT	TEST LEVEL <sup>(1)</sup>
		MIN	TYP	MAX	MIN	TYP	MAX		
<b>INPUT</b>									
Common-Mode Input Voltage Low			-0.1	-0		-0.1	0	V	A
Common-Mode Input Voltage High		1.8	1.9		1.8	1.9		V	A
Common-Mode Rejection Ratio (CMRR)		80	105		74	98		dB	A
Input Resistance			154  3.2			12.3  46		kΩ  pF	C
<b>OUTPUT</b>									
Output Voltage Low			0.09	0.25		0.09	0.31	V	A
Output Voltage High		2.95	3.11		2.85	3.05		V	A
Output Current Drive (for linear operation)	$R_L = 50\ \Omega$		±35 <sup>(4)</sup>			±33 <sup>(4)</sup>		mA	C
<b>POWER SUPPLY</b>									
Specified Operating Voltage		2.5		3.6	2.5		3.6	V	A
Quiescent Operating Current, per channel		0.85	1	1.3	0.9	1.1	1.4	mA	A
Power-Supply Rejection Ratio (±PSRR)		66	85		60	80		dB	A
<b>POWER DOWN</b>									
Enable Voltage Threshold	Assured on above 2.2 V		1.6	2.2		1.6	2.2	V	A
Disable Voltage Threshold	Assured off below 0.7 V	0.7	1.6		0.7	1.6		V	A
Disable Pin Bias Current			1			1		μA	C
Power Down Quiescent Current			2			10		μA	C
Turn-On Time Delay	Time to $V_{OUT} = 90\%$ of final value, $V_{IN} = 2\text{ V}$ , $R_L = 200\ \Omega$		86.5			99		ns	C
Turn-Off Time Delay	Time to $V_{OUT} = 10\%$ of original value, $V_{IN} = 2\text{ V}$ , $R_L = 200\ \Omega$		136			144.5		ns	C
<b><math>V_{OCM}</math> VOLTAGE CONTROL</b>									
Small-Signal Bandwidth			21			13		MHz	C
Slew Rate			49			39		V/μs	C
Gain		0.97	0.99	1.02	0.97	1.0	1.03	V/V	A
Common-Mode Offset Voltage from $V_{OCM}$ Input	Measured at $V_{OUT}$ with $V_{OCM}$ input driven, $V_{OCM} = 1.65\text{ V} \pm 0.5\text{ V}$		±0.2	±4		±0.7	±10	mV	A
Input Bias Current	$V_{OCM} = 1.65\text{ V} \pm 0.5\text{ V}$		±0.9	±2.73		±0.91	±2.75	μA	A
$V_{OCM}$ Voltage Range		1.01	0.8 to 2.5	2.3	1.09	0.8 to 2.5	2.3	V	A
Input Impedance			114  3.6			148  3.7		kΩ  pF	C
Default Output Common-Mode Voltage Offset from $(V_{S+} - V_{S-})/2$	Measured at $V_{OUT}$ with $V_{OCM}$ input open		±0.3	±5		±0.6	±10	mV	A

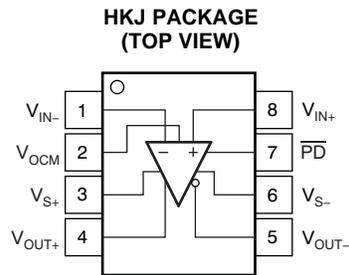
(4) Continuous operation with high current loads at elevated temperature may affect product reliability. Refer to operating lifetime chart (Figure 1).



- (1) See data sheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

**Figure 1. THS4521SHKJ/SKGD1 Operating Life Derating Chart**

DRAFT

**DEVICE INFORMATION**

**TERMINAL FUNCTIONS**

PIN NO.	NAME	DESCRIPTION
1	$V_{IN-}$	Inverting amplifier input
2	$V_{OCM}$	Common-mode voltage input
3	$V_{S+}$	Amplifier positive power-supply input
4	$V_{OUT+}$	Noninverting amplifier output
5	$V_{OUT-}$	Inverting amplifier output
6	$V_{S-}$	Amplifier negative power-supply input. Note that $V_{S-}$ is tied together on multi-channel devices.
7	$\overline{PD}$	Power down. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
8	$V_{IN+}$	Noninverting amplifier input

## TYPICAL CHARACTERISTICS

Table of Graphs<sup>(1)</sup>:  $V_{S+} - V_{S-} = 3.3\text{ V}$

TITLE	FIGURE
Small-Signal Frequency Response	Figure 2
Large-Signal Frequency Response	Figure 3
Large- and Small-Signal Pulse Response	Figure 4
Slew Rate vs $V_{OUT}$ Step	Figure 5
Overdrive Recovery	Figure 6
10-kHz Output Spectrum on AP Analyzer	Figure 7
Harmonic Distortion vs Frequency	Figure 8
Harmonic Distortion vs Output Voltage at 1 MHz	Figure 9
Harmonic Distortion vs Gain at 1 MHz	Figure 10
Harmonic Distortion vs Load at 1 MHz	Figure 11
Harmonic Distortion vs $V_{OCM}$ at 1 MHz	Figure 12
Two-Tone, Second- and Third-Order Intermodulation Distortion vs Frequency	Figure 13
Single-Ended Output Voltage Swing vs Load Resistance	Figure 14
Main Amplifier Differential Output Impedance vs Frequency	Figure 15
Frequency Response vs $C_{LOAD}$ ( $R_{LOAD} = 1\text{ k}\Omega$ )	Figure 16
$R_O$ vs $C_{LOAD}$ ( $R_{LOAD} = 1\text{ k}\Omega$ )	Figure 17
Rejection Ratio vs Frequency	Figure 18
Turn-on Time	Figure 19
Turn-off Time	Figure 20
Input-Referred Voltage Noise and Current Noise Spectral Density	Figure 21
Main Amplifier Differential Open-Loop Gain and Phase	Figure 22
Output Balance Error vs Frequency	Figure 23
$V_{OCM}$ Small-Signal Frequency Response	Figure 24
$V_{OCM}$ Large-Signal Frequency Response	Figure 25
$V_{OCM}$ Input Impedance vs Frequency	Figure 26

(1) Graphs are plotted for room temperature only and are given only for reference.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3.3\text{ V}$**

At  $V_{S+} = +3.3\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$  (differential),  $R_L = 1\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.

**SMALL-SIGNAL FREQUENCY RESPONSE**

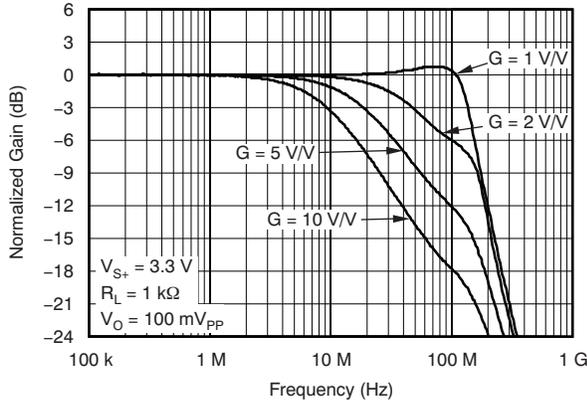


Figure 2.

**LARGE-SIGNAL FREQUENCY RESPONSE**

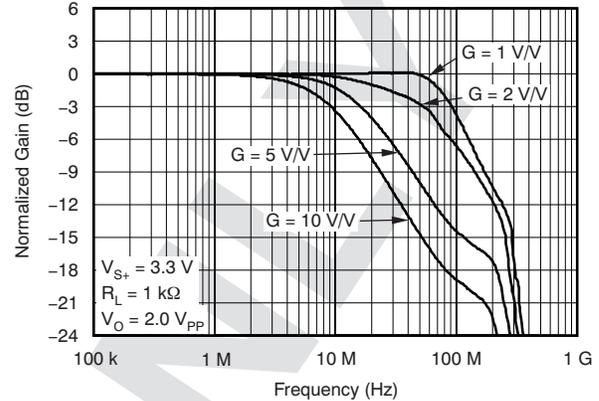


Figure 3.

**LARGE- AND SMALL-SIGNAL PULSE RESPONSE**

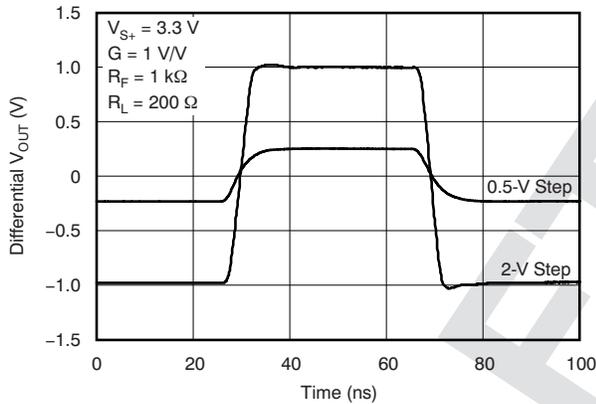


Figure 4.

**SLEW RATE vs  $V_{OUT}$**

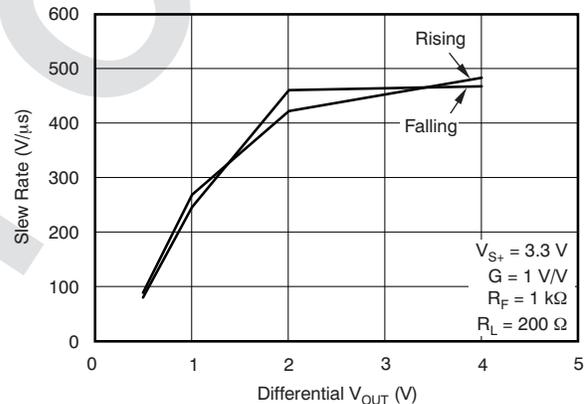


Figure 5.

**OVERDRIVE RECOVERY**

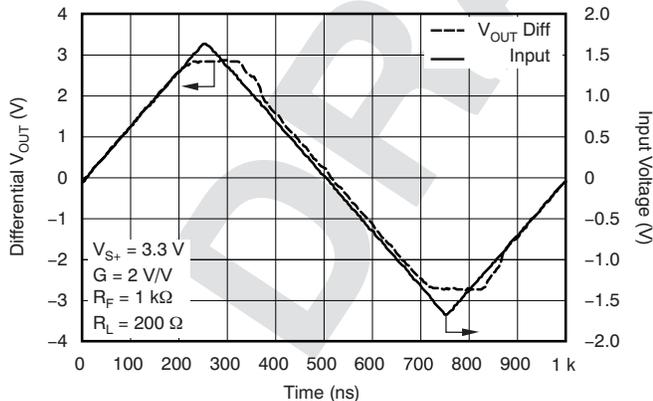


Figure 6.

**10-kHz OUTPUT SPECTRUM ON AP ANALYZER**

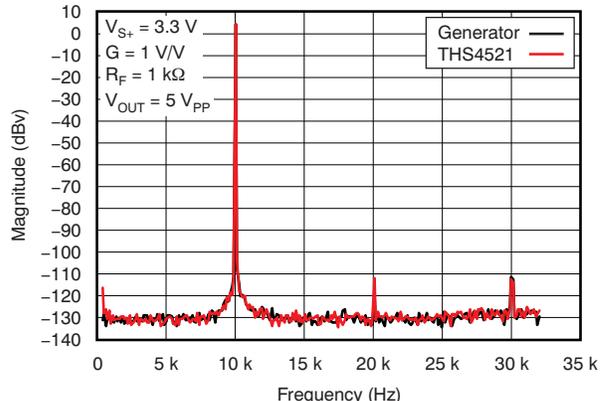


Figure 7.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3.3\text{ V}$  (continued)**

At  $V_{S+} = +3.3\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$  (differential),  $R_L = 1\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.

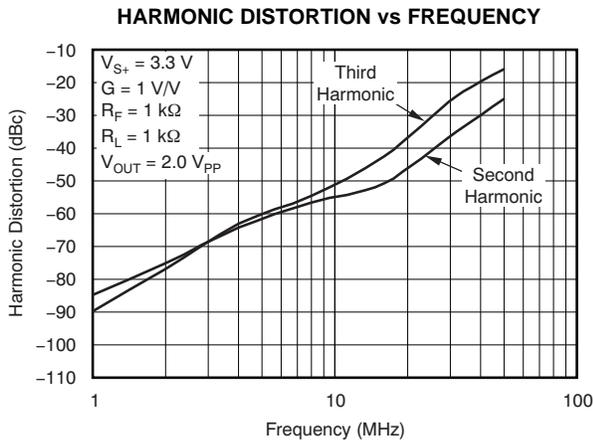


Figure 8.

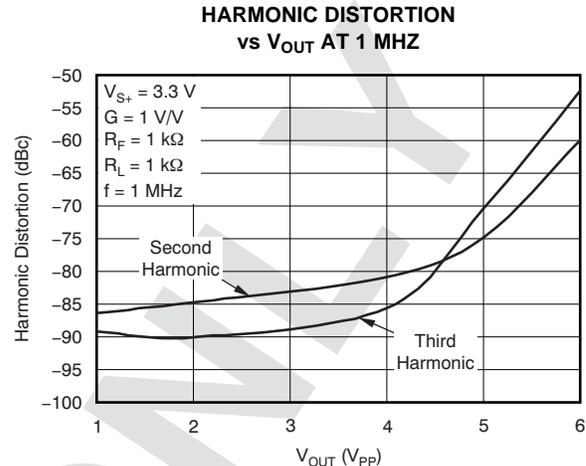


Figure 9.

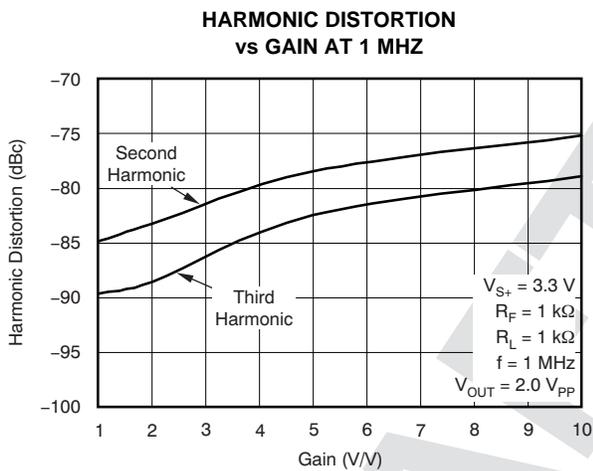


Figure 10.

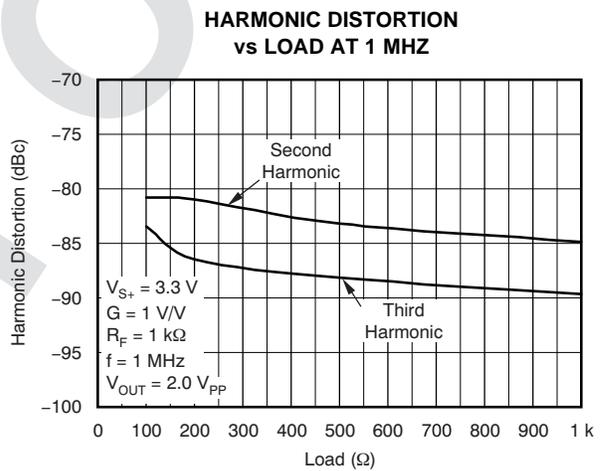


Figure 11.

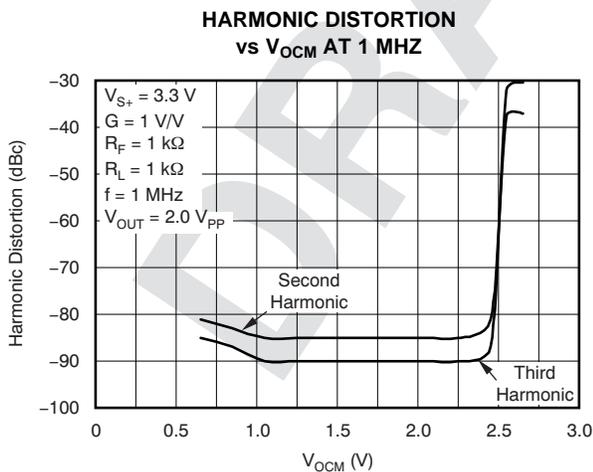


Figure 12.

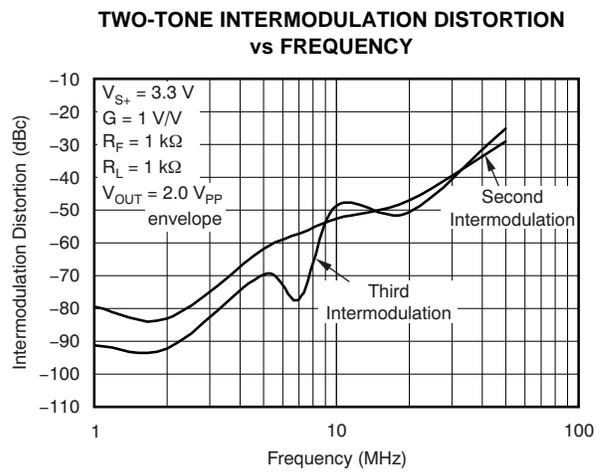


Figure 13.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3.3\text{ V}$  (continued)**

At  $V_{S+} = +3.3\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$  (differential),  $R_L = 1\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.

**SINGLE-ENDED OUTPUT VOLTAGE SWING vs LOAD RESISTANCE**

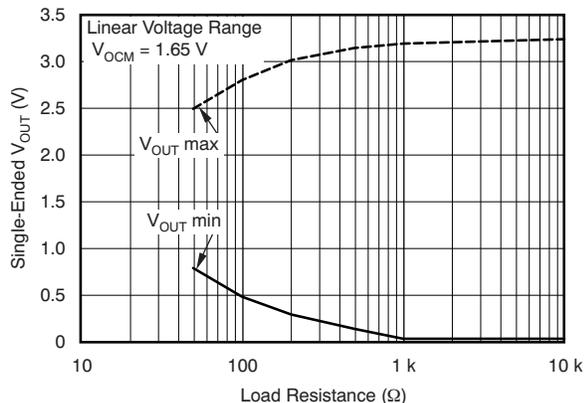


Figure 14.

**MAIN AMPLIFIER DIFFERENTIAL OUTPUT IMPEDANCE vs FREQUENCY**

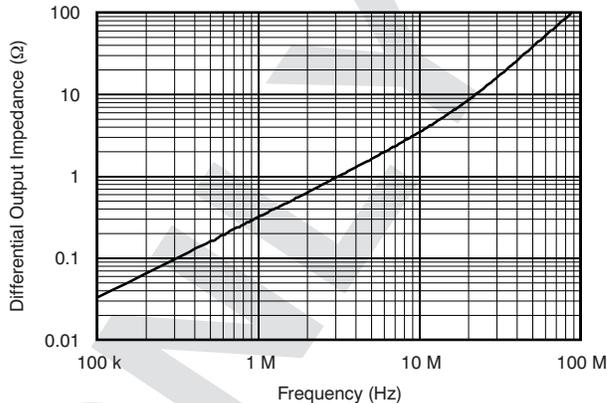


Figure 15.

**FREQUENCY RESPONSE vs  $C_{LOAD}$   
 $R_{LOAD} = 1\text{ k}\Omega$**

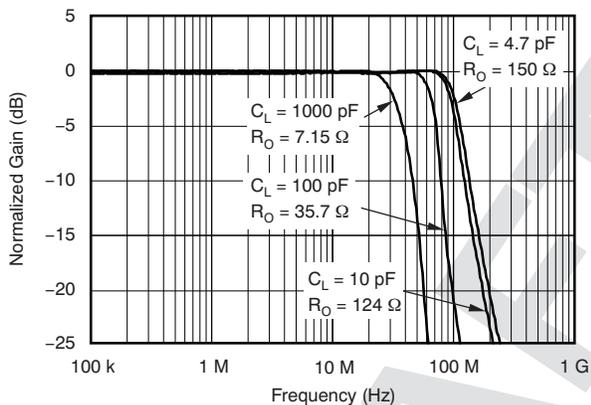


Figure 16.

**$R_O$  vs  $C_{LOAD}$   
 $R_{LOAD} = 1\text{ k}\Omega$**

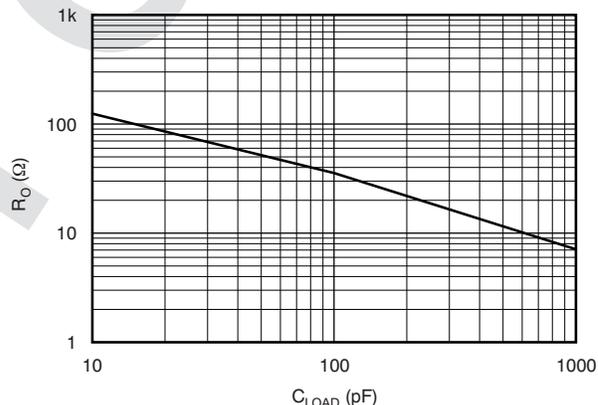


Figure 17.

**REJECTION RATIO vs FREQUENCY**

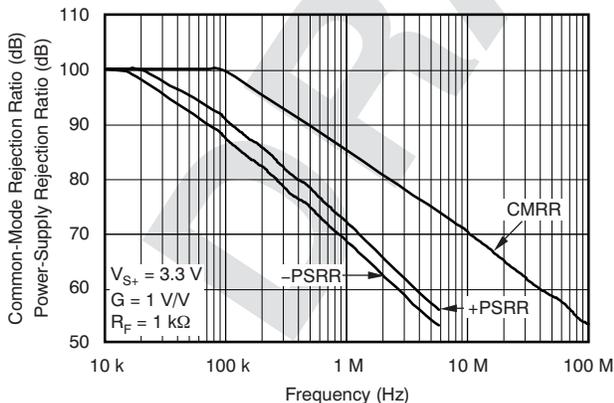


Figure 18.

**TURN-ON TIME**

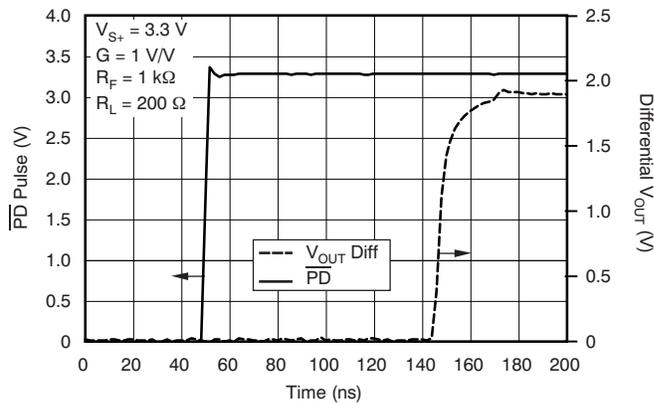


Figure 19.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3.3\text{ V}$  (continued)**

At  $V_{S+} = +3.3\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$  (differential),  $R_L = 1\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.

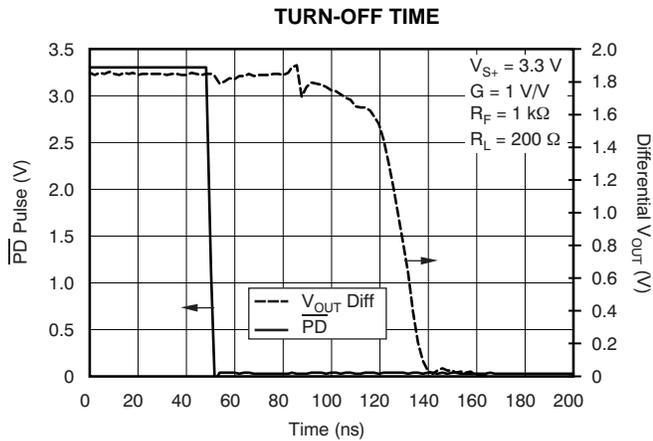


Figure 20.

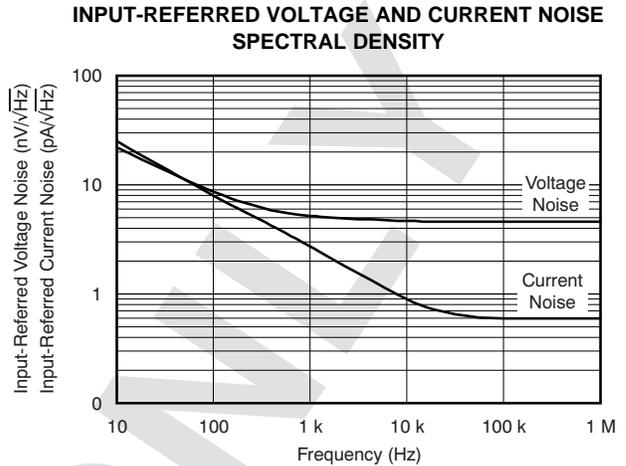


Figure 21.

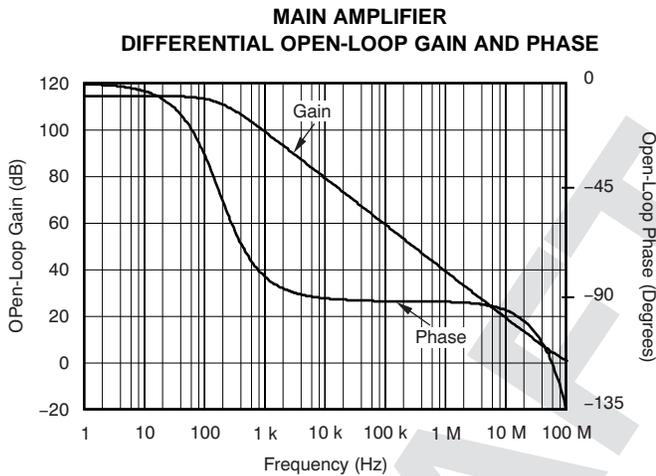


Figure 22.

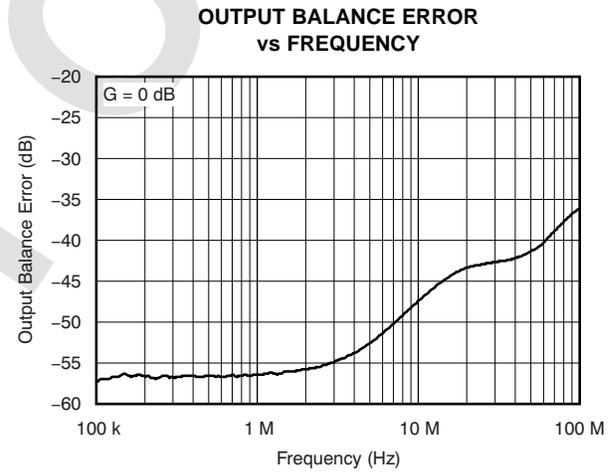


Figure 23.

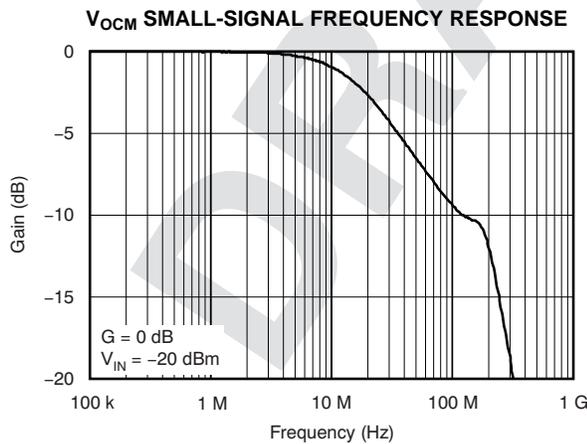


Figure 24.

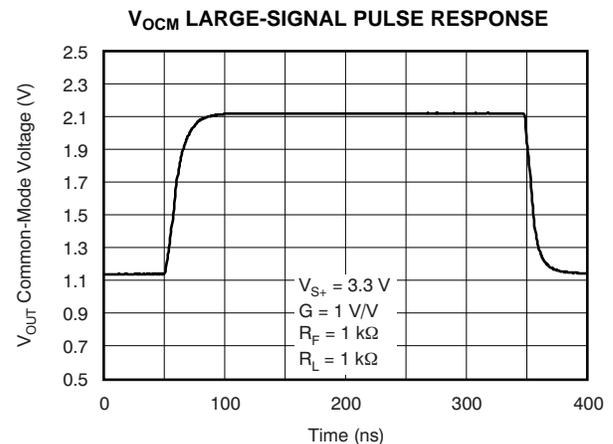
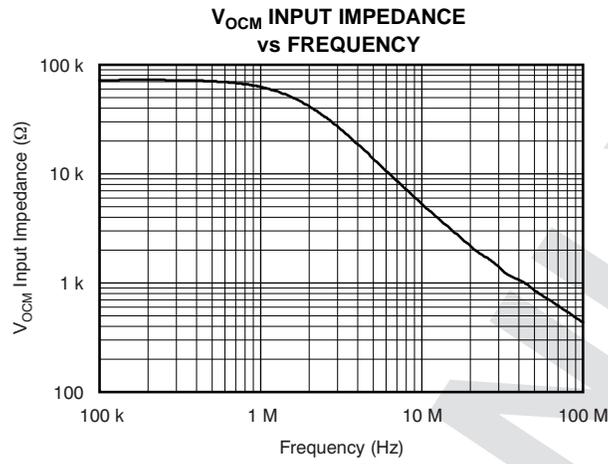


Figure 25.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3.3\text{ V}$  (continued)**

At  $V_{S+} = +3.3\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2 V_{PP}$  (differential),  $R_L = 1\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.



**Figure 26.**

## TEST CIRCUITS

### Overview

The THS4521 is tested with the test circuits shown in this section; all circuits are built using the available THS4521 evaluation module (EVM). For simplicity, power-supply decoupling is not shown; see the layout in the [Applications](#) section for recommendations. Depending on the test conditions, component values change in accordance with [Table 2](#) and [Table 3](#), or as otherwise noted. In some cases the signal generators used are ac-coupled and in others they dc-coupled 50-Ω sources. To balance the amplifier when ac-coupled, a 0.22-μF capacitor and 49.9-Ω resistor to ground are inserted across  $R_{IT}$  on the alternate input; when dc-coupled, only the 49.9-Ω resistor to ground is added across  $R_{IT}$ . A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated in a single-supply configuration as described in the [Applications](#) section with no impact on performance. Also, for most of the tests, except as noted, the devices are tested with single-ended inputs and a transformer on the output to convert the differential output to single-ended because common lab test equipment has single-ended inputs and outputs. Similar or better performance can be expected with differential inputs and outputs.

As a result of the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The **Atten** column in [Table 3](#) shows the attenuation expected from the resistor divider. When using a transformer at the output (as shown in [Figure 28](#)), the signal sees slightly more loss because of transformer and line loss; these numbers are approximate.

**Table 2. Gain Component Values for Single-Ended Input<sup>(1)</sup>**

Gain	$R_F$	$R_G$	$R_{IT}$
1 V/V	1 kΩ	1 kΩ	52.3 Ω
2 V/V	1 kΩ	487 Ω	53.6 Ω
5 V/V	1 kΩ	187 Ω	59.0 Ω
10 V/V	1 kΩ	86.6 Ω	69.8 Ω

- Gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and

50-Ω input termination.

**Table 3. Load Component Values For 1:1 Differential to Single-Ended Output Transformer<sup>(1)</sup>**

$R_L$	$R_O$	$R_{OT}$	Atten
100 Ω	24.9 Ω	Open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1 kΩ	487 Ω	52.3 Ω	31.8 dB

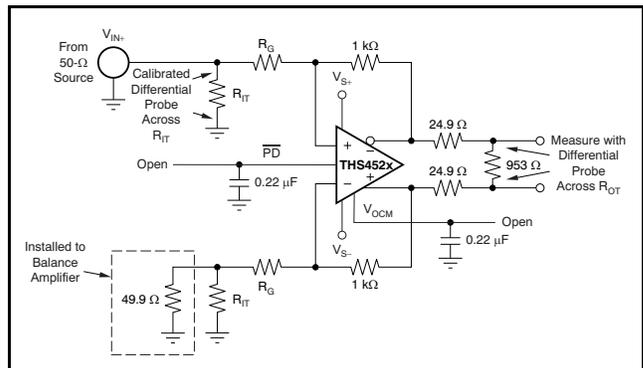
- Total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

### Frequency Response

The circuit shown in [Figure 27](#) is used to measure the frequency response of the circuit.

An HP network analyzer is used as the signal source and the measurement device. The output impedance of the HP network analyzer is dc-coupled and is 50 Ω.  $R_{IT}$  and  $R_G$  are chosen to impedance-match to 50 Ω and maintain the proper gain. To balance the amplifier, a 49.9-Ω resistor to ground is inserted across  $R_{IT}$  on the alternate input.

The output is probed using a Tektronix high-impedance differential probe across the 953-Ω resistor and referred to the amplifier output by adding back the 0.42-dB because of the voltage divider on the output.



**Figure 27. Frequency Response Test Circuit**

## Distortion

The circuit shown in Figure 28 is used to measure harmonic and intermodulation distortion of the amplifier.

An HP signal generator is used as the signal source and the output is measured with a Rhode and Schwarz spectrum analyzer. The output impedance of the HP signal generator is ac-coupled and is 50 Ω.  $R_{IT}$  and  $R_G$  are chosen to impedance match to 50 Ω and maintain the proper gain. To balance the amplifier, a 0.22-μF capacitor and 49.9-Ω resistor to ground are inserted across  $R_{IT}$  on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured and then a high-pass filter is inserted at the output to reduce the fundamental so it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single-ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

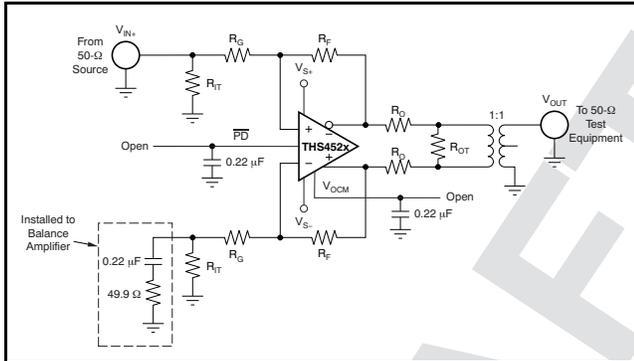


Figure 28. Distortion Test Circuit

## Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Turn-Off Time

The circuit shown in Figure 29 is used to measure slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and amplifier turn-on/turn-off time. Turn-on and turn-off time are measured with the same circuit modified for 50-Ω input impedance on the PD input by replacing the 0.22-μF capacitor with a 49.9-Ω resistor. For output impedance, the signal is injected at  $V_{OUT}$  with  $V_{IN}$  open; the drop across the 2x 49.9-Ω resistors is then used to calculate the impedance seen looking into the amplifier output.

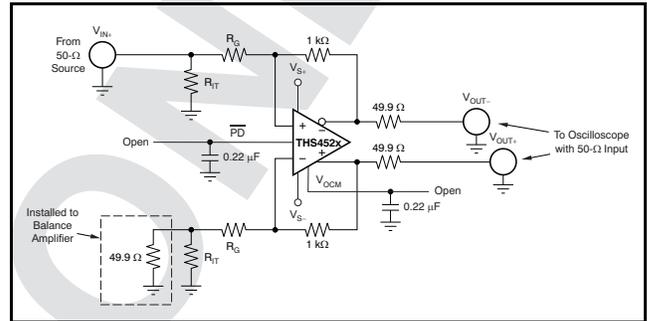


Figure 29. Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive Recovery,  $V_{OUT}$  Swing, and Turn-On/Turn-Off Test Circuit

### Common-Mode and Power-Supply Rejection

The circuit shown in Figure 30 is used to measure the CMRR. The signal from the network analyzer is applied common-mode to the input. Figure 31 is used to measure the PSRR of  $V_{S+}$  and  $V_{S-}$ . The power supply under test is applied to the network analyzer dc offset input. For both CMRR and PSRR, the output is probed using a Tektronix high-impedance differential probe across the 953- $\Omega$  resistor and referred to the amplifier output by adding back the 0.42-dB as a result of the voltage divider on the output. For these tests, the resistors are matched for best results.

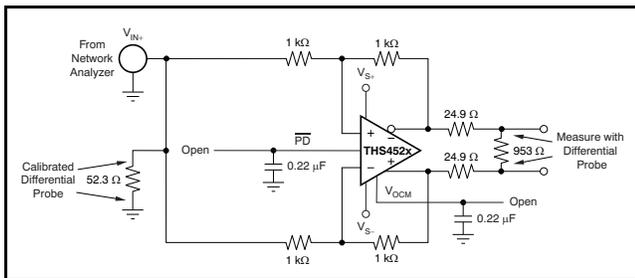


Figure 30. CMRR Test Circuit

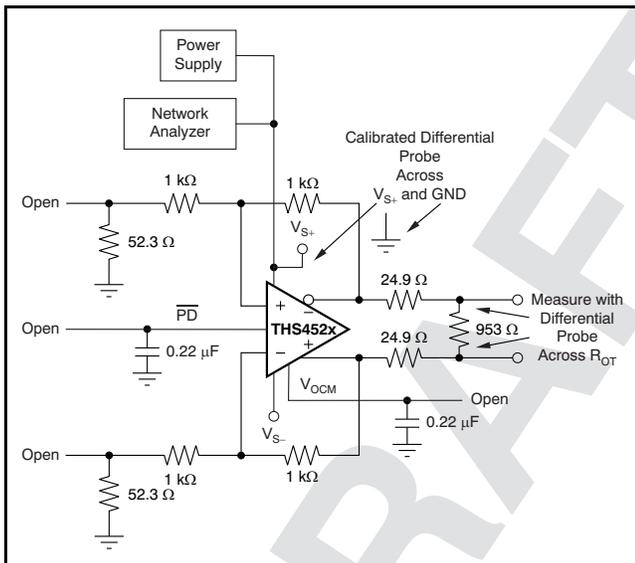


Figure 31. PSRR Test Circuit

### $V_{OCM}$ Input

The circuit illustrated in Figure 32 is used to measure the frequency response and input impedance of the  $V_{OCM}$  input. Frequency response is measured using a Tektronix high-impedance differential probe, with  $R_{CM} = 0 \Omega$  at the common point of  $V_{OUT+}$  and  $V_{OUT-}$ , formed at the summing junction of the two matched 499- $\Omega$  resistors, with respect to ground. The input impedance is measured using a Tektronix high-impedance differential probe at the  $V_{OCM}$  input with  $R_{CM} = 10 \text{ k}\Omega$  and the drop across the 10-k $\Omega$  resistor is used to calculate the impedance seen looking into the amplifier  $V_{OCM}$  input.

The circuit shown in Figure 33 measures the transient response and slew rate of the  $V_{OCM}$  input. A 1-V step input is applied to the  $V_{OCM}$  input and the output is measured using a 50- $\Omega$  oscilloscope input referenced back to the amplifier output.

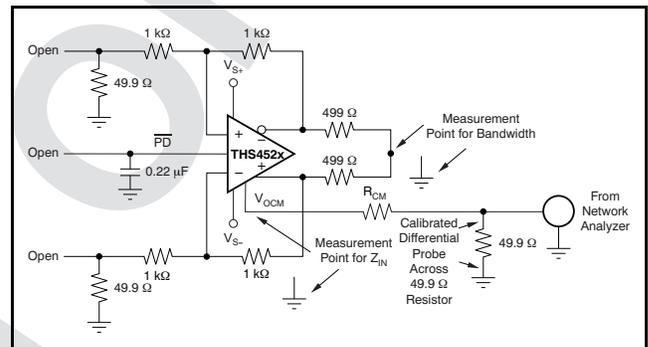


Figure 32.  $V_{OCM}$  Input Test Circuit

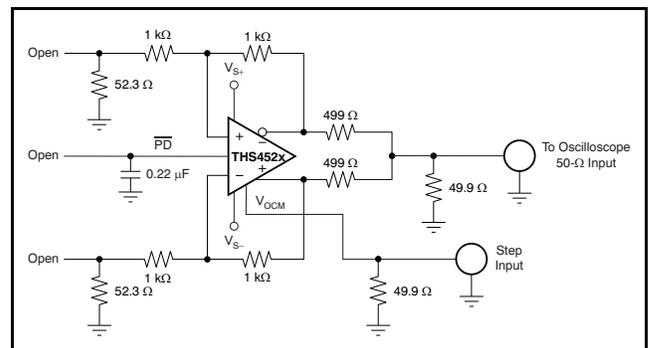


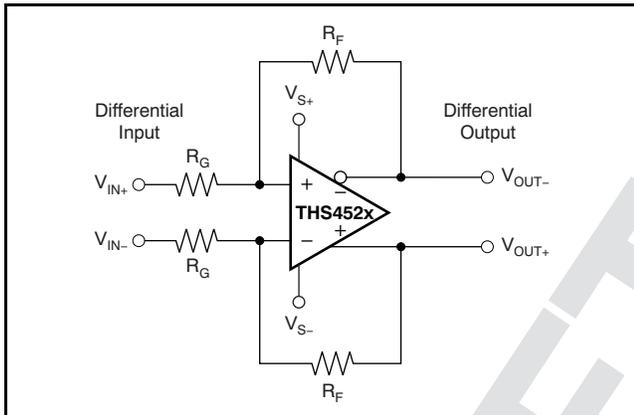
Figure 33.  $V_{OCM}$  Transient Response and Slew Rate Test Circuit

## APPLICATION INFORMATION

The following circuits show application information for the THS4521. For simplicity, power-supply decoupling capacitors are not shown in these diagrams; see the [EVM and Layout Recommendations](#) section for suggested guidelines. For more details on the use and operation of fully differential op amps, refer to the Application Report [Fully-Differential Amplifiers \(SLOA054\)](#), available for download from the TI web site at [www.ti.com](http://www.ti.com).

### Differential Input to Differential Output Amplifier

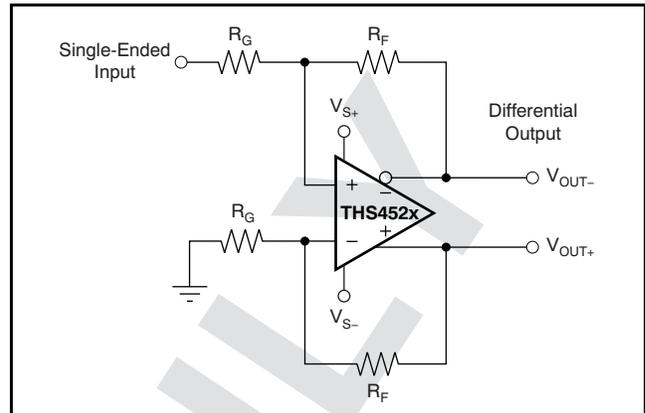
The THS4521 is fully-differential operational amplifiers that can be used to amplify differential input signals to differential output signals. [Figure 34](#) shows a basic block diagram of the circuit ( $V_{OCM}$  and PD inputs not shown). The gain of the circuit is set by  $R_F$  divided by  $R_G$ .



**Figure 34. Differential Input to Differential Output Amplifier**

### Single-Ended Input to Differential Output Amplifier

The THS4521 can also amplify and convert single-ended input signals to differential output signals. [Figure 35](#) illustrates a basic block diagram of the circuit ( $V_{OCM}$  and PD inputs not shown). The gain of the circuit is again set by  $R_F$  divided by  $R_G$ .



**Figure 35. Single-Ended Input to Differential Output Amplifier**

### Input Common-Mode Voltage Range

The input common-mode voltage of a fully-differential op amp is the voltage at the + and – input pins of the device.

It is important to not violate the input common-mode voltage range ( $V_{ICR}$ ) of the op amp. Assuming the op amp is in linear operation, the voltage across the input pins is only a few millivolts at most. Therefore, finding the voltage at one input pin determines the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by [Equation 1](#):

$$\left( V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left( V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \quad (1)$$

To determine the  $V_{ICR}$  of the op amp, the voltage at the negative input is evaluated at the extremes of  $V_{OUT+}$ . As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

### Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the  $V_{OCM}$  pin. The internal common-mode control circuit maintains the output common-mode voltage within 5-mV offset (typ) from the set voltage. If left unconnected, the common-mode set point is set to midsupply by internal circuitry, which may be overdriven from an external source.

Figure 36 represents the  $V_{OCM}$  input. The internal  $V_{OCM}$  circuit has typically 23 MHz of  $-3$  dB bandwidth, which is required for best performance, but it is intended to be a dc bias input pin. A  $0.22\text{-}\mu\text{F}$  bypass capacitor is recommended on this pin to reduce noise. The external current required to overdrive the internal resistor divider is given approximately by the formula in Equation 2:

$$I_{EXT} = \frac{2V_{OCM} - (V_{S+} - V_{S-})}{50\text{ k}\Omega}$$

where:

- $V_{OCM}$  is the voltage applied to the  $V_{OCM}$  pin (2)

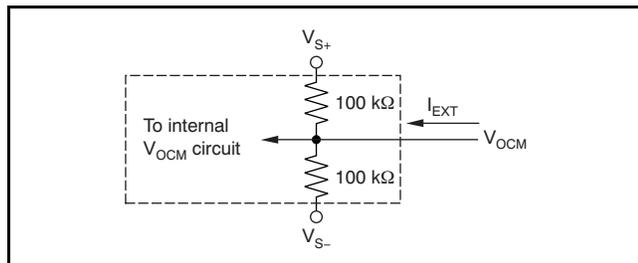


Figure 36.  $V_{OCM}$  Input Circuit

### Typical Performance Variation with Supply Voltage

The THS4521 provides excellent performance across the specified power-supply range of 2.5 V to 3.3 V with only minor variations. The input and output voltage compliance ranges track with the power supply in nearly a 1:1 correlation. Other changes can be observed in slew rate, output current drive, open-loop gain, bandwidth, and distortion.

### Single-Supply Operation

To facilitate testing with common lab equipment, the THS4521EVM allows for split-supply operation; most of the characterization data presented in this data sheet is measured using split-supply power inputs. The device can easily be used with a single-supply power input without degrading performance.

Figure 37 shows a dc-coupled single-supply circuit with single-ended inputs. This circuit can also be applied to differential input sources.

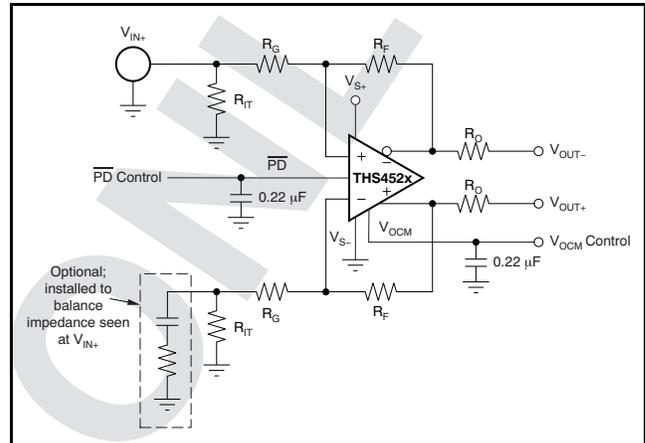


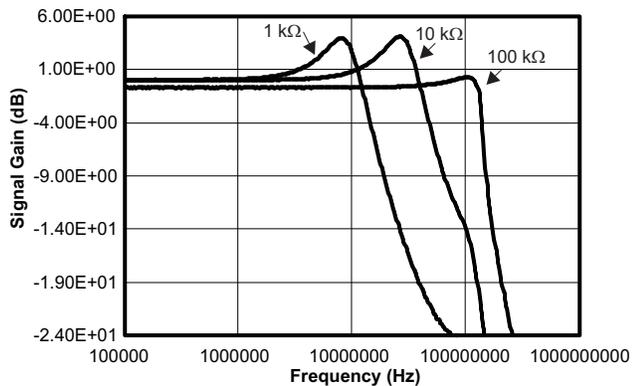
Figure 37. THS4521 DC-Coupled Single-Supply with Single-Ended Inputs

The input common-mode voltage range of the THS4521 is designed to include the negative supply voltage. In the circuit shown in Figure 37, the signal source is referenced to ground.  $V_{OCM}$  is set by an external control source or, if left unconnected, the internal circuit defaults to midsupply. Together with the input impedance of the amplifier circuit,  $R_{IT}$  provides input termination, which is also referenced to ground.

Note that  $R_{IT}$  and optional matching components are added to the alternate input to balance the impedance at signal input.

### Low-Power Applications and the Effects of Resistor Values on Bandwidth

For low-power operation, it may be necessary to increase the gain setting resistors values to limit current consumption and not load the source. Using larger value resistors lowers the bandwidth of the THS4521 as a result of the interactions between the resistors, the device parasitic capacitance, and printed circuit board (PCB) parasitic capacitance.



**Figure 38. THS4521 Frequency Response with Various Gain Setting and Load Resistor Values**

### Driving Capacitive Loads

The THS4521 is designed for a nominal capacitive load of 1 pF on each output to ground. When driving capacitive loads greater than 1 pF, it is recommended to use small resistors ( $R_O$ ) in series with the output, placed as close to the device as possible. Without  $R_O$ , capacitance on the output interacts with the output impedance of the amplifier and causes phase shift in the loop gain of the amplifier that reduces the phase margin. This reduction in phase margin results in frequency response peaking; overshoot, undershoot, and/or ringing when a step or square-wave signal is applied; and may lead to instability or oscillation. Inserting  $R_O$  isolates the phase shift from the loop gain path and restores the phase margin, but it also limits bandwidth.

## LAYOUT RECOMMENDATIONS

It is recommended to follow the layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. Follow these general guidelines:

1. Signal routing should be direct and as short as possible into and out of the op amp circuit.
2. The feedback path should be short and direct.
3. Ground or power planes should be removed from directly under the amplifier input and output pins.
4. An output resistor is recommended in each output lead, placed as near to the output pins as possible.
5. Two 0.1- $\mu$ F power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 10- $\mu$ F power-supply decoupling capacitors should be placed within 1 inch of the device and can be shared among multiple analog devices.
7. A 0.22- $\mu$ F capacitor should be placed between the  $V_{OCM}$  input pin and ground near to the pin. This capacitor limits noise coupled into the pin.
8. The  $\overline{PD}$  pin uses TTL logic levels; a bypass capacitor is not necessary if actively driven, but can be used for robustness in noisy environments whether driven or not.

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