



# Micron CMOS Sensor Daughter Card for DM642 Evaluation Module

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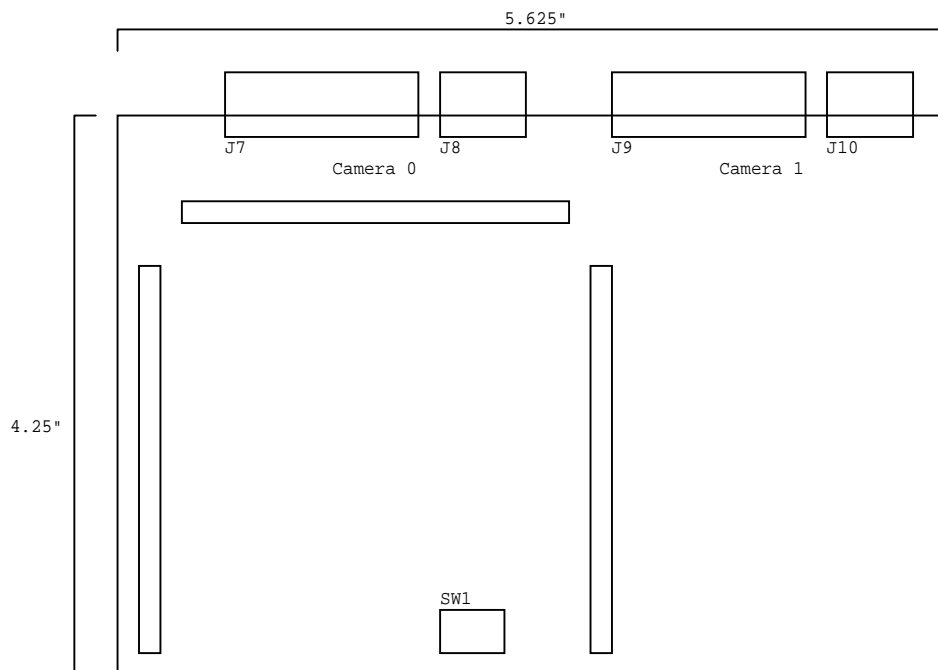
- 1) Contents, Notes, & Revisions
- 2) EMIF DC Interface
- 3) VPO/1 DC Interface
- 4) VP2 DC Interface
- 5) Sensor Connection
- 6) Bus Switches for VPO
- 7) Bus Switches for VP1

### Notes:

- 1) RESISTANCE VALUES ARE IN OHMS.
- 2) CAPACITANCE VALUES ARE IN MICRO-FARADS (uF).
- 3) BOARD PROPERTIES
  - A. ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE
  - B. 50 OHM MATCHED IMPEDANCE FOR DIGITAL LINES.
  - C. OUTER LAYERS 0.5 OZ CU & 0.5 OZ AU PLATING
  - D. INNER LAYERS 1.0 OZ CU
  - E. FR4 BOARD MATERIAL
  - F. MINIMUM TRACE WIDTH/SPACING 4/8 MILS
  - G. MINIMUM VIA SIZE 10/19 MIL
  - H. APPROXIMATE BOARD SIZE 3.5 x 5.125 INCHES
  - I. THERMAL RELIEFS SHOULD NOT BE USED

## Revision History

Rev. #	Description	Date	Approval
0.1	Preliminary Schematics Completed	3/15/04	JBF
1.1	- Fixed DC_EXP_CAPTUREx_EN# issue with respect to Bus Switches - Fixed Muxing for 16-bit Mode - Added TPs to I2C - Fixed PCA9540B footprint - Adjusted Size of DC - Use Edge Connectors for Camera 0/1 Headers - Added Gnd TPs	7/14/04	JBF



- J7 and J9 are 13x2 Edge Connectors
- J8 and J10 are 7x2 Edge Connectors
- Label J7 and J8 as Camera 0, J9 and J10 as Camera 1



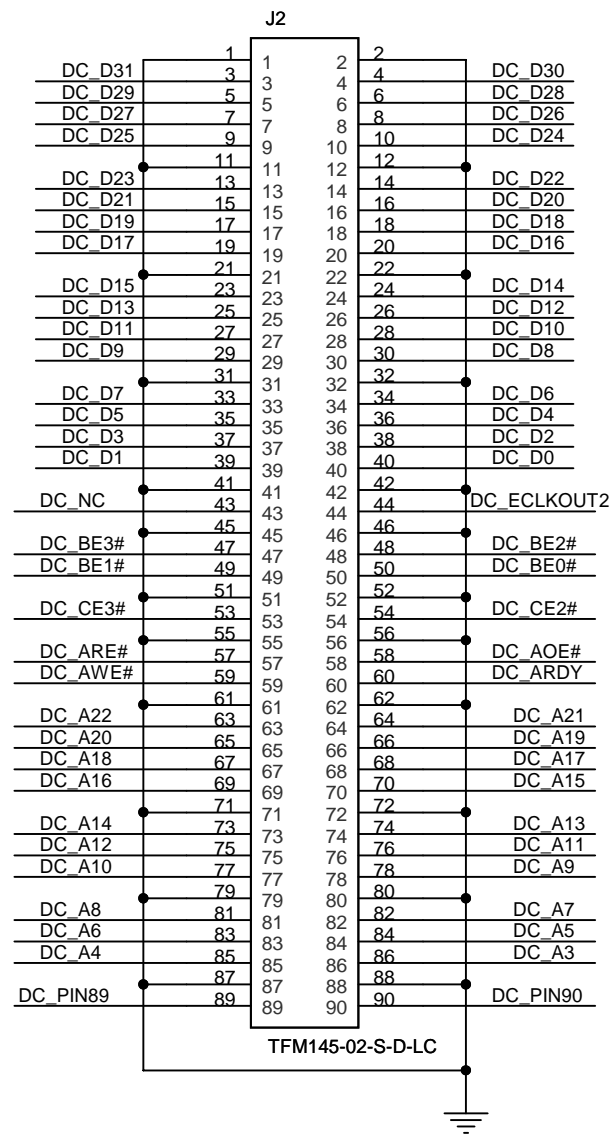
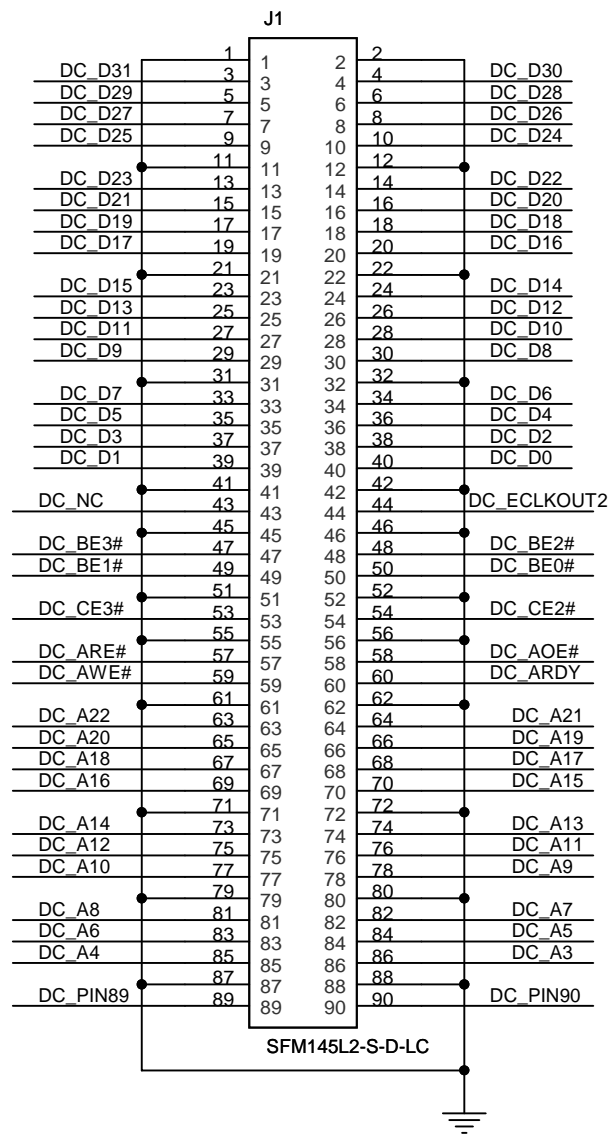
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Description: Contents, Notes, & Revisions

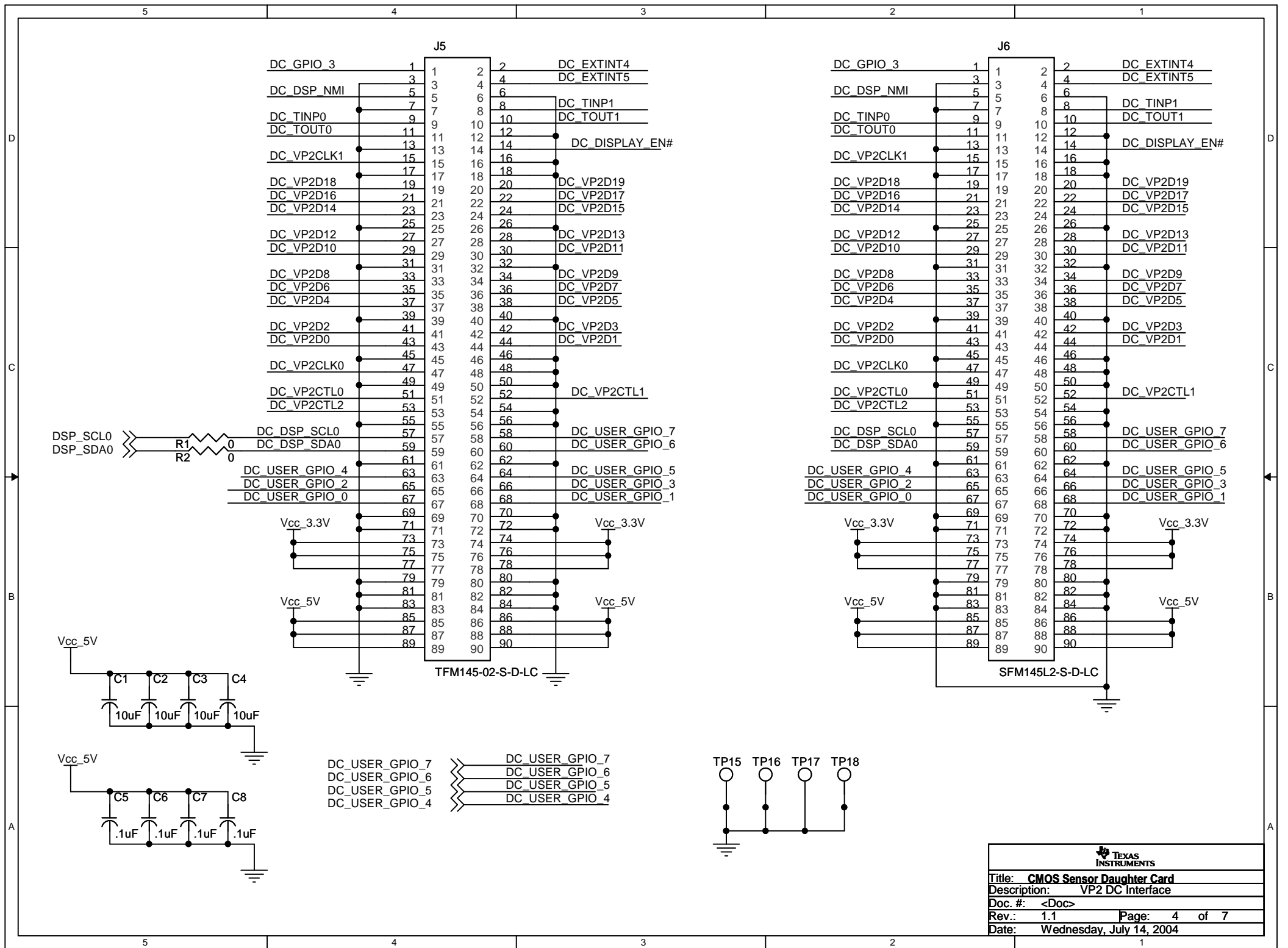
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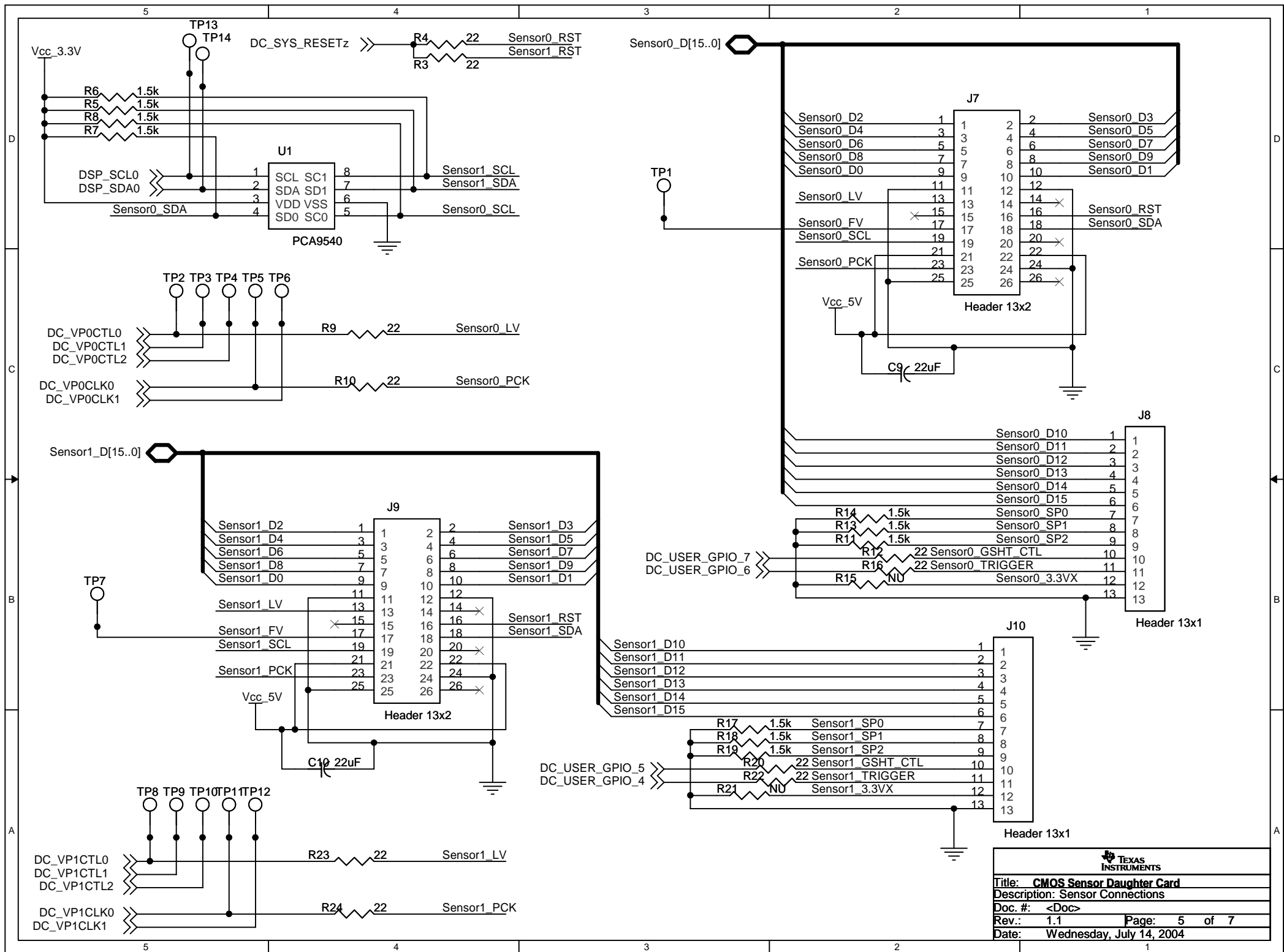
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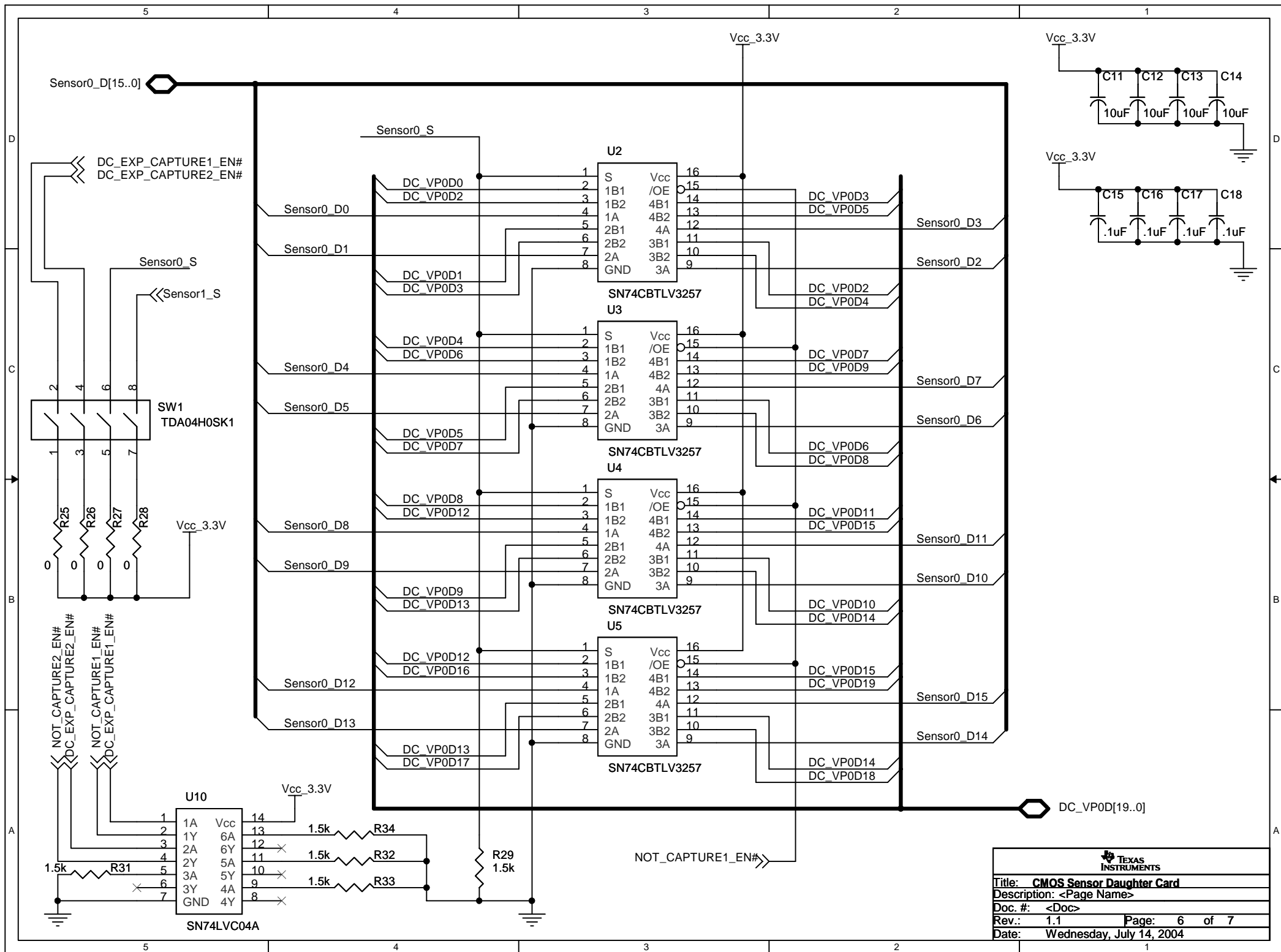
Date: Wednesday, July 14, 2004











Sensor1\_D[15..0]

Sensor1\_S >>

Sensor1\_D0

Sensor1\_D1

Sensor1\_D4

Sensor1\_D5

Sensor1\_D8

Sensor1\_D9

Sensor1\_D12

Sensor1\_D13

U6

SN74CBTLV3257  
U7

SN74CBTLV3257  
U8

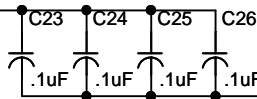
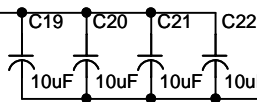
SN74CBTLV3257  
U9

SN74CBTLV3257

Vcc\_3.3V

Vcc\_3.3V

Vcc\_3.3V



R30  
1.5k

NOT\_CAPTURE2\_EN# >>



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