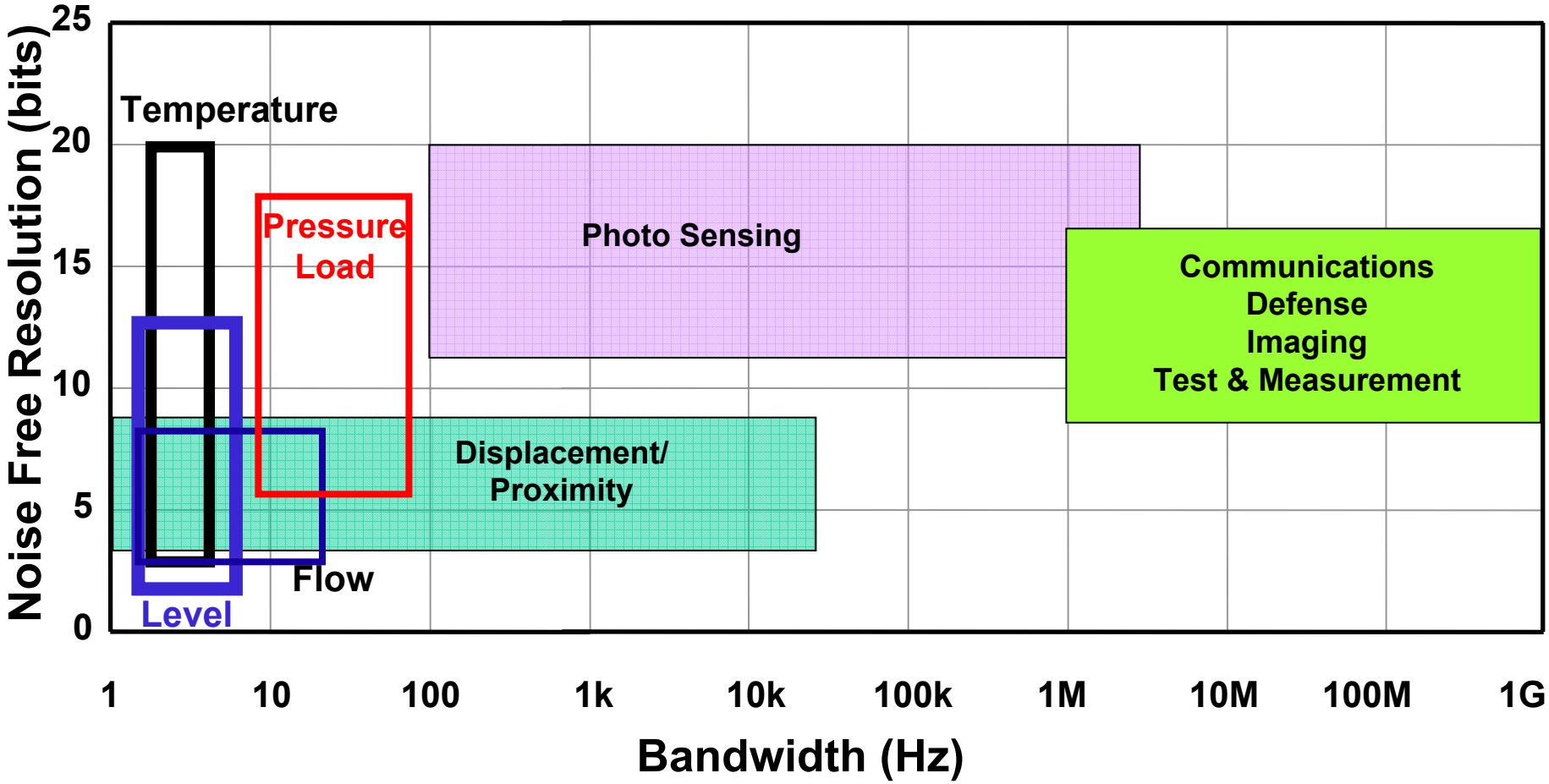
Choose the right A/D converter for your application

Agenda

- What are the Signal Frequencies
  - Analog Classes of applications
  - Frequency ranges of ADCs
- Nuts and Bolts of ΔΣ (Delta-Sigma) Converters
  - ΔΣ-Converter Core and Auxiliary ΔΣ-Functions
  - Applications for the ΔΣ Converter
- The SAR ADC
  - Input Stage Dynamics
  - Applications for the SAR Converter
- The High-speed Pipeline Topology
  - Driving the Capacitive Input Stage
  - Applications for the Pipeline Converter
- Conclusion

Real World vs. Bandwidth



ADC Architectures

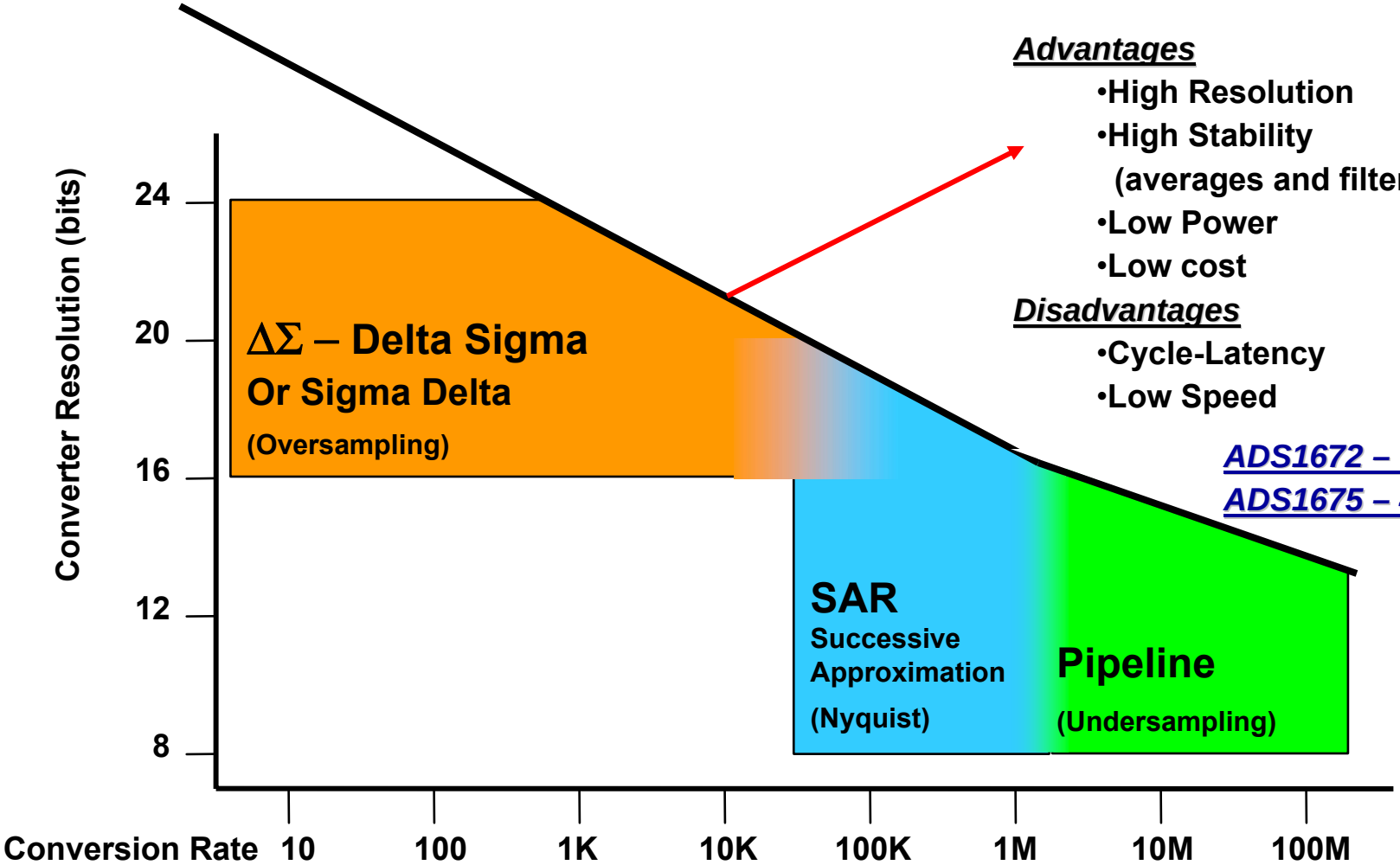
- There are many different ADC Architectures
  - Successive Approximation (SAR)
  - Delta-Sigma ($\Delta\Sigma$)
  - Pipeline
  - (Flash)

- Delta-Sigma converters determine the digital word by
  - Oversampling
  - Applying Digital Filtering

- SARs determine the digital word by
  - Sampling the input signal
  - Using an iterative process

- Pipeline converters determine digital word by
  - Undersampling
  - With Sample / Gain Algorithm Topology
  - Multiple stages / Larger Cycle-latency

ADC Technologies - ΔΣ



Advantages

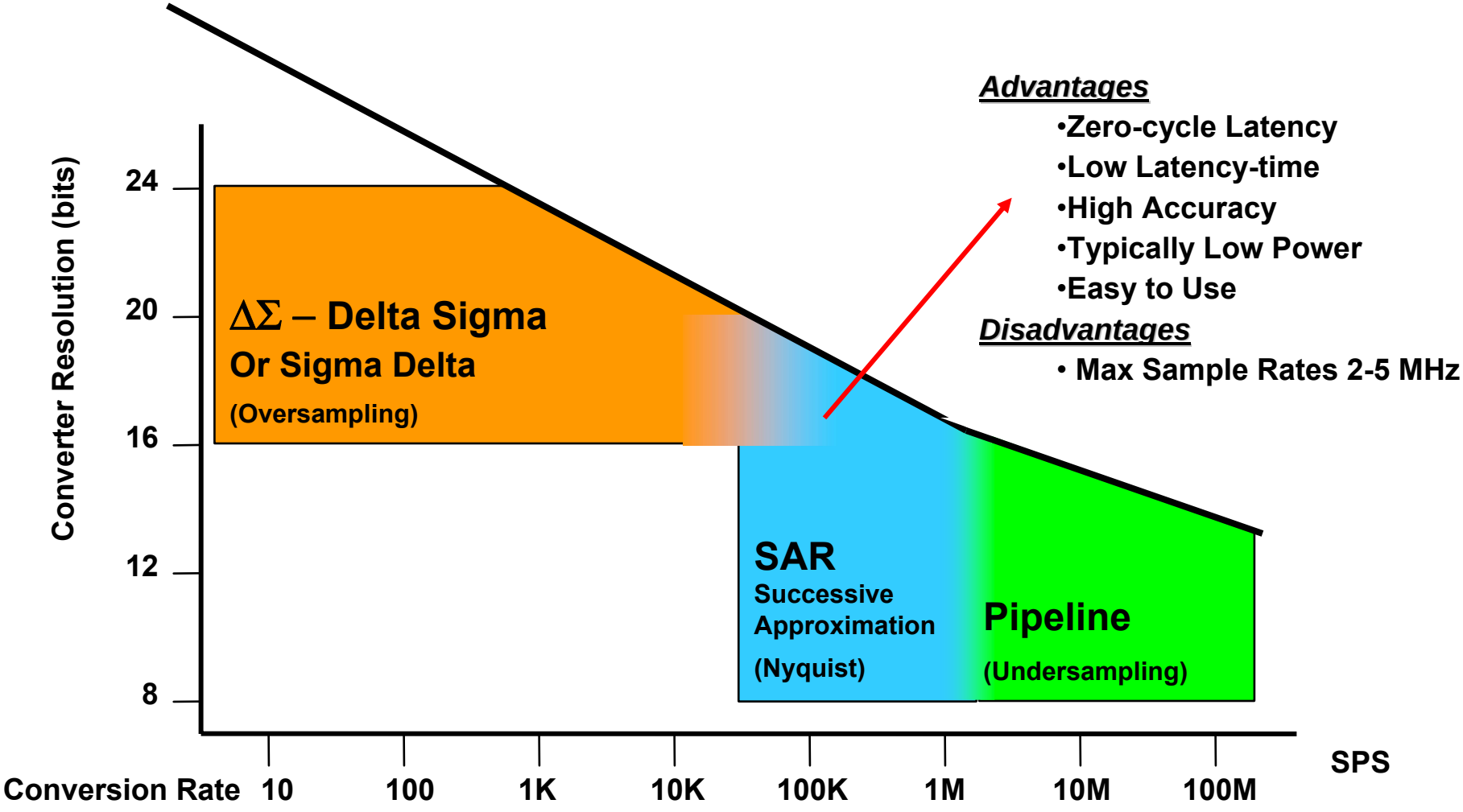
- High Resolution
- High Stability
  (averages and filters out noise)
- Low Power
- Low cost

Disadvantages

- Cycle-Latency
- Low Speed

ADS1672 – 625k, 24-bit
ADS1675 – 4 M, 24-bit

ADC Technologies - SAR



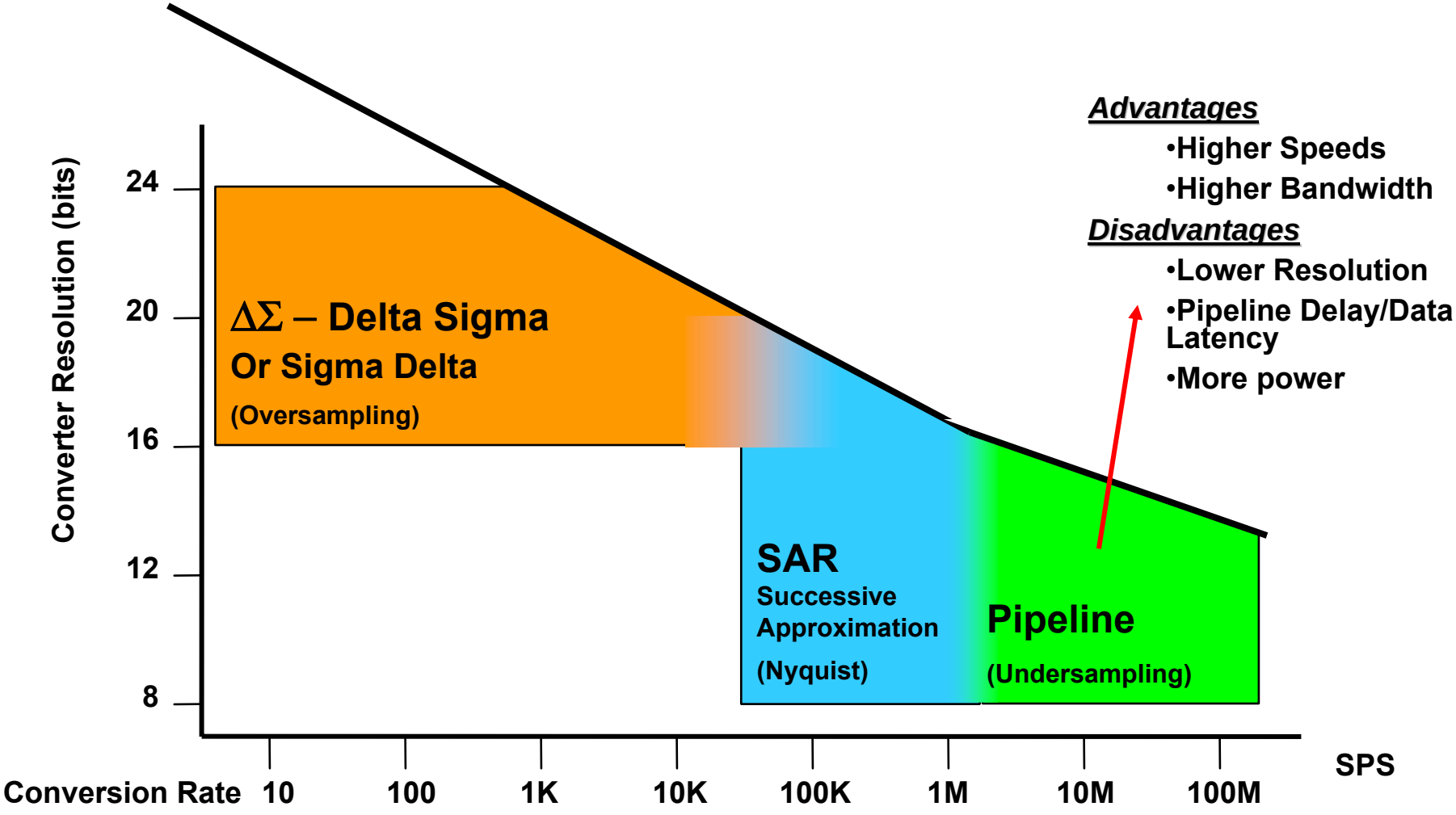
Advantages

- Zero-cycle Latency
- Low Latency-time
- High Accuracy
- Typically Low Power
- Easy to Use

Disadvantages

- Max Sample Rates 2-5 MHz

ADC Technologies - pipeline



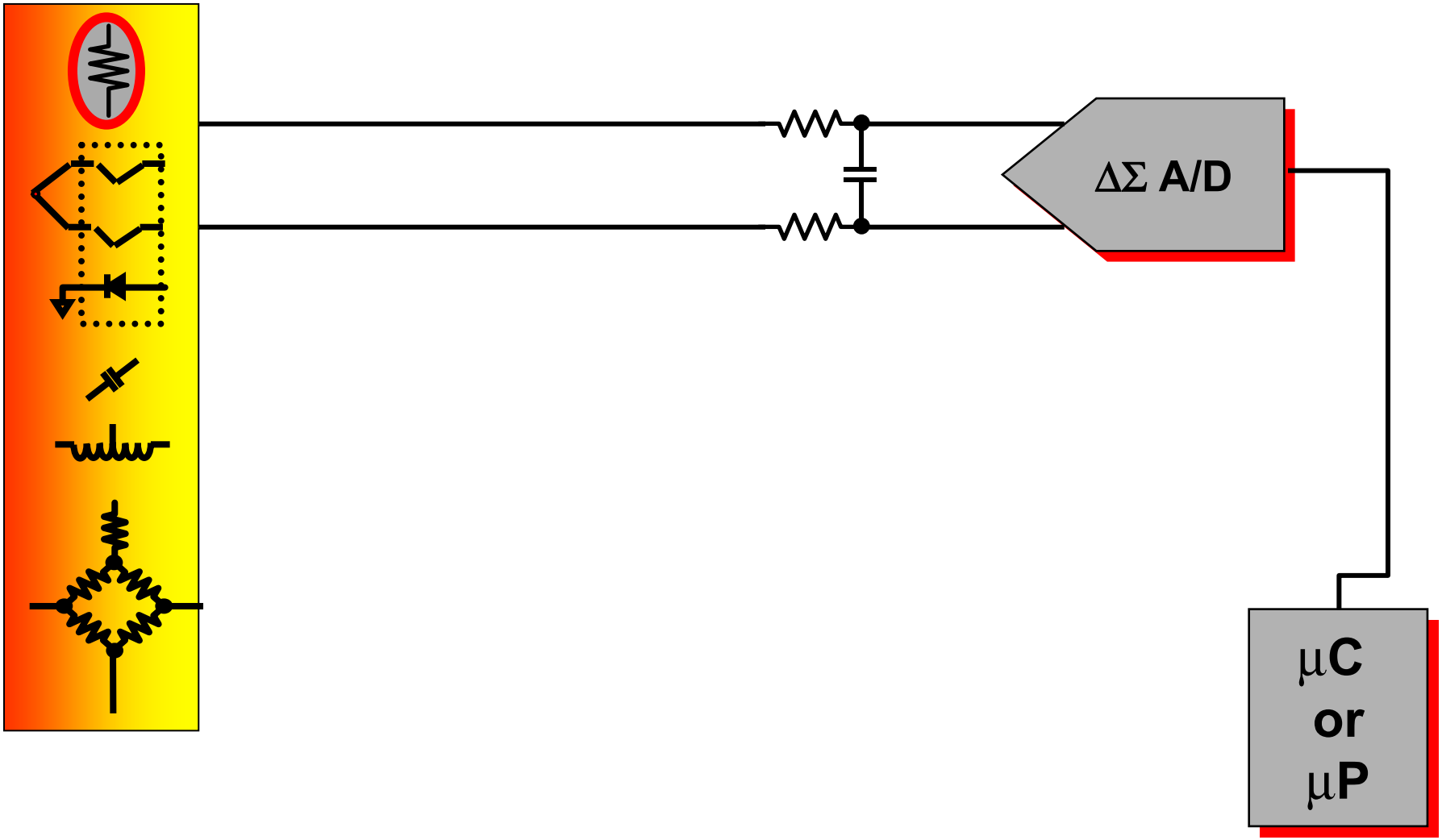
Selecting ADC Topology

ADC Topology	*F Conversion*	*Resolution*	*Comments*
SAR	**≤ 4Msps** **≤ 1.25Msps**	**≤ 16-bit** **≤ 18-bit**	**Simple operation, low cost, low power.**
Delta-Sigma	**≤ 4ksps** **≤ 4Msps** **≤ 10Msps**	**≤ 31-bit** **≤ 24-bit** **≤ 16-bit**	**Moderate cost.**
Pipeline	**≤ 200Msps** **≤ 250Msps** **≤ 550Msps**	**≤ 16-bit** **≤ 14-bit** **≤ 12-bit**	**Fast, expensive, higher power requirements.**

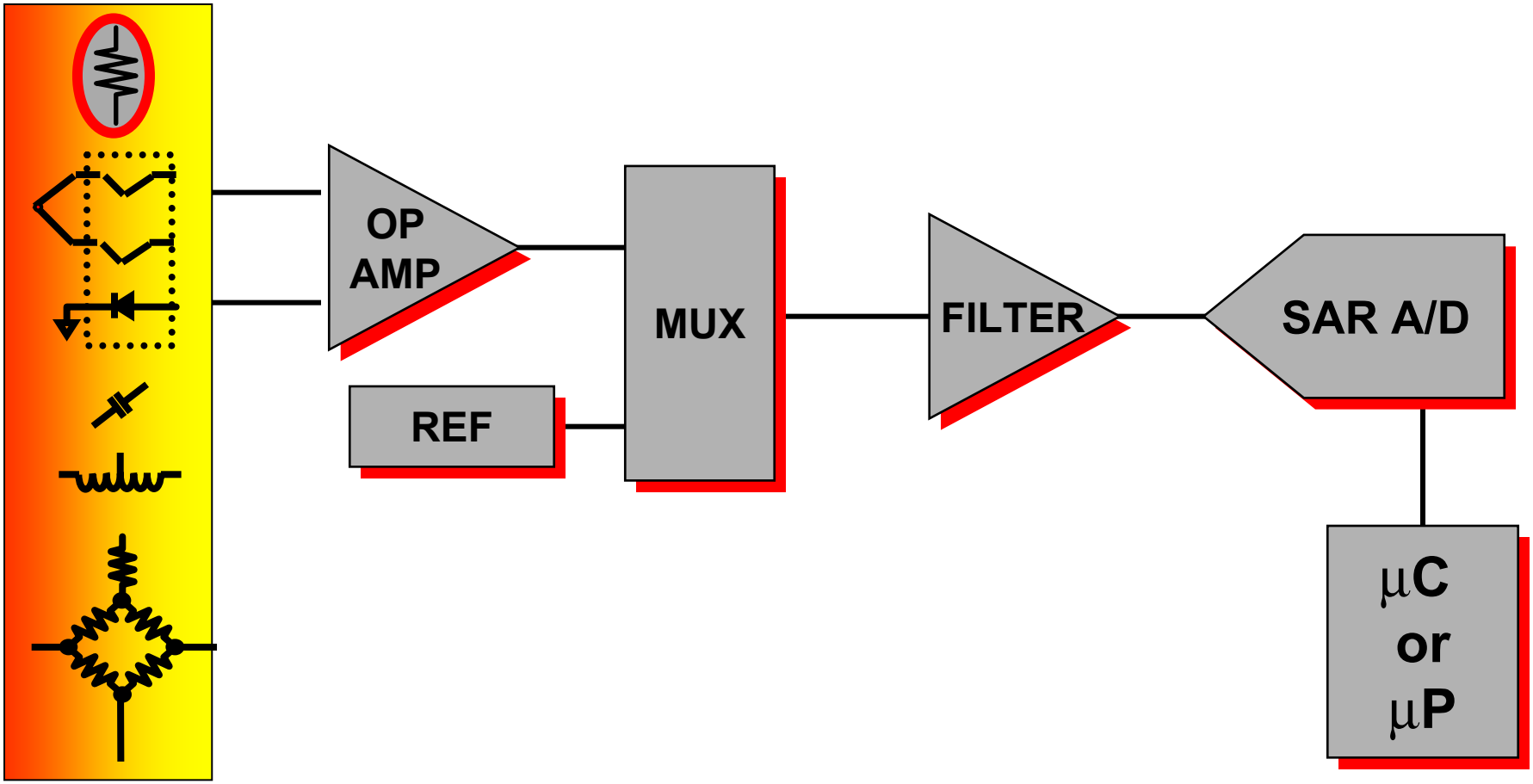
Which ADC Architecture to Use??

Characteristic	Pipelined	SAR	Delta Sigma
Throughput (samples/sec)	1	2	3
Resolution (ENOB)	3	2	1
Latency (Sample-to-Output)	2	1	3
Suitability for converting Multiple Signals per ADC	2	1	3
Capability to convert non-periodic multiplexed signals	2	1	3
Simplified anti-aliasing filter requirements			**
Power Consumption	Scales with Sample Rate or Constant	Scales with Sample Rate	Constant

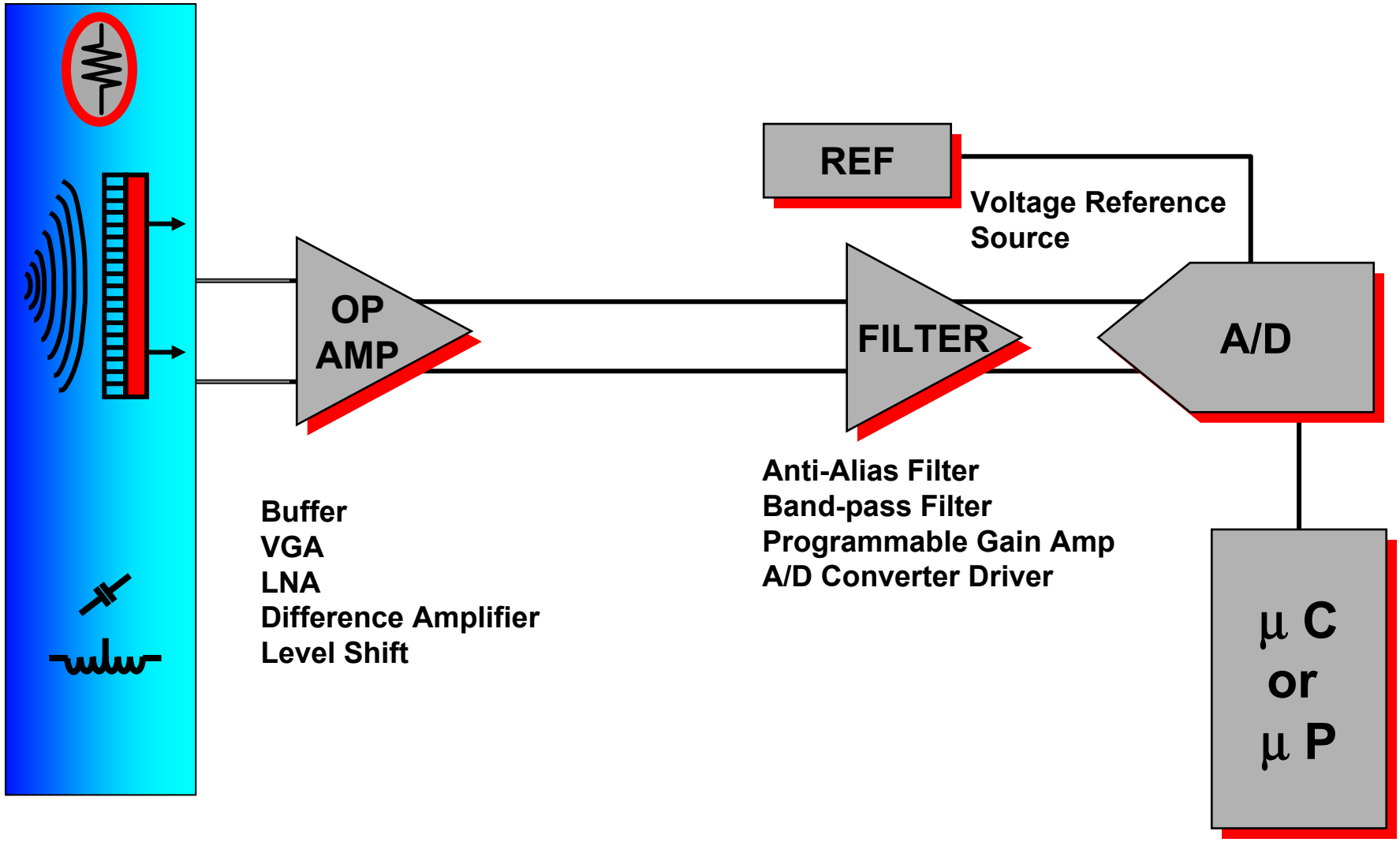
Where to Find Low Freq ADCs



Where to Find Middle Freq ADCs



Where to Find High Freq ADCs



Resolution

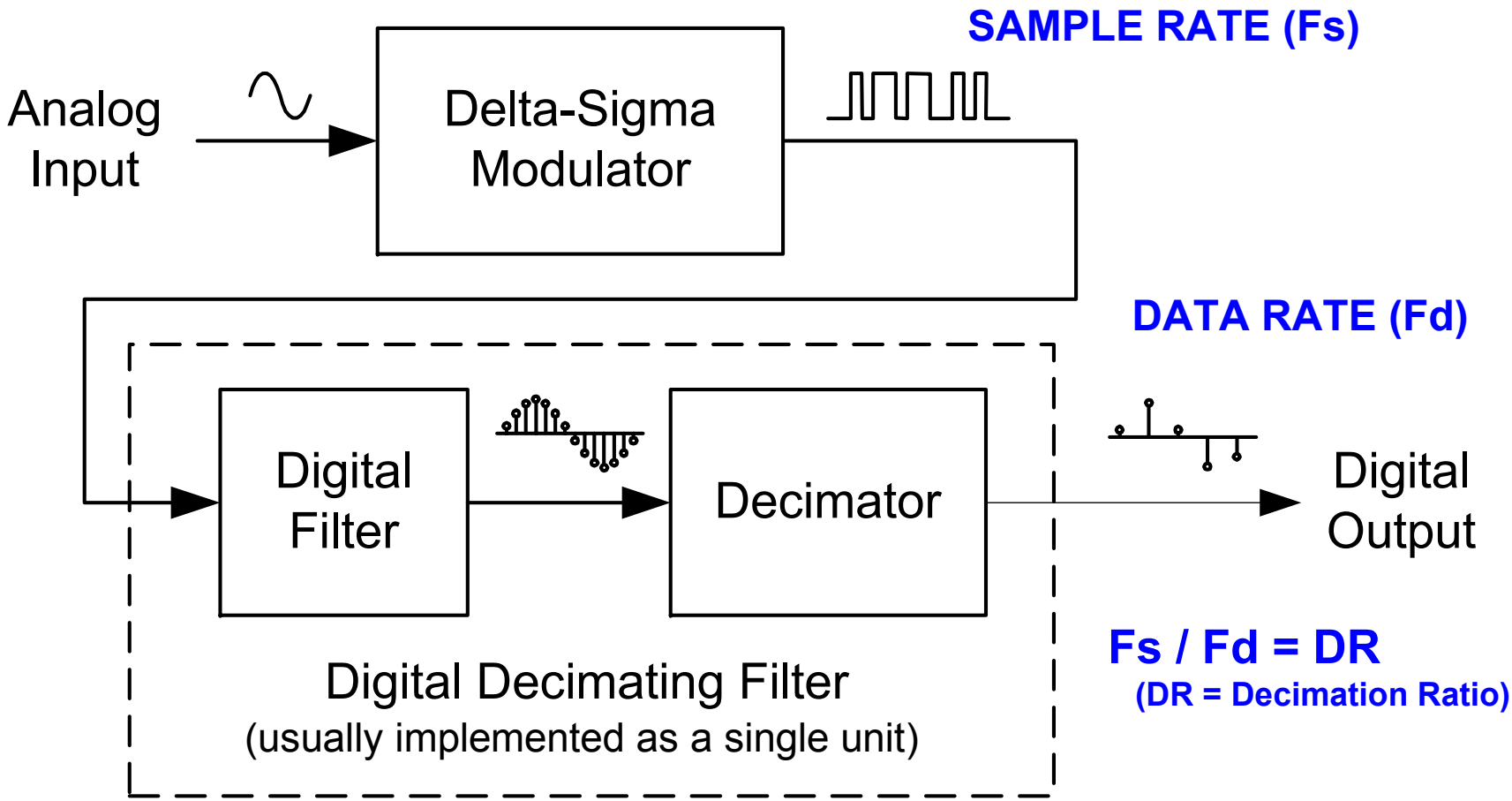
RESOLUTION N	2^N	VOLTAGE of LSB (10V FS)	ppm FS	% FS	dB FS
2-bit	4	2.5 V	250,000	25	-12
4-bit	16	625 mV	62,500	6.25	-24
6-bit	64	156 mV	15,625	1.56	-36
8-bit	256	39.1 mV	3,906	0.39	-48
10-bit	1,024	9.77 mV (10 mV)	977	0.098	-60
12-bit	4,096	2.44 mV	244	0.024	-72
14-bit	16,384	610 µV	61	0.0061	-84
16-bit	65,536	153 µV	15	0.0015	-96
18-bit	262,144	38 µV	4	0.0004	-108
20-bit	1,048,576	9.54 µV (10 µV)	1	0.0001	-120
22-bit	4,194,304	2.38 µV	0.24	0.000024	-132
24-bit	16,777,216	596 nV*	0.06	0.000006	-144

*600nV is the Johnson Noise in a 10kHz BW of a 2.2kΩ Resistor @ 25°C

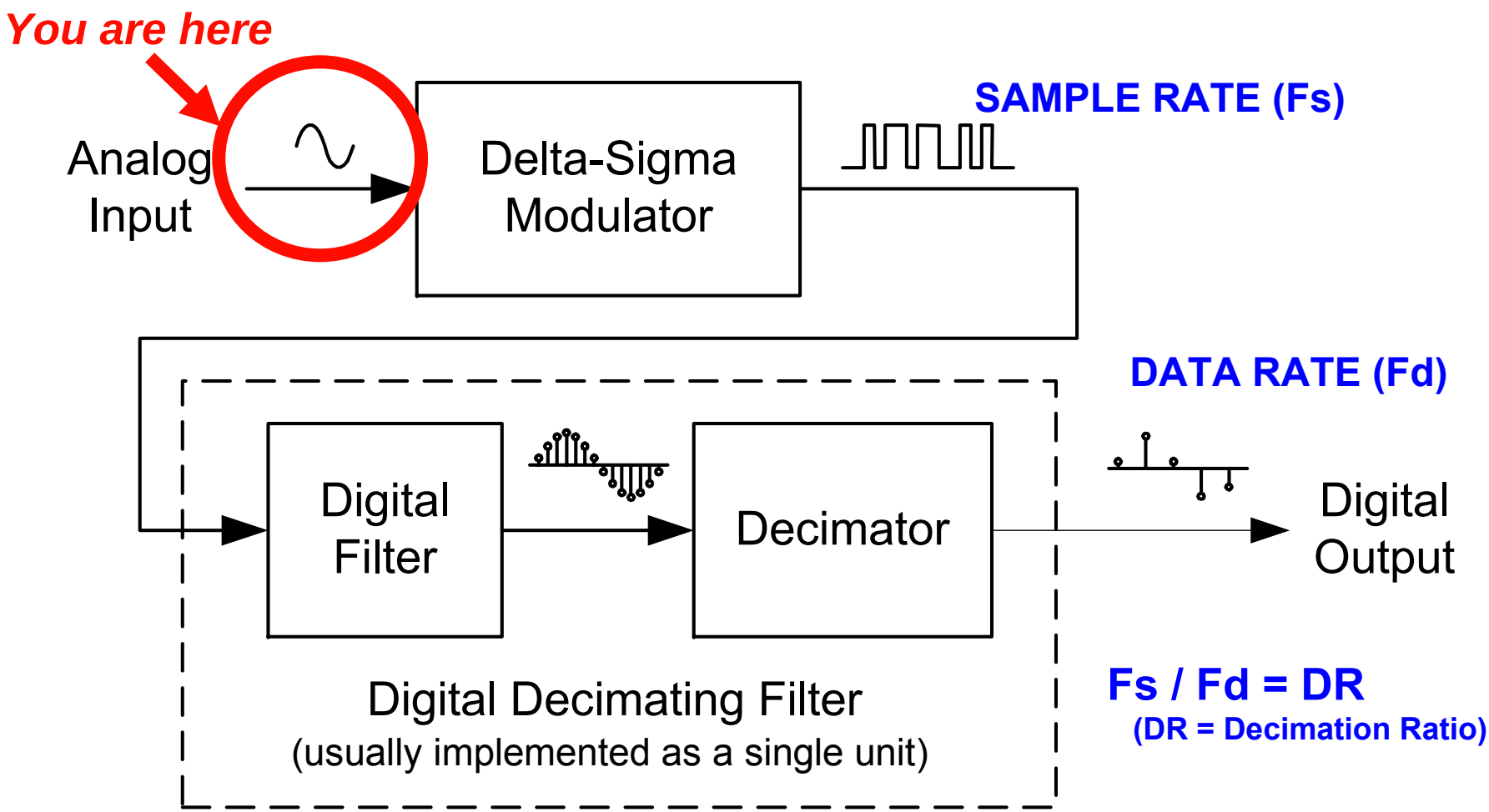
Agenda

- What are the Signal Frequencies
  - Analog Classes of applications
  - Frequency ranges of ADCs
- Nuts and Bolts of Delta-Sigma Converters
  - $\Delta\Sigma$ Converter Core and Auxiliary $\Delta\Sigma$ Functions
  - Applications for the $\Delta\Sigma$ Converter
- The SAR ADC
  - Input Stage Dynamics
  - Applications for the SAR Converter
- The High-speed Pipeline Topology
  - Driving the Capacitive Input Stage
  - Applications for the Pipeline Converter
- Conclusion

Delta-Sigma A/D Converters

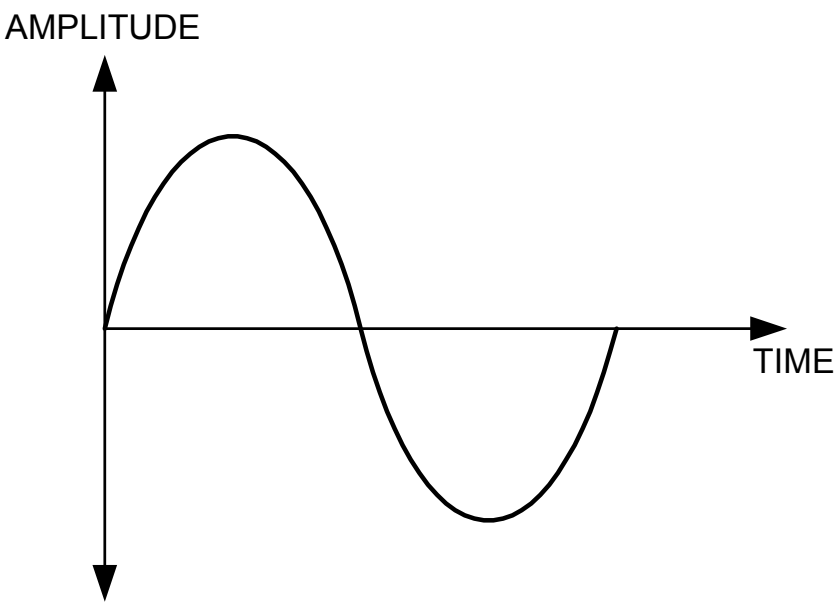


Input to the Delta-Sigma A/D

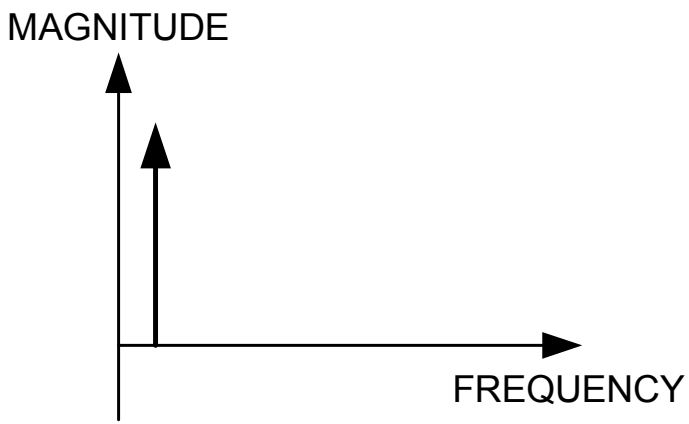


Input Signal

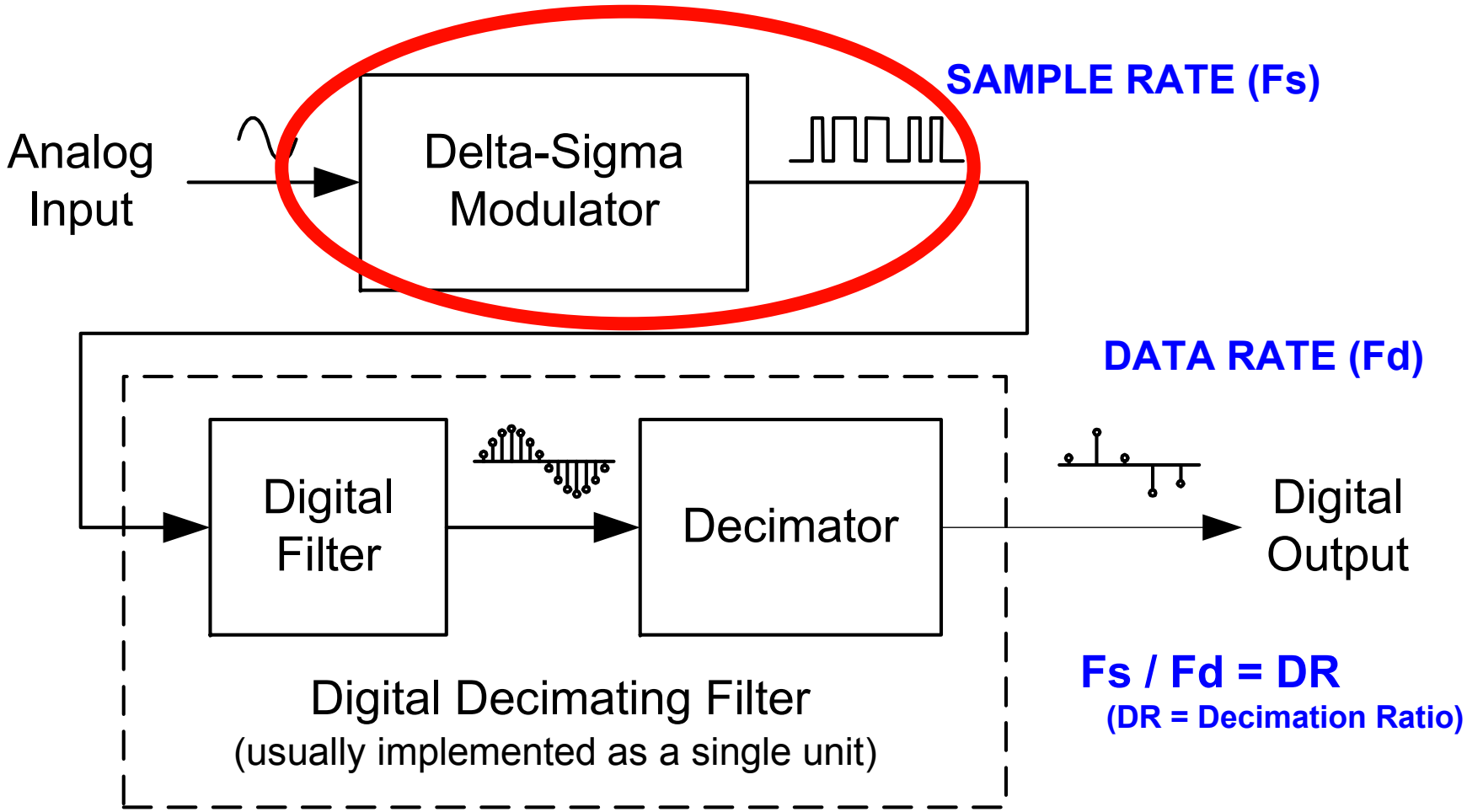
Input Signal:
TIME DOMAIN



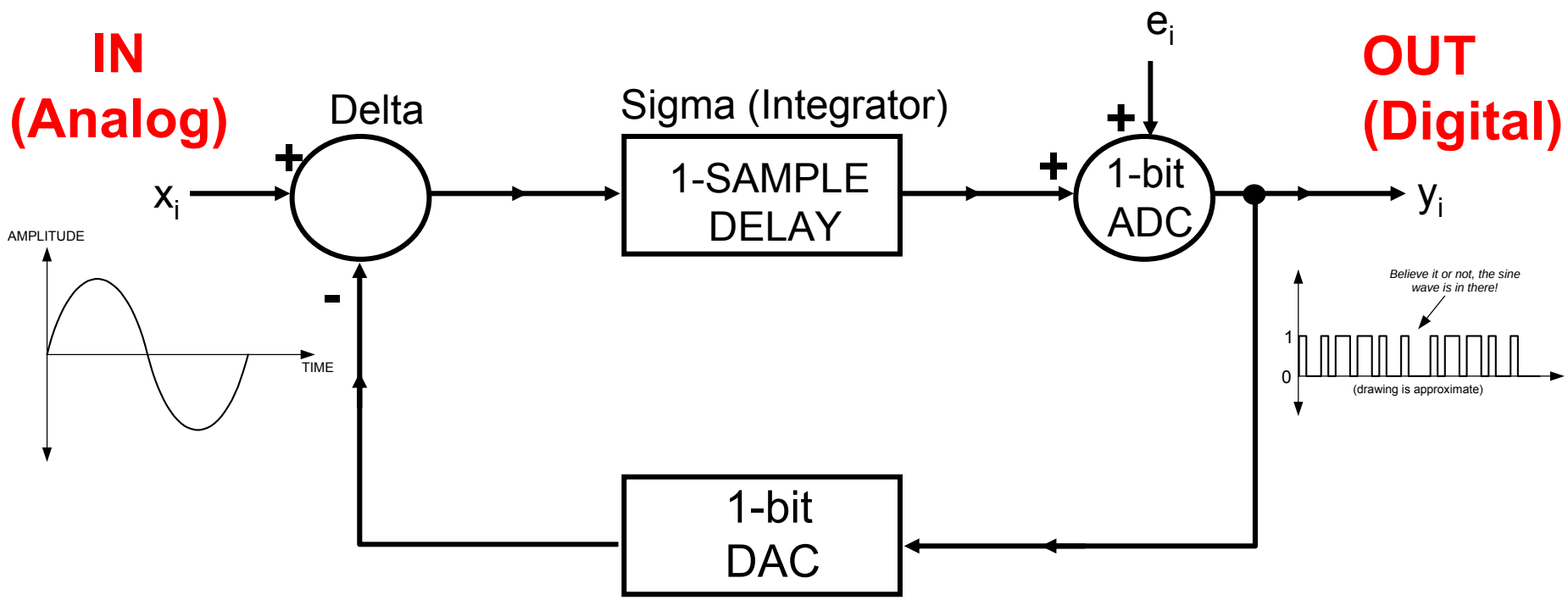
Input Signal:
FREQUENCY DOMAIN



Modulator Output

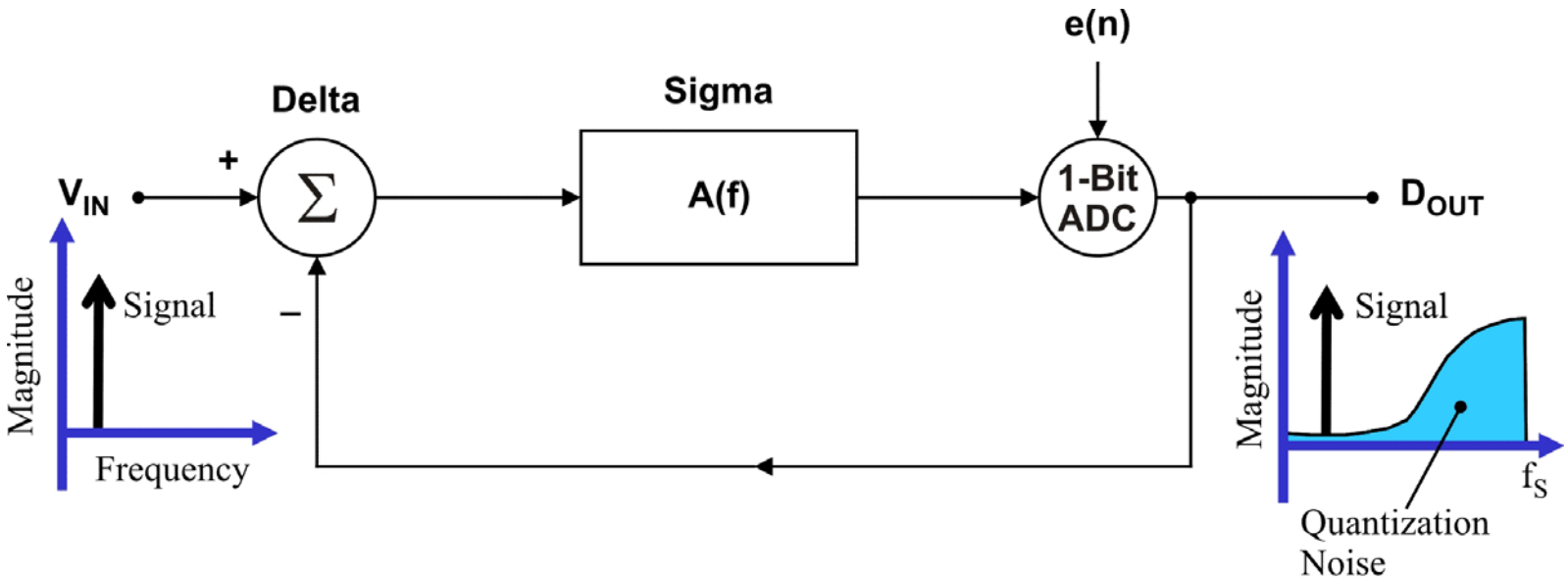


1st Order Delta-Sigma Modulator TIME DOMAIN



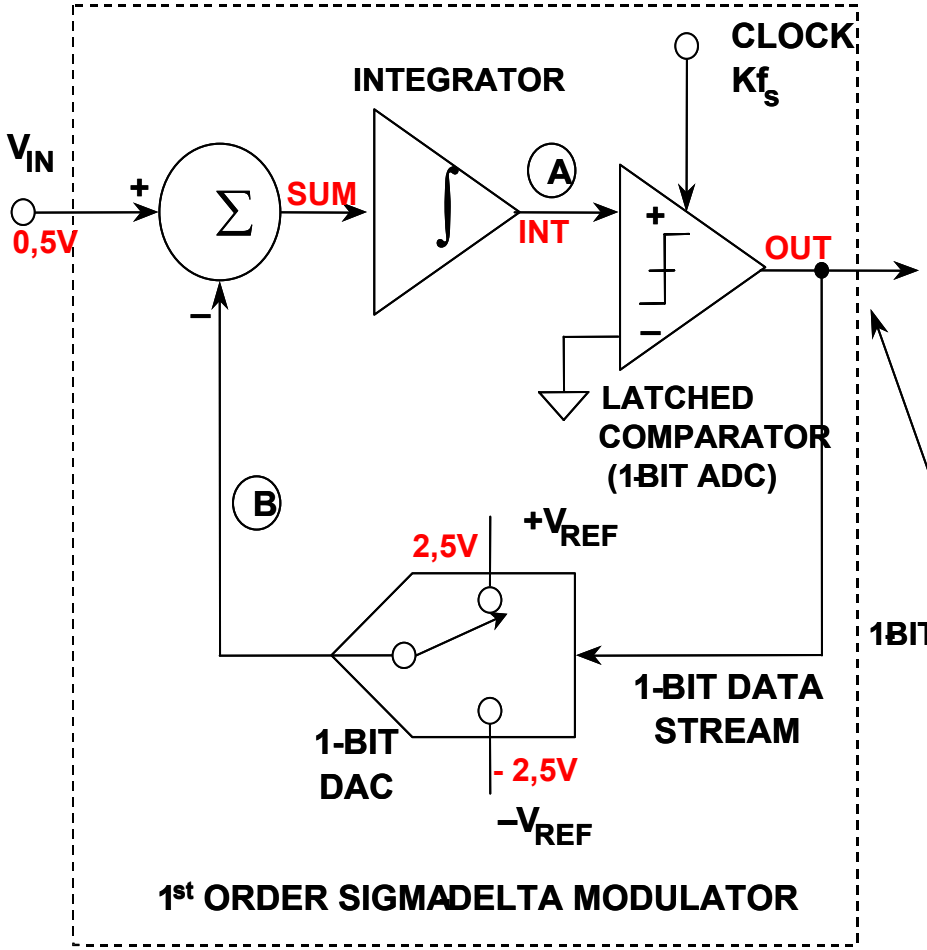
$$y_i = x_{i-1} + (e_i - e_{i-1})$$

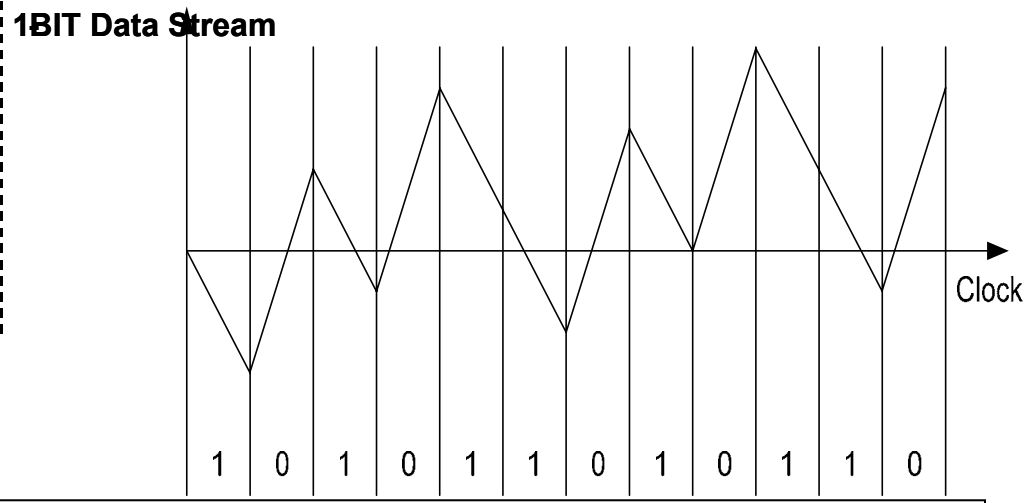
1st Order Delta-Sigma Modulator FREQUENCY DOMAIN



$$D_{OUT}(f) = \underbrace{\left(\frac{e(n)}{1+A(f)}\right)}_{\text{Noise Transfer Function}} + \underbrace{\left(\frac{V_{IN}(f)A(f)}{1+A(f)}\right)}_{\text{Signal Transfer Function}}$$

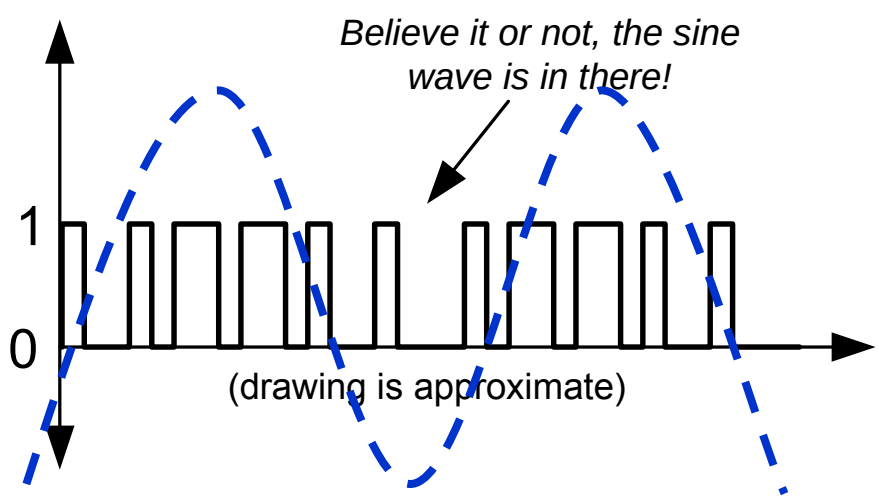
The Delta-Sigma Modulator



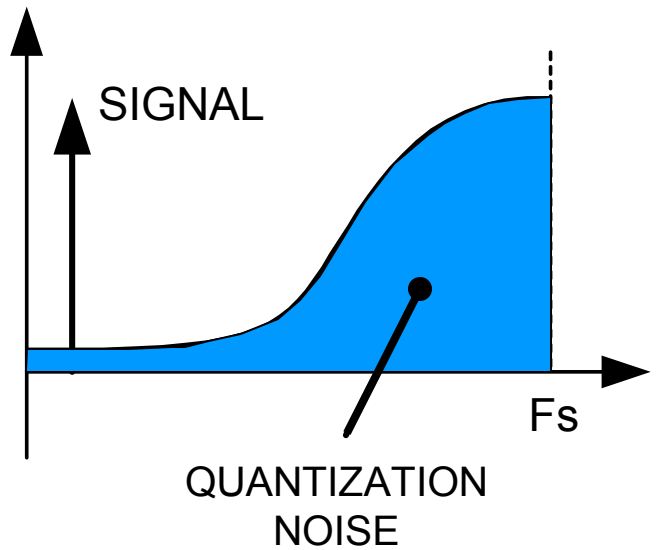


Modulator Output Signal

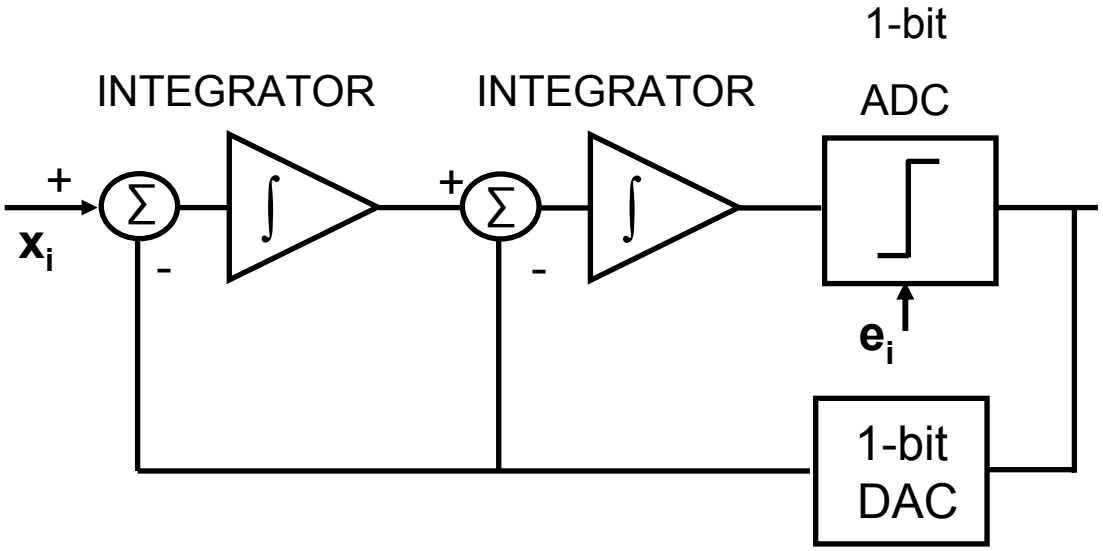
Modulator Output:
TIME DOMAIN



Modulator Output:
FREQUENCY DOMAIN

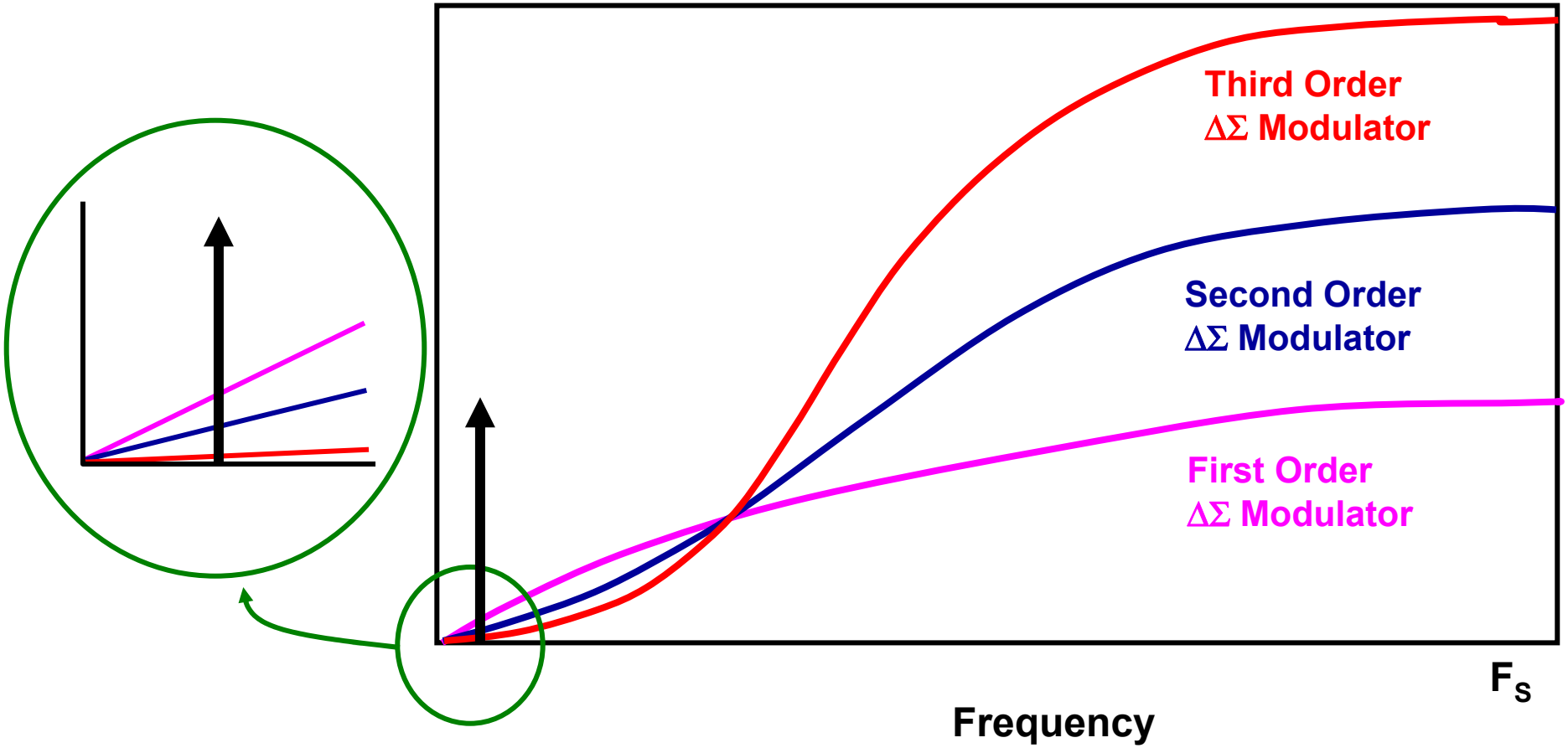


2nd order Delta-Sigma Modulator

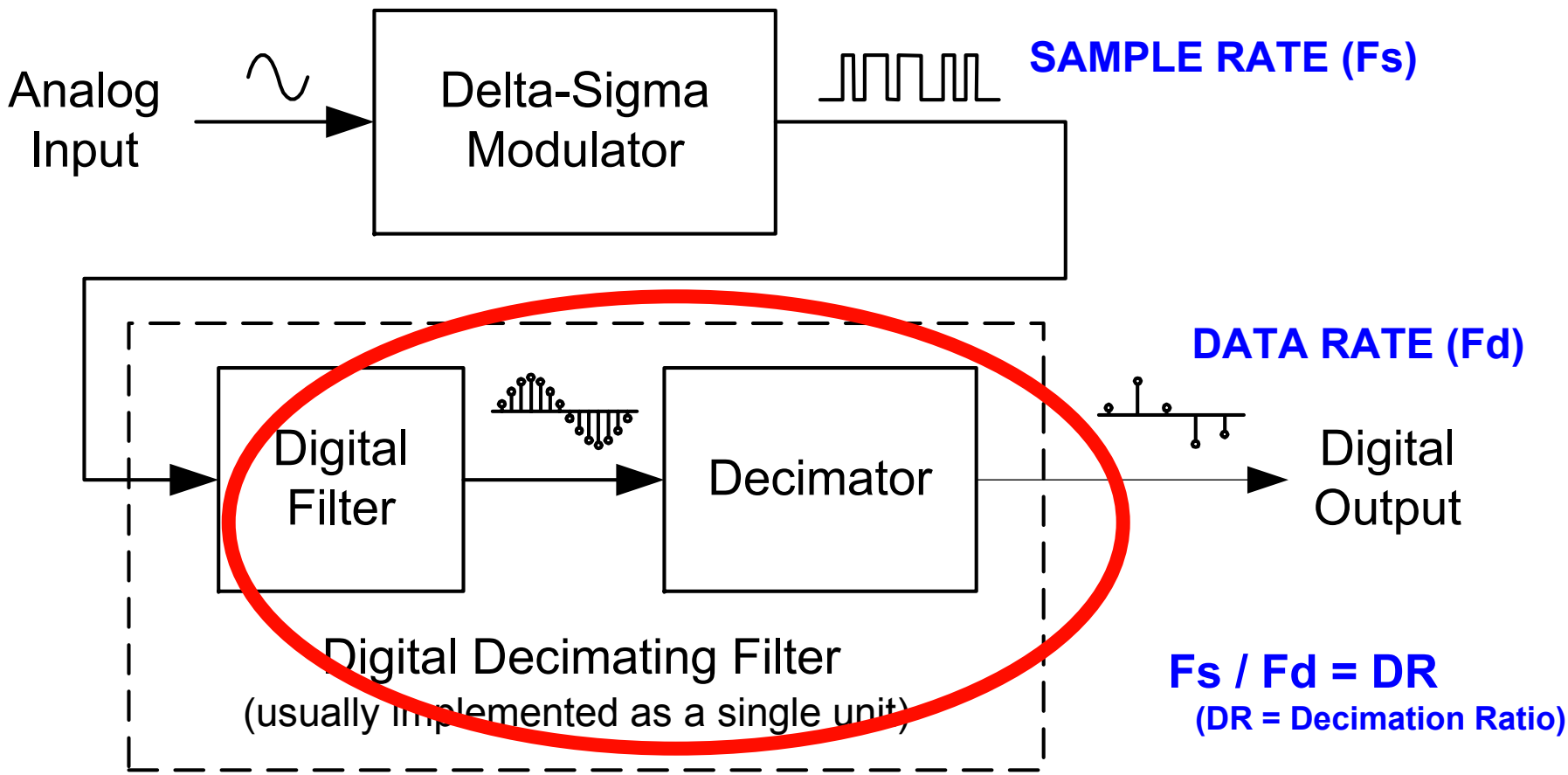


$$y_i = x_{i-1} + \left(e_i - 2 \cdot e_{i-1} + e_{i-2}\right)$$

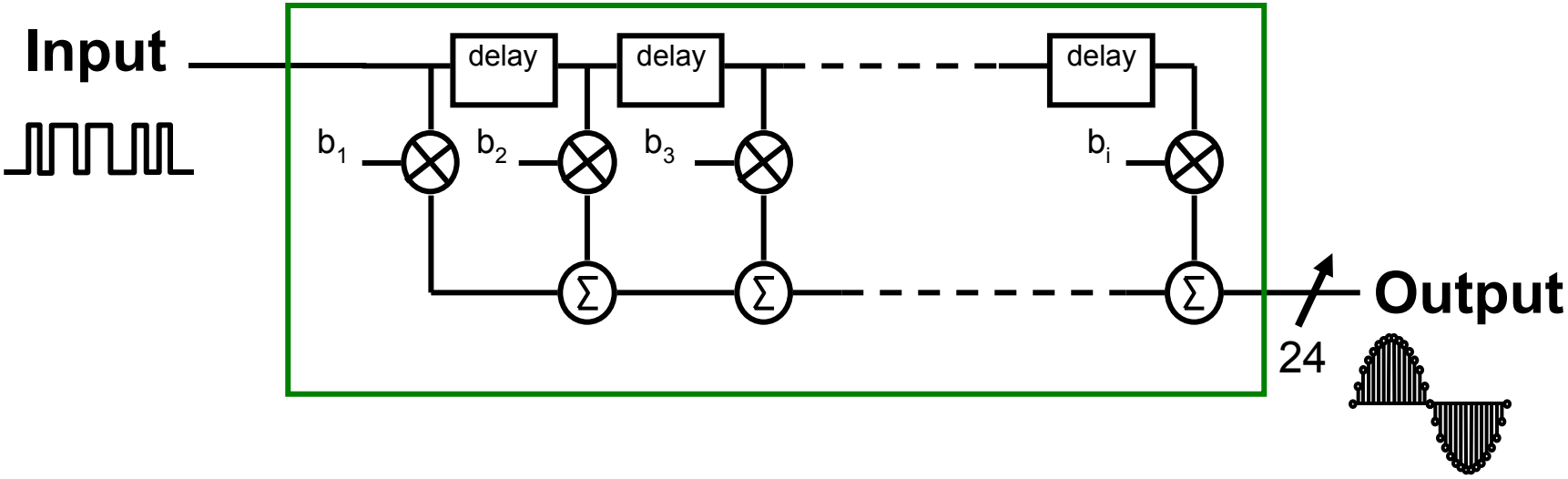
Multi-order Delta-Sigma Modulators



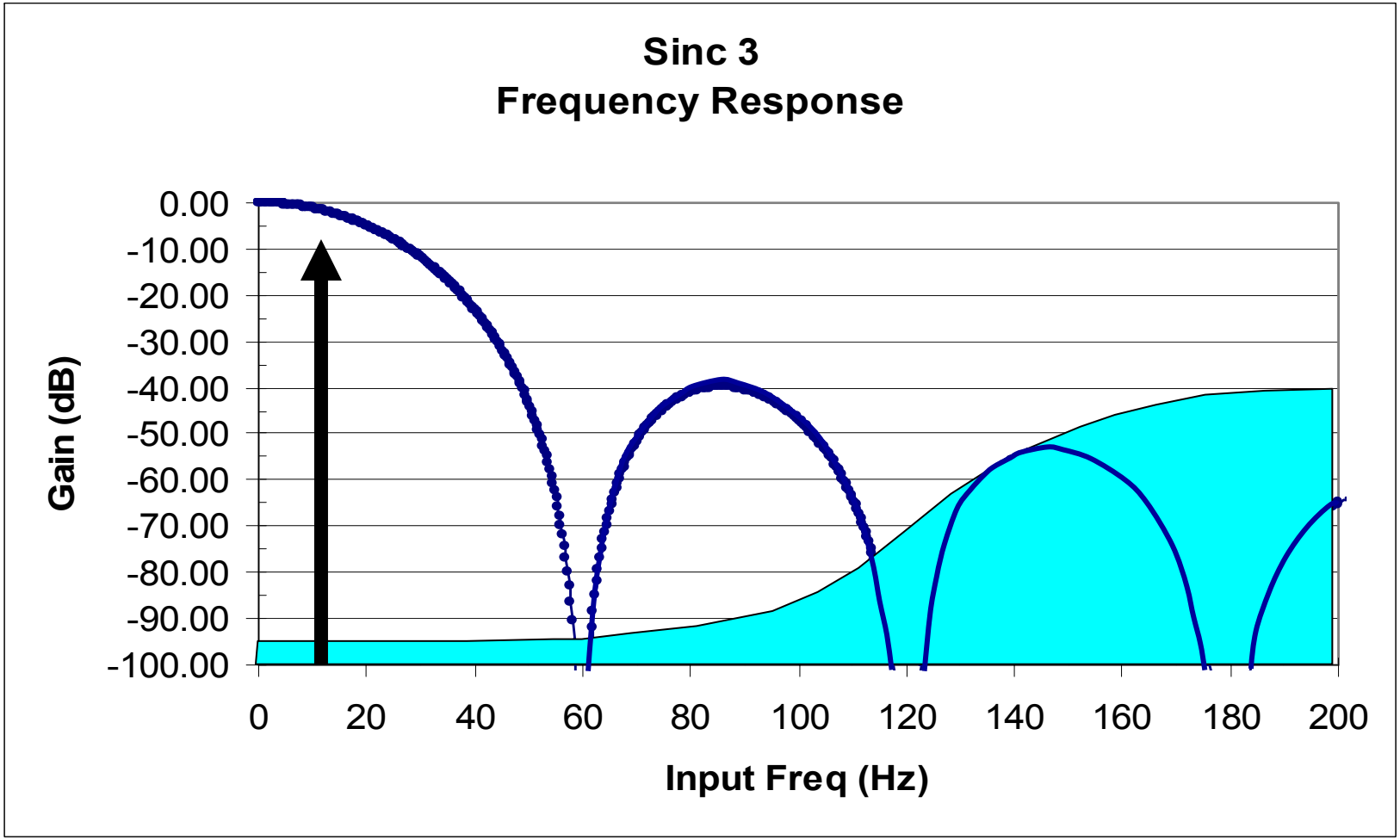
Delta-Sigma A/D Signal Path



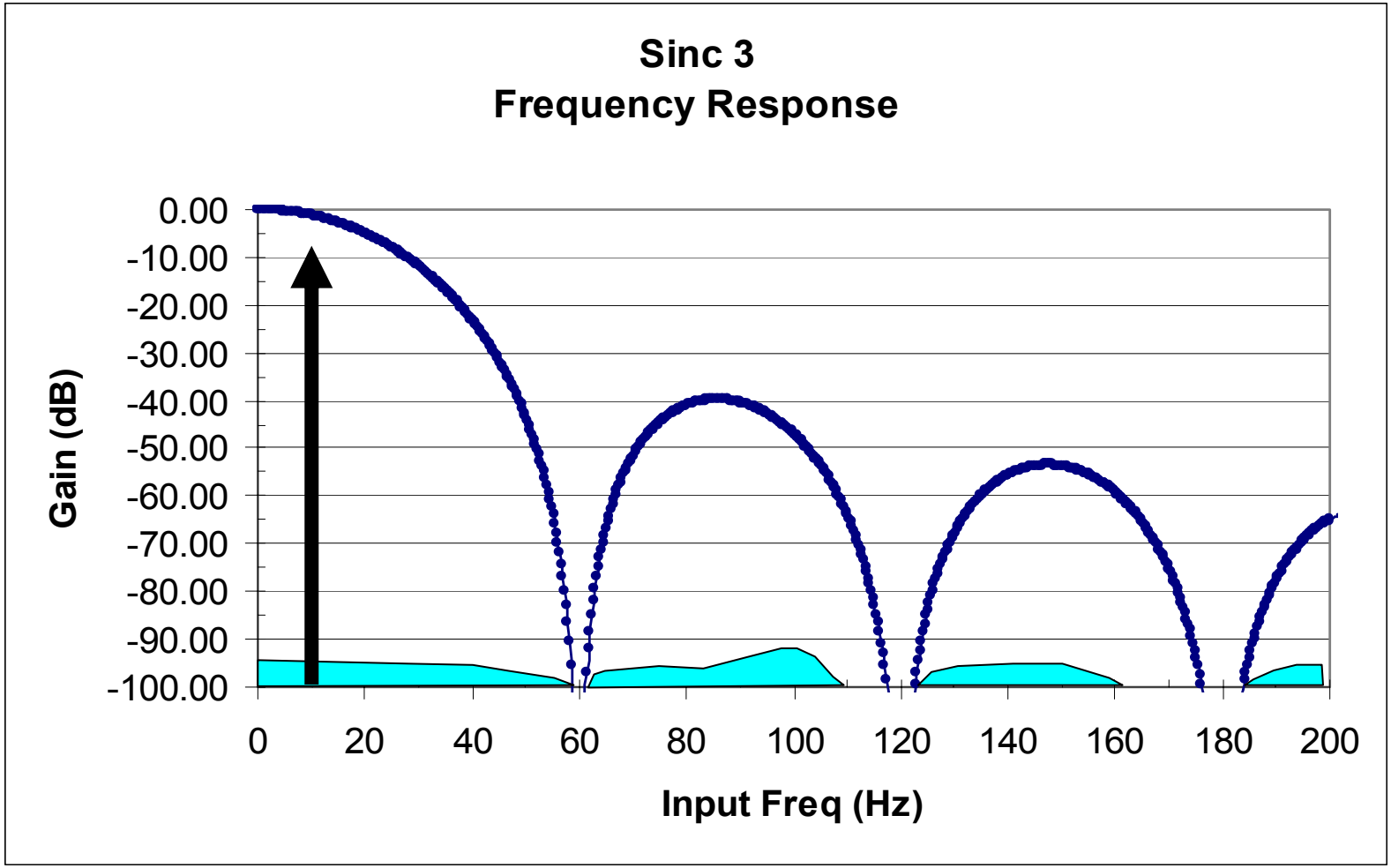
Digital Filter Function



High Frequency Noise Reduction

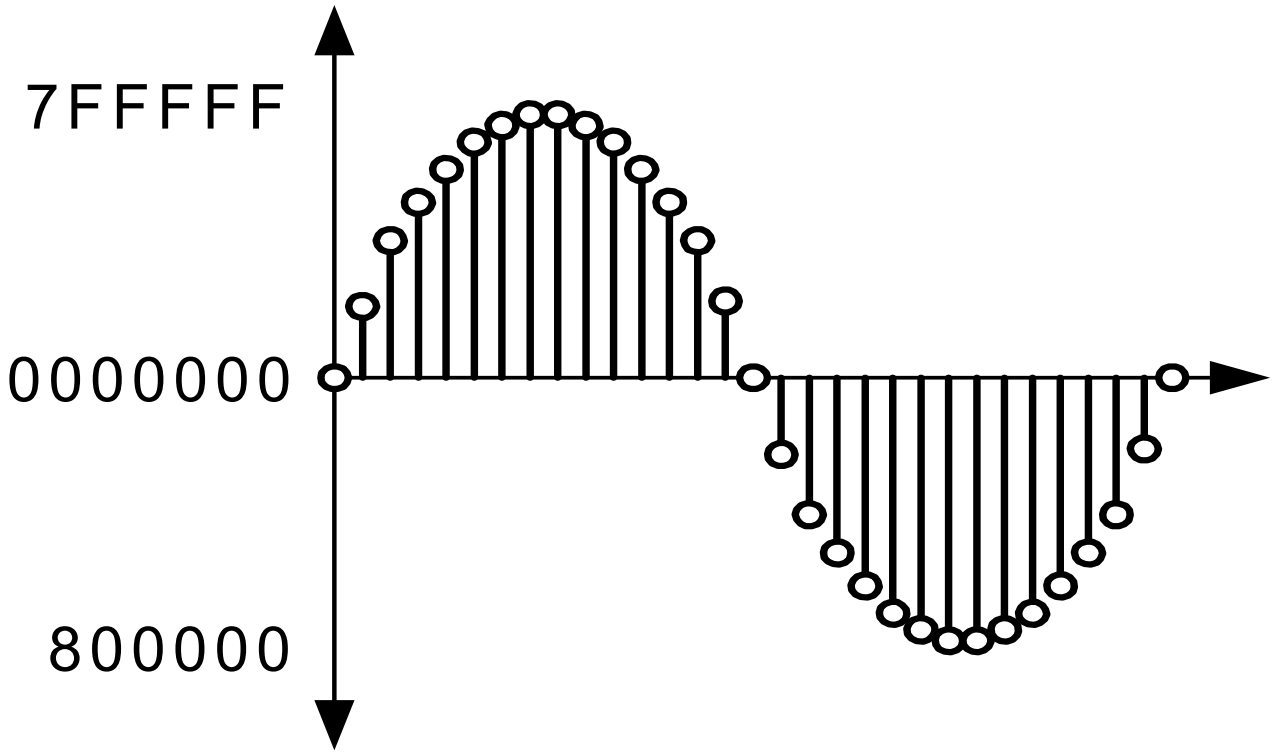


High Frequency Noise Reduction

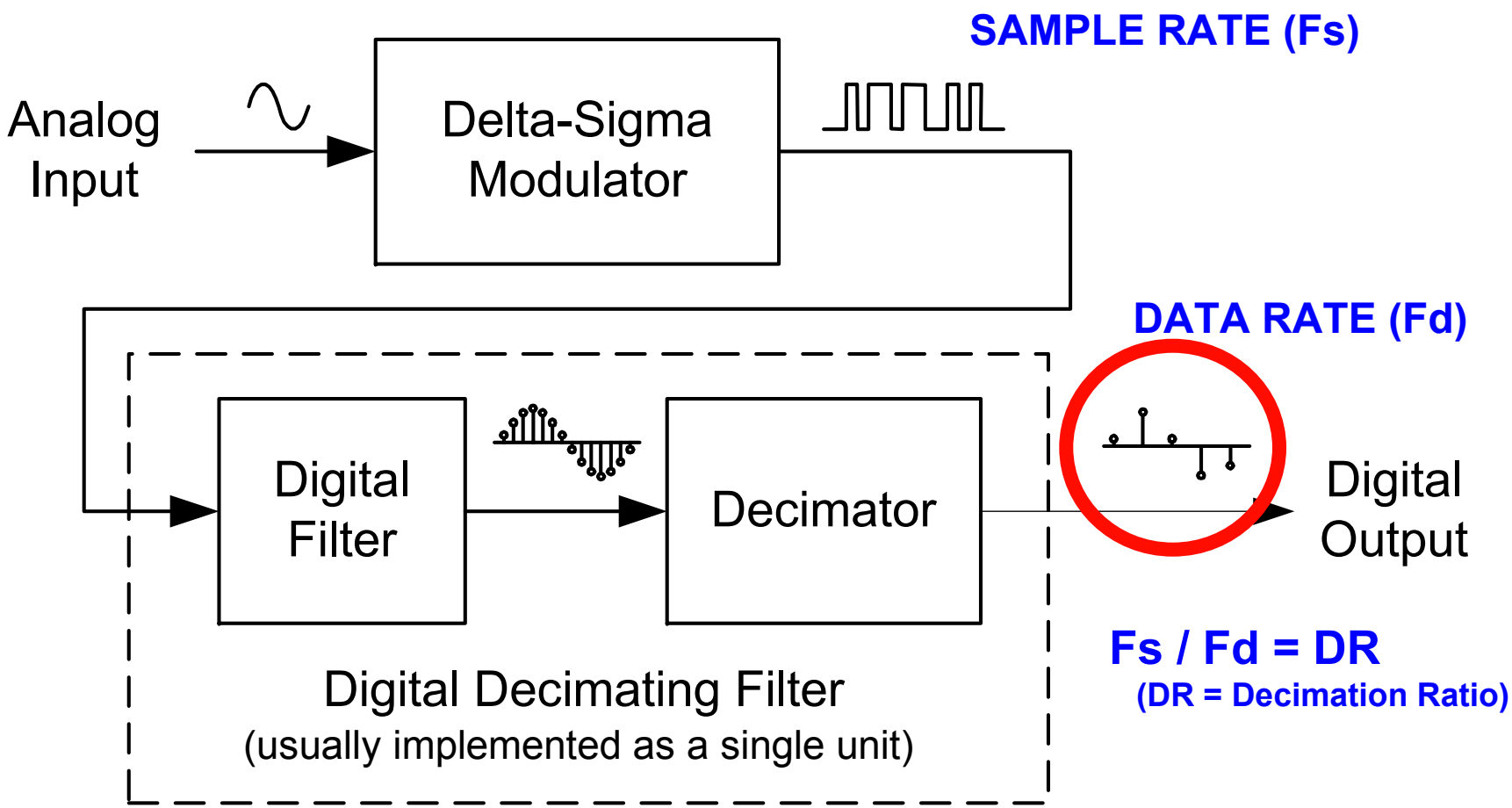


Outcome of Digital Filter Function

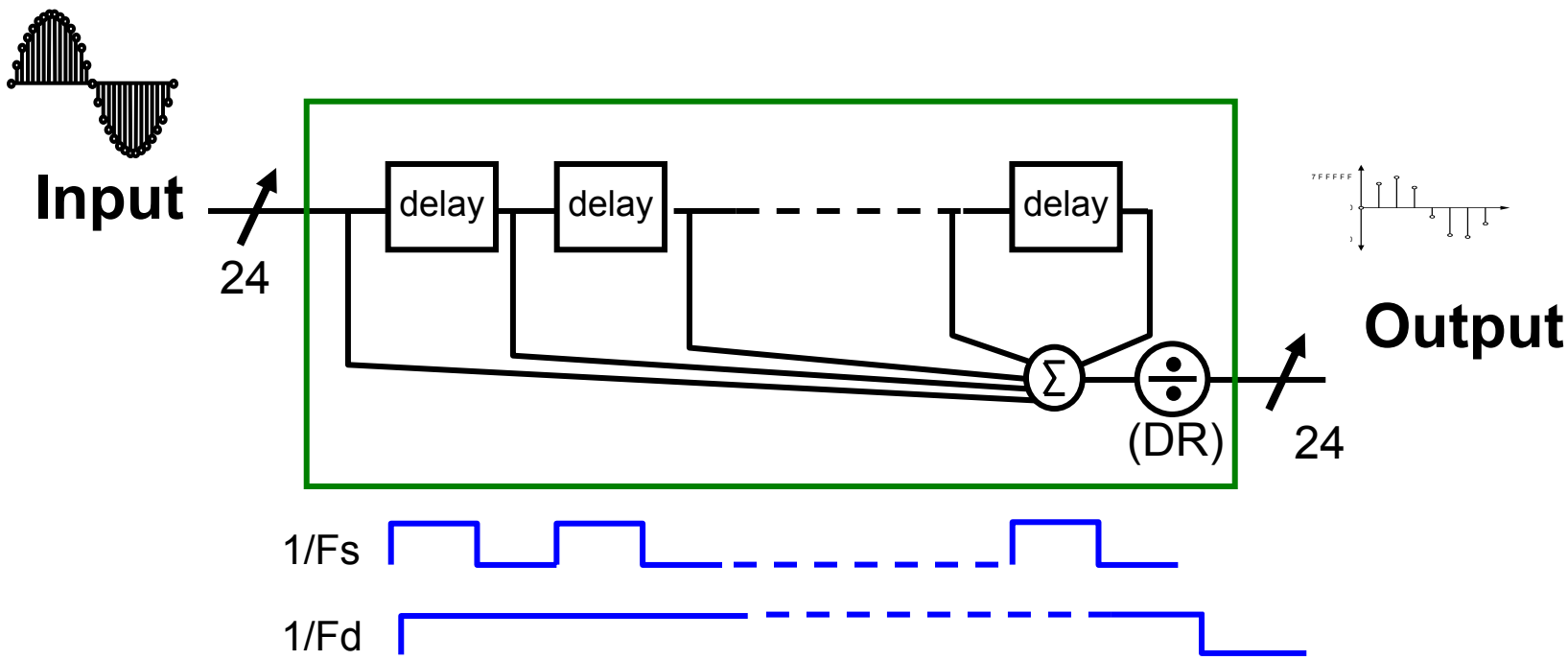
TIME DOMAIN



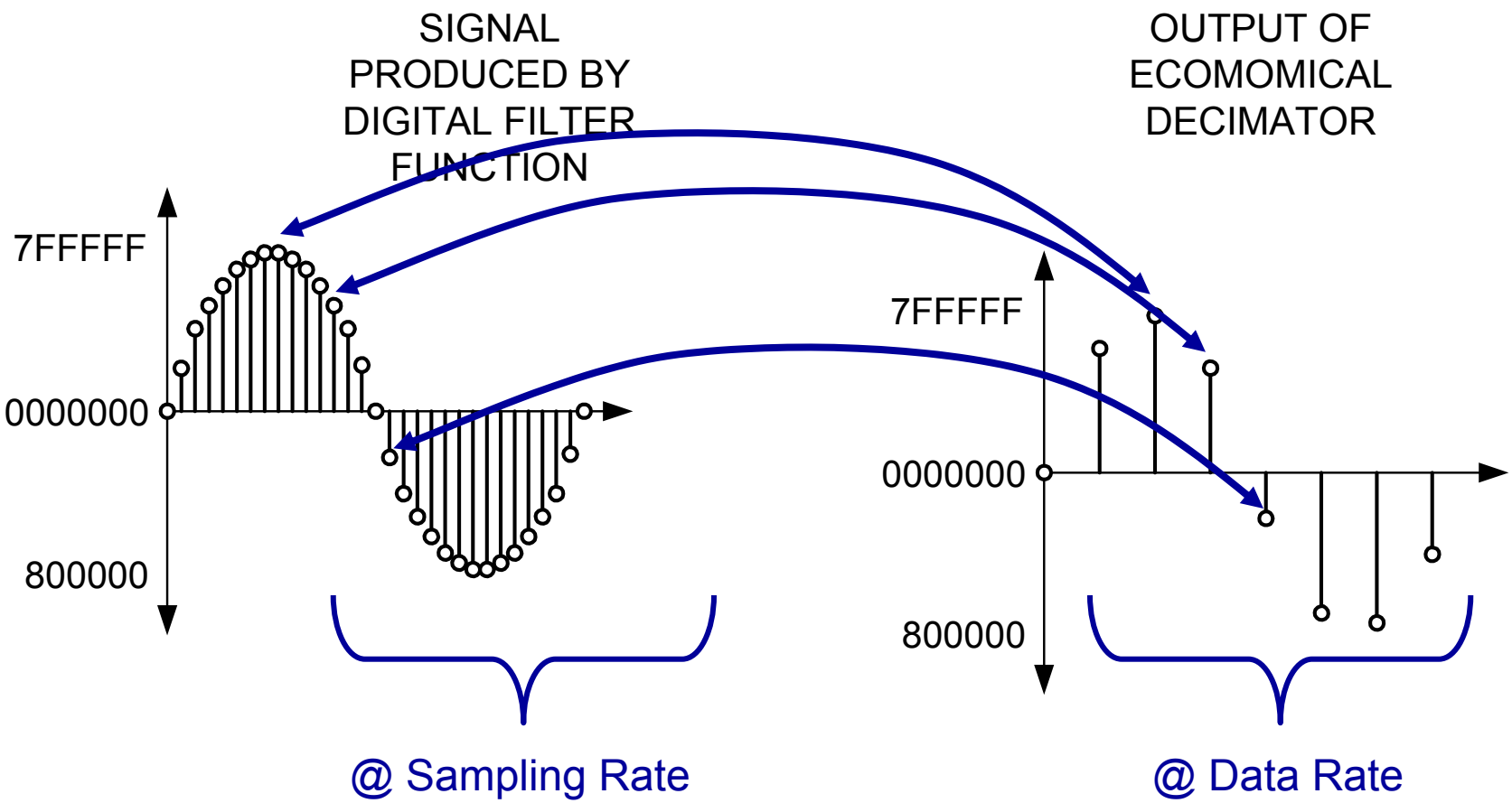
Decimation Digital Filter



Decimator Function: Averager

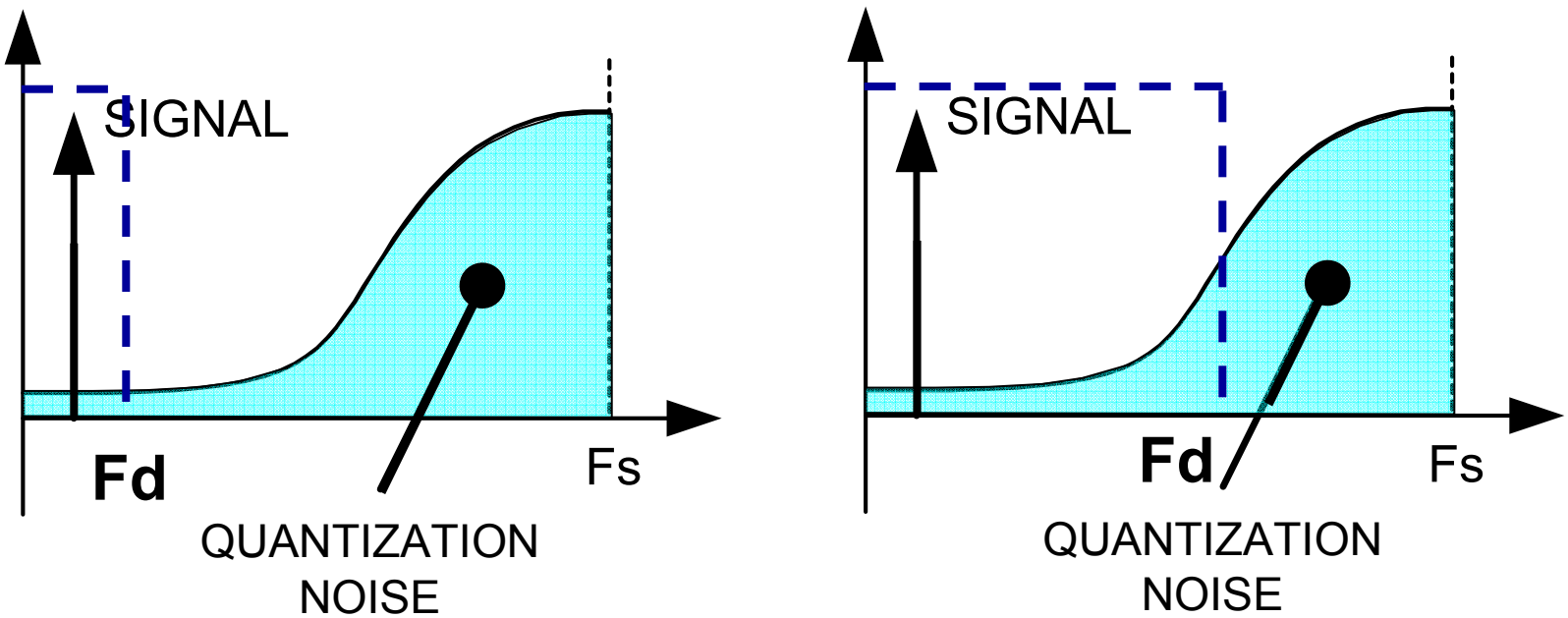


Decimator Function: Pick & Dump



Sampling speed vs. ENOB

Fs / Fd = DR = K



$DR_A > DR_B$

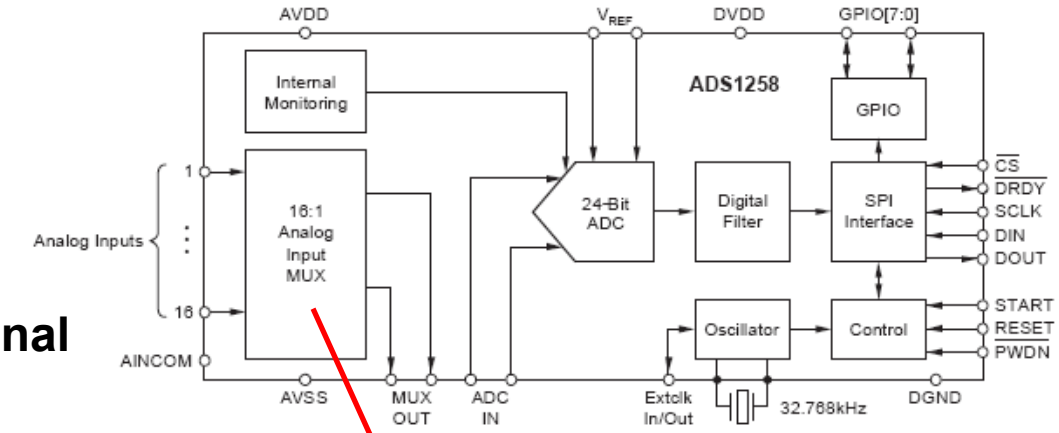
A.

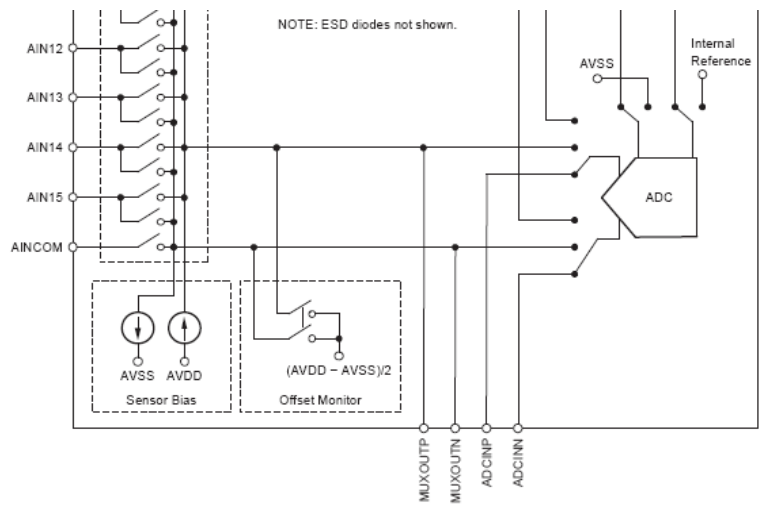
B.

Additional Features

ΔΣ-Converter often have additional features for data acquisition

- **PGA**
- **Input Buffer**
- **Burnout Current Sources**
- **Multiplexers**
- **GPIO**
- **More complete system solution**





Applications for ΔΣ Converters

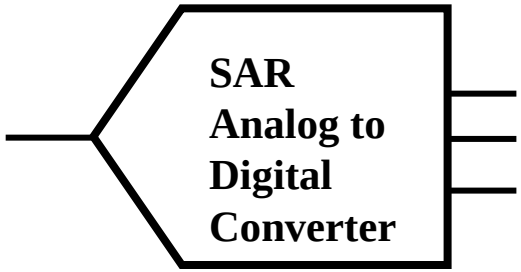
- **Signal Level**
  - High DC accuracy
  - High Resolution – up to 24 bits
  - High Integration level
    - Medical, Avionics, and Process Control
    - Machine and System Monitoring
    - Fast Scan Multi-Channel Instrumentation
    - Industrial Systems and Sensors
    - Test and Measurement Systems
- **Audio**
  - Optimized noise performance
  - Optimized filter in audio frequency for flatness
- **High Speed**
    - Scientific Instruments
    - Test Equipment
    - Communications

Agenda

- What are the Signal Frequencies
  - Analog Classes of applications
  - Frequency ranges of ADCs
- Nuts and Bolts of Delta-Sigma Converters
  - $\Delta\Sigma$ Converter Core and Auxiliary $\Delta\Sigma$ Functions
  - Applications for the $\Delta\Sigma$ Converter
- The SAR ADC
  - Input Stage Dynamics
  - Applications for the SAR Converter
- The High-speed Pipeline Topology
  - Driving the Capacitive Input Stage
  - Applications for the Pipeline Converter
- Conclusion

The SAR ADC

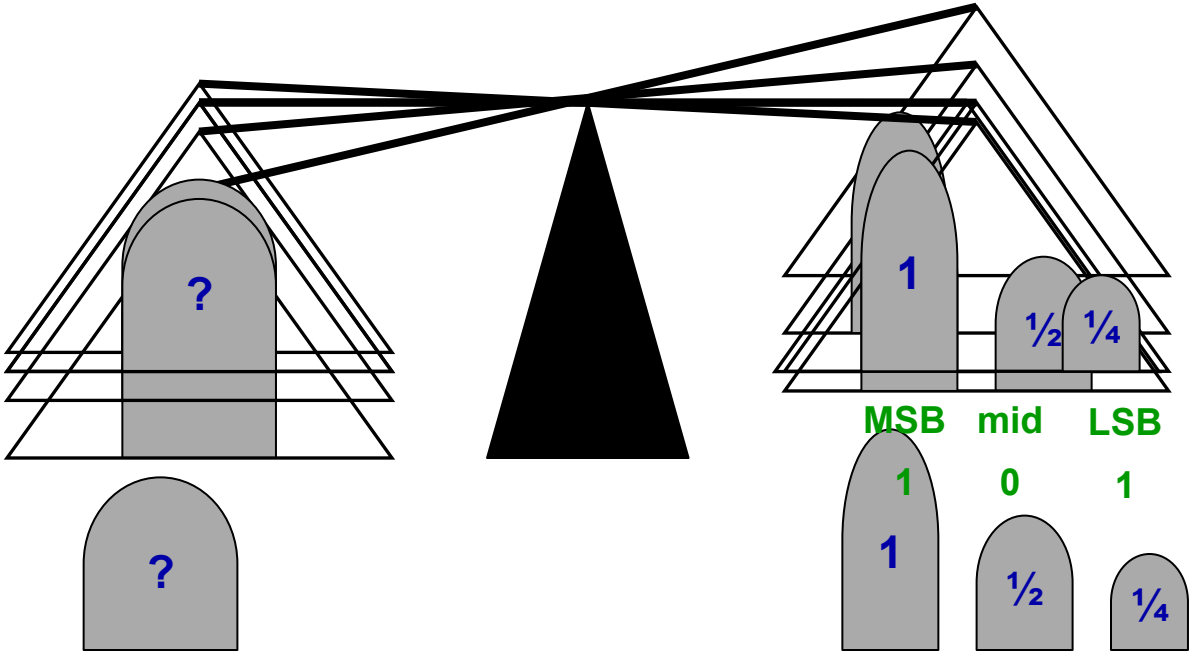
- Most Serial ADCs are SARs or Delta-Sigmas
- SARs are Best for General Purpose Apps
  - Data Loggers,
  - Temp Sensors,
  - Bridge Sensors,
  - General Purpose
- In the Market SARs
  - Can be 8 to 18 bits of resolution
  - Speed range: > DC to < 5 Msps
- SARs found as
  - Stand-alone
  - Peripheral in Microcontrollers, Processors



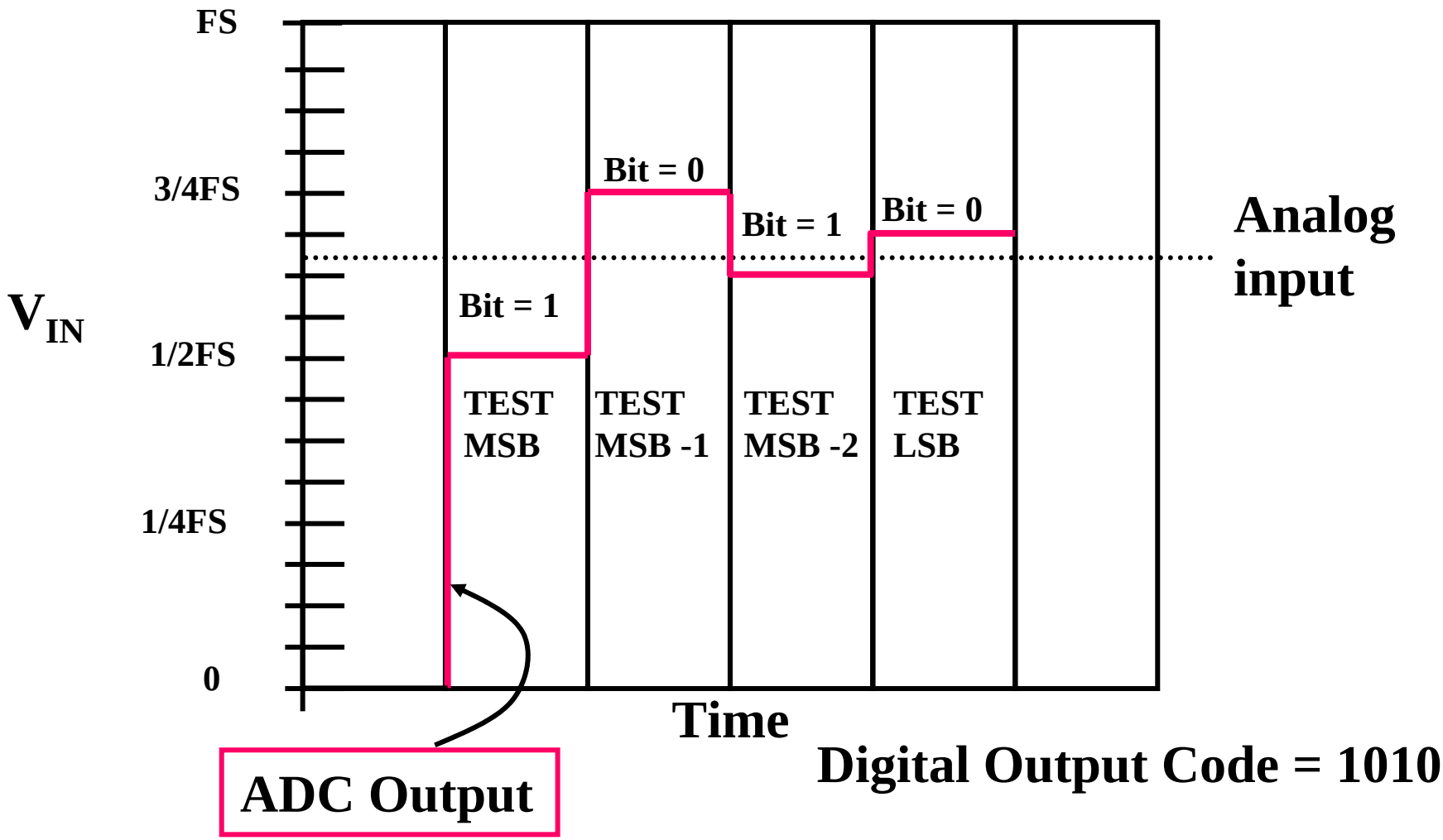
How Does a SAR work?

- Similar to a balance scale

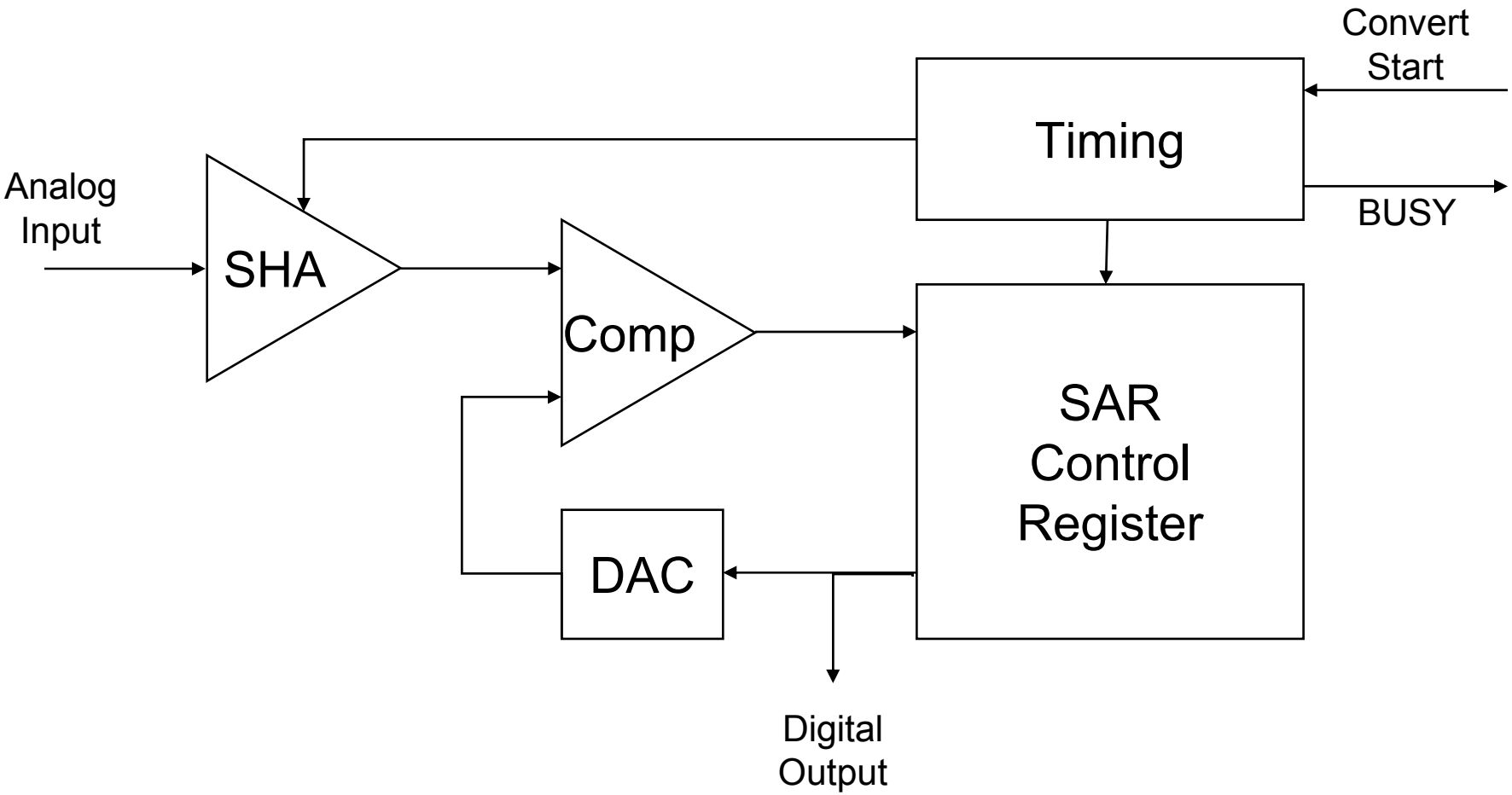
the MSB is determined first



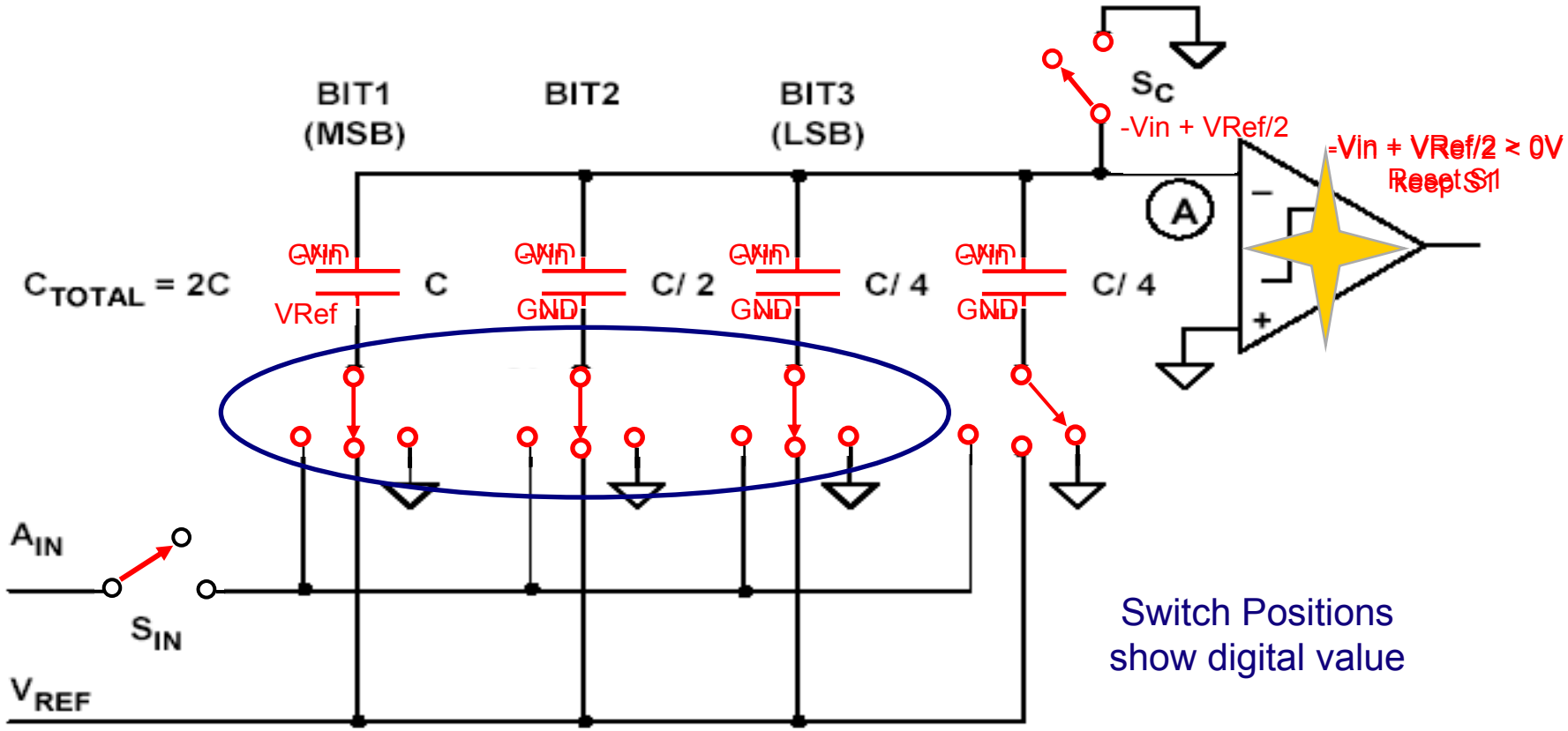
SAR Conversion Concept



Blockdiagram Successive Approximation ADC

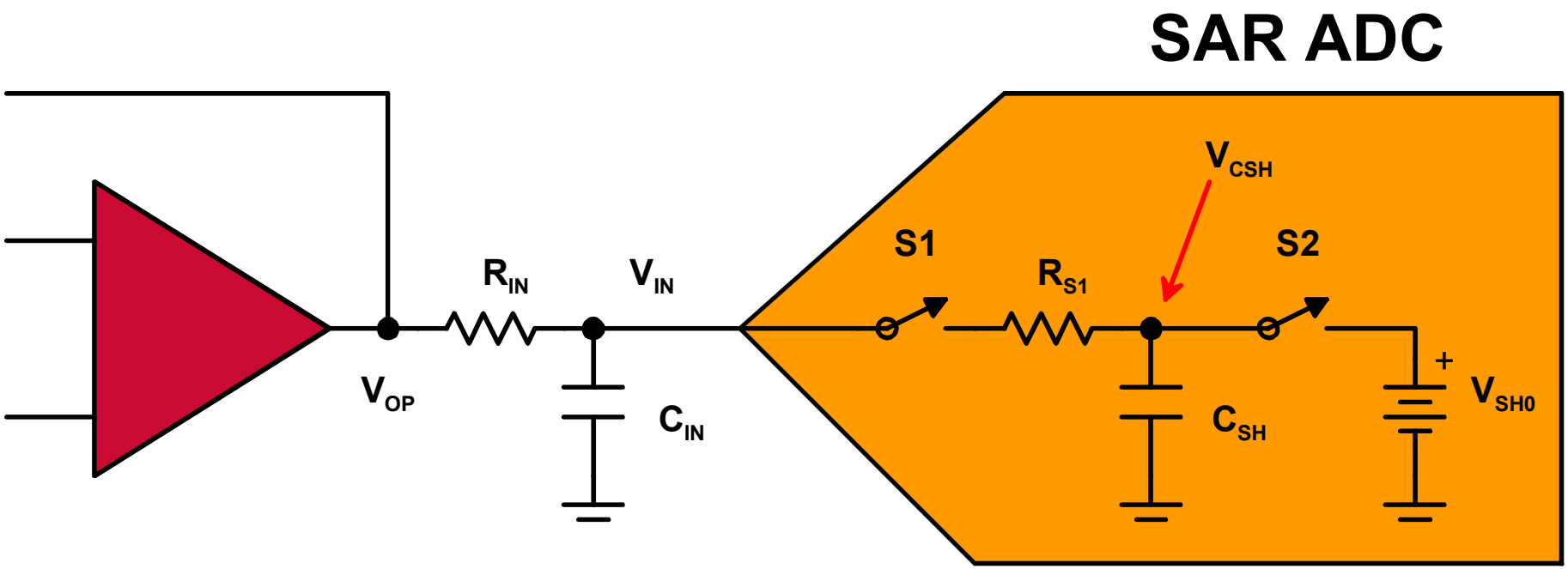


3-Bit SAR ADC with switched Capacitor DAC

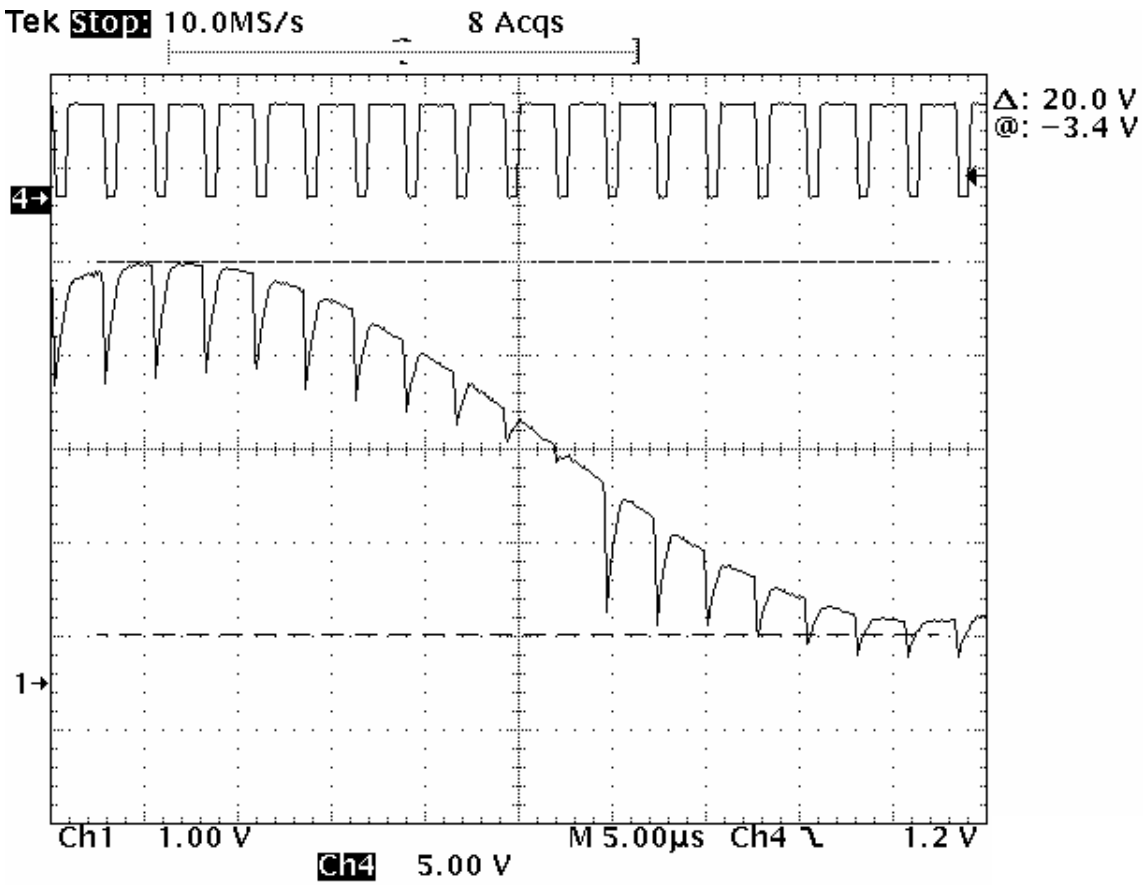


SWITCHES SHOWN IN TRACK (SAMPLE) MODE

SAR Converter – Input Stage

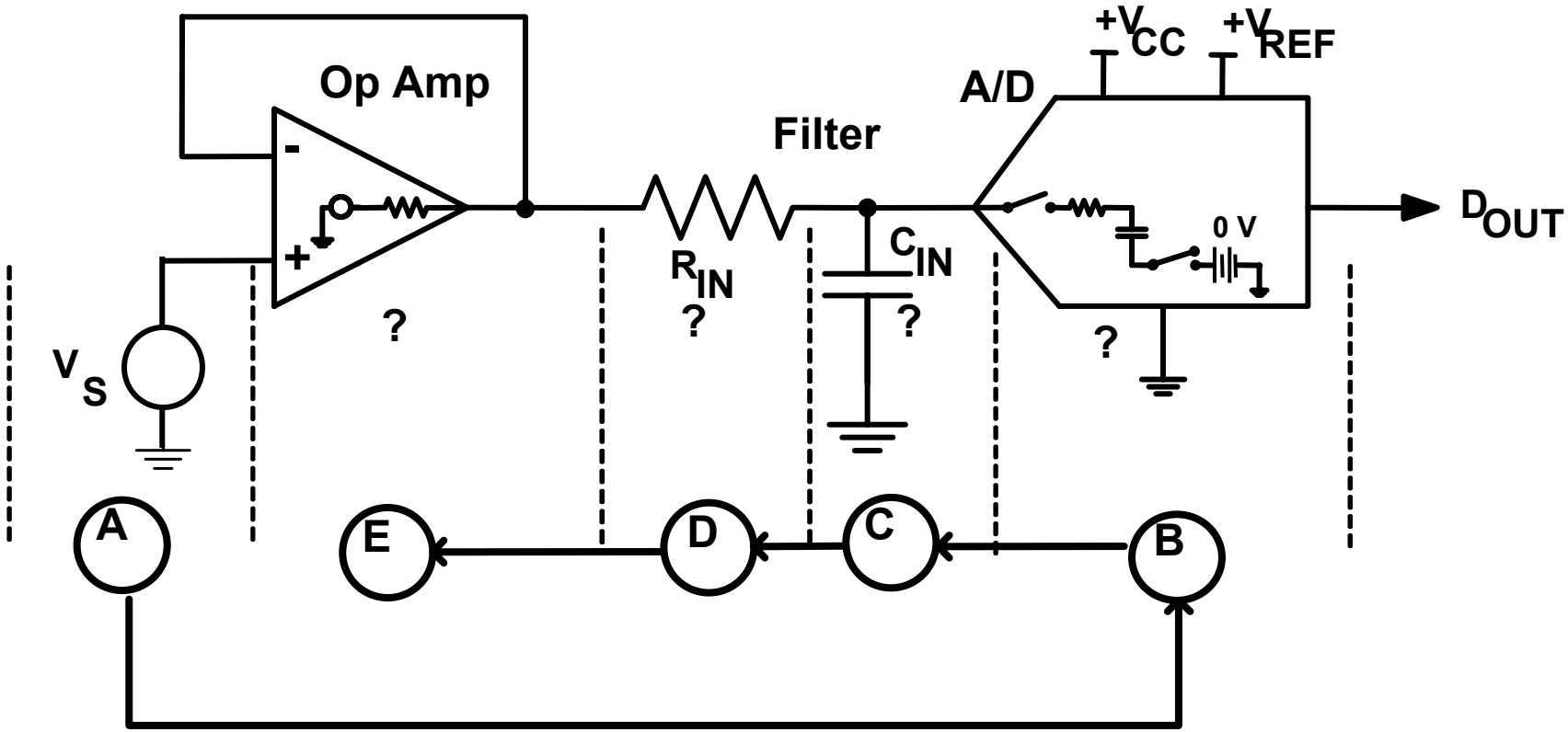


SAR ADC Input Charge Distribution



- **Op amp requirements**
  - **Must charge the ADC cap quickly & accurately**

Design Procedure



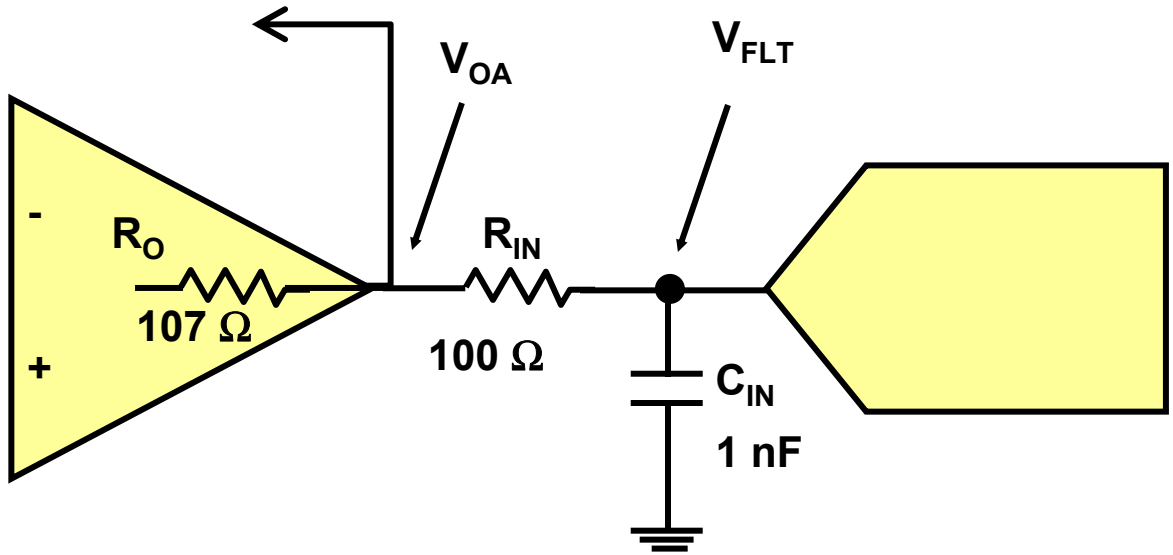
Signal (1)
- Bandwidth
- Full-scale Range

Op amp (5)
- Input Stage
- Bandwidth
- Output R_O
- Settling Time

RC pair (3,4)
- ADC vs cap
- Cap quality
- Opa vs Resistor

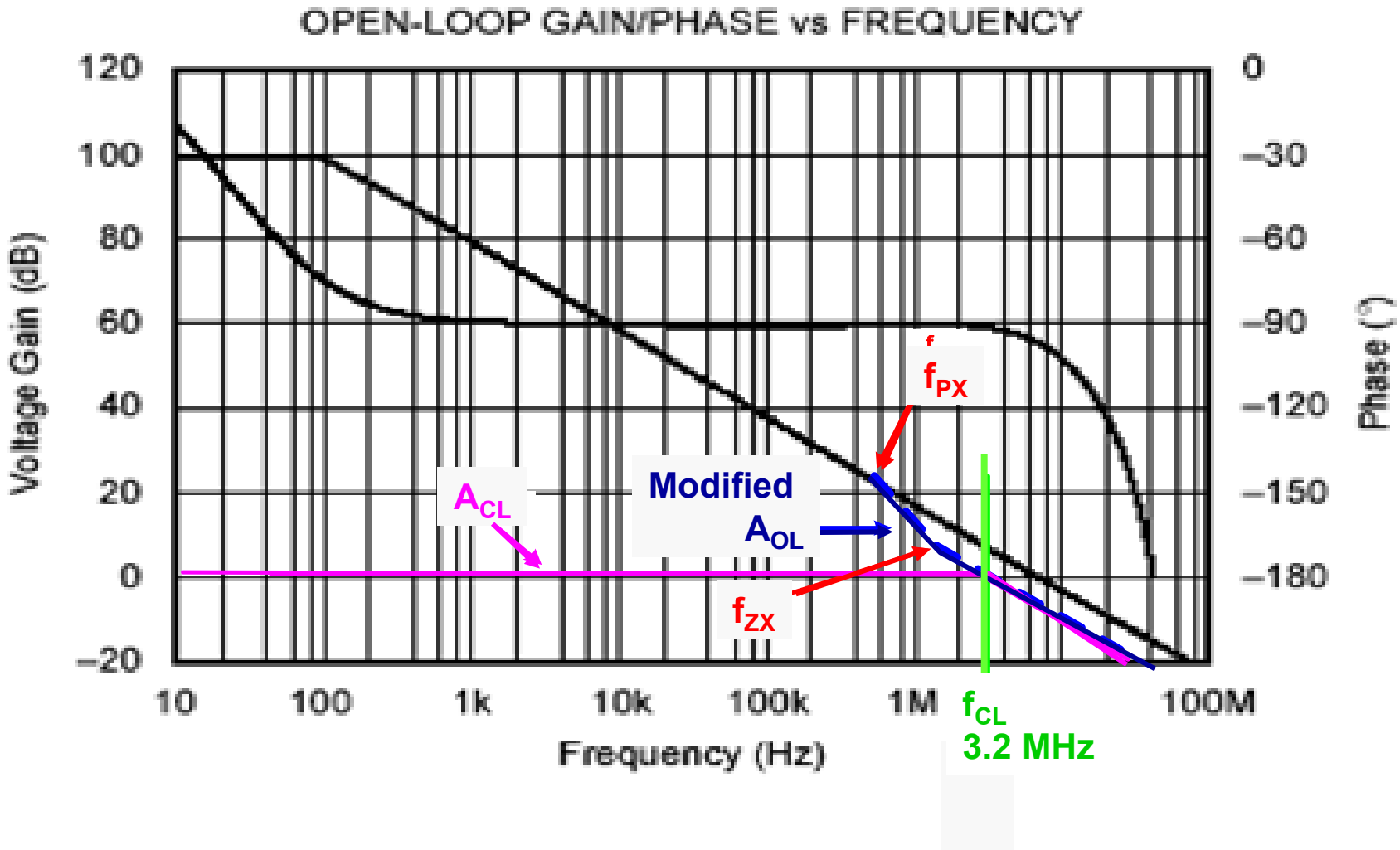
ADC (2)
- Full-scale input range
- Acquisition time
- Kick Back Voltage & Charge

OpAmp + Filter: Small Signal

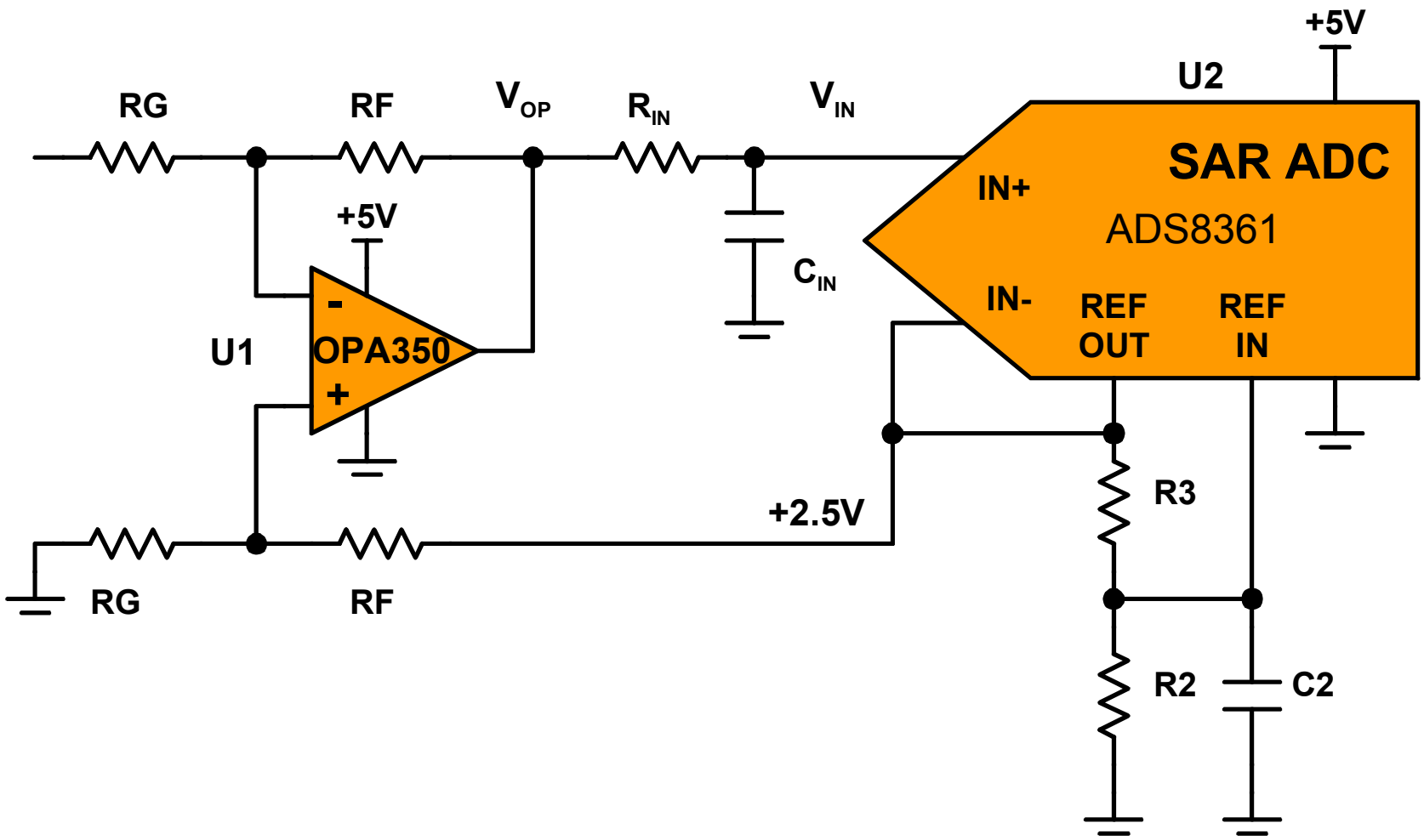


- **Modify AoI due to R_{IN} & C_{IN}**
  - $f_{PX} = 1/[2\pi(R_O + R_{IN})C_{IN}]$
    - $f_{PX} = 1/[2\pi(107\Omega + 100\Omega)1\text{ nF}] = 768\text{kHz}$
  - $f_{ZX} = 1/[2\pi R_{IN}C_{IN}]$
    - $f_{ZX} = 1/[2\pi \times 100\Omega \times 1\text{ nF}] = 1.6\text{MHz}$

OpAmp + Filter: Frequency Response



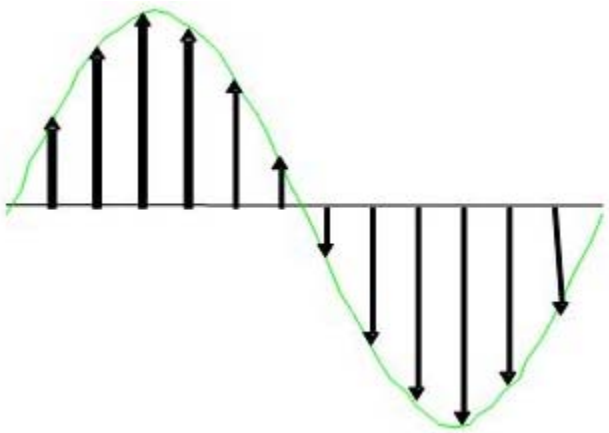
Driving SAR Converters

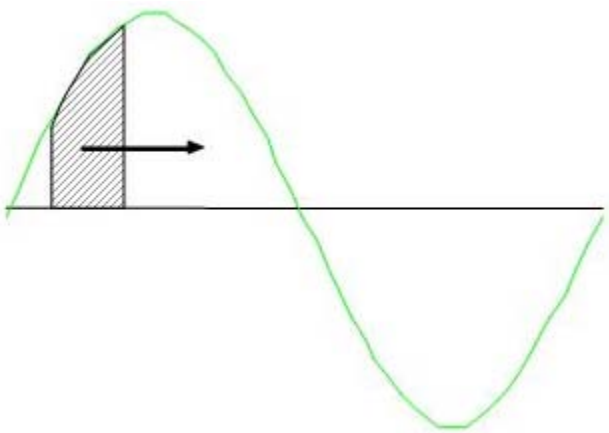


Additional Features

- Fewer options with SARs
  - Some converters have multiplexers (ADS82xx)
  - References (ADS78xx, ADS84xx)
  - Input Buffers/Drivers (ADS8254/55/84)
  - PGA (ADS7870/71)

Delta Sigma or SAR ?





SAR ADC takes „snaphots“

Each conversion command captures the signal level, at the point in time onto the sample&hold

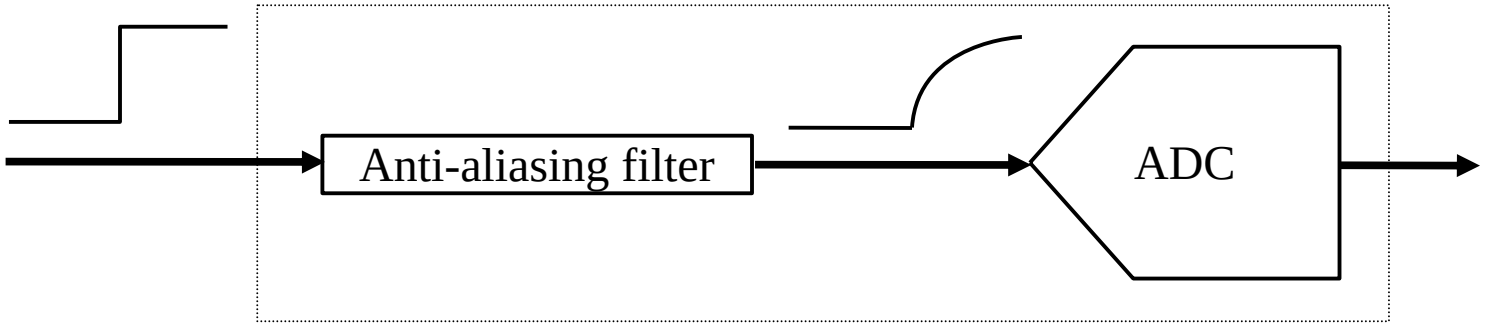
The conversion happen at defined points in time

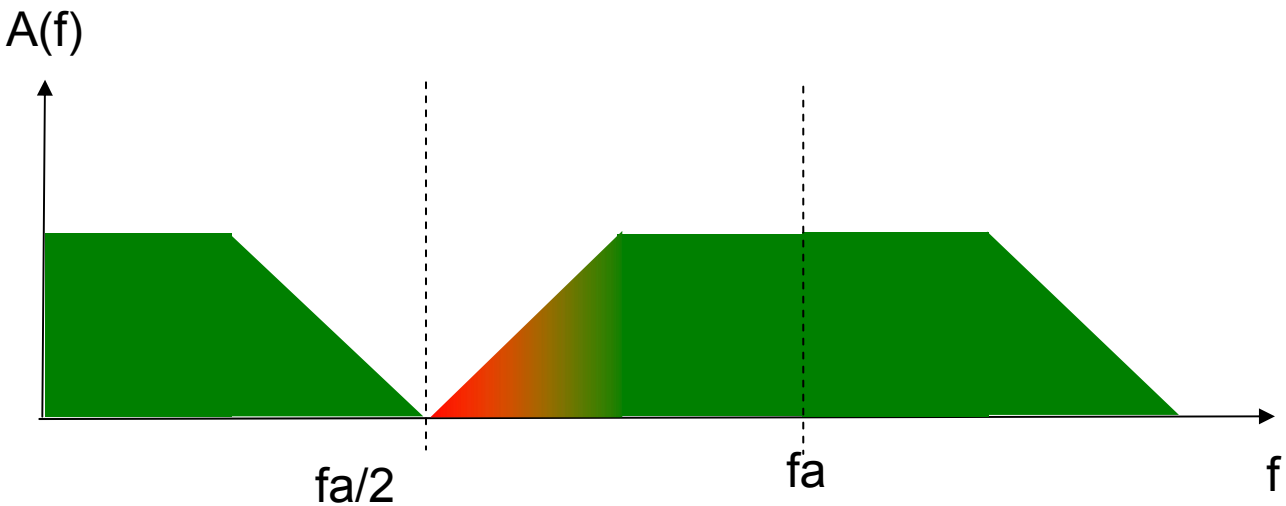
ΔΣ ADC takes an average

There is no defined conversion point and time

The more averages the higher the resolution

Delta Sigma or SAR ?

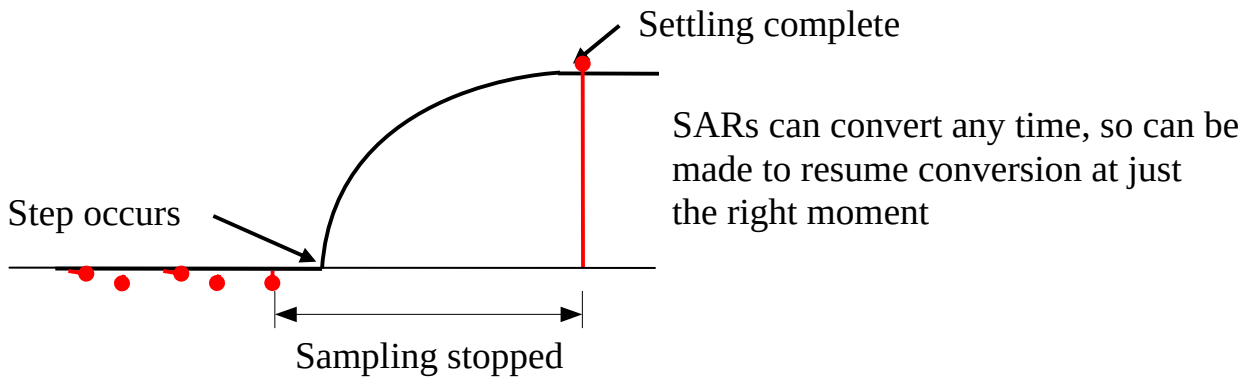


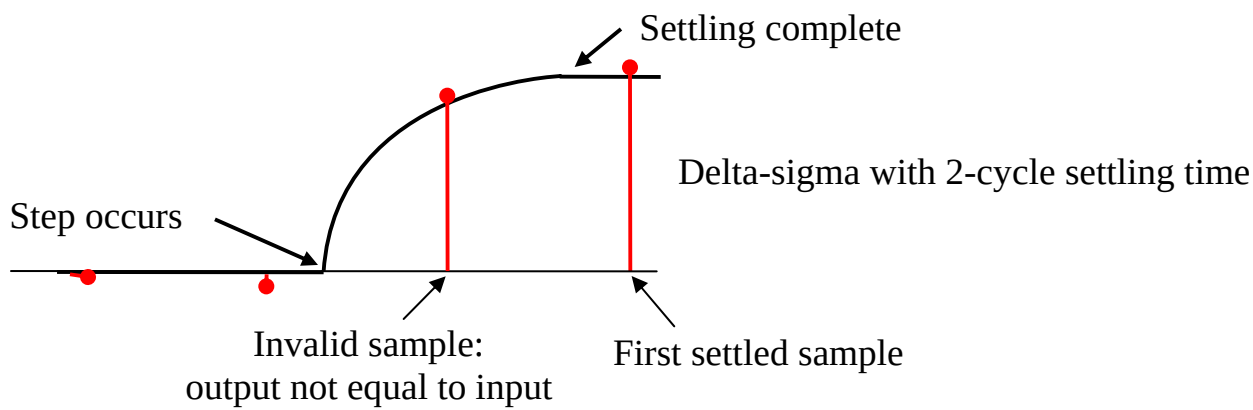


SAR ADC needs Anti Aliasing Filter 2th up to 8th order in continous sampling application

ΔΣ ADC Anti Aliasing relaxed Due to oversampling topology 2nd oder a simple 1st order R/C is sufficient.

Settling time: SAR vs. del-sig





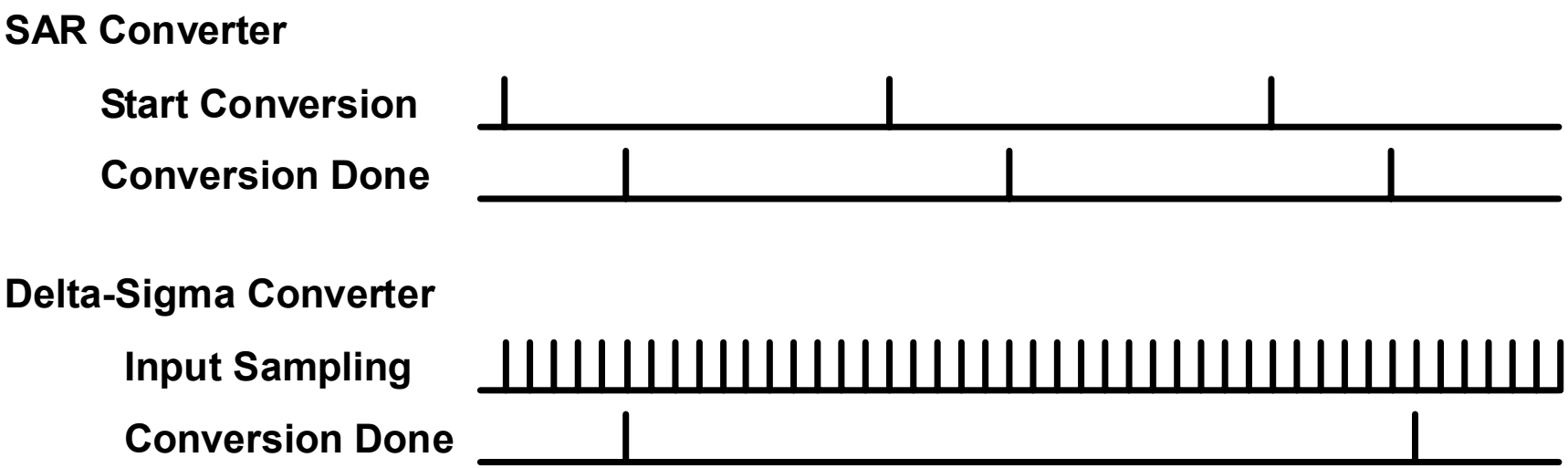
Settling/Latency Comparison

- **SAR has fixed acquisition time**
  - Can multiplex easily
  - Takes a “snapshot” of signal in time
  - Can synchronize sampling to external events
    - Better for control systems!

- **Delta-sigma constantly sampling but complete system**
  - PGA
  - Input Buffer
  - Burnout Current Sources
  - Multiplexers
  - More complete system solutions

SAR vs Delta-Sigma Conversions

- SAR conversions have Start Conversion Signal
- Delta-Sigma is always sampling/converting



Agenda

- What are the Signal Frequencies
  - Analog Classes of applications
  - Frequency ranges of ADCs
- Nuts and Bolts of Delta-Sigma Converters
  - $\Delta\Sigma$ Converter Core and Auxiliary $\Delta\Sigma$ Functions
  - Applications for the $\Delta\Sigma$ Converter
- The SAR ADC
  - Input Stage Dynamics
  - Applications for the SAR Converter
- The High-speed Pipeline Topology
  - Driving the Capacitive Input Stage
  - Applications for the Pipeline Converter
- Conclusion

What's the Application?

Pipeline converters fit high-speed applications (5 MHz to >100MHz).

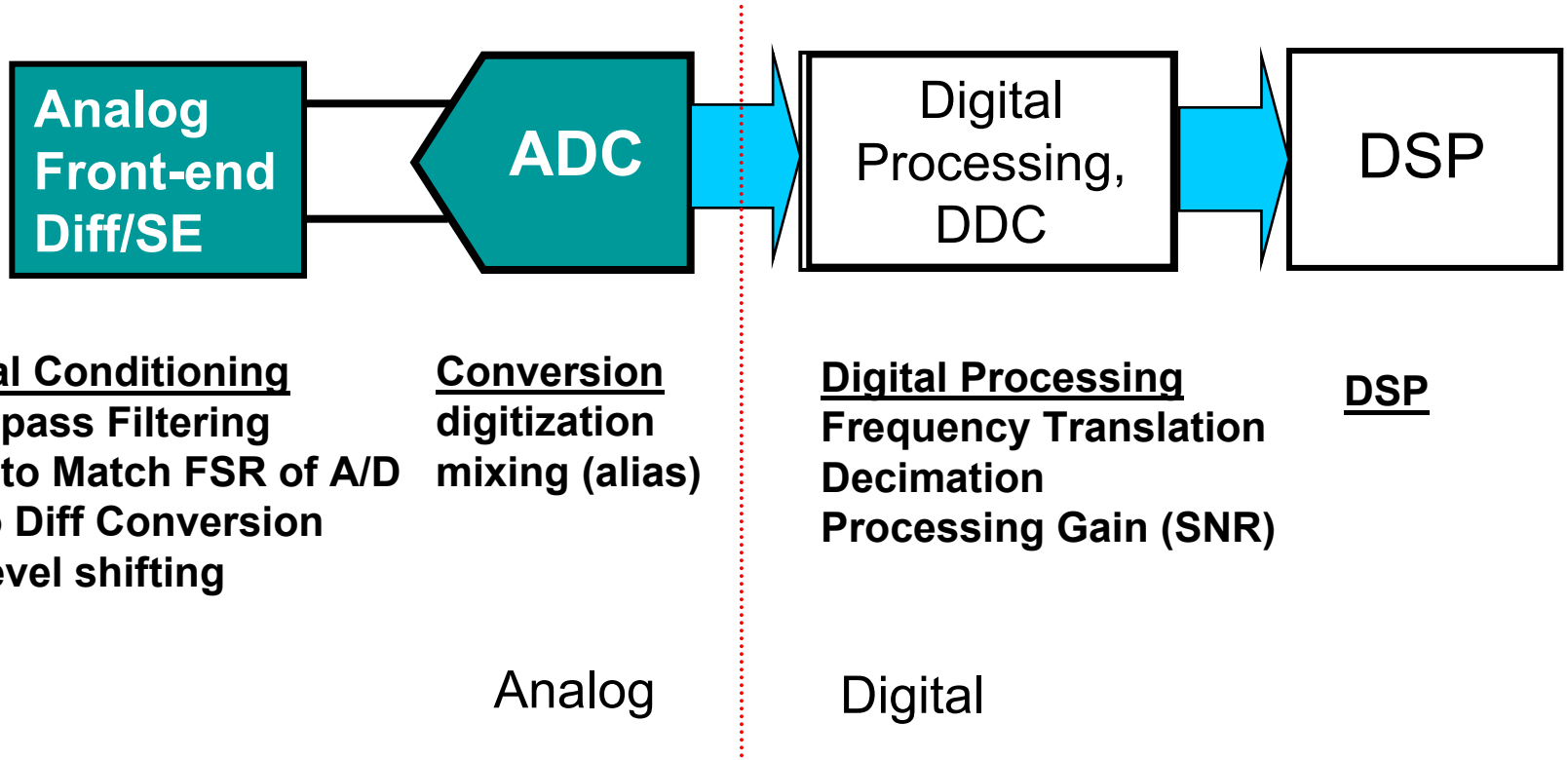
Time Domain

- **Imaging (CCD)**
  - **Camcorders**
  - **Digital Cameras**
  - **Scanner**
  - **RGB/Comp. Video**
  - **Test Instrumentation**
  - **Medical**
- **Important Specs:**
  - **SNR**
  - **Slew-Rate/ tset**
  - **DNL**
  - **DC-Accuracy/ Drift**

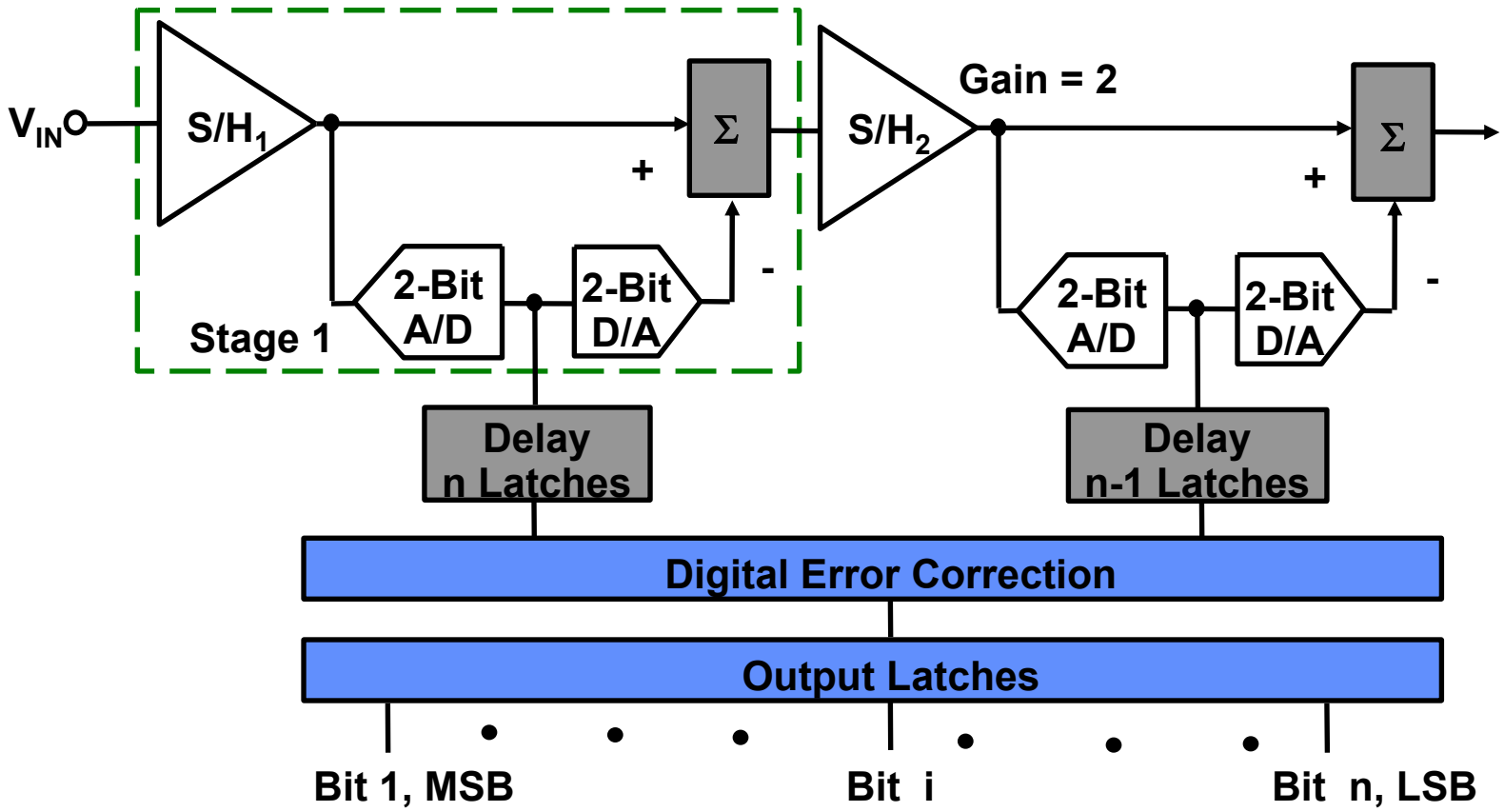
Frequency Domain

- **Communications**
  - **Set-Top Box**
  - **Cable Modem**
  - **Basestation**
  - **IF Digitizer**
  - **GPS**
  - **Frequency Synthesizer**
- **Important Specs:**
  - **SFDR**
  - **ENOB**
  - **Analog Input Bandwith**
  - **Jitter**

System

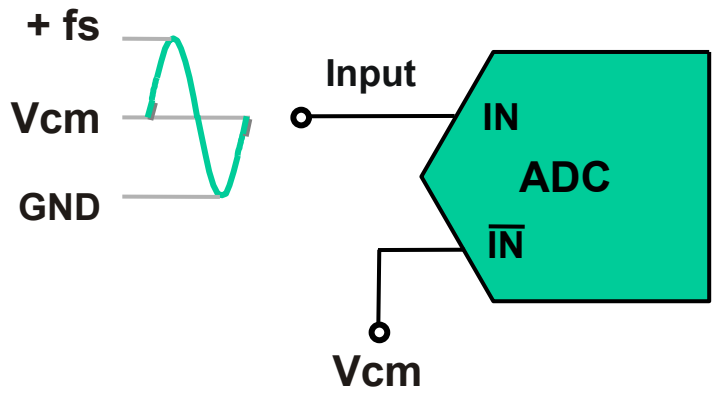

Analog Front-end Diff/SE
ADC
Digital Processing, DDC
DSP
Signal Conditioning
Bandpass Filtering
Gain to Match FSR of A/D
SE to Diff Conversion
DC-level shifting
Conversion
digitization
mixing (alias)
Digital Processing
Frequency Translation
Decimation
Processing Gain (SNR)
DSP
Analog
Digital

Pipeline A/D Converter Architecture Overview



ADC Interface Solutions
Principle Configuration Choices

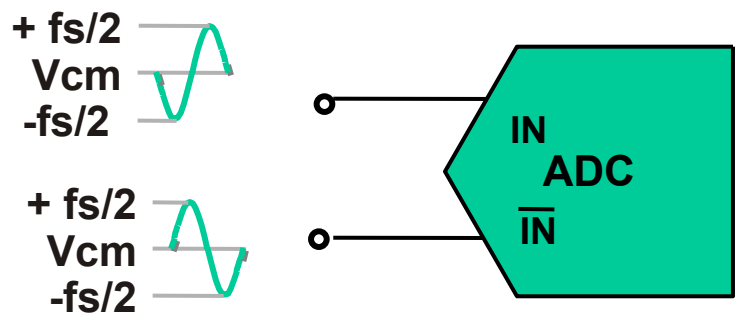
Single-Ended Input (SE)



Requires full input swing from +fs to –fs
2x the swing compared to differential
Input signal at IN typically requires a common-mode voltage for bias
Input IN\ also requires a Vcm for correct dc-bias

ADC Interface Solutions
Principle Configuration Choices

Differential Input (DE)



Combined Differential inputs result in full-scale input of +fs to –fs

Each input only requires 0.5x the swing compared to single-ended

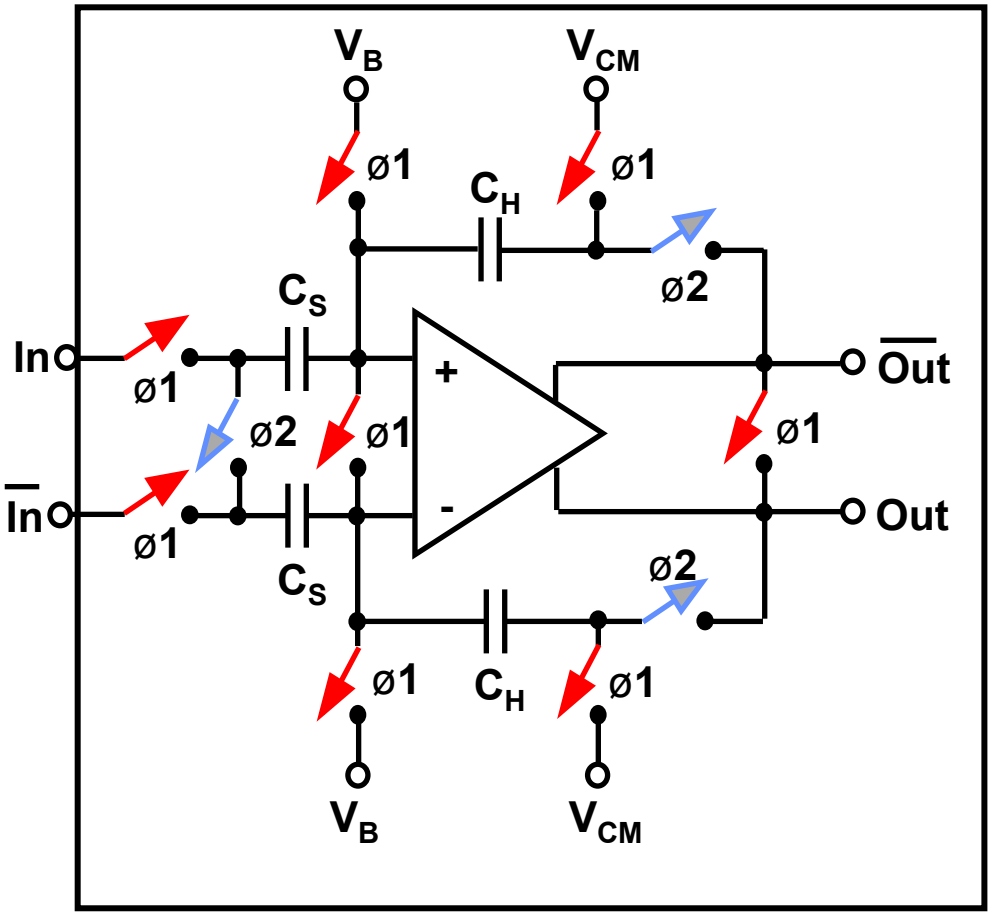
Both inputs require a Vcm for correct dc-bias

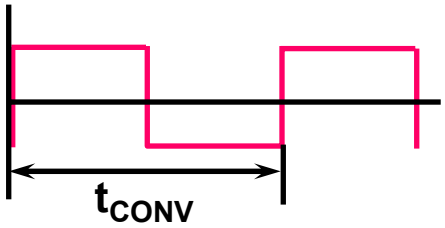
SE vs. DE Issues

- Single-ended Inputs (SE)
  - Degraded dynamic performance
  - Common-mode voltage and op amp headroom may limit use for dc-coupling
  - Best suited for Time Domain applications

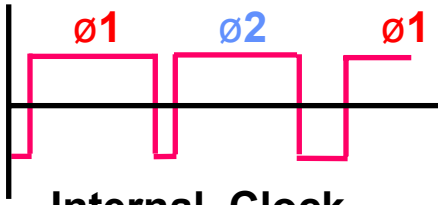
- Differential (DE)
  - Optimized performance due to reduction of even-order and common-mode components
  - Best for higher input frequencies (IFs)
  - More complex driver circuitry (consider Diff – Amps)
  - Best suited for Frequency Domain applications

HS-ADC Simplified Input Circuit





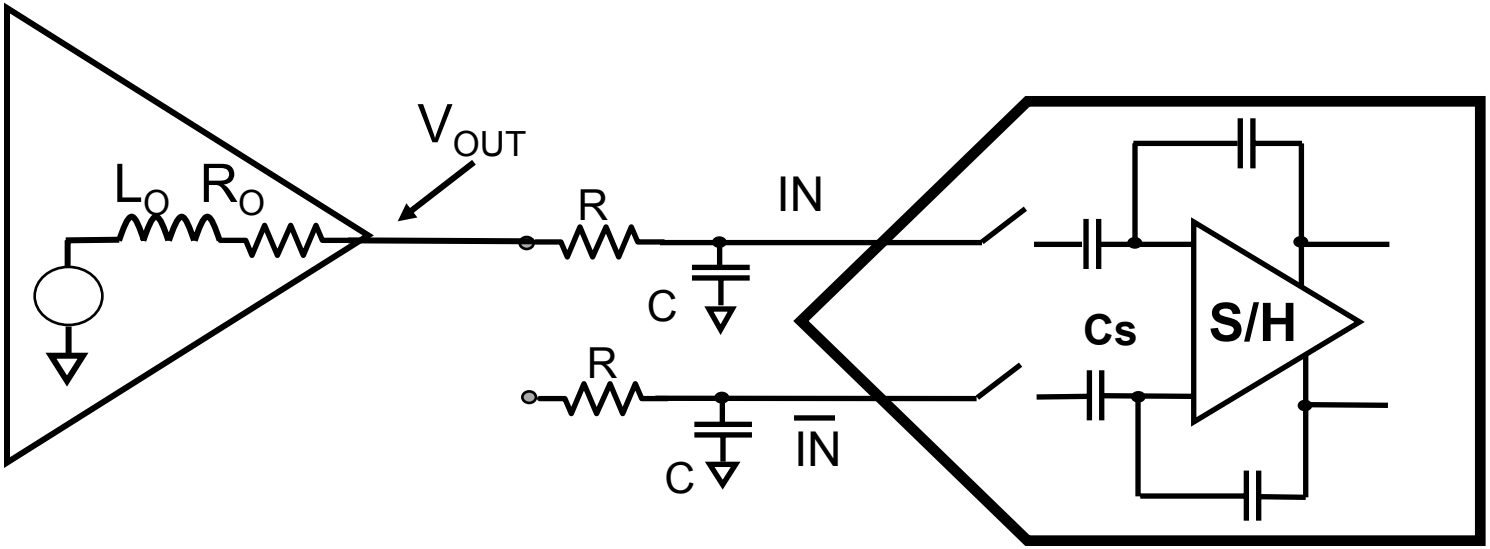
Input Clock



Internal Clock, non-overlapping

- Requires minimum clock frequency

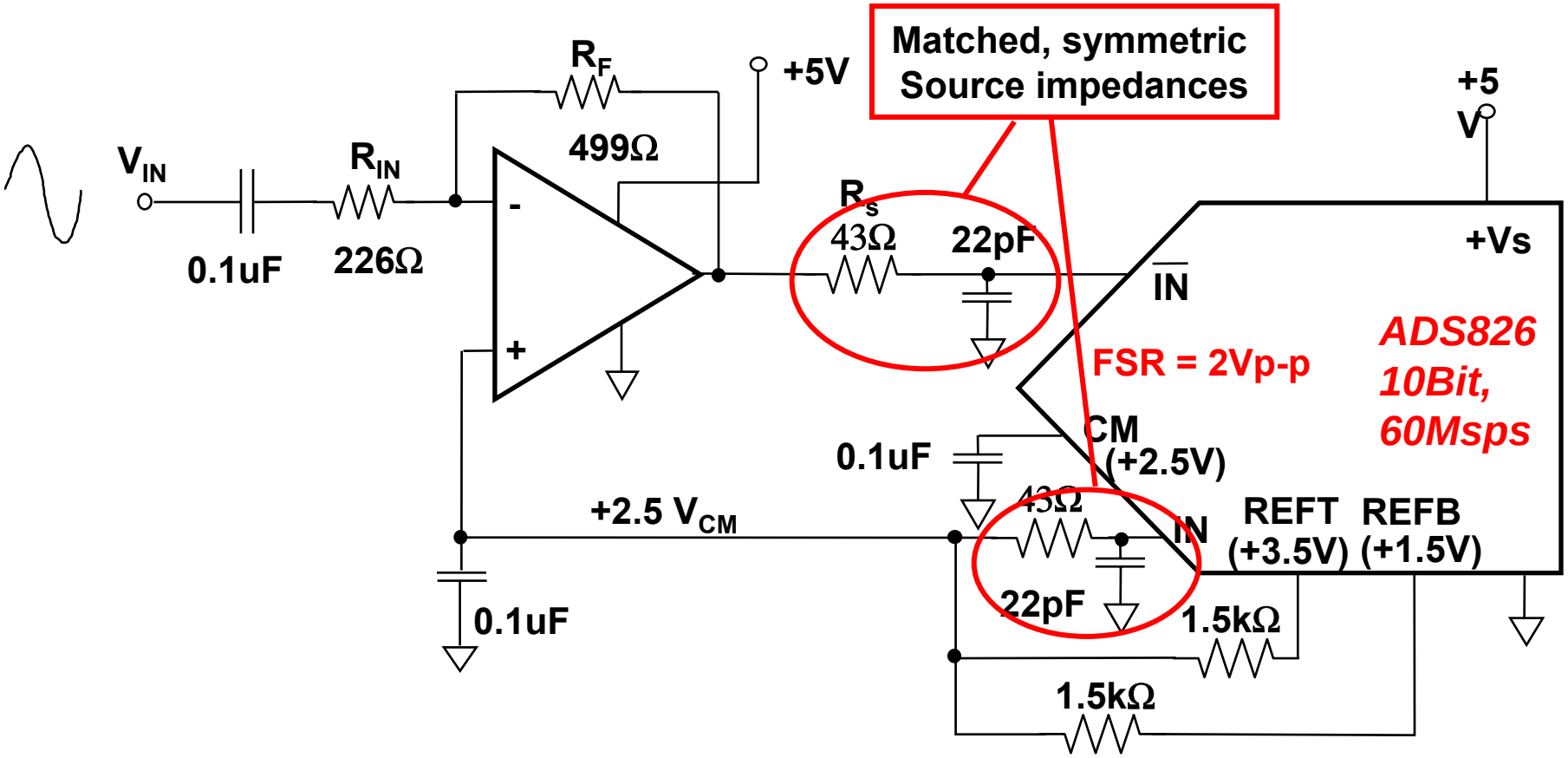
Driving Capacitive Input ADCs



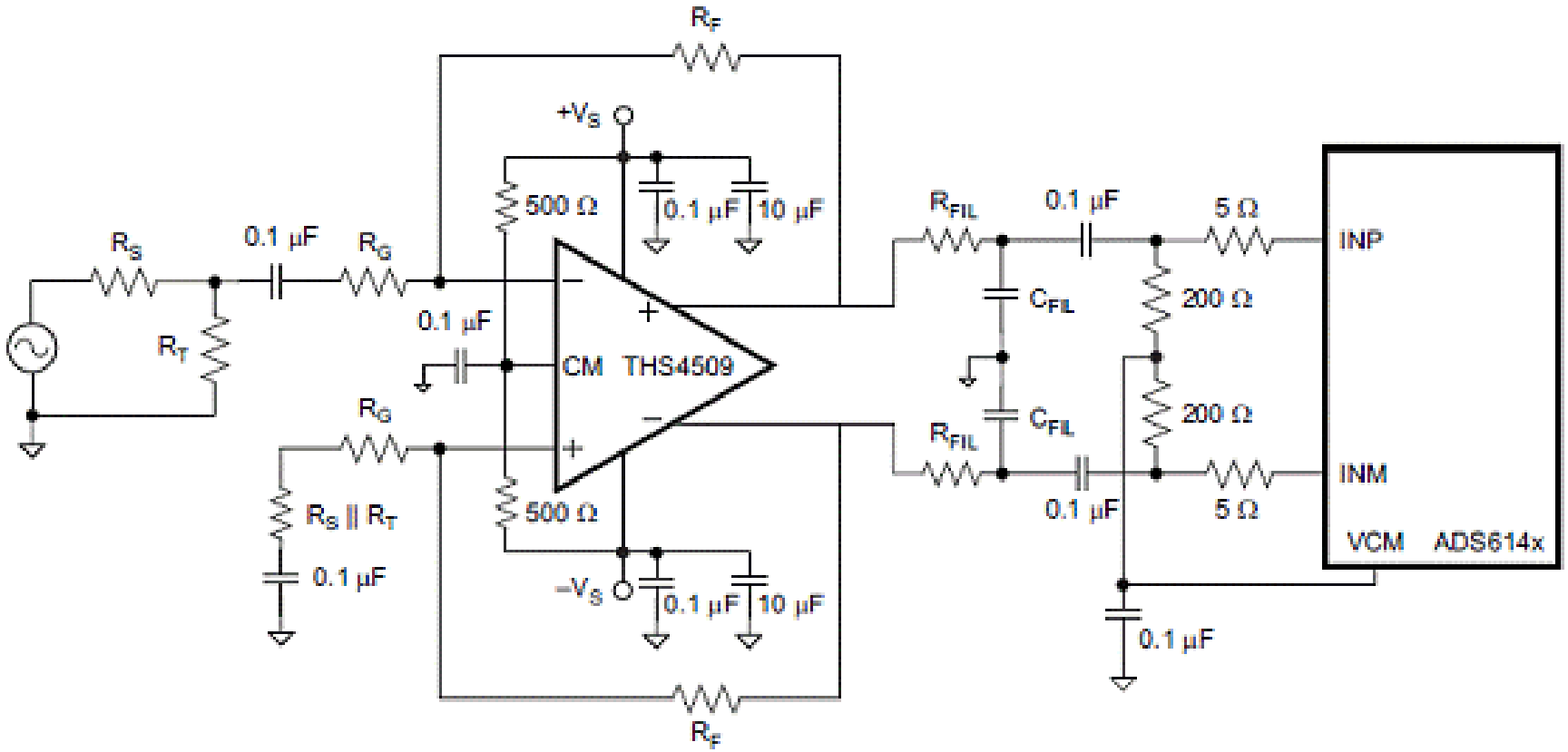
- Due to Opamp's finite (R_O) output impedance, V_{OUT} will drop momentarily when cap load is switched.
- As the output recovers, ringing may occur, which results in increased settling time.
- Use external R: isolates OpAmp output from capacitive load and improves settling.

SE –Interface

Single-ended, ac-coupled driver for single supply operation



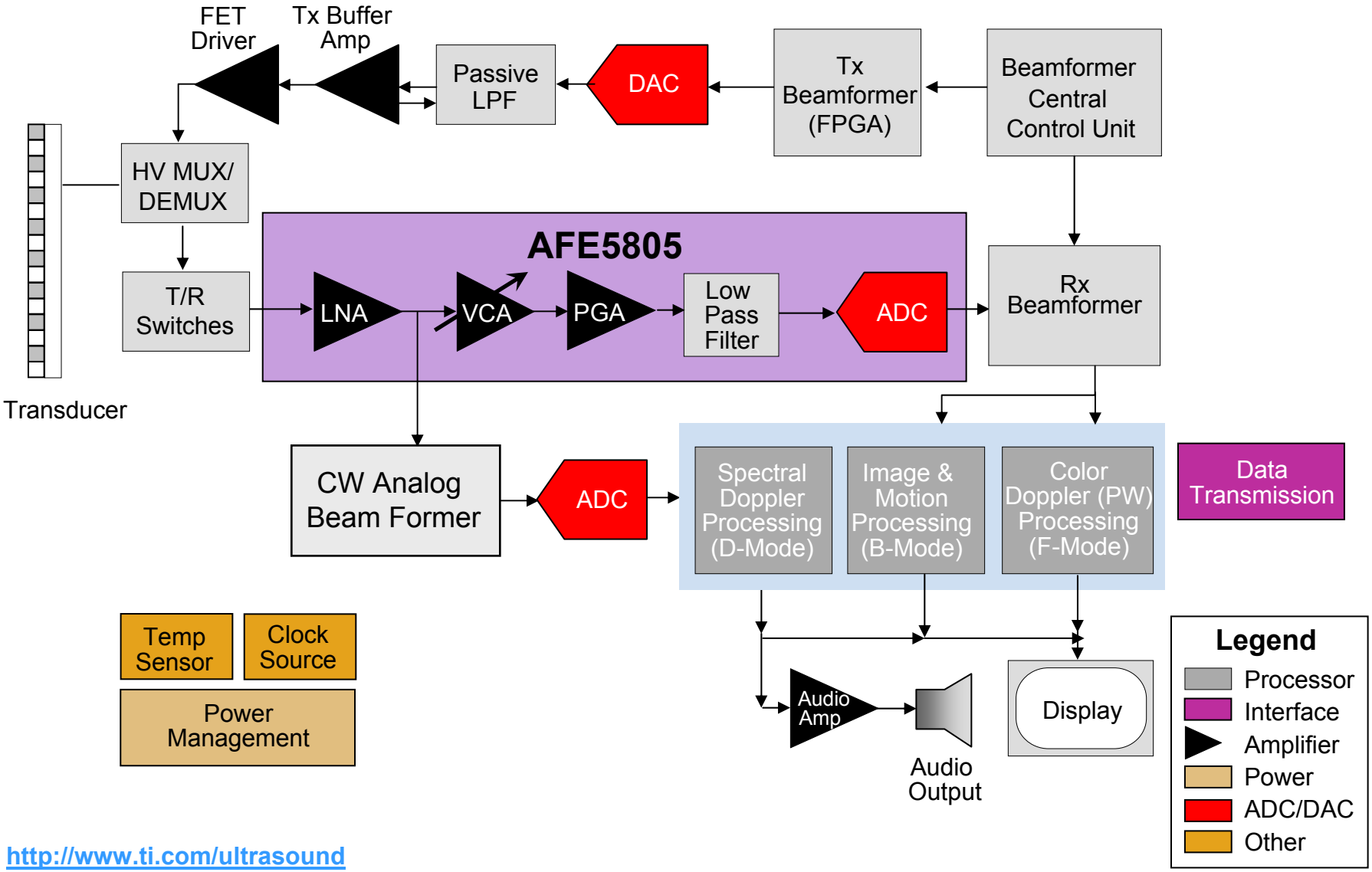
Differential ADC Driver



Driver Solution:

- No Transformer
- VCM matched to ADC
- Good even-order harmonic rejection
- Easily configured for gain and low-pass filter

Ultrasound system block diagram



http://www.ti.com/ultrasound

CONCLUSION: Delta-sigma, SAR, Pipeline ADCs

- Commonalities
  - Input Stage
  - Input Driving Amplifier
- Differences
  - Sampling Frequencies
- Appropriate Applications
  - Delta-Sigma: DC up to 30 ksps
  - SAR: 10 ksps up to 5 Msps
  - Pipeline: 1 Msps up to 550 Msps

Choose the right A/D converter for your application