Techday Kiev

Precision Analog Components for low power Applications

Texas Instruments

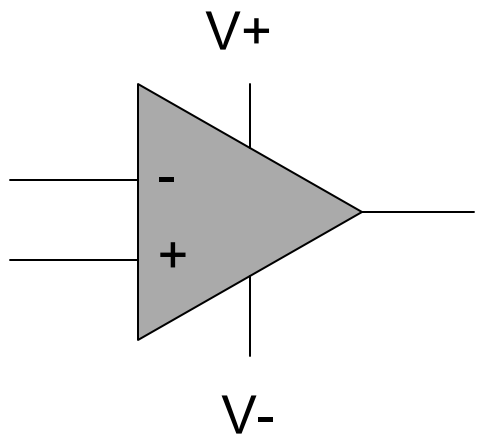
Precision Analog Components for low power Applications

- Amplifier Family-Overview
- Process Overviews
- Zero-Drift Amplifiers
- e-trim'ed Amplifiers
- Zero-Crossover Amplifiers
- Differential & Instrumentation Amplifiers
- Audio Amplifiers
- ADC power-criteria

Everfit OPAMP

Unlimited VDD and VSS
Zero Quiesent Current
∞ Power Supply Rejection Ratio

Zero Input Current
∞ Input Impedance
Unlimited Input Voltage Range
Zero Noise (Current and Voltage)
Zero Offset
∞ Common Mode Rejection



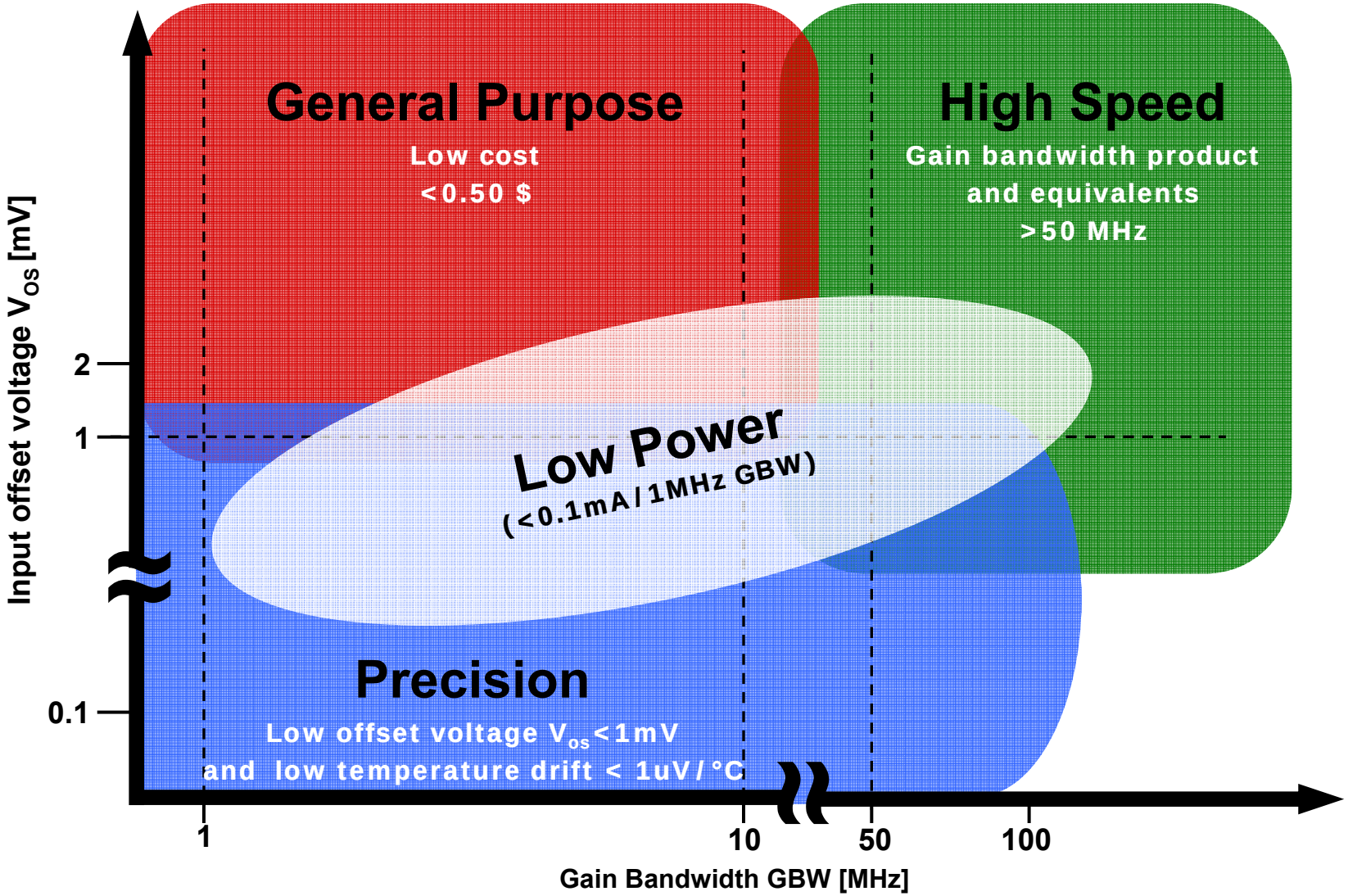
Unlimited Vout
Unlimited Iout
∞ Slew Rate
Zero Output Impedance

∞ Open Loop Gain
∞ Bandwidth
Zero Distortion

Without any temperature influence (Zero Drift)

Zero Cost ;-)

Amplifier overview

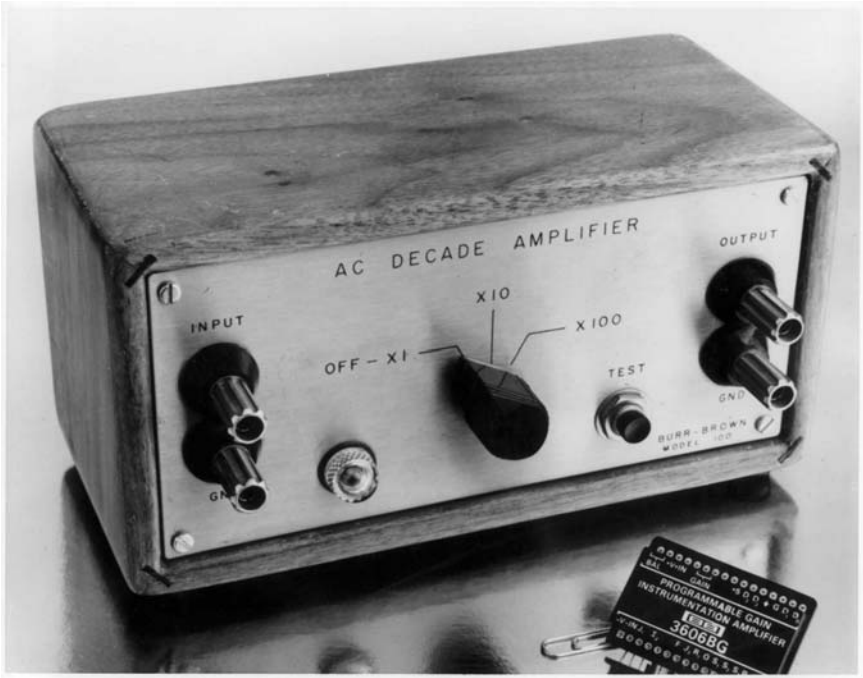


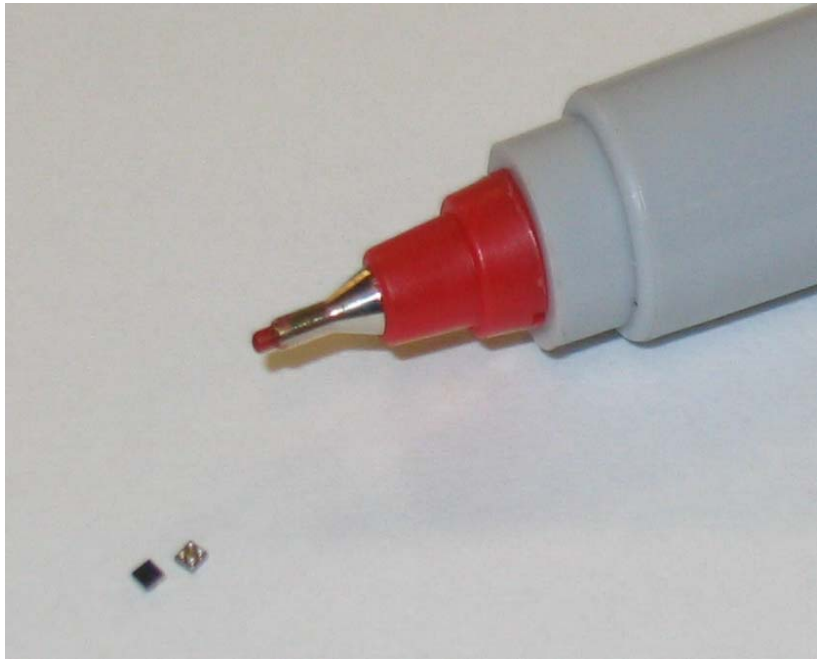
Smaller, higher performance, cheaper

Smaller and cheaper

Smaller and cheaper

Smaller and cheaper





Process overviews

Two main Processes: Bipolar and CMOS

Dataconverters are nearly all built on CMOS. Internal Caps are needed and they are easier to realize with CMOS. Also the internal switches work more precise when realized with FETs.
Only some R2R DACs used to be Bipolar.

Amplifiers are built on Bipolar and CMOS Processes.

What about JFET Amplifiers?

They are built on a bipolar process.
Therefore usually only the Inputstage is JFET and the rest of the part bipolar.
We have one exception, the OPA604 which has all-FETs Signalpath.
Purpose was Audio-applications. The sound is more of a tube-sound.

TI Mixed-Signal Roadmaps

Analog CMOS:
- Logic, Passives, Analog
- Integration & Voltage
- High-Performance Branch

Power BiCMOS:
- Logic, Passives, & Power
- LDMOS, Thick Cu Enablers
- Voltages up to 120V

High-Performance BiCMOS:
- Complementary Bipolar
- Speed & Precision
- SiGe & SOI

HPA07 Overview

– Data Converters & Amplifiers –

- Technology Features:
- 200mm Wafers
- 0.30 um Features
- 5V (3V) Operation
- 120 A (75 A) Gate Ox
- TLM (0.7 um Pitch)
- SiCr Thin Film Resistor
- Metal-Silicide Capacitor
- Optimized CMOS Noise
- Cu Power Metal Option
- Laser Trimming
- 17K Gates/mm^2

Component Set:

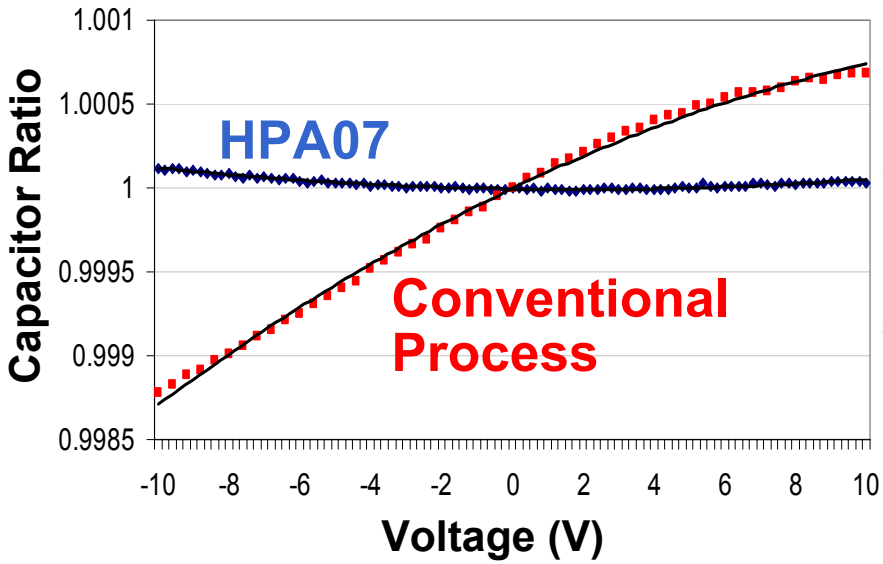
- CMOS: 5V or 3.3V
- Low-VT CMOS
- Isolated CMOS
- Poly Resistors
- Well Resistors
- Thin Film Resistor
- TiN-Polycide Capacitor
- DECMOS: 18V – 30V
- Isolated VNPN
- PNP
- JFET

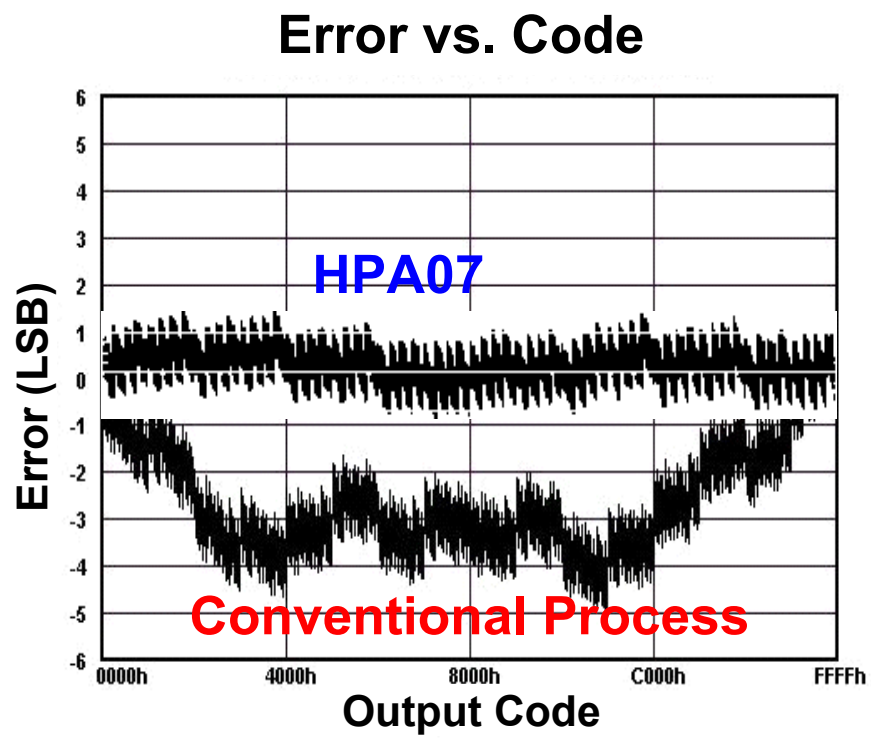
HPA07 High-Precision Analog CMOS

HPA07

Features	Benefits
◆ 0.3 µm feature sizes	◆ Higher speeds and accuracy
◆ 5V isolated CMOS transistors	◆ Improved Signal-to-Noise Ratio (SNR) ◆ Integration of analog and digital
◆ Very low noise	◆ Improved Signal-to-Noise Ratio (SNR)
◆ Metal-metal capacitor	◆ 4x increase in accuracy ◆ 40% area reduction
◆ Precision thin-film resistors	◆ Lower test costs ◆ 30% reduction in package size

HPA07: Better Capacitors Mean Better A/D Converters





The Most Important Component in Precision A/D Converters

Technology Leadership

HPA07

For High Precision

- Extremely Low CMOS 1/f Noise
- Advanced TFR and Capacitor
- Low Parasitics – Aggressive Metal Pitch
- Fully Qualified, in Production

HPA07HV

For High Precision & Voltage

- Leverages Advanced HPA07 Process
- Adds True 36V CMOS Capability
- Advanced TFR and Capacitor

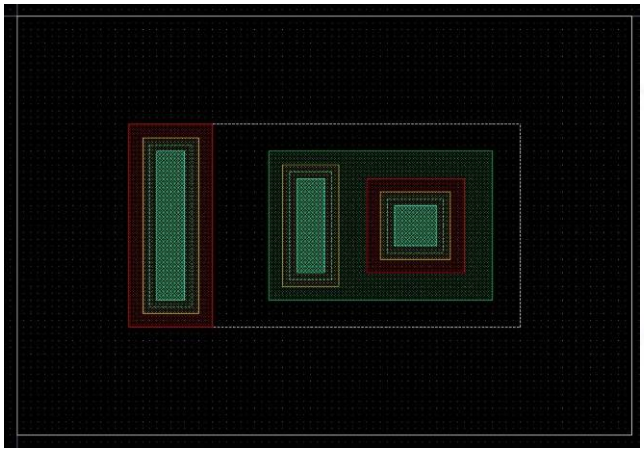
HPA07HVBJT

For Highest Speeds and Precision

- **Leverages Advanced HPA07HV Process**
- **Add Complimentary 42V NPN & PNP Devices**

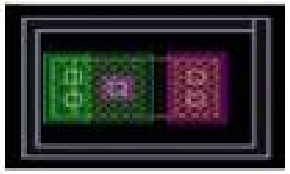
BiCom3xHV
Transistor Area Comparison

P435
Minimum NPN
108 um x 76 um
(8,200 um^2)



1980 NPN

Competitive technology
Minimum NPN
42 um x 28 um
(1,176 um^2)
~ 7X Area Reduction



2005 NPN Competition

BiCom3HV
Minimum NPN
11.5 um x 9.4 um
(108 um^2)
~ 11X Area Reduction
77X Total!

TI 2006 NPN

SOIC

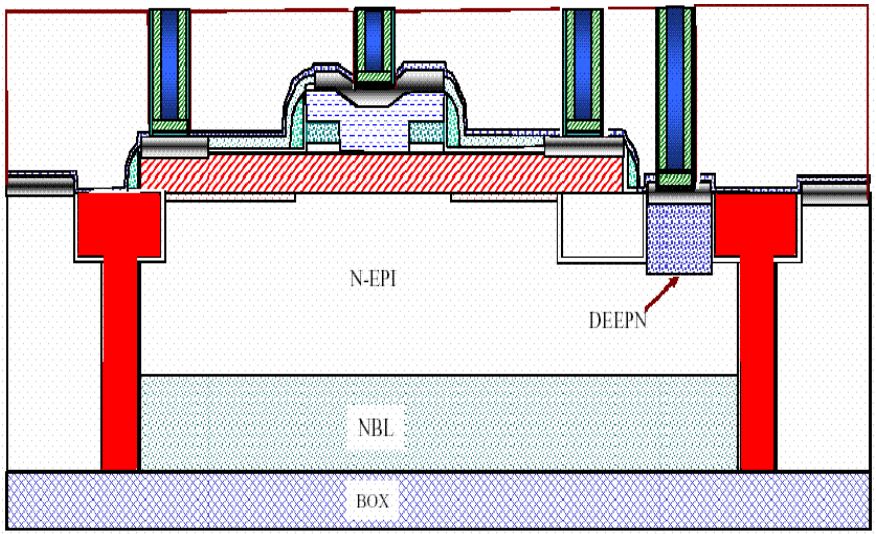
MSOP

SOT23

SC70

Bicom3xHV – State of the Art 36V Process

- **Silicon on Insulator**
- Transistors are isolated with true insulator or trench
- Parasitics Eliminated or Reduced
- Reduced leakage: Low Ib
- Reduced Capacitance: Speed
- Zero variation of capacitance vs. voltage: Improved THD



- **Features**
- SiGe for best speed/power ratio.
- Goal for Max Supply: 40V
- Precision SiCr Thinfilm Resistors
- JFet
  - Low Leakage: 1pA
  - Low Noise: 1/f and wideband
  - Input can extend to GND
- Bipolar
  - Very low Offset and Drift
  - Low Ib though Super-β Transistor
  - Low Noise
- Small Feature size
  - Small Package Size

Why Does Process Technology Matter?

- The process used to build an Op-Amp has a significant impact on performance
- Four types are used
  - Bipolar
  - JFET
  - CMOS
  - Difet
- These technologies are sometimes combined
  - BiFET or Bipolar and JFET combination
- Process description is usually associated with input stage of the Op-Amp

CMOS Operational Amplifiers

- **CMOS devices are characterized as having**
  - Large Input Voltage Range, Input can often exceed both supplies,
  - Excellent Output Drive Capability, Output swings to within 1mV,
  - Excellent V_{OS}, 125µV
  - Very Low Power Requirements, Iq < 1 µA,
  - High Input Impedance, I_{bias} of 10 pA,
  - Low Cost, Built using small geometry "Digital" processes,
  - Wide variety of bandwidth and accuracy offerings.
  - Wide temperature range, -65 to +150 ° C

- **Battery powered, low to moderate performance systems**
  - Glucometer, CDAC ADC driver, CO and Smoke detectors

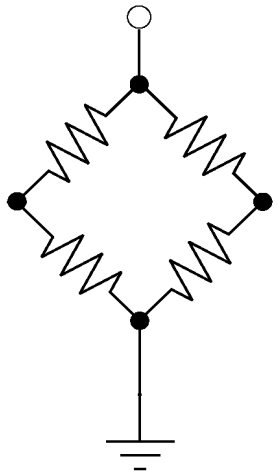
- **Example device OPA336**
  - ± 300mV, 3mV,125uV, 125µV, 1pA, 100kHz

Bipolar Operational Amplifiers

- **Bipolar Op-Amps are characterized by**
  - **Low input impedance, I_{bias} of 1 to 100 nA,**
  - **Low offset voltage , Vos as low as 10 μV,**
  - **Temperature Stability, Drift as low as 0.1 μV / °C,**
  - **Low Voltage Noise, Low as 1 nV√Hz.**

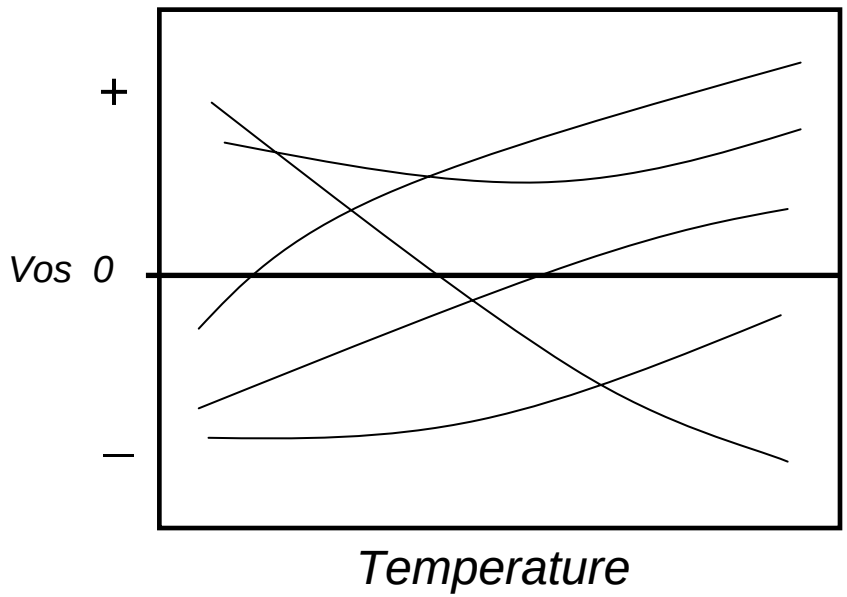
- **Small signal, low impedance high gain applications**
  - **Weigh Scales, Geophysical Analysis, High Precision Temperature Measurement.**

- **Example device OPA277**
  - **2.5nA, 10 μV, 0.1 μV / °C, 3 nV√Hz**



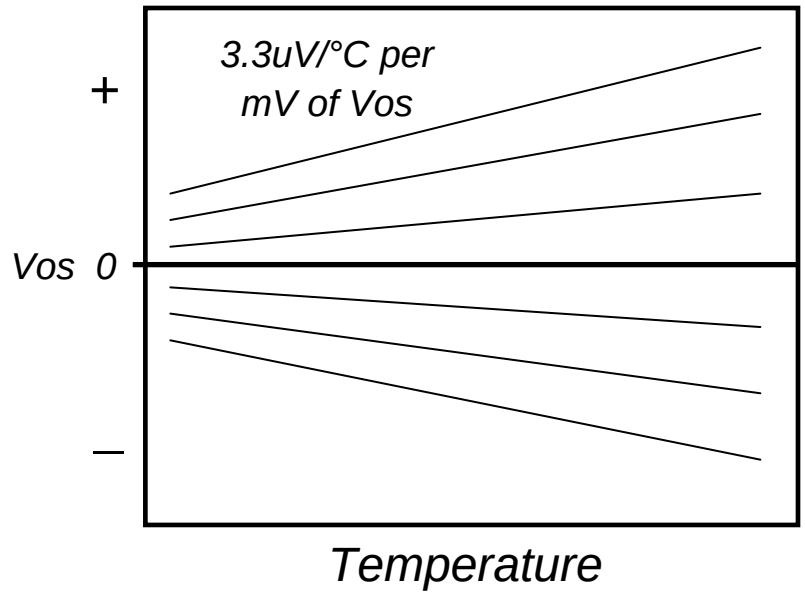
Offset and Offset Drift – CMOS vs. Bipolar

CMOS



- *Frequently have more curvature than bipolar*
- *When V_{os} trimmed to zero, drift remains.*

Bipolar

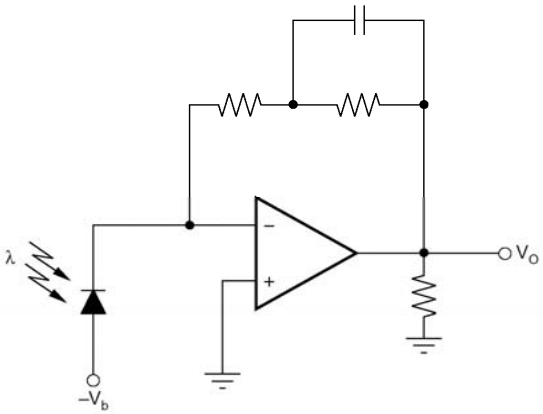


- *Drift is proportional to offset*
- *When V_{os} trimmed to zero, drift is near zero.*

Methods to produce CMOS Amplifiers with good Offset behavior include Auto-zero and eTrim

JFET Operational Amplifiers

- JFET Op-Amps are characterized as having
  - Moderately High Input Impedance, I_{bias} of 10 to 100pA,
  - Moderate Offset Voltage, V_{os} of 0.1 to 5 mV,
  - Large bias current changes with temp., I_{bias} doubles every 10 °C,
  - Lowest I_{bias} noise, As low as 4 fA/√Hz.
- High source impedance, moderate gain applications
  - Blood Analysis, CT Scanner, and Audio applications
- Example device OPA130
  - 20 pA, 1mV, 5 pA, 4 fA/ √Hz



Power-trade-off's

- Low noise
- High slew-rate
- Large Bandwidth
- High gain

Precision operational amplifiers

1.8V — 16V — 4.5V — 36V

Single supply CMOS

HPA07 (HV)

Dual supply Bipolar & J-FET

BiCom3 (HV)

OPA333 — Zero-drift

Stability over lifetime, drift matters

OPA364 — Zero-crossover

Ideal, homogenous rail-to-rail input with lowest distortion, i.e. Audio or ADC driver

OPA376 — e-trim

Low noise precision with guaranteed drift spec, i.e. test & measurement

OPA277 — Bipolar

Stability in rugged environments at lowest noise levels, i.e. weigh scales

OPA132 — J-FET

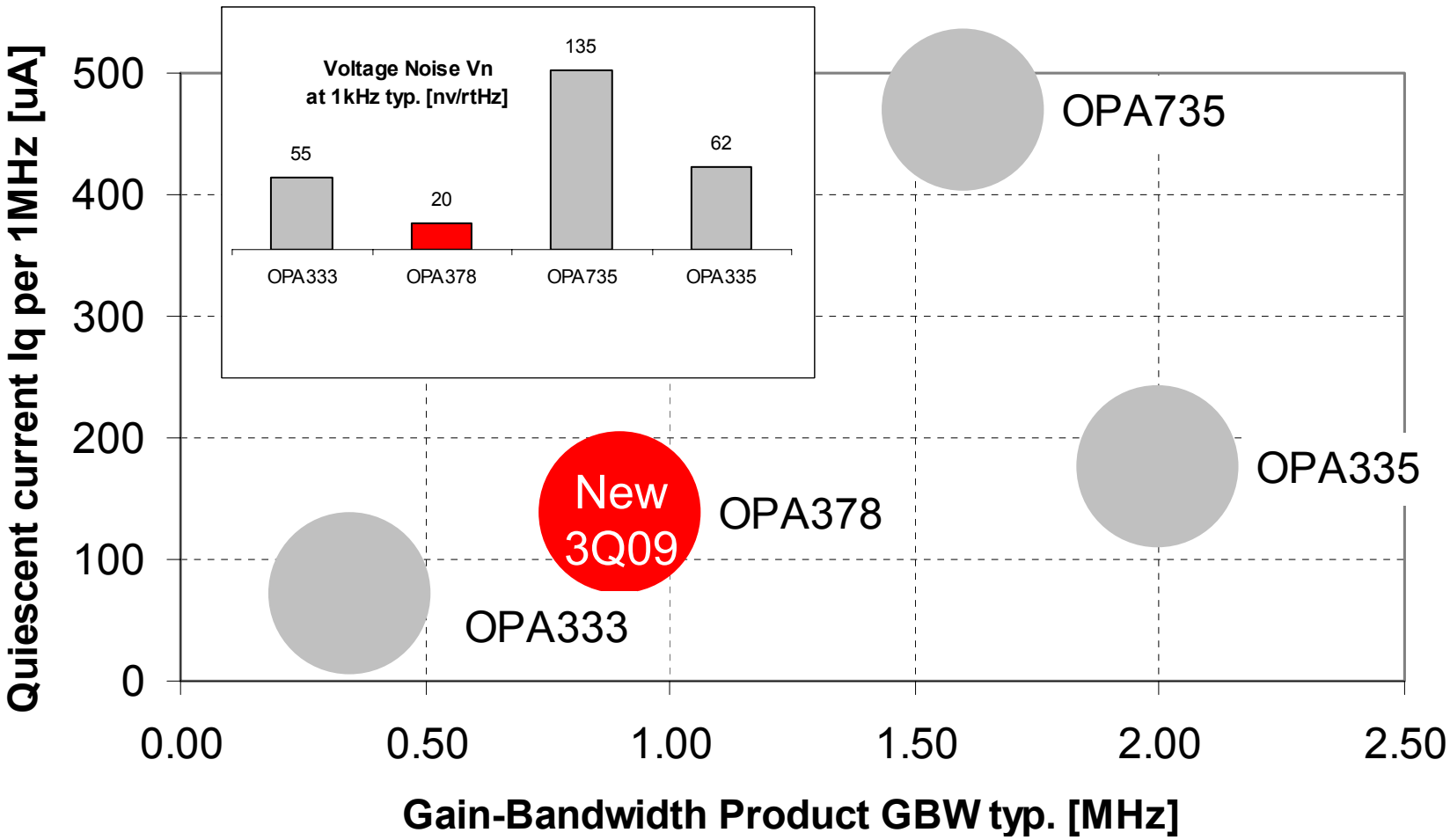
Signal conditioning for high impedance sources, i.e. sensors

Zero-Drift amplifiers

Bias current Ib *range* [pA]		
10	**100**	1000

Voltage noise Vn at 1kHz *range* [nV/rtHz]		
<10	25	**>50**

Offset voltage drift *range* [uV/degC]		
<0.1	1.0	>1.0



Zero-Drift Technology vs. Conventional Chopper Op Amp

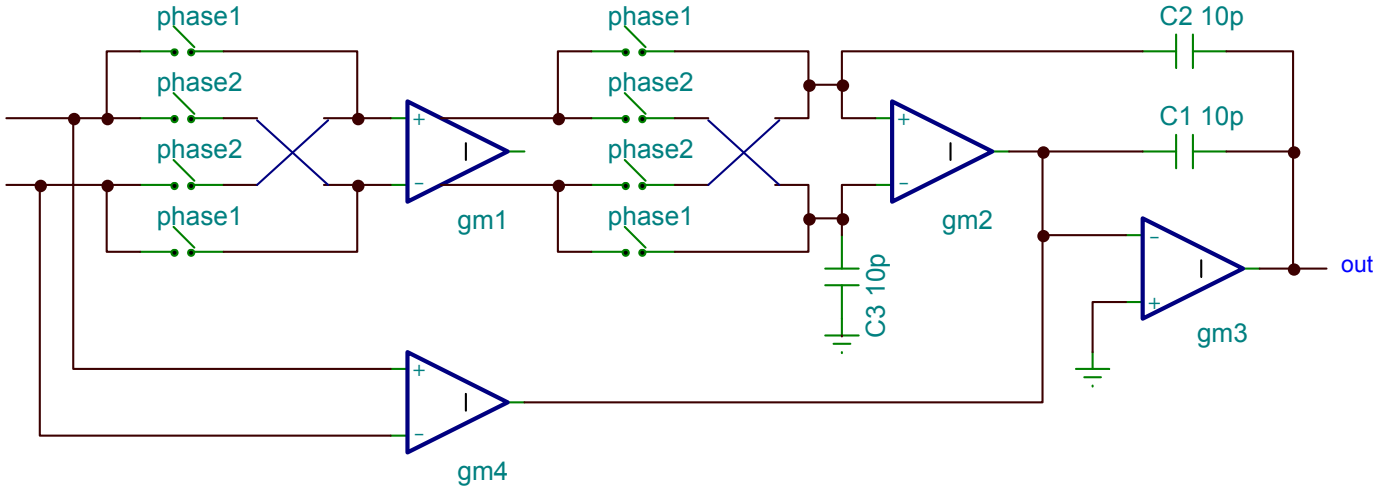
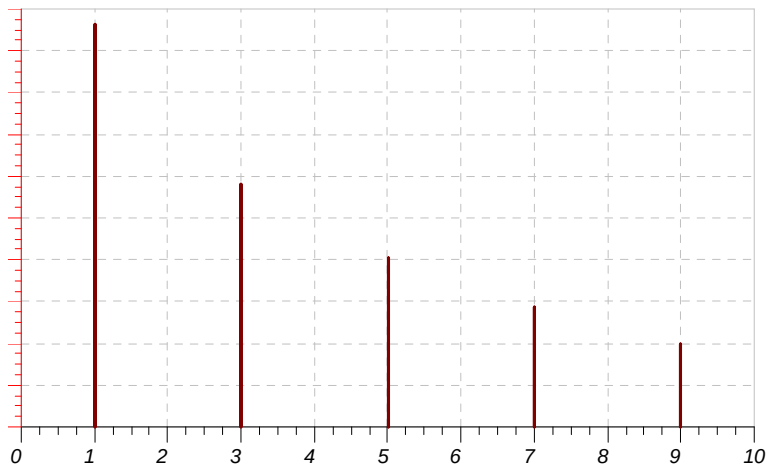


Figure 1. Low-speed zero-offset path (10,000x gain of high-speed path)

Frequency Domain



New Synchronous Notch Filter Technology

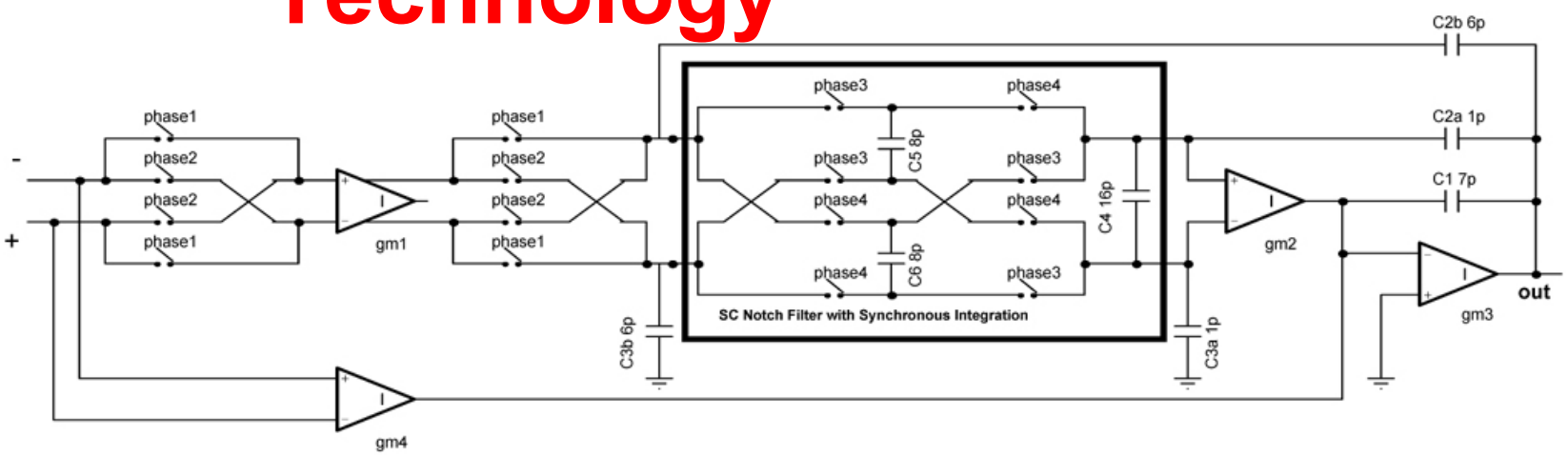
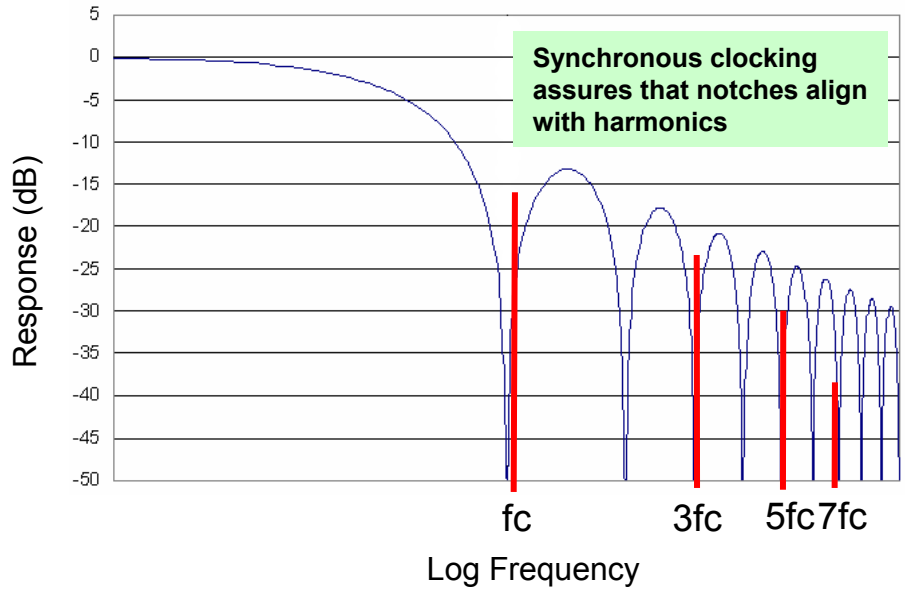
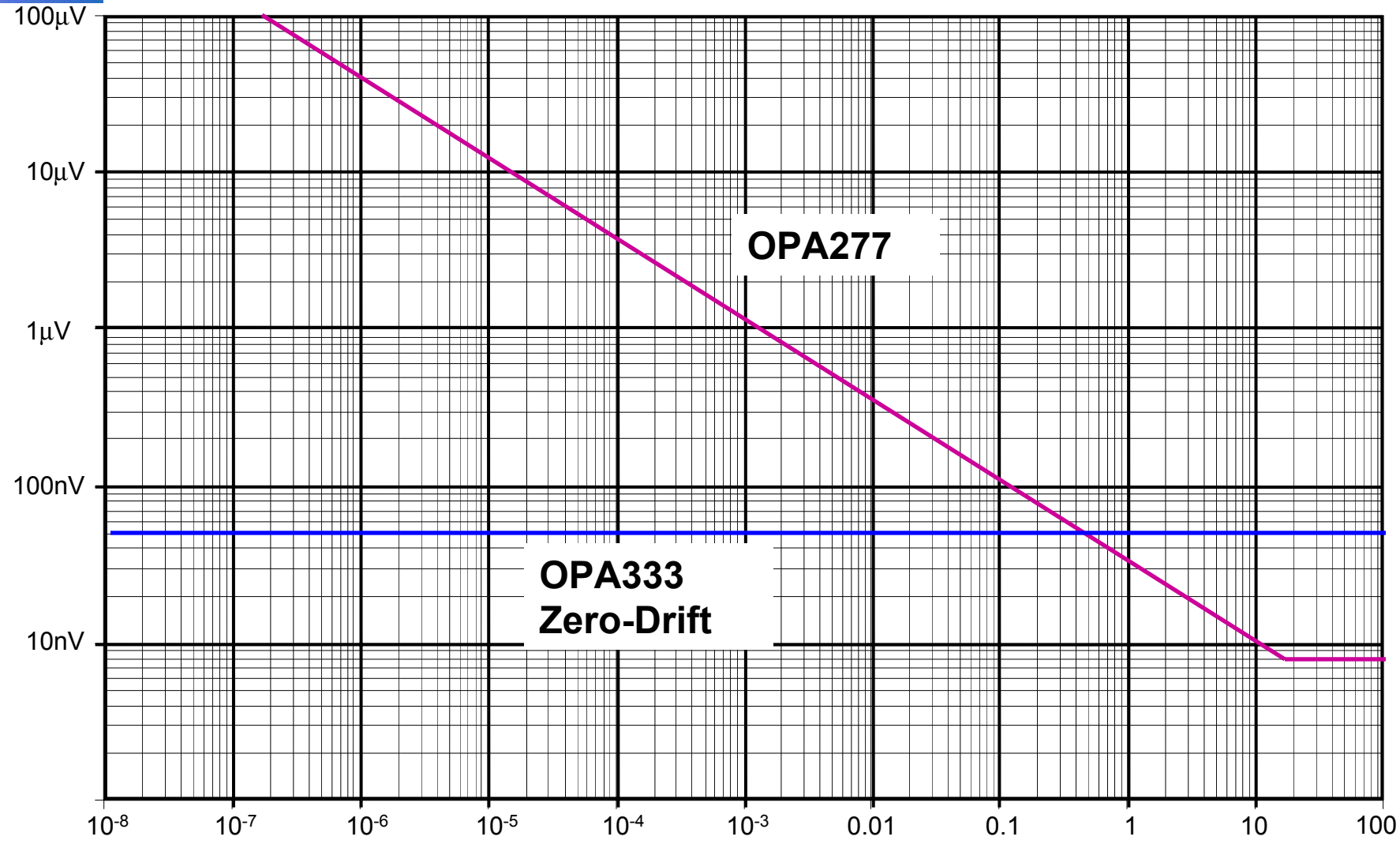


Figure 1. Switched-capacitor notch filter with synchronous integration included

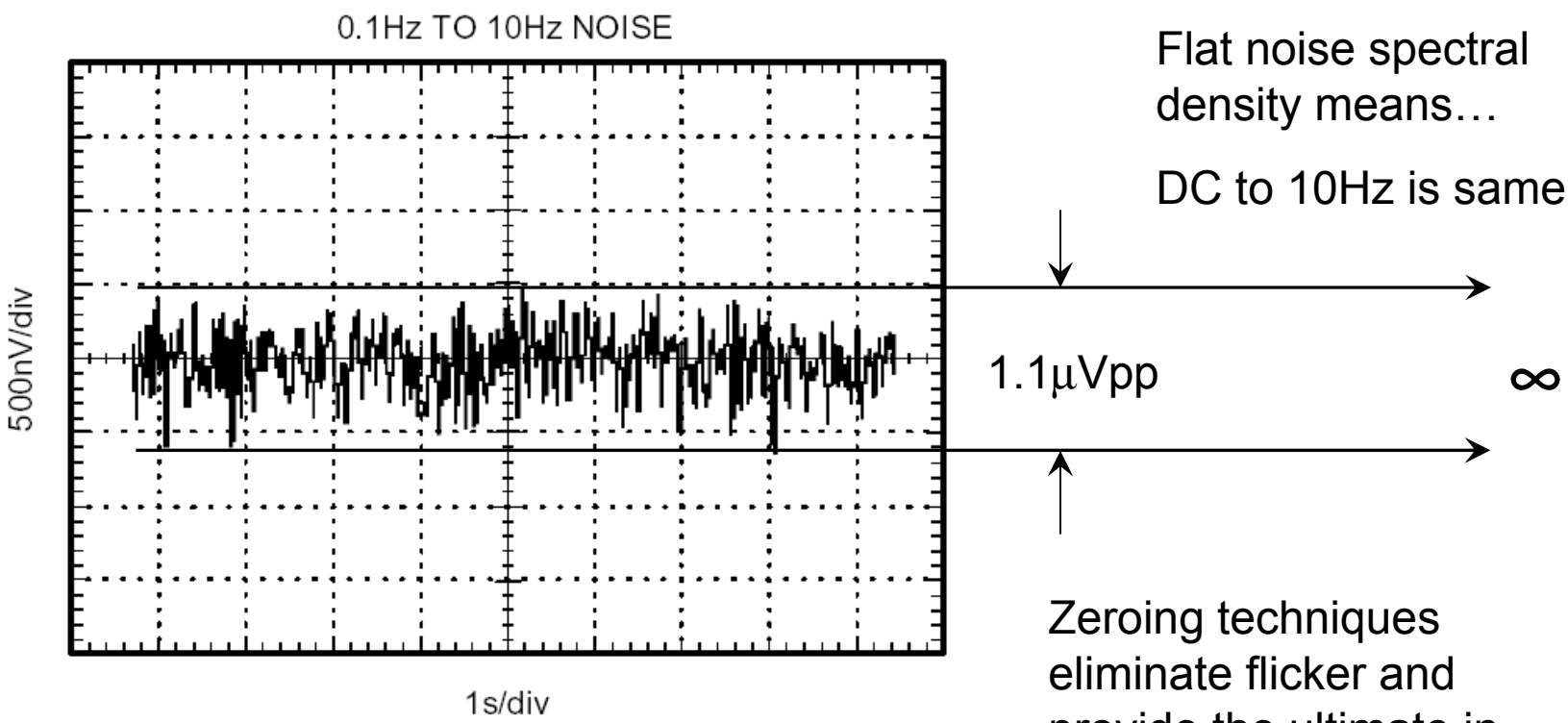
Synchronous Filter Response



Noise Density



Looking at Long Term Stability



Flat noise spectral density means…

DC to 10Hz is same.

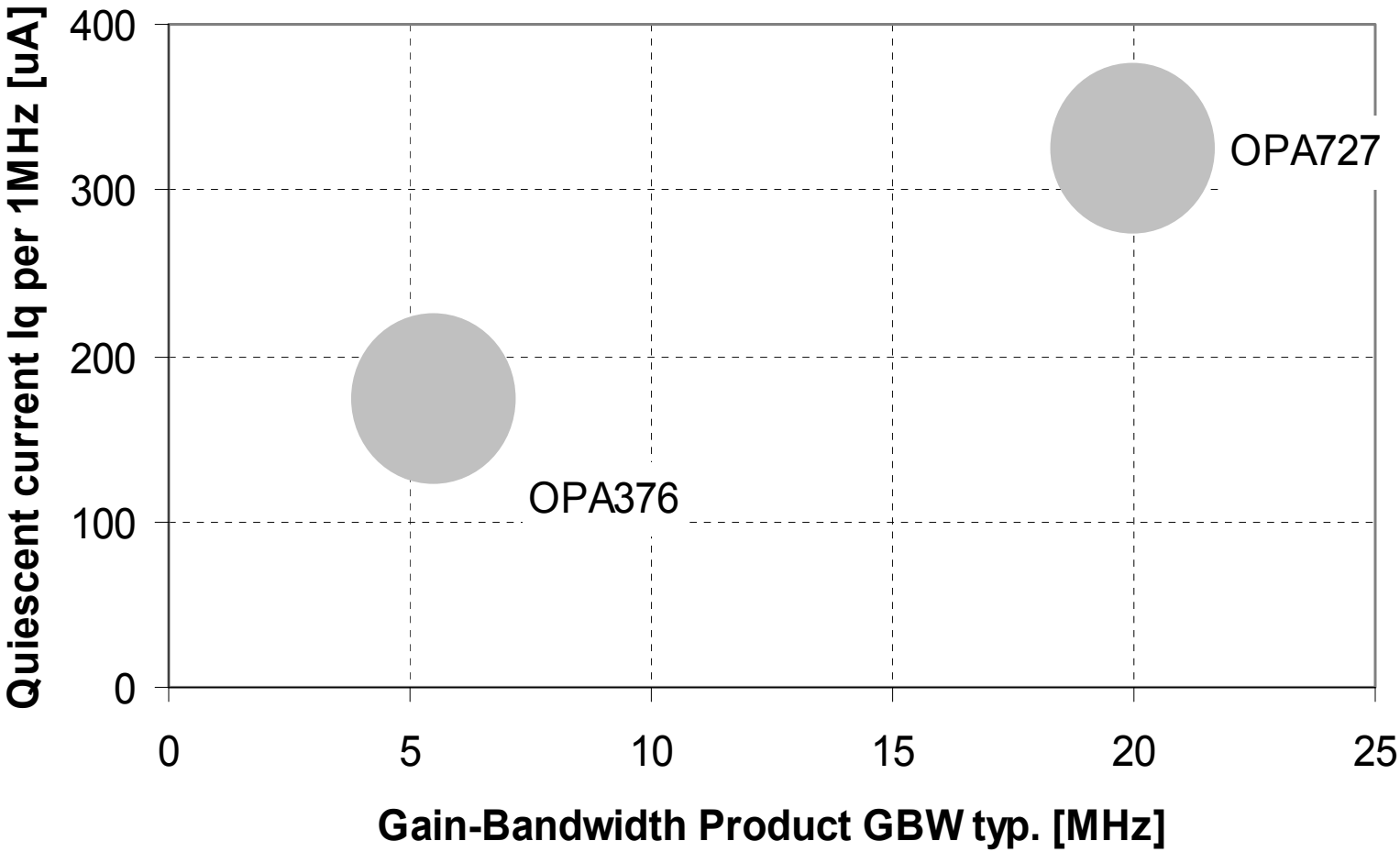
Zeroing techniques eliminate flicker and provide the ultimate in long-term stability.

e-trim Amplifiers

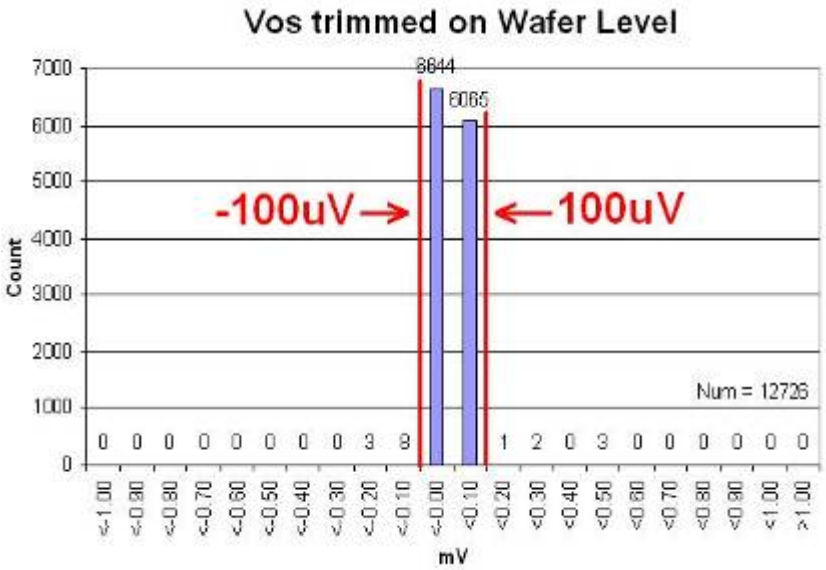
Bias current Ib *range* [pA]		
10	100	1000

Voltage noise Vn at 1kHz *range* [nV/rtHz]		
<10	**25**	>50

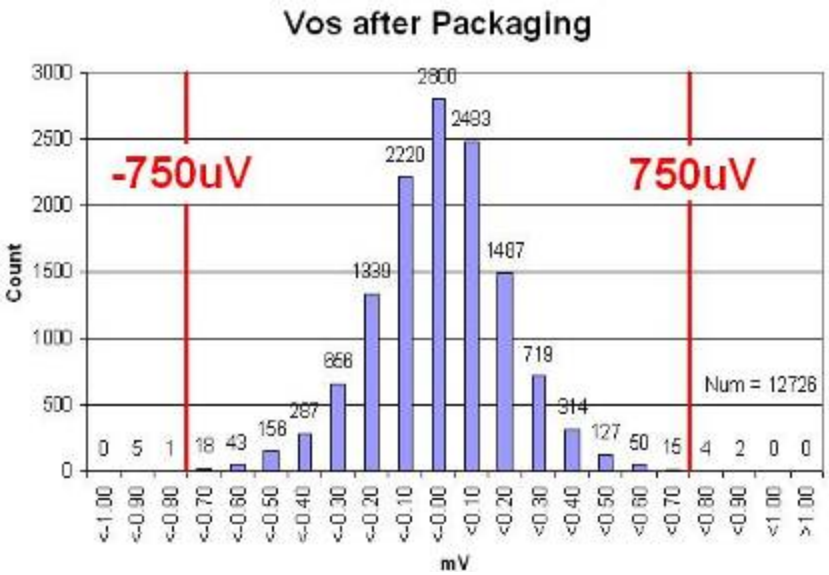
Offset voltage drift *range* [uV/degC]		
<0.1	**1.0**	>1.0



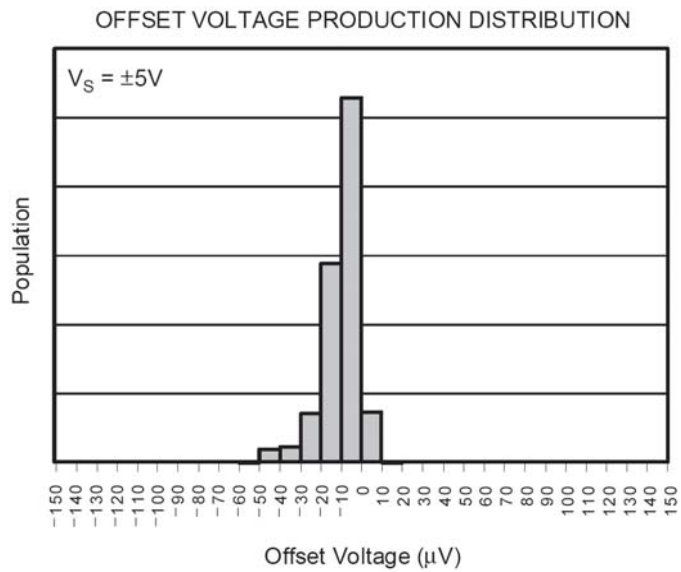
e-trim Technology



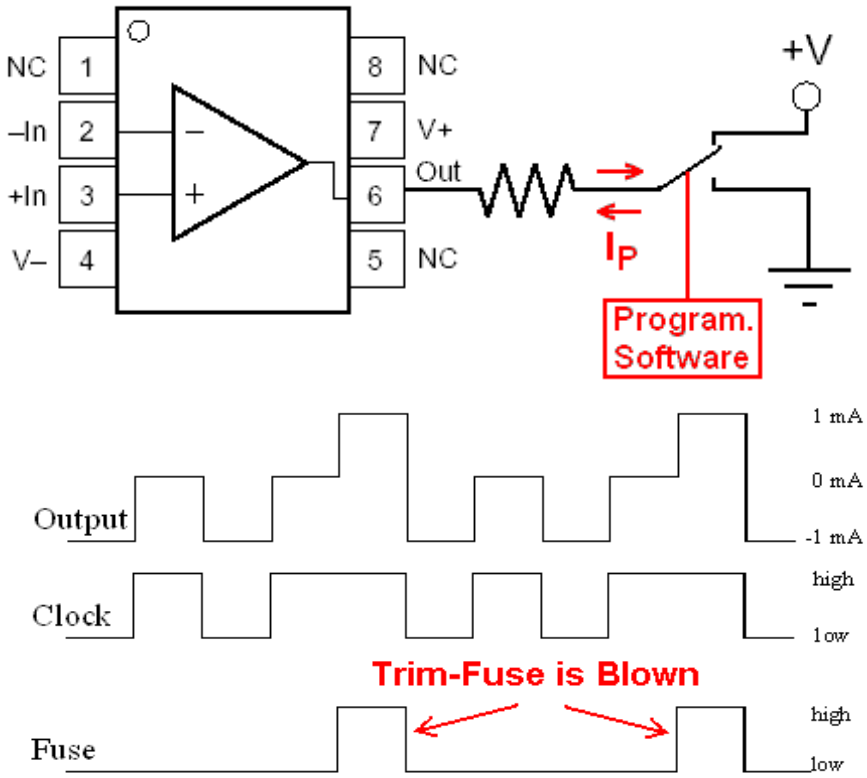
Packaging Stress



With e-Trim: 150uV!

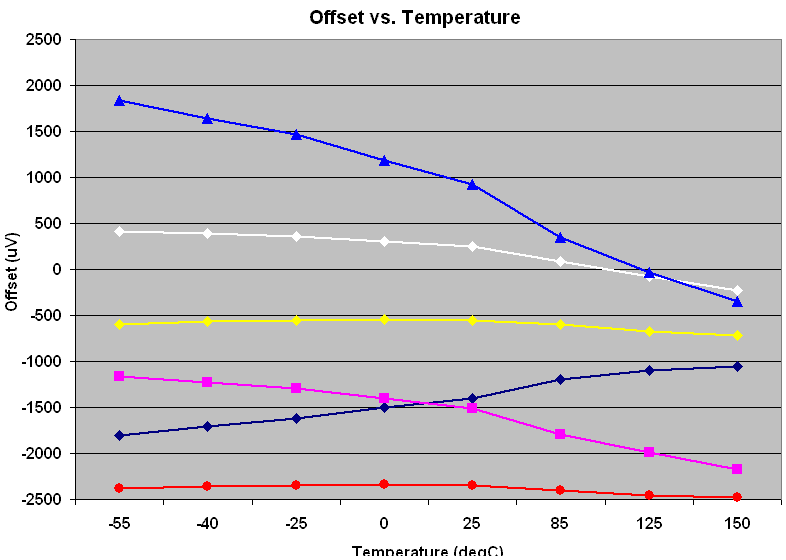


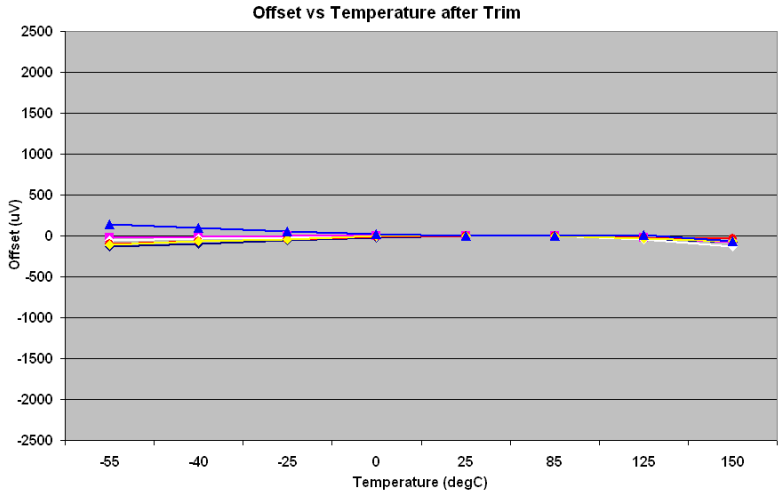
How is e-Trim Accomplished?



- **Standard Pinout!!**
  Trim Data is entered through output current load
- **Blow internal Fuses**
- **Fuses are read at each power-on**

What Parameters are Trimmed?





- Trimmed Parameters
- Tail Current
- Offset
- Offset Drift over Temperature

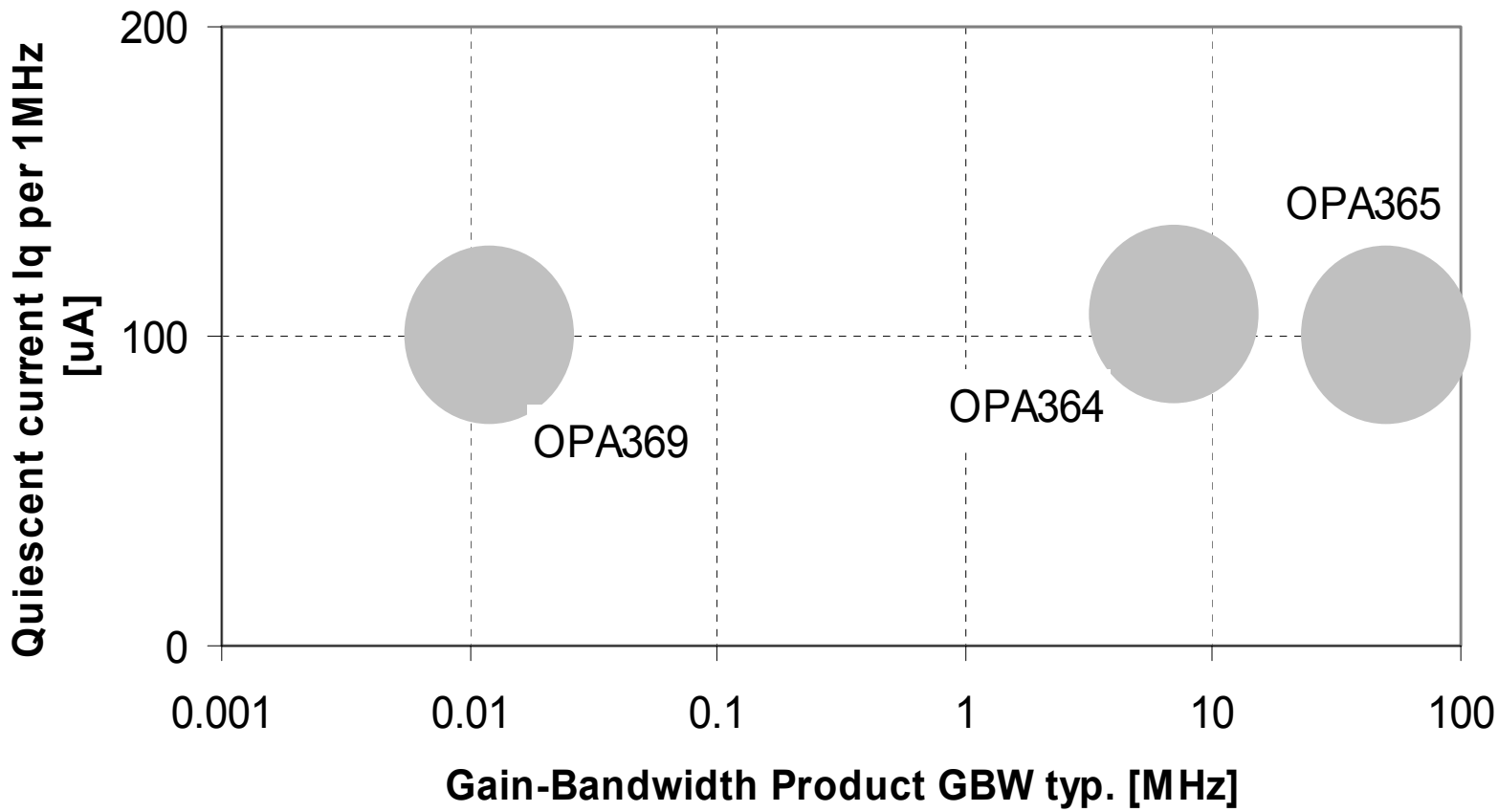
- Why is low Drift Important?
- Static Offset often Calibrated
- Temperature Drift often not Calibrated

Zero-crossover amplifiers

Bias current Ib *range* [pA]		
10	100	1000

Voltage noise Vn at 1kHz *range* [nV/rtHz]		
<10	**25**	>50

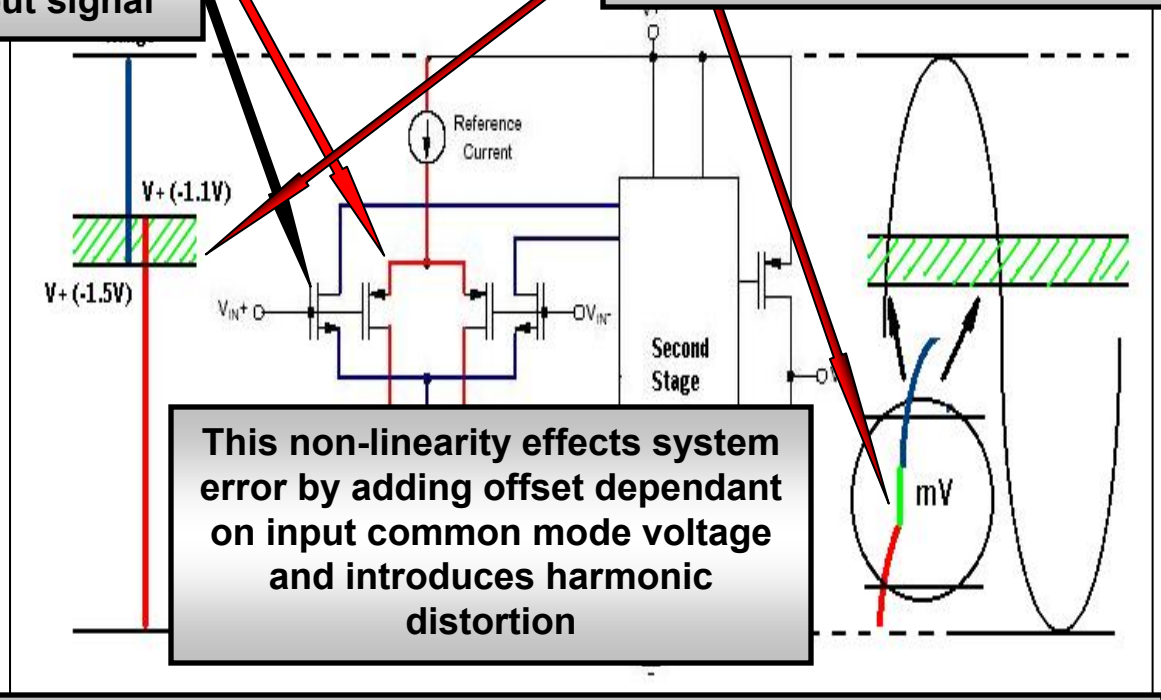
Offset voltage drift *range* [uV/degC]		
<0.1	1.0	**>1.0**



Typical Single Supply Rail-to-Rail Input Topology

Conventional Rail-to-Rail Input amplifiers require 2 input stages for positive and negative input signal

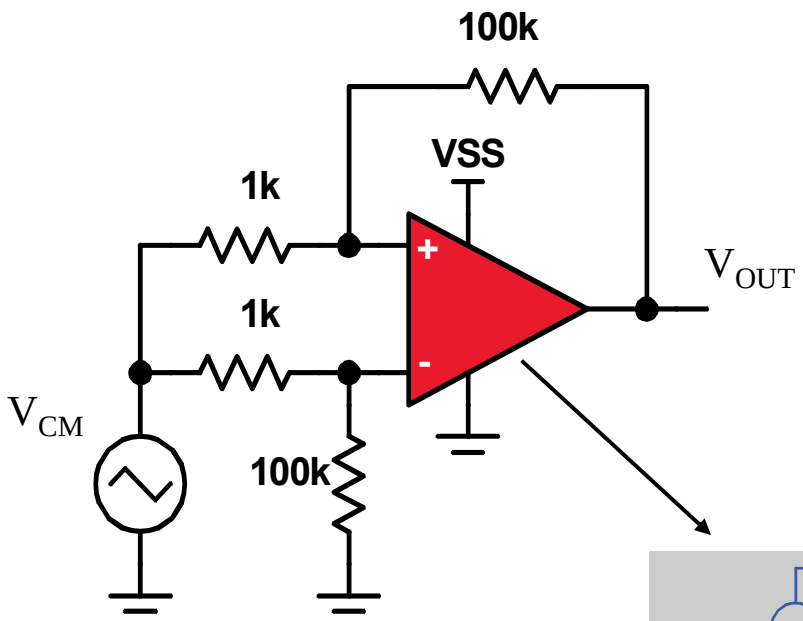
At the 'cross-over' region between these 2 stages, output linearity errors occur

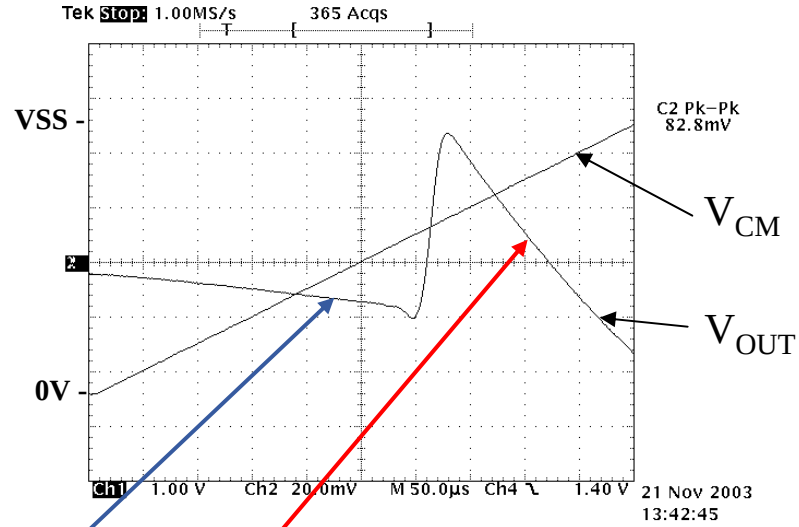


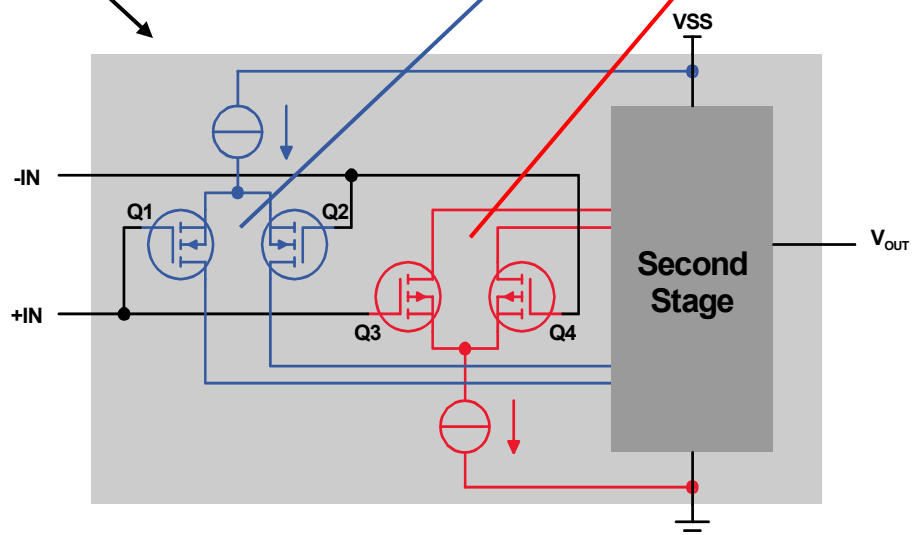
This non-linearity effects system error by adding offset dependant on input common mode voltage and introduces harmonic distortion

This input 'cross-over' distortion is present in all RRIO single supply operational amplifiers, except those with the unique 'Zero-Crossover Input Topology'

Input Stage Performance of Conventional RRIO



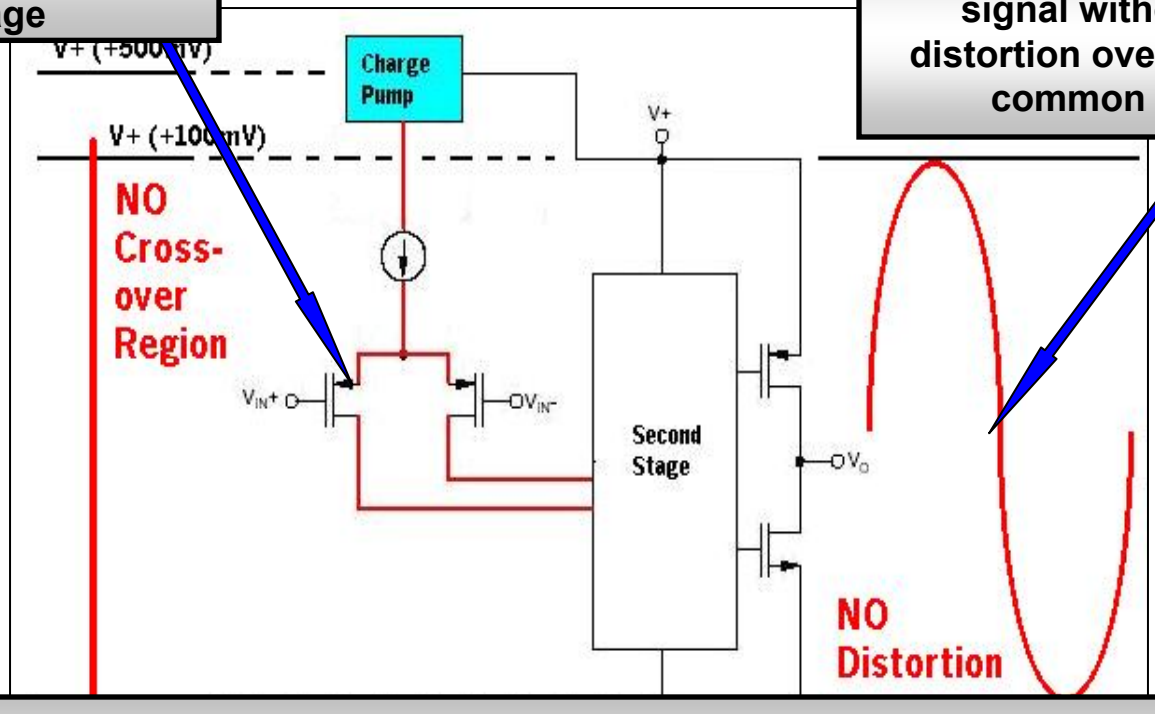




Zero Crossover Rail-to-Rail Input Topology

Zero Crossover Topology uses charge pump to achieve beyond the rail input swing with single input stage

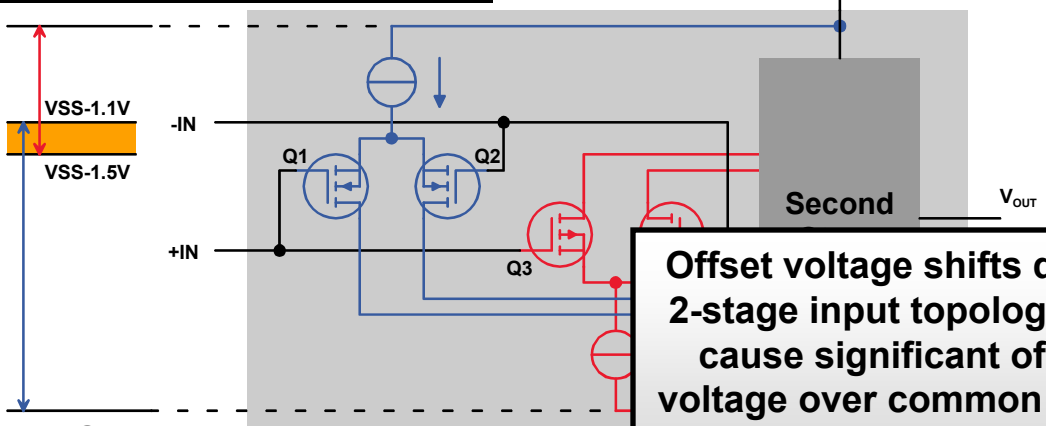
The result is a linear output signal without additional distortion over the entire input common mode range

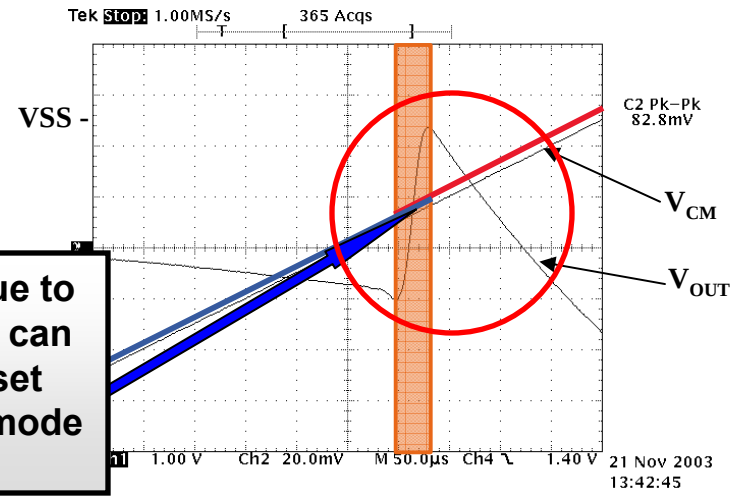


The OPA365 Zero-Cross-over input topology offers unparalleled THD and linear offset voltage to single supply applications

What are the benefits of the Zero-Crossover Input Stage?

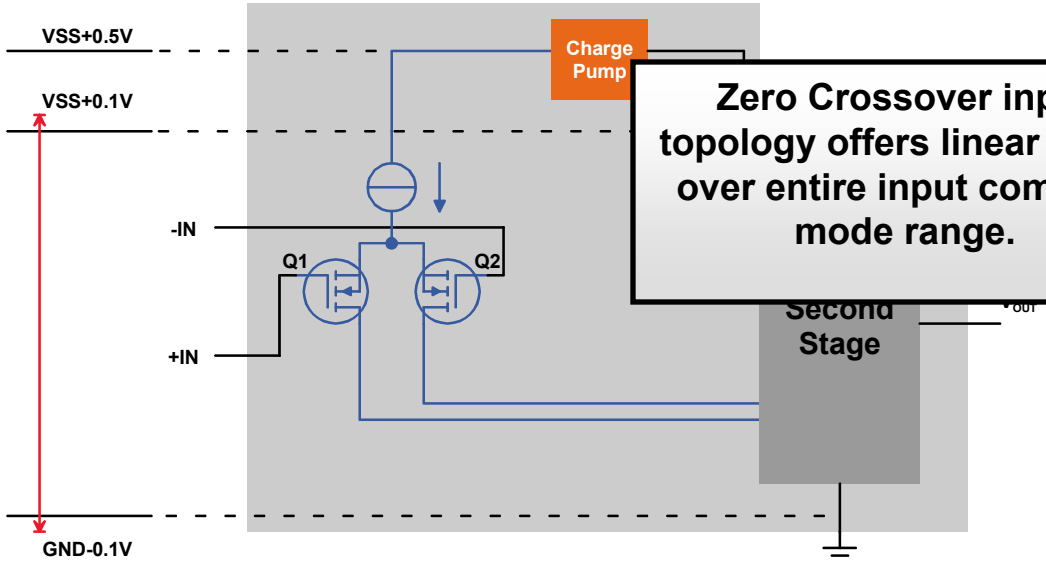
Standard Two-Stage Input

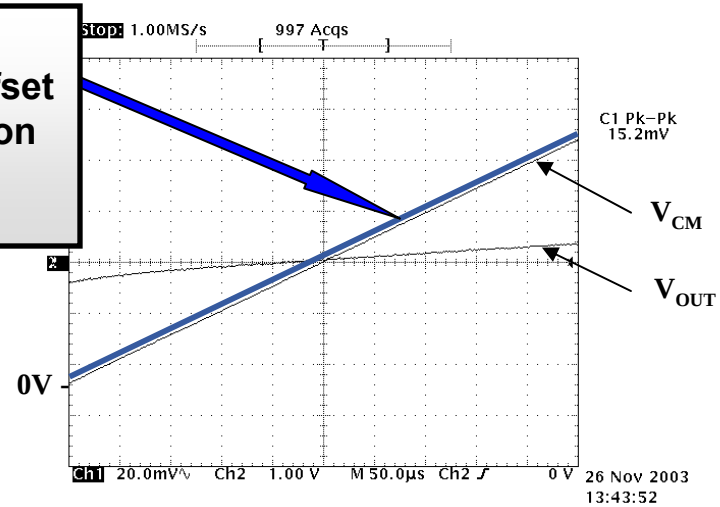




Offset voltage shifts due to 2-stage input topology can cause significant offset voltage over common mode

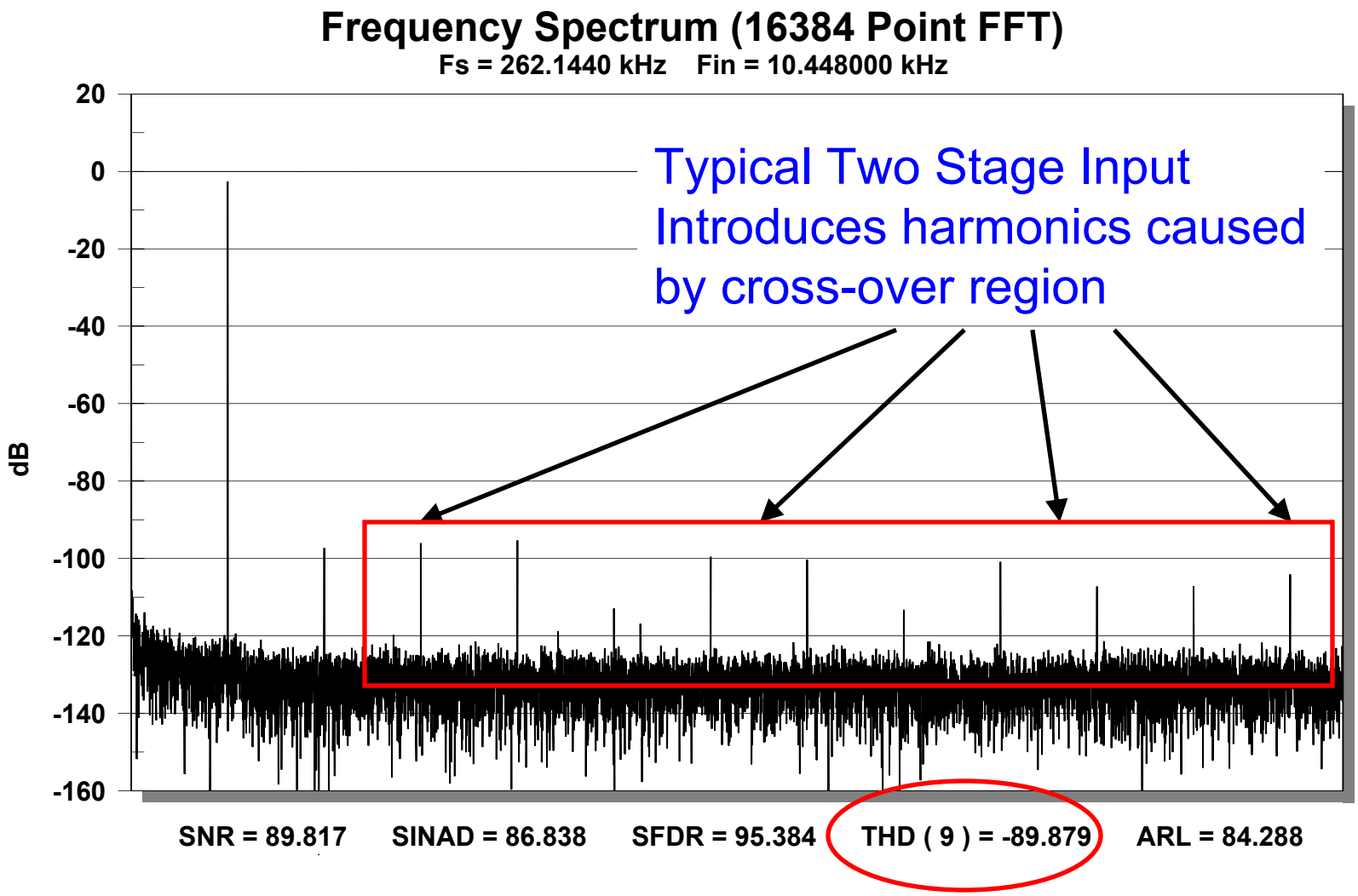
Zero-Crossover Input Stage



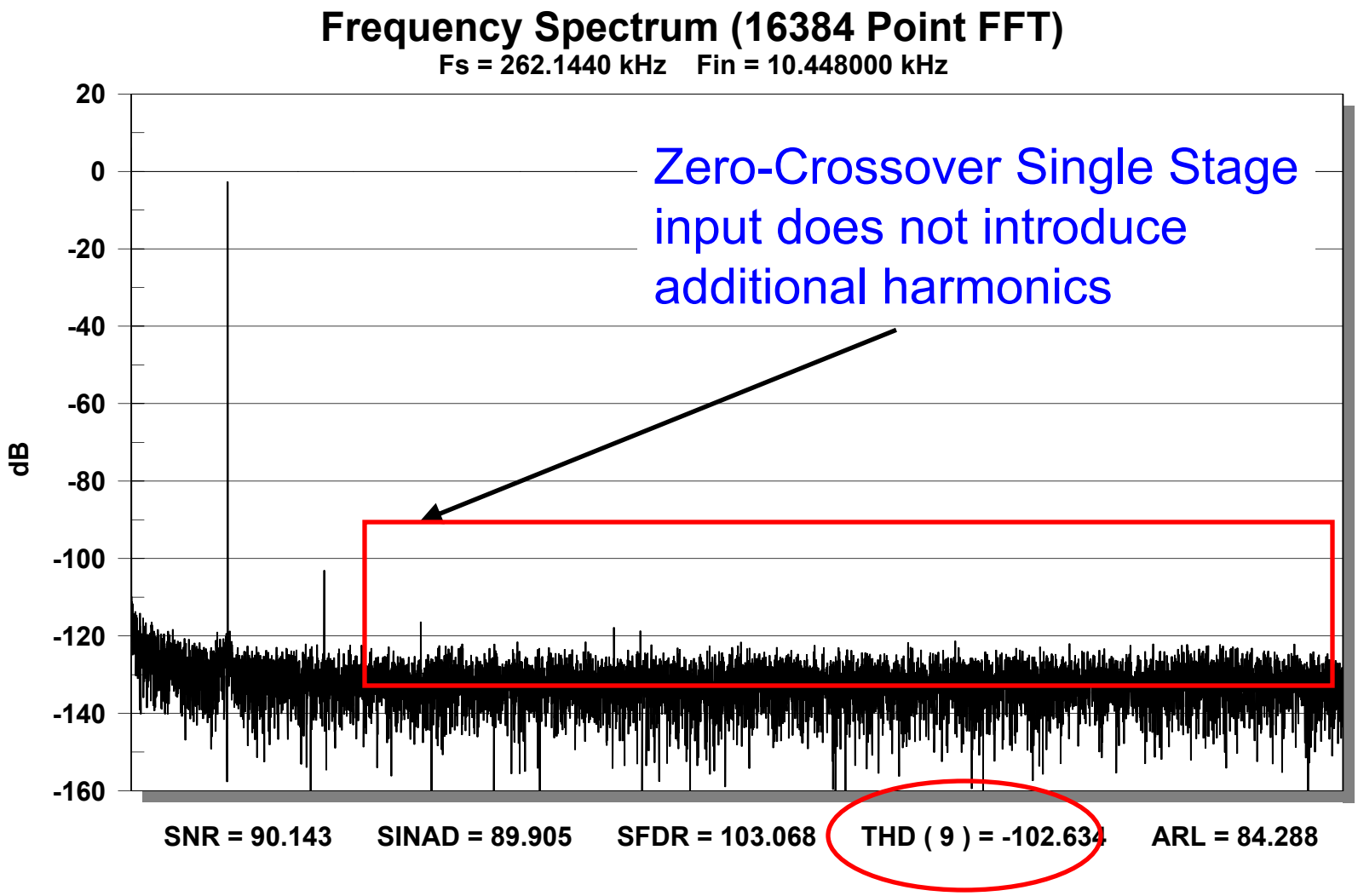


Zero Crossover input topology offers linear offset over entire input common mode range.

FFT of Typical 2-Stage Input Topology Harmonic Distortion

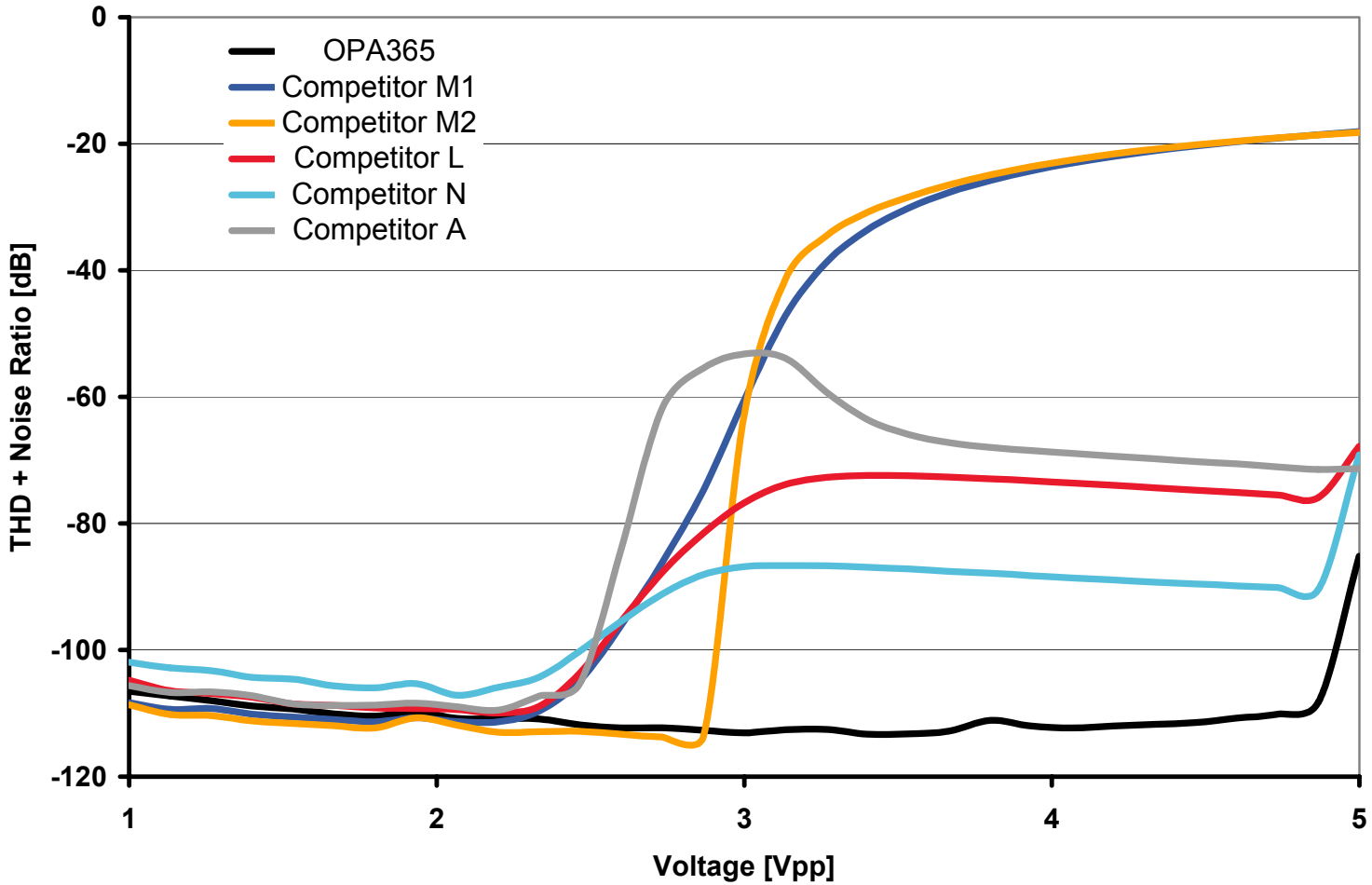


OPA365 Zero Crossover Input Harmonic Distortion

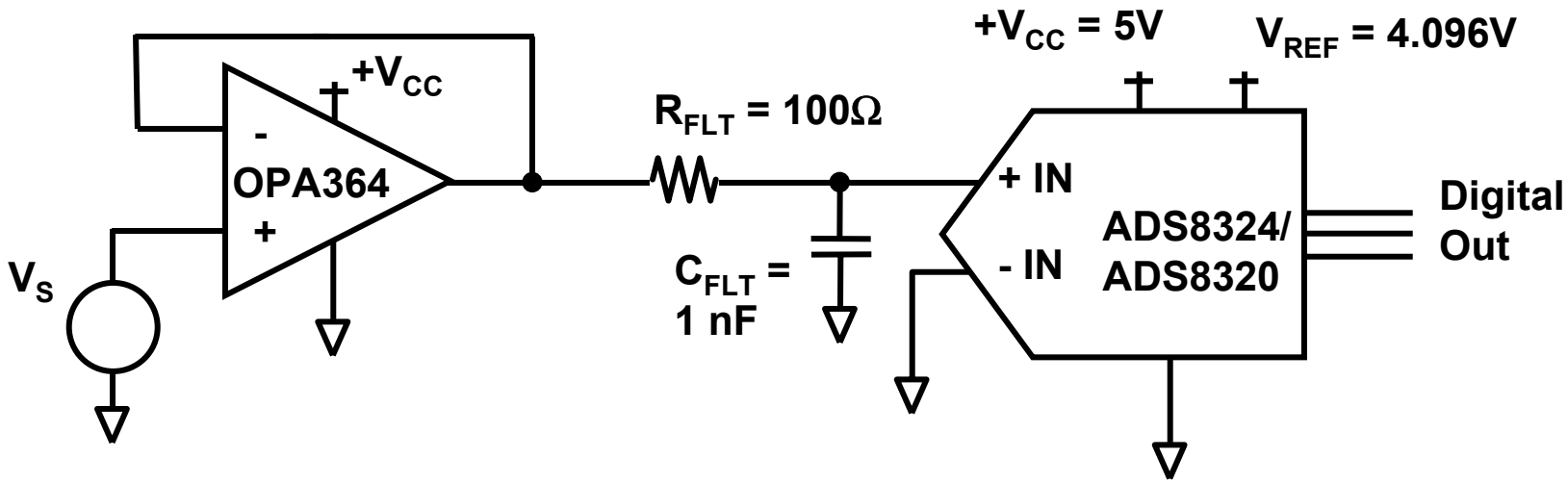


Competitive Comparison OPA365

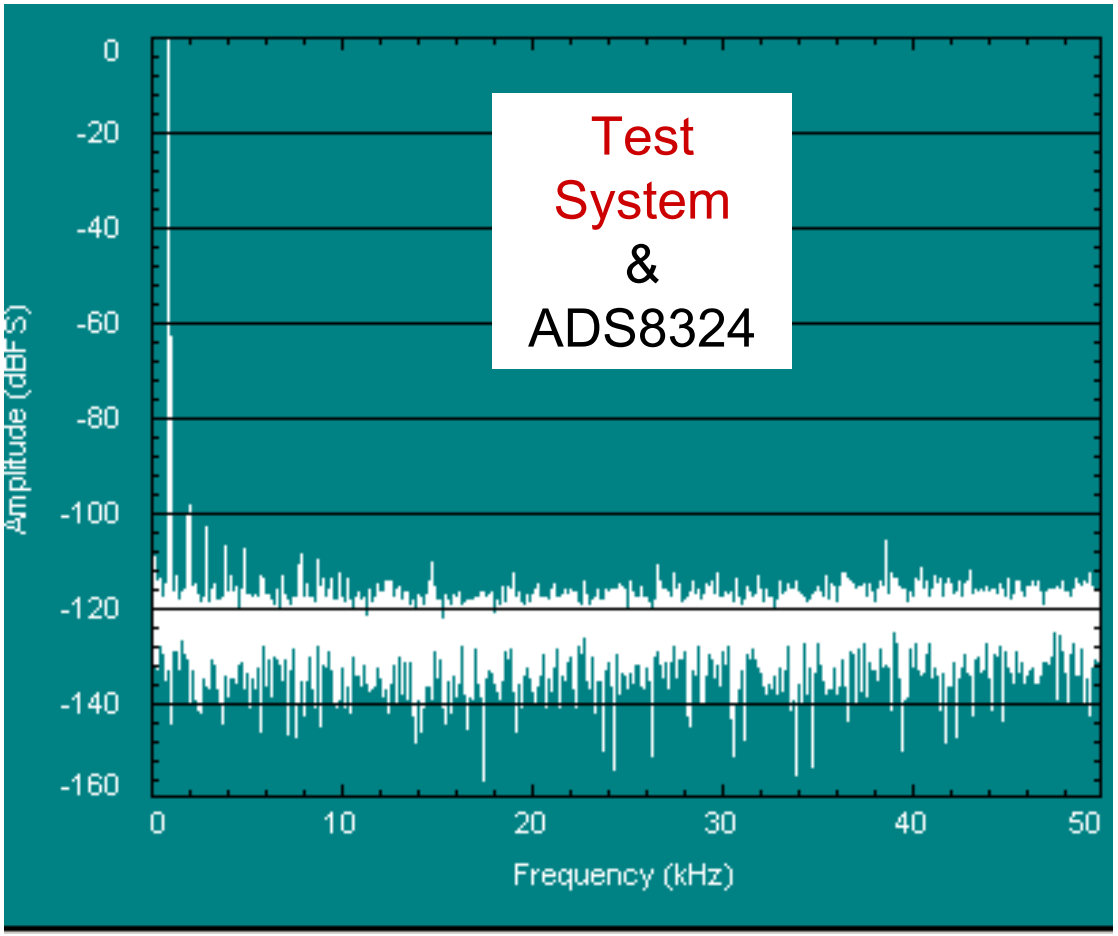
Gain +1, Supply 5V, Signal 10kHz @2.5V
Measuremnt bandwith 20Hz-30kHz

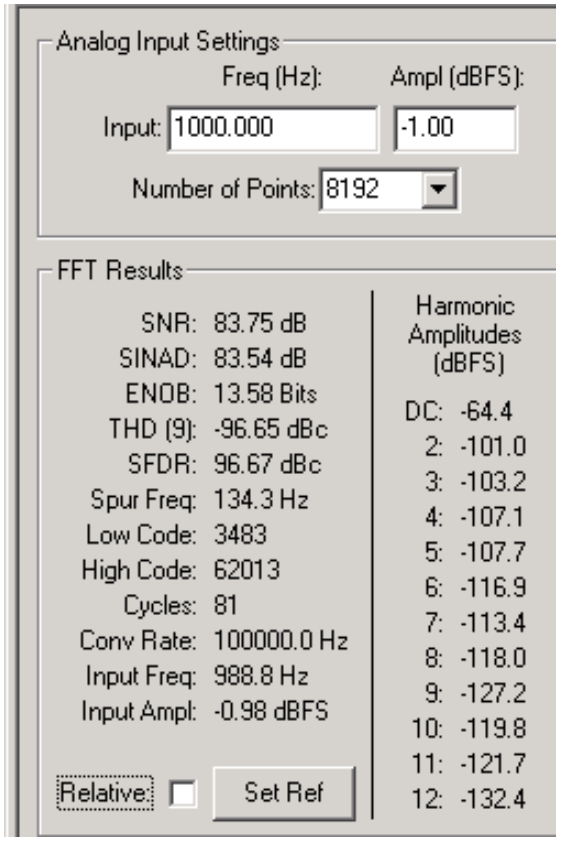


OPA-SAR Circuit Design



Signal Acquisition Results





Analog Input Settings

	Freq (Hz):	Ampl (dBFS):
Input:	1000.000	-1.00

Number of Points: 8192

FFT Results

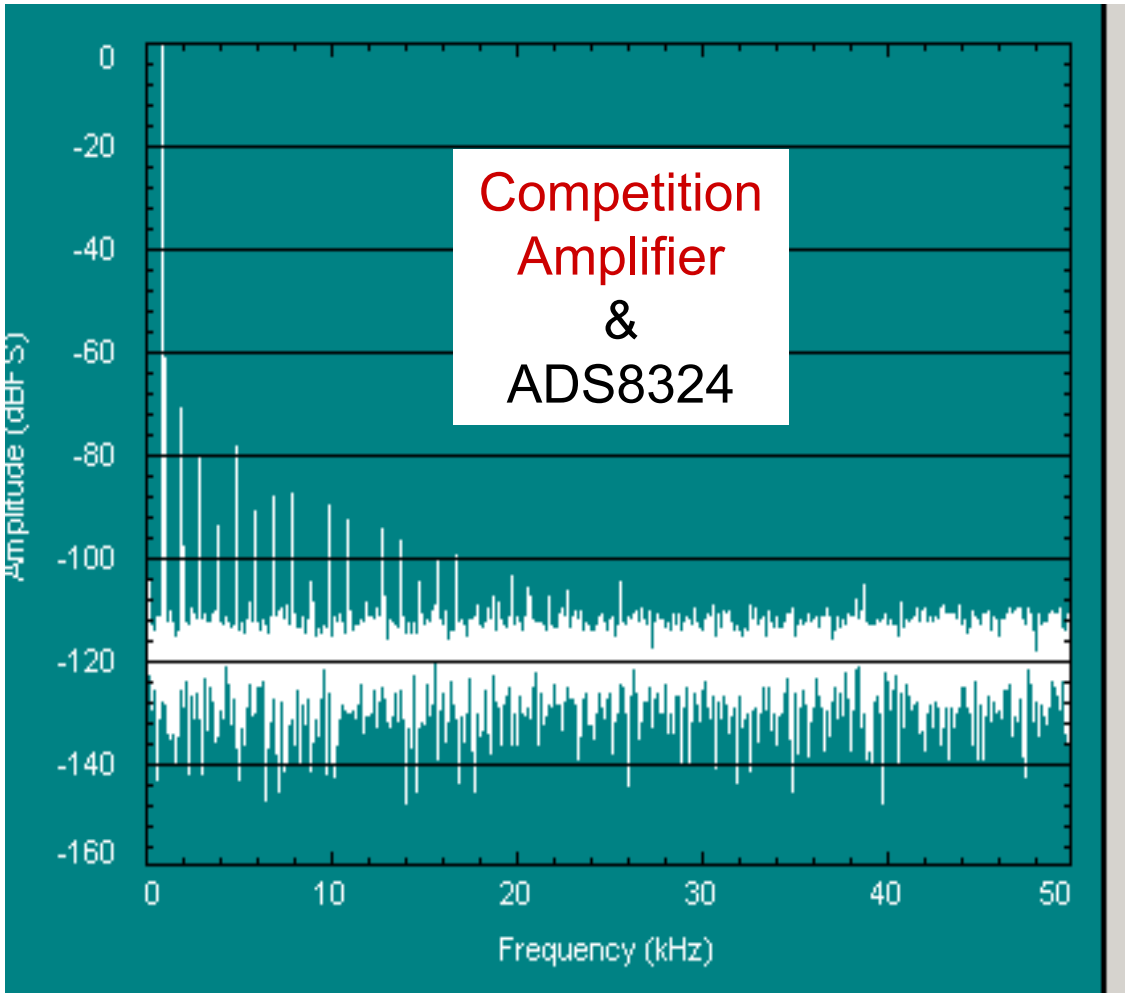
SNR:	83.75 dB
SINAD:	83.54 dB
ENOB:	13.58 Bits
THD (9):	-96.65 dBc
SFDR:	96.67 dBc
Spur Freq:	134.3 Hz
Low Code:	3483
High Code:	62013
Cycles:	81
Conv Rate:	100000.0 Hz
Input Freq:	988.8 Hz
Input Ampl:	-0.98 dBFS

Relative: Set Ref

Harmonic Amplitudes (dBFS)

DC:	-64.4
2:	-101.0
3:	-103.2
4:	-107.1
5:	-107.7
6:	-116.9
7:	-113.4
8:	-118.0
9:	-127.2
10:	-119.8
11:	-121.7
12:	-132.4

Signal Acquisition Results



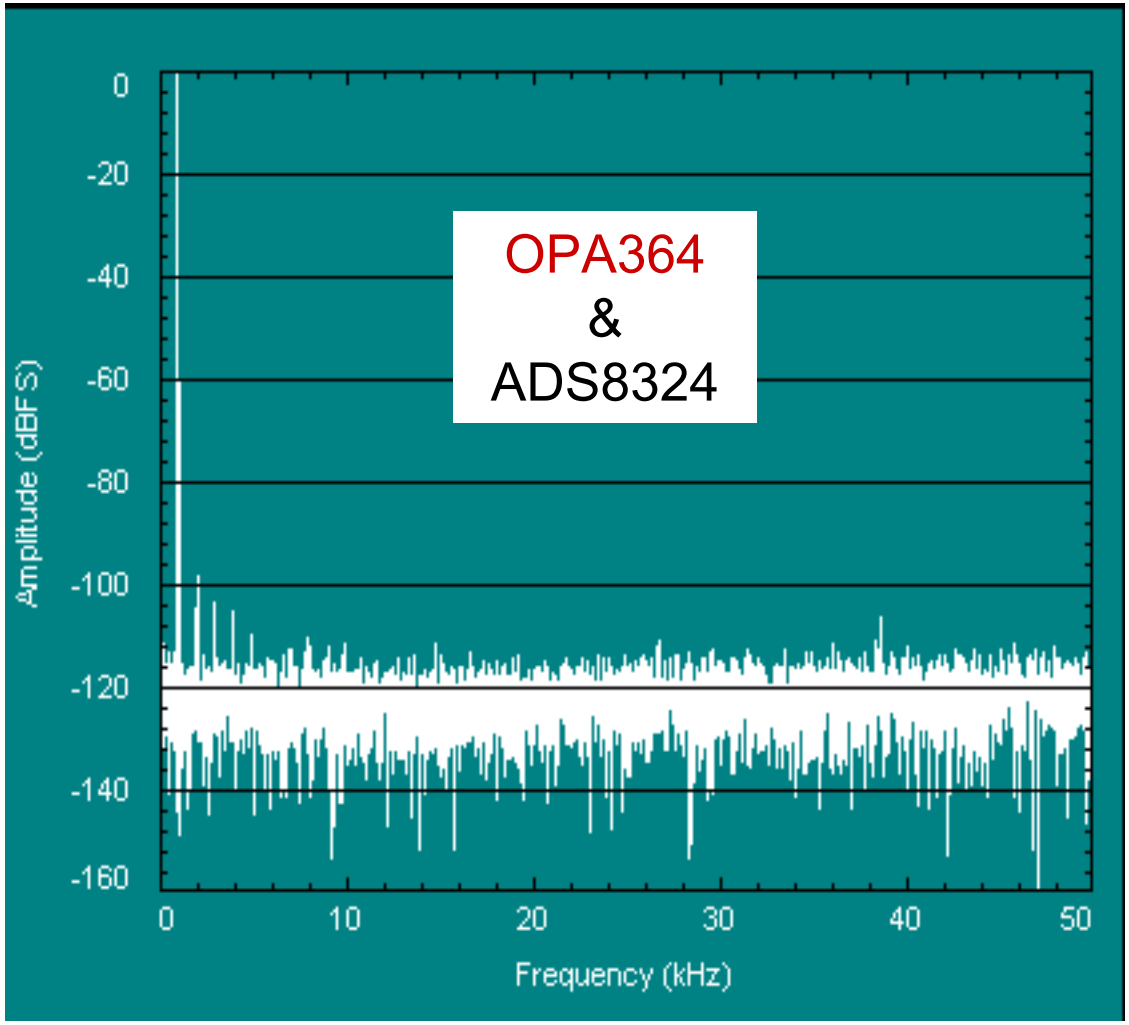
FFT Results

SNR:	79.06 dB
SINAD:	68.34 dB
ENOB:	11.06 Bits
THD (9):	-68.72 dBc
SFDR:	69.95 dBc
Spur Freq:	1977.5 Hz
Low Code:	3523
High Code:	62051
Cycles:	81
Conv Rate:	100000.0 Hz
Input Freq:	988.8 Hz
Input Ampl:	-0.98 dBFS

Relative: ☐ Set Ref

Harmonic Amplitudes (dBFS)	
DC:	-70.5
2:	-70.9
3:	-81.1
4:	-94.0
5:	-78.8
6:	-91.4
7:	-88.2
8:	-87.8
9:	-104.7
10:	-90.1
11:	-92.8
12:	-109.0

Signal Acquisition Results



FFT Results

SNR:	83.18 dB
SINAD:	83.04 dB
ENOB:	13.50 Bits
THD (9):	-97.93 dBc
SFDR:	96.37 dBc
Spur Freq:	134.3 Hz
Low Code:	3482
High Code:	62002
Cycles:	81
Conv Rate:	100000.0 Hz
Input Freq:	988.8 Hz
Input Ampl:	-0.98 dBFS

Relative: Set Ref

Harmonic Amplitudes (dBFS)

DC:	-62.0
2:	-104.7
3:	-104.0
4:	-105.2
5:	-110.0
6:	-115.4
7:	-112.6
8:	-117.8
9:	-114.9
10:	-121.4
11:	-124.2
12:	-121.3

Comparison of Tests (14-bit ADC) @ 1kHz Fin

	Test System & ADS8324	Competition Amplifier & ADS8324	OPA364 & ADS8324
FFT Results		FFT Resu	FFT Results
SNR:	83.75 dB	79.06 dB	83.18 dB
SINAD:	83.54 dB	68.34 dB	83.04 dB
ENOB:	13.58 Bits	11.06 Bits	13.50 Bits
THD (9):	-96.65 dBc	-68.72 dBc	-97.93 dBc
SFDR:	96.67 dBc	69.95 dBc	96.37 dBc
Spur Freq:	134.3 Hz	1977.5 Hz	134.3 Hz
Low Code:	3483	3523	3482
High Code:	62013	62051	62002
Cycles:	81	81	81
Conv Rate:	100000.0 Hz	100000.0 Hz	100000.0 Hz
Input Freq:	988.8 Hz	988.8 Hz	988.8 Hz
Input Ampl:	-0.98 dBFS	-0.98 dBFS	-0.98 dBFS

Comparison of Tests (16-bit ADC)

ADS8320 Only

Lynium ATS4000 Test S

File Edit Panel Help

Analog Input Settings

Freq (Hz):

Input: 1000.000

FFT Results

SNR: 88.16 dB
SINAD: 87.53 dB
ENOB: 14.25 Bits
THD (9): -96.15 dBc
SFDR: 96.97 dBc
Spur Freq: 134.3 Hz
Low Code: 740
High Code: 64591
Cycles: 81
Conv Rate: 100000.0 Hz
Input Freq: 988.8 Hz
Input Ampl: -0.23 dBFS

Relative: Set Ref

Save to File

Working Directory:

C:\ATS4000_temp

Part Information:

ADS8320

Information for Most Recent

15:27:04 9/27/2002 Part: +V
100000.000Hz, clks per con

OPA364, Filter, ADS8320

Lynium ATS4000 Test System

File Edit Panel Help

SETUP DUT SETUP AC SETUP DC DEBUG

Analog Input Settings

Freq (Hz): Ampl (dBFS):

Input: 1000.000 -0.25

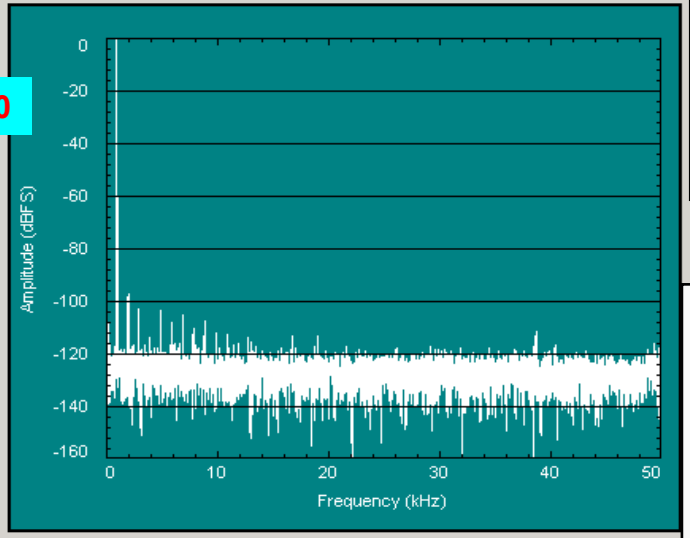
FFT Results

SNR: 87.78 dB
SINAD: 87.02 dB
ENOB: 14.16 Bits
THD (9): -94.90 dBc
SFDR: 97.13 dBc
Spur Freq: 2111.8 Hz
Low Code: 846
High Code: 64682
Cycles: 81
Conv Rate: 100000.0 Hz
Input Freq: 988.8 Hz
Input Ampl: -0.23 dBFS

Relative: Set Ref

Harmonic Amplitudes (dBFS)

DC: -77.2
2: -98.6
3: -103.0
4: -114.2
5: -103.7
6: -108.0
7: -105.3
8: -111.2
9: -107.6
10: -116.7
11: -112.7
12: -116.5



Save to File

Working Directory: C:\ATS4000_temp

Full File Name: OPA2364 @ 5V @ 1kHZ.fft

Browse...

Part Information: ADS8320

Header
Bin Amplitude
Bin # & Freq.
ADC Results
Comma Sep.
Tab Separated

Save
Append

Information for Most Recent Test Results

13:32:03 9/27/2002 Part: +VCC: 4.999629V, 0.980mA uncal, VREF: 4.999938V, 0.872mA uncal, CM: GND, extra S/H: 0, SPI Mode: disabled, TSUCS: 1/2 clk, conv rate: 100000.000Hz, clks per conv: 24. AC Test: run once, soak: 1 sec. System #2, test head: MCP3201.

Run
Continuous
Stop

ADS8320:

SNR = 88dB
ENOB = 14.33

Op Amp+ Filter+ ADS8320:

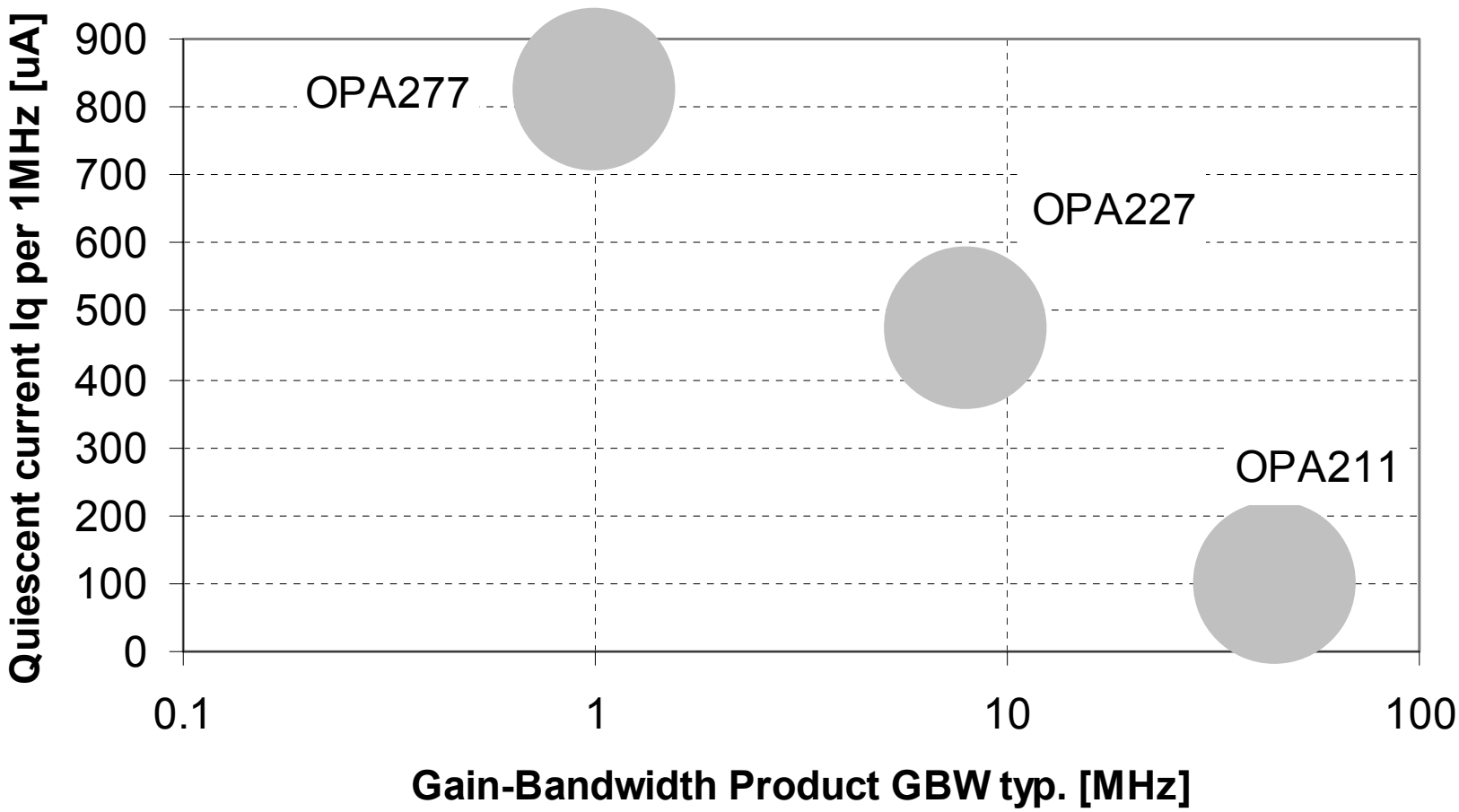
SNR = 87.78dB
ENOB = 14.19

Bipolar amplifiers

Bias current Ib *range* [pA]		
10	100	**1000**

Voltage noise Vn at 1kHz *range* [nV/rtHz]		
<10	25	>50

Offset voltage drift *range* [uV/degC]		
<0.1	**1.0**	>1.0

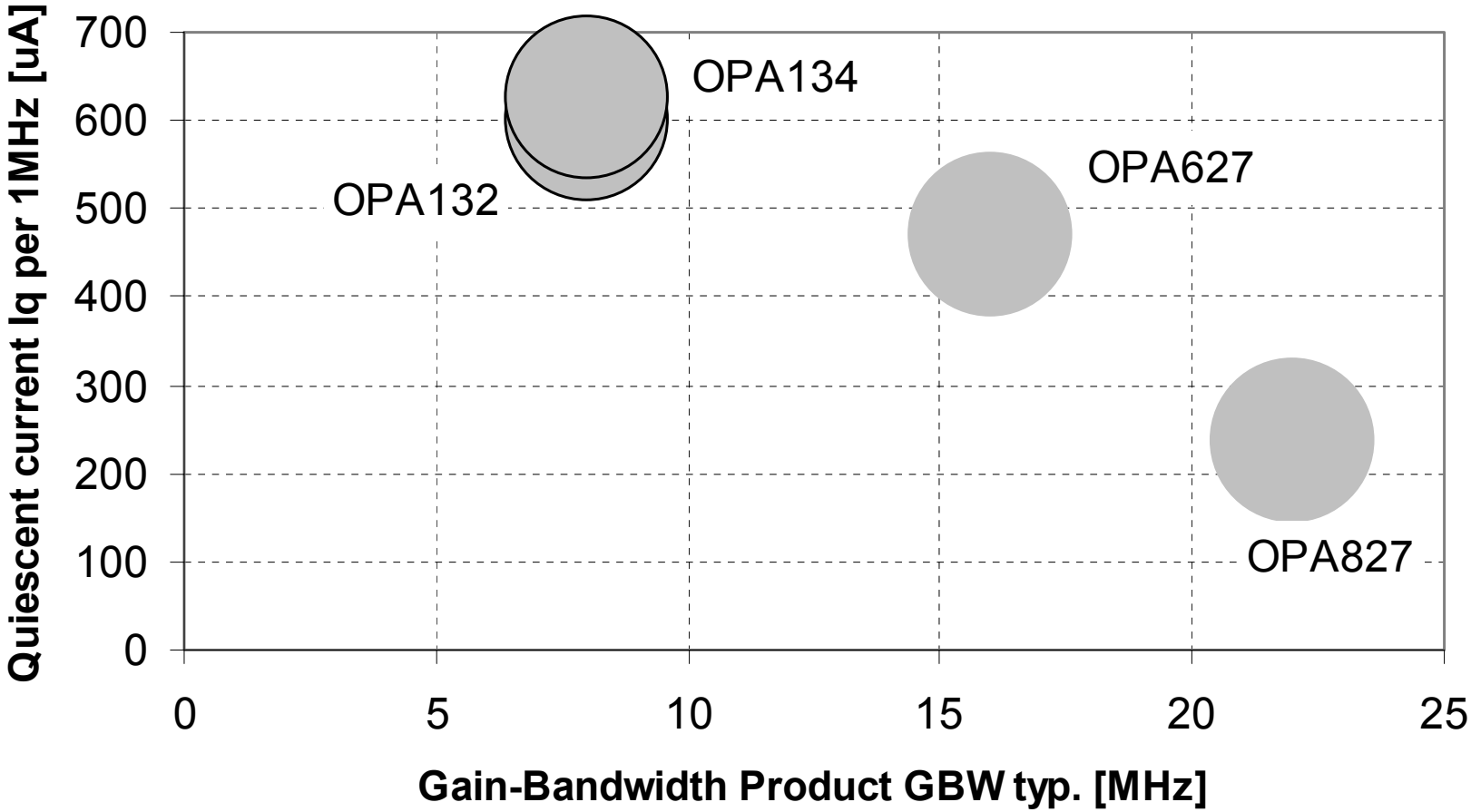


J-FET amplifiers

Bias current Ib *range* [pA]		
10	100	1000

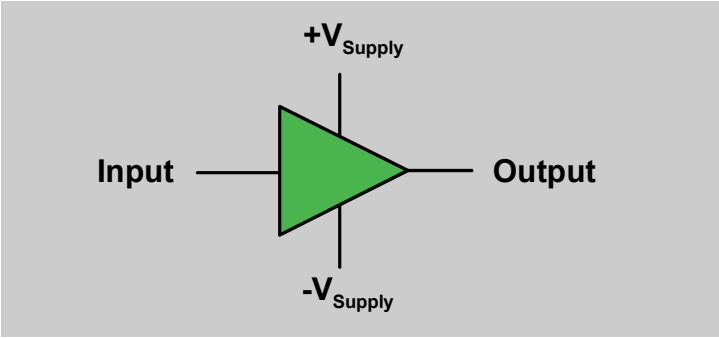
Voltage noise Vn at 1kHz *range* [nV/rtHz]		
<10	25	>50

Offset voltage drift *range* [uV/degC]		
<0.1	1.0	>1.0

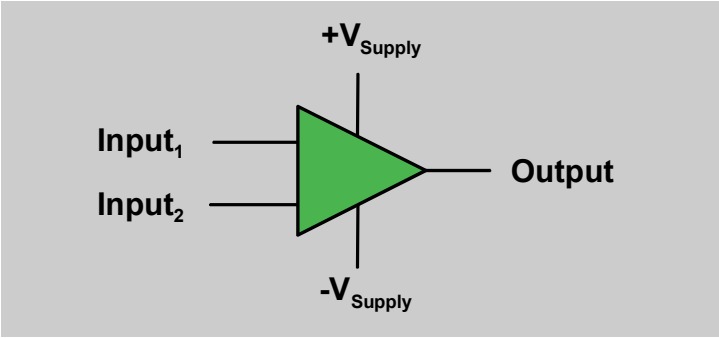


Op Amps vs. INA's

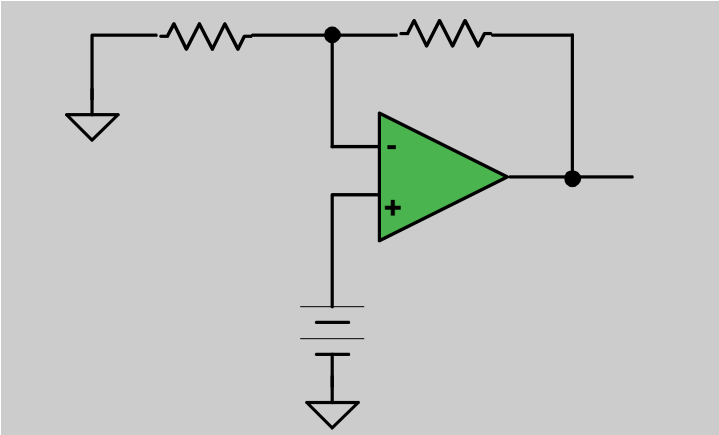
Single Ended Amplifier



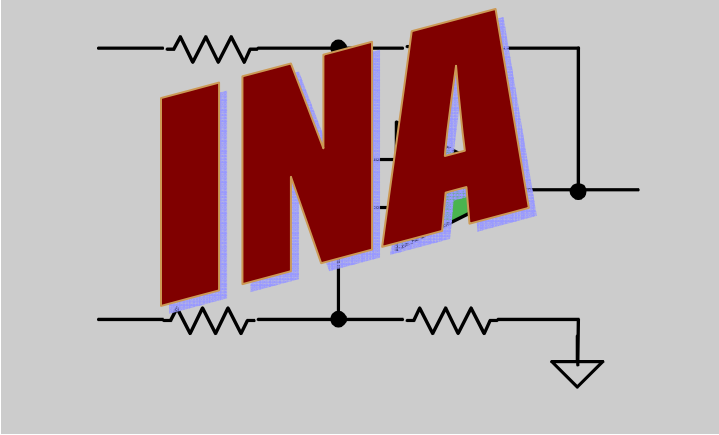
Differential Amplifier



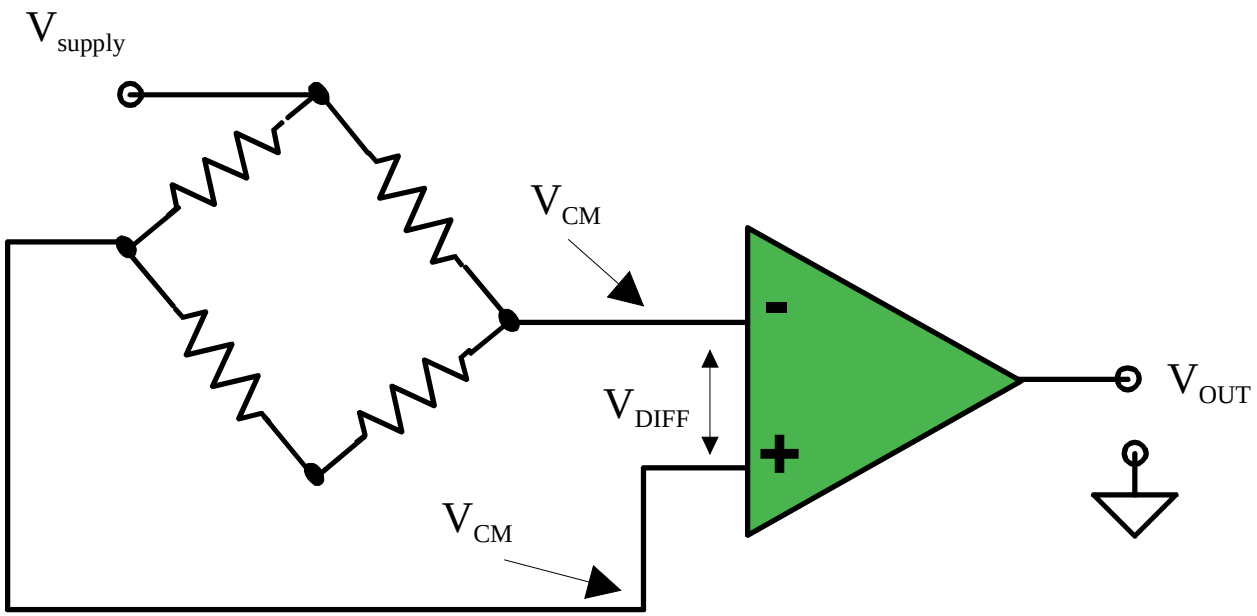
Single Ended Amplifier w/ Feedback



Differential Amp w/ resistor network



Op Amps vs. INA's



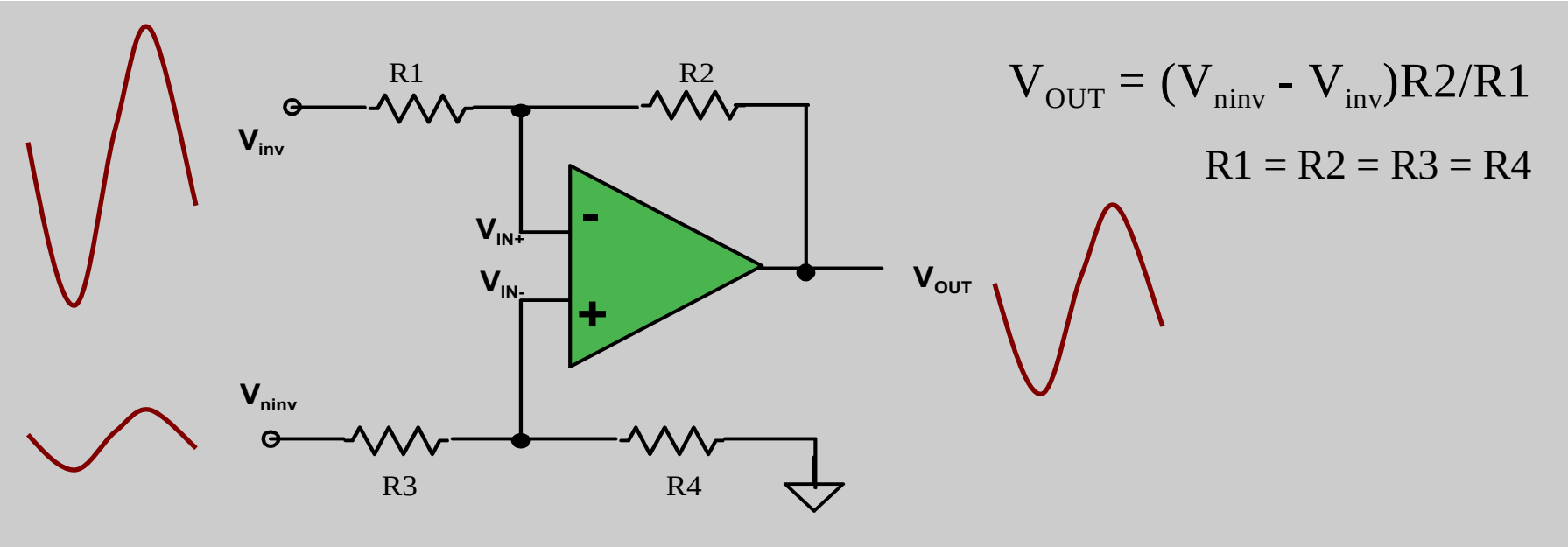
INA Output

$$V_{OUT} = (V_{inv} - V_{ninv})\ Gain$$

OPA Output

$$V_{OUT} = V_{in} * Gain + V_{CM} * Gain$$

Difference Amplifiers



$$V_{OUT} = (V_{ninv} - V_{inv})R2/R1$$

$$R1 = R2 = R3 = R4$$

$$CMRR = 20 * \log(x)$$

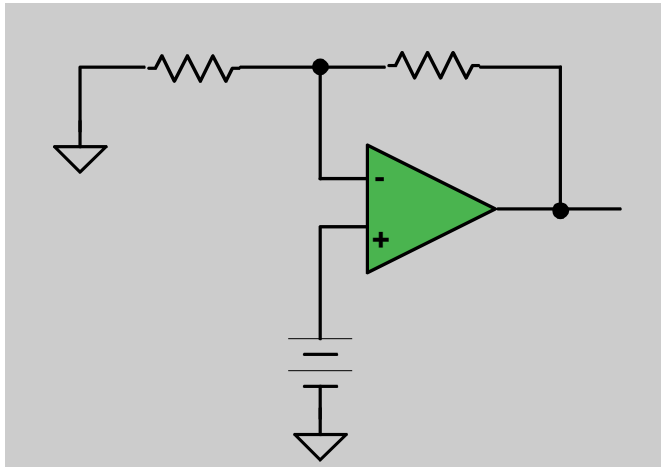
$$x = R4/(R3 + R4) * (R1 + R2)/R1 - R2/R1$$

- ►1% Discrete = 40dB
- ►0.1% Discrete = 60dB
- ►Silicon Ratio Match = 100dB

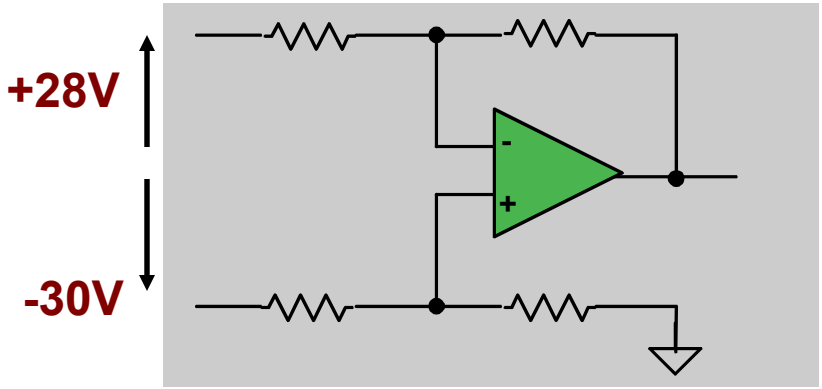
Difference Amplifiers

Strength: Common-Mode Voltage Range

CMV Range of Op Amp (V)	
Min	$(V_{S-}) + 2$
Max	$(V_{S+}) - 2$



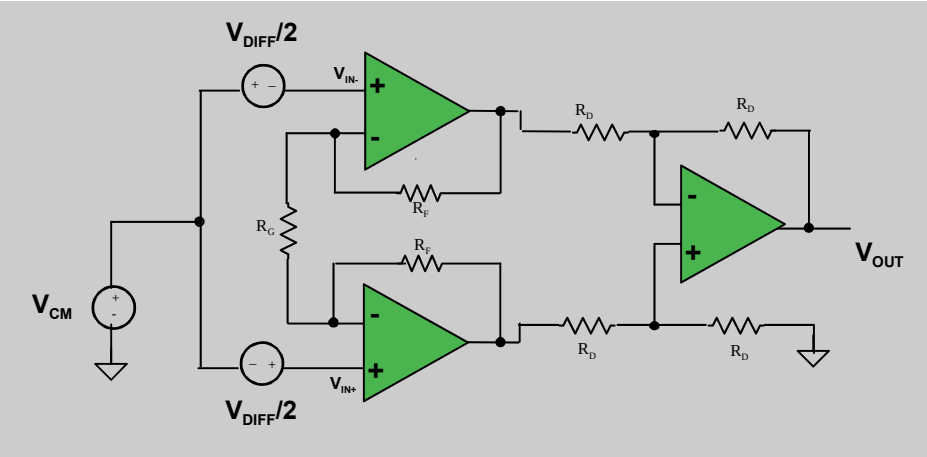
CMV Range of Diff Amp (V)	
Min	$2(V_{S-})$
Max	$2(V_{S+}) - 2$

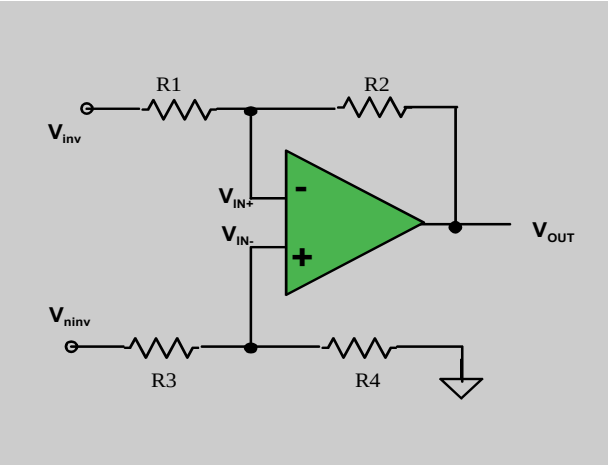


Limitation: Low input resistance, low fixed gains

3 Stage INA

Strength: High Input Impedance, wide gain range



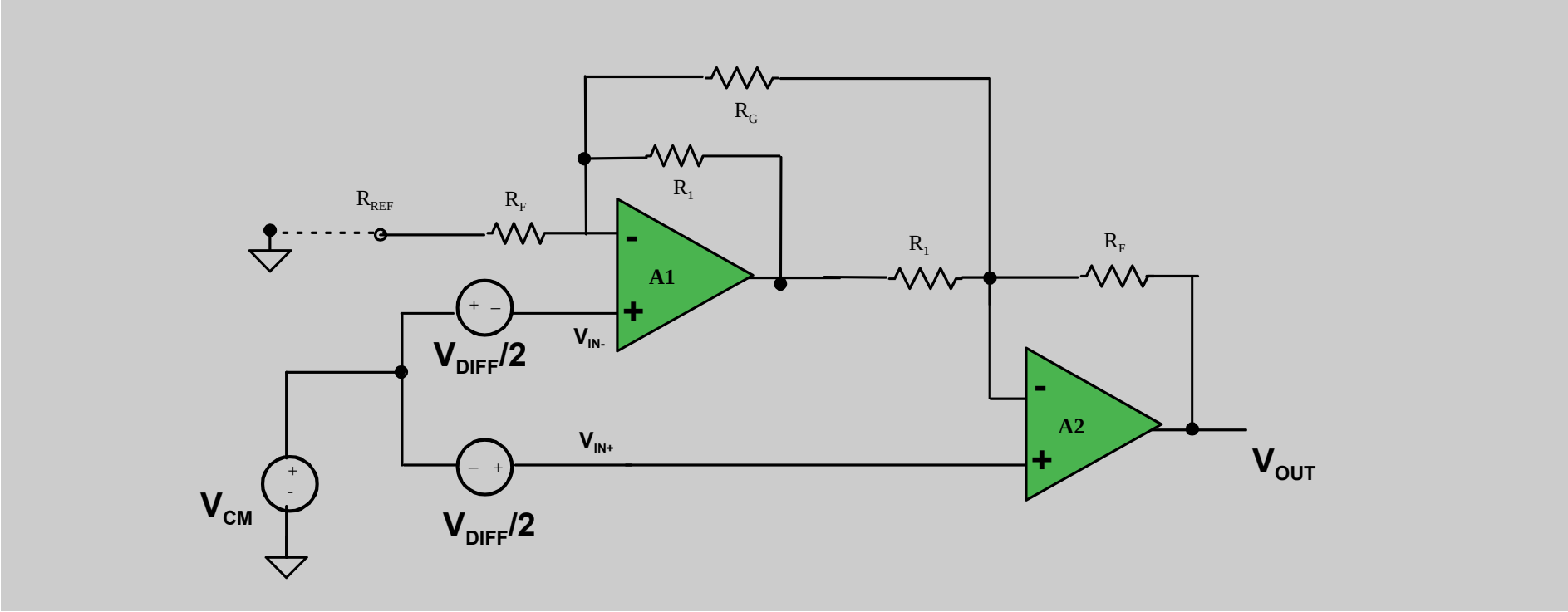


Limitation: common-mode voltage range

Limitation: increases: size, cost, power consumption

2 Stage INA

Strength: lower cost, size, power vs. 3 stage INA



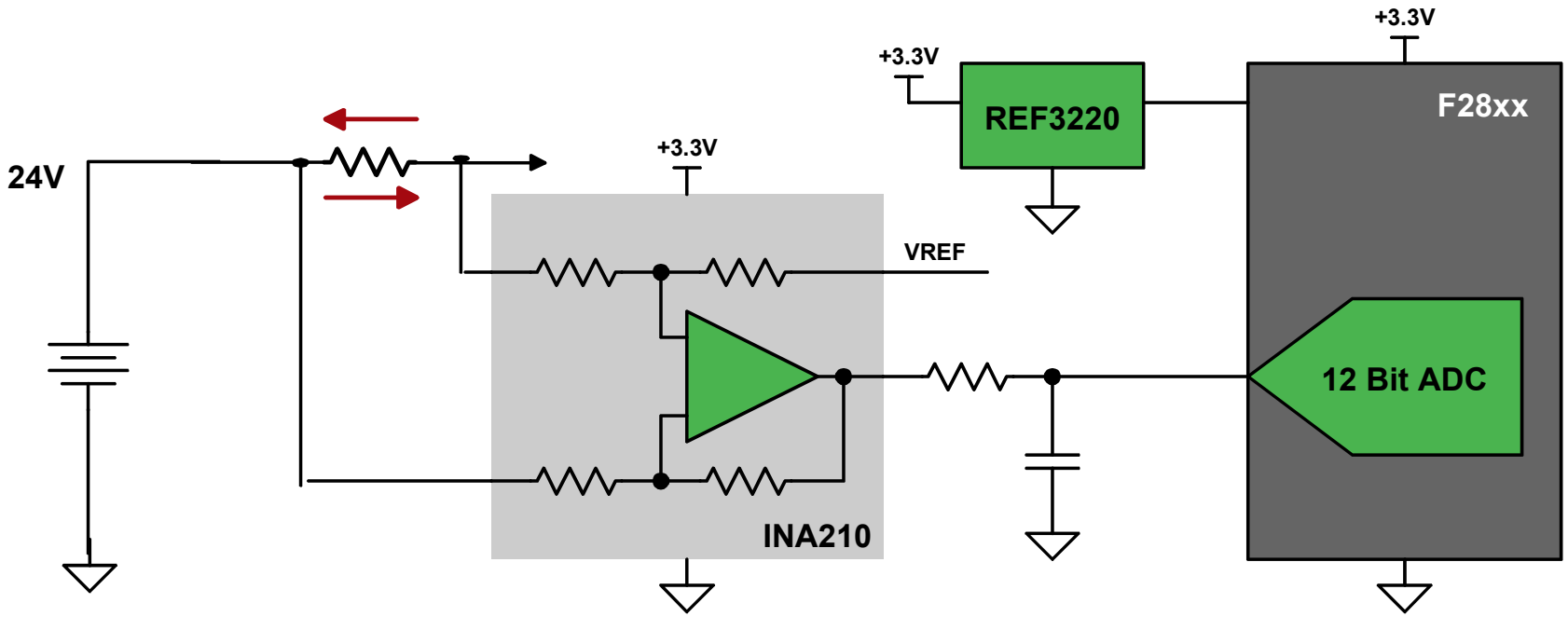
Limitation: common-mode voltage range

Limitation: Lower CMRR at high frequency

Limitation: minimum gain of 2V/V (sometimes 5V/V)

Current Shunt Monitors

Strength: Common-mode range not related to supply voltage



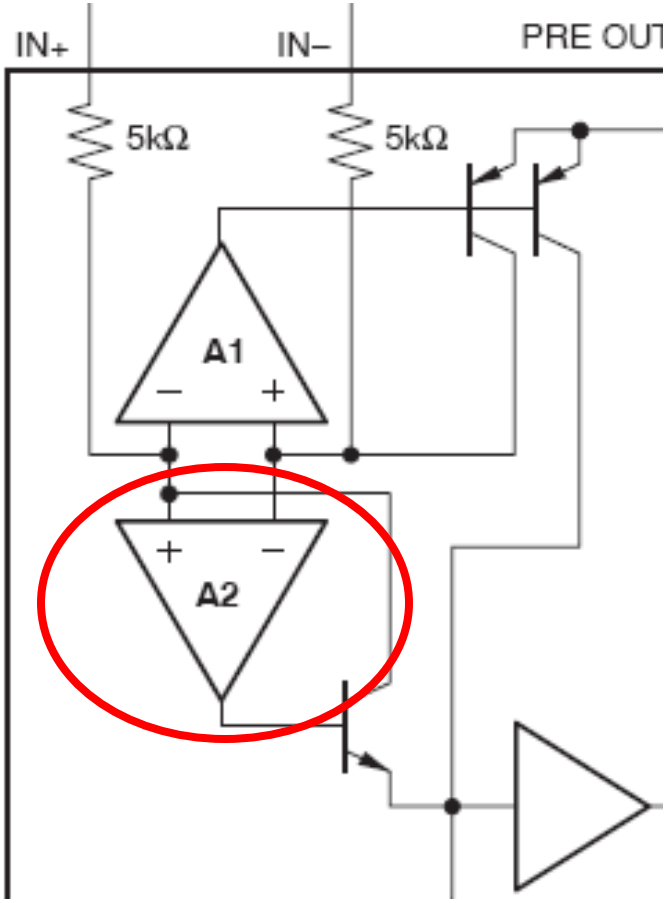
Limitation: Different ranges of operation performance

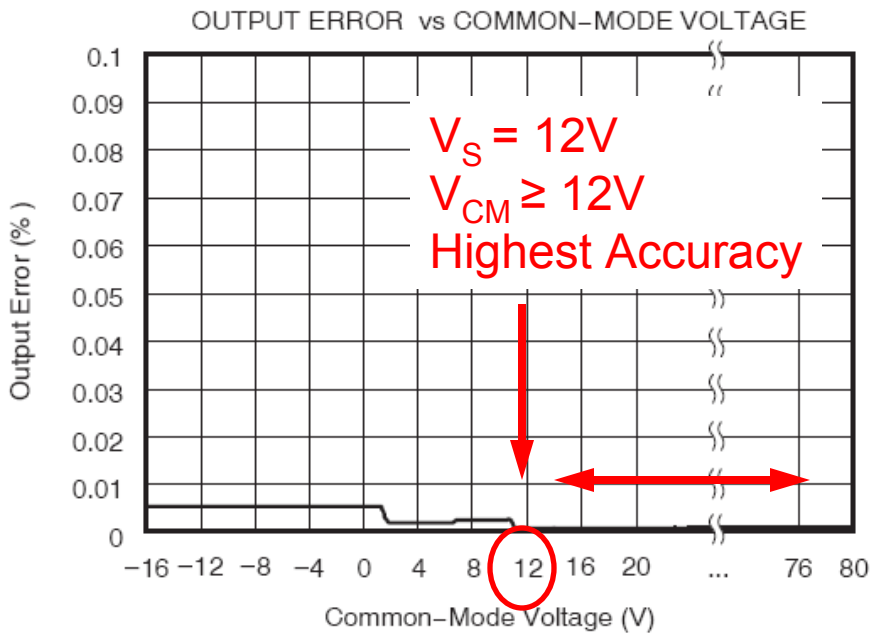
Limitation: Few uses outside current measurement

Accuracy – Normal Case 1: $V_{SENSE} \geq 20mV$, $V_{CM} \geq V_S$

$$V_{SENSE} = (V_{IN}+) - (V_{IN}-)$$

$$V_{CM} = \frac{(V_{IN}+) + (V_{IN}-)}{2}$$

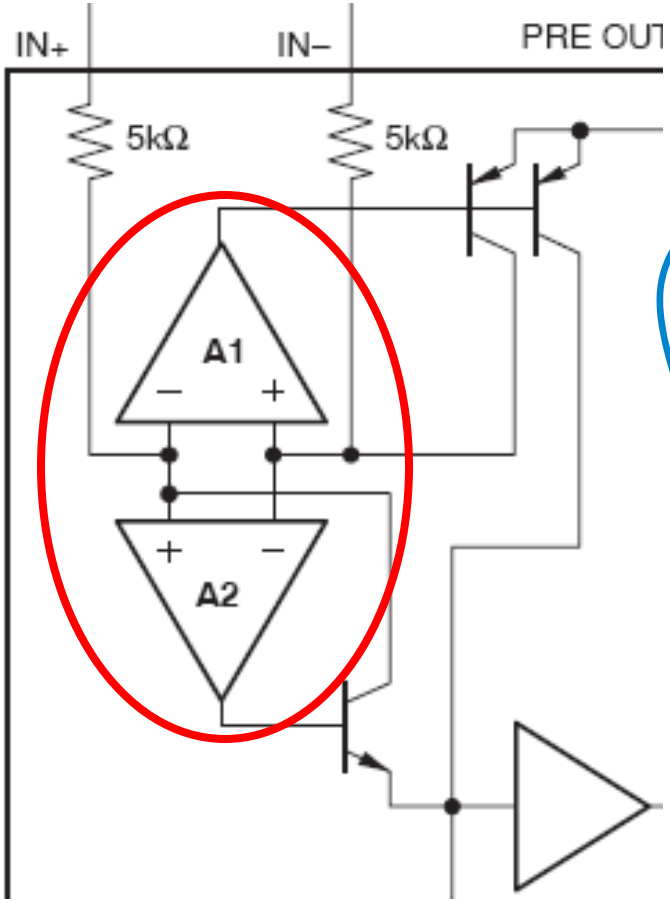


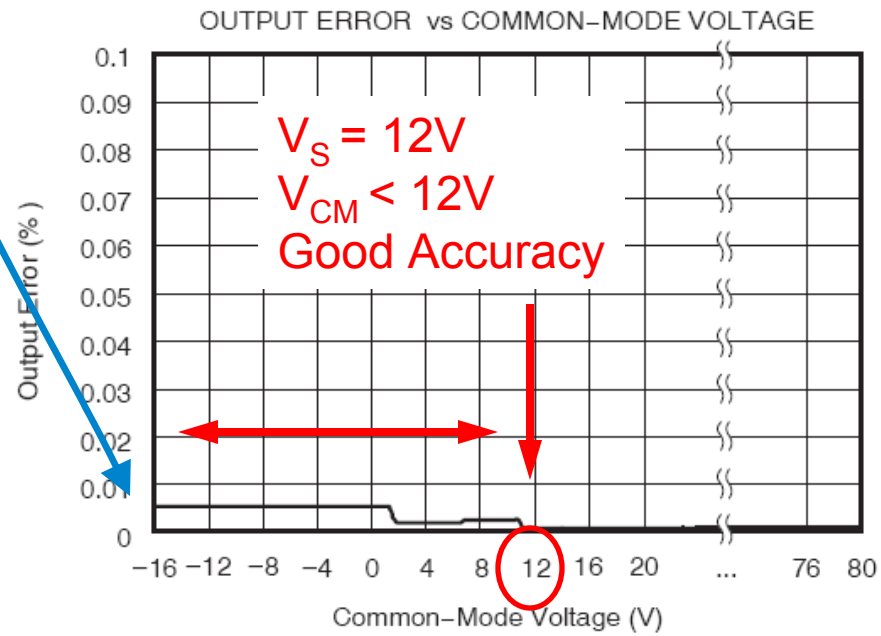


Accuracy – Normal Case 2: $V_{SENSE} \geq 20mV$, $V_{CM} < V_S$

$$error \leq 0.005\%$$

$$V_{CM} = -16V$$

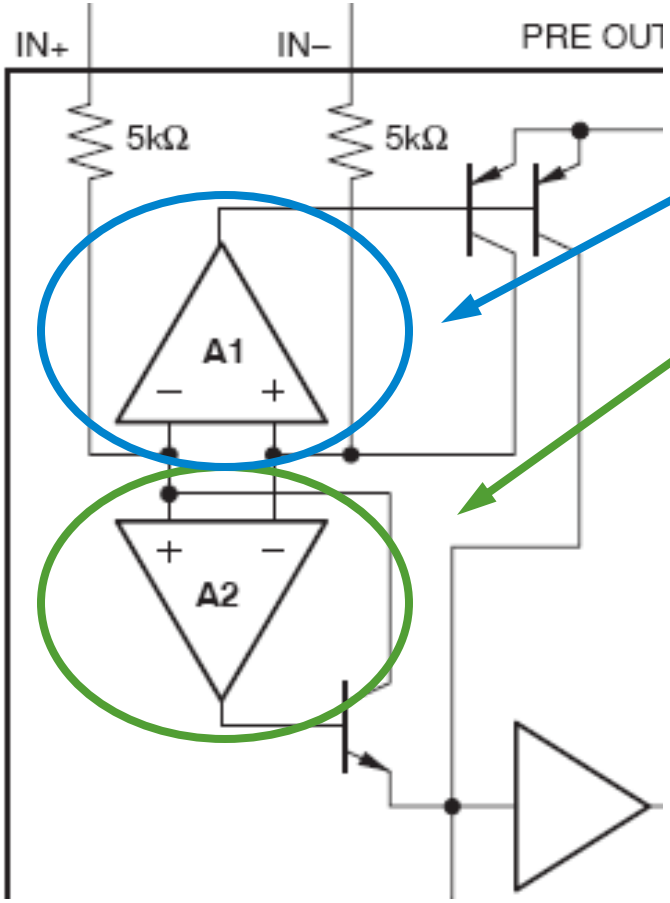


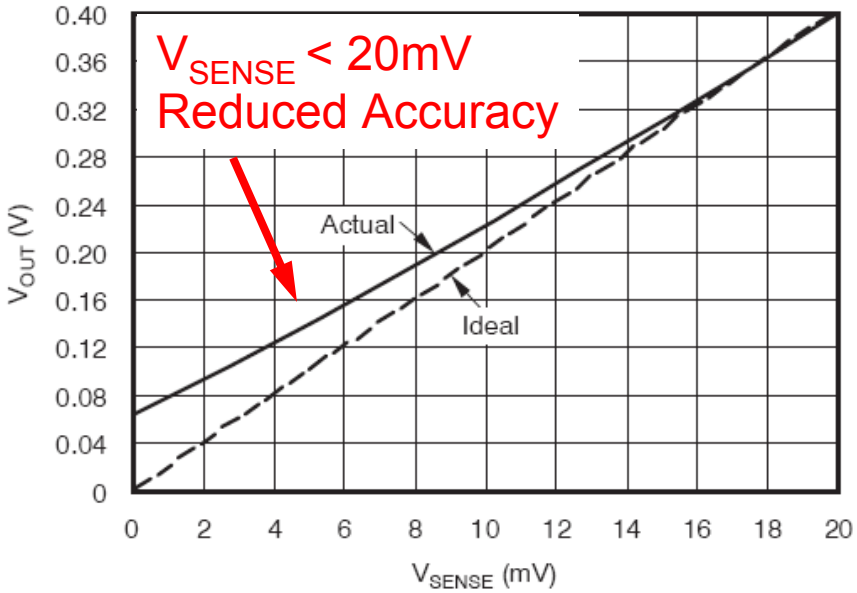


Accuracy – V_{SENSE} < 20mV: V_{CM} < 0V and V_{CM} > V_S

$$-16V \le V_{CM} < 0V$$

$$V_S < V_{CM} \le 80V$$

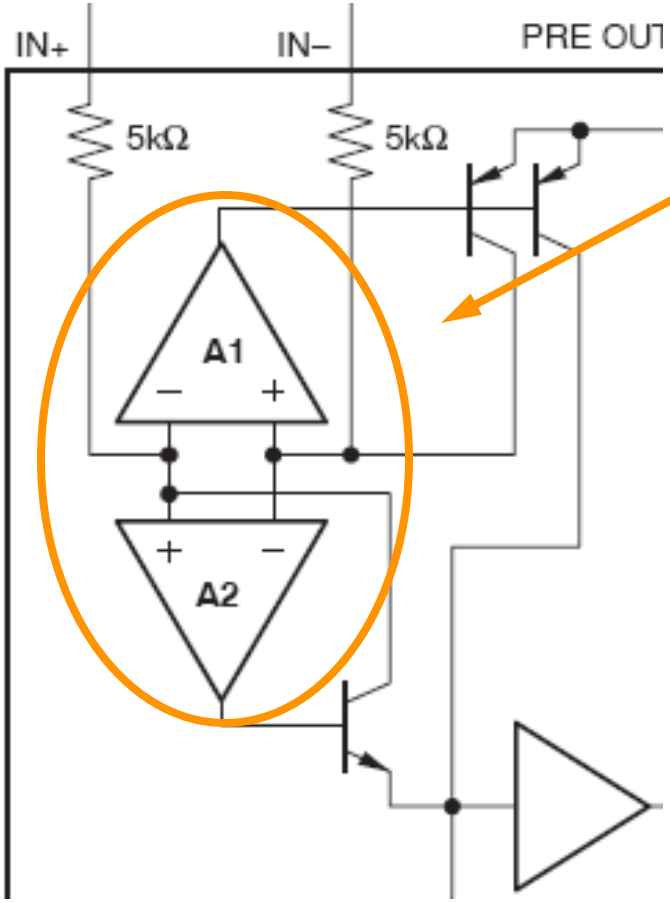




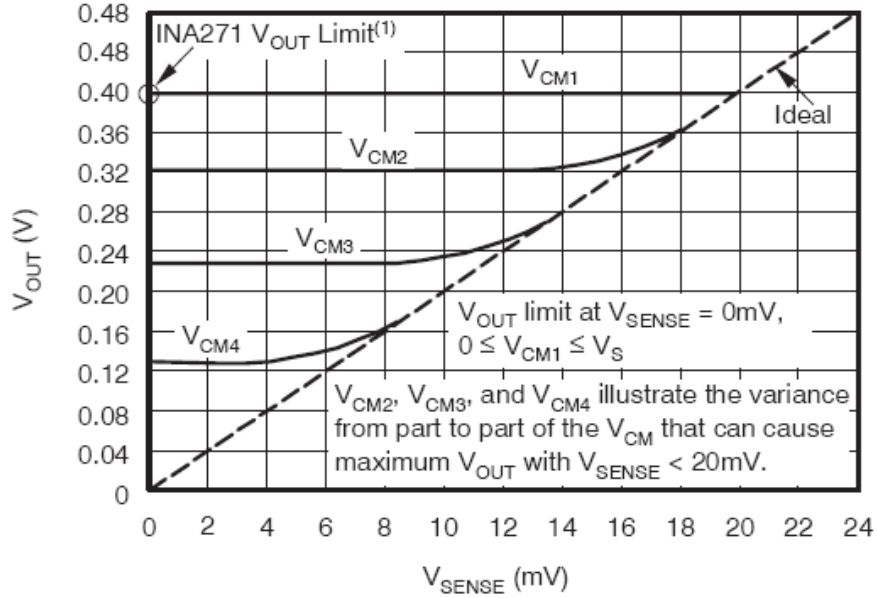
Accuracy – V_{SENSE} < 20mV: $0V \le V_{CM} \le V_S$

$$0V \le V_{CM} \le V_S$$

$$V_{SENSE} < 20mV$$



Least Accurate



Summary of INA Topologies

	Diff Amp INA	3 stage INA	2 stage INA	Current Shunt Monitor
Input impedance	• Low	• Highest	• Highest	• Low
Common-mode Range	•High beyond supply rails • related to power supply	•Lower • related to power supply	•Lower • related to power supply	•High beyond supply rails • independent of power supply
CMRR	•Good	•Best	•Best	•Good
Gains	•Unity or low gains • best for large differential inputs	•Variable low to very high for small differential inputs	•Variable low to very high for small differential inputs	•Fixed or adjustable in low to medium gain range
Power	•Low	•Highest power	•Higher than diff INA • lower than 3 stage INA	•Low to high

Choosing: Diff Amp or Instrumentation Amplifier?

► What is your source impedance?

- **High – use 2 or 3 stage INA**
- **Low - can use either**

► What is your common-mode range and supply voltage

- **common-mode voltage exceeding supply – Diff Amp**
- **common-mode within supply – Can use either**

Narrowing Down Choices

► Noise

- low source impedance needs low voltage noise
- high source impedance needs low current noise
- the smaller in the input signal, the more the noise sensitive

► Bandwidth

- 2 stage INA's have lower CMRR at high BW
- More difficult to achieve enough BW at high gain

► CMRR

- the bigger the common-mode voltage, the bigger CMRR needed
- should be high over the range of input frequencies

Narrowing Down Choices

► RRIO

- most important when operating on low single supply voltages
- maximizes usable dynamic range

► Voltage Offset and Drift

- error from voltage offset will be gained up and result in larger output error
- initial offset CAN be calibrated out, but drift cannot

► Power vs. BW, Slew Rate, and Noise

- higher BW and lower noise means higher power
- always a trade off between low power and noise/bw

► Input Bias Current

- creates an imbalance in the signal source resistance resulting in output error
- **more important in high input impedance apps**

Choosing a Current Shunt Monitor

► Current Shunt Monitor Considerations

- **What is the desired common-mode range?**
- **Do you have a voltage, current, or I^2C output preference?**
- **Do you need bi-directional measurement?**
- **What kind of accuracy do you need?**

REF30xx

50ppm/°C Max, 20ppm/ºC Typ. SOT23-3 Voltage Reference

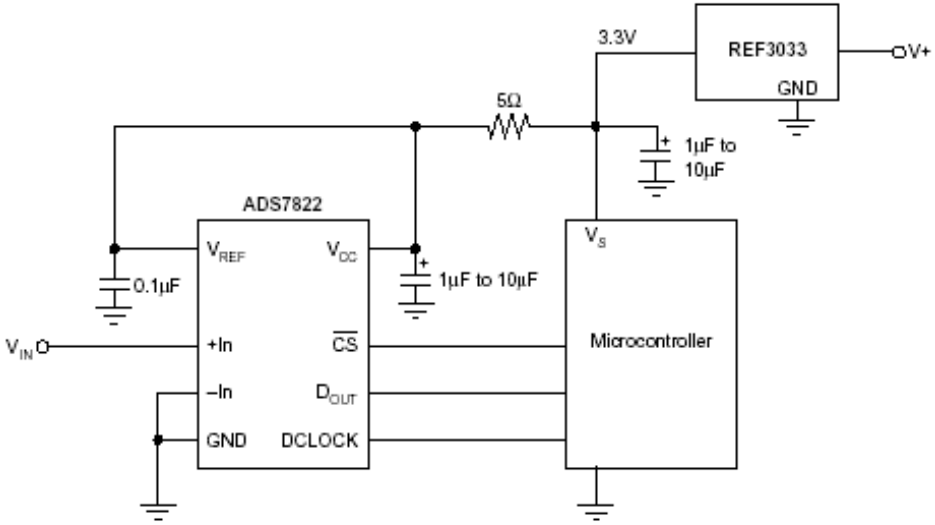
Features

µSIZE Package: SOT23-3

- High Output Current: ±10mA
- Low Temperature Drift: 50ppm/°C Max
- Long-term Stability 24ppm (Typ)
- High Accuracy 0.2% Max
- Low Iq: 50µA Max
- Output Voltage Noise 39µVpp (Typ)
- Low Dropout 50 mV Max
- Voltages 1.25 2.048 2.5 3.0 3.3 4.0

Key Benefits

- Lowest power, lowest cost 50ppm reference
- Reduces need for EE temperature calibration.
- Very good long term stability 0 to 1000h
  - Great for weight scale applications



Applications

- Data Acquisition Systems
- Portable Equipment
- Medical Equipment
- Test Equipment

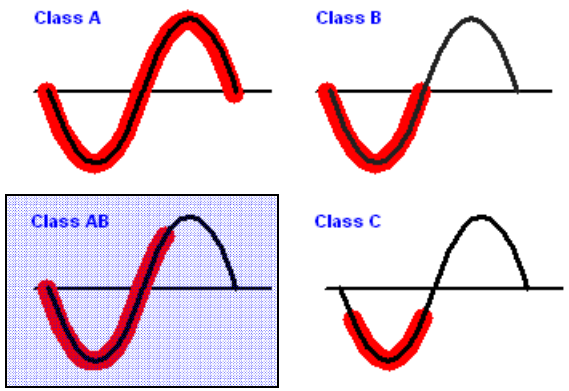
Analog Audio Amplifiers

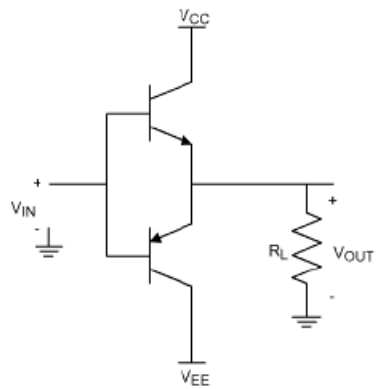
- **Class A**
  - conducts current throughout the entire cycle (360º)
  - most inefficient (15% efficient, with 85% of the energy wasted as heat)

- **Class B**
  - conducts current for half the cycle (180º)
  - two transistors can be used in a push-pull fashion, each one operating for 180º
  - more efficient than Class A, it is typically used in low-end audio products

- **Class AB**
  - conducts current for 180º to 200º
  - widely used in audio applications
  - reduces cross-over distortion
  - typically about 50% efficient

- **Class C**
  - conducts less than half of one wave cycle (100º to 150º)
  - the most efficient, but not used for audio applications because of their excessive distortion.

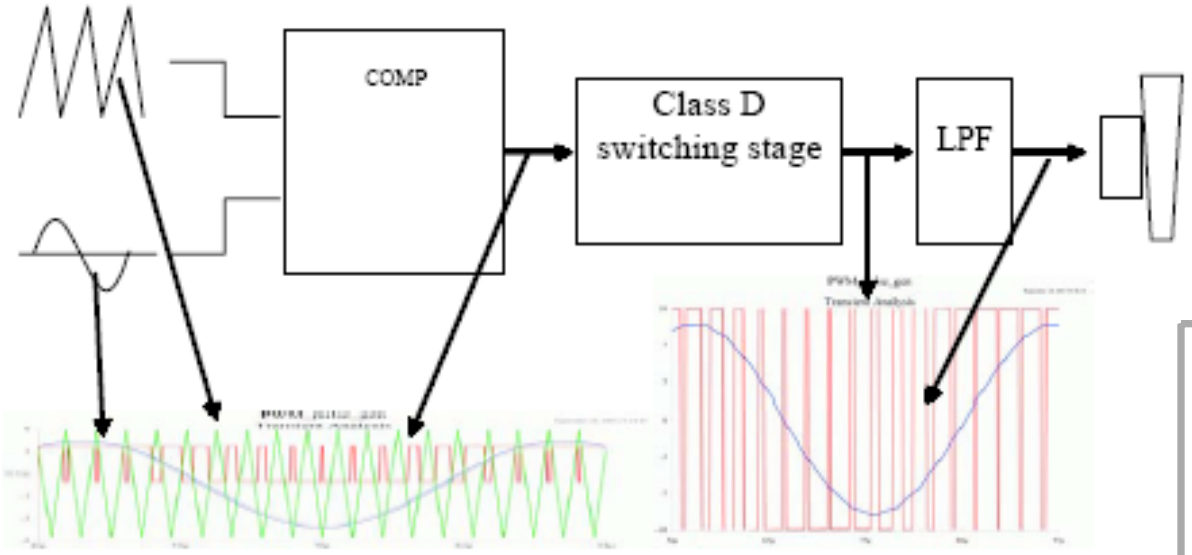


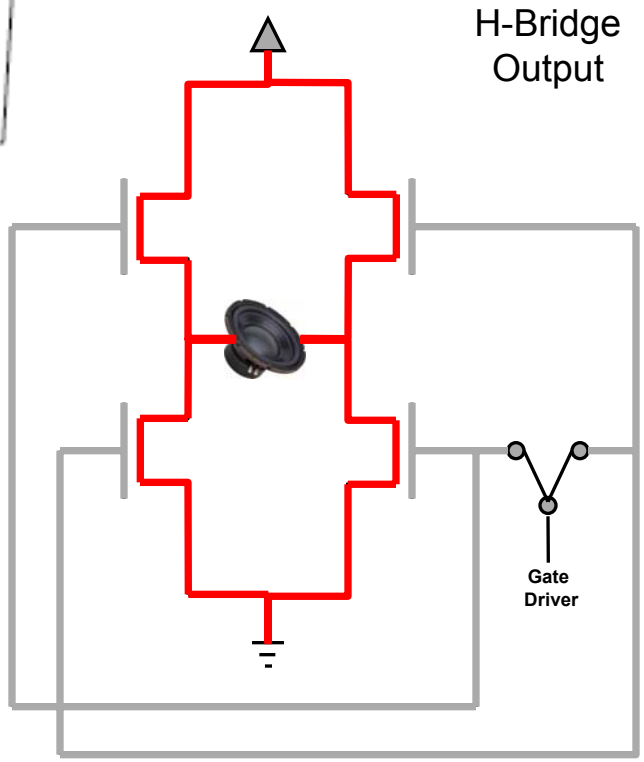


Digital Audio Amplifiers

- **Class D**

Class D is a digital-like amplifier that works by turning a transistor (FET) fully on or off. There little VI loss across the FET.

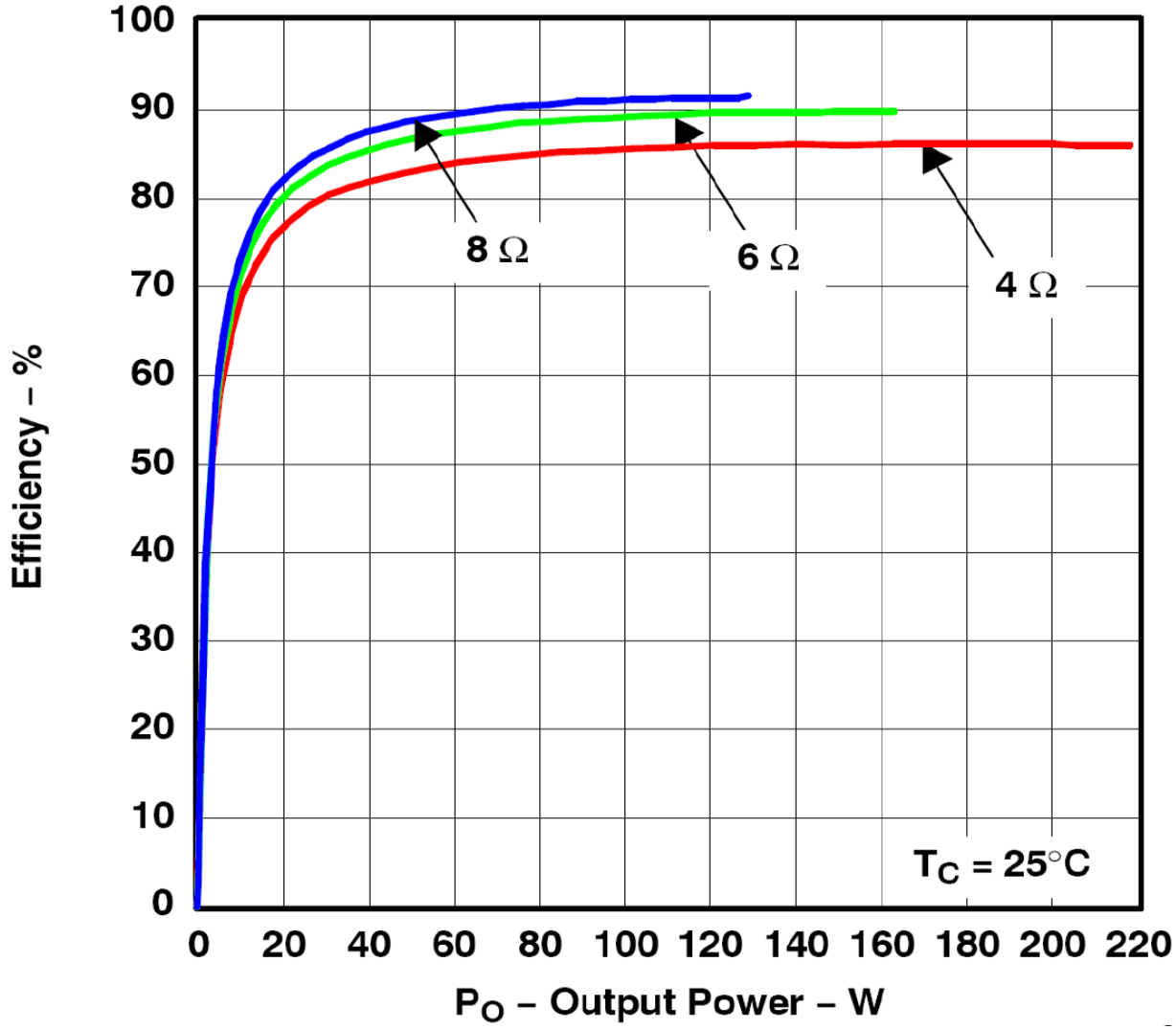




- **Interesting facts:**

Class D was not coined for “Digital;" it was the next letter after Class C.

Audio Efficiency is Impedance-dependent

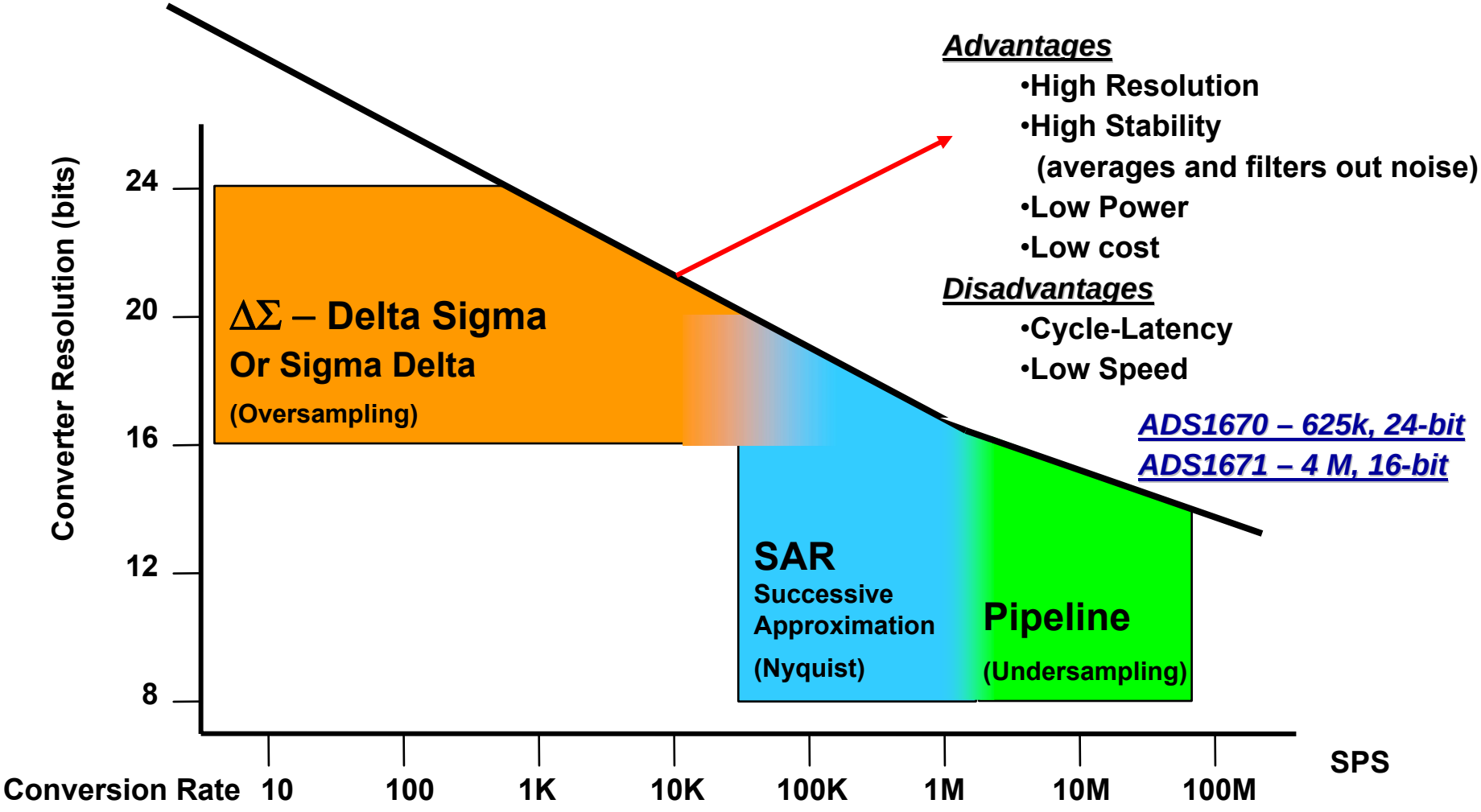


Power savings with ADC-selection

- Parameters Influencing Power Consumption:
- Architecture (Delta-Sigma, SAR, Pipeline, Flash)
- Sampling Rate
- Resolution
- Buffering
- Interface (parallel/serial, CMOS/LVDS)

  - See “Choose the right AD-Converter for your Application” in this presentation series for more Details on ADC selection.

ADC Technologies - ΔΣ



Advantages

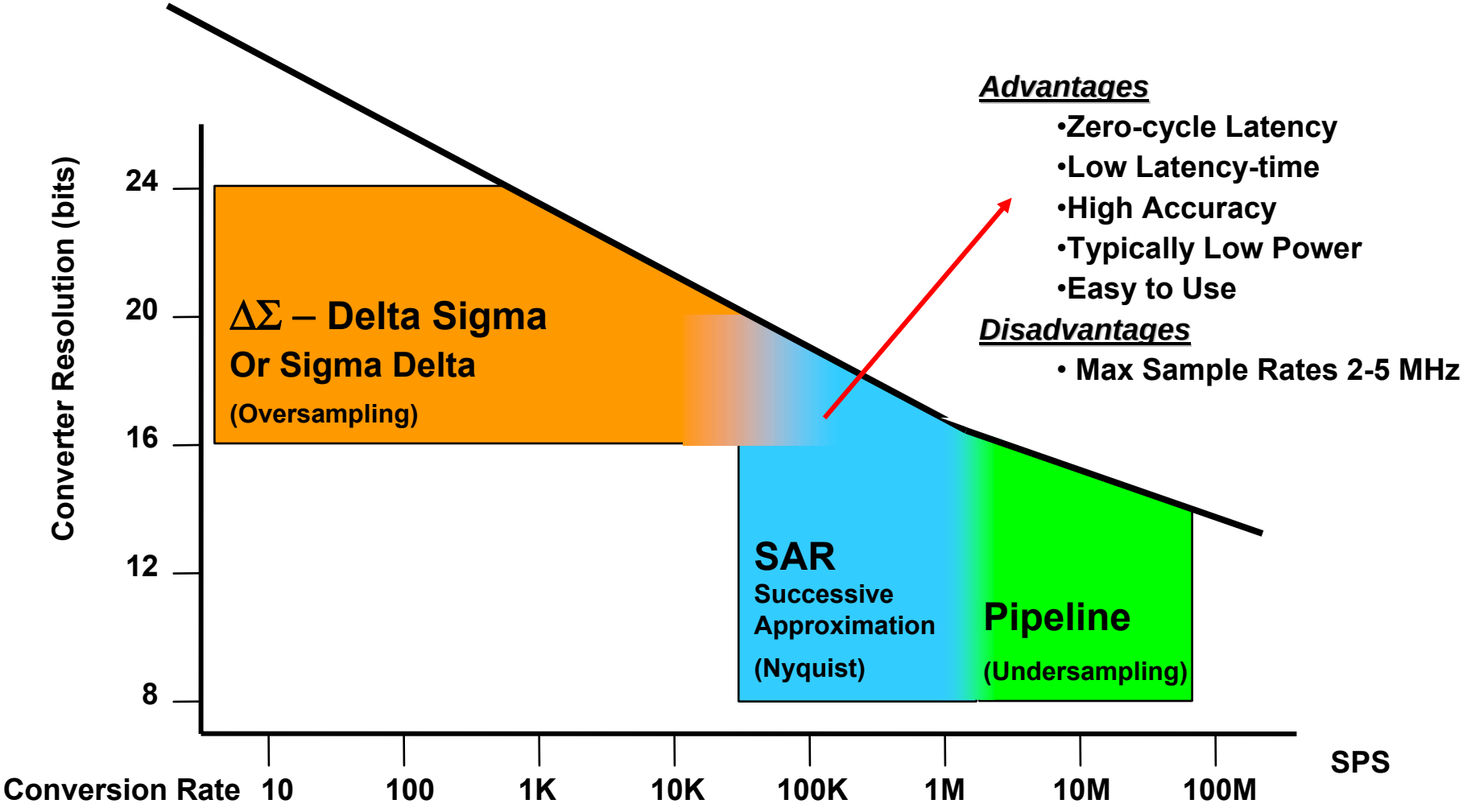
- High Resolution
- High Stability
  (averages and filters out noise)
- Low Power
- Low cost

Disadvantages

- Cycle-Latency
- Low Speed

ADS1670 – 625k, 24-bit
ADS1671 – 4 M, 16-bit

ADC Technologies - SAR



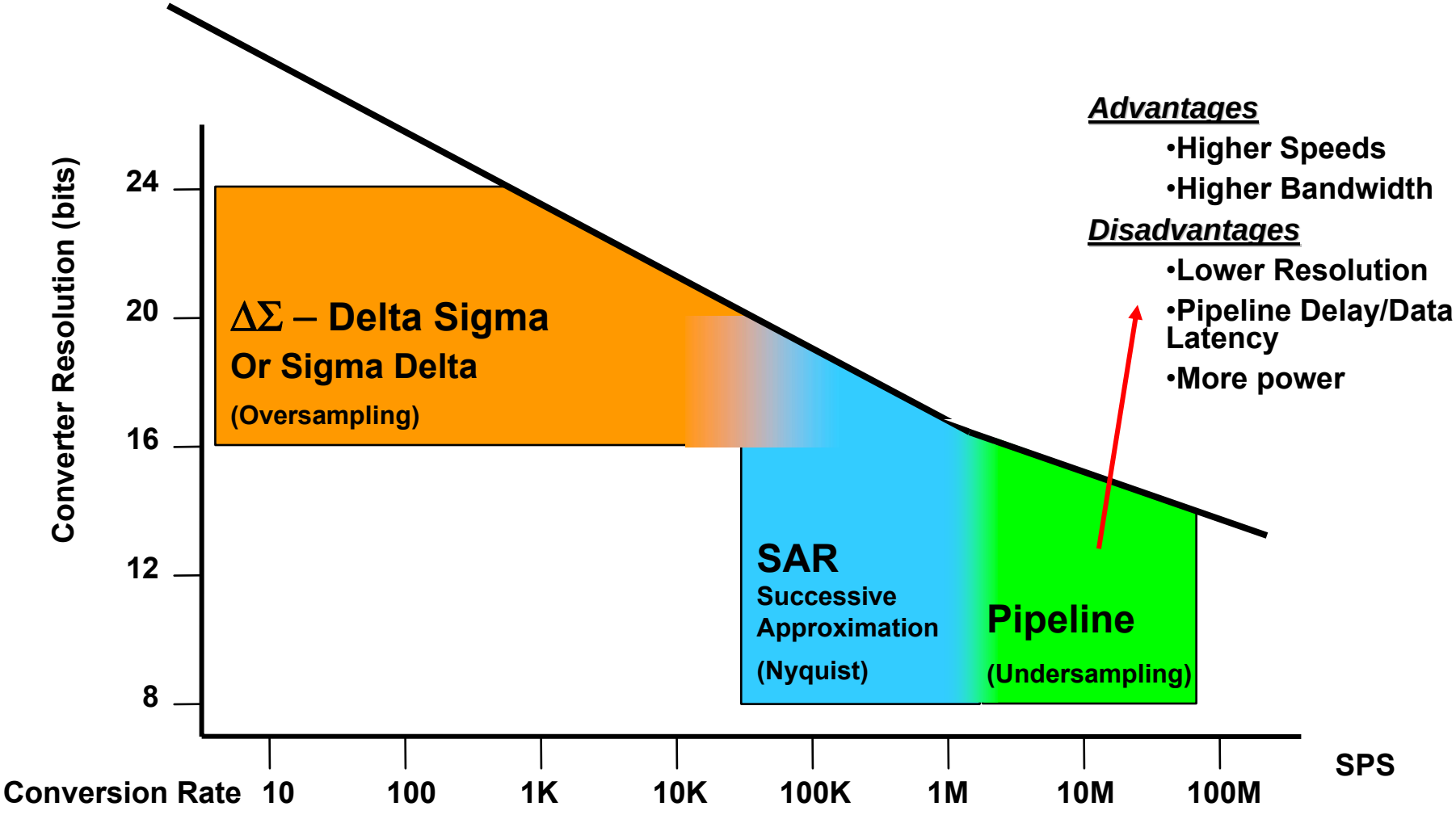
Advantages

- Zero-cycle Latency
- Low Latency-time
- High Accuracy
- Typically Low Power
- Easy to Use

Disadvantages

- Max Sample Rates 2-5 MHz

ADC Technologies - pipeline



Advantages

- Higher Speeds
- Higher Bandwidth

Disadvantages

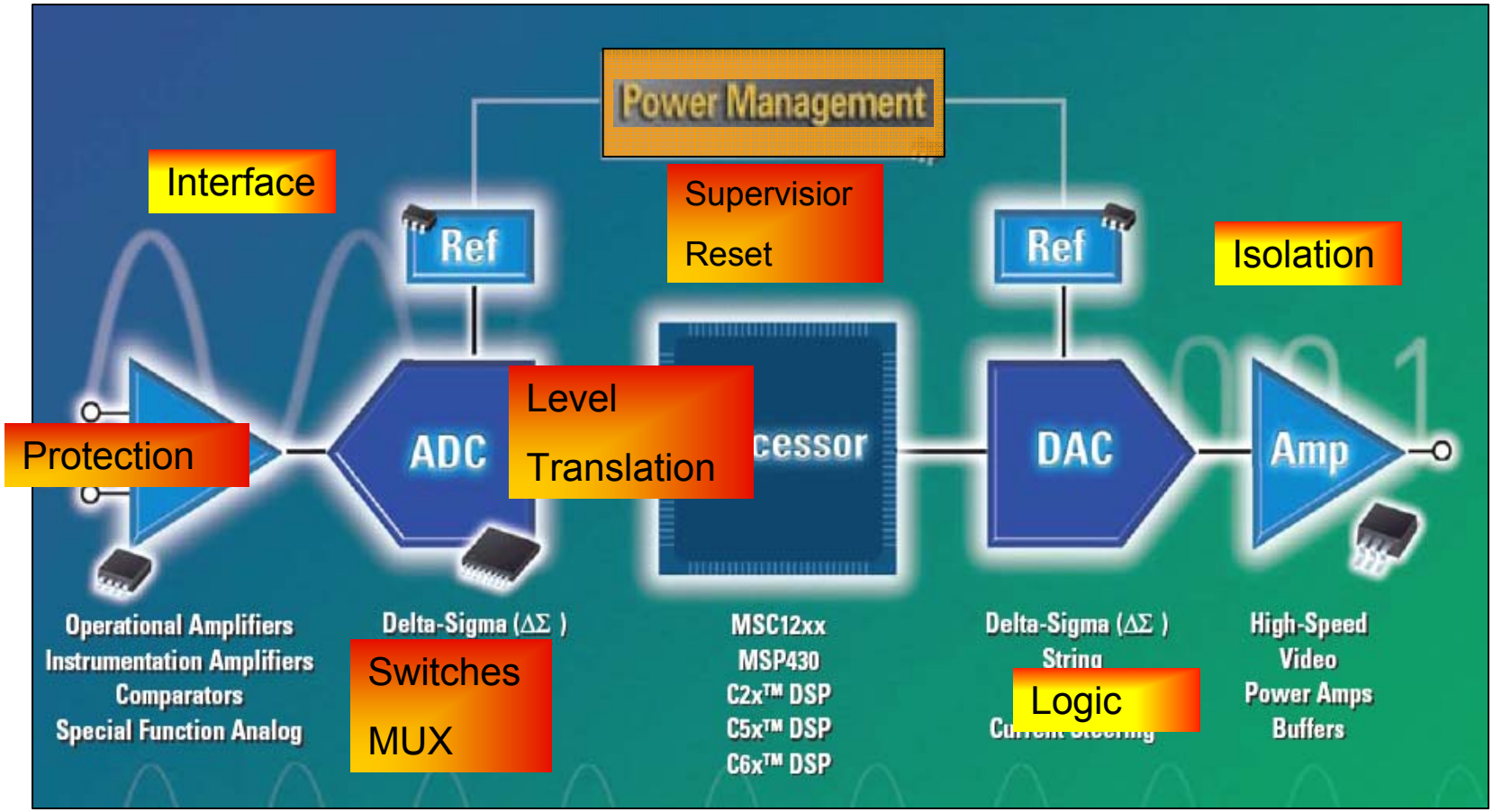
- Lower Resolution
- Pipeline Delay/Data Latency
- More power

Selecting ADC Topology

ADC Topology	*F Conversion*	*Resolution*	*Comments*
SAR	**< 5Msps**	**Up to 18-bit**	**Simple operation, low cost, low power.**
Delta-Sigma	**< 625ksps** **< 10MSPS**	**Up to 24-bit** **Up to 16-18 bits**	**Slow, moderate cost.**
Pipeline	**< 550Msps**	**Up to 16-bit**	**Fast, expensive, large power requirements.**

The Analog & Embedded world :

Only with.....



Precision Analog Components for low power Applications