Processors for computation intensive industrial applications

ARM9 + C647x

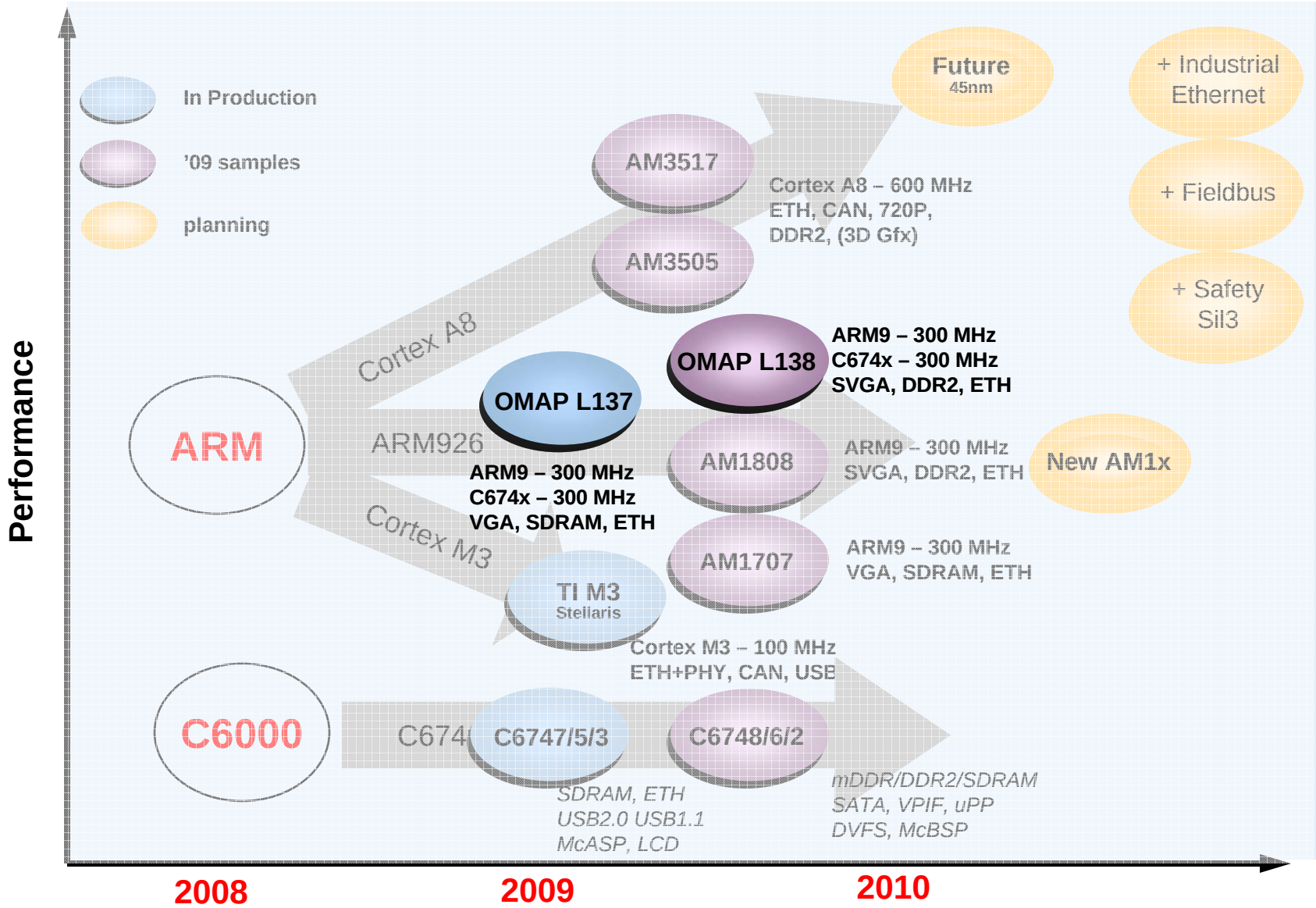
Agenda

- TI Embedded Processing
- Roadmap
- OMAP L1 for Industrial Automation Controller
  - System Interconnect
  - Programmable Fieldbus Subsystem
  - Interfaces
- Tools

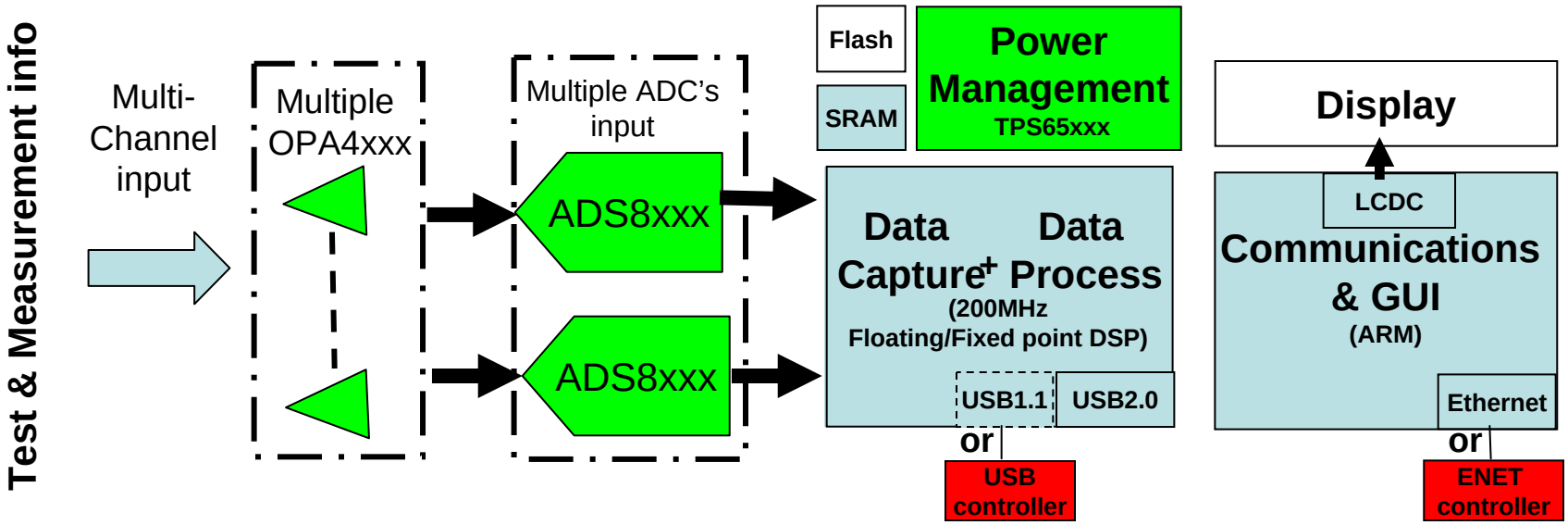
TI: Largest Portfolio of Embedded Processors

TI Embedded Processors						
Microcontrollers (MCUs)		ARM®-Based Processors			Digital Signal Processors (DSPs)	
16-bit ultra-low power MCUs	32-bit real-time MCUs	32-bit ARM Cortex™-M3 MCUs	ARM9/ARM Cortex-A8 MPUs	Application-specific processors	Low-power DSPs (*fixed-point*)	High-perf & multicore DSPs (*fixed & floating-point*)
MSP430	C2000™ Delfino™ Piccolo™	Stellaris®	Sitara™	DaVinci™ video processors OMAP™ mobile application processors	C5000™	C6000™

Industrial Processors Roadmap



Existing solutions



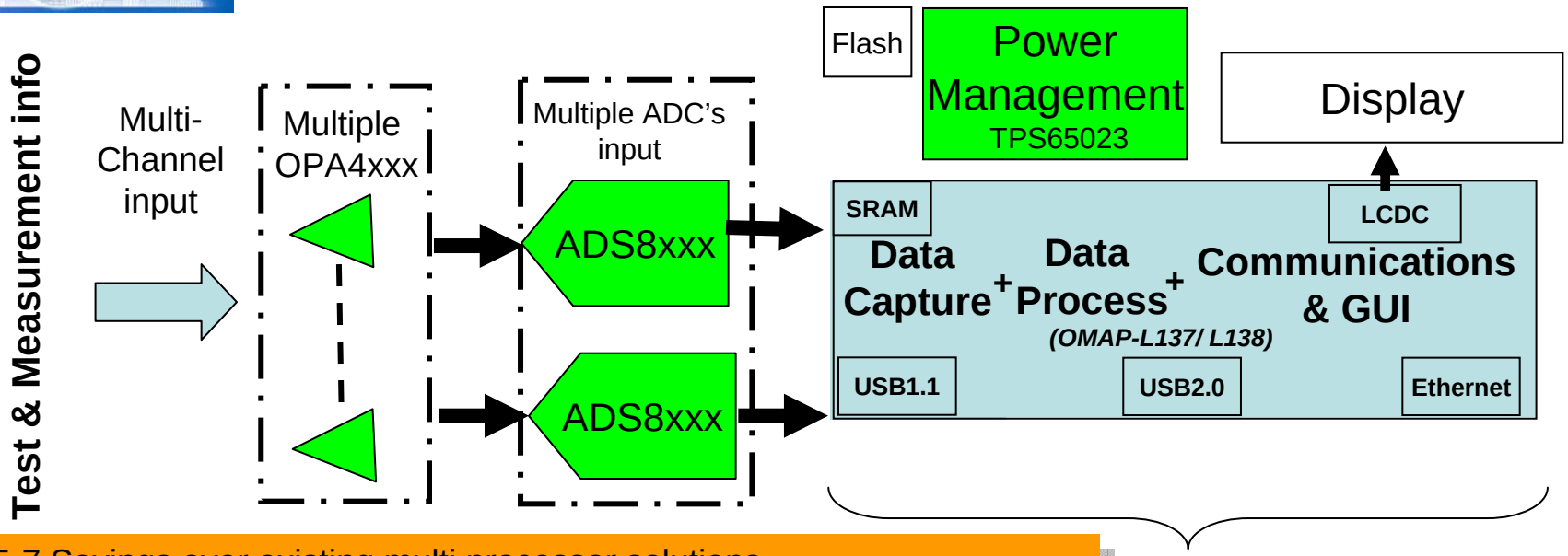
Approx. Cost (Option 1)
ARM9 (no EMAC) ~ $6 in 10ku
DSP (1 USB2.0) ~ $6 in 10ku
USB Controller ~ $2-3
EMAC Controller ~$3-4
SRAM ~ $2-4
Total ~$19-23

Communication
1 x EMAC and 2 USB

Approx. Cost (Option 2)
ARM9 with EMAC ~ $9 in 10ku
DSP (1 USB2.0)~ $6 in 10ku
USB Controller ~ $2-3
SRAM ~ $2-4
Total ~$19-22

Communication
1 x EMAC and 2 USB

Benefits of OMAP-L1x solution

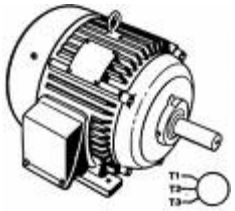


- $5-7 Savings over existing multi processor solutions
  - **OMAP-L137 processor controls both Data capture/ data processing, communications and GUI**
- 2x less processor power consumption
  - **Existing multi-processor solutions with external controllers and memories take up to 1.0W, OMAP-L137 Total power is less than 0.50W (300MHz, 1.2V)**
- Easy system connectivity
  - **One OMAP-L137 can support 1x EMACs and 2x USBs**
  - **On chip peripherals (SPI, UART, etc) simplify interfacing with other systems**
- LCD support up to QVGA allows rich user interface
- Industrial temp. allows maximum product lifetime and reliability

Approx. Cost
OMAP-L137 ~ $14.45 in 10ku
Total ~ $14.45

Communication
1 x EMAC and 2 x USB

Programmable Automation Controller



IGBT drivers

Isolated Current Measurem.

OMAP L137

Motion Control
C674x DSP
3x ePWM
2x eQEP
3x eCAP
Isolated current

HMI / Monitor
LCD Controller
Touchscreen
GPIOs

Safety

Application - softPLC
ARM9
L1P/D 16k/16k
MMU
128K RAM

Communication
GSM Interface
RT Ethernet
Master (Profinet)
Profibus
CAN i/f
RS485

GSM Module

RTE Slave ASIC

CAN transceiver

Profibus RS485

CoDeSys:
IEC 61131-3
softPLC
softMotion
Visualization

RT LINUX
2.6.28+

Standards:
IEC 61131-3
IEC 61508
RT-Ethernet

OMAP L137

Applications

- SDR, Portable Catalog, Bar Code Scanners, Portable Communications, Portable Medical, Portable Audio, PLC, PAC, HMI, Drives, Fieldbus

Features

CPU Cores

- **ARM926EJ-S™ (MPU) at 300 MHz**
- **C674x™ DSP Core at 300MHz**
- **2 x Processing Realtime Units (PRU) at 150 MHz**

Memory

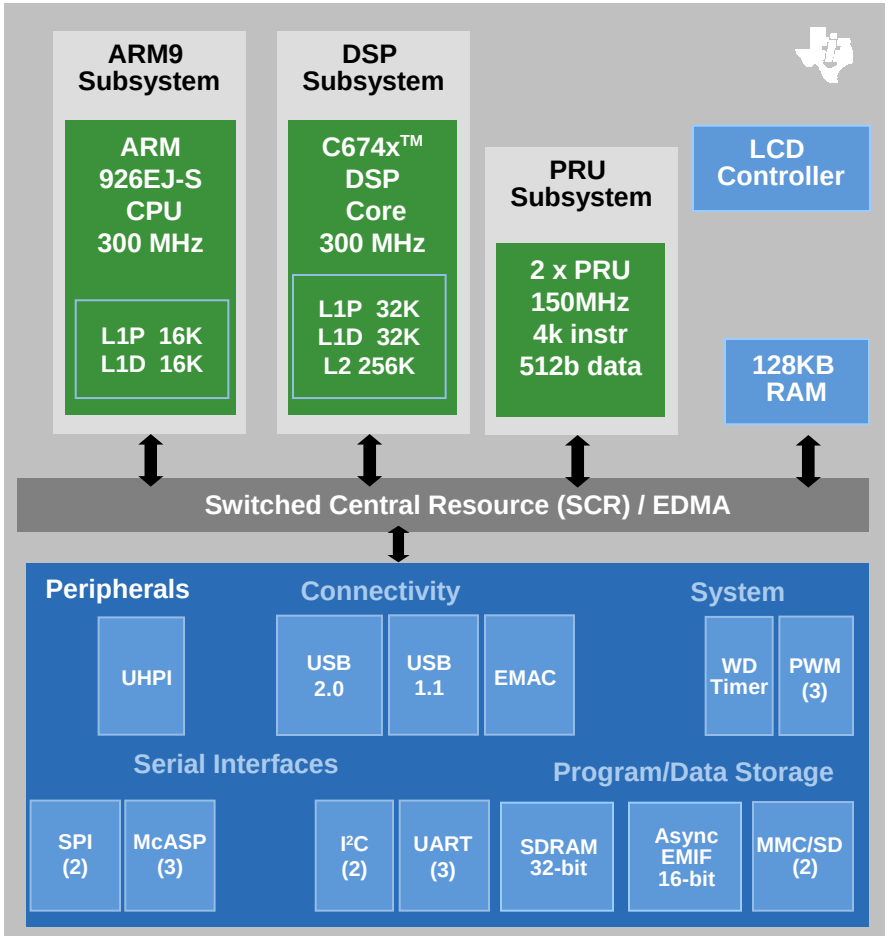
- ARM**: 16K I$, 16K D$, 64K ROM**
- DSP**: 32K L1D, 32K L1P, 256K L2 Cache, 128K RAM**
- **1MB ROM**

Peripherals (1.8/ 3.3V IOs)

- **10/100 Ethernet MAC**
- **EMIF1 – Supports 133 MHz SDRAM (16/32-bit)**
- **EMIF2 – Supports Async/NAND Flash (8/16 bit)**
- **USB 2.0 - USB OTG**
- **USB 1.1 – USB Full speed (OHCI)**
- **UHPI, McASP (3), UART(3), I²C (2), SPI (2), RTC, Timers (3), MMC/SD (2), LCD Controller, GPIO,**

- Package - 17 x 17mm BGA (1.0mm pitch) ~256pins
- Pin to pin compatible with C6747
- Power (1.0-1.2V Core, 3.3V IOs)
  - **Active < 500 mW @ 300MHz/1.2V/70C (estimate)**
  - **Standby < 100 mW @ 300MHz/1.2V/25C (estimate)**

OMAP-L137 ARM + DSP + PRUs



EVM Available 4Q08

Coming soon: OMAP-L138 (ARM9 + C674x DSP)

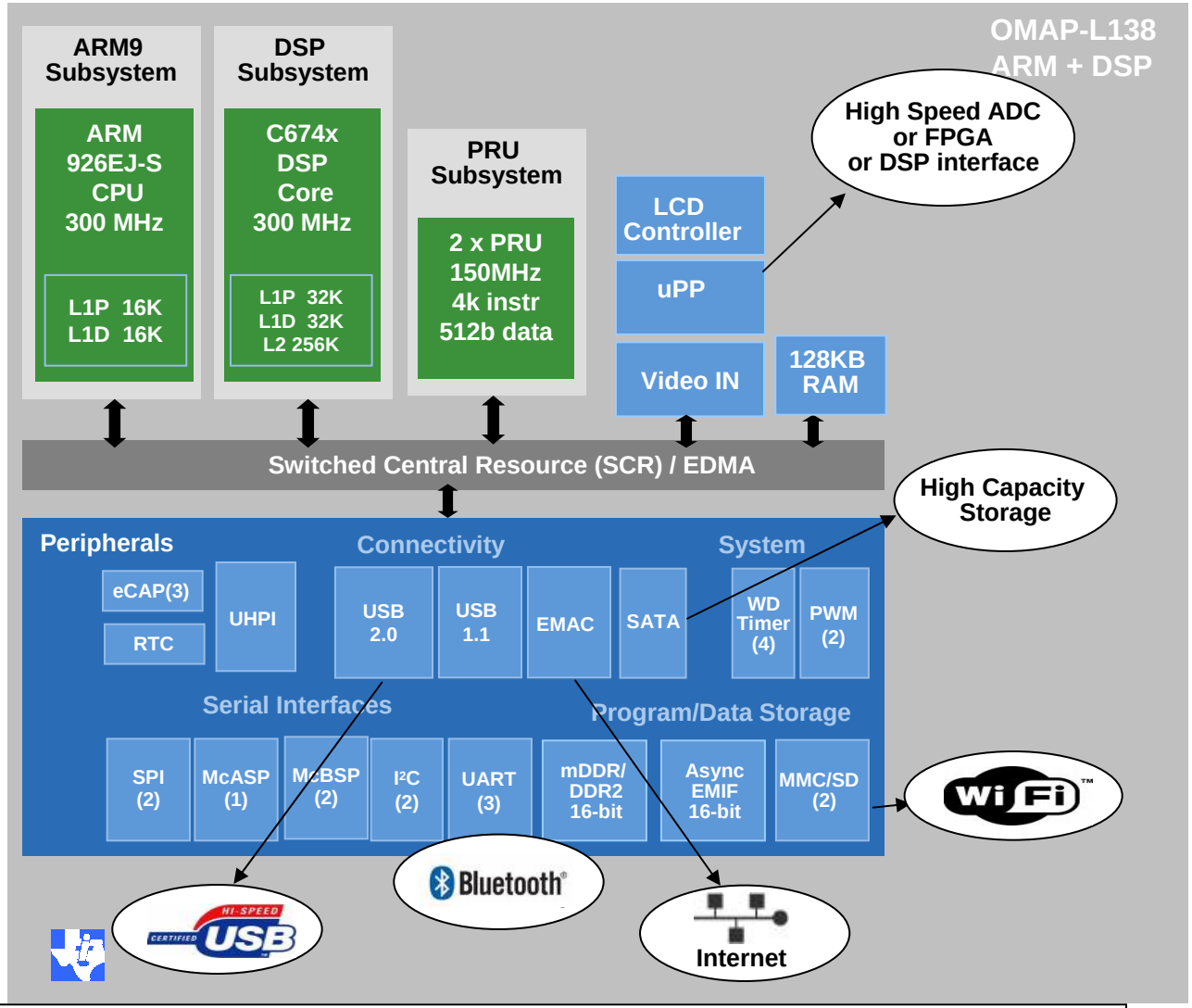
Schedule: TMX – June 09; TMS – 1Q10

- CPU Cores
  - ARM926EJ-S™ (MPU) upto 300 MHz
  - C674x DSP Core upto 300MHz
- Peripherals (1.8/ 3.3V IOs)
  - 10/100 Ethernet MAC
  - EMIFA - DDR (mDDR/DDR2)
  - EMIFB – SDRAM/NAND Flash
  - Video Port I/F
- Power (0.9-1.2V Core, 1.8/3.3V IOs)
  - Total Power < 440 mW @ 300Mhz, 1.2V, 25C

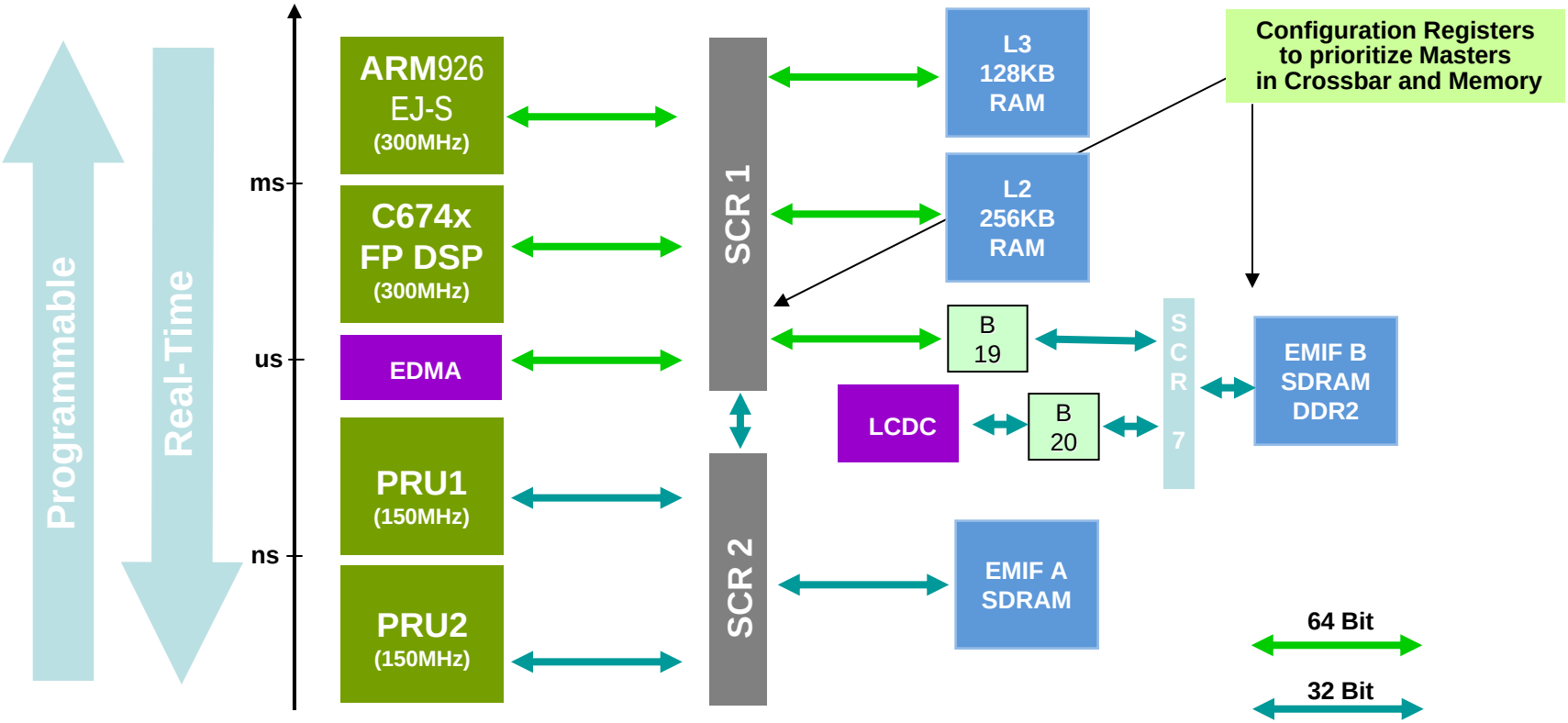
    For DSP at 70% loading, ARM at 50% loading; mDDR 50% active at 135MHz
  - Standby Power

    < 15mW @ 1.0V/ 25C;

    < 20mW @ 1.2V/25C
- Package
  - 13 x13mm nFBGA (65nm), 16x16mm BGA (0.8mm)
  - Pin to pin compatible with OMAP-L118/108, C6748/6/2
- Applications
  - SDR, Portable Catalog, Bar Code Scanners, Portable Communications, Portable Medical, Portable Audio



OMAP L1 Multi-Core Architecture

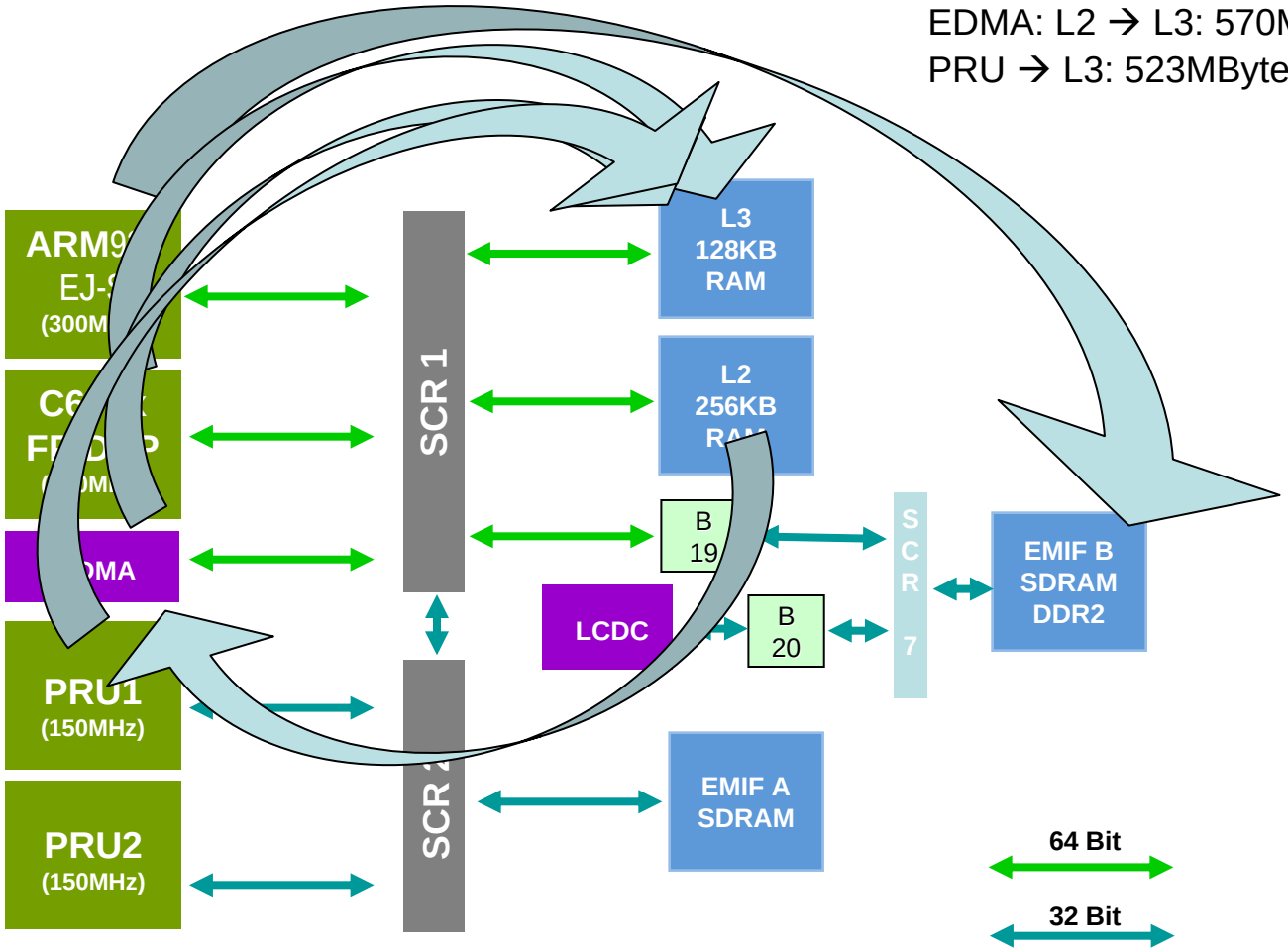


"Multi-Issue" Switched Central Resource 1 has 12x4 crossbar with 64 bit path at 150MHz.

With concurrent operation of up to 4 slaves the peak throughput is 4,8 GB/s!

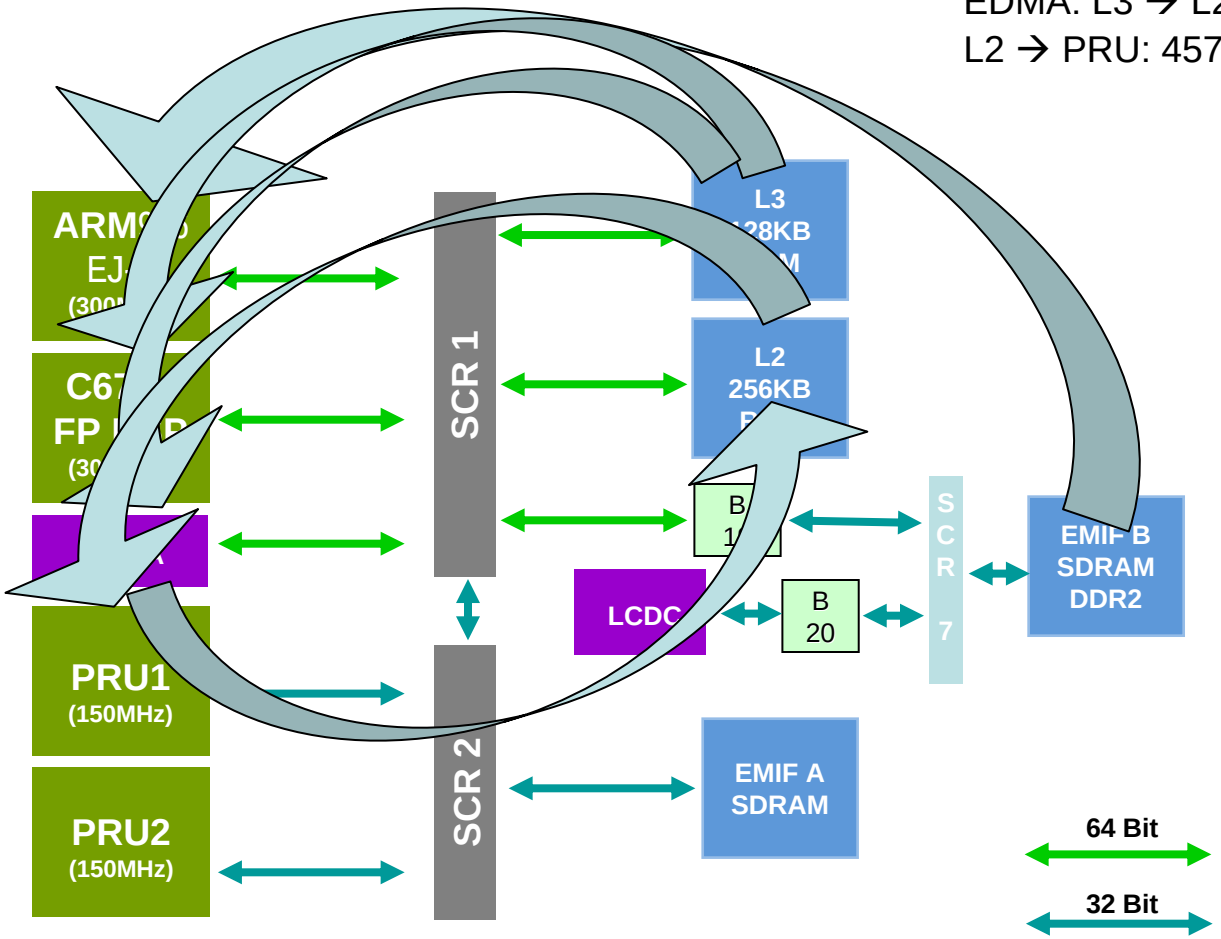
Memory Throughputs: Master to Slave

ARM → EMIFB: 175MByte/sec (8 byte burst)
DSP → L3: 44MByte/sec (4 byte burst)
EDMA: L2 → L3: 570MByte/sec
PRU → L3: 523MByte/sec (128bye burst)



Memory Throughput: Slave to Master

EMIFB → ARM: 24MByte/sec (8 byte burst)
L3 → DSP: 19MByte/sec (4 byte burst)
EDMA: L3 → L2: 457MByte/sec
L2 → PRU: 457MByte/sec (64bye burst)



EDMA 3.0 & SCR–3-Component Architecture

Benefit: Enhanced DMA engine for efficient movement of data between memory and peripherals. Switch Central Resource for high speed, concurrent interconnect

EDMA 3.0

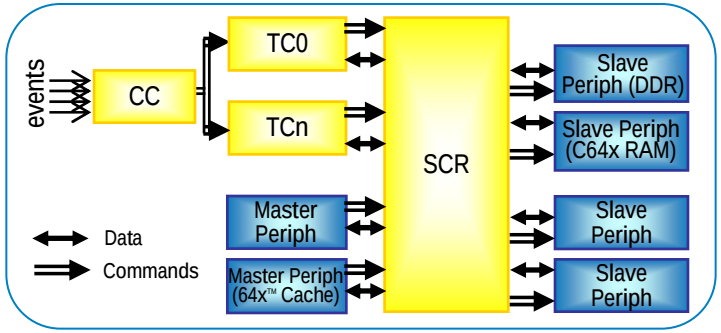
Channel Controller

- **Supports flexible 1D,2D and 3D transfers**
- **32 DMA Channels, 8 QDMA Channels**
- **Submits transfer requests (TR) to TC for data transfers between slave peripherals/memories**
- **Manages events (manual, external, chained)**
  - **Detects, prioritizes, queues**
- **Manages programmable channel store**
- **Supports transfer chaining and linking**
- **Stores/Manages context for multi-frame transfers, ping-pong buffers, circular buffers etc**
- **Improved debug visibility**

Transfer Controllers (TCs)

– **Performs slave-to-slave transfer requests from CC**

– **Responsible for data movement from SRC to DST**



Switched Central Resource (SCR)

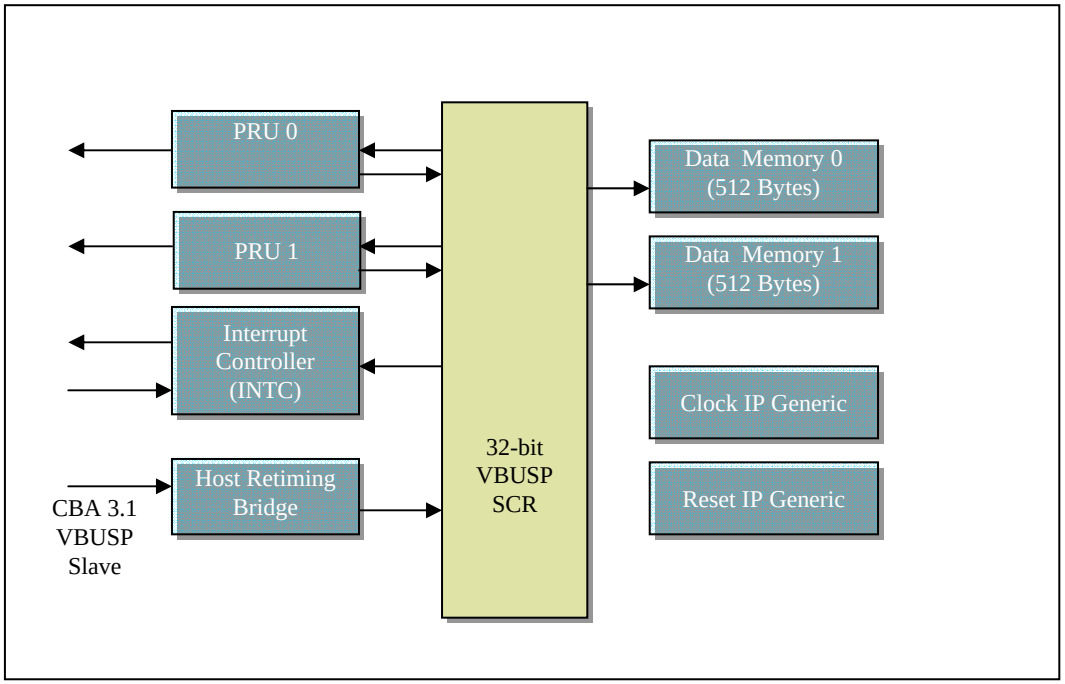
– New switch fabric separate from TC

– High Speed , Low Latency Interconnect

– Enables more concurrency

PRU Subsystem on OMAP L1

- Provides 2 Independent Programmable Realtime Units (PRU)
  - 32-Bit Load/Store RISC architecture
  - 4K Byte instruction RAM per core
  - 512 Bytes data RAM per core
  - Register 30 of each PRU is exported from the subsystem in addition to the normal R31 output of the PRU cores.
  - Each core runs at half of main processor speed (150MHz)



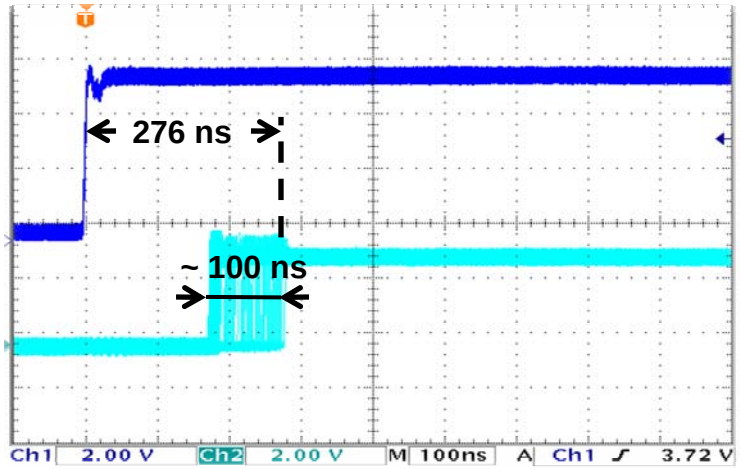
- PRU intended operation is little endian similar to ARM and DSP processors.
- Provides standard power management mechanism
  - PRU can be disabled via software to save power
  - Entire subsystem under a single PSC clock gating domain
- Provides interrupt controller for system events handling(No vectorization supported)

PRU – Value Proposition

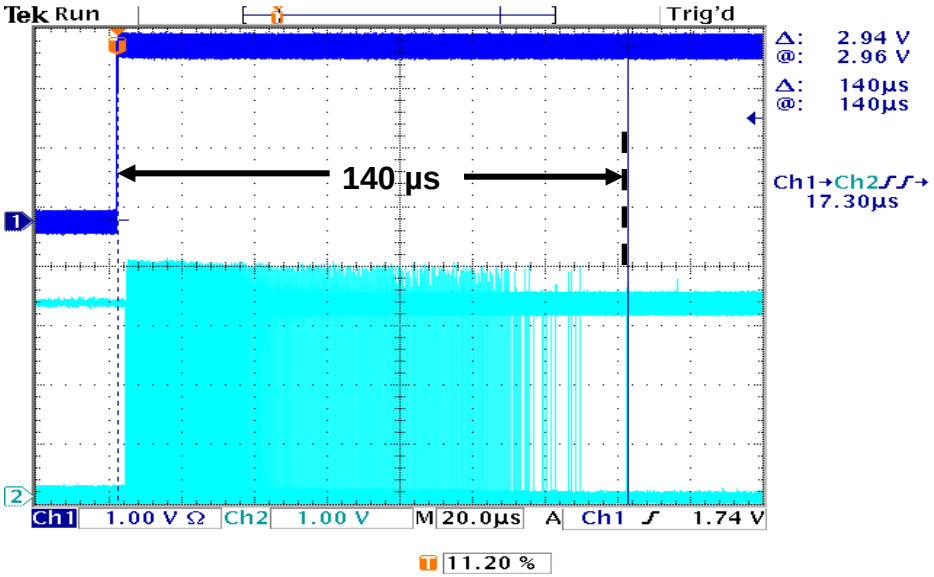
- Additional resources for Realtime Functions
- Full system visibility including Memory, IOs and Interrupts
- High bandwidth interconnect up to 550 MB/s (L2/L3 write)
- Interfaces
  - Profibus, CAN (tba), IEEE1588
  - 8 x UART for IO-LINK M
  - Industrial Ethernet Slaves (tba)
  - Sampling and Signal Conditioning (Offest, MIN, MAX, Interleave)
- Control
  - GPIO Latency in ns
  - ECAP for time stamping
  - PWMs
- Safety/Integrity
  - Memory, CPU, IO
- Power Monitor

Interrupt-Latency Results

– Hard Real-Time Requirements for the OS
  - **Jitter < 25 µs**
  - **Response time from 10 to 50 µs**

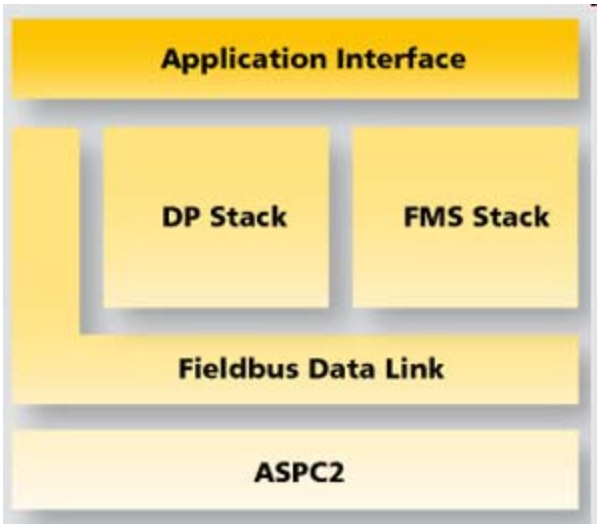


PRU

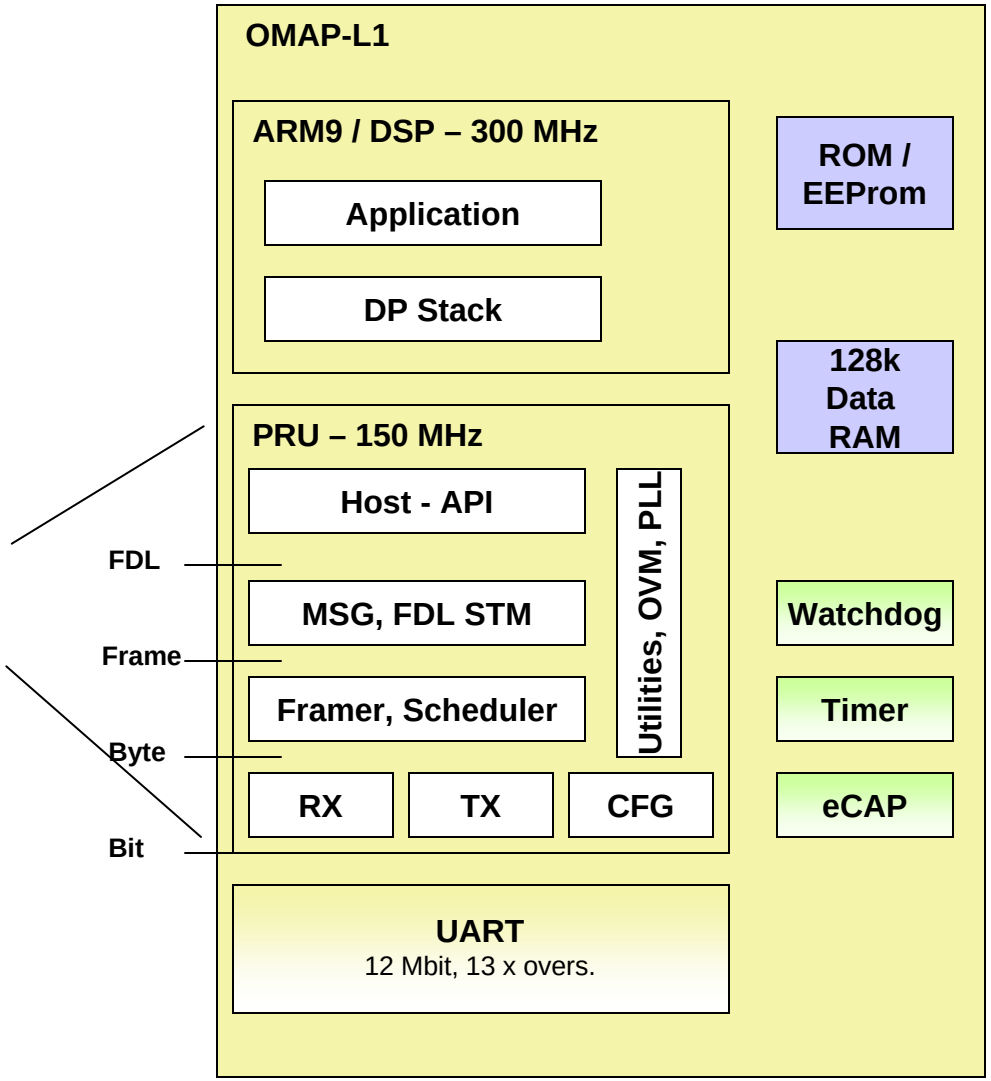


ARM Linux 2.6.18

Profibus DP – Master and Slave



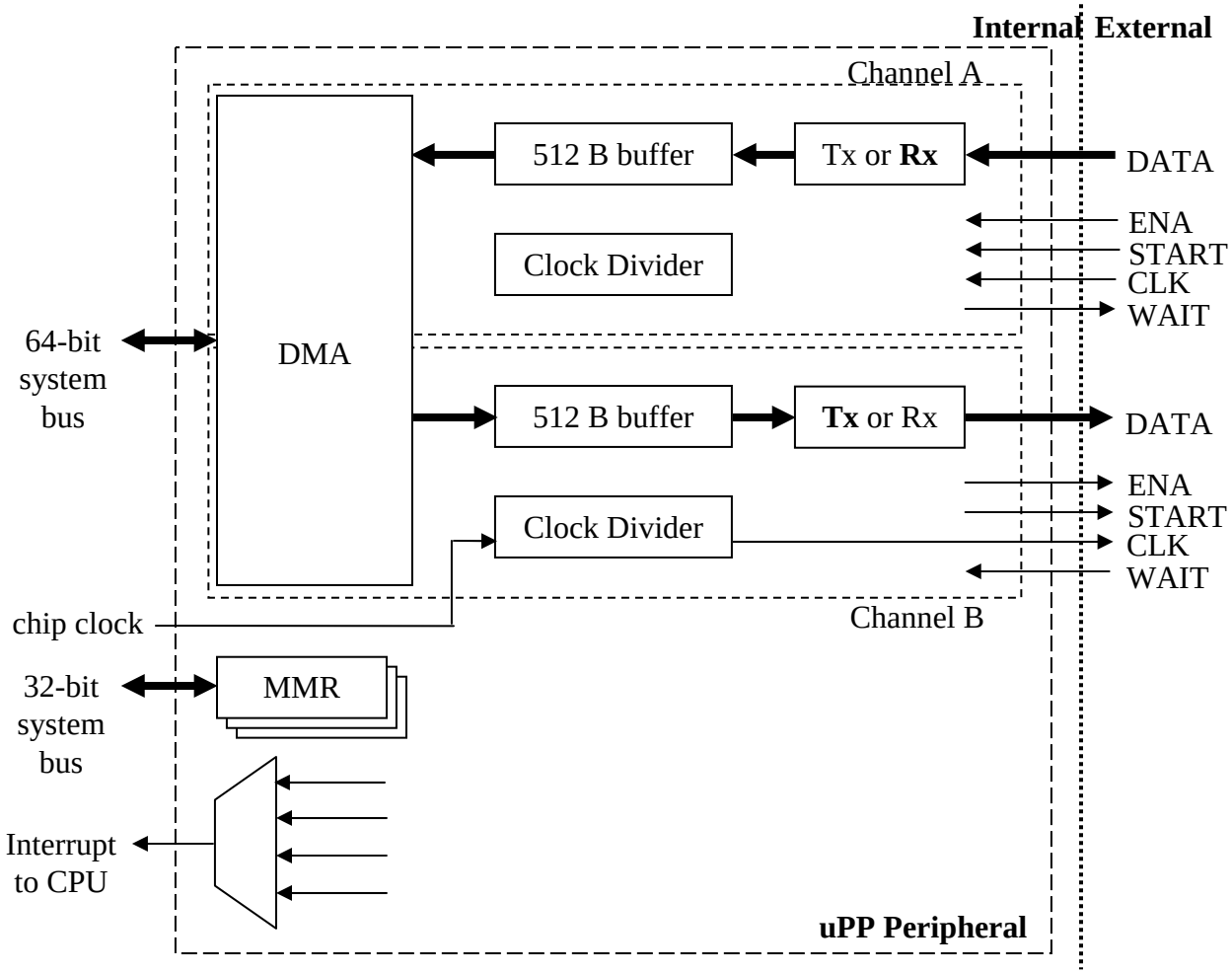
Token Passing (MultiMaster)
Live List – Identi - LSAP
Error Correction
Time Synchronization
(IEEE1588)



UPP at a Glance

- Universal Parallel Port – new peripheral on C6746/C6748/OMAP-L1x8
- Parallel data bus with 2 independent channels
- I/O speeds up to 75 MHz with 8-16 bit data width per channel
  - Up to 120 MB/s (sustained throughput) per channel
  - Faster than video port or HPI
- DDR support -> rising and falling edge sampling
- Internal DMA – leaves CPU EDMA free
- Few control pins – 2-4 (configurable) per channel
- Channels can operate in same or opposing directions
- 2D Programming Model. Multiple Lines per Window and Interleaving
- Additional System DMA in loopback mode

UPP – Functional Diagram



Enhanced Capture Module (eCAP)

Benefit: The Enhanced Capture Module (ECAP) is essential in systems where accurate timing of external events is important.

eCAP

Features of the eCAP include:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event timestamps
- Continuous mode capture of timestamps in a four-deep circular buffer
- Absolute timestamp capture
- Difference (Delta) mode timestamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the eCAP module can be configured as a single channel PWM output

OMAP L1 vs Competitor (x86)

Core SoC	ARM926 OMAP L1	C674x OMAP L1	PRU1 OMAP L1	PRU2 OMAP L1	x86 + Chipset
MHZ	300	300	150	150	1600
Cache, Local Memory	16k I, 16k D, 8K RAM, 64 K ROM	32 k I, 32 k D 256k L2 1M L2 ROM	4K I, 512 D	4k I, 512 D	24k I, 32k D 512k L2
Multiscalar	1	8, 2.4 GMAC, 1.8 GFLOPS	1	1	2 HT SSE3
Pipeline	5	13	0	0	16
Interconnect	"multi issue" SCR1 4,8 GB/s		"single issue" SCR2		FSB 3,2 GB/s
Power Consumption	SoC < 500 mW				Incl. Chip Set < 5 W
Form Factor	13x13 mm (0.65 pitch) 16x16 mm (0.8 pitch)				13x14 mm + 22x22 mm (NB)

OMAP L1 competes against x86 through flexibility, high level of integration and Interconnect

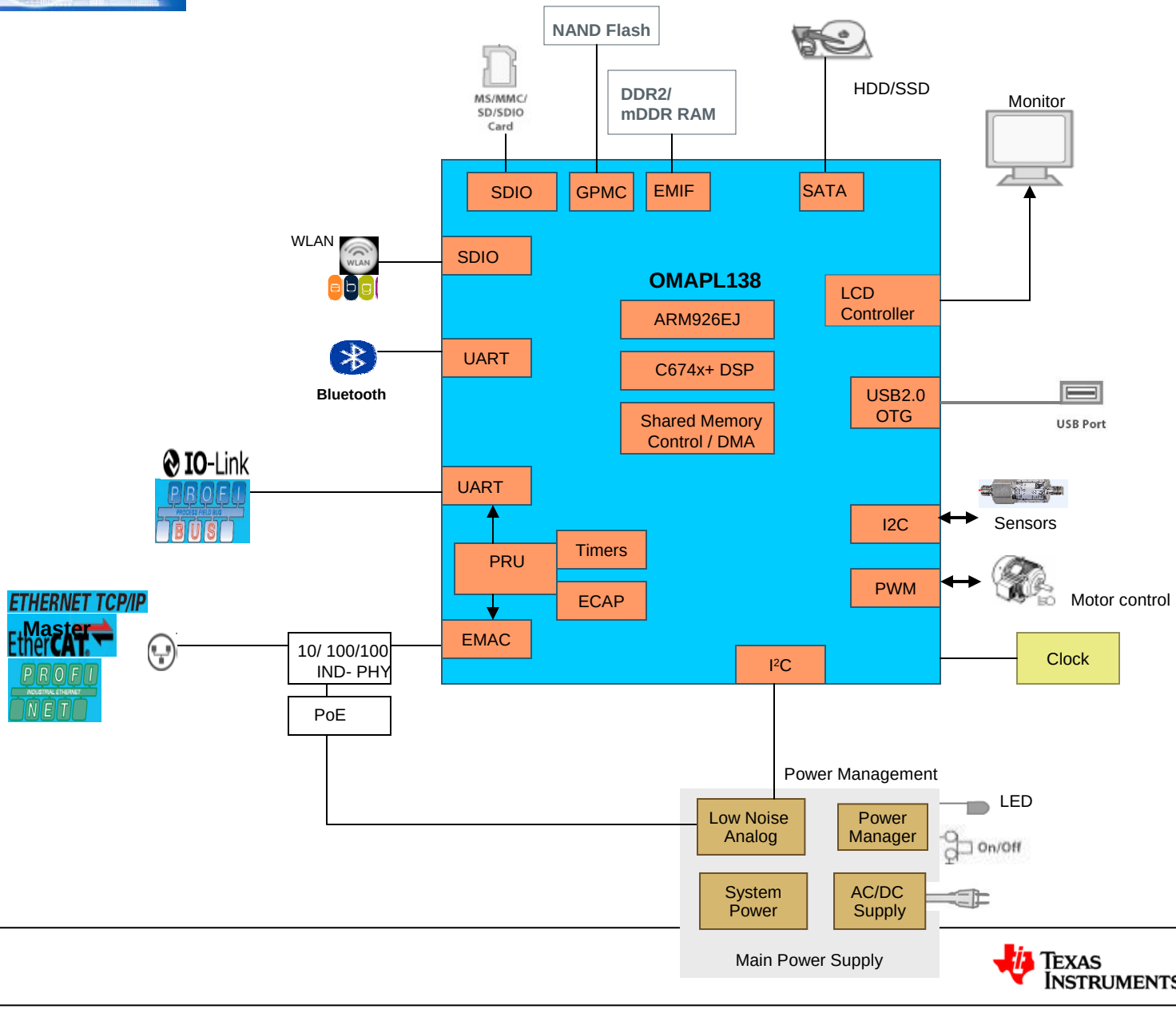
OMAP L1 Selection Criteria

- Is there real-time control or communication with the application?
- Are there multiple tasks running in parallel?
- Are their power constraints?
- Are their heat constraints?
- Are their space constraints?
- Do you need programmable Fieldbus?
- Do you need hardware support for Safety (SIL) compliance?
- Is there Signal Processing with Floating Point Precision?
- Is there a need for USB powered System or PoE?
- Does your application fit in on-chip 448 K RAM?

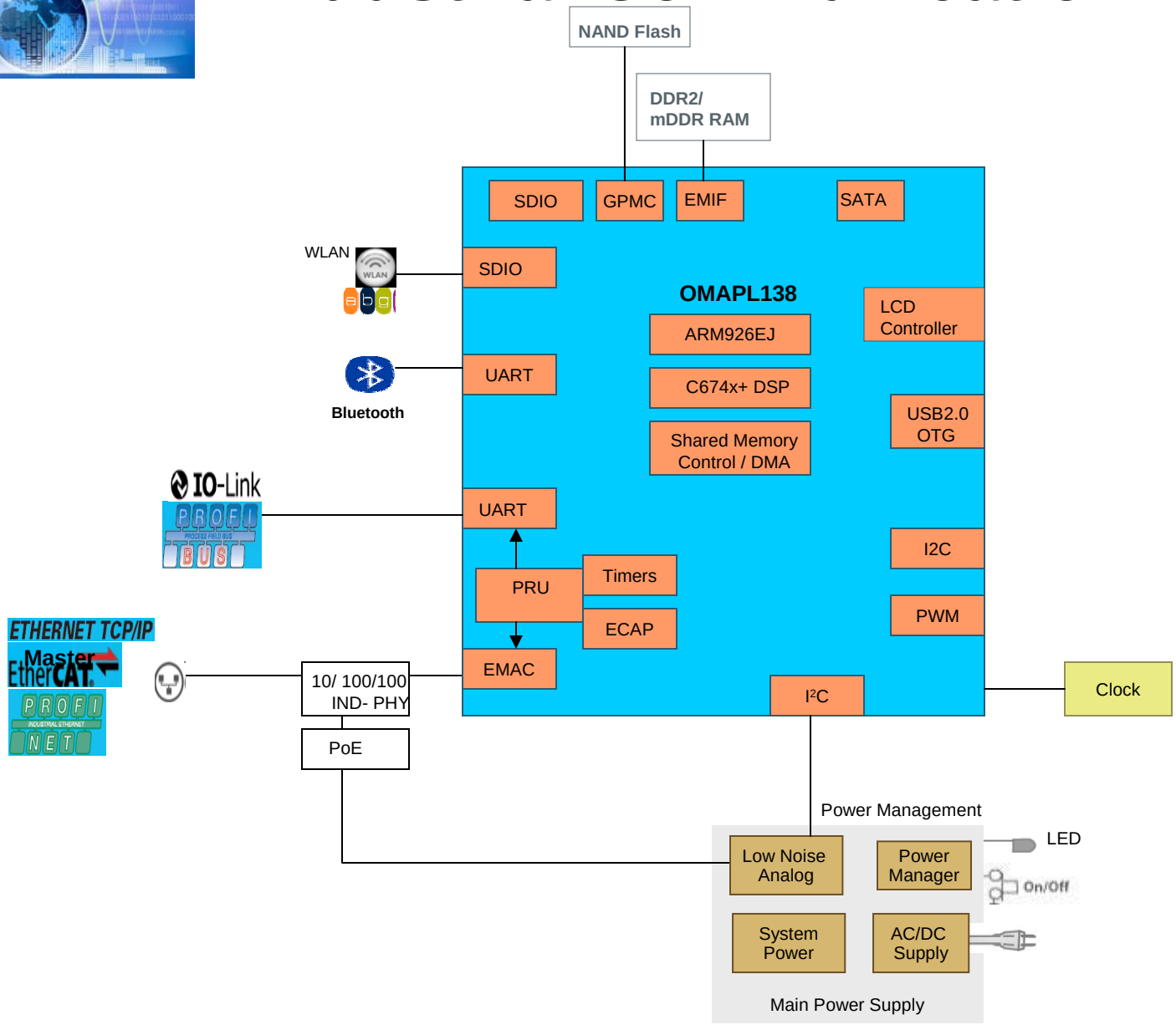
OMAP L1 Value is given by a combination of key requirements in the System.

FPGA + x86 Architecture lacks programmability, integration and determinism.

Programmable Logic Control



Industrial Communication Interface



OMAP-L137/TMS320C6747 Floating Point Starter Kit

SPECTRUM DIGITAL INCORPORATED

Starter Kit

Available Now: $395

Hardware

OMAP-L137 EVM

- OMAP-L137™ – 300MHz
- 24-bit stereo CODEC
- Four 3.5 millimeter audio jacks
- 64Mb SPI Flash memory
- 512Mb SDRAM
- ETH MAC, USB 2.0, USB 1.1, MMC/SD, LCDc
- HPI, McASP & I^2C interface header emulation
- On-board standard JTAG interface
- Embedded JTAG support via USB
- +5V universal power supply
- Expansion ports for plug-in modules

Software

- Code Composer Studio™ IDE
- Simulator included
- DSP/BIOS™ RTOS, eXpressDSP, and Monta Vista Linux Pro 5.0 Software support
- Fast run-time library available on the web
- MATLAB/Simulink Support (FUTURE)
- LabVIEW for Embedded Applications Support (FUTURE)
- Quick Start Guide and technical reference

OMAP-L137/TMS320C6747 Floating Point Starter Kit on TI eStore:
http://www.ti-estore.com/Merchant2/merchant.mvc?Screen=PROD&Product_Code=TMDXOSKL137BET

Tools for varying customer requirements

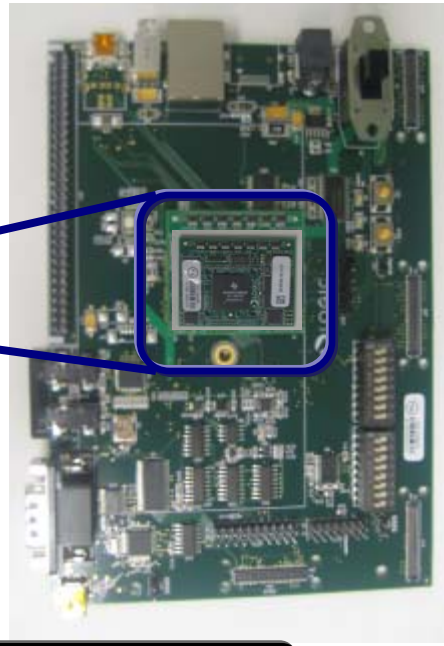
System-on-Module

- OMAP-L138 processor
- 64 or 128MB mDDR
- Ethernet PHY

**Available from Logic for ~$99*

Small FF Confirmed mDDR design

PN: SOMOMAPL138-10-1602AHCR
for 128MB mDDR support
PN: SOMOMAPL138-10-1502AHCR
For 64MB mDDR support



+

Only $149

Experimenter board

- OMAP-L138 SOM
- 64MB mDDR
- **Access to key peripherals:**
  - **SATA, USB, EMAC, Audio**
- TPS65070 power management
- DSP/BIOS™ peripheral drivers
- CCStudio™ 3.3
- **Community supported**
- **Available from TI & Logic for $149*

Open source Linux peripheral drivers

PN: SDK-OMAPL138-10-6408R

OMAP-L138/C6748 EVM

2x the memory w/128MB

- **Full peripheral access:** SATA, uPP, EMAC, USB 2.0/1.1 and MMC/SD, VPIF, LCDC
- Software included
- TI supported
- LCD display option

Additional C6748 SOM

**Available from TI for $795-$849*

PN: TMDXOSKL138BET

Software Overview

- ARM side
  - MontaVista Linux kernel, drivers, tool chain etc. (for OMAPl137)
  - Open source kernel/driver from GIT tree (for OMAPL138)
  - Other OSes: WinCE, VxWorks
- DSP side
  - TI DSP/BIOS 5.33
  - BIOS based drivers
  - CSL based OS-agnostic examples
  - Network Development Kit (NDK) – APIs very similar to Berkeley socket APIs
  - File system: ERTFS
  - JUNGO USB Stack
- ARM/DSP
  - DSPLINK

Linux Platform Support Package

- UBOOT
  - 1.3.3 for OMAPL137
- Utility program to flash DSP UBL, ARM UBL, UBOOT and Linux kernel in flash media
- LSP user guide explains
  - LSP installation
  - How to build kernel/driver/UBOOT
  - How to setup Linux host (briefly)
  - Different kernel boot options
- Open source kernel (+ drivers)
  - OMAPL137: MV 2.6.18 kernel; Will be pushed to open source later
  - OMAPL138: Development from the latest kernel in the open source

DSP/BIOS

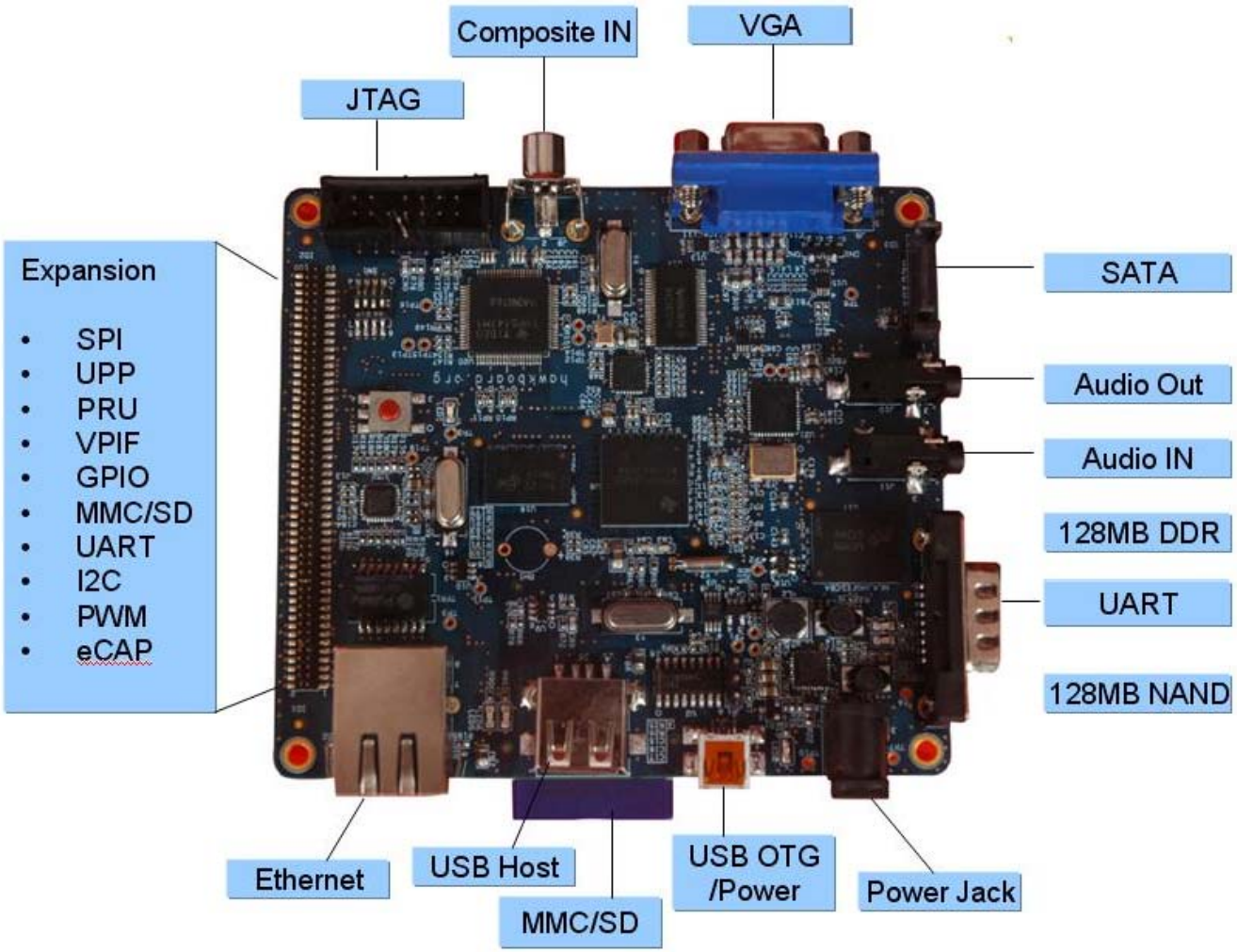
- TI Real Time OS (free to use)
- Support prioritized HWI, SWI, TSK
- 1 ms scheduling interval vs. 10ms on Linux
- Low overhead:
  - No user/kernel transition latency
  - Low Interrupt latency: 97 cycles.
  - Low task context switching time.
- No MMU and memory protection
- Global memory share between threads
- Application + BIOS = .out image; Cannot dynamically load and run application executable

DSP/BIOS Platform Support Package

- BIOS 5.33 drivers
  - Serial (UART, I2C and SPI)
  - Audio (McASP, AUDIO interface and CODEC)
  - Storage (Block media, MMCSD and NAND)
  - LCDC Raster and LIDD drivers
  - GPIO driver
  - PSC (clock on/off for the modules)
- BIOS 5.33 driver examples (1 for each driver)
- Chip Support Library (CSL)
  - .h: Macros define peripheral registers and fields
  - Examples: C code showing how to program HW using .h
    - CACHE, GPIO, I2C, IDMA, INTC, PLLC, SDRAM, SPI, TIMER, UART

DSPLINK

- Provides a standard way of multi-processor communication
- Allows “master” processor to control execution of “slave” processor(s)
  - ARM can boot-load the DSP
  - ARM can stop execution of the DSP or place it in reset
- OS: ARM side is Linux; DSP side is BIOS
- Provides peer-to-peer protocols for communication between the multiple processors in the system
  - Includes complete protocols such as MSGQ, CHNL, RingIO
  - Includes building blocks such as POOL, NOTIFY, MPCS, MPLIST, PROC_read/PROC_write which can be used to develop different kinds of frameworks above DSPLINK

hawkboard.org

A Open Community Portal for OMAP L 138 (ARM 9 & C674x Floating Point DSP) Applications