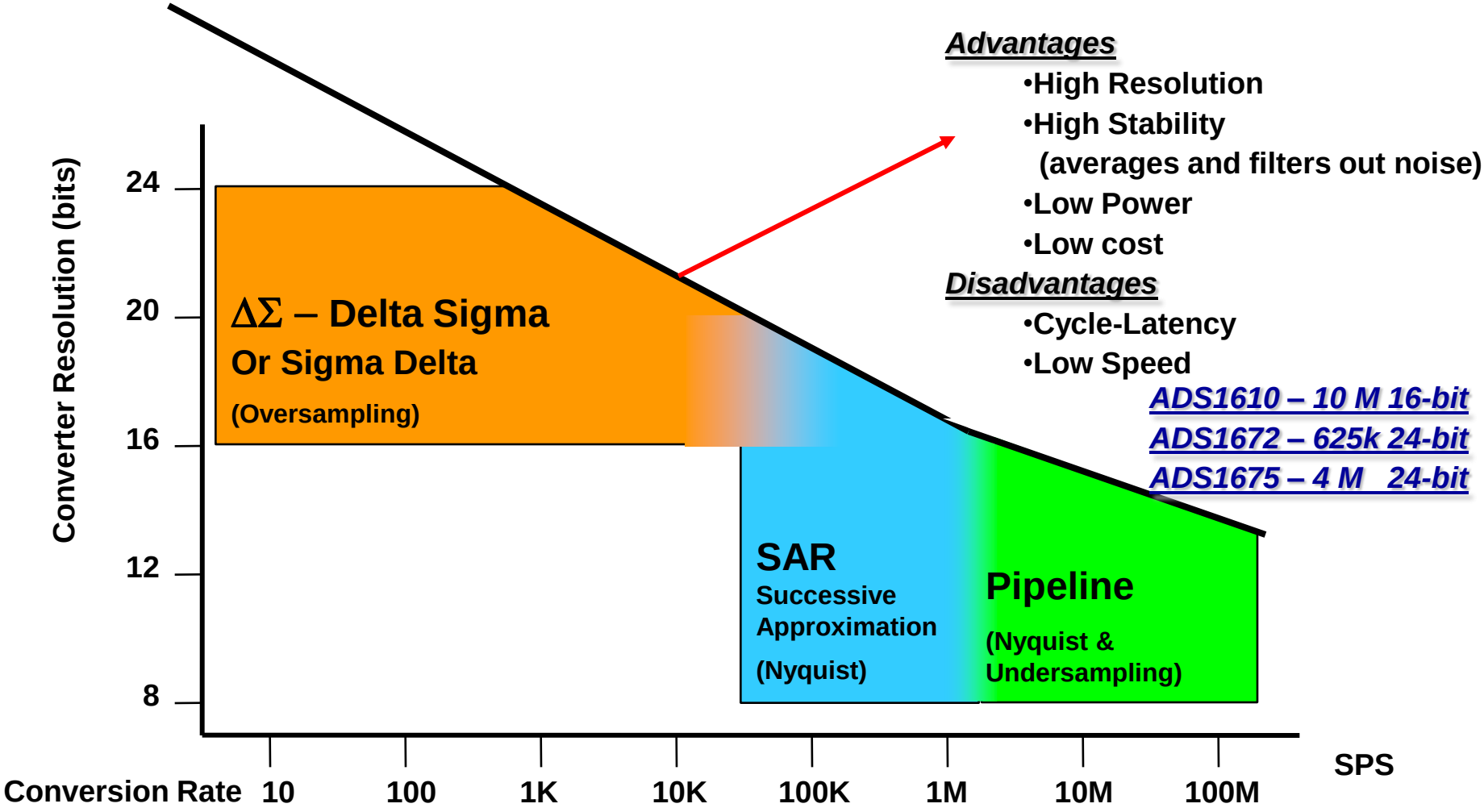
TI Technology Days 2010

Hochauflösende Delta Sigma Wandler

Funktion und Besonderheiten

Katharina Berberich

ADC Technologies - ΔΣ



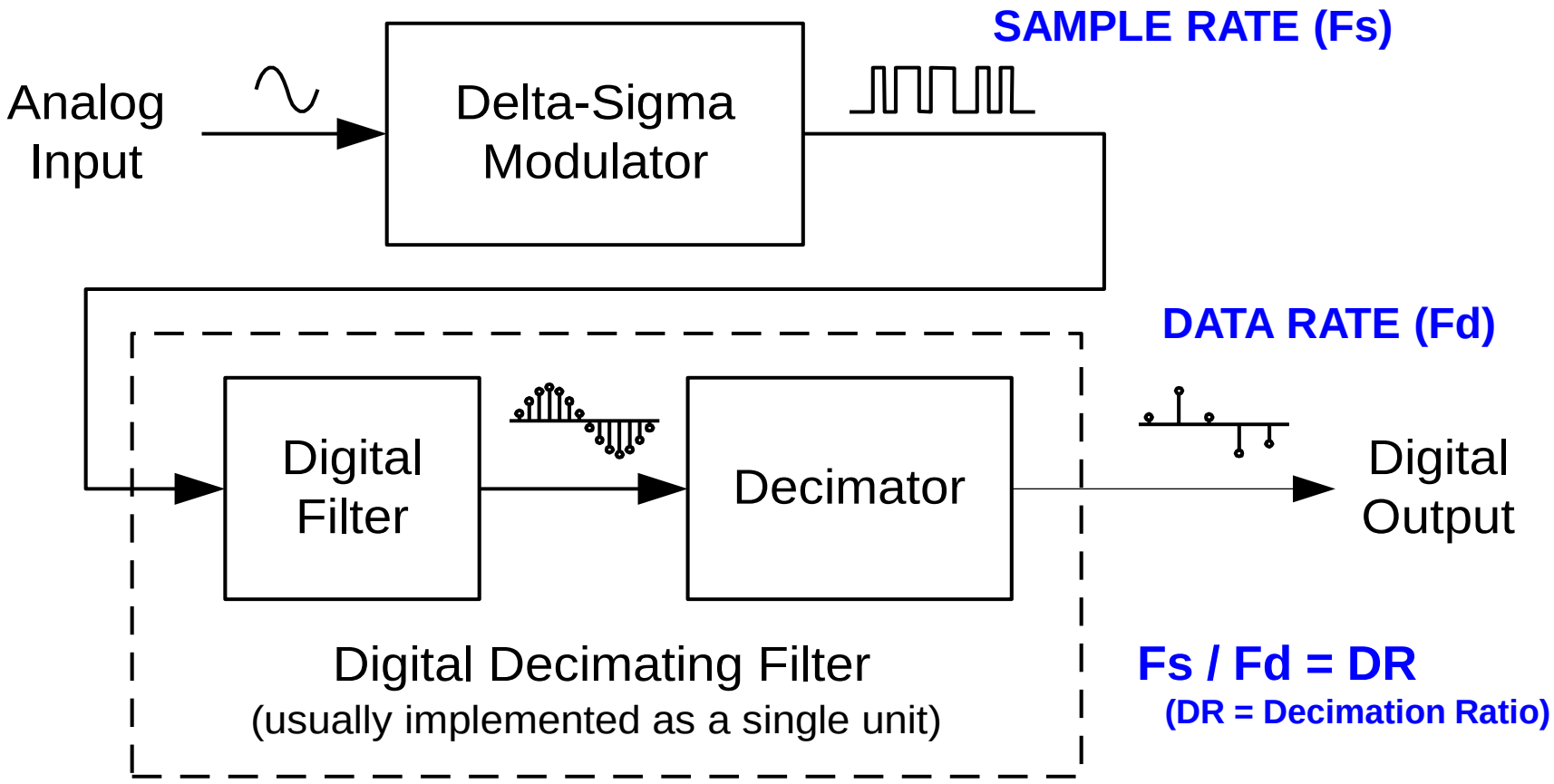
Typical Applications for ΔΣ Converters

- **High resolution up to 24bits**
  - **Sensors – Temperature, Pressure, Current, weightscales**
  - **Medical instruments**

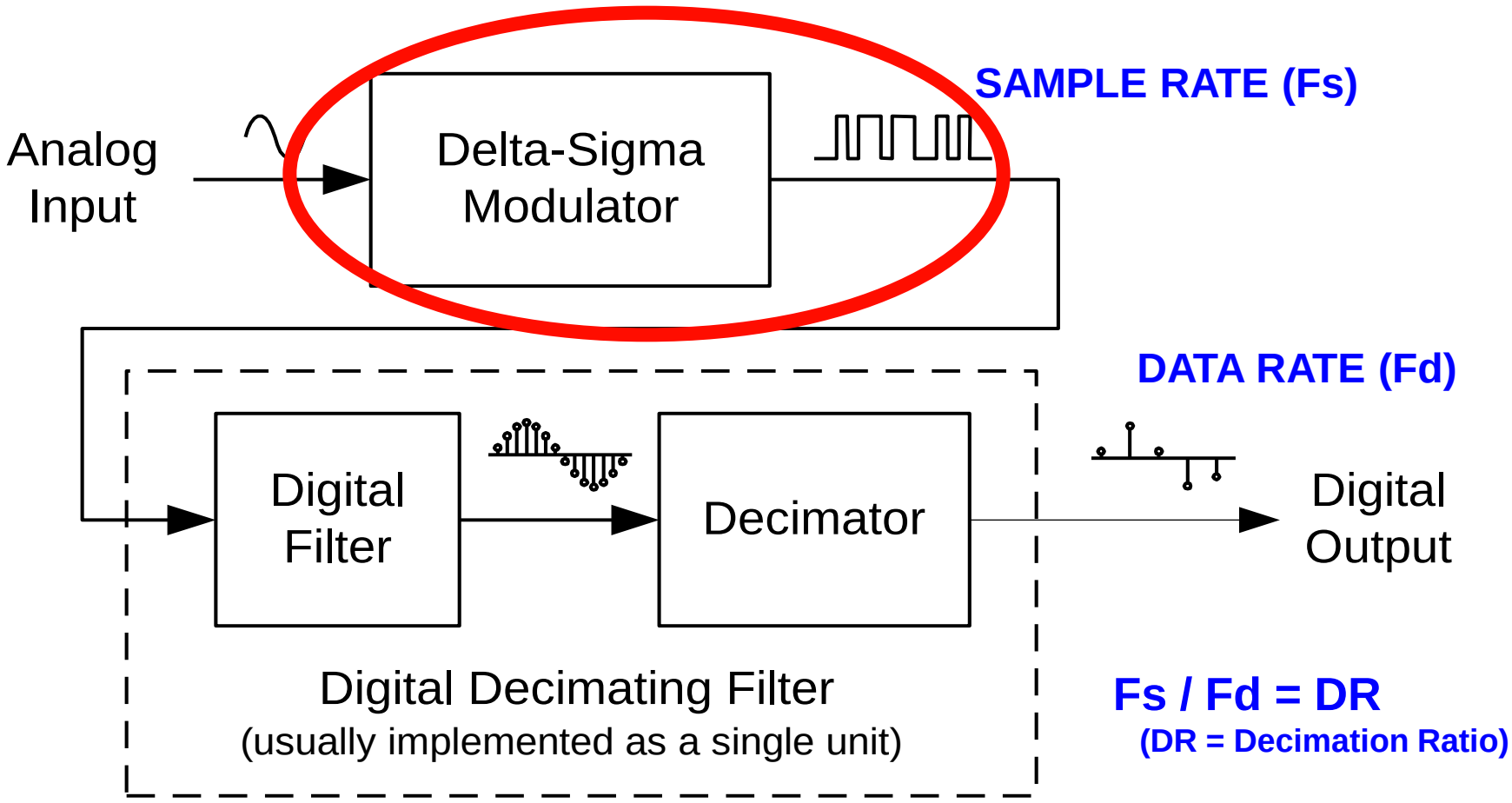
- **Audio – System clock range ~ 20 to 40 MHz**
  - **Optimized noise performance**
  - **Optimized filter in audio frequency for flatness**

- **High Speed**
  - **Has an Internal Digital Band-Pass Filter**
    - **Uses a band-pass topology instead of integrator**

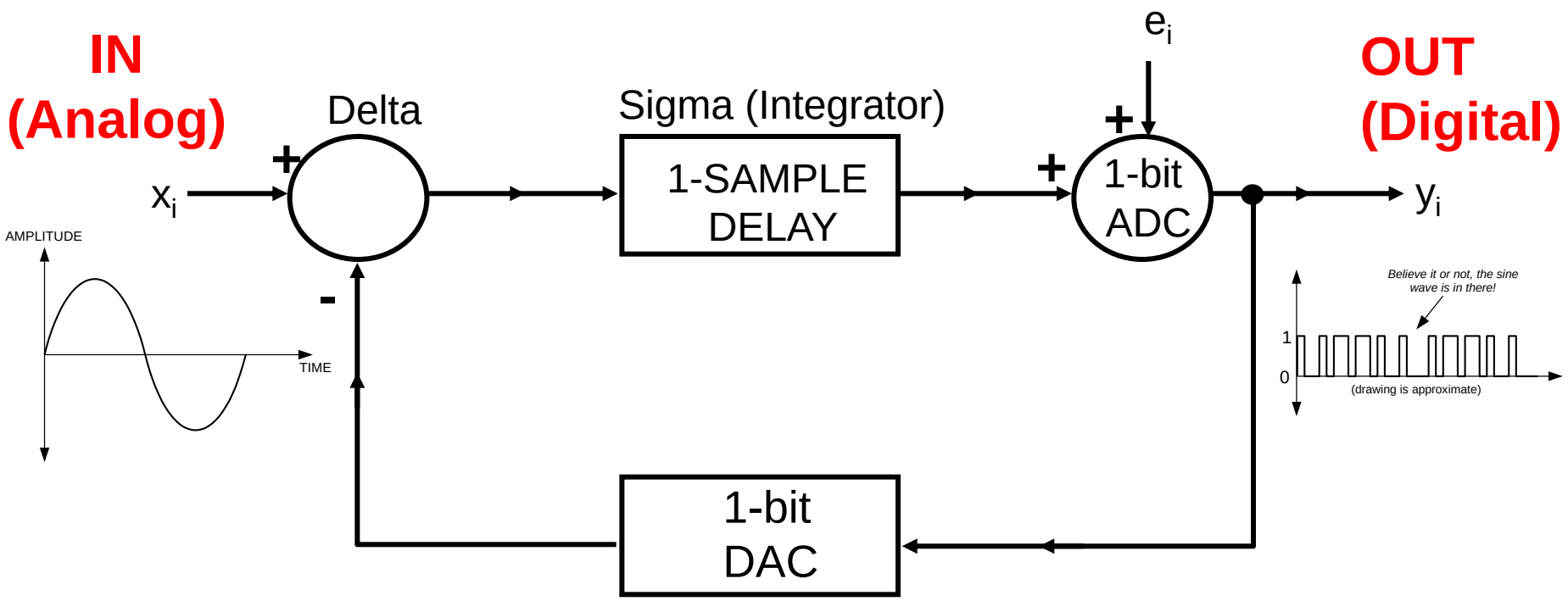
Delta-Sigma A/D Converters



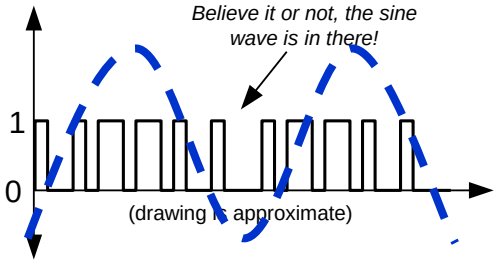
Modulator Output



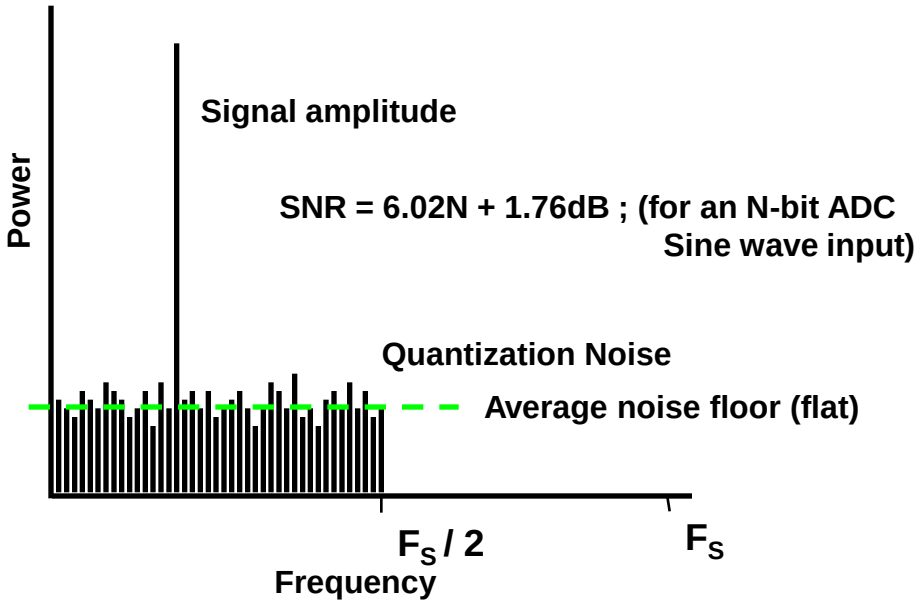
1st Order Delta-Sigma Modulator
TIME DOMAIN

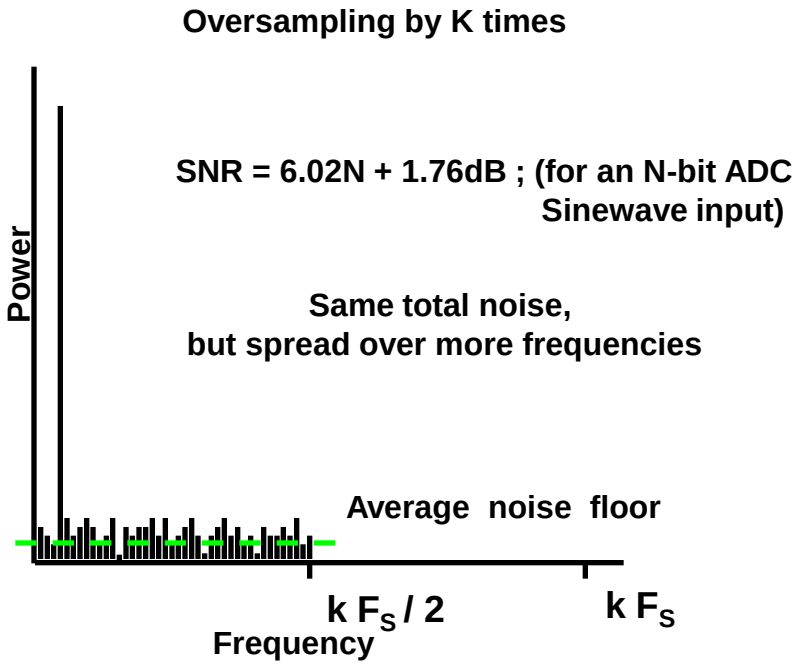


$$y_i = x_{i-1} + (e_i - e_{i-1})$$

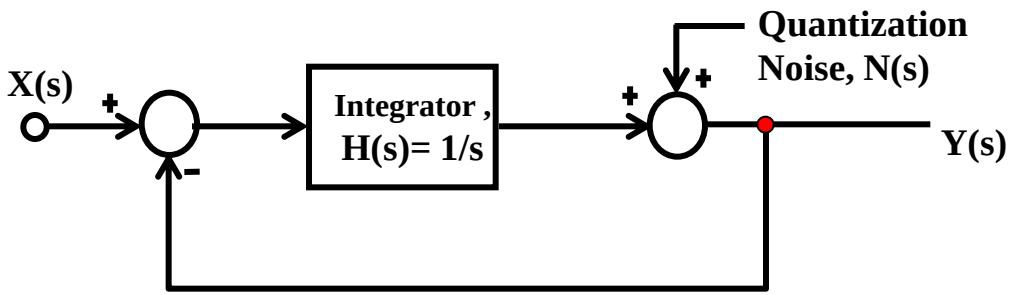


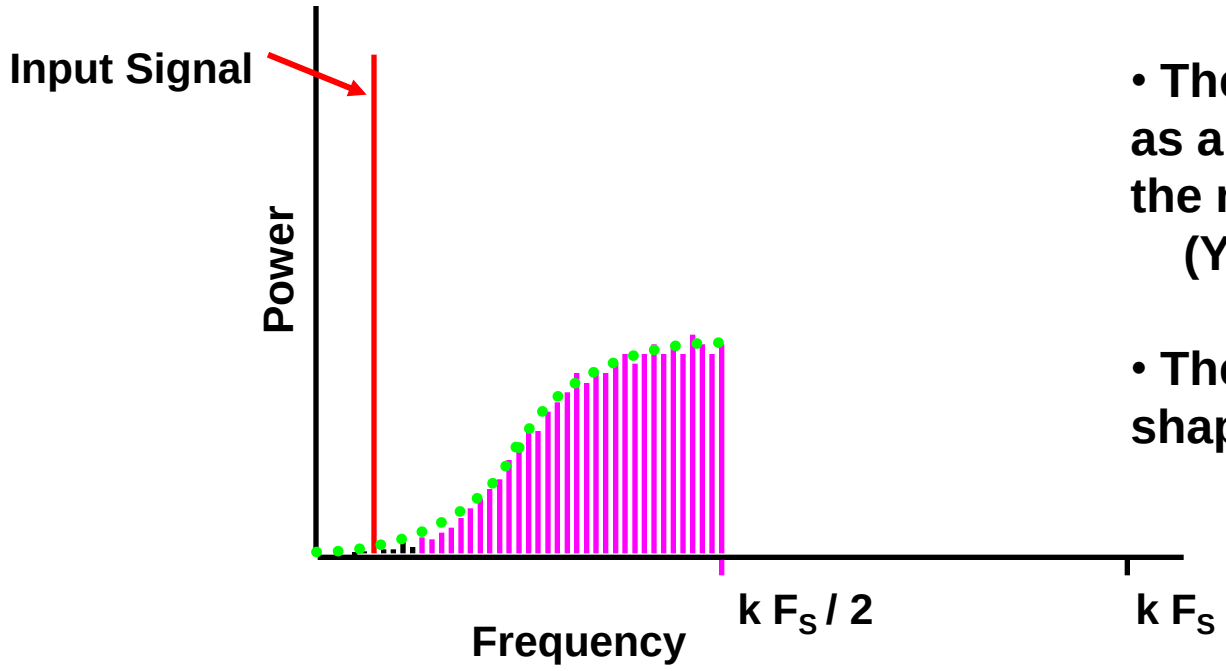
Oversampling





ΔΣ Modulator Frequency Domain



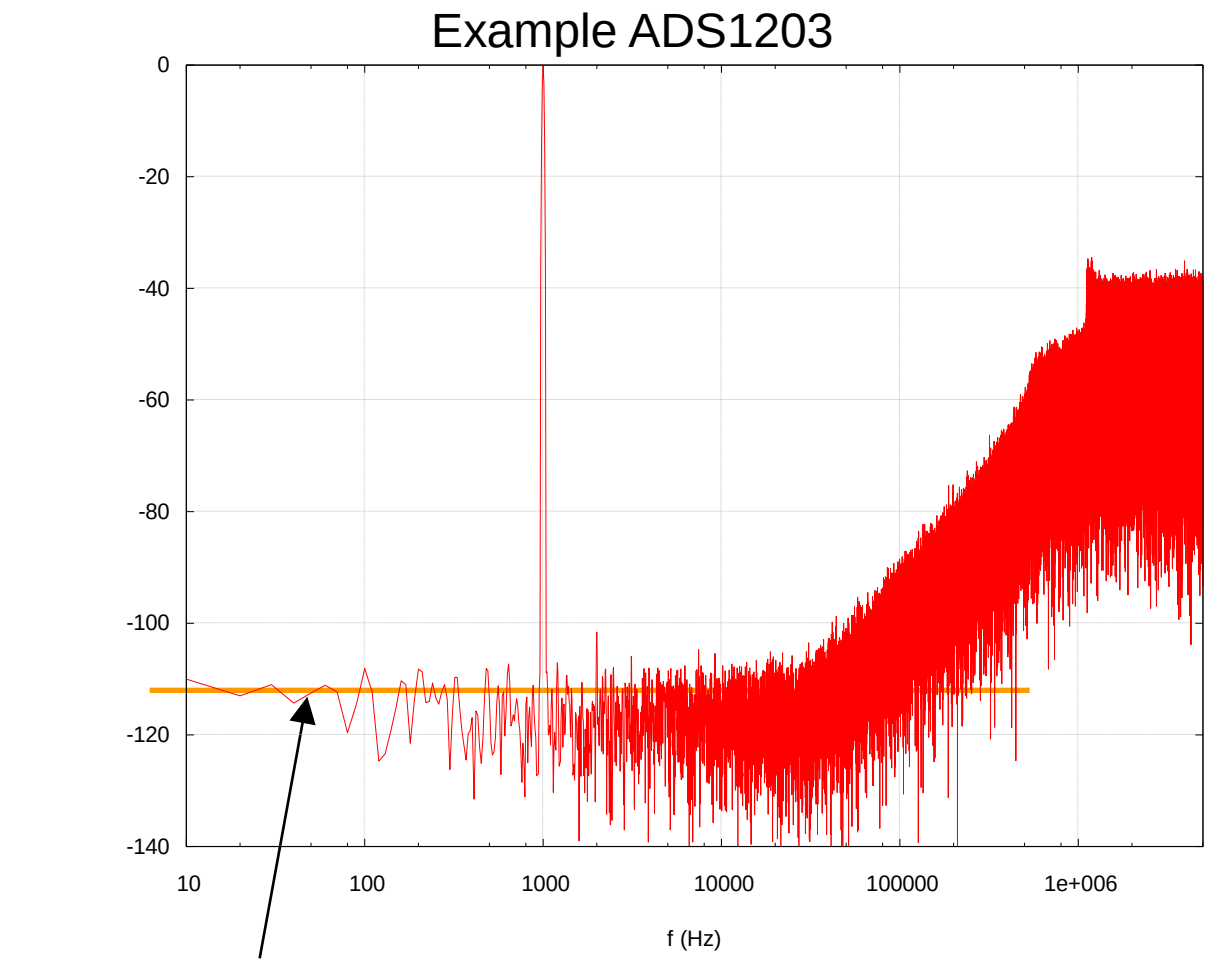


- The integrator serves as a low-pass filter to the signal.
  (Y(s)/N(s) = 1 / (s+1)

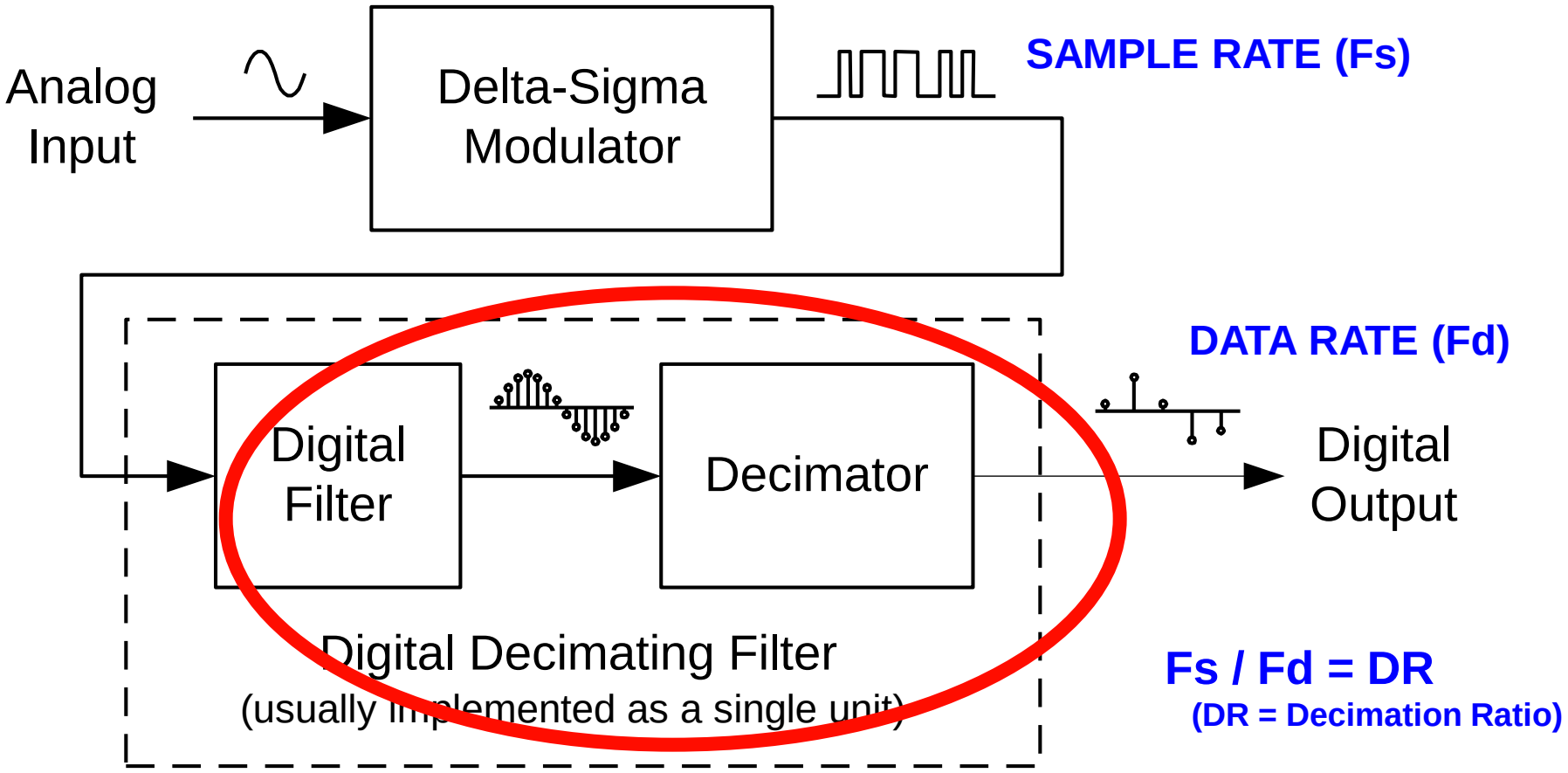
- The integrator serves as a high-pass filter to the noise.
  (Y(s)/N(s) = s / (s+1)

- The result is noise shaping

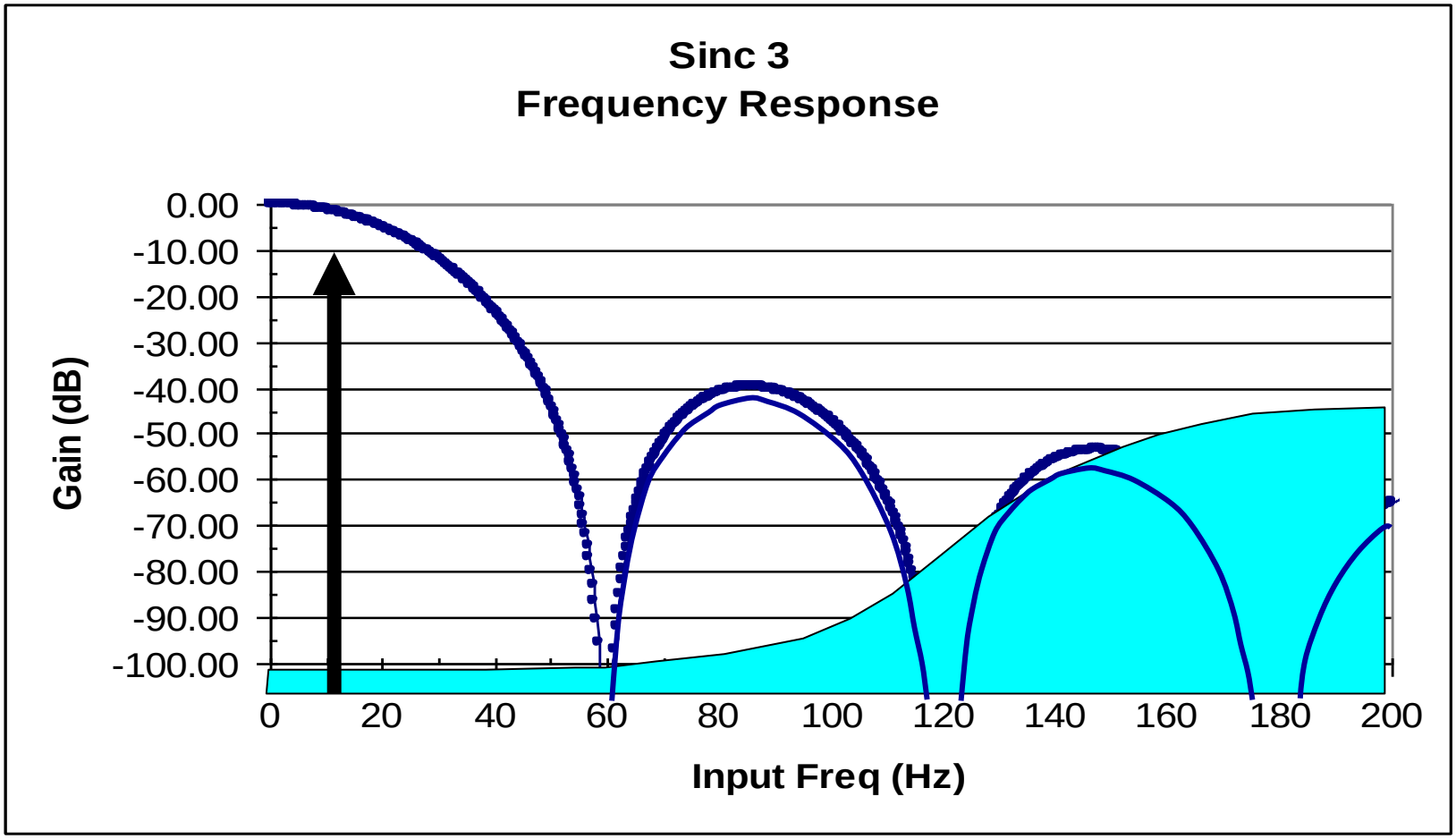
Quantization Noise



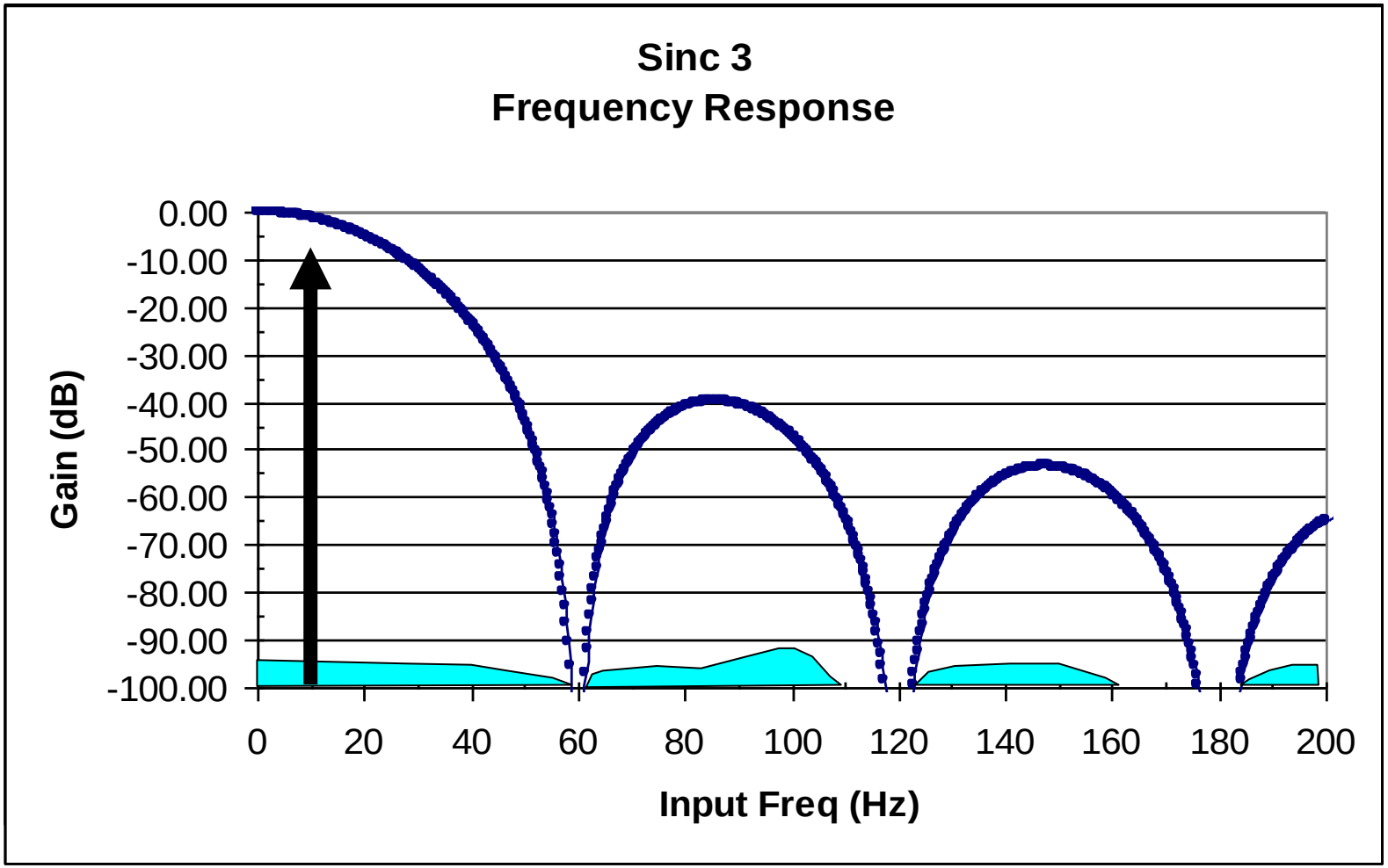
Delta-Sigma A/D Signal Path



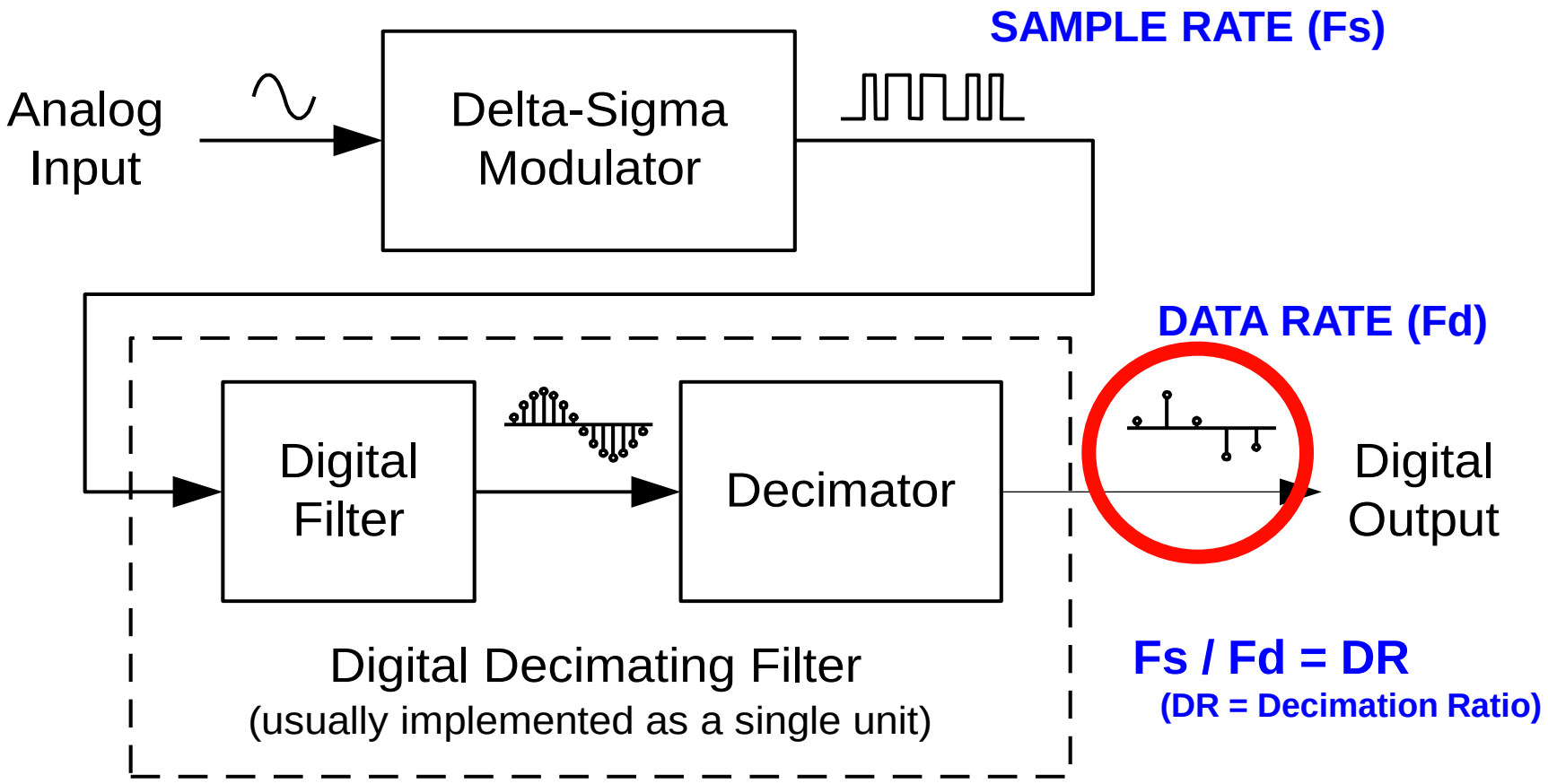
High Frequency Noise Reduction



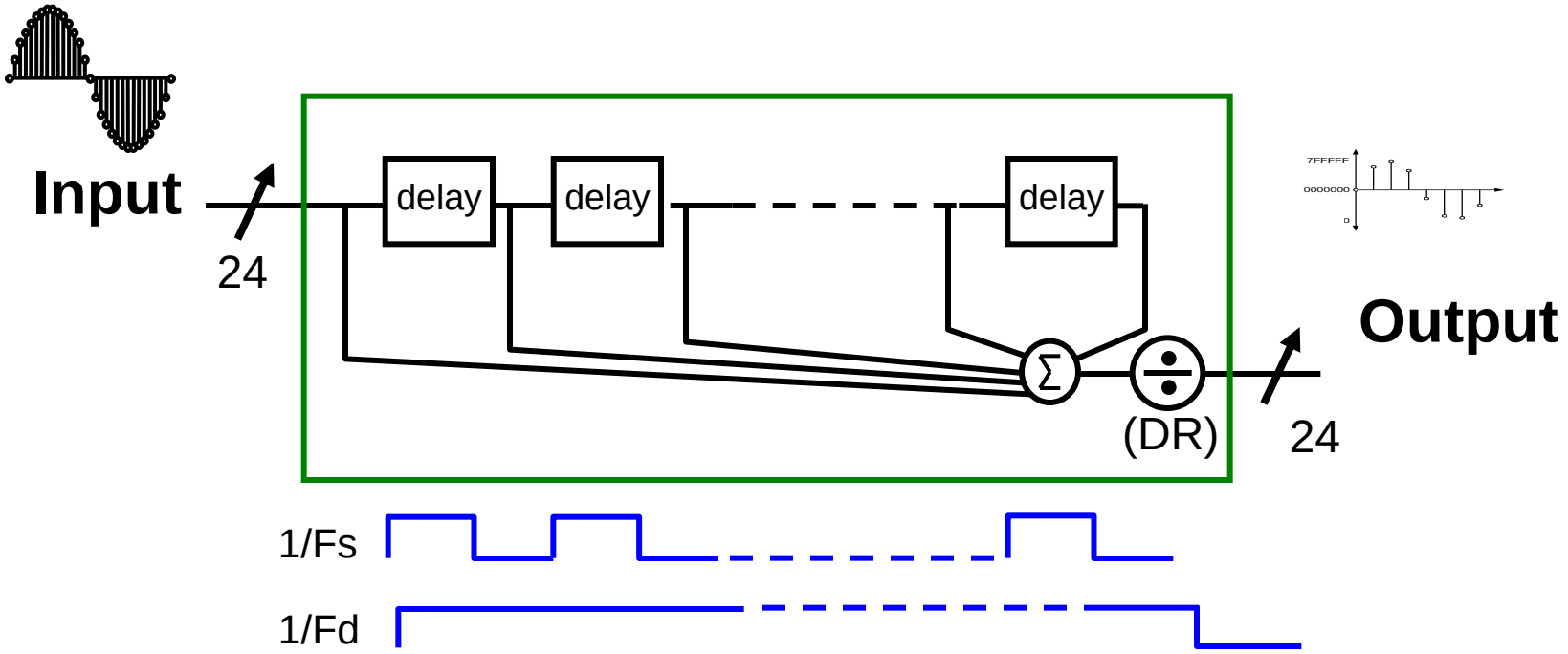
High Frequency Noise Reduction



Decimation Digital Filter



Decimator Function: Averager



Noise specifications

As found in the Delta Sigma converters datasheets

Noise specification in the ADS1259 datasheet

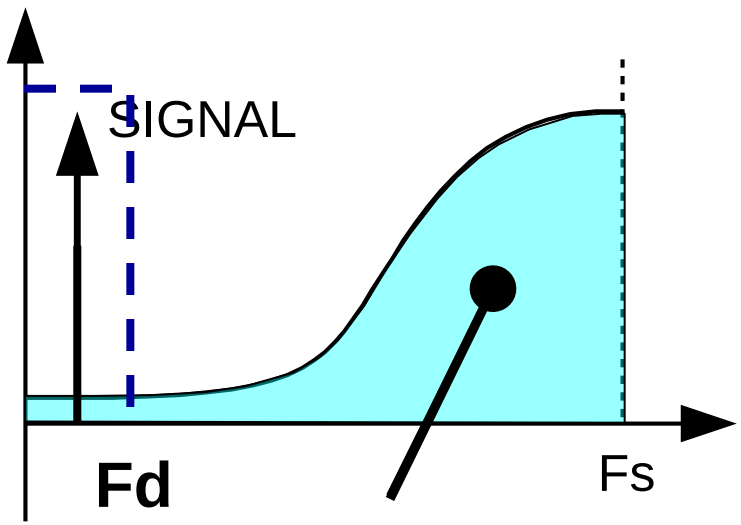
Table 1. Typical Noise Data vs Data Rate and Digital Filter(1)

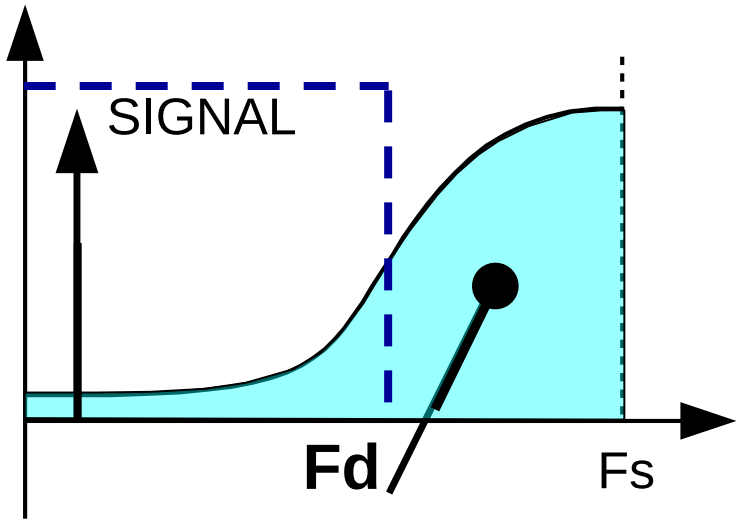
DATA RATE (SPS)	SAMPLE SIZE(2)	SINC^1 DIGITAL FILTER				SINC^2 DIGITAL FILTER			
		NOISE (μV_{RMS})	NOISE (μV_{PP})	ENOB (RMS)	NOISE-FREE BITS	NOISE (μV_{RMS})	NOISE (μV_{PP})	ENOB (RMS)	NOISE-FREE BITS
10	128	0.5	1.8	23.3	21.4	0.45	1.6	23.4	21.6
16.6	256	0.55	2.4	23.1	21.0	0.5	2	23.3	21.3
50	512	0.65	3.5	22.9	20.4	0.6	3	23.0	20.7
60	512	0.7	4	22.8	20.3	0.65	3.5	22.9	20.4
400	4096	1.4	9.5	21.8	19.0	1.2	8.3	22.0	19.2
1200	8192	2.3	17	21.1	18.2	2	14	21.3	18.4
3600	8192	3.9	32	20.3	17.3	3.4	27	20.5	17.5
14400	8192	6.2	50	19.6	16.6	(3)	(3)	(3)	(3)

(1) Noise data taken with shorted analog inputs and internal 2.5V reference using the circuit of Figure 63.
(2) Data sample sizes used for analysis.
(3) Same as sinc^1 mode.

Datarate vs. noise

$$Fs / Fd = DR = K$$



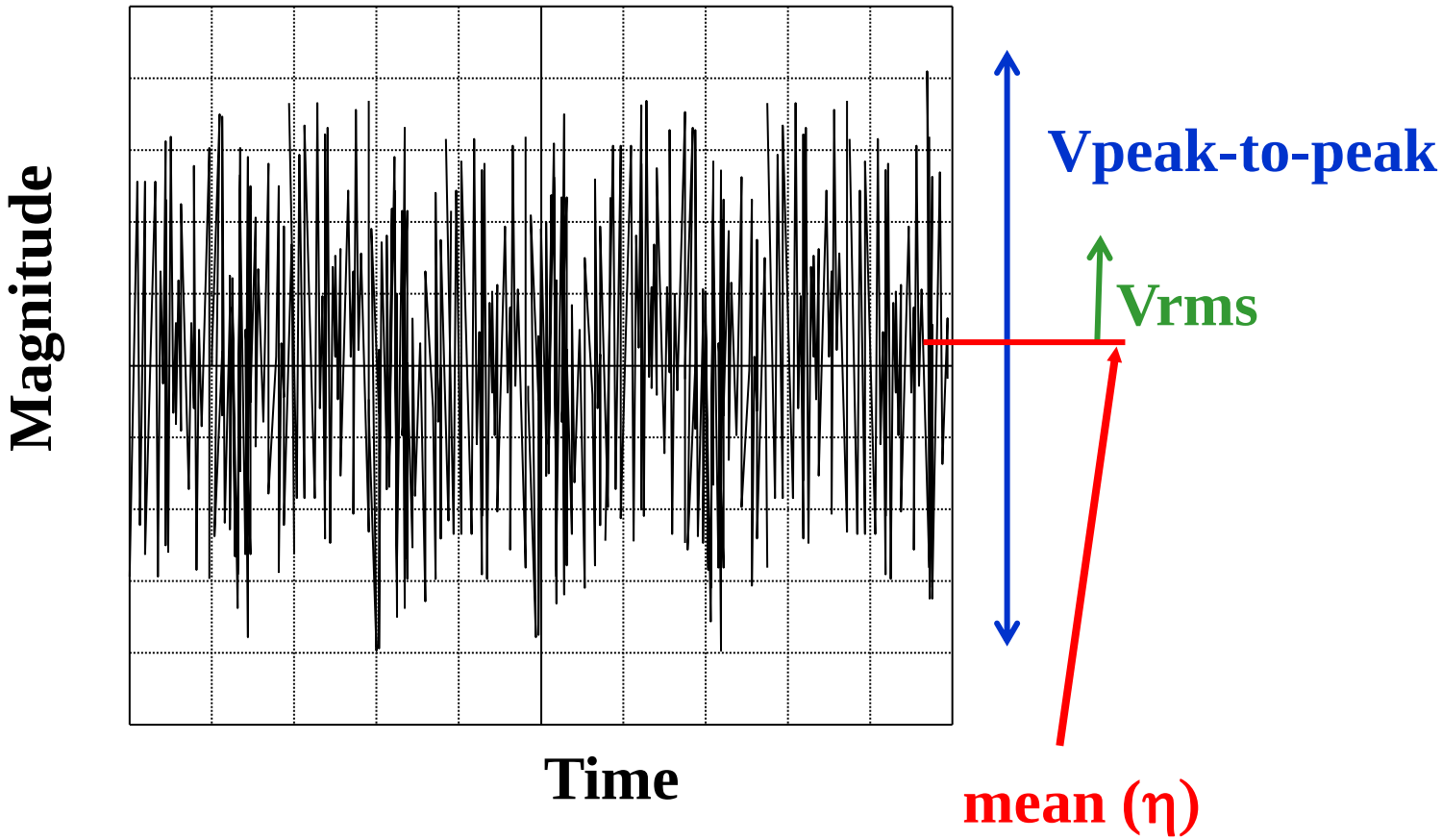


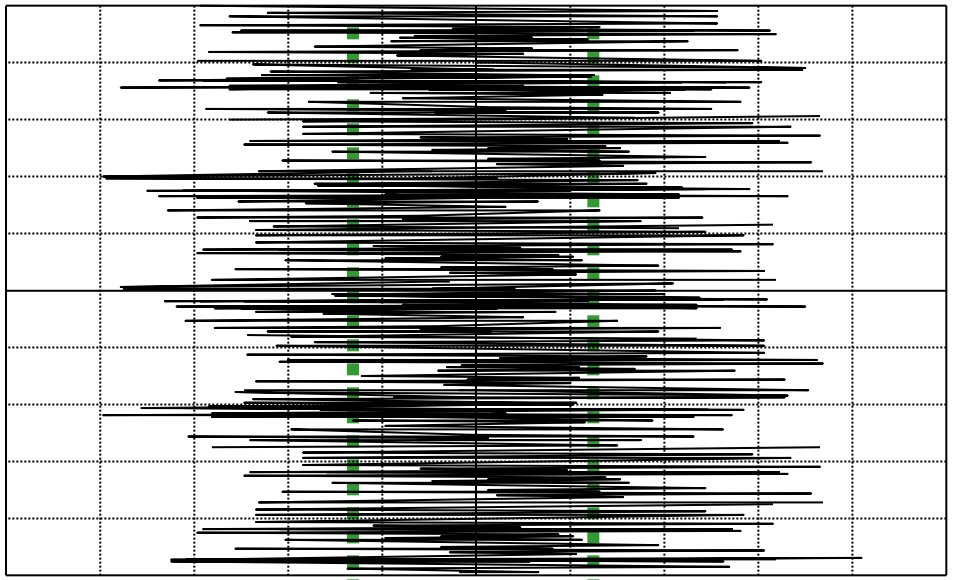
$DR_A > DR_B$

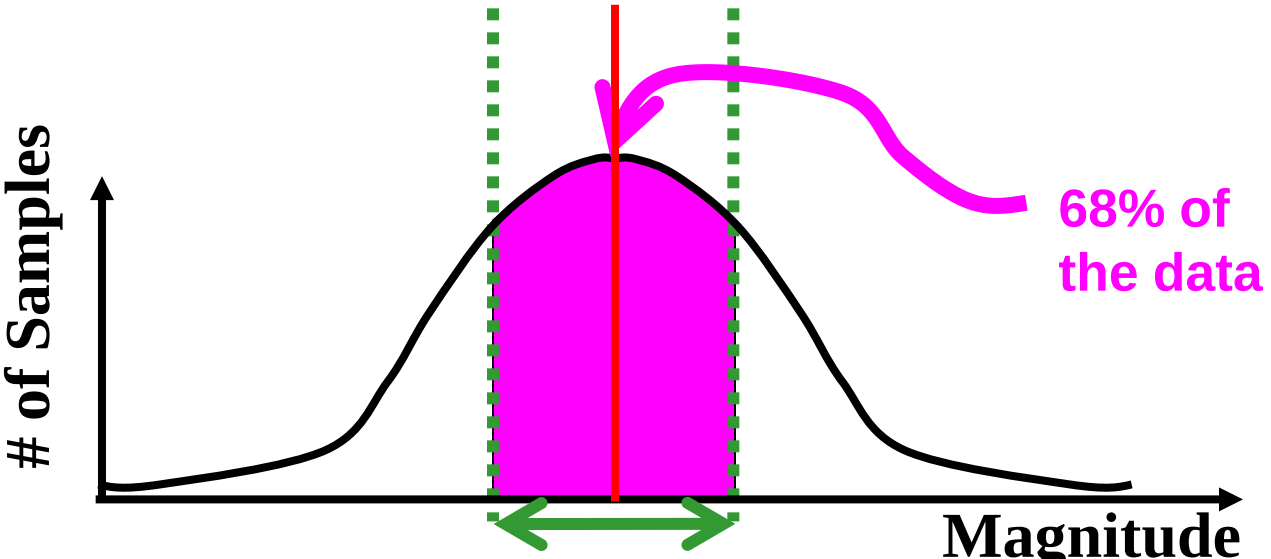
A.

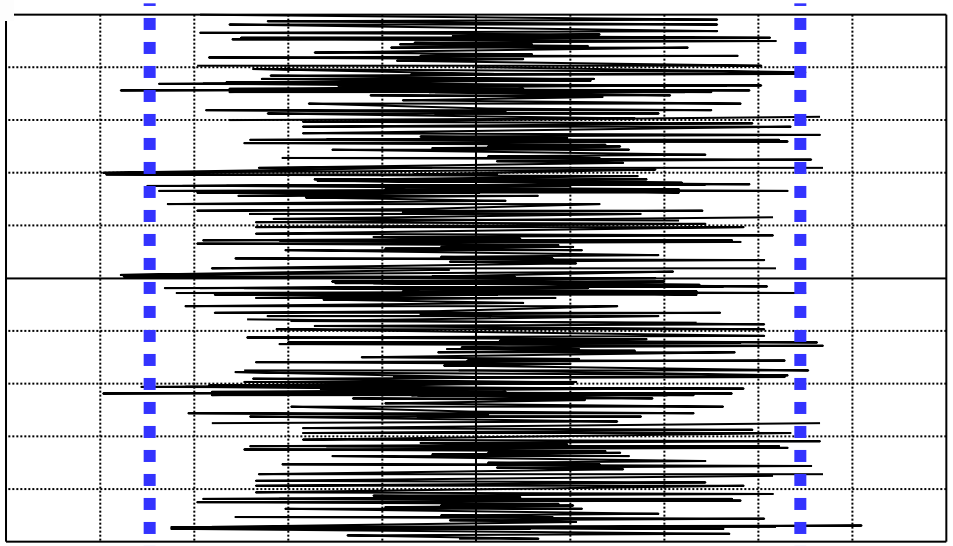
B.

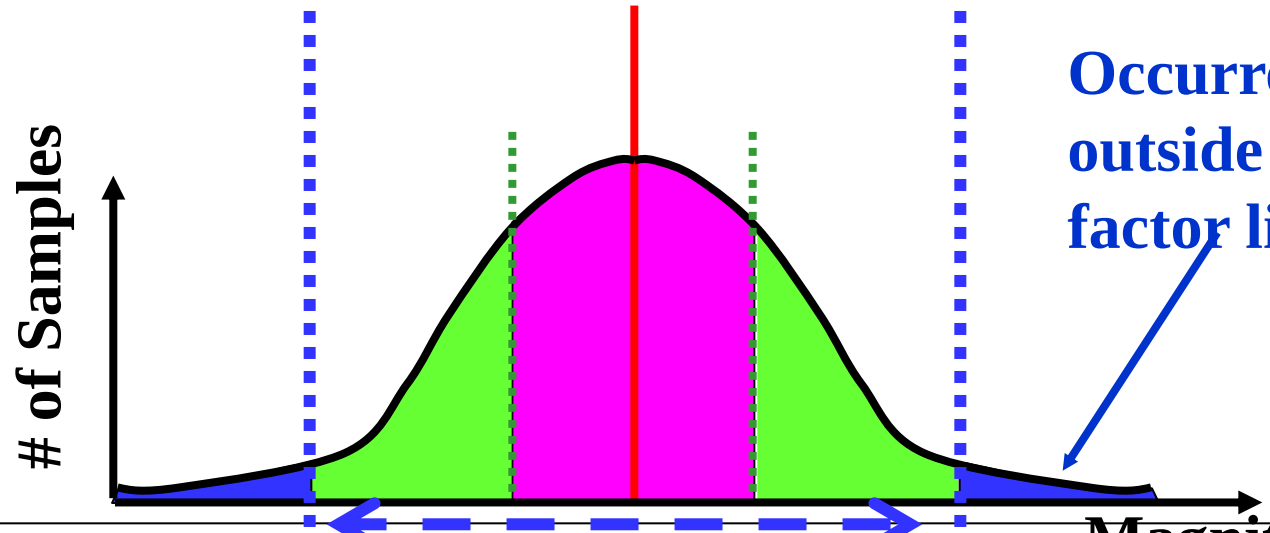
Scope Characteristics Noise






# of Samples
Magnitude
68% of the data
±RMS or
± one standard deviation




# of Samples
Occurrences outside the crest factor limits
Peak-to-peak
Magnitude

The Statistics of Noise

Crest Factor (CF)	Percentage of Occurrences Inside Limits	Percentage of Occurrences where Peaks are Exceeded
2.6	99%	1%
3.3	99.9%	0.1%
3.9	99.99%	0.01%
4.4	99.999%	0.001%
4.9	99.9999%	0.0001%

Industry Standard

Stable to 5 Display Digits

$$Noise_{peak\text{-}to\text{-}peak} = 2 \times Noise_{rms} \times Crest\ Factor$$

The Statistics of Noise

Crest Factor (CF)	Crest Factor (BCF,bits)	Percentage of Occurrences where Peaks are Exceeded
2.6	2.38	1%
3.3	2.72	0.1%
3.9	2.94	0.01%
4.4	3.13	0.001%
4.9	3.29	0.0001%

$$\text{Noise}_{\text{peak-to-peak volts}} = 2 \times \text{Noise}_{\text{rms}} \times \text{Crest Factor}$$

$$\text{Noise}_{\text{peak-to-peak bits}} = \text{Noise}_{\text{rms bits}} - (\text{Crest Factor in bits})$$

Noise specification in the ADS1259 datasheet

Table 1. Typical Noise Data vs Data Rate and Digital Filter(1)

DATA RATE (SPS)	SAMPLE SIZE(2)	SINC^1 DIGITAL FILTER				SINC^2 DIGITAL FILTER			
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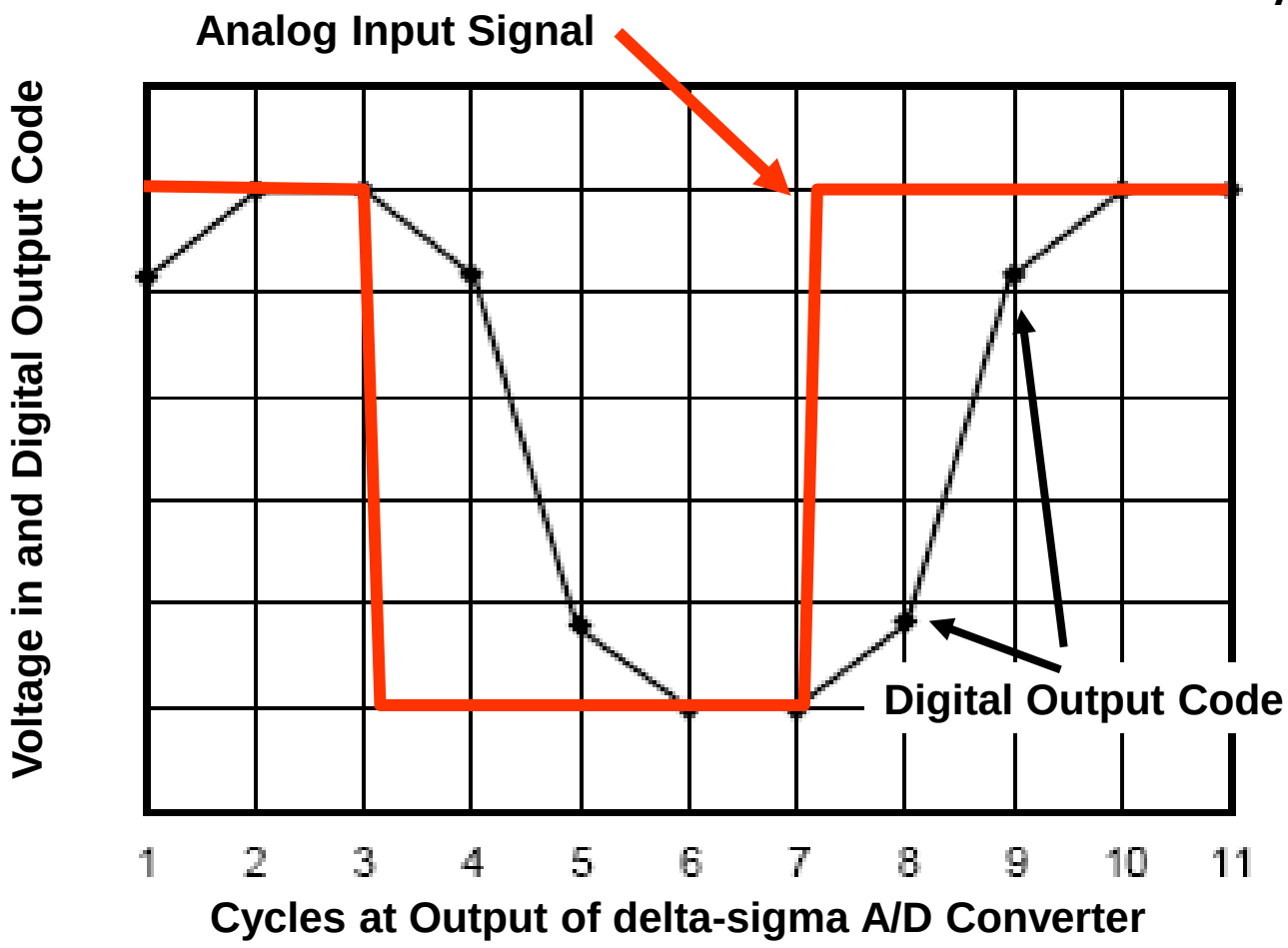
14400	8192	6.2	50	19.6	16.6	(3)	(3)	(3)	(3)

(1) Noise data taken with shorted analog inputs and internal 2.5V reference using the circuit of Figure 63.
(2) Data sample sizes used for analysis.
(3) Same as sinc^1 mode.

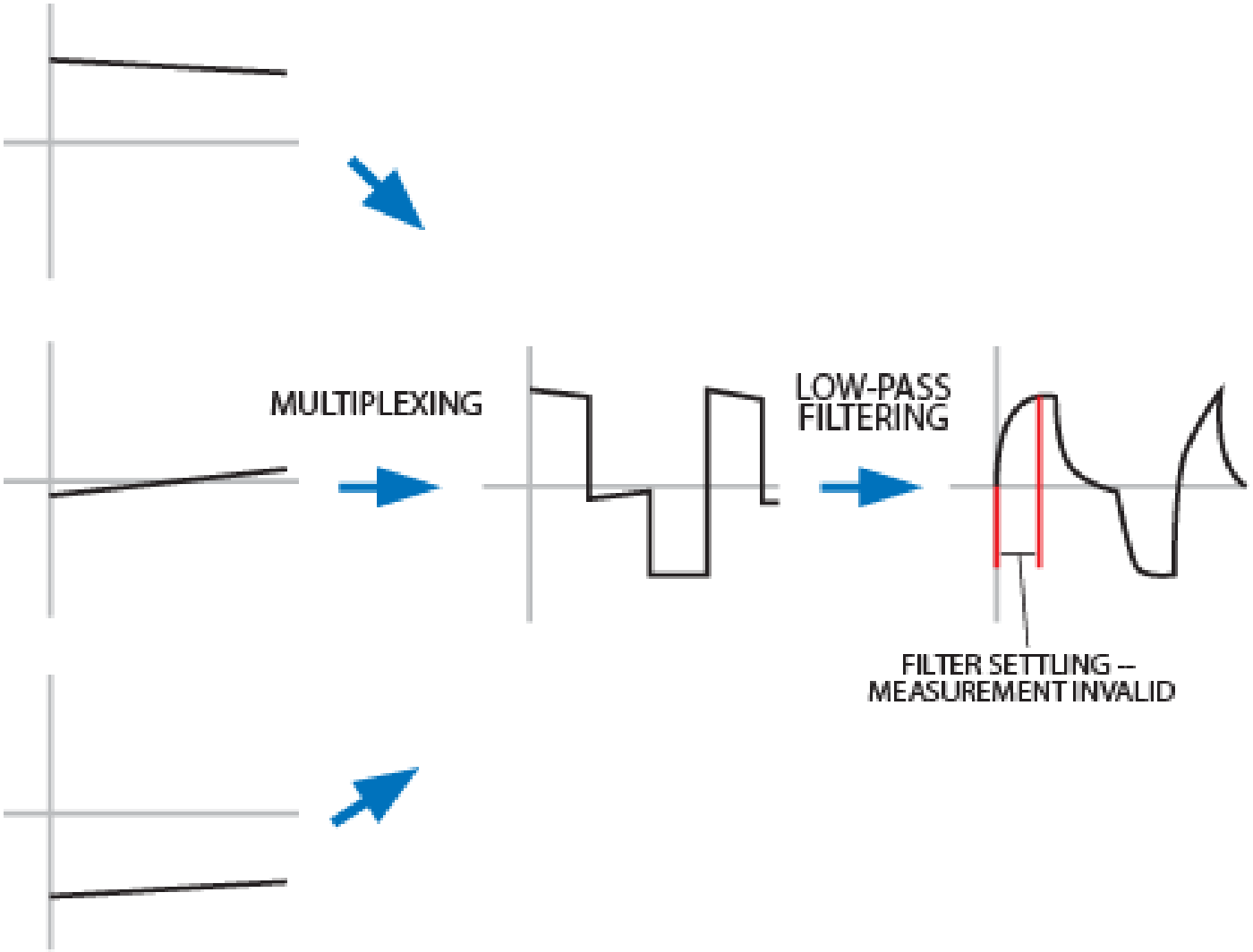
Filter

Settling Time

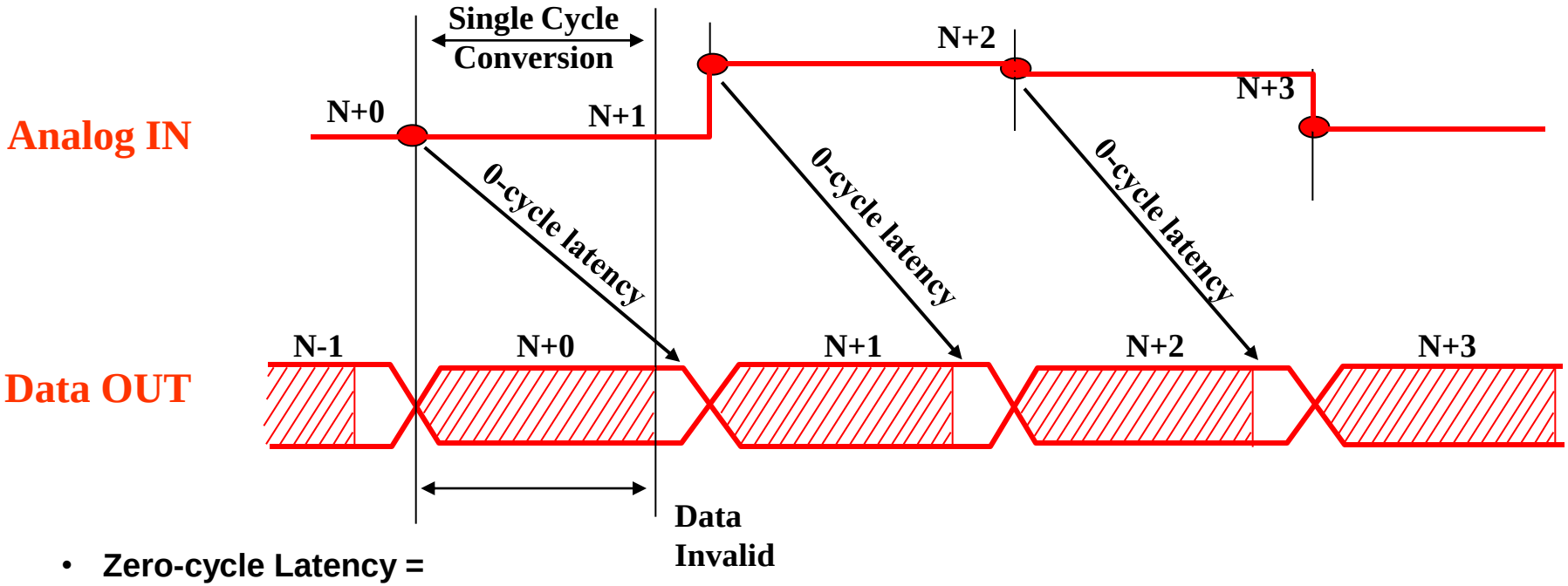
ADS1211



The effect of settling time

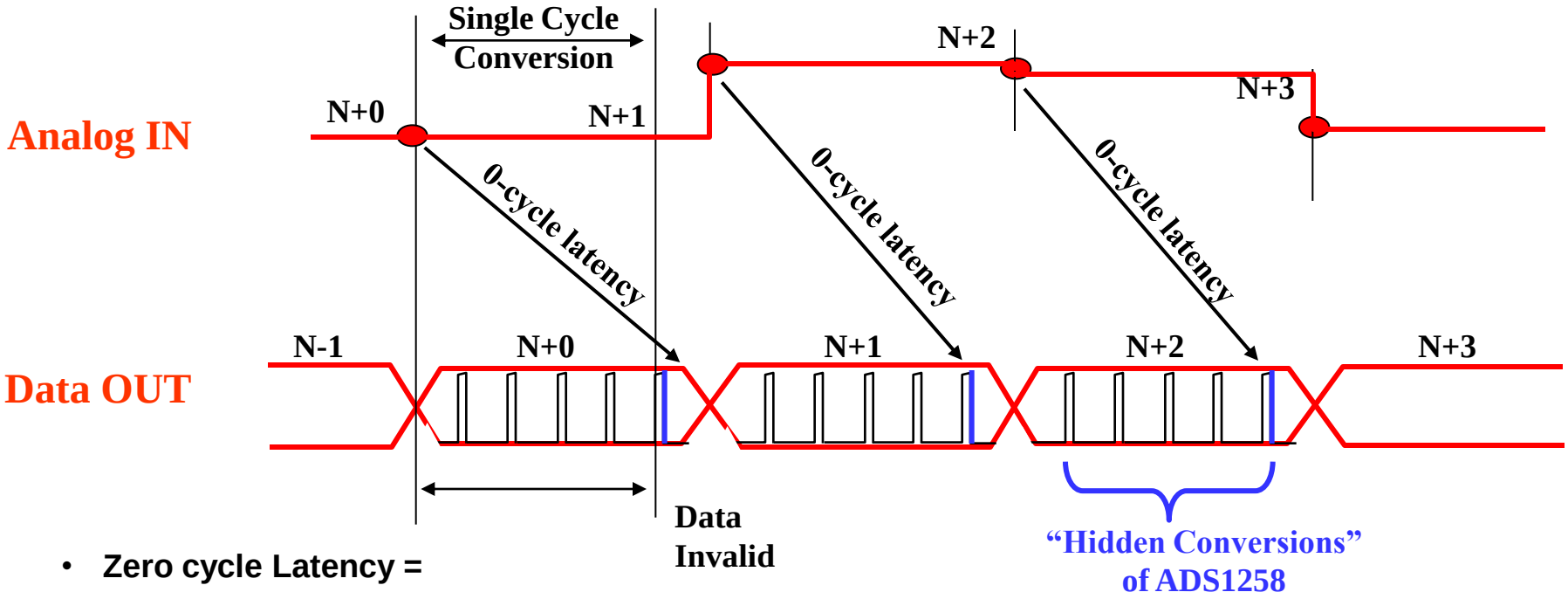


Zero cycle Latency



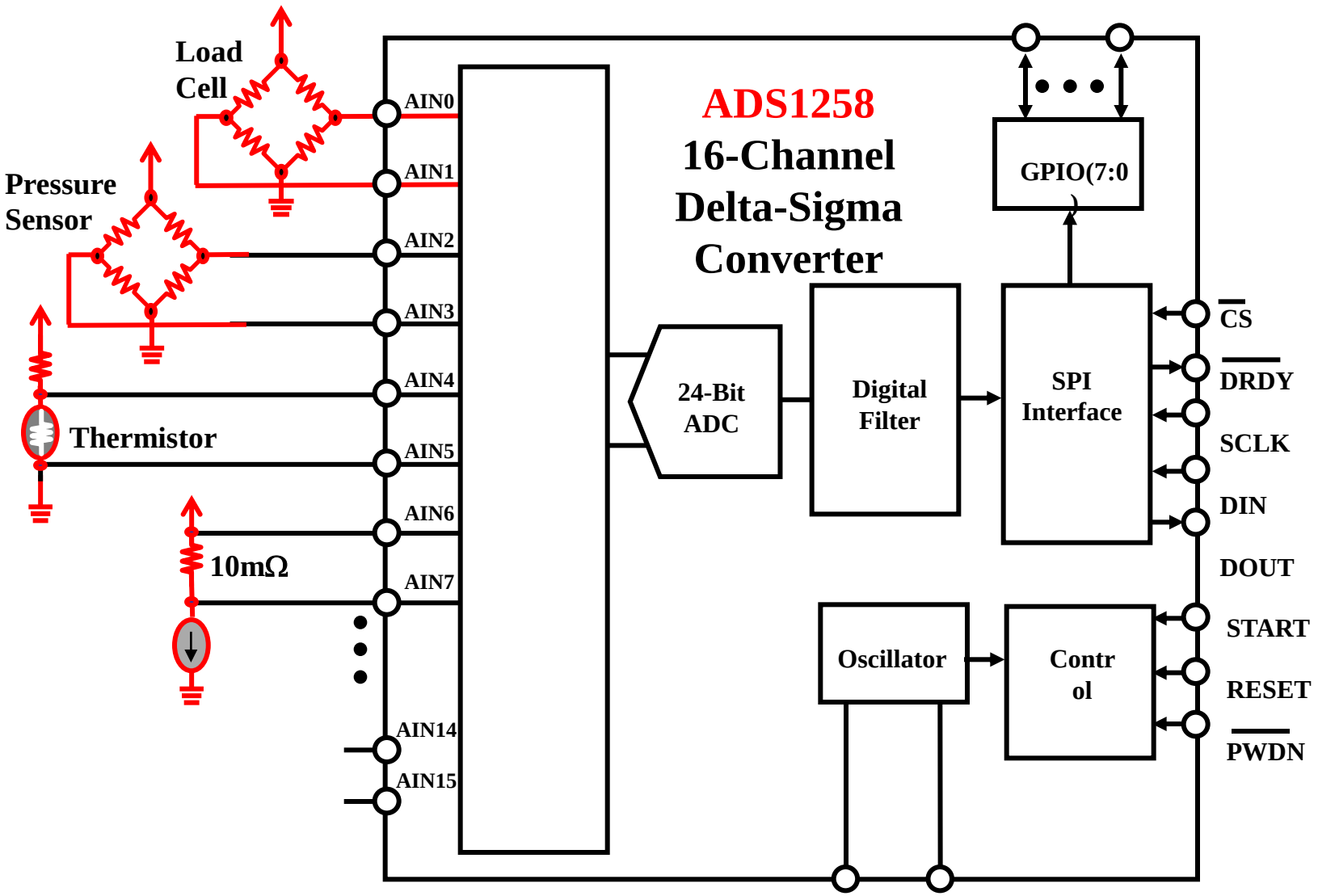
- Zero-cycle Latency =
  - Zero latency
  - Single cycle conversion
  - Single cycle settling
  - No Latency

Zero cycle Latency

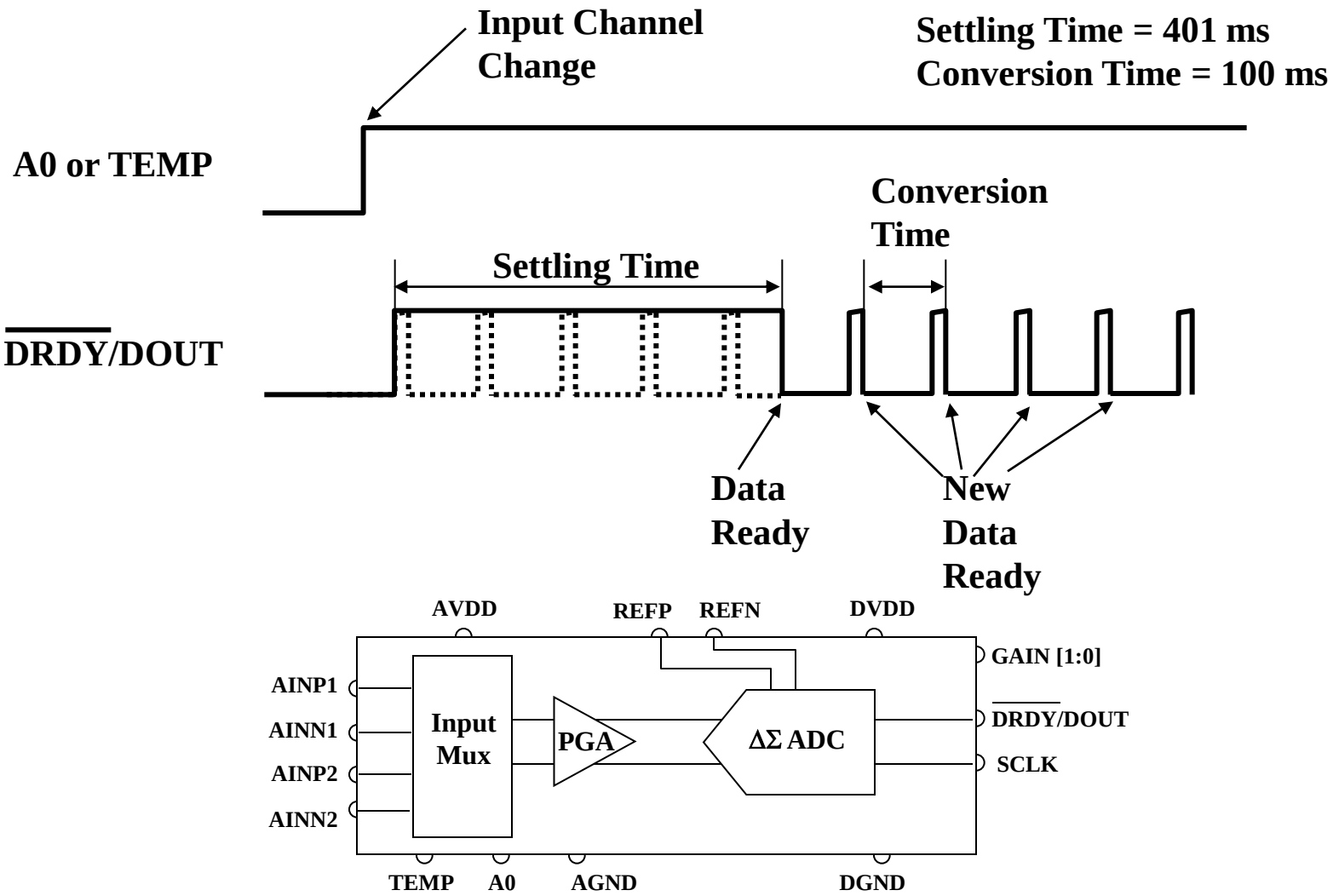


- Zero cycle Latency =
  - Zero latency
  - Single cycle conversion
  - Single cycle settling
  - No Latency

Zero Latency in Mux Applications

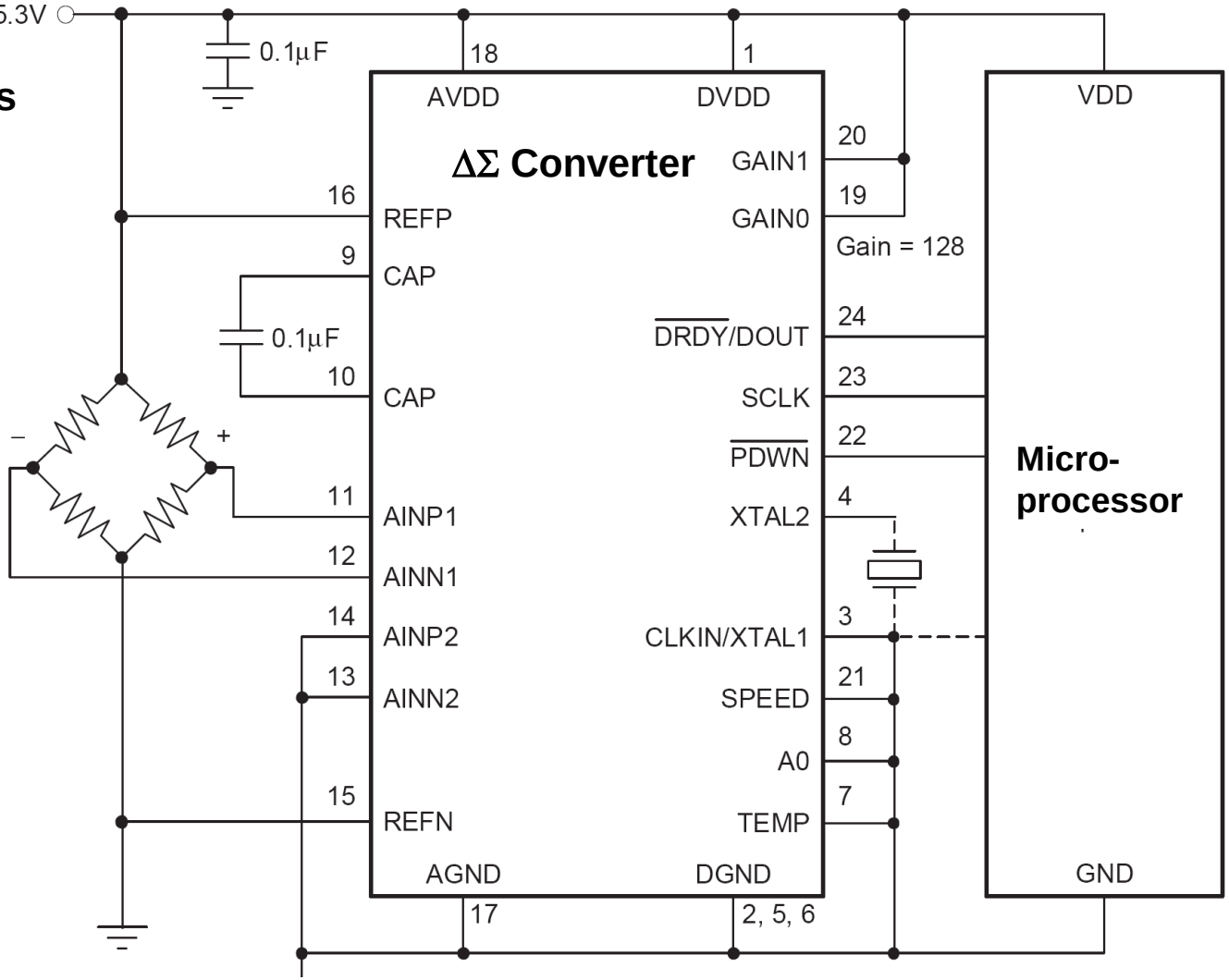


Variable Cycle-Latency ADS1232



ADS1232 Pressure Sensing

- **Zero-latency when Mux channel changes**
- **Internal Temp Sensor**
- **Internal or External Oscillator**
- **Internal Multiplexer**



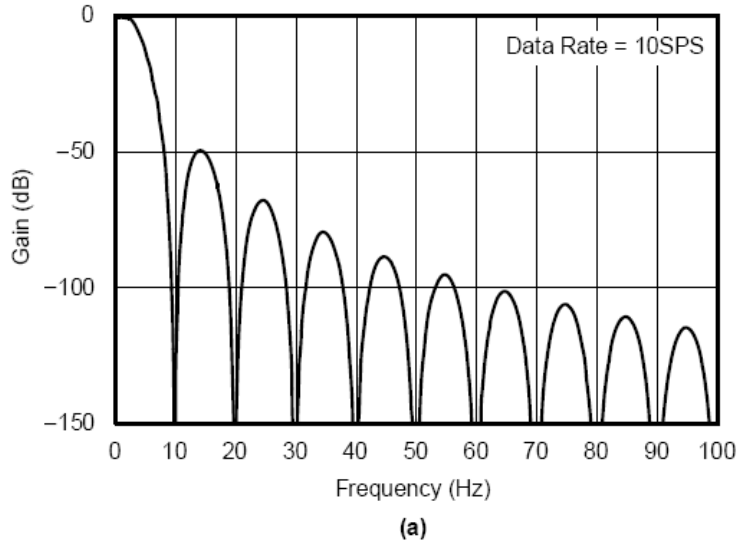
Types of Filters

Delta-Sigma (ΔΣ) ADCs

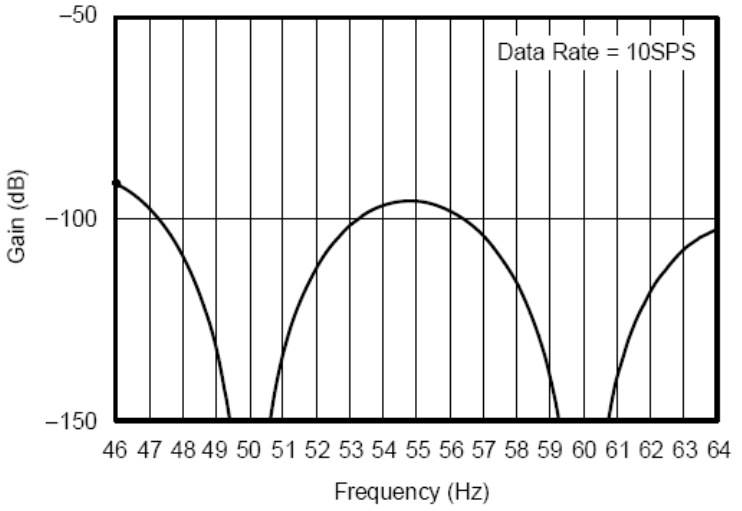
'Ultra' Precision Delta-Sigma Parts :

Sinc$^{(x)}$ Filter Response

- High Rejection @ Notches
- Trade-off data rate vs accuracy
  - slow @ high-accuracy
- Trade-off settling time vs accuracy
  - 1 to x settling cycles
    - fixed and programmable
- Programmable & Fixed Filters



(a)



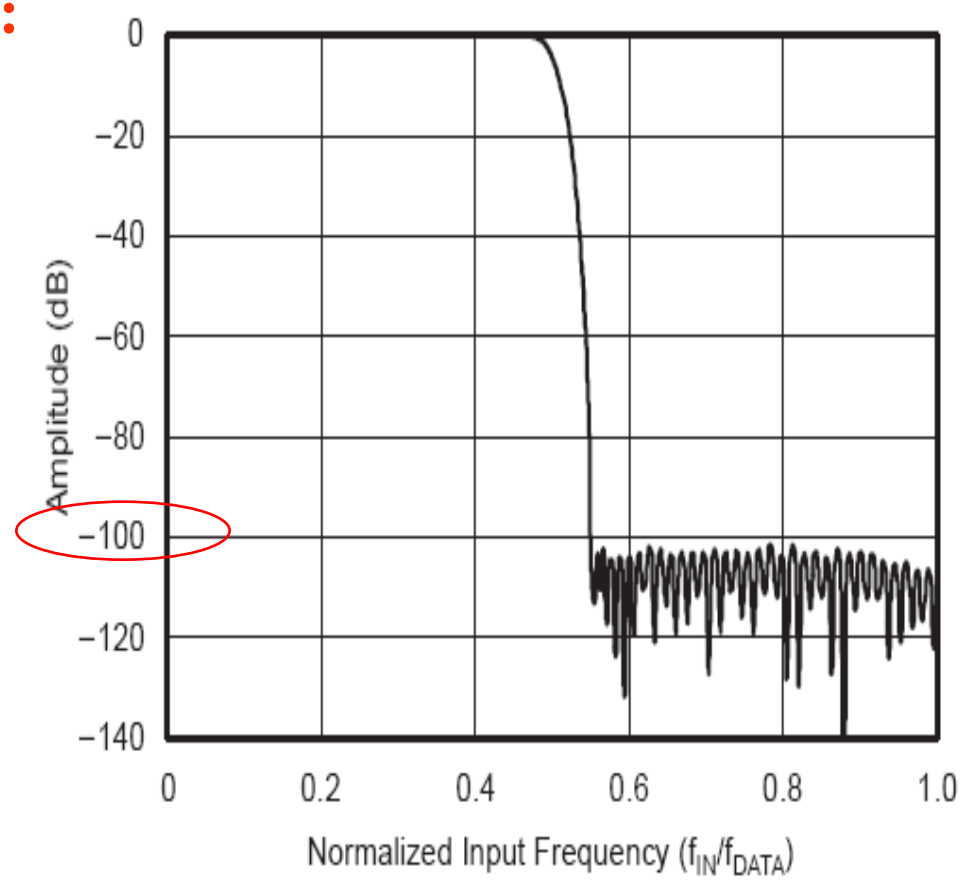
(b)

Delta-Sigma (ΔΣ) ADCs

High Speed Delta-Sigma Parts:

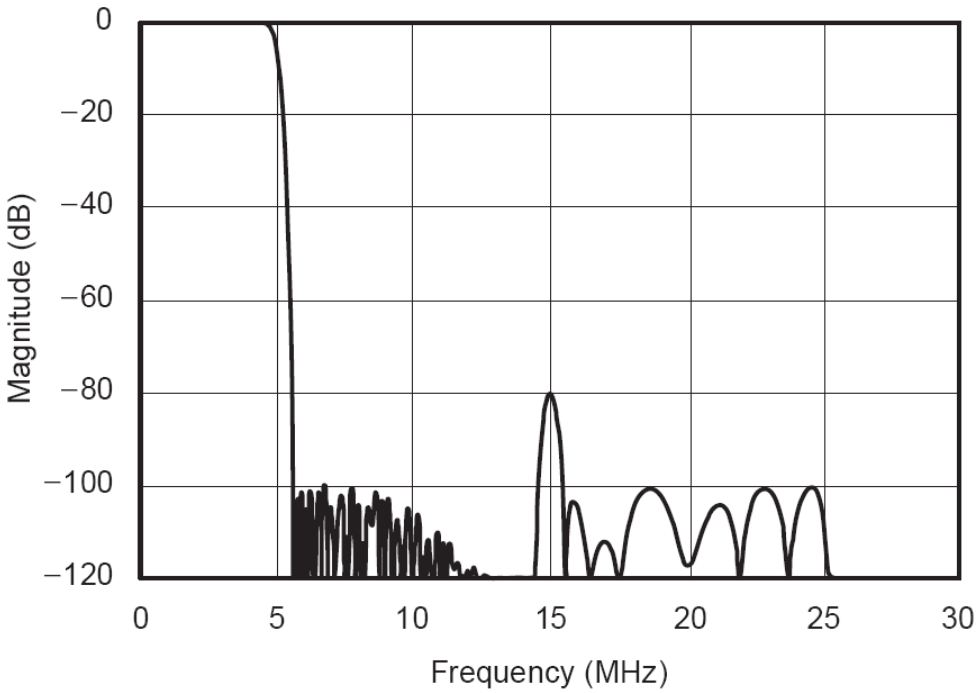
Linear FIR Filter Response

- Flat Passband to DR/2
- 'Brick Wall Filter'
- Low Pass-band Ripple
  - Long Settling Times

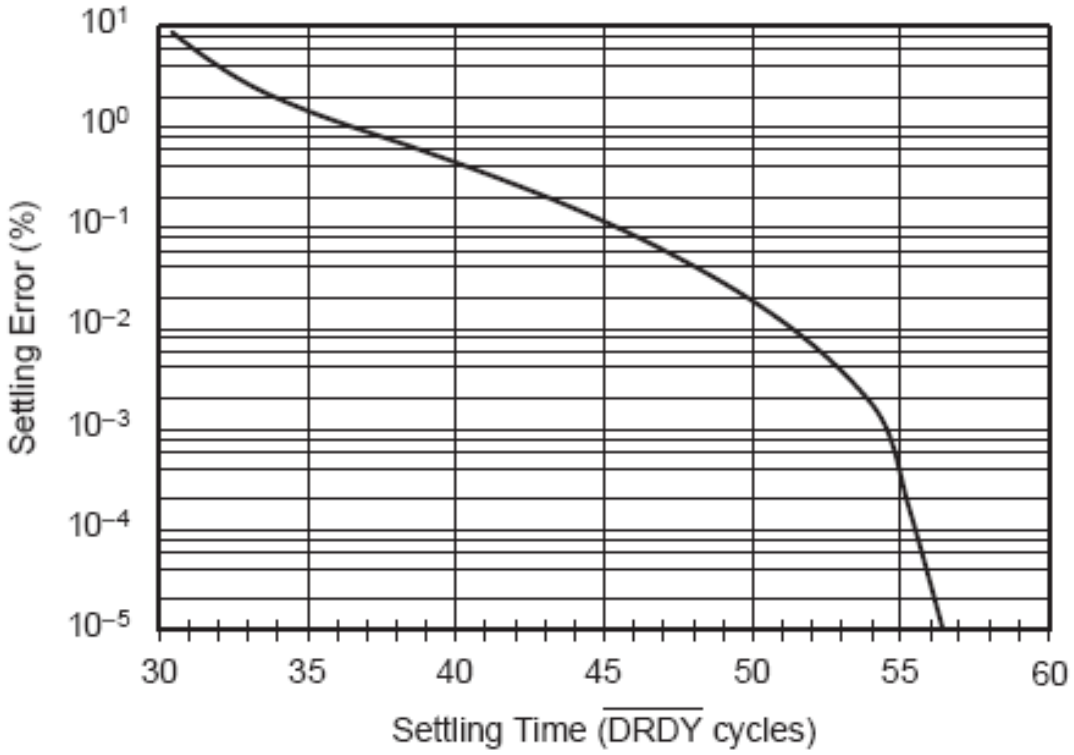


ADS1610 Characteristics

- High-Speed, Wide Bandwidth ΔΣ ADC
- 10 MSPS Output Data Rate
- 4.9 MHz Signal Bandwidth (linear phase)



ADS1610 Settling Time



Maximum $\overline{\text{DRDY}}$ frequency = 10 MHz

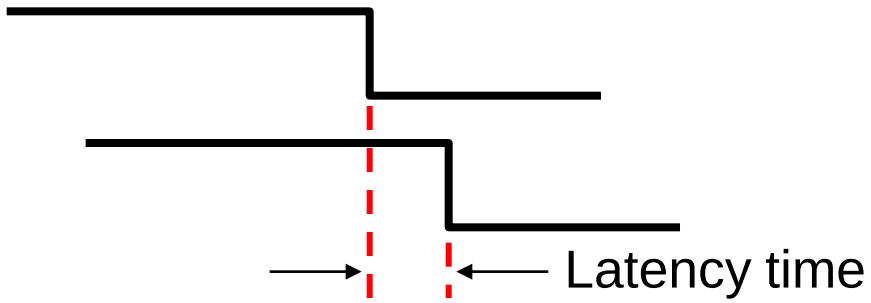
Settling Time or Latency Time = 5.5 μs

Latency of Other ΔΣ ADCs

Device	Cycle Latency	Latency Time	Data Rate	Effective Resolution
ADS1252	5-cycle	150 μs	40 ksps	19 bits
ADS1254	5-cycle	300 μs	20 ksps	19 bits
ADS1601	50-cycle	41 μs	1.25 Msps	17 bits
ADS1602	46-cycle	19 μs	2.5 Msps	17 bits
ADS1605	46-cycle	9.4 μs	5 Msps	16 bits
ADS1610	54-cycle	5.5 μs	10 Msps	16 bits
ADS1625	45-cycle	37 μs	1.25 Msps	15 bits

Don’t let High Cycle-Latency Bother You

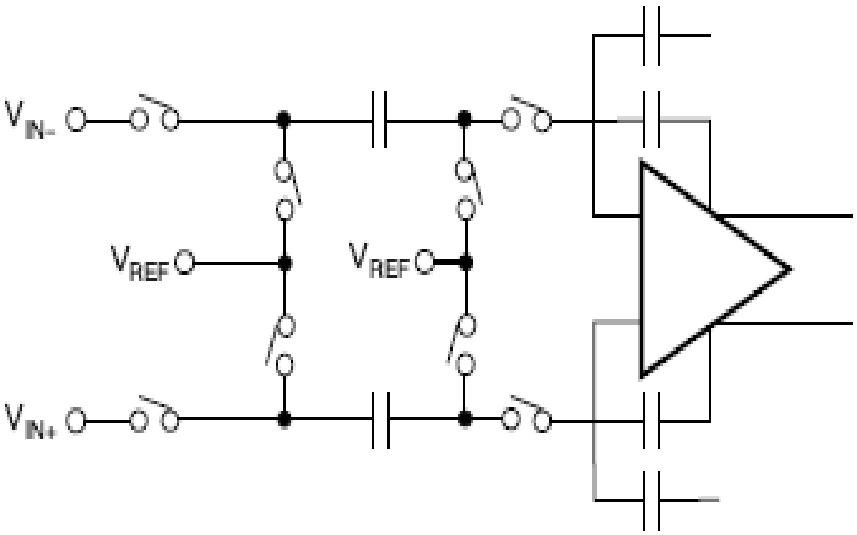
Control systems == Cause and Effect



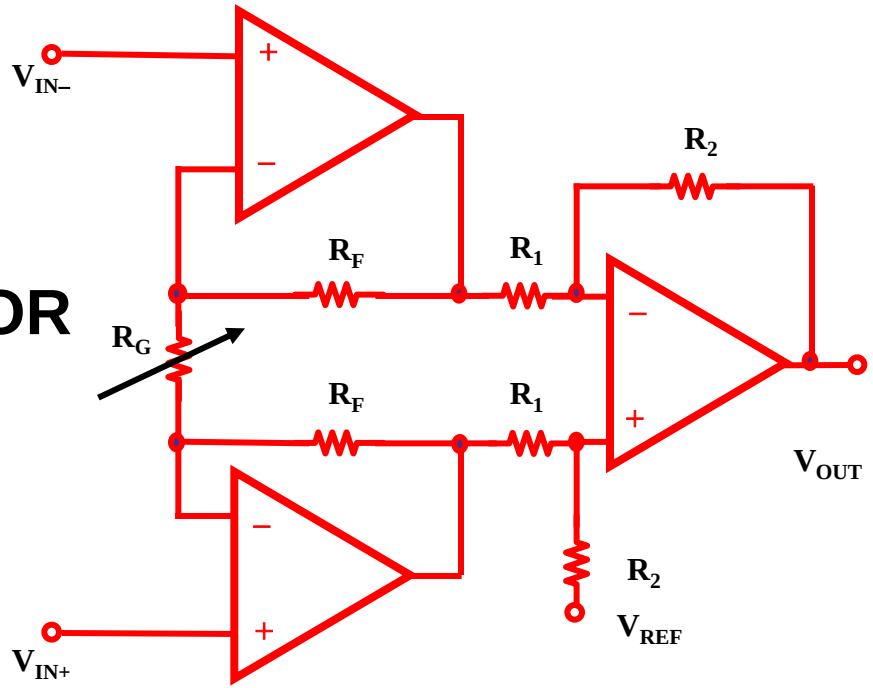
Cycle Latency	Latency Time	Total Latency - System Issues
Zero	Very Low	**The Best of BOTH Worlds**
Zero	High	Wait for first data out, Could be Slow
High	Very Low	Count Data Out – Processor Overhead, Could still be Fastest Solution
High	High	Count Data Out – Processor Overhead Slowest solution

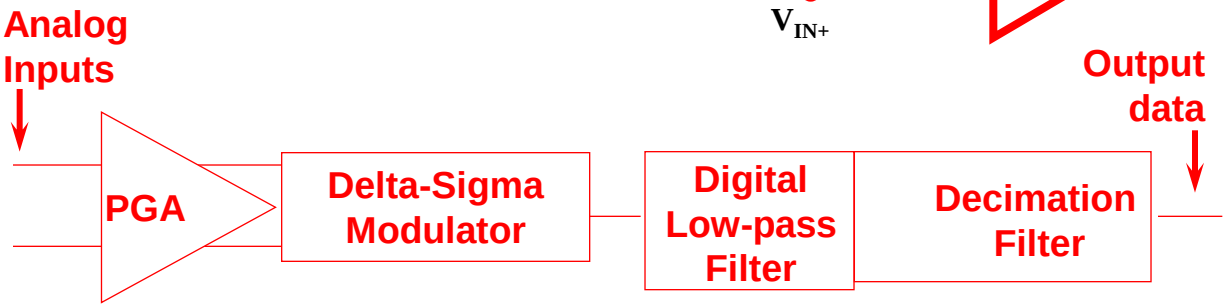
PGAs in Delta Sigma Converters

Programmable Gain Amplifier (PGA)



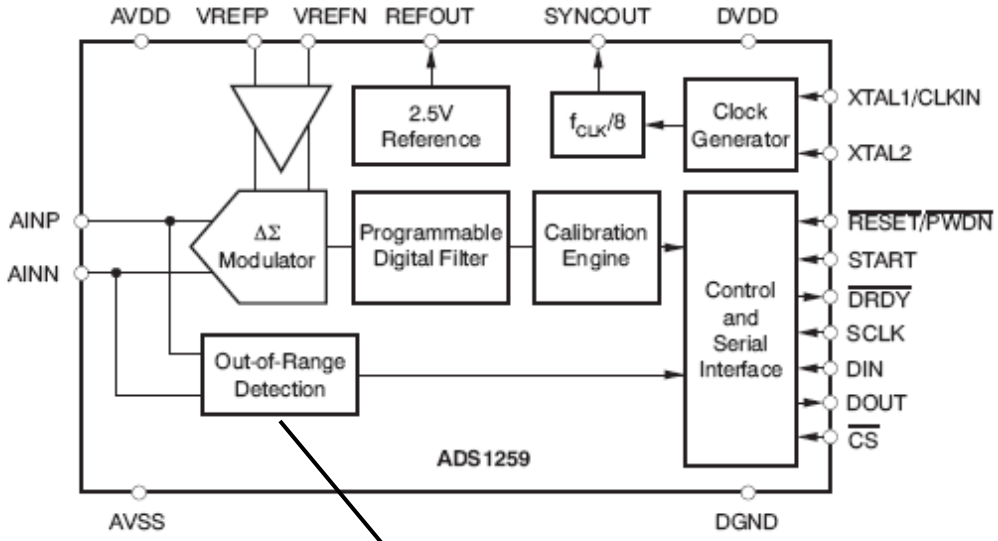
OR



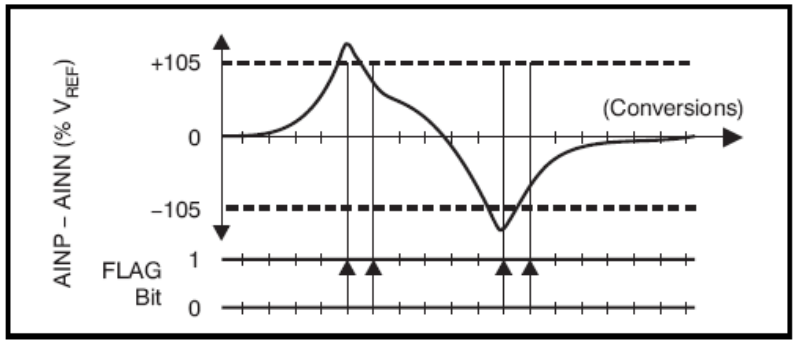


Out of Range Detection

Out of Range Detection

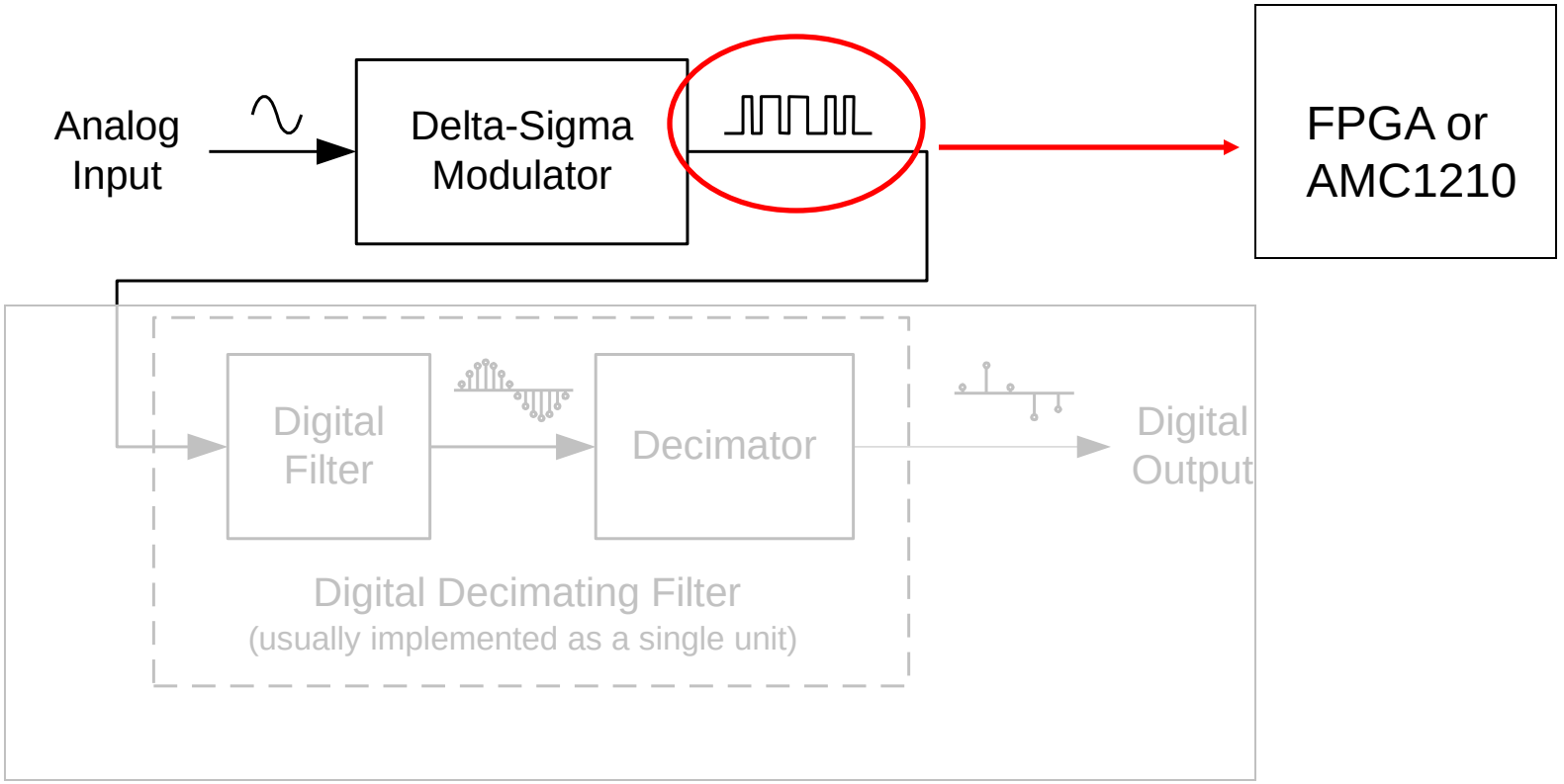


ADS1259



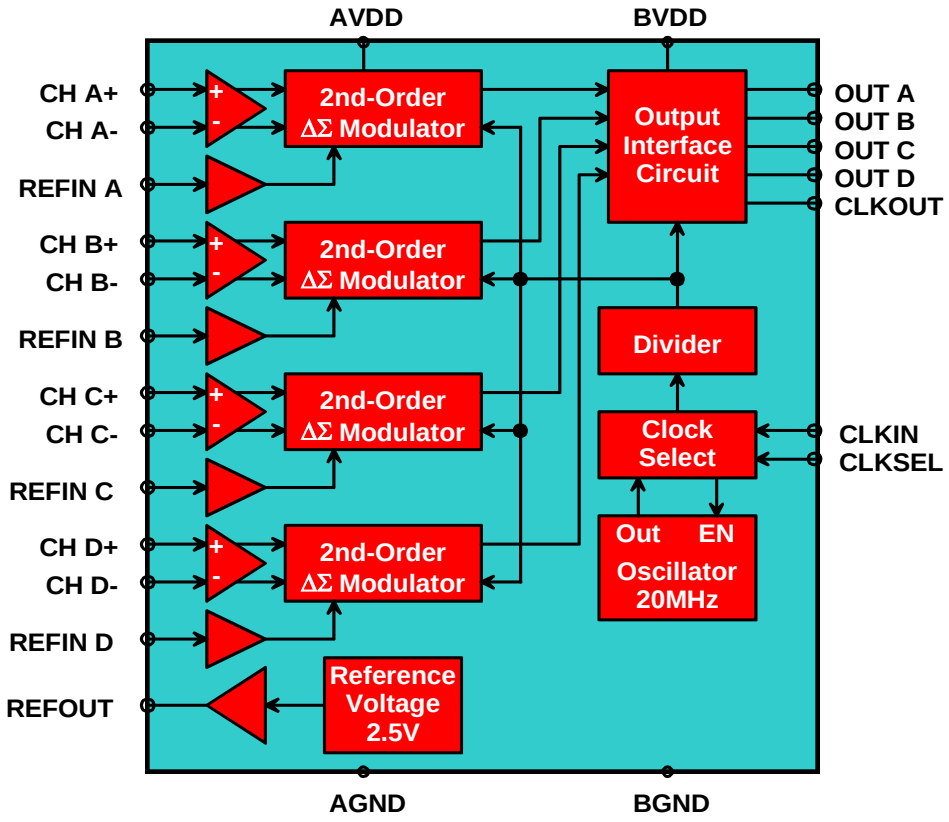
Delta Sigma Modulators

Modulator Output



ADS1204 1-bit, 10 MHz, 4 Ch., 2nd Order Modulator

- 16-Bit Effective Resolution
- Input Range 2.5 V @ 2.5 V
- 86 dB SNR Min
- Four Independent Modulators
- Four Input Reference Buffers
- On Board 20 MHz Oscillator
- QFN-32 (5x5 mm) Package



- **Current Measurement**
- **Magnetic Sensors**
- **Motor Control**
- **Power Converters**

ADS1282

Ultra-High Performance ΔΣ ADC with PGA

Features

- Extremely High Resolution
  - SNR: 130dB (250SPS, G=1)
  - SNR: 125dB (250SPS, G=16)
- Ultra-Linear
  - THD -122dB, INL: 0.5ppm
- Flexible Data Rate
  - 250SPS to 4kSPS
- Onboard High Performance Digital Filter
  - SINC + FIR + IIR (selectable)
  - Linear or Minimum Phase
  - 0.5Hz to 7.5Hz High Pass
  - Filter Bypass Mode
- Low Power
  - ADS1282: 25mW (17mW Low Power Mode)

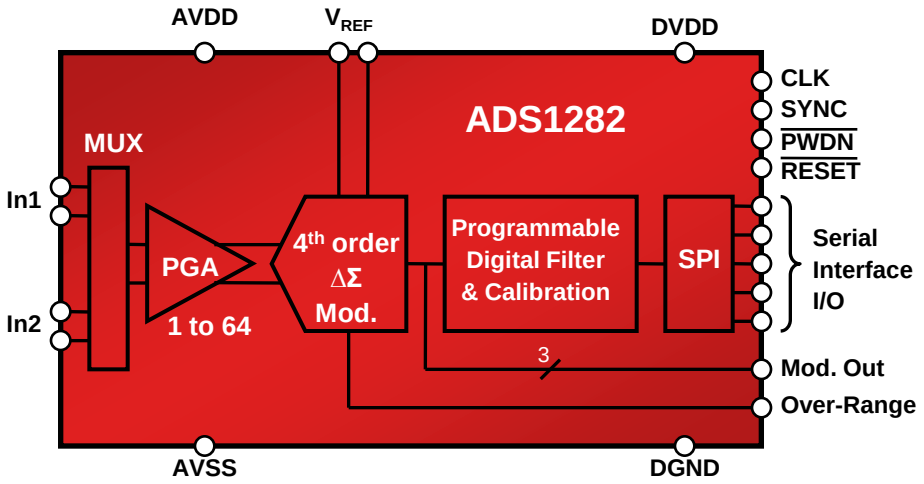
Applications

- Seismic / Energy Exploration
- Geophone / Hydrophone Recording
- Earthquake/Building Monitoring
- Scientific Instrumentation

Benefits

- ***Unmatched Performance, Integration and Low-power Operation***
- **Single-chip Solution for Digitizing Geophones or Hydrophones**
- **Filter Bypass Mode Allows Direct Access to Modulator Data for Use with External Digital Filter**

ADS1282: MUX + PGA + Mod. + Dig. Filter



ADS1282: $36.95 (1k pcs)

Texas Instruments