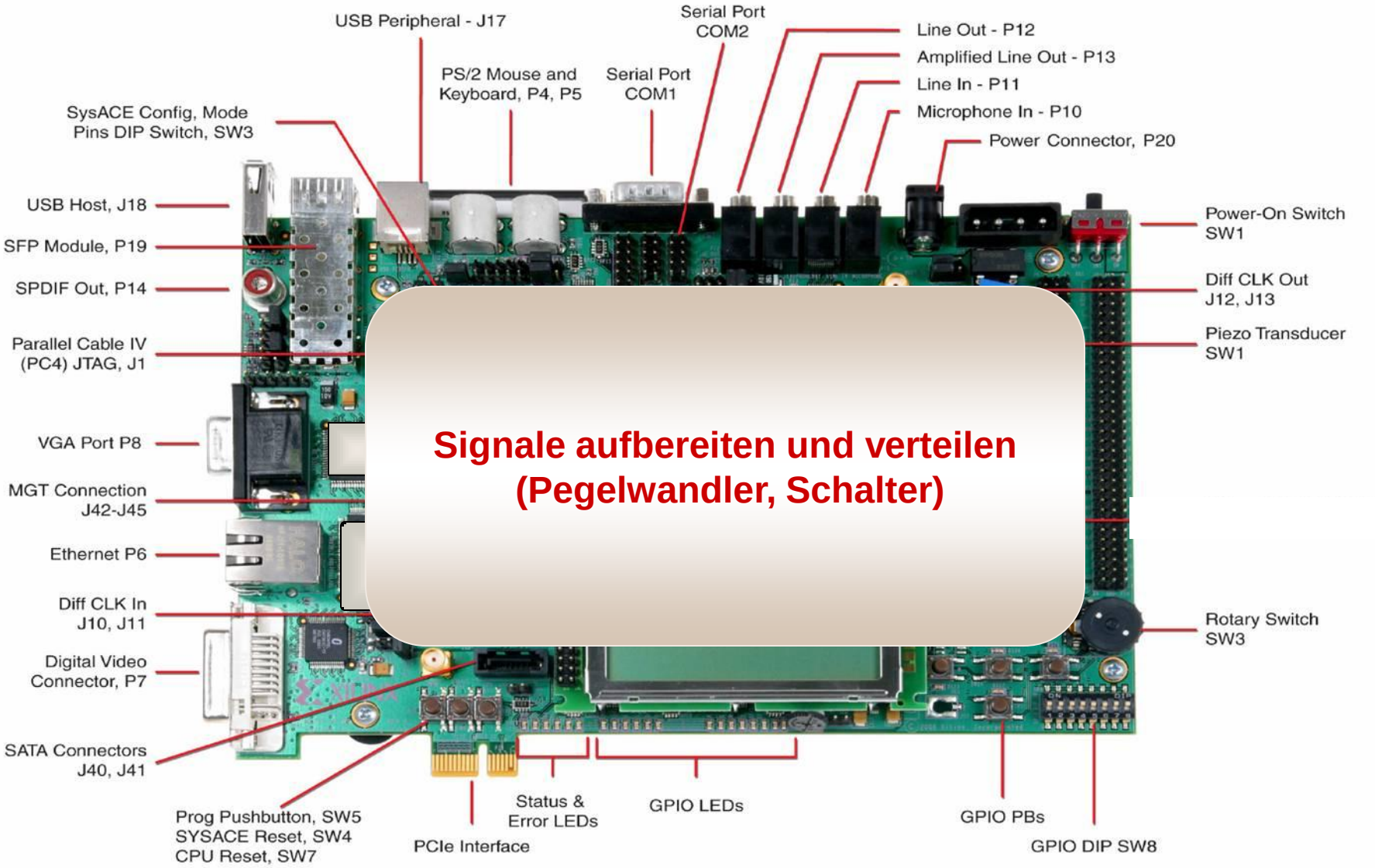
TI Technology Days 2010

HVL-SLL-Analog Lösungen für typische Schaltungsprobleme

Agenda

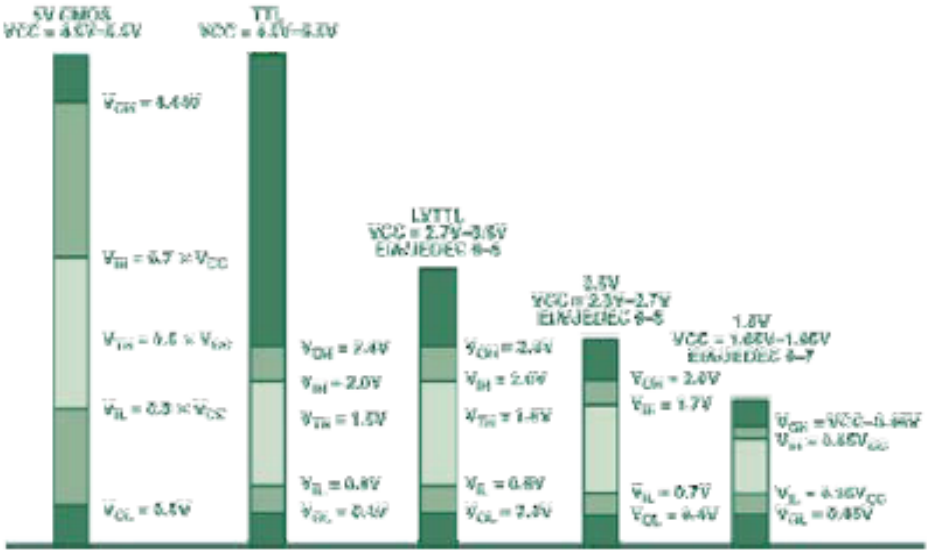
- Lösungen für typische Schaltungsprobleme

- Signale aufbereiten und verteilen (Pegelwandler, Schalter)
- Leistung steuern und einsparen (Analogschalter und LED-Treiber)
- Schnittstellen schützen (ESD/EMI)
- Typische Entwurfsprobleme (PCB) vermeiden (intelligente Logik)


USB Peripheral - J17
Serial Port COM2
Line Out - P12
Amplified Line Out - P13
Line In - P11
Microphone In - P10
Power Connector, P20
PS/2 Mouse and Keyboard, P4, P5
Serial Port COM1
SysACE Config, Mode Pins DIP Switch, SW3
USB Host, J18
SFP Module, P19
SPDIF Out, P14
Parallel Cable IV (PC4) JTAG, J1
VGA Port P8
MGT Connection J42-J45
Ethernet P6
Diff CLK In J10, J11
Digital Video Connector, P7
SATA Connectors J40, J41
Power-On Switch SW1
Diff CLK Out J12, J13
Piezo Transducer SW1
Rotary Switch SW3
Signale aufbereiten und verteilen (Pegelwandler, Schalter)
Prog Pushbutton, SW5
SYSACE Reset, SW4
CPU Reset, SW7
PCIe Interface
Status & Error LEDs
GPIO LEDs
GPIO PBs
GPIO DIP SW8

Logic Levels Overview

- 5V TTL
- 5V CMOS
- LVTTL



5V	Inputs VIH/VIL	Output VOH/VOL	Reference Logic
5V-CMOS	0.7 x Vcc/ 0.3xVcc	4.44V/0.5V	LV-A, AHC
TTL	1.5V/0.8V	2.4V/0.4V	F, ALS
3.3V			
LVTTL	1.5V/0.8V	2.4V/0.4V	LVC/LV-A
2.5V			
CMOS	1.7V/0.7V	2V/0.4V	LVC/LV-A
1.8V			
CMOS	0.65xVcc/ 0.35x Vcc	Vcc-0.45V/ 0.45V	AUC

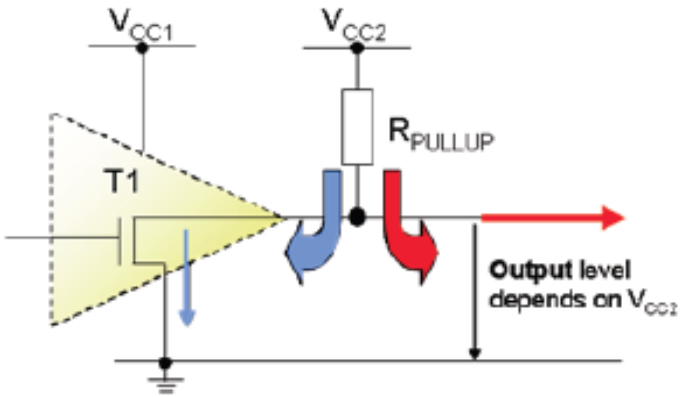
- CMOS
- Open Drain

Open-Drain Switching Level

The Input (VIH/VIL/VOL) is referenced to Supply Vcc of the Chip and Outputs (VOH) is referenced to external Pull-Up Resistor)

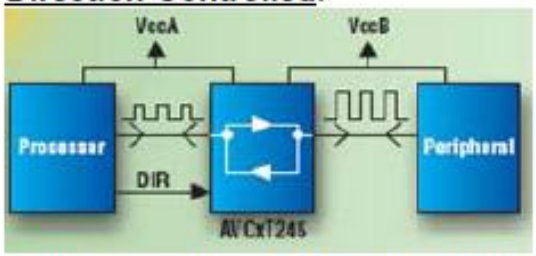
Supply Voltage Vccn	LVC07 understands	Pull-up resistor may be connected to	Level Conversion range
1.8V	1.8V Levels	1.8V, 2.5V, 3.3V and 5V	1.8V -> 1.8V – 5.5V
2.5V	2.5V Levels	1.8V, 2.5V, 3.3V and 5V	2.5V -> 1.8V – 5.5V
3.3V	3.3V Levels	1.8V, 2.5V, 3.3V and 5V	3.3V -> 1.8V – 5.5V
5V	5V Levels	1.8V, 2.5V, 3.3V and 5V	5V -> 1.8V – 5.5V

Required **Input** level depends on V_{CC1}



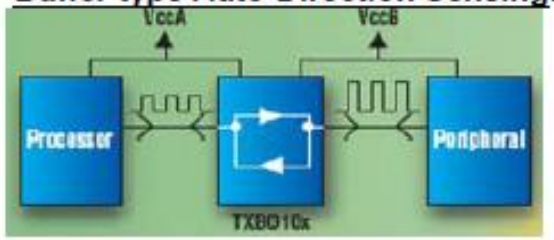
Four Different Voltage Translation Classes

Direction-Controlled:



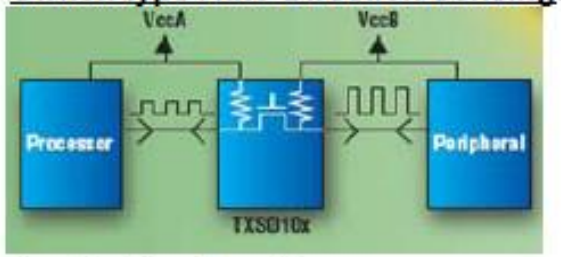
- Support signal Data Rates of 200 Mb/s + ✓
- Offered in variety of bit-widths (i.e. 1 – 32) ✓
- Supports supply-voltages from 1.2V to 5.5V ✓
- Good DC drive strength of 12mA ✓
- Capable of driving Resistive loads ✓

Buffer type Auto-Direction Sensing:



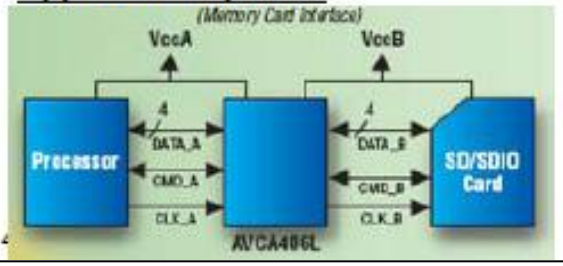
- Support signal Data Rates up to 100 Mb/s ✓
- Offered in variety of bit-widths (i.e. 1 – 8) ✓
- Supports supply-voltages from 1.2V to 5.5V ✓
- Average DC drive strength of 100's uA capable of driving Hi-Z loads up to 70pF ✓
- Push-Pull driver optimized ✓

Switch type Auto-Direction Sensing:



- Support signal Data Rates up to 40 Mb/s + ✓
- Offered in variety of bit-widths (i.e. 1 – 8) ✓
- Supports supply-voltages from 1.2V to 5.5V ✓
- Average DC drive strength of 100's uA capable of driving Hi-Z loads up to >100pF ✓
- Open-Drain driver optimized ✓

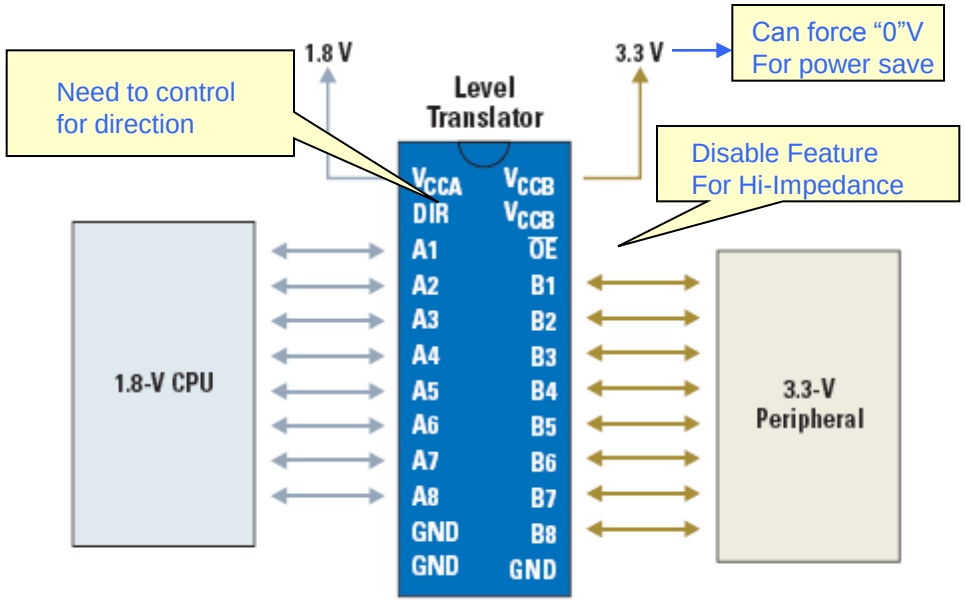
Application Specific:

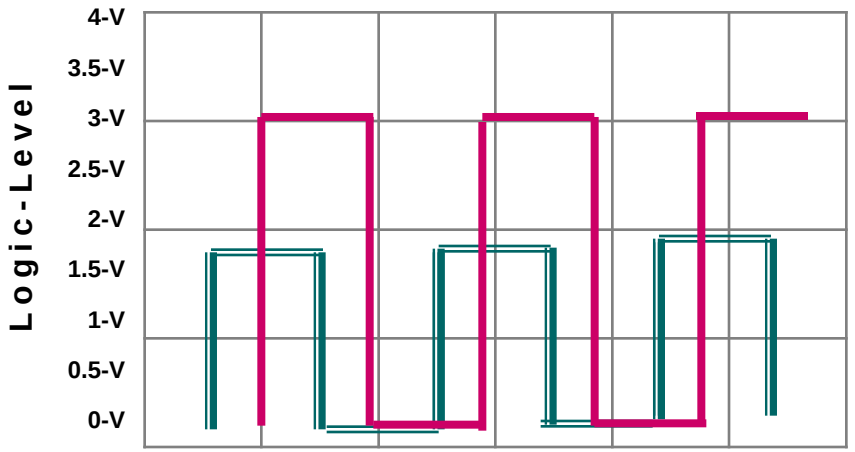


- Hybrid architecture solutions ✓
- Offered in variety of bit-widths (i.e. 1 – 32) ✓
- Supports supply-voltages from 1.2V to 5.5V ✓
- Includes translators with integrated LDO power-sources ✓

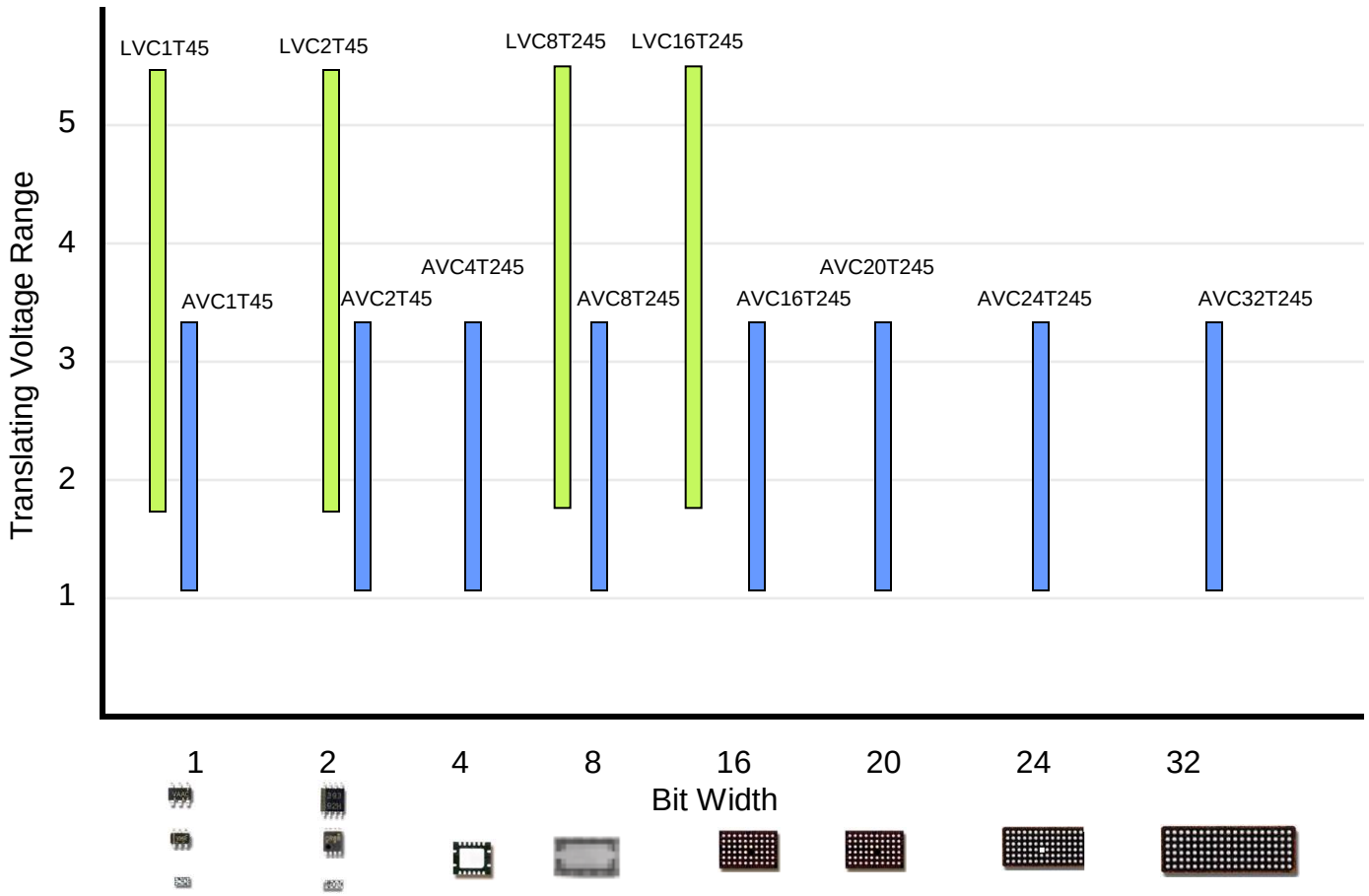
AVC Technology Translator

- Translate the particular logic level to another required logic Voltage Level(e.g:1.8V to/from 3.3V)
- Driving capability to ensure the signal integrity.
- DIR control pin to manage the direction of data transmission.
- /Output enable to reduce power consumption.
- Partial power down (Ioff)



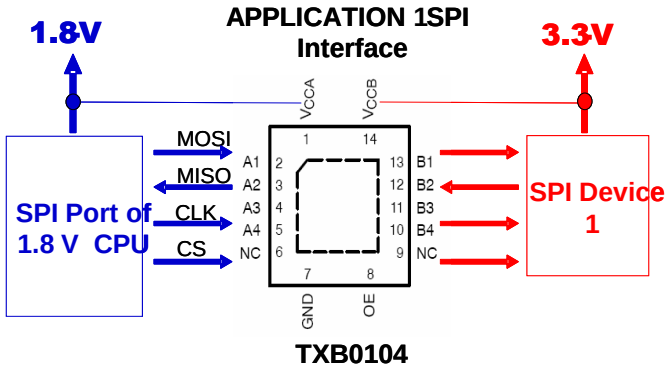


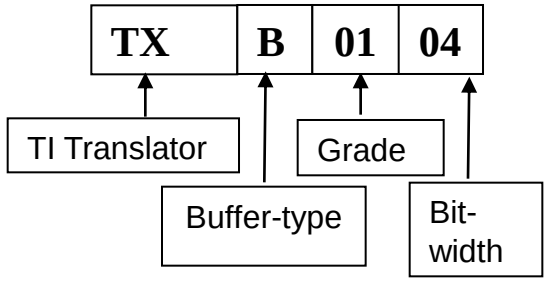
Direction-Controlled Voltage Translation

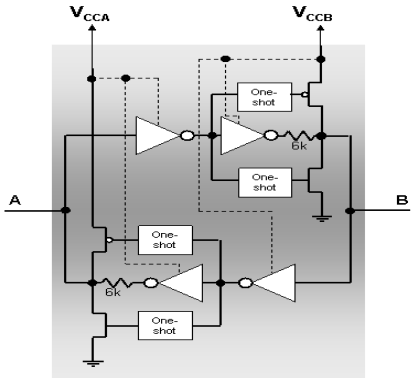


TXB Translator

- Data-Rate
  - V_{CCA} 1.2V <> V_{CCB} 20 Mbps
  - V_{CCA} 1.5V <> V_{CCB} 40 Mbps
  - V_{CCA} 1.8V <> V_{CCB} 60 Mbps
  - V_{CCA} 2.5V <> V_{CCB} 100 Mbps
  - V_{CCA} 3.3V <> V_{CCB} 100 Mbps
- Low Power Consumption 4-µA Max. I_{CC}
- I/Os Push-Pull CMOS
  - $V_{IH} = V_{CCI}$ X 0.65
  - $V_{IL} = V_{CCI}$ X 0.35
  - $V_{OH} = V_{CCI}$ – 0.4V,
  - V_{OL} = 0.4V
- OE is referenced to V_{CCA} and 5.5V Input Tolerant (CMOS)
- Either V_{CCA} or V_{CCB} Power-Supply can be ramped first
- Driving Load Capacitance up to 70-pF
- External Pull-Up/Down Resistors must be >50kΩ



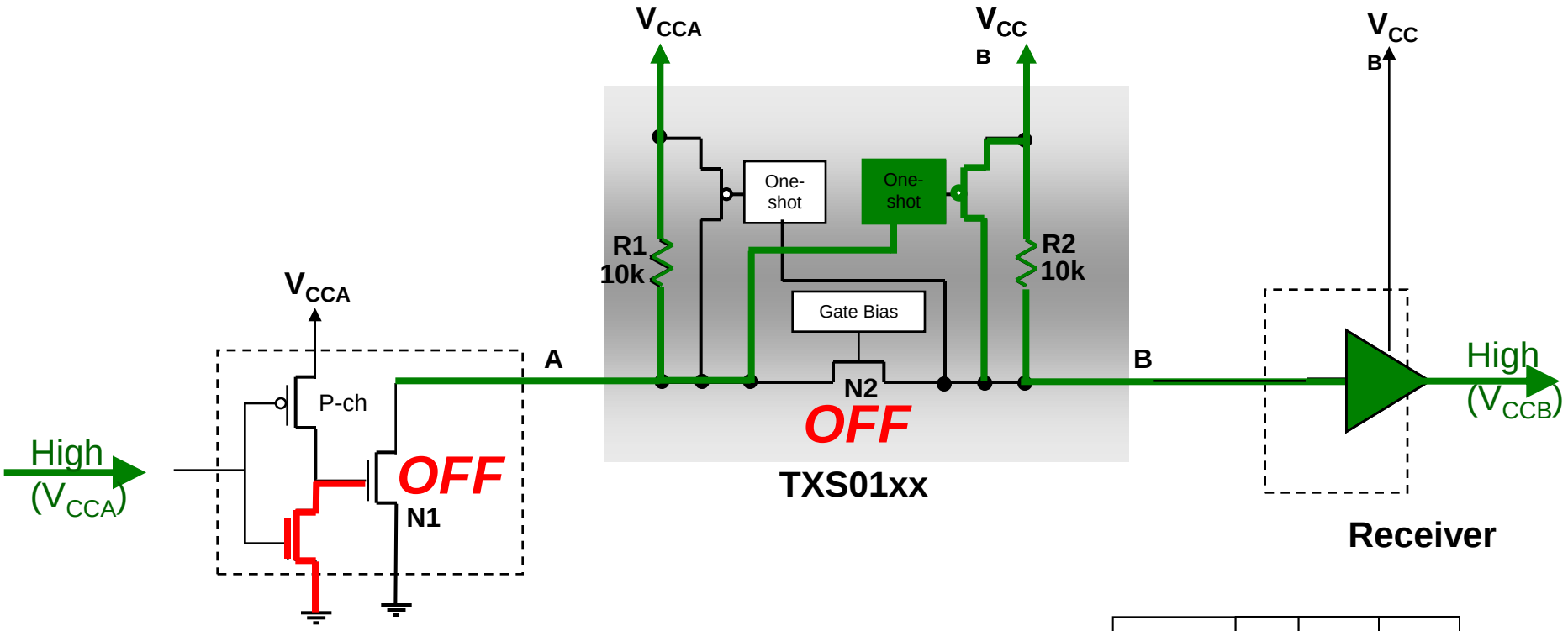


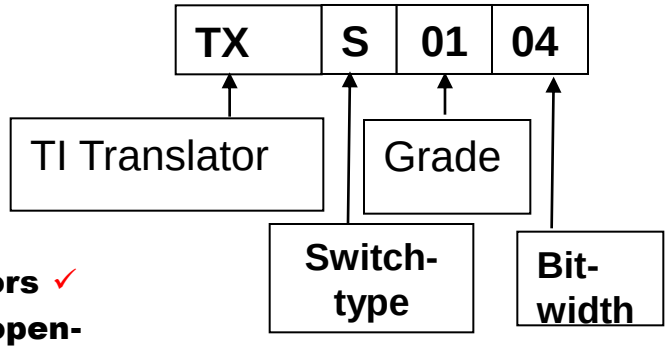


Device	Pins.	# bits	I/O Level Translator Range	ESD (B-Ports)	Ioff	HI-z	DCK	DCU	SOIC	TSSOP	QFN(RGY)	uQFN	WCSP/BGA
TXB0101	6	1	1.5V, 1.8V, 2.5V, 3.3V, 5V	HBM: ± 15KV	✓	✓	⊙						⊙
TXB0102	8	2	1.5V, 1.8V, 2.5V, 3.3V, 5V	HBM: ± 15KV	✓	✓		⊙					⊙
TXB0104	14/12	4	1.5V, 1.8V, 2.5V, 3.3V, 5V	HBM: ± 15KV	✓	✓			⊙	⊙	⊙		⊙
TXB0106	16	6	1.5V, 1.8V, 2.5V, 3.3V, 5V	HBM: ± 15KV	✓	✓			⊙		⊙		
TXB0108	20	8	1.5V, 1.8V, 2.5V, 3.3V, 5V	HBM: ± 15KV	✓	✓				⊙	⊙	⊙	

Auto-Direction Sensing Switch Type Translators

Device Operation – Transmitting a High Signal





Features:

- **No Direction Control Signal Needed** ✓
- **Up to 20Mbps Data Rates** ✓
- **One-shots act to speed up Low to High Transitions** ✓
- **Can drive heavier Capacitive Loads than the TXB Translators** ✓
- **Integrated pull-up resistors save board space and cost in open-drain applications** ✓

TXS "Switch" Type Translator

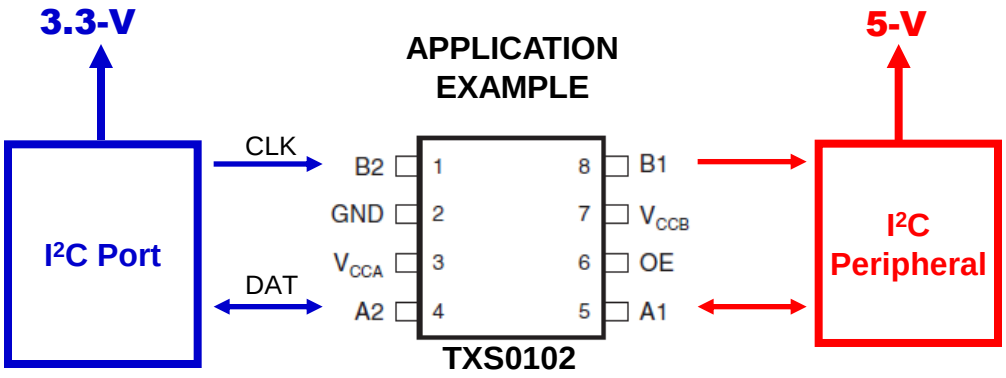
- **Data-Rate**
  20-Mbps to 24-Mbps
- **10K-Ω Integrated R_{PU} on both I/Os**
- **I/Os Push-Pull/Open Drain**
- **OE is referenced to V_{CCA} and 5.5V Input Tolerant**
- **Open Drain/Push Pull Type**
- **I²C, 1-Wirebus, MMC Card I/F**

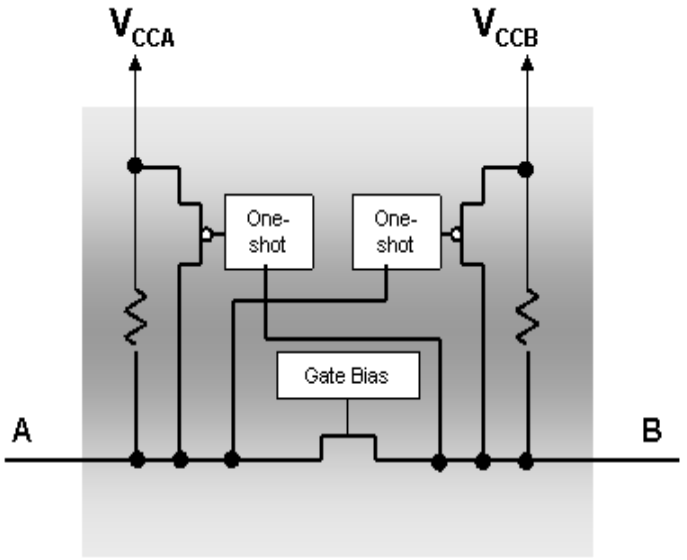
B Port for TXS0104E/0108E
- 15-kV Human-Body Model (A114-B)
- 200-V Machine Model (A115-A)
- 1000-V Charged-Device Model (C101)

IEC 61000-4-2 ESD (B Port)

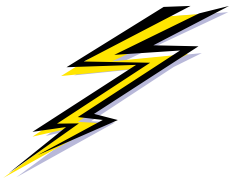
- ±8-kV Contact Discharge
- ±10-kV Air-Gap Discharge

TXS010**X** **E** **xxx**
- E → Air-Gap/Contact ESD
- X → Number Of Bits





Device	Pins.	# bits	I/O Level Translator Range	ESD (B-Ports)	Air Gap	Ioff & HI-z	DCK	DCU	SOIC	TSSOP	QFN(RGY)	WCSP/BGA
TXS0101	6	1	1.8V, 2.5V, 3.3V, 5V	HBM: ± 8KV		✓	⊙					⊙
TXS0102	8	2	1.8V, 2.5V, 3.3V, 5V	HBM: ± 8KV		✓		⊙				⊙
TXS0104E	14/12	4	1.8V, 2.5V, 3.3V, 5V	HBM: ± 15KV	± 10KV				⊙	⊙	⊙	⊙
TXS0108E	20	8	1.8V, 2.5V, 3.3V, 5V	HBM: ± 15KV	± 15KV					⊙	⊙	



For every protocol a translator

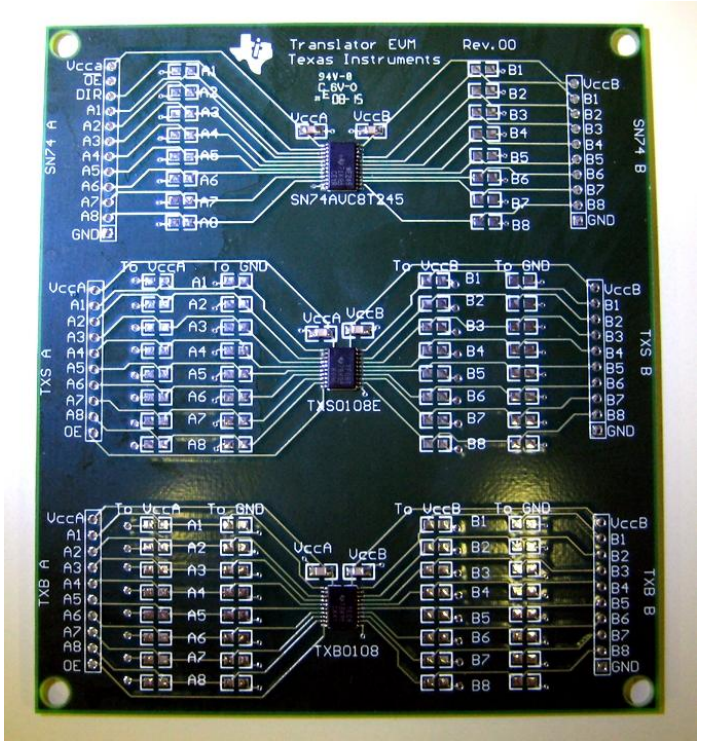
Interface	Name	Spec-Type	VLT-Type	# bits	Data Rate (Mb/s)	Clock Rate (MHz)	Signal Names	Voltage-Levels	TI-Translator
SDIO	Secure-Digital I/O	Full-Speed	Switch	4	100	0 - 25	DAT[3:0], CMD, CLK	Initialization: 2V to 3.6V Operation: 3.1V to 3.5V	TXB0104, TXS0206
SDIO	Secure-Digital I/O	Low-Speed	Switch	4		0 - 0.4	DAT[3:0], CMD, CLK	Initialization: 2V to 3.6V Operation: 3.1V to 3.5V	TXB0104, TXS0206
SPI	Serial-Peripheral-Interface	4-wire Synchronous Serial I/F	Switch	4	20	0,5	MOSI (Serial Data Input) - MISO (Serial Data Output) - SCK (Serial Clock)	1.5V, 1.8V, 2.5V, 3.3V, 5V	TXB0104
I^2C	Inter-Integrated-Circuit	Fast-Mode	Switch	2	0,4		SCL = Serial Clock SDA = Data I/O	1.5V, 1.8V, 2.5V, 3.3V, 5V	TXS0102
I^2C	Inter-Integrated-Circuit	Fast-Mode-Plus	Switch	2	1		SCL = Serial Clock SDA = Data I/O	1.5V, 1.8V, 2.5V, 3.3V, 5V	TXS0102
I^2C	Inter-Integrated-Circuit	High-Speed-Mode	Switch	2	3,4		SCL = Serial Clock SDA = Data I/O	1.5V, 1.8V, 2.5V, 3.3V, 5V	TXS0102
SMBus	System-Management-Bus	SMBus 2.0	Switch	2			SCL = Serial Clock SDA = Data I/O	1.5V, 1.8V, 2.5V, 3.3V, 5V	TXS0102
PMBus	Power-Management-Bus	PMBus	Switch	2	0,4		SCL = Serial Clock SDA = Data I/O	1.5V, 1.8V, 2.5V, 3.3V, 5V	TXS0102
1-wire	One-Wire	Microlan	Switch	1	0,163		1WI/1WO	1.5V, 1.8V, 2.5V, 3.3V, 5V	TXS0101
SIM	Subscriber Identity Modul	ISO/IEC7812	Switch/Buffer	3			RST = Reset CLK = Clock I/O = Data I/O	Input = 3.05V to 5V Output = 1.8V or 3.0V	TXS02326E
IC-USB	Inter-Chip USB			2	12		D+ = Diff Data Line D- = Diff Data Line	1.1V to 3.6V	AVC2T872, TXS0202
HSIC	High-Speed Inter-chip USB			2	480		D+ = Diff Data Line D- = Diff Data Line	1.1V to 3.6V	TXS0202
LCD	Liquid Crystal Display		Buffer	32				1.1V to 3.6V	AVC32T245

Voltage Translation EVM

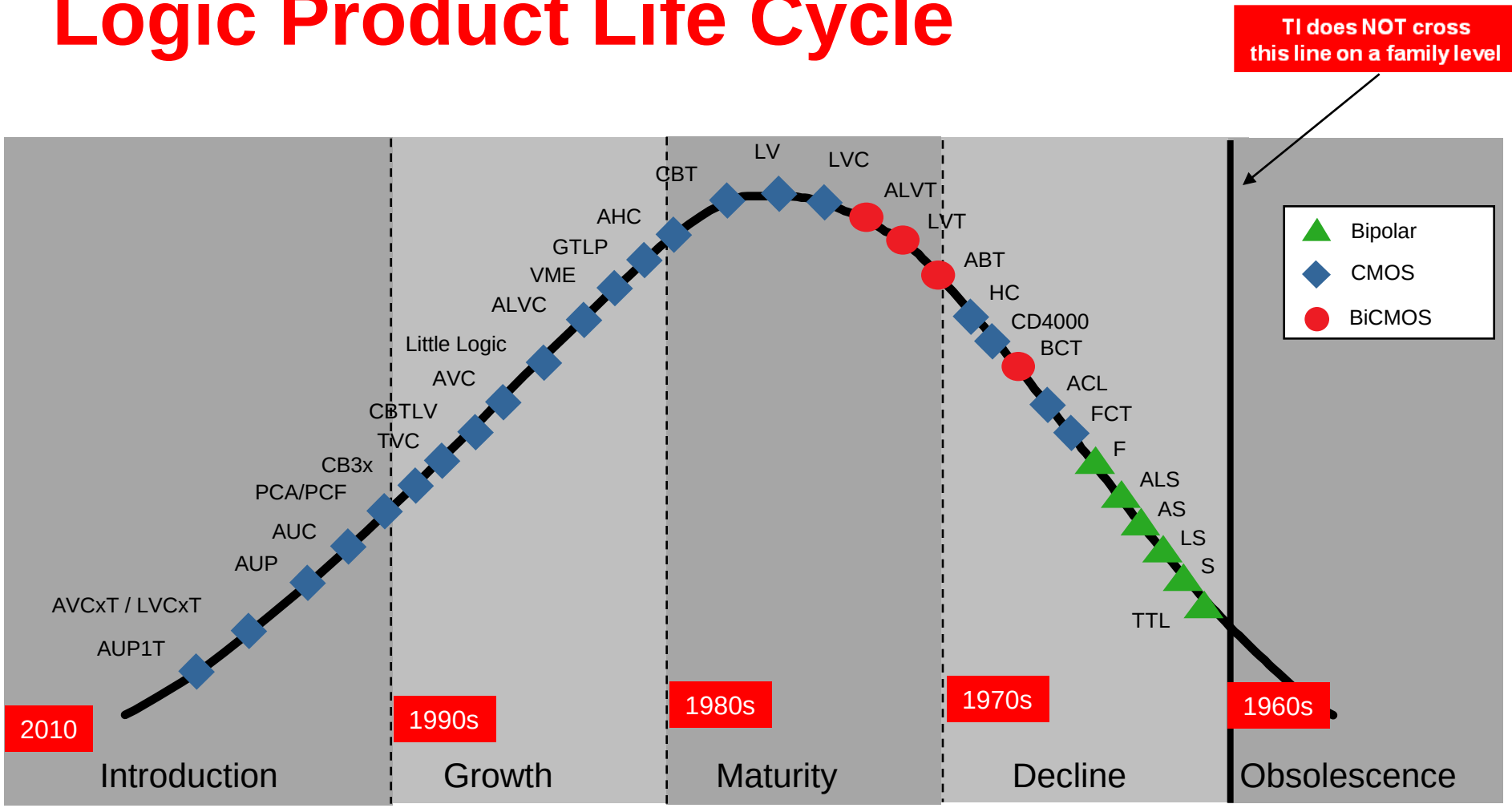
Features

- Demonstrates capabilities of our Direction controlled and Auto-Direction Voltage Translators
- Includes foot-print for I/O data line R_{PU} and R_{PD} and/or Capacitors
- EVM supports three separate 8-bit width voltage translators
  - **SN74AVC8T245PWR**
    - Supports 1.2V – 3.3V V_{CC} Supplies
  - **TXB0108PWR**
    - "Buffer-Type" for "Push-Pull" (PP) Apps
    - Supports 1.2V – 5.5V V_{CC} Supplies
  - **TXS0108PWR**
    - "Switch-Type" for PP (60 Mbps) "Open-Drain" (OD) 2 Mbps

CONNECTION DESCRIPTION	
Label	**Description**
V_{CCA}	**A-side Power-Supply**
V_{CCB}	**B-side Power-Supply**
GND	**Power-Supply Ground (i.e. 0V)**
A1 – A8	**A-side Data Signal I/O pins**
B1 – B8	**B-side Data Signal I/O pins**
OE	**Output Enable control signal pin (Active Low for AVC8T245 and active High for the TXB0108 and TXS0108E)**
DIR	**Direction control signal pin (Applicable for the AVC8T245)**



Logic Product Life Cycle

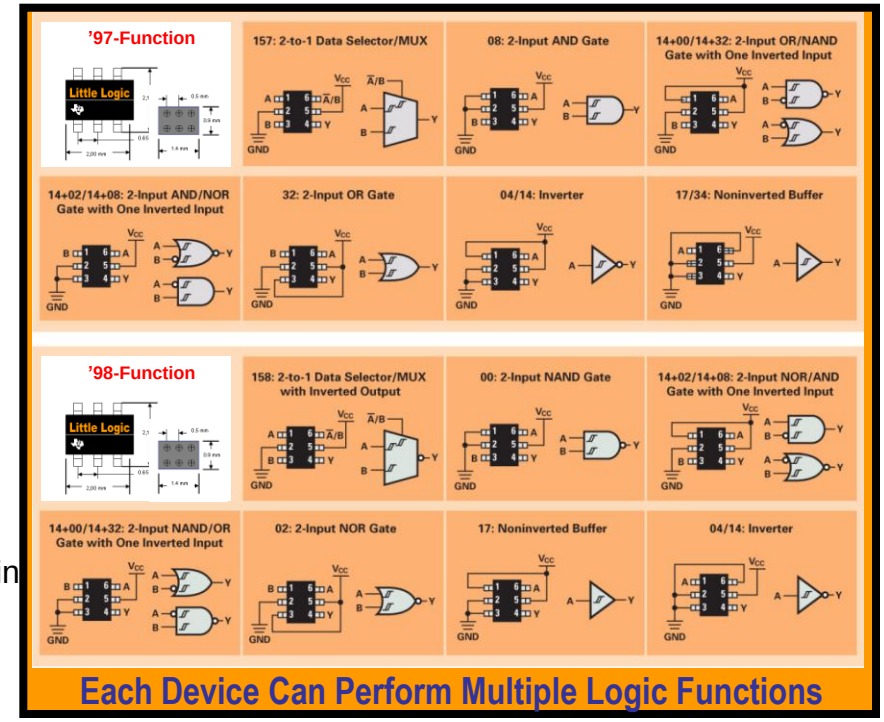


TI remains committed to be the last major supplier in every logic family

SN74AUP1T97/98
Single-Supply Voltage Level Translator w/9 Logic Functions

- **Features**
- Single Supply Voltage Translator
  - 1.8 V to 3.3 V (at V_{CC} = 3.3 V)
  - 2.5 V to 3.3 V (at V_{CC} = 3.3 V)
  - 1.8 V to 2.5 V (at V_{CC} = 2.5 V)
  - 3.3 V to 2.5 V (at V_{CC} = 2.5 V)
- Can be configured as 1 of 9 logic functions
- Schmitt-Trigger Inputs

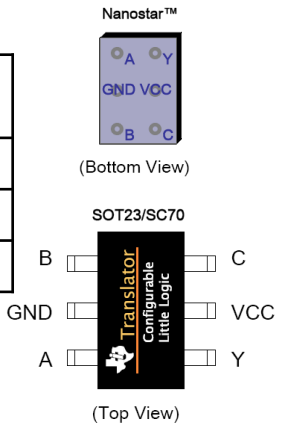
- **Benefits**
- Simplified PCB Routing
- Flexible Functionality Simplifies Inventory Management (9-in
- Tolerant to Slow Input Transitions and Noisy Signals

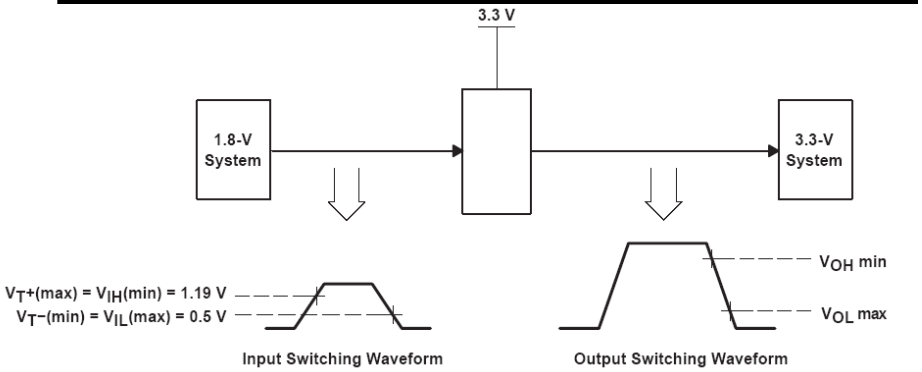


Each Device Can Perform Multiple Logic Functions

	Body Length	Package Width
NanoStar/NanoFree	1.4mm	0.9mm
SC-70	2mm	2mm
SOT-23	2.9mm	2.8mm

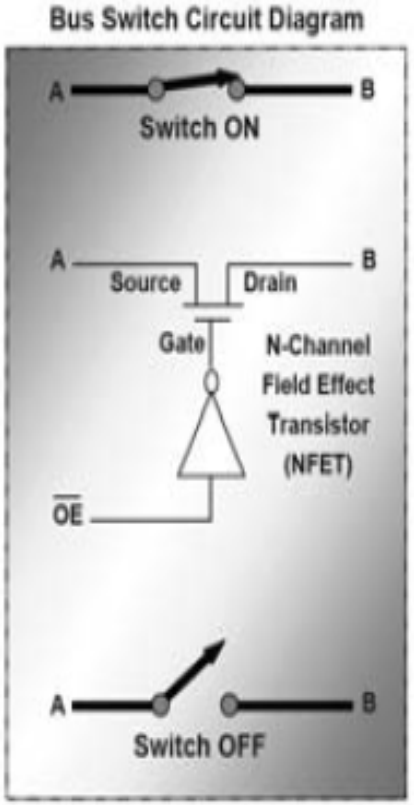
Package Dimensions





Example: 1.8V LVCMOS to 3.3V LVTTL/LVCMOS Translation

Translating FET Switches / BUS Switches:



FET switches are ideal for translation applications in which active current drive is not required or where very fast propagation delays are desired.

When ON, a Bus Switch Provides

- –Bi-directional signal passing
- –Near zero propagation delay (0.25ns) for maximum system performance
- –Very low resistance (Ron ≈ 5Ω to 10Ω)
- –Very low capacitance (Cio ≈ 8pF to 12pF)
- –Fast data throughput (100MHz to 500MHz)
- –No drive current (pass-through current only)

When OFF, a Bus Switch Provides

- –Excellent isolation with very high resistance (Ron = 10's of MΩ)
- –Very low capacitance (Cio ≈ 3pF to 5pF) minimizes capacitive loading and signal distortion

Many Bit width Options

Many Signal Routing Options (Isolation, MUX, DeMUX, Exchange)

Digital Bus Switch

CB3T – 2.5V/3.3V Low-Voltage Translator Bus Switch
• Output Voltage Translation Tracks Vcc
• Supports Mixed-Mode Signal Operation On All Data I/O Ports
  - 5V Input Down to 3.3V Output Level Shift with 3.3V Vcc
  - 5V/3.3V Input Down to 2.5V Output Level Shift with 2.5V Vcc
• Ideal for Low-Power Portable Equipment

CB3Q – 3.3V/2.5V High-Bandwidth Bus Switch Family
• High-Bandwidth Data Path (Up to 500MHz)
• Provides Low and Flat On-State Resistance (Ron) Characteristics
• Supports Rail-to-Rail I/O (RRIO) Switching from 0V to 5V
• Ideal for Broadband Communications and Networking Systems

CBT-C – Improved 5V General Purpose Bus Switch Family
• Active Undershoot Protection Circuitry Provides Protection to -2V
• Ioff Supports Partial-Power-Down Mode Operation
• Enhanced Performance vs. CBT (Faster Ten/Tdis, Lower Ron)
• Improved ESD Protection; 2KV HBM, 1KV CDM

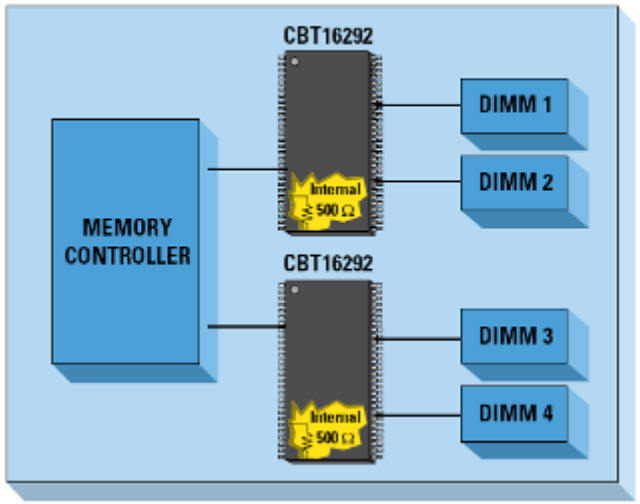
CBT – 5V General Purpose Bus Switch Family
• Supports 5V Operation (Vcc = 4V – 5.5V)
• CBTD Switches Configured as Level Shifter with Level Shifting Diode
• CBTR Features Series Damping Resistors for Improved Noise Control

CBTLV – 3.3V/2.5V General Purpose Bus Switch Family
• Supports 3.3V/2.5V Operation (Vcc = 2.3V – 3.6V)
• Offers Rail-to-Rail I/O (RRIO) Signal Transmission (No Voltage Clamping)

Parameters	CBT	CBT-C	CBTLV	CB3T	CB3Q
VCC	5V	5V	2.5/3.3V	2.5/3.3V	2.5/3.3V
R_{ON}	5Ω	3Ω	5Ω	5Ω	4Ω
R_{ON} Flat	na	na	na	na	YES 4Ω
Speed	0.25ns	0.15ns	0.15/0.25ns	0.15/0.25ns	0.12/0.2ns
Bandwidth	na	na	na	na	500MHz
Undershoot (Off)	na	-2V	na	na	na
Translation	na	na	na	YES	na

CBT Application Diagram

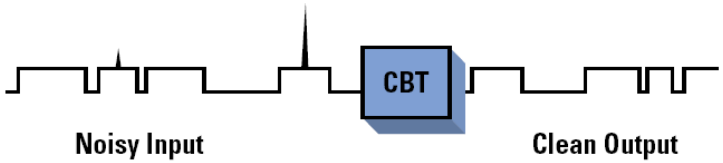
5-V Bus Switch Application



Memory Bus Data-bus loading sharing

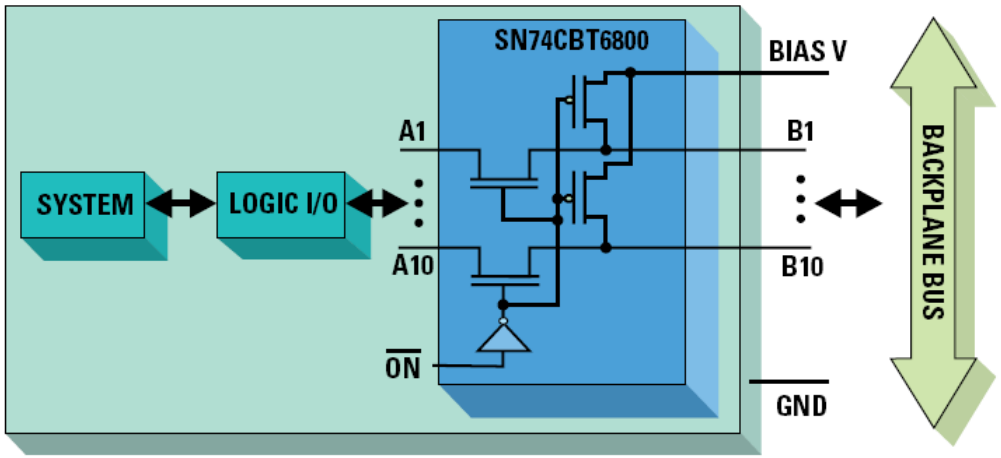
- CBT16292 is internal pull down when disconnected.
- Optimized on memory data-bus load sharing with Zero Delay switching the MUX.

Noise Filtering



CBTs reduce switching noise from voltage spikes and overshooting generated by line reflections, crosstalk or simultaneous switching.

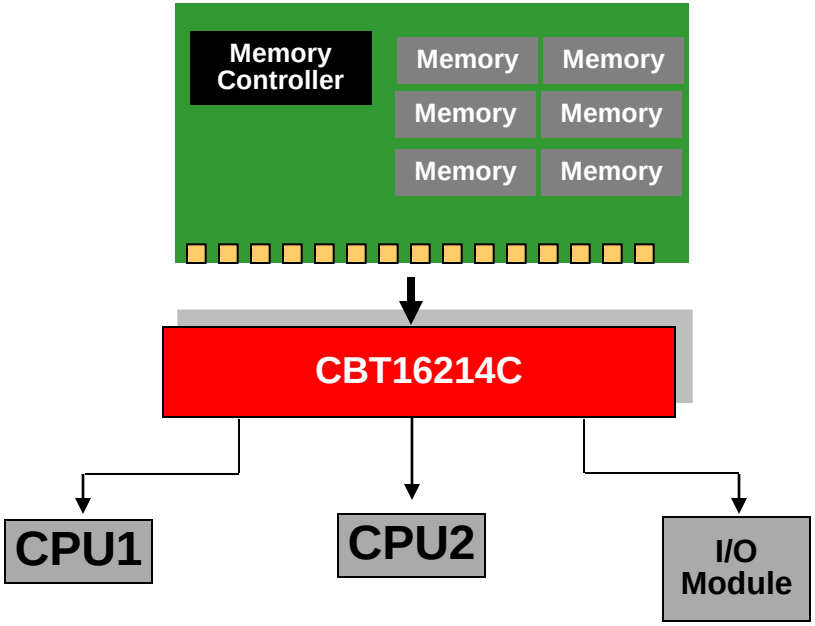
5-V Bus Switch Application



- *Flow-through pinout for simpler board layouts*
- *Precharged outputs for live insertion*

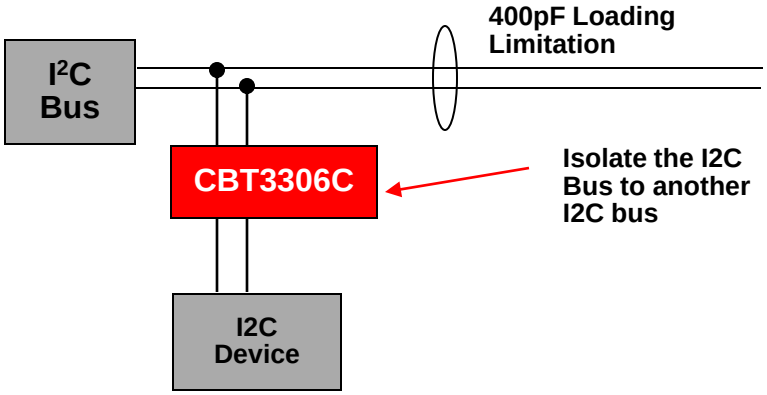
Precharge is optional feature to ensure the signal at proper level when Card Insertion.

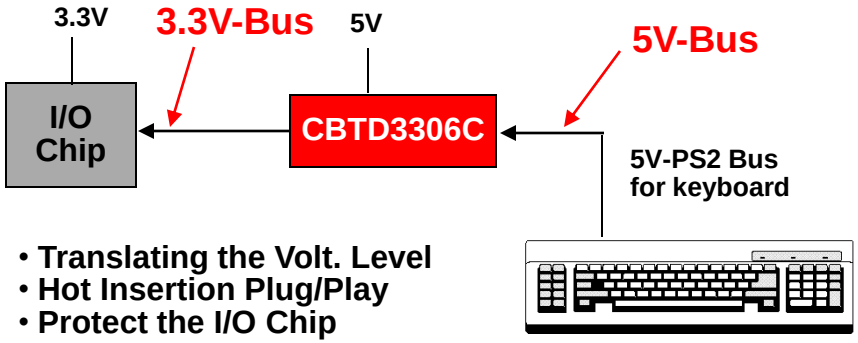
CBT Application Diagram



Server Workstation

- **Switching 1:3 Mux to different Module and CPU.**



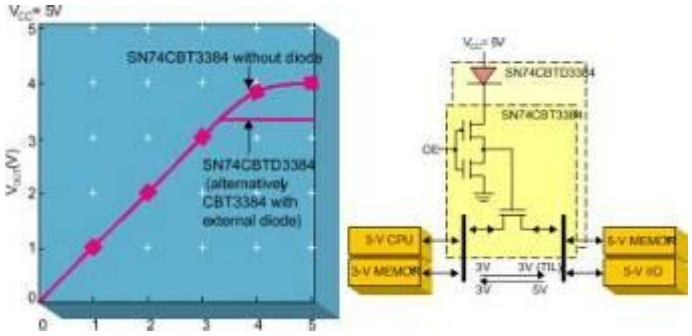


- **Translating the Volt. Level**
- **Hot Insertion Plug/Play**
- **Protect the I/O Chip**

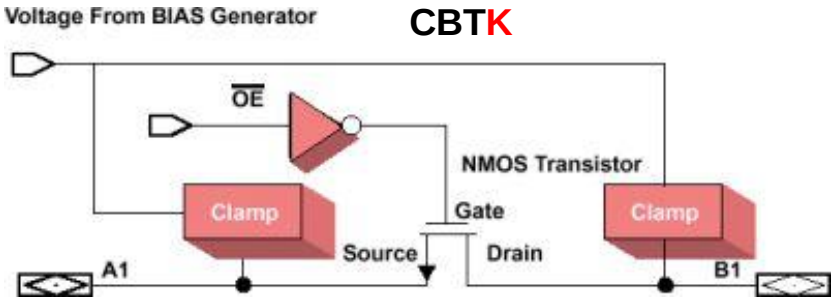
CBT with Additional Features

	CBT/C	CBTD	CBTS	CBTK	CBTH
Vcc(V)	4 – 5.5	4.5 – 5.5	4 – 5.5	4 –5.5	4 – 5.5
Speed	250 ps	250 ps	250 ps	250ps	250 ps
Benefits	Very Fast	Ext. Diode to Vcc	Improve Undershoot	Enhance Undershoot	Bus-Hold
Optimized Application	Isolation	Level-shifting	Isolation	Isolation	Latch data

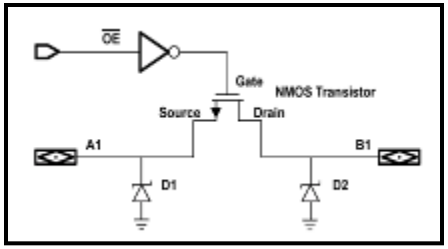
CBTD



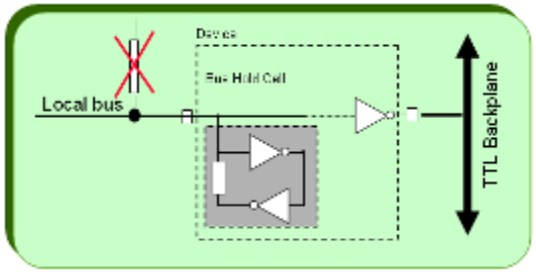
CBTK



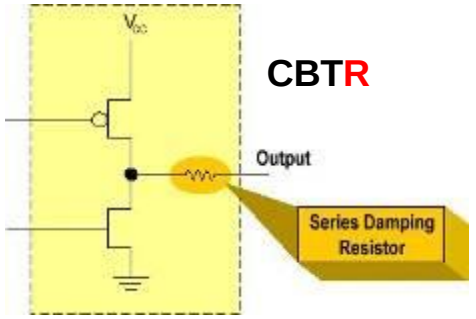
CBTS



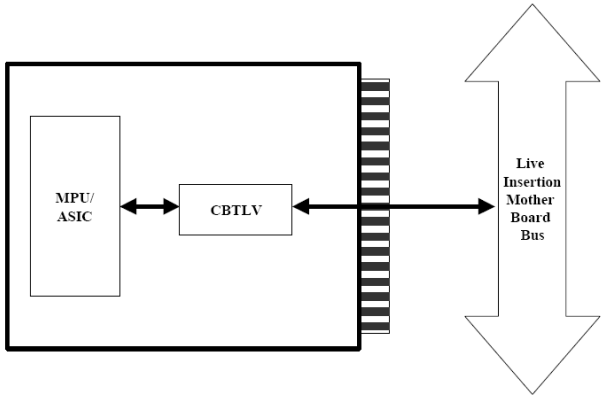
CBTH



CBTR



CBTLV Application

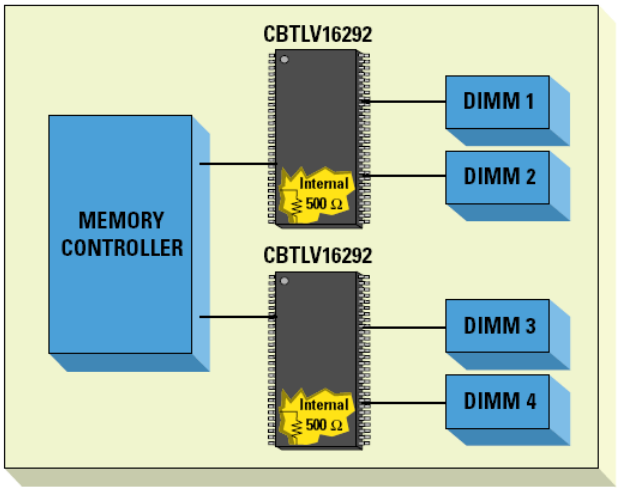


3.3V Live Insertion Bus

- **Backplane Module**
- **TTL/CMOS Camera Module**

Hot Swapping the Bus

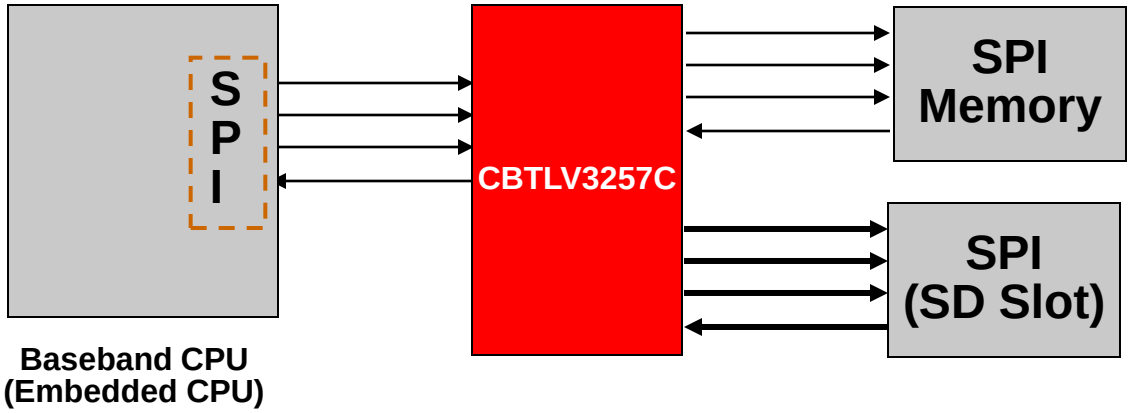
3.3-V Bus Switch Application



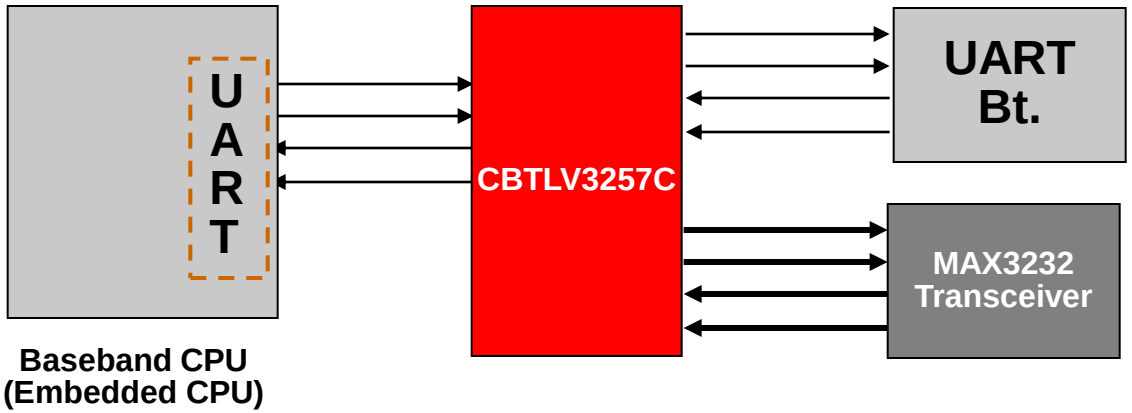
Memory Bus Data-bus loading sharing

- **CBT16292 is internal pull down when disconnected.**
- **Optimized on memory data-bus load sharing with Zero Delay switching the MUX.**

CBTLV Application

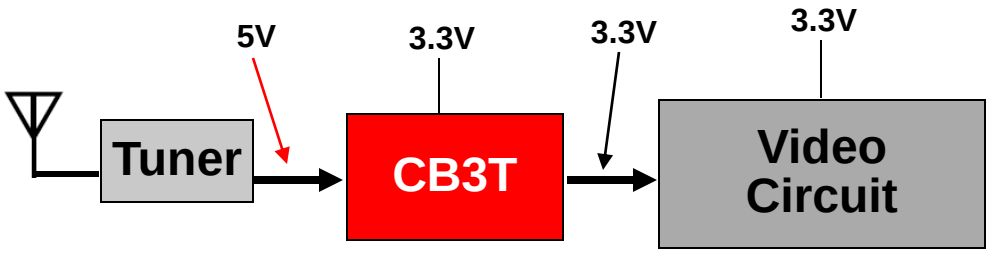


- Expand SPI Bus.
- SD Memory Bus Mux
- PDA Mobile Phone
- Portable Equipments

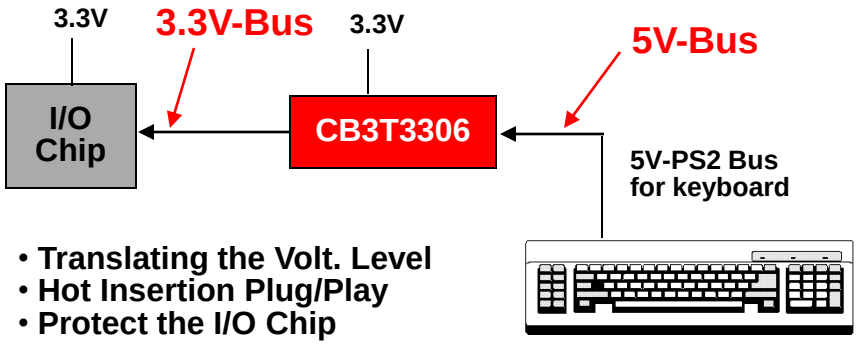


- Expand RS-232
- 2 Tx, 2 Rx
- Using Bi-directional Switch MUX

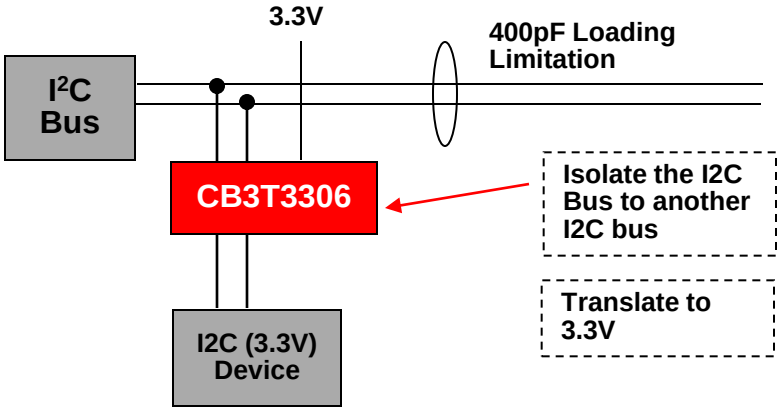
CB3T Application



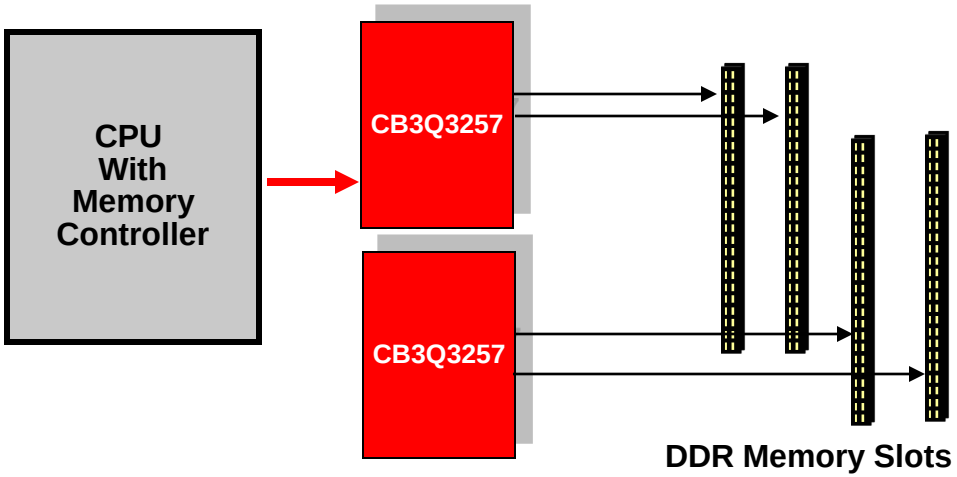
- Most Video Input from Tuner is 5V Voltage Level.
- CB3T can limit the output to 3.3V protect the Video Chip.



- Translating the Volt. Level
- Hot Insertion Plug/Play
- Protect the I/O Chip

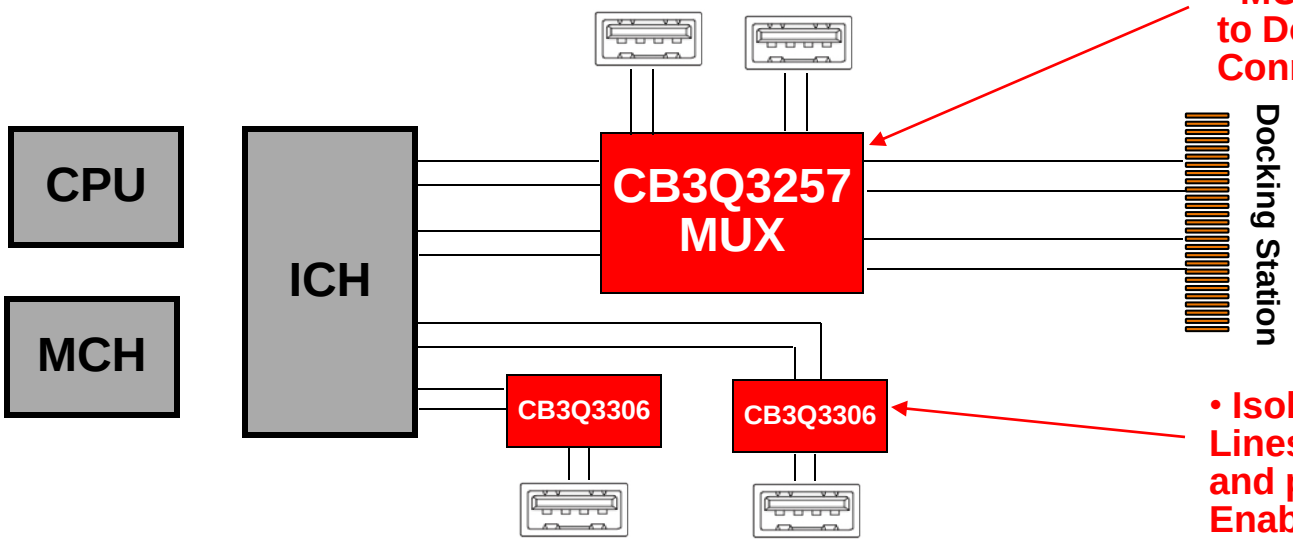


CB3Q Switch Application



Laser Memory Interleaving

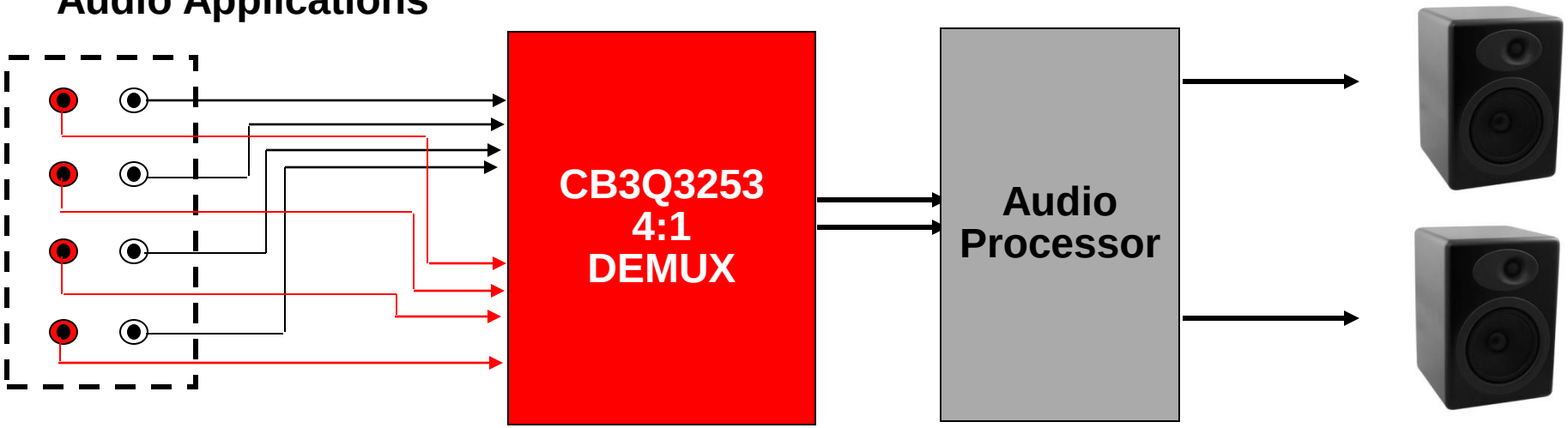
- High densities of memory at high speed will increase the loading huge data.
- CB3Q High Speed Switch MUC can share the loading of Address, RAS, CAS which are connecting to all Memory Chips.



- MUX High Speed USB 2.0 to Docking and USB Connector
- Isolating the D+ D- Data Lines and protect the chip and power saving with Enable Pin

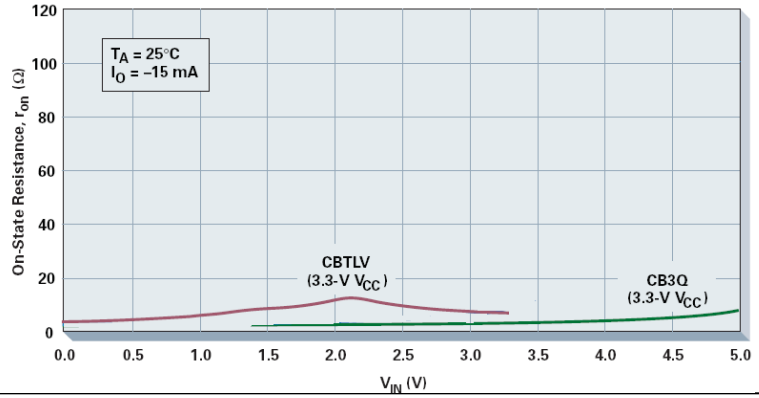
CB3Q Switch Application

Audio Applications

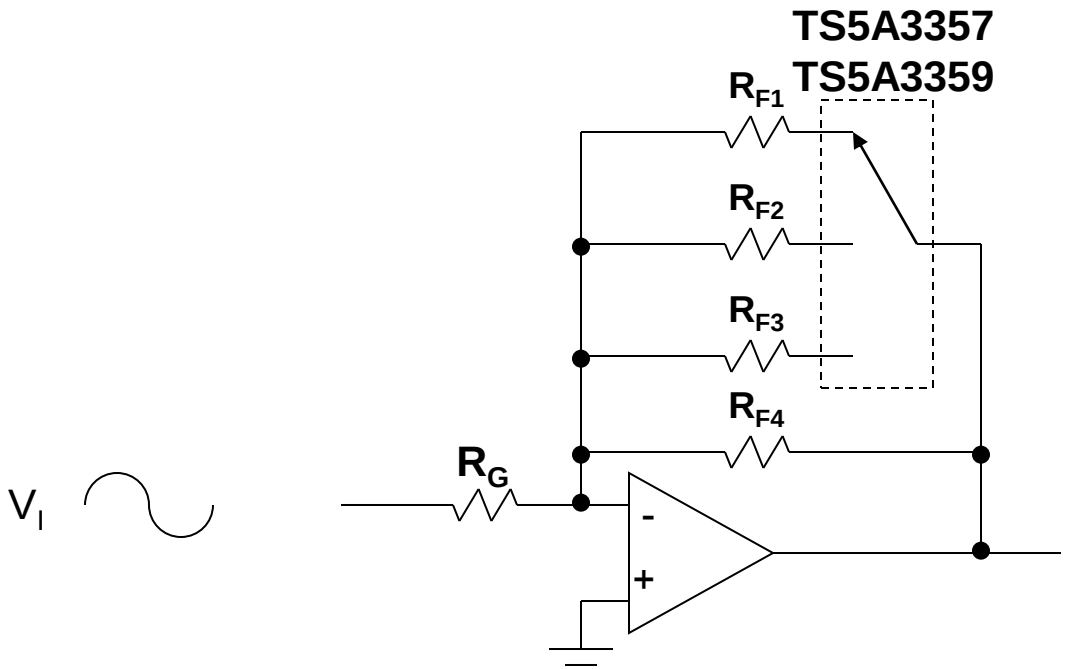


Internal Speaker

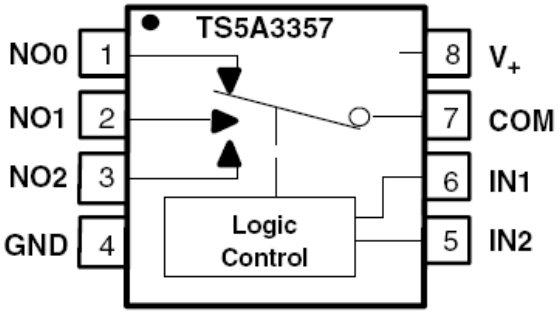
- **CB3Q is Ron (FLAT) which make Audio Signal (Analog) output less distortion.**



Applications - Single SP3T – Amplifier Gain Adjustment



Single SP3T – Amplifier Gain Adjustment



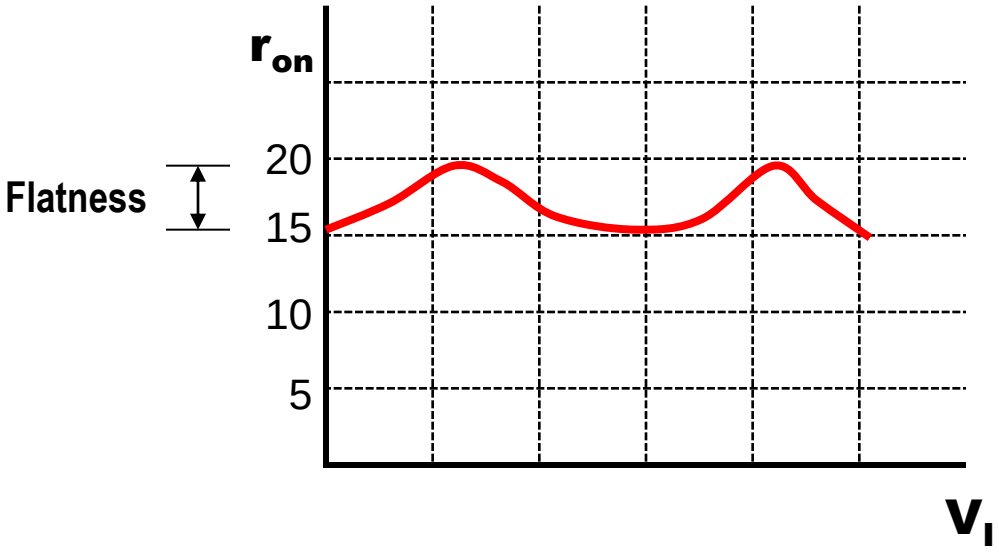
SM8 package currently in development!

Considerations:

1. R_{Fx} versus r_{on}
2. r_{on} flatness
3. $C_{I/O}$
4. Bandwidth, Off-Isolation, Cross-Talk

Parameter Definitions

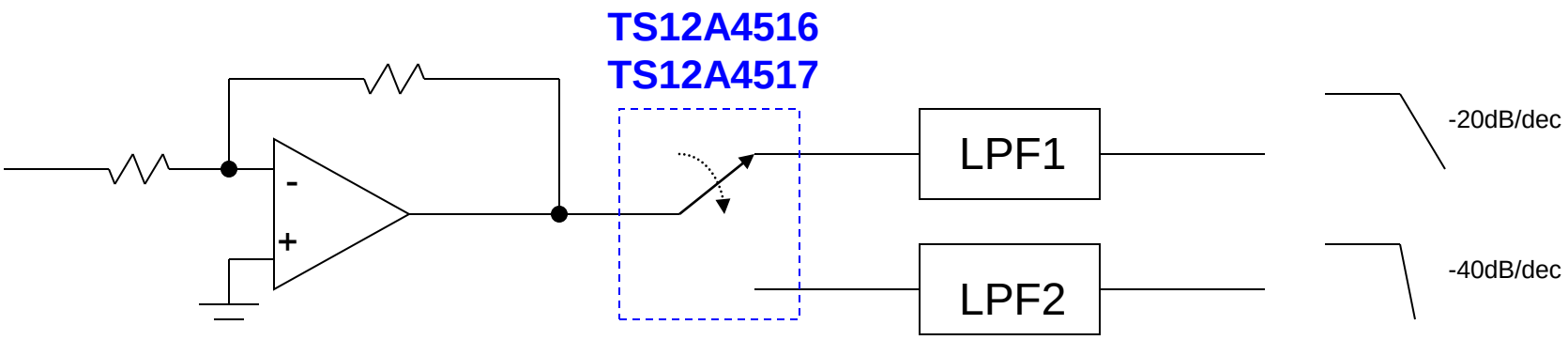
- **On-resistance** –The resistance inserted into the signal path as a result of the switch path being turned on.
- **On-resistance flatness** - Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions. Sometimes tested over the full range, or at fixed points where the variation is likely highest.



Flatness = 5 ohms

Analog Switch Applications

Single SPDT – Low Pass Filter Select



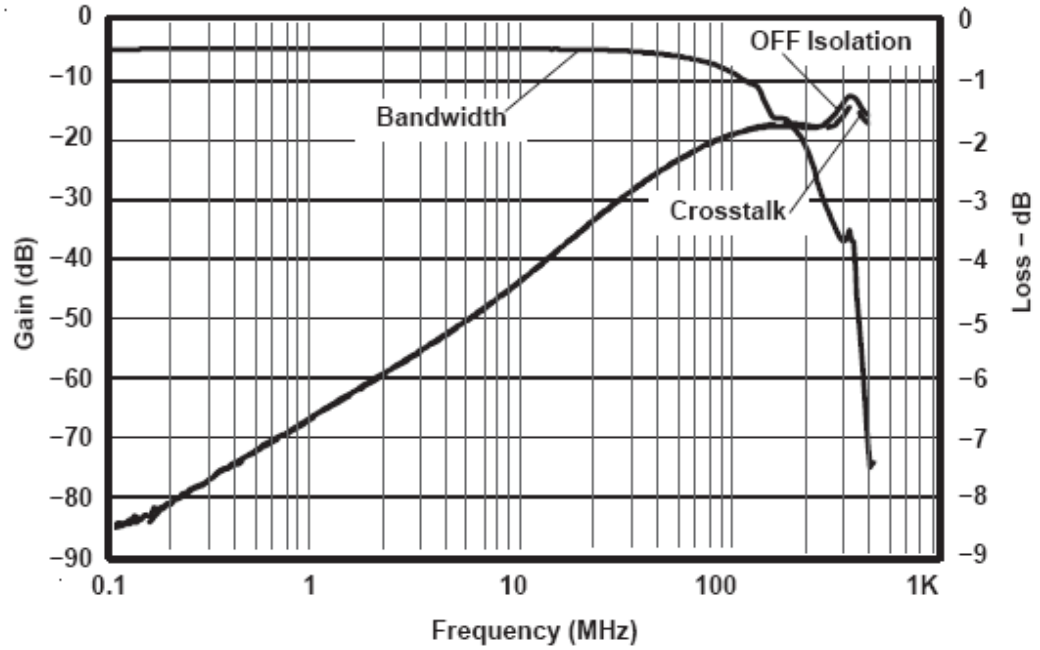
Single SPDT – Low Pass Filter Select

Considerations:

1. Bandwidth, Off-Isolation, Cross-Talk
2. Break-Before-Make Switching
3. $C_{I/O}$
4. r_{on}
5. r_{on} flatness

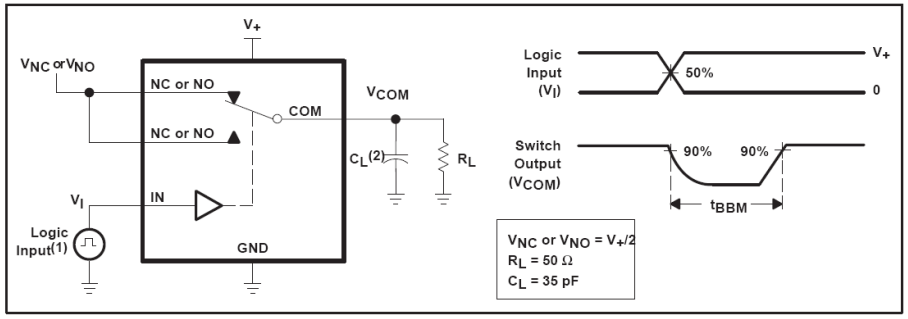
Parameter Definitions

- **Bandwidth** – The 3dB frequency response.
- **Cross-Talk** – A measurement of unwanted signal coupling from an ON channel to an OFF channel. This is measured in a specific frequency and in specified in dB.
- **Off-Isolation** – A measurement of OFF-state switch impedance. This is measured in dB at a specific frequency, with the corresponding channel in the OFF state.



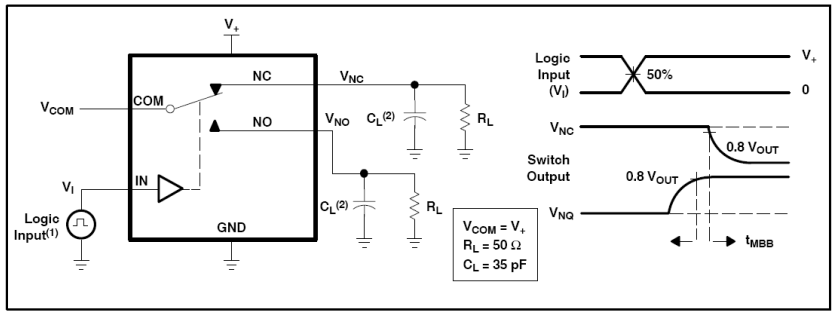
Parameter Definitions

- **Make-Before-Break (MBB) time** – Guarantees that in a multiplexer, two mux signal paths are never electrically connected when the signal path is changed by the select input. This parameter is measured under a specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO), when the control signal changes state.
- **Break-Before-Make (BBM) time** – Guarantees that in a multiplexer, two multiplexer paths are never open when the signal path is changed by the select input. This parameter is measured under a specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO), when the control signal changes state.



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 16. Break-Before-Make Time (t_{BBM})

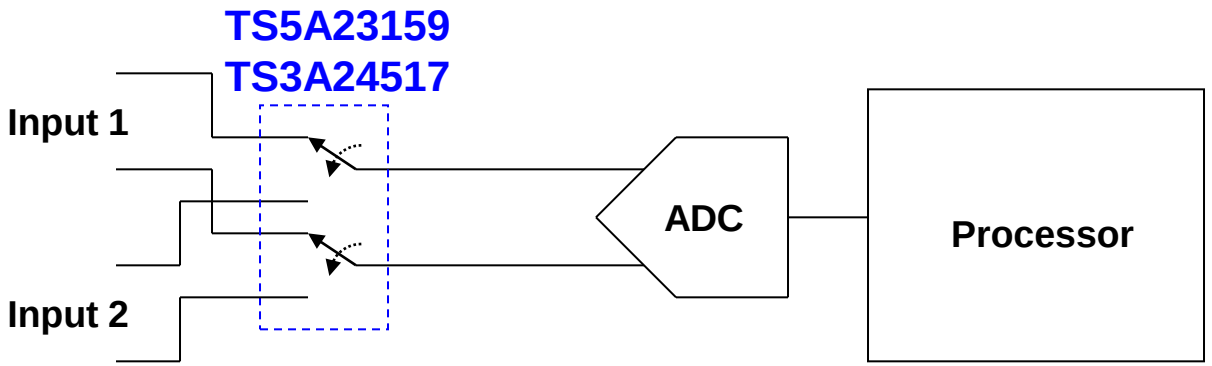


(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 18. Make-Before-Break Time (t_{MBB})

Analog Switch Applications

Dual SPDT – Mux ADC inputs



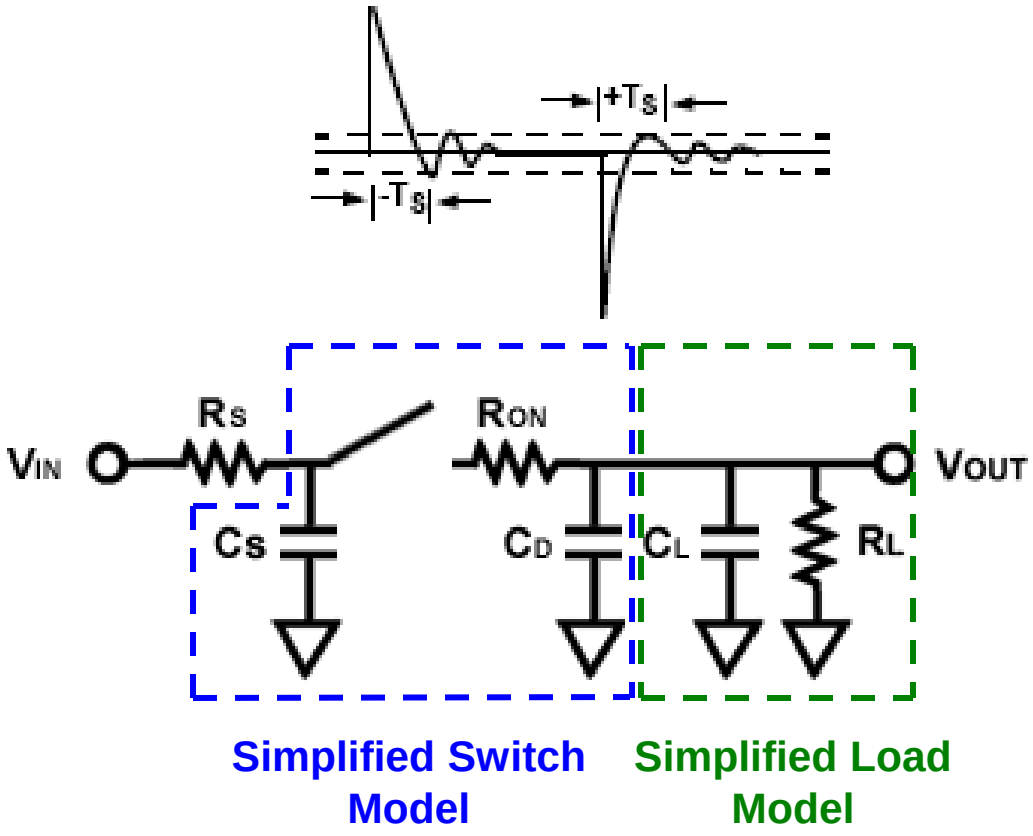
Dual SPDT – Mux ADC inputs

Considerations:

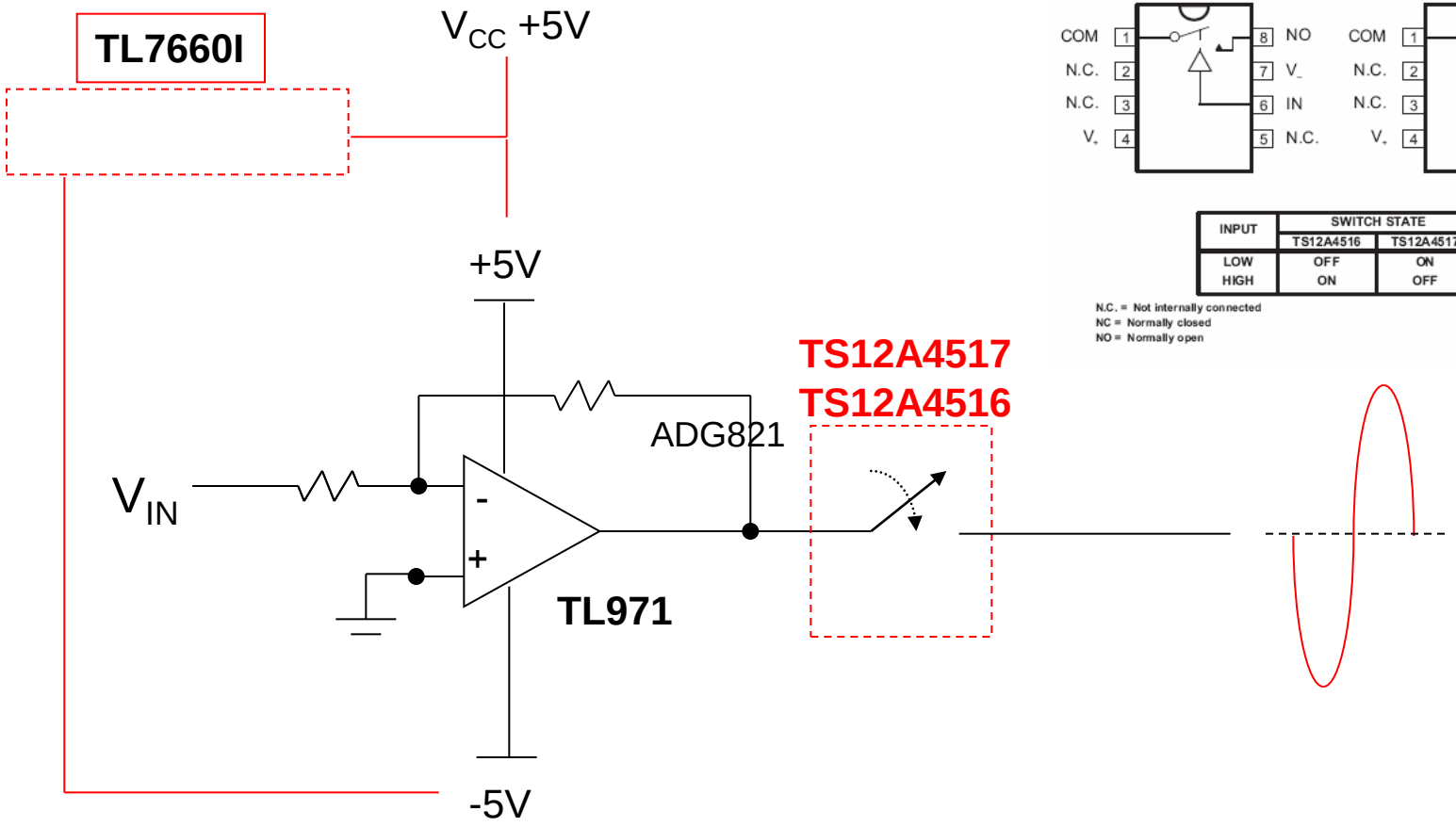
1. Settling Time
2. Bandwidth, Off-Isolation, Cross-Talk
3. Break-Before-Make Switching
4. $C_{I/O}$
5. r_{on}
6. r_{on} flatness
7. THD
8. Charge Injection

Parameter Definitions

- **Settling Time** – The time required for the switch output to settle within a given percentage of the final value following a change in the digital input level. Usually the worst-case settling time occurs when the switch is required to slew across its full dynamic range.



Application Example with Medium Voltage Analog Switches



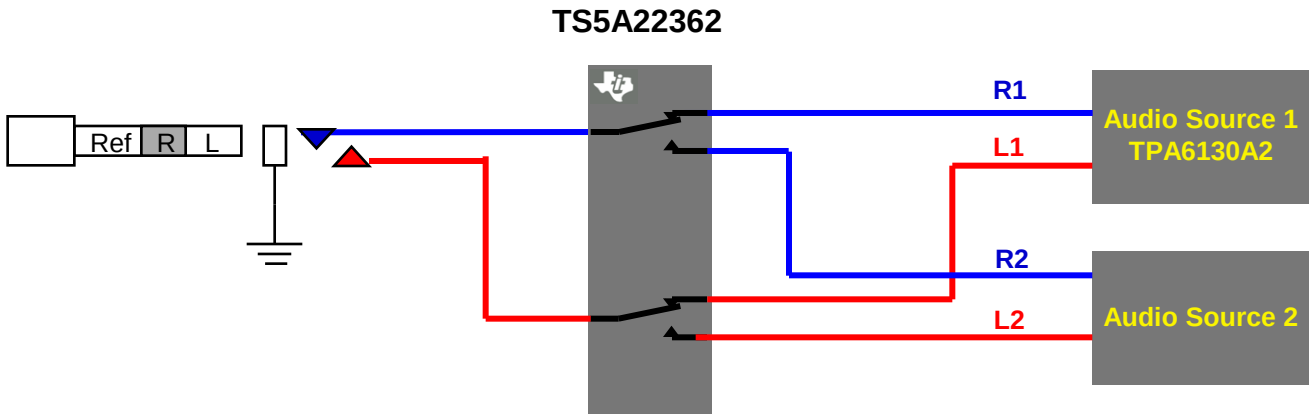
INPUT	SWITCH STATE	
	TS12A4516	TS12A4517
LOW	OFF	ON
HIGH	ON	OFF

N.C. = Not internally connected
NC = Normally closed
NO = Normally open

0.6-Ω Dual SPDT Analog Switch With Negative Rail Capability and Click-Pop Suppression for audio routing
TS5A22362, TS5A22364

Features

- ***Negative Signaling Capability : Analog I/O Range = V_+ - 5.5V to V+***
- **Internal Shunt Switch prevents audible click-and pop when switching between two sources (TS5A22364 only)**
- **Low ON-State Resistance (0.6-Ω typ or 0.8-Ω typ for TS5A22366)**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **2.3-V to 5.5-V Power Supply (V+)**
- **Packaging Options**
  - **10-WCSP (0.5mm pitch - YZP) 1.9 x 1.4**
  - **SON-10 (DRC) 3 x 3**
  - **VSSOP-10 (DGS) 4.9 x 3**



TI Signal Switch

Overview – 3 general categories available in the market

1. Digital "bus" Switches

- Designed to pass (or isolate) digital signal levels.
- Signal integrity is important, but some distortion is allowed
- Wide variety of pin counts (5-96 pins, 1-32 "bit" buses)

2. Analog Switches

- Designed to pass (or isolate) analog signals.
- Usually low pin count parts (5-16 pins)
- Provide analog specs similar to op amps (BW, X-Talk, Off-Isolation, THD)
- Major Suppliers:

3. Application Specific (aka "Specialty") Switches (ASSP)

- Targeted directly for use in application specific areas – Video, LAN, Network, USB, Audio, PCI Express, etc.
- More application specific specs than Digital or Analog

I²C Product Groups

GPIO expanders
I/Os, LED Blink

- 4, 8, 16 Bits I/O Expansions
- LED Driver (Programmable Blink Rate)
- 1.8V I²C Level with 5V Open-Drain

I²C
MUX/DEMUX

- I²C Bus Expands to 4 I²C Bus With Translation Function by Pull Up.

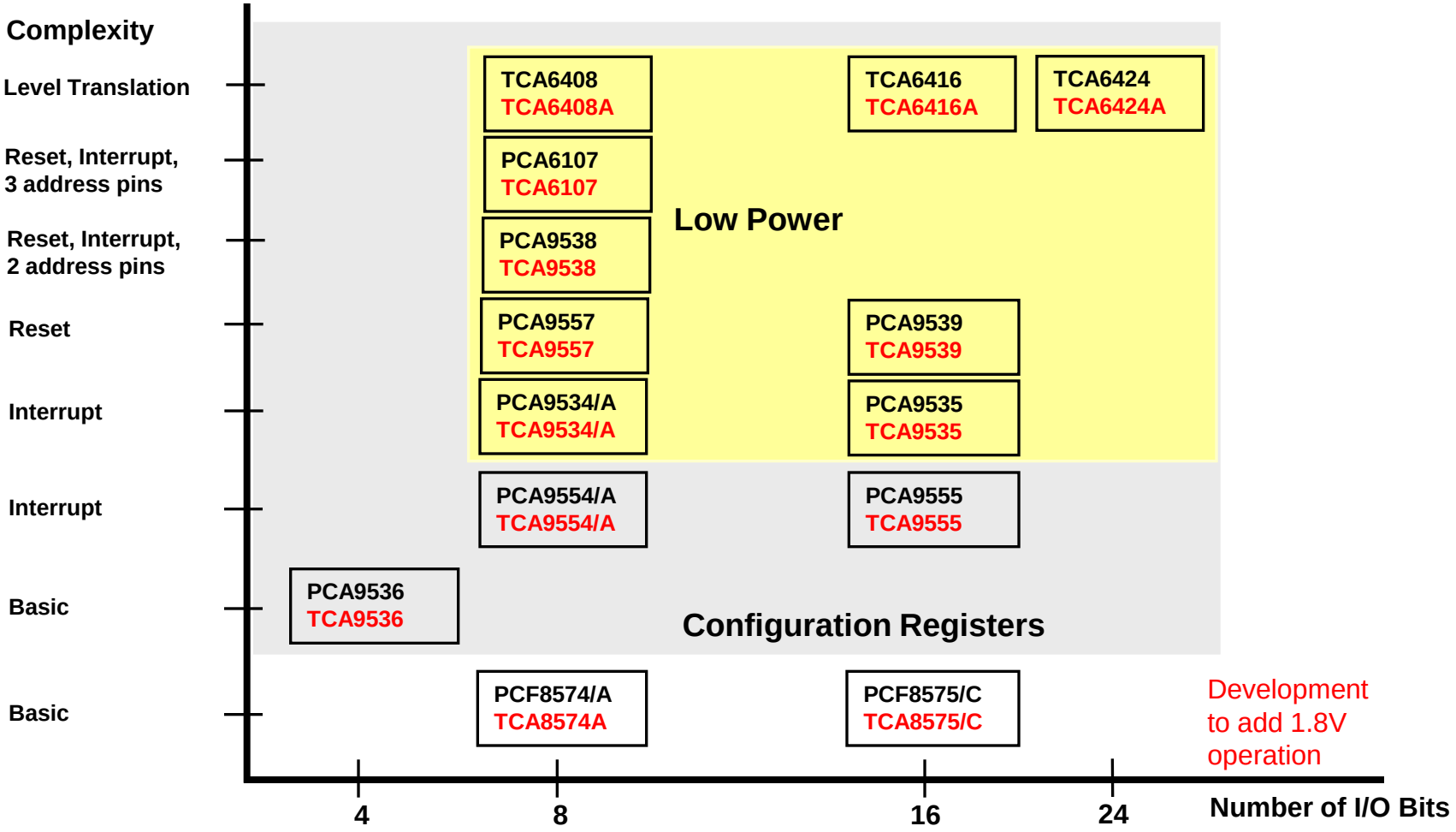
PCA9306 = I²C Level Translators

I2C
Buffer/Repeater

- P82B96 Bus Buffer Up to 20-M)
- PCA9515A Bus Repeater

I²C I/O Expanders

- General Purpose I²C I/O Expanders support low level control features
- Moving all devices into 1.8V operation-node for next-gen applications



TCA6408A, TCA6416A, TCA6424A
1.8-V I/O Expander w/ Interrupt & Reset

Features

- 8-, 16-, or 24-bit variants
- V_{CC} range of 1.65V to 5.5V on I^2C and I/O side
- Bidirectional voltage-level translation and GPIO expansion between
  - 1.8V SCL/SDA and 1.8V, 2.5V, 3.3V, or 5V P Port
  - 2.5V SCL/SDA and 1.8V, 2.5V, 3.3V, or 5V P Port
  - 3.3V SCL/SDA and 1.8V, 2.5V, 3.3V, or 5V P Port
  - 5V SCL/SDA and 1.8V, 2.5V, 3.3V, or 5V P Port
- 400 kHz operation

Benefits

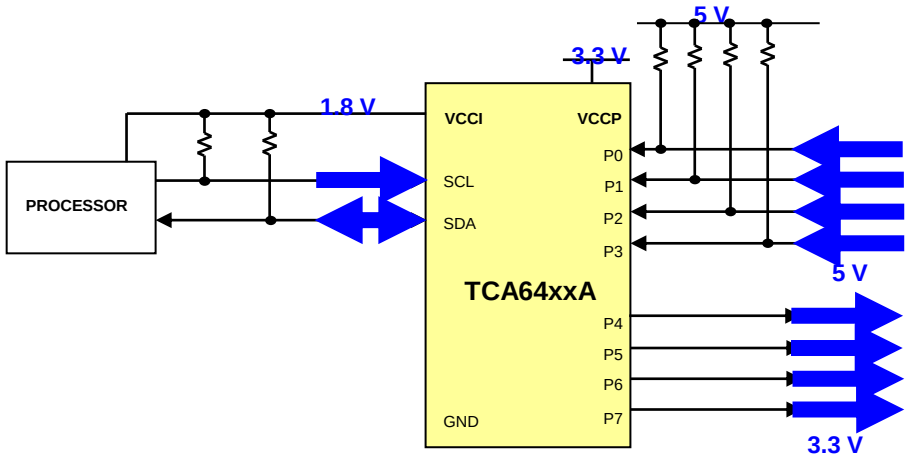
- Built-in voltage level translation eliminates the need for external translators on the I^2C and I/O side
- Can interface with legacy and next generation processors
- Lower power consumption

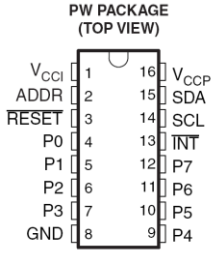
Applications

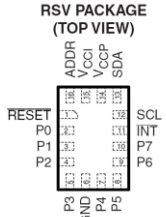
- Housekeeping Functions
  - Temperature, Fan, Audio Control
  - Humidity Sensors
  - LED Status
  - Hardware Control Monitor
- Keypad control

Packages

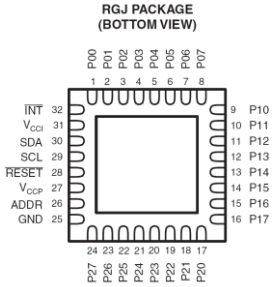
- TCA6408A – Standard TSSOP (PW), QFN (RSV) – 1.8 x 2.6 mm
- TCA6416A – Standard TSSOP (PW), QFN (RTW) – 4 x 4 mm, BGA (ZQS) – 3 x 3 mm
- TCA6424A – QFN (RGJ) – 5 x 5 mm



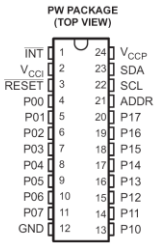


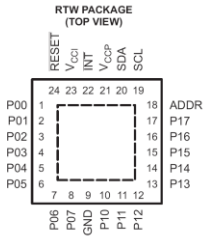


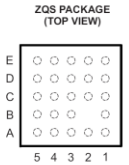
TCA6408A



TCA6424A







TCA6416A

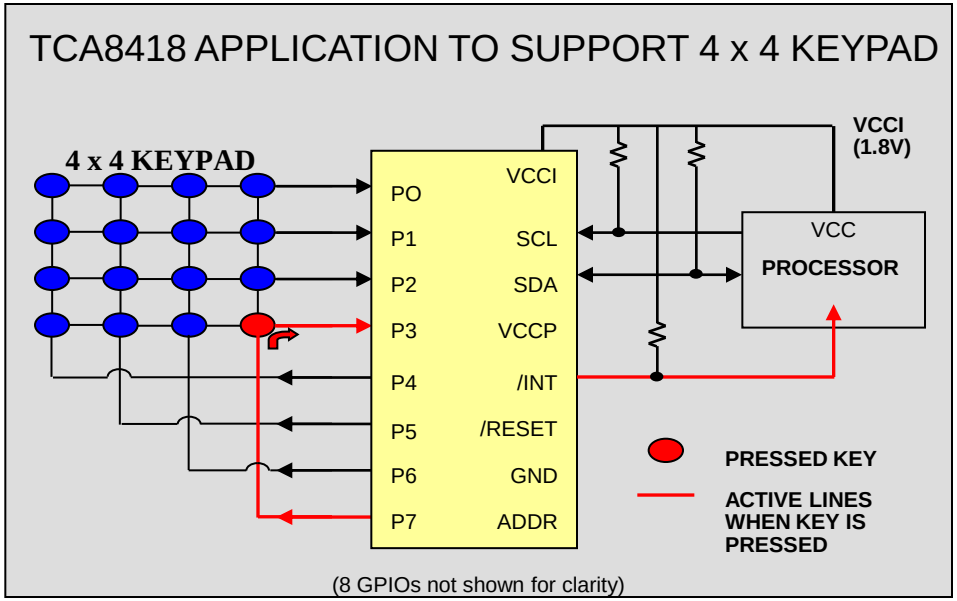
TCA6408A	TCA6416A	TCA6424A
Product Released	Product Released	Call For More Info

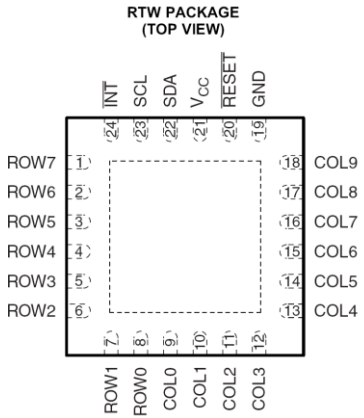
Texas Instruments

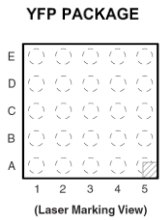
TCA8418: Next Gen Keypad Controller

Features

- 18 GPIOs can be Configured into Eight Inputs and Ten Outputs to Support an 8 x 10 Keypad Array (80 Buttons)
- ESD Protection Exceeds IEC61000-4-2 on all 18 GPIOs:
  - ±15-kV Human Body Model (HBM)
  - ±8-kV IEC61000-4-2, Contact Discharge
  - ±15-kV IEC61000-4-2, Air-Gap Discharge
- 10 Byte FIFO to Store 10 Key Presses and Releases
- Supports 1-MHz Fast Mode Plus I2C Bus
- Open-Drain Active-Low Interrupt Output, Asserted when Key is Pressed and Key is Released
- I/Os not used for keypad control can be used as GPIOs
- Ultra-small Packages:
  - 24-pin RTW Package (QFN) – 4mm x 4mm
  - 25-ball YFP Package (WCSP) – 2mm x 2mm







I^2C Muxes, Switches and Buffers

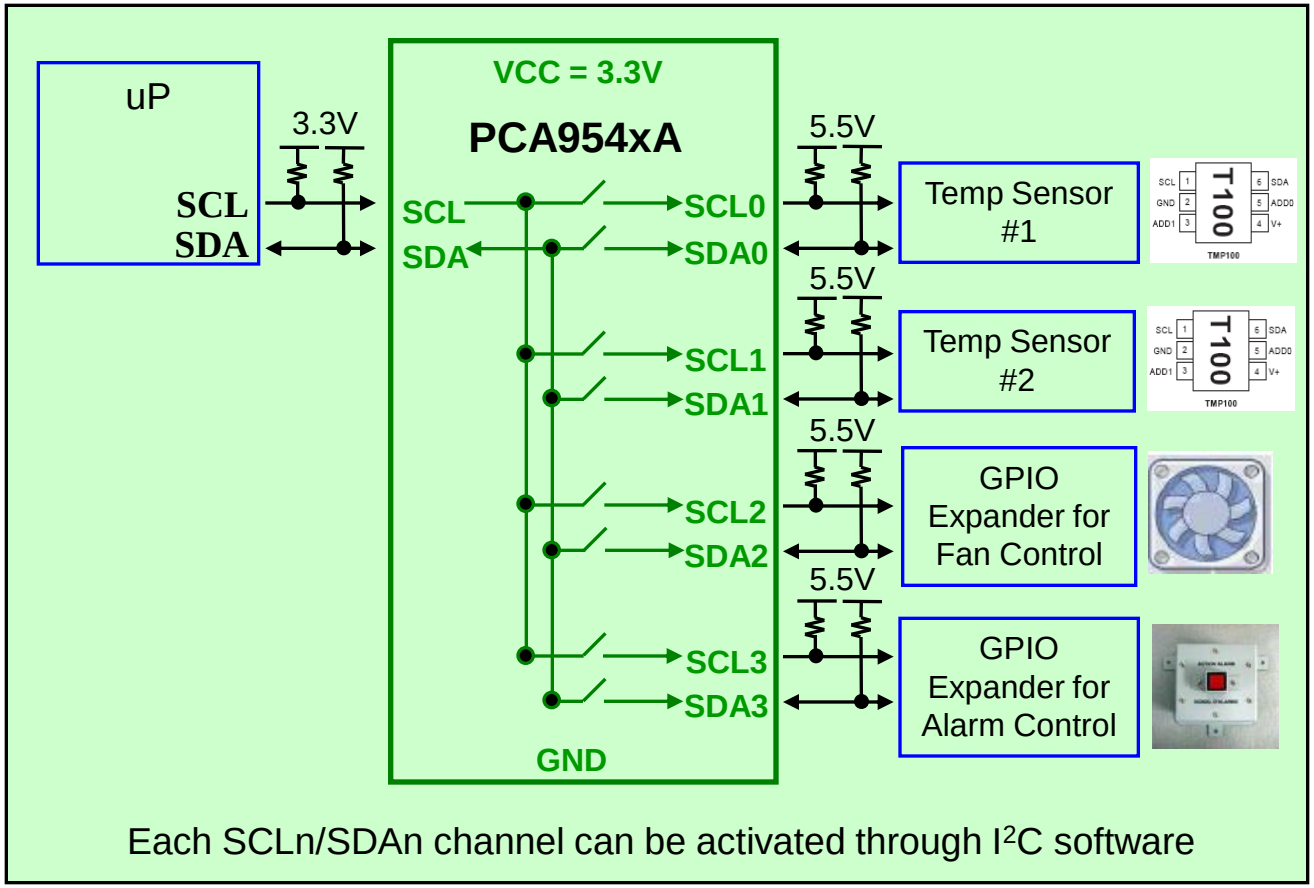
I²C Multiplexers and Switches

Resolves I²C address conflicts.
The microprocessor can select and activate 1 of the 2 temp sensors based on system area that needs to be monitored.

Can isolate a section on the I²C Bus.
If the system temperature is at the optimal level, SCL3/SDA3 can be isolated such that the alarm system is deactivated.

Saves GPIO pins on microprocessor as each SCLn/SDAn channel is activated or isolated through the I²C software

Supports voltage level translation between 2.5V, 3.3V and 5V buses which is essential in mixed voltage I2C systems. Here, the microprocessor is at 3.3V while the peripheral components need to operate at 5V.



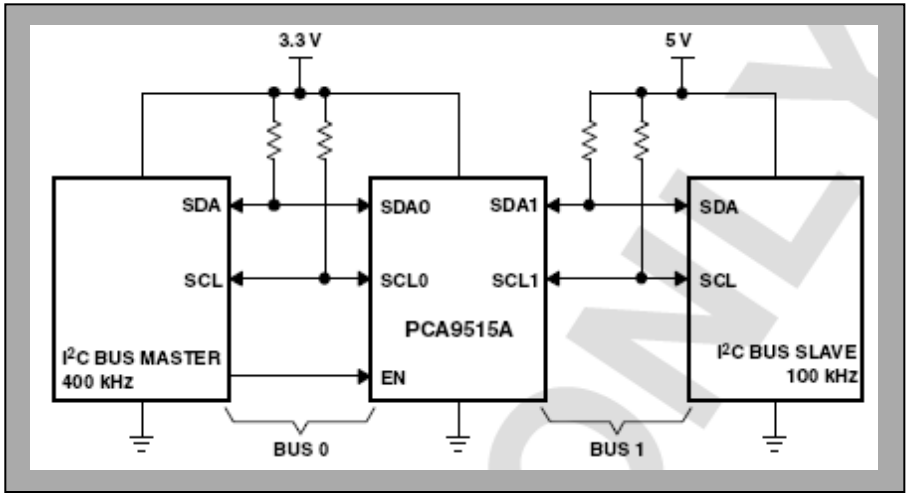
I²C Multiplexers and Switches Portfolio

I²C Muxes & Switches	Max Frequency (kHz)	I²C Address	Vcc Range (V)	Number of Channels	Additional Features			
					Interrupt	Reset	5-V Tolerant I/O	Open-drain I/Os
PCA9544A	400	1110 xxx	2.3 to 5.5	4	Yes		Yes	Yes
PCA9545A	400	1110 0xx	2.3 to 5.5	4	Yes	Yes	Yes	Yes
PCA9546A	400	1110 xxx	2.3 to 5.5	4		Yes	Yes	Yes
PCA9548A	400	1110 xxx	2.3 to 5.5	8		Yes	Yes	Yes
PCA9543A	400	1111 0xx	2.3 to 5.5	2	Yes	Yes	Yes	Yes
TCAxxxx	400	xxxx xxx	2.3 to 5.5	16	Yes	Yes	Yes	Yes
TCAxxxx (w/ Hot-swap)	400	xxxx xxx	2.3 to 5.5	2	Yes	Yes	Yes	Yes
TCAxxxx (w/ Hot-swap)	400	xxxx xxx	2.3 to 5.5	4	Yes	Yes	Yes	Yes

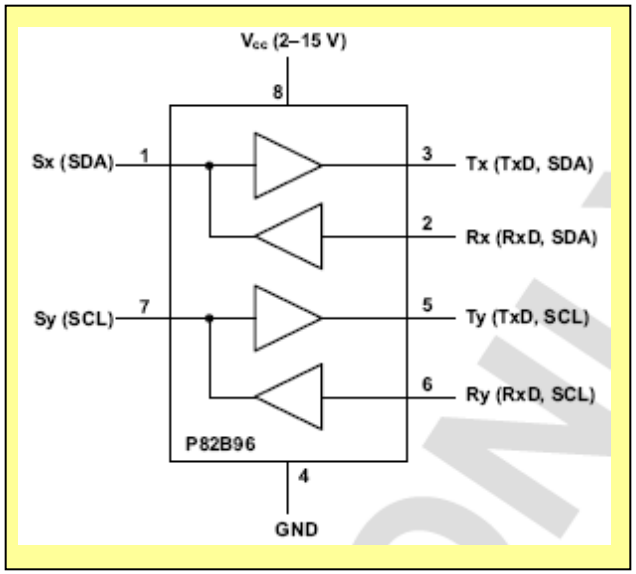
Future Trends:

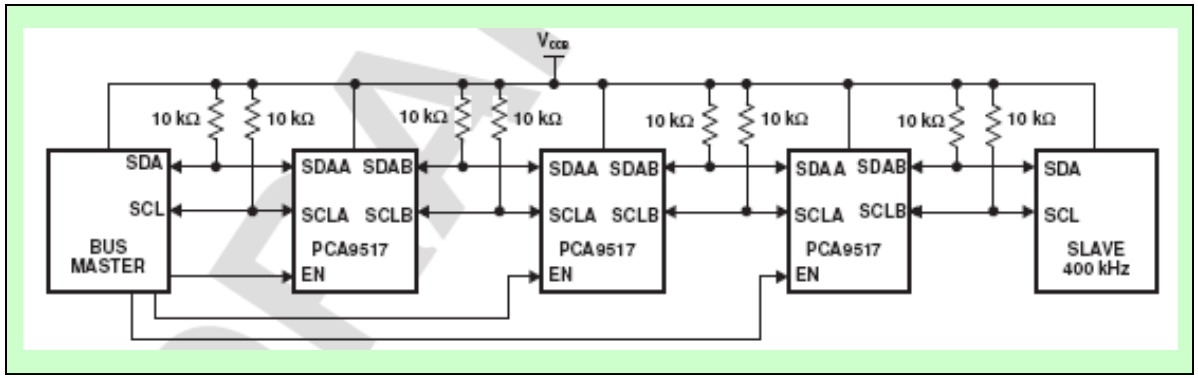
I²C switch with hot-swap capability

I²C Buffers and Repeaters



- Extends the I²C bus without degradation of system performance:
  - **PCA9515A/PCA9517**: Enables two buses of 400-pF bus capacitance to be connected in an I²C application
    - 2 PCA9517 devices can be connected together
  - **P82B96**: Enables bus of 400pF capacitance on I²C side and 4000pF on slave side. Also, useful for operation with opto-couplers.
- I²C Bus Expansion
- Resolve I²C Address Conflicts
- Supports voltage level translation between 2.5V, 3.3V and 5V buses which is essential in mixed voltage I²C systems



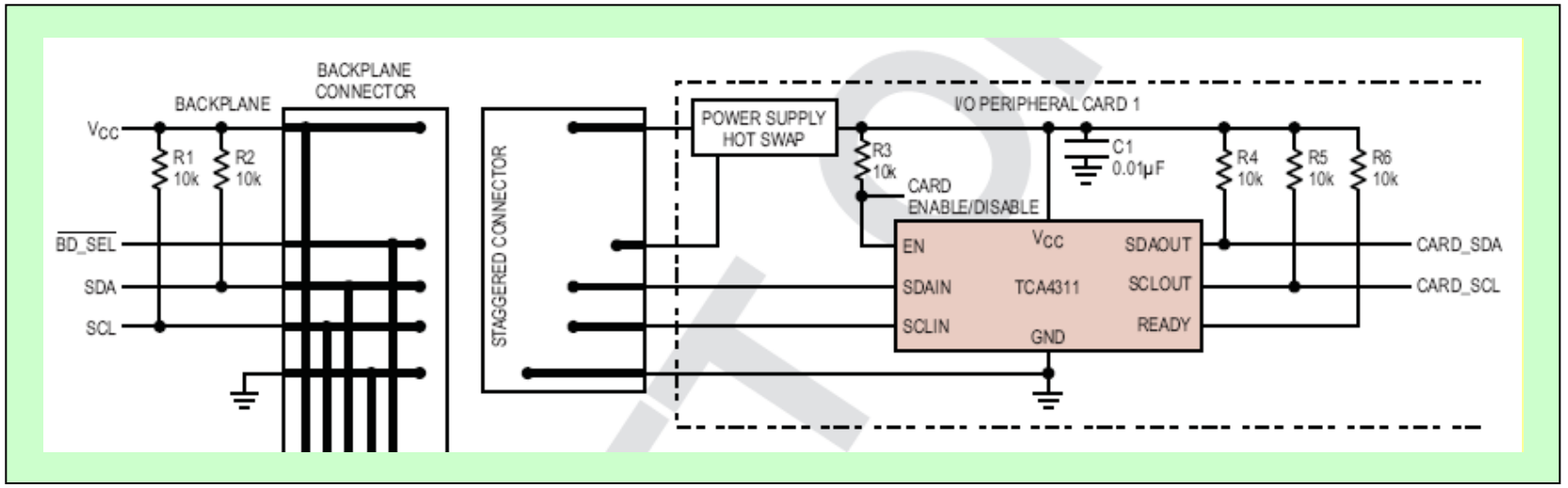


I²C Buffers Portfolio

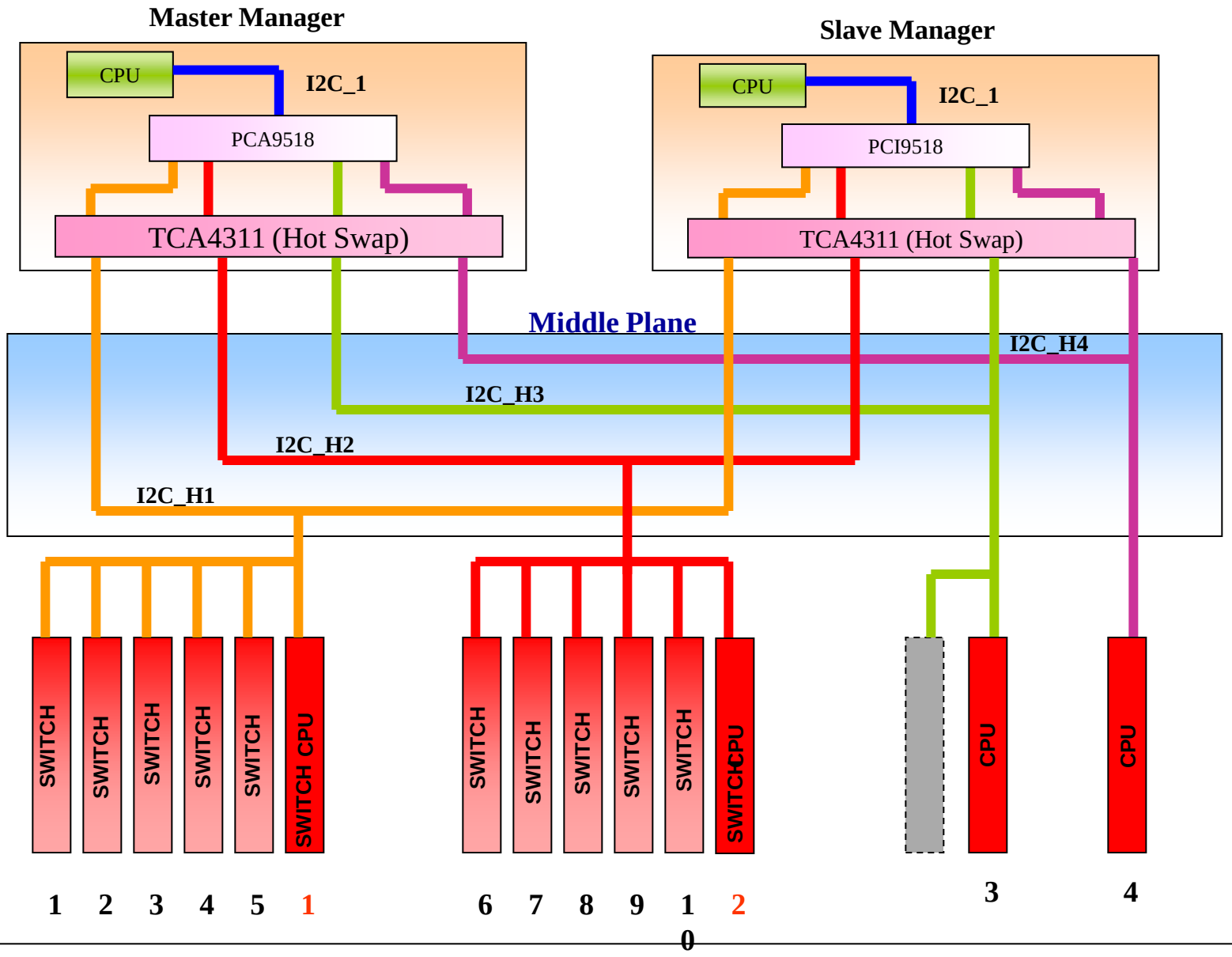
Device	Freq. (kHz)	Pin	IN/OUT (I²C)	Bus-Capacitance	Vcc (V)	I²C Level Shift Range					5V I/O Tolerant	Enable Pins	QSOP/SSOP	SOIC	TSSOP	MSOP	DCT	QFN	BGA
						>1.8V	2.5V	3.3V	5V	Max									
PCA9515A	400	8	1:1	400pF	2.3 to 5.5		✓	✓	✓		✓	1		o	o	o	o	o	
PCA9517	400	8	1:1	400pF	VccA: 0.9 to 5.5 VccB: 2.7v to 5.5	✓	✓	✓	✓		✓	1		o		o			
PCA9518	400	20	1:5	400pF	3V to 3.6		✓	✓	✓		✓	4	o	o	o				
P82B96	400	8	1:1	4000pF	2 to 15		✓	✓	✓	15	20-M Cable			o	o	o			
P82B715	400	8	1:1	3000pF	3 to 12			✓	✓	12	50-M Cable			o					
TCA4311	400	8	1:1	400pF	2.7 to 5.5			✓	✓		Hot Swap			o		o			

TCA4311 – Hot-Swappable I2C-Bus Buffer

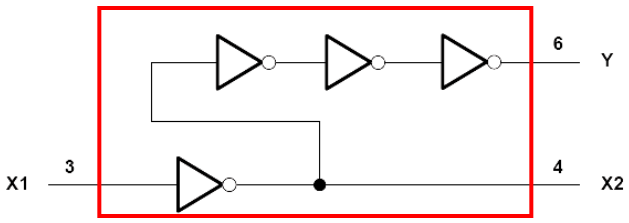
- Supports I/O card insertion into a live backplane without corruption of the data and clock busses
- 1 V Pre-charge on all SDA and SCL Lines
  - minimizes the worst-case voltage differential these pins will see at the moment of connection
  - minimizes the amount of disturbance caused by the I/O card
- Bi-directional buffering, keeping the backplane and card capacitances isolated



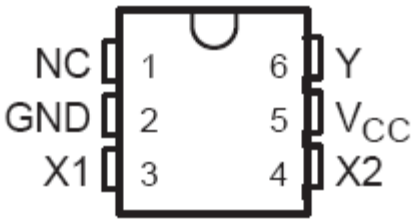
I²C-Bus Hot-Swappable Buffer-Channel



LVC1GX04 (Crystal OSC Driver)

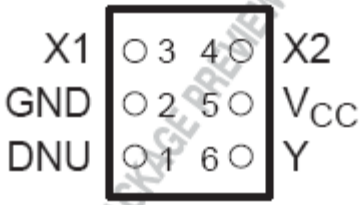


DBV OR DCK PACKAGE
(TOP VIEW)



NC – No internal connection

YEP OR YZP PACKAGE
(BOTTOM VIEW)



DNU – Do not use

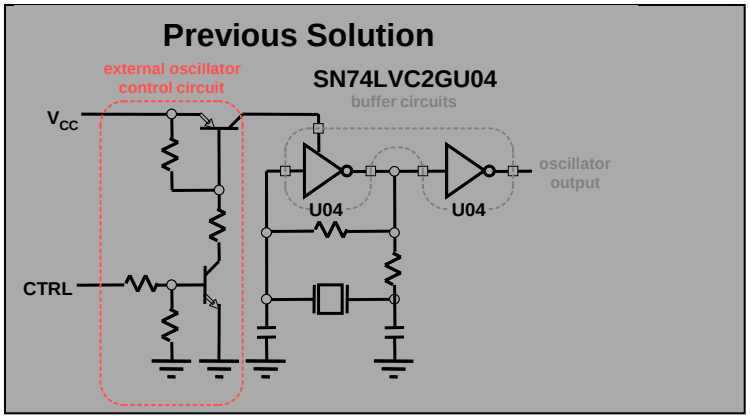
Features:

- Available in Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- One Unbuffered Inverter (SN74LVC1GU04) and One Buffered Inverter (SN74LVC1G04)
- Suitable for Commonly Used Clock Frequencies:
  - 15 kHz, 3.58 MHz, 4.43 MHz, 13 MHz, 25 MHz, 26 MHz, 27 MHz, 28 MHz
- Max t_{pd} of 2.4 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

LVC1404 (OSC Buffer with Enable)

Benefits:

- Can set CLK Output Range by Vcc.
- Can filter Clock Noise by Driving.
- Control Pin to enable/disable Clock.
- Convert to a single Clock Output
- from XIN and XOUT.
- Additional LVC1G14 integrated



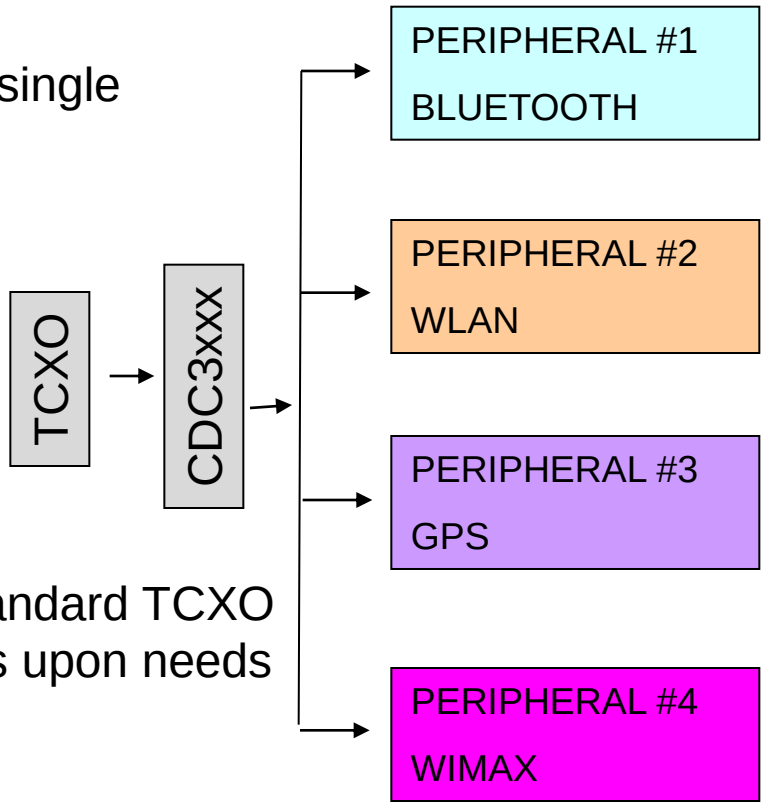
Features:

- Up to 28Mhz Common Frequency.
- Wide Operating Voltage range 1.65V to 5.5V.
- 24mA Output Driving at 3.3V.
- Integrated with Dual LVC1GU04 with Control Circuit enable/disable Clock Output.
- Smaller Package US8(DCT), SM8(DCU).
- ESD Protection HBM 2KV

Clock Tree Solution

Board Space:
Multiple TCXOs, VCTCXOs are replaced with a single centralized clock distributor packaged in CSWP or SMD or QFN

Power Consumption :
Each output is individually switchable
An internal LDO acts as TCXO switch



Noise :
We guarantee the same PN performances of standard TCXO
We offer both sine-wave or square-wave outputs upon needs

Price:
If you technically like our solution you will like our price even more

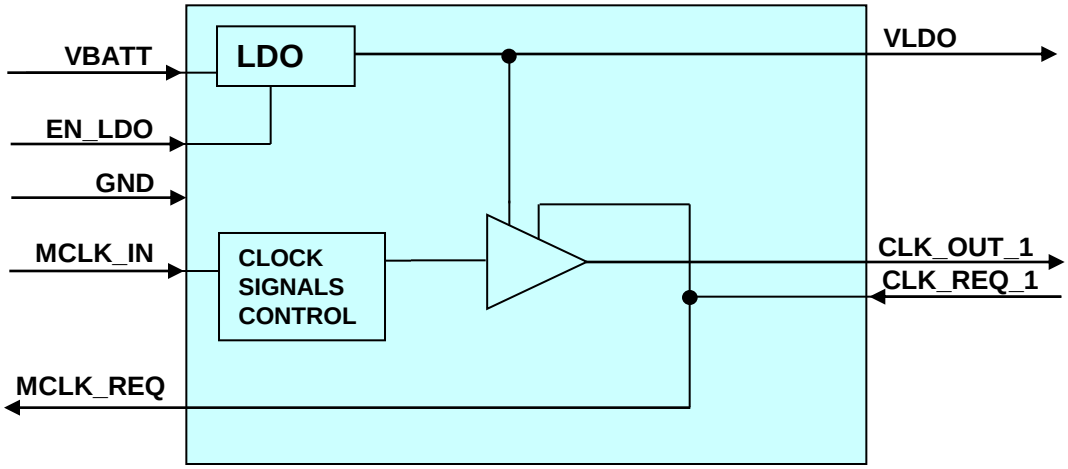
CDC3RL01

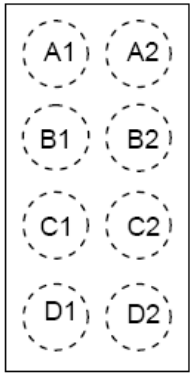
Sampling Now

1:1 Channel Clock buffer with LDO

FEATURES

- Fans out the master clock signal (from the processor) to 1 clock output based on external clock request
- Tight jitter specifications
  - 10 ps (typ) for output peak-to-peak jitter
  - Superior phase noise of -143 dBc/Hz
- Supports output load of 10 pF to 50 pF
- Supports an output rise time of 1 ns to 5 ns
- LDO specs:
  - 50 mA
  - 1.8 V Output Voltage
  - VBATT of 2.3 V to 5.5 V
- 8-ball WCSP (YFP): 1.6 mm x 0.8 mm, 0.4 mm pitch





	1	2
A	VBATT	EN_LDO
B	VLDO	CLK_OUT
C	GND	CLK_REQ
D	MCLK_IN	MCLK_REQ

BENEFITS

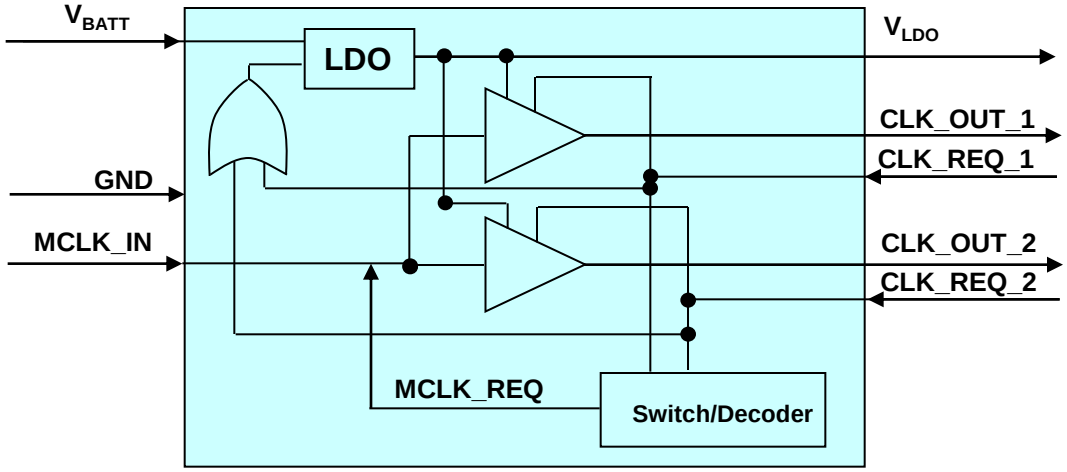
- Inputs can be sine or square waveforms
- Outputs are square waveforms
- Independent outputs enable for power saving
- Internal LDO acts as TCXO switch

CDC3RL02

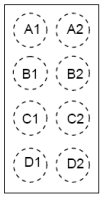
1:2 Channel Clock buffer with Integrated LDO

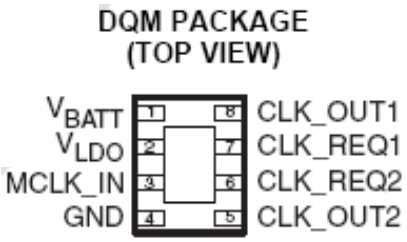
FEATURES

- Fans out the master clock signal (from the processor) to 2 clock outputs based on external clock requests
- Tight jitter specifications
  - 10 ps (typ) for output peak-to-peak jitter
  - Superior phase noise of -143 dBc/Hz
- Supports output load of 10 pF to 50 pF
- Supports an output rise time of 1 ns to 5 ns
- LDO specs:
  - 50 mA
  - 1.8 V Output Voltage
  - VBATT of 2.3 V to 5.5 V
- 8-ball WCSP (YFP): 1.6 mm x 0.8 mm, 0.4 mm pitch **Engineering samples AVAILABLE**
- 8-pin DQM: 1.2 mm x 1.8 mm, 0.4-mm Pitch MicroQFN **Engineering samples in 1Q'10**



	1	2
A	VBATT	CLK_OUT_1
B	VLDO	CLK_REQ_1
C	MCLK_IN	CLK_REQ_2
D	GND	CLK_OUT_2



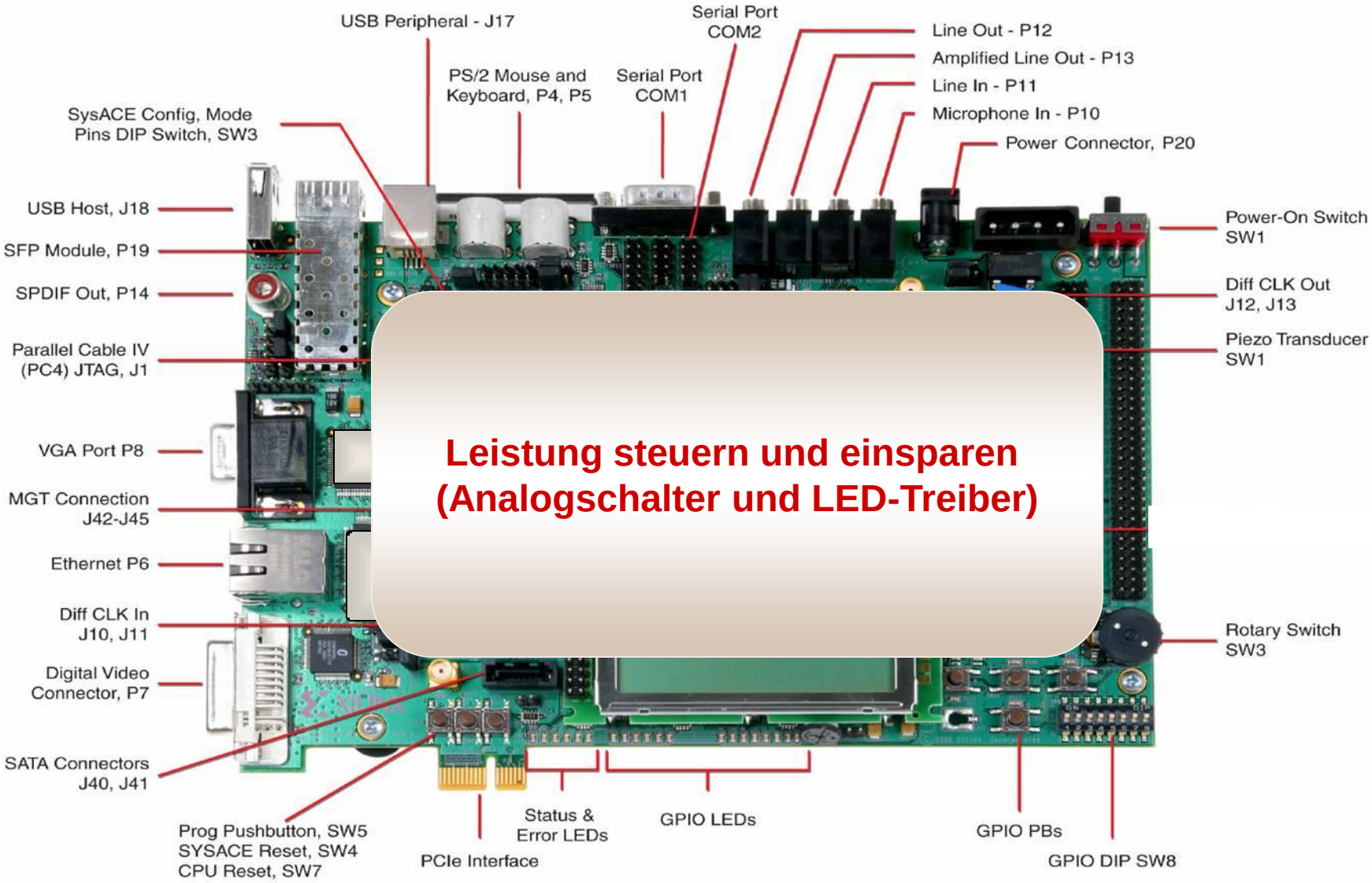


BENEFITS

- Inputs can be sine or square waveforms
- Outputs are square waveforms
- Independent outputs enable for power saving
- Internal LDO acts as TCXO switch

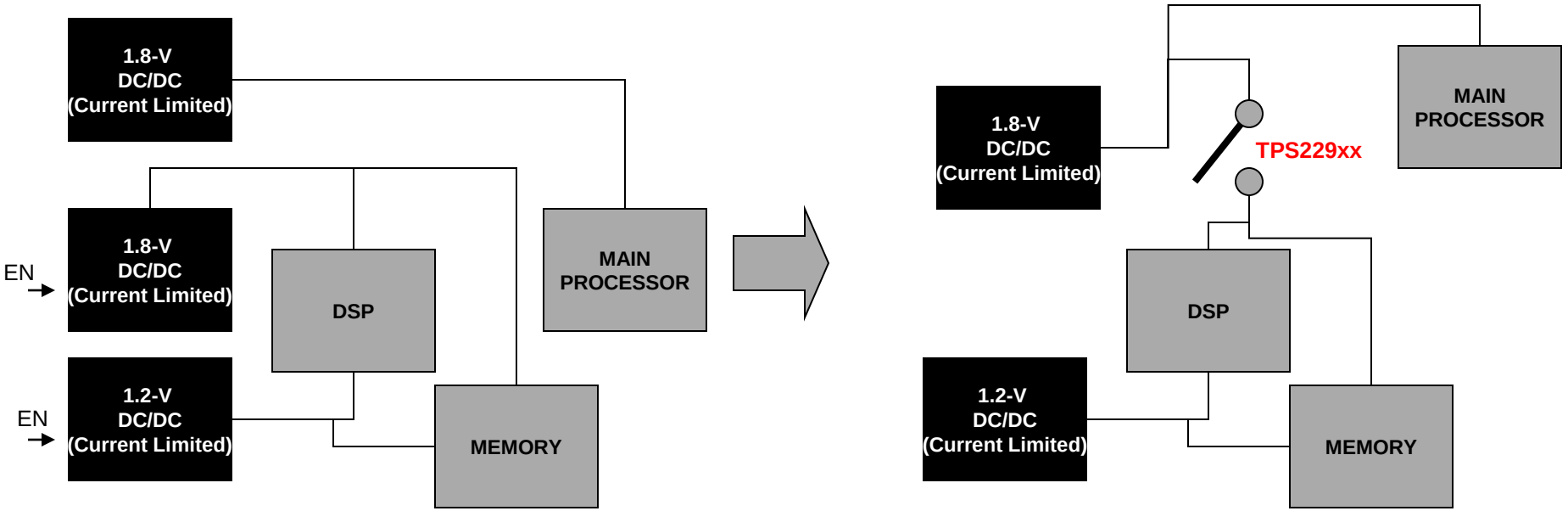
Sampling Now
4Q'09 RTM

Texas Instruments



Leistung steuern und einsparen (Analogschalter und LED-Treiber)

Application Example



Conventional Solution

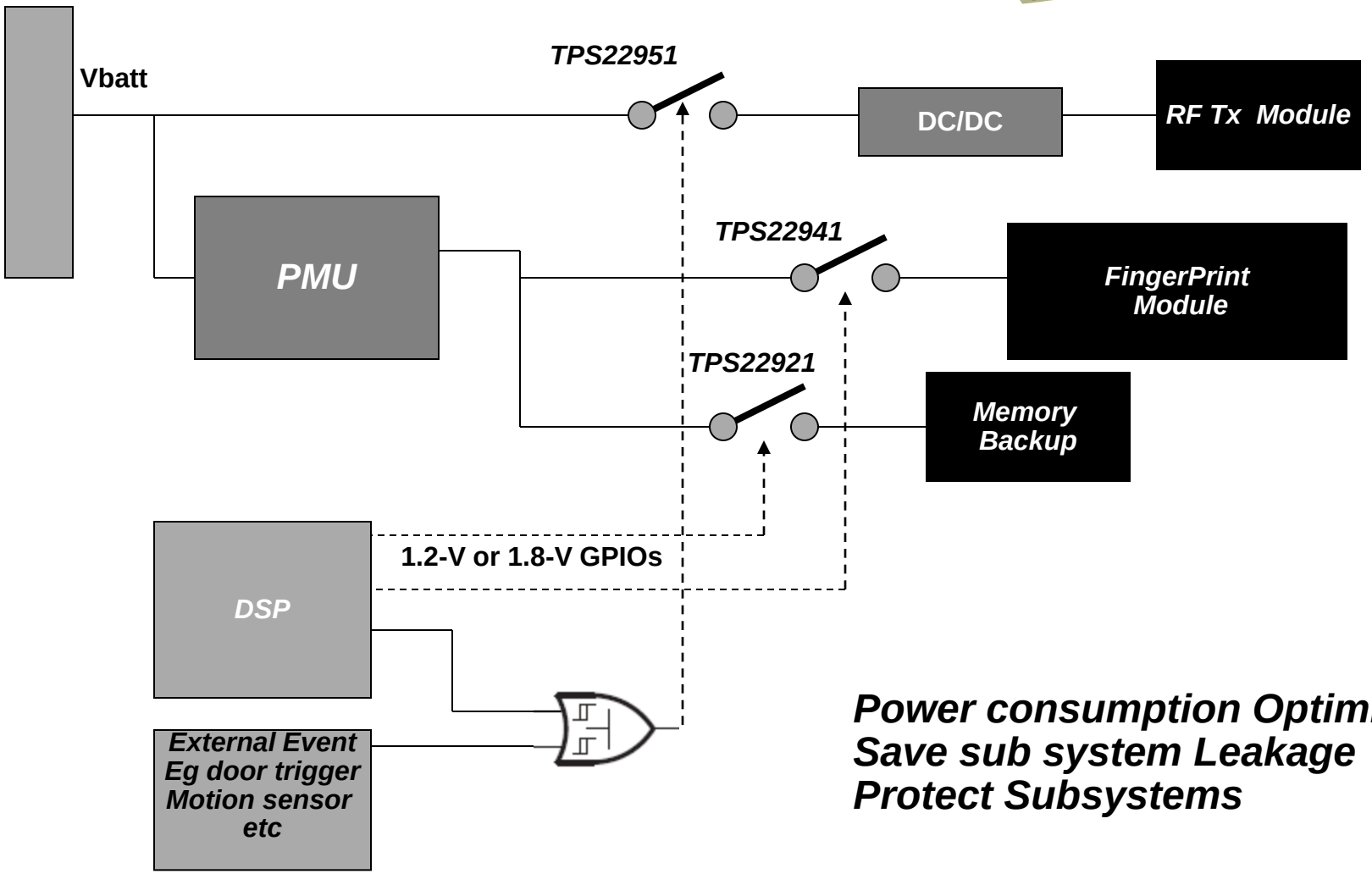
(Switch-off the DSP & Memory sub-system using EN of the SMPS)

Load Switch Solution

➔Save board space
➔Cost optimized Solution
➔Save Camera sub-system leakage

Application Example

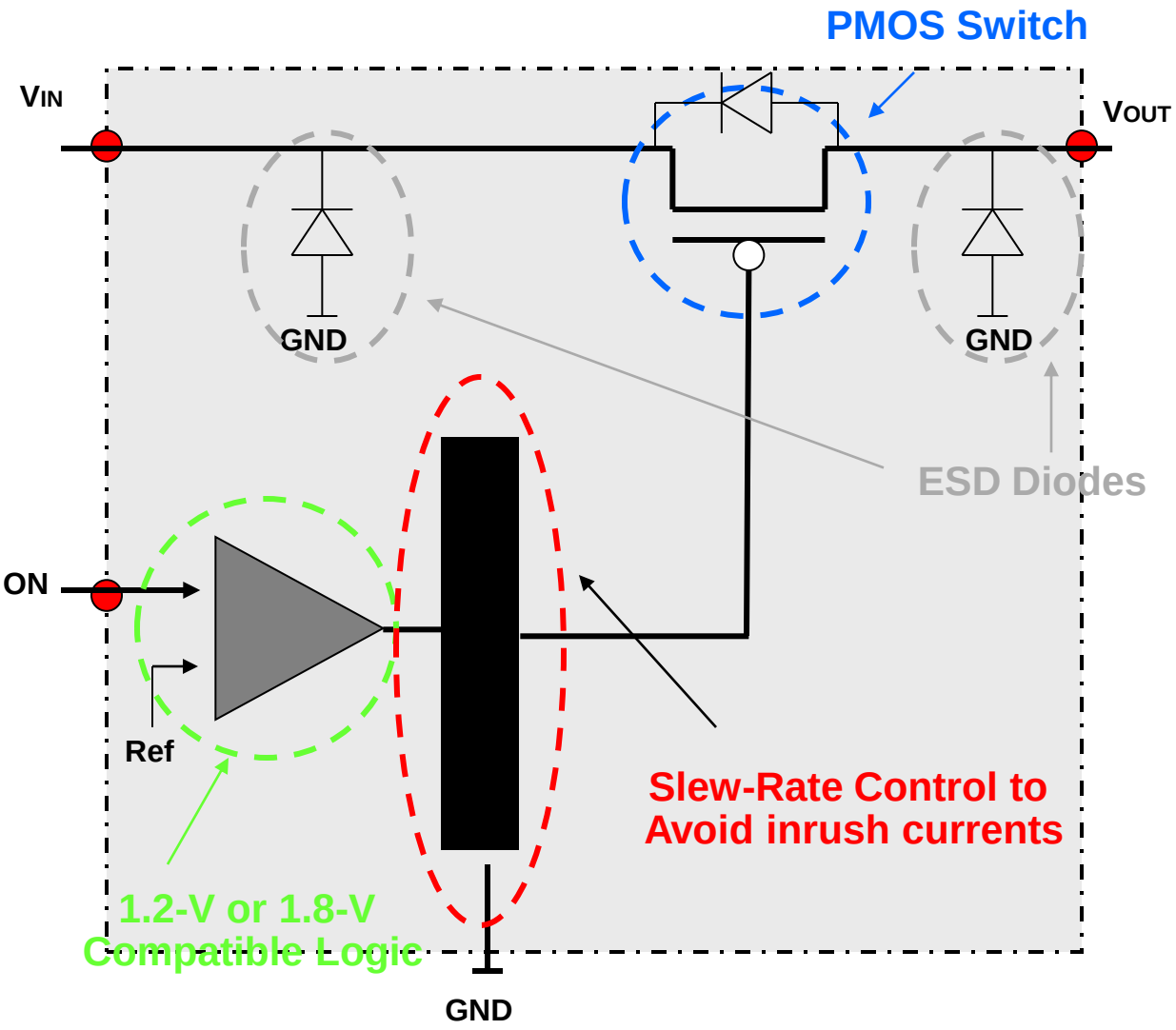
Advanced Alarm System



Power consumption Optimization
Save sub system Leakage
Protect Subsystems

Conventional Solution

Example : Non Current-Limited Load Switch



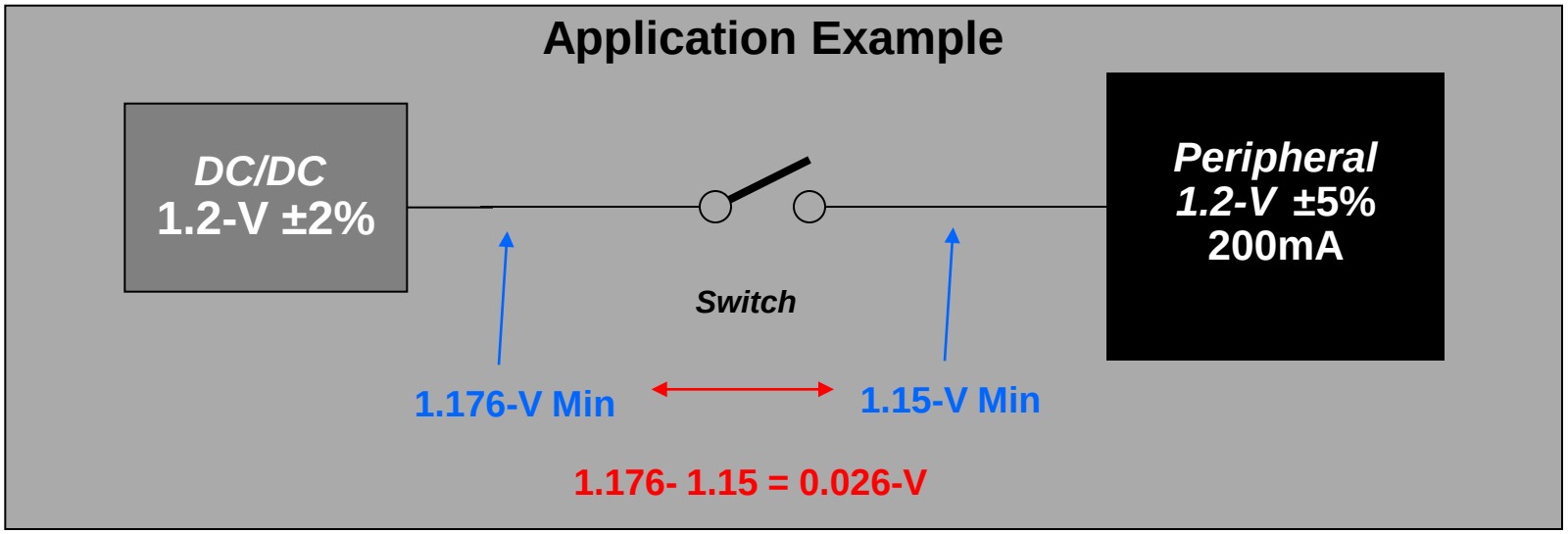
Discrete Solution =

- Several components
  - Complex
  - PCB Area
- Design and Layout
  - Need expertise
  - Need time

Integrated Solution =

- 1 unique device
  - Small PCB Area
- Design and Layout
  - Easy to design
  - Fast to design

Key Parameter : ON resistance (1/2)

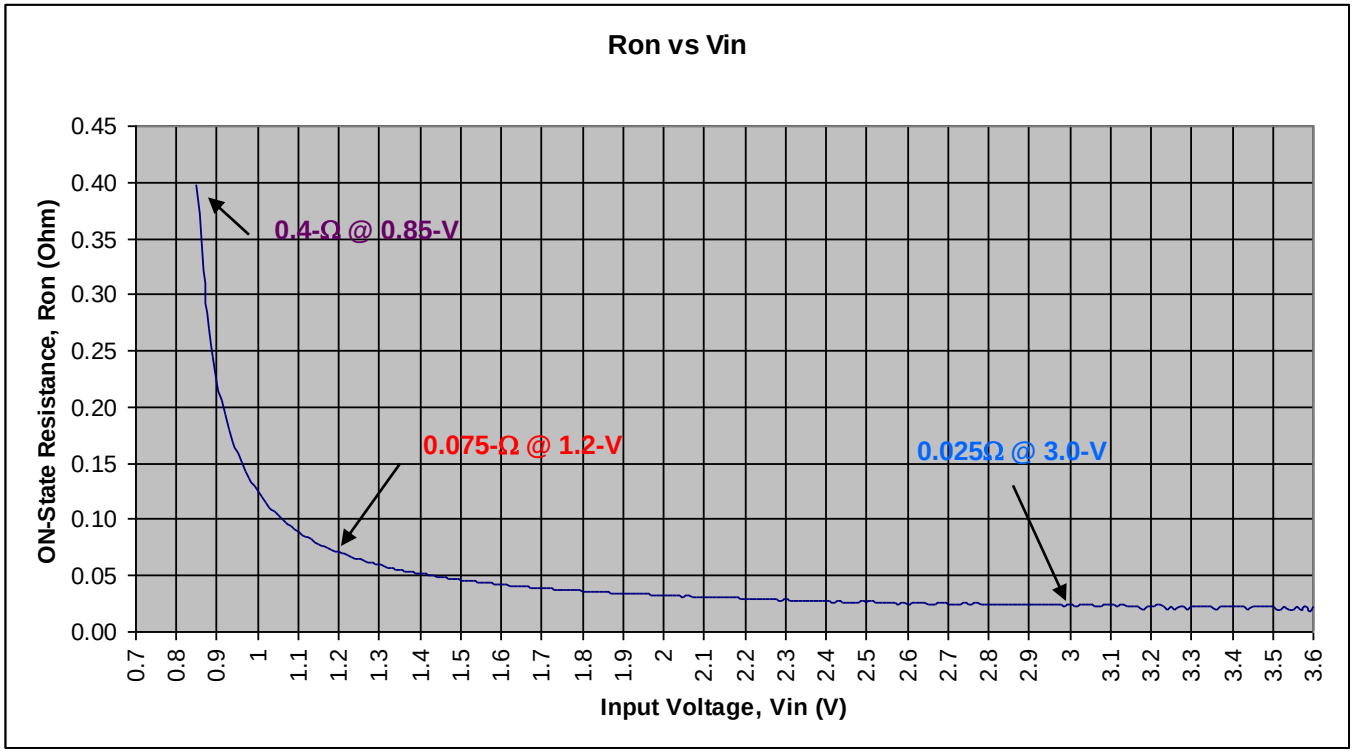


- User has a 0.026-V dropout maximum
  - R_{LOADSW} = V / I = 0.026 / 0.2 = 0.13

➔ ***Conclusion: the switch solution must be***

➔ ***130-mΩ at 1.2-V Over Temperature***

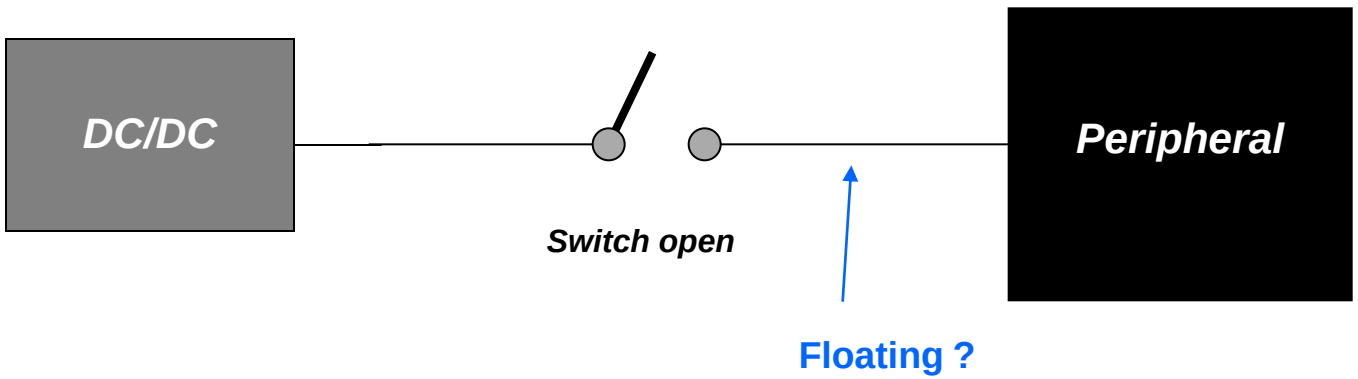
Key Parameter : ON resistance (2/2)



Example for a 200mA Load

- **For a 3.3-V Rail … V_{DROP} = 0.025 * 0.2 = 0.005-V ➔ 0.02% of the rail (acceptable)**
- **For a 1.2-V Rail … V_{DROP} = 0.075 * 0.2 = 0.015-V ➔ 1.25% of the rail (acceptable)**
- **For a 0.85-V Rail … V_{DROP} = 0.4 * 0.2 = 0.08-V ➔ 9.4% of the rail (non acceptable)**

Key Parameter : Output Discharge

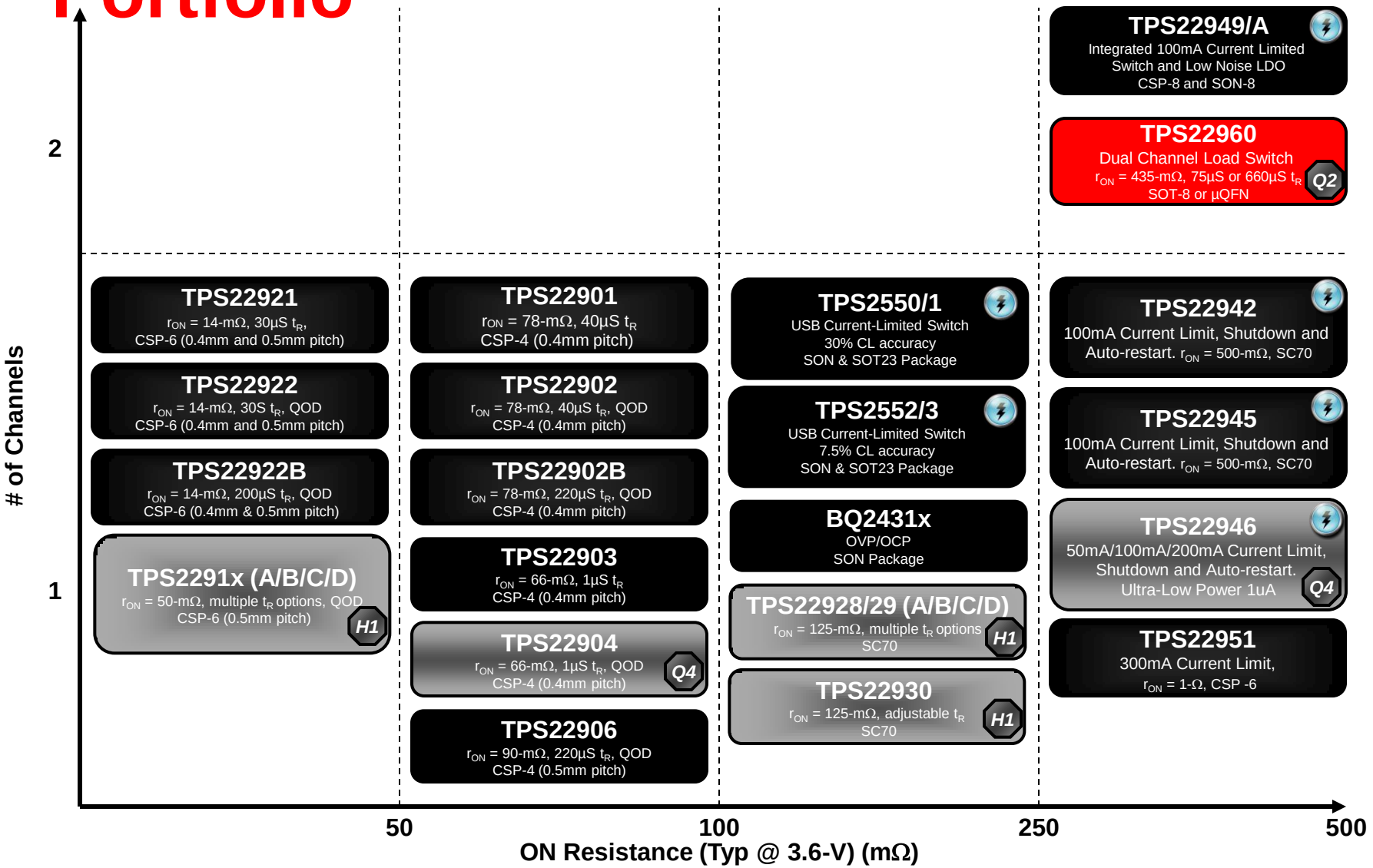


- When the switch is turned off
  - Some users prefer to not have the power rail floating : need to tie Vout to Ground with a transistor
  - Some users prefer to not have the rail tied to ground to avoid any leakages coming from the peripheral supply line

- TI Load Switch have integrated output discharge (TPS229x2) or not (TPS229x1)

Integrated Power Switch Product Portfolio

(Products Highlighted in RED are New Arrivals, and Gray are Future)



= Current Limited Load Switch

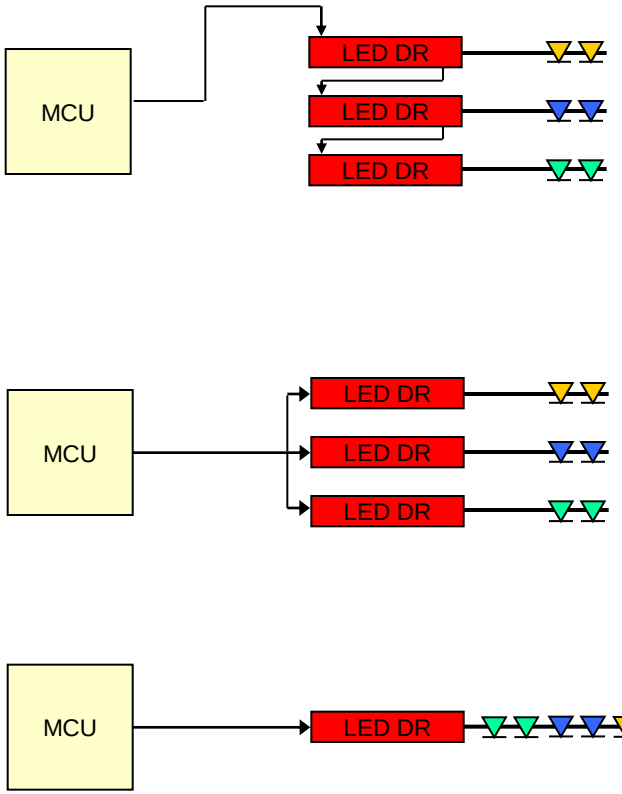
QTD = Quick Output Discharge

Q4 = Expected Quarter Of Release

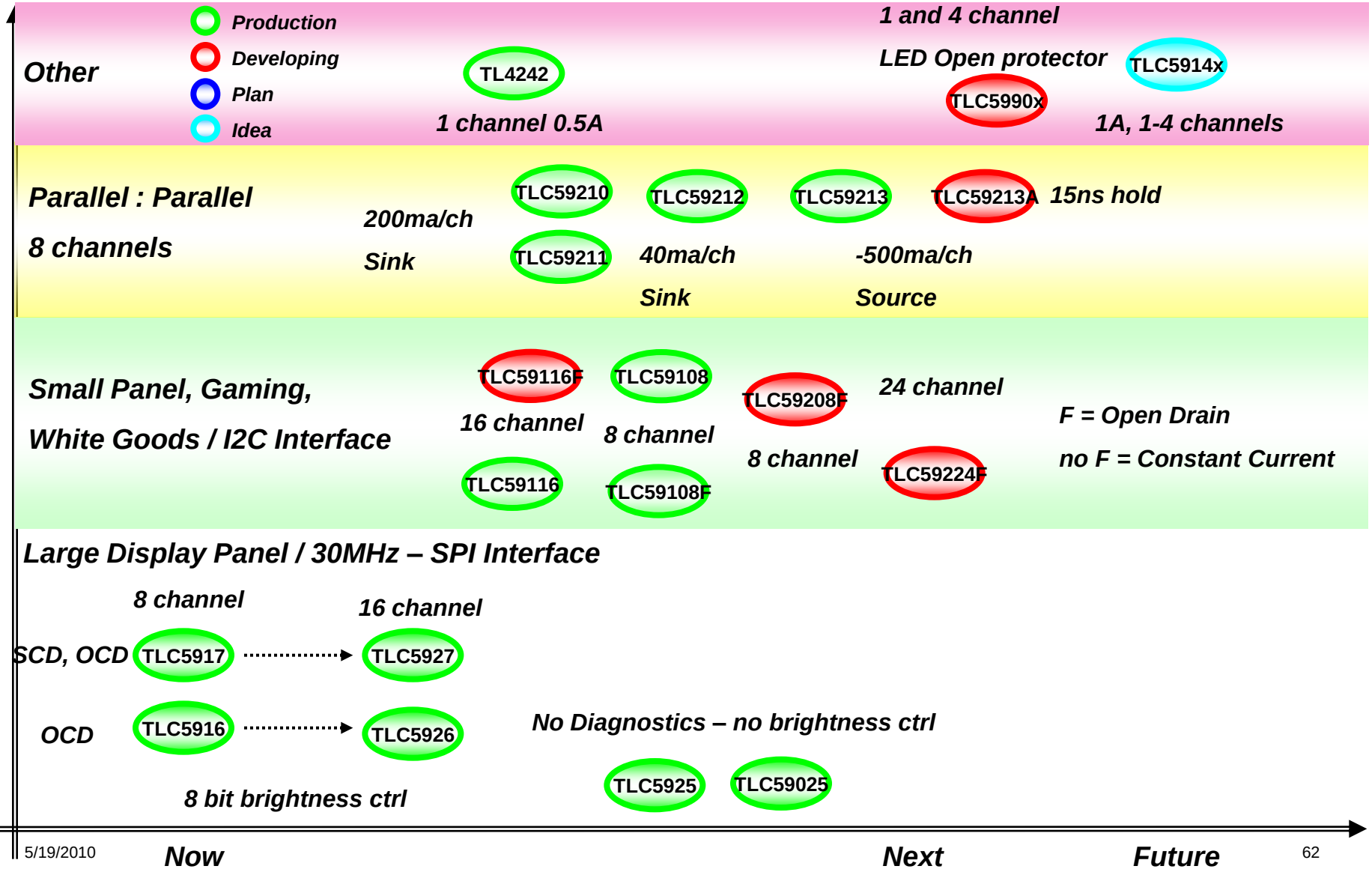
Texas Instruments

DLS LED Driver Types

- Serial In – Parallel Out (SIPO)
  - Cascade-able – high speed communication (30MHz)
    - Large and Medium full-motion video panels
    - Billboards (motion and stable)
    - Scrolling Signs
    - Informational Panels
    - Constant Current, Sink Drivers
  - Non-Cascade-able (w/Address) – medium speed communication (1MHz)
    - Small display panels
    - Indicator lights
    - Scrolling signs
    - Informational Panels
    - Constant current and Open-drain, Sink Drivers
- Parallel In – Parallel Out (PIPO)
  - Clocked
    - Small system indicator
    - 7-segment display control
    - Open-Collector, Sink or Source
  - Non-Clocked
    - Small system indicator
    - Open-Collector, Sink or Source
- Other
  - Single Channel – Lighting
  - Open Detection - Lighting



DLS LED Driver Portfolio



TLC5916/17/25/025/26/27

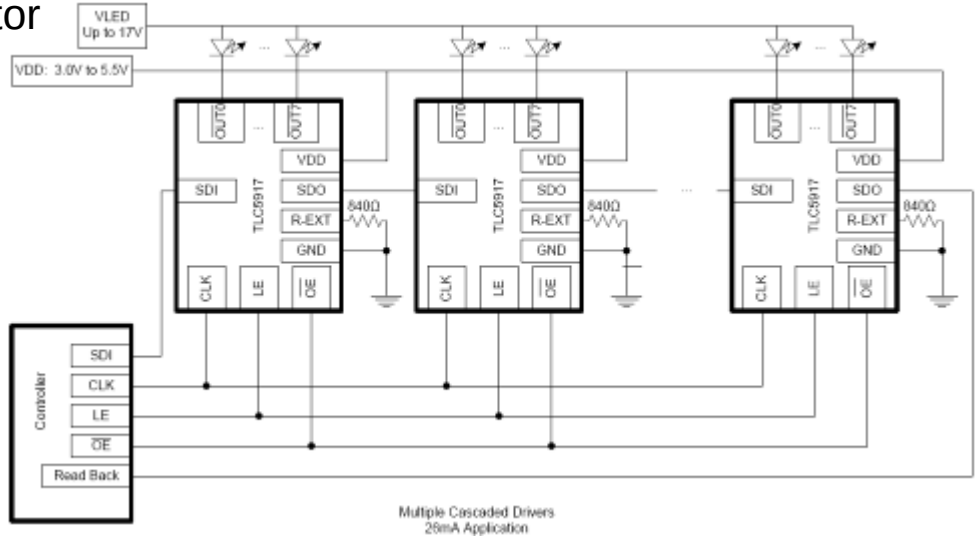
8 & 16 Channel SIPO Constant Current Sink Drivers

- 8 or 16 Channels
- 8-bit Global Brightness (0~100%)
- 45mA / 120mA Constant Current
- LED Open, Short and Over-Temperature Detection
- 3.0V-5.5V Input Voltage Range
- Chip to Chip Accuracy: 3% typical
- Serial Communication Interface (4-wire, 30MHz)
- Current Programmable by External Resistor

- Programmable constant load current
- Fault Reporting
- Cascade-able for large panels

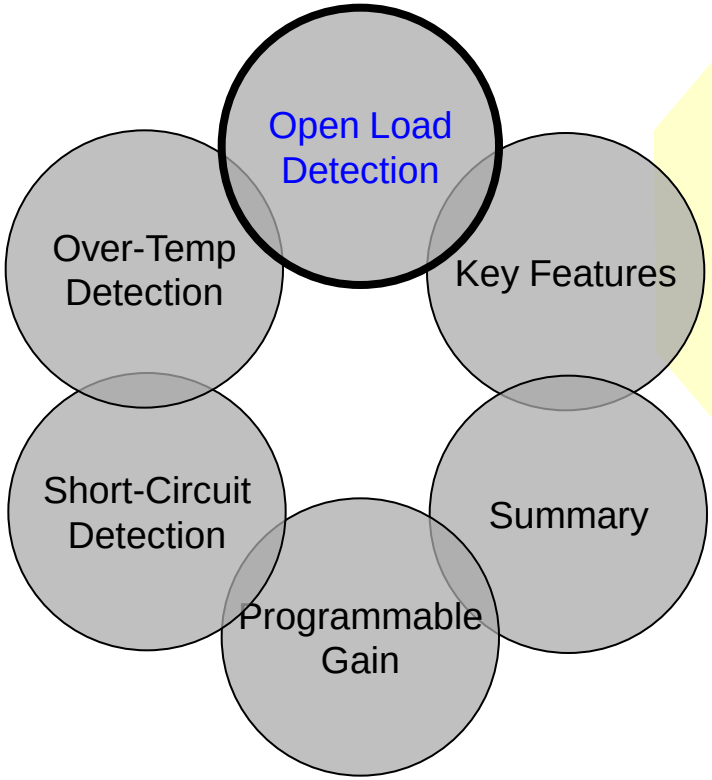
- LED illumination and intensity control
- Video walls and signs
- Traffic Signalization
- Scrolling Signs

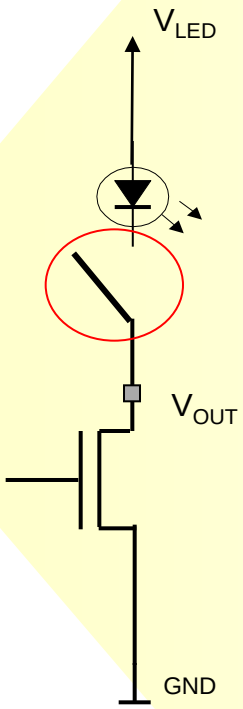
(Contact Factory)



Multiple Cascaded Drivers
26mA Application

Open-Load Detection





If open-circuit then : $I_{OUT} \rightarrow I_{THRESHOLD}$ (1)

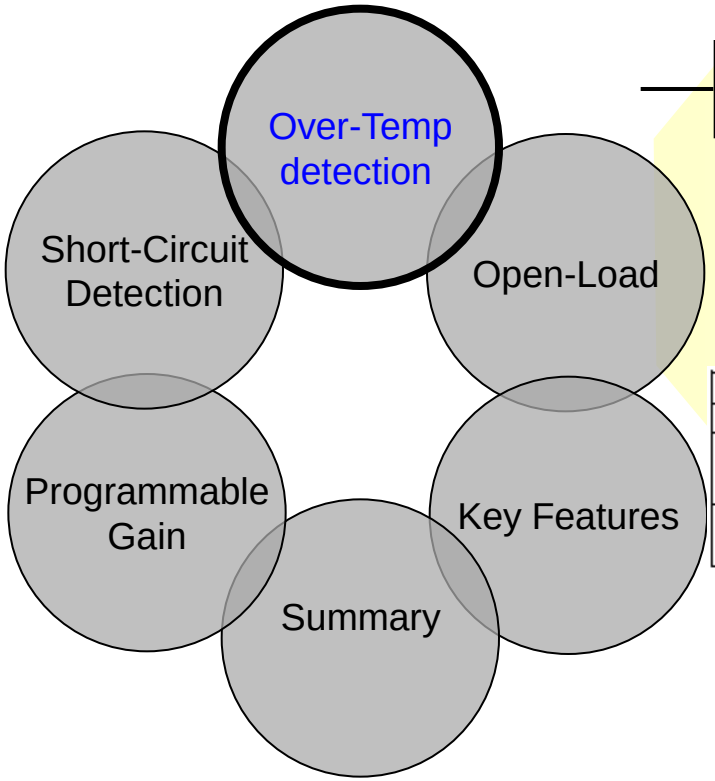
If $I_{OUT} < I_{TRESHOLD} \rightarrow$ Open-Circuit

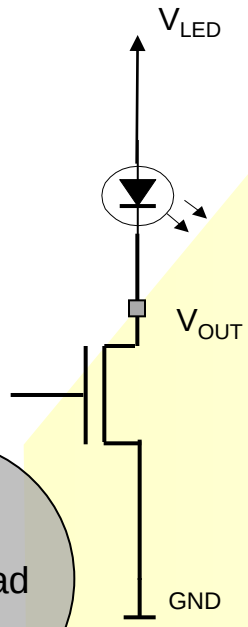
	Open on LED detected	No error Detected
I_{OUT}	$I_{OUT} < I_{TRESHOLD}$	$I_{OUT} >= I_{TRESHOLD}$
Error bit	**0**	**1**

V_{DD} = 3.3V to 5V

(1) $I_{THRESHOLD} = 0.5 * I_{OUT,target}$ (typical)

Over-Temperature Detection



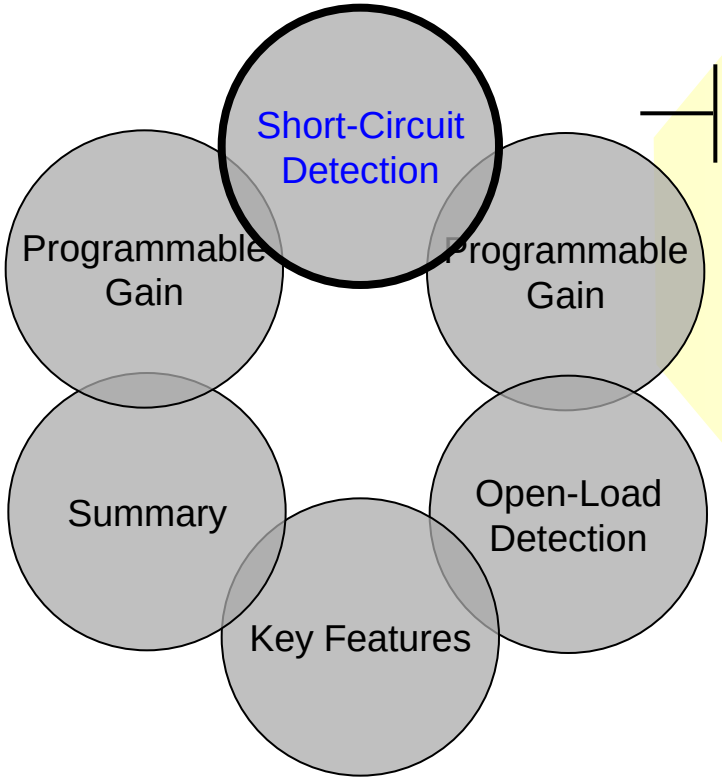


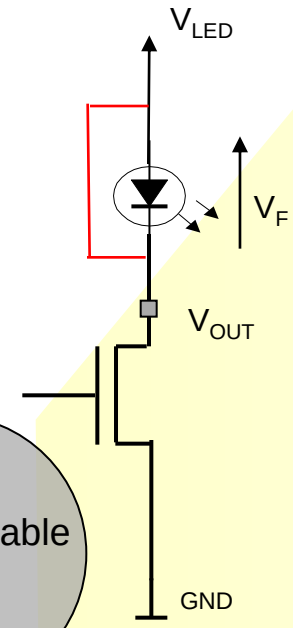
Each device is equipped with :

- A global over temperature sensor
- 8/16 individual, channel-specific over temperature sensors.

STATE OF OUTPUT PORT	CONDITION	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	
On On → all channels Off	$T_J < T_{J,trip}$ global	1	Normal
	$T_J > T_{J,trip}$ global	All error status bits = 0	Global overtemperature
On On → Off	$T_J < T_{J,trip}$ channel n	1	Normal
	$T_J > T_{J,trip}$ channel n	Channel n error status bit = 0	Channel n overtemperature

Short-Circuit Detection





If short-circuit then :

- $V_F \rightarrow 0$
- $V_{OUT} \rightarrow V_{LED}$

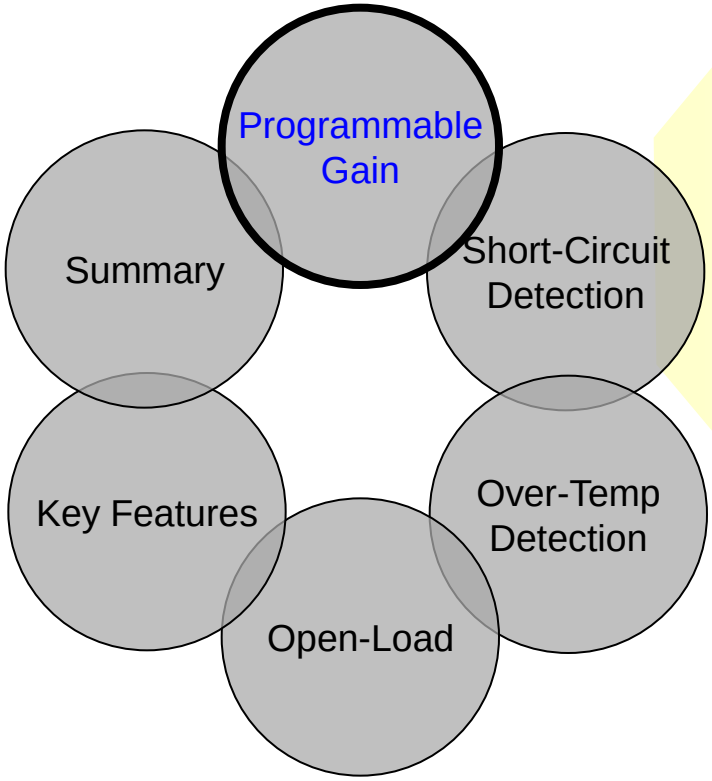
If $V_{OUT} > V_{TRESHOLD} \rightarrow$ Short-Circuit

	Short on LED or Short to V_{LED} detected	No error Detected
V_{OUT}	$V_{OUT} >= V_{TRESHOLD}$	$V_{OUT} < V_{TRESHOLD}$
Error bit	**0**	**1**

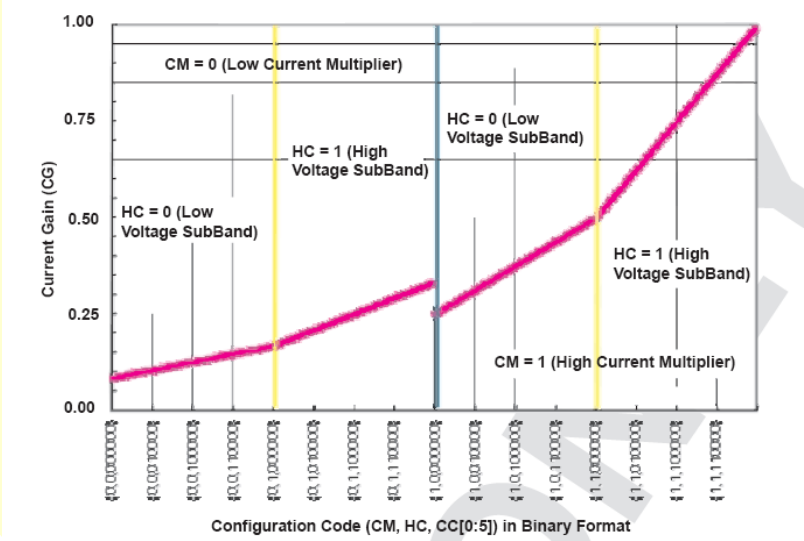
V_{DD} = 3.3V to 5V

Part-Numbers	Short-Circuit Detection
TLC5916, TLC5926	None
TLC5917, TLC5927	Fixed $V_{THRESHOLD}$ = 2.5V

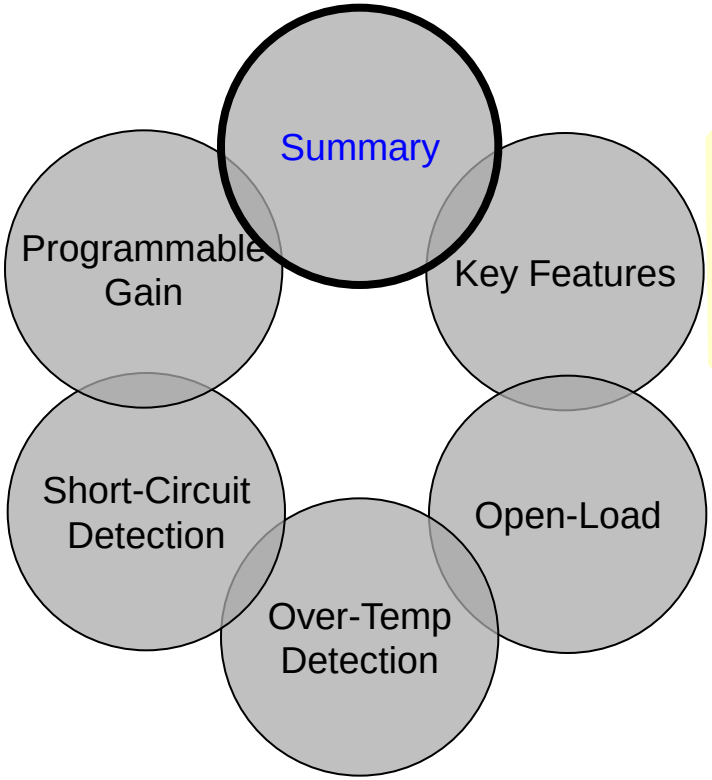
Programmable Gain (Dimming)



- Programmable Gain
  - 8 bit current setting (256 steps)
  - I ref set with the external resistance
  - from the 100% value down to almost 0



Summary



	TLC5916 TLC5917	TLC5926 TLC5927	TLC5925	TLC59025
Channels	8	16	16	16
Current	5mA - 120mA	5mA - 120mA	3mA - 45mA	5mA - 45mA
Input Voltage	3V - 5.5V	3V - 5.5V	3V - 5.5V	3V - 5.5V
Output Voltage	17V	17V	17V	17V
accuracy channel / chip	3% / 6%	6% / 6%	6% / 6%	6% / 6%
Data transfer	30MHz	30MHz	30MHz	30MHz
Switch time on/ off (ns)	370 / 105ns	485 / 245ns	485 / 245ns	485 / 245ns
Open Load (Current detection)	Yes	Yes	No	No
short circuit / over voltage detection	TLC5917 Only Fixed 2.5V Threshold	TLC5927 Only Fixed 2.5V Threshold	No	No
Over-temperature protection	Yes	Yes	Yes	Yes
Current gain	256 steps	256 steps	N/A	N/A
Packages	16 (D, N, PW)	16 (D, N, PW)	24 (DBQ, PW, DW)	24 (DBQ, PW, DW)

TLC59108/108F/116/116F/208F/224F

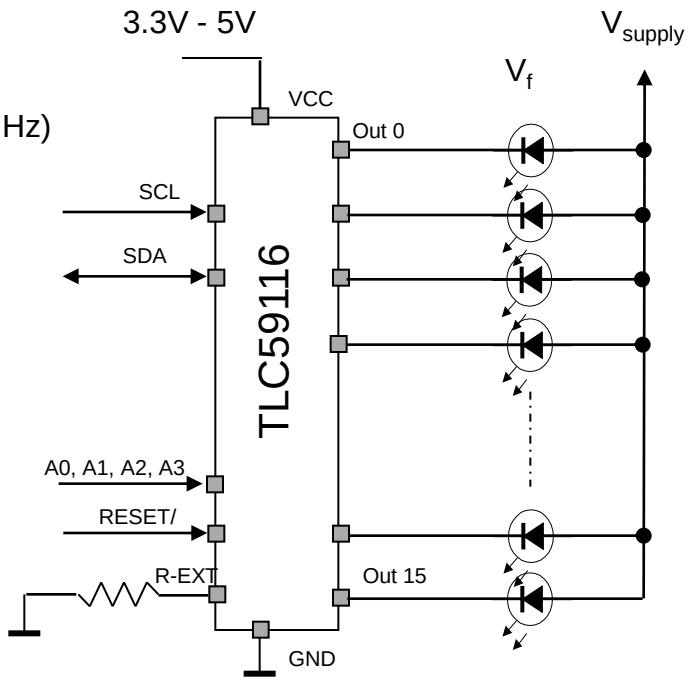
8 & 16 Channel I2C Sink Drivers with PWM / Channel

- 8 or 16 Channels
- 8-bit Global Brightness (8~99%)
- 8-bit PWM per pin
- 100mA Constant Current (Open-Drain on “F” versions)
- 1MHz Fast-Mode Plus Transfer Rate
- 256 step Group Blinking (42ms – 10.73s)
- 3.0V-5.5V Input Voltage Range
- LED Open Detection
- Channel Over-Temperature Detection
- Chip to Chip Accuracy: 4% typical
- I²C Serial Communication Interface (2-wire, 100KHz, 400KHz and 1MHz)
- Current Programmable by External Resistor
- 4 Software Programmable I²C Addresses

- Programmable constant load current
- Fault Reporting
- Independent PWM per Channel

- LED illumination and intensity control
- Video walls and signs
- Traffic Signalization
- Scrolling Signs

TLC59116EVM



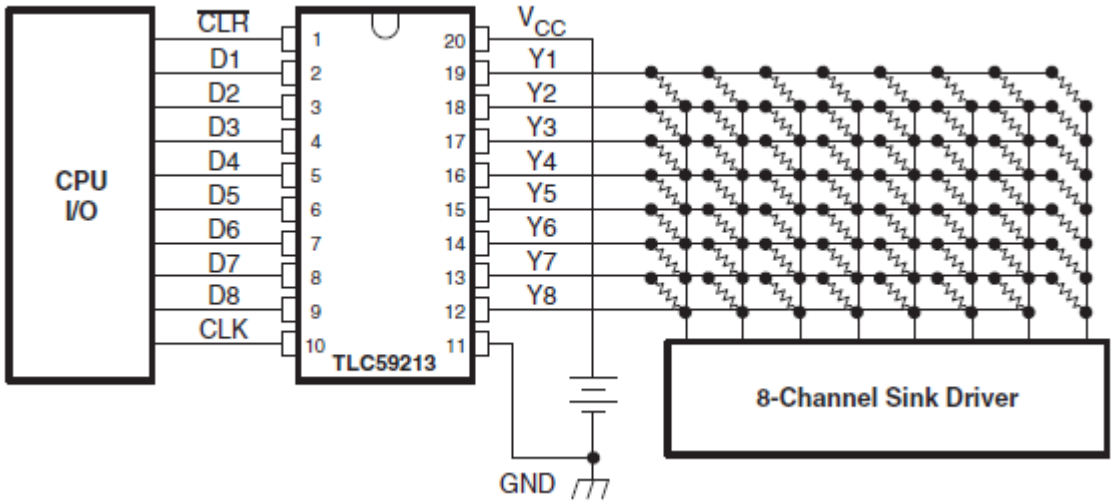
TLC59210/211/212/213/213A

8 Channel PIPO Sink Drivers or Source Driver

- 8 Channels
- 40mA or 200mA Sink Current per Channel
- -500mA Source Current per Channel
- 3.0V-5.5V Input Voltage Range
- V_{DS} = 24V or 30V
- Clear function turns all channels off
- Clock pin for data latch
- Clock speeds up to 1MHz
- Schmitt-trigger buffers
- 20-pin PW, 20-pin N

- Direct Control of Outputs
- Outputs Stable During Data Transition
- Outputs Change on Clock

- LED illumination
- Lamps and Displays
- Traffic Signalization
- Gaming, Relays

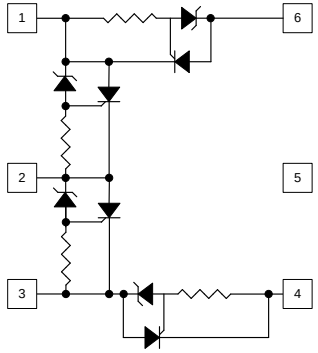


TLC59901 / TLC59904 Q3-2010

1 and 4 Channel LED Open Protectors

- Monitors LED for open condition
- Protects individual LED or LED strings
- Turns ON when LED Open Detected
- 1-channel and 4-channel versions
- 350mA per channel
- Detection Voltage ~7V (typical)
- On Voltage ~ 1V (typical)
- 35V Input Voltage Range

- LED String protection
- Fault reporting
- Cascade-able for strings

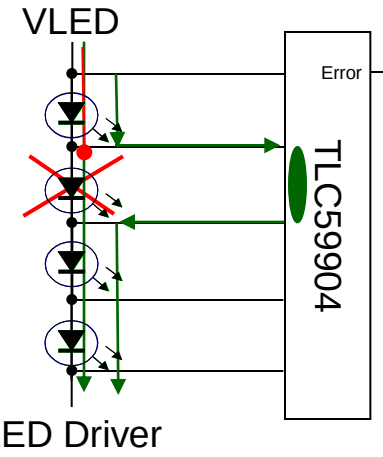


- LED strings
- General Lighting
- Traffic Signalization

TLC59904 senses open LED

Current flows around open LED

All good LEDs turn on



All LEDs good, current flowing

LED2 = Open

No current flow

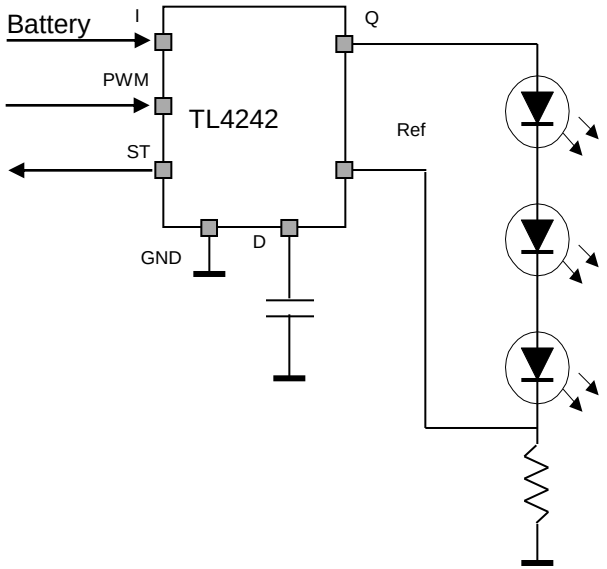
All LEDs OFF

TL4242

1 Channel 42V, 500mA Linear LED Driver

- Adjustable current up to 500mA (+/-5%)
- Wide input voltage range – up to 42V
- LED Open Detection
- Die Over-temperature shutdown and restart
- Short circuit proof
- Reverse voltage protection
- Wide operating temperature (-40ºC to +150ºC)
- SON – 8-pin with power pad

- Supply voltage independent current and brightness
- Fault reporting
- Programmable constant current load

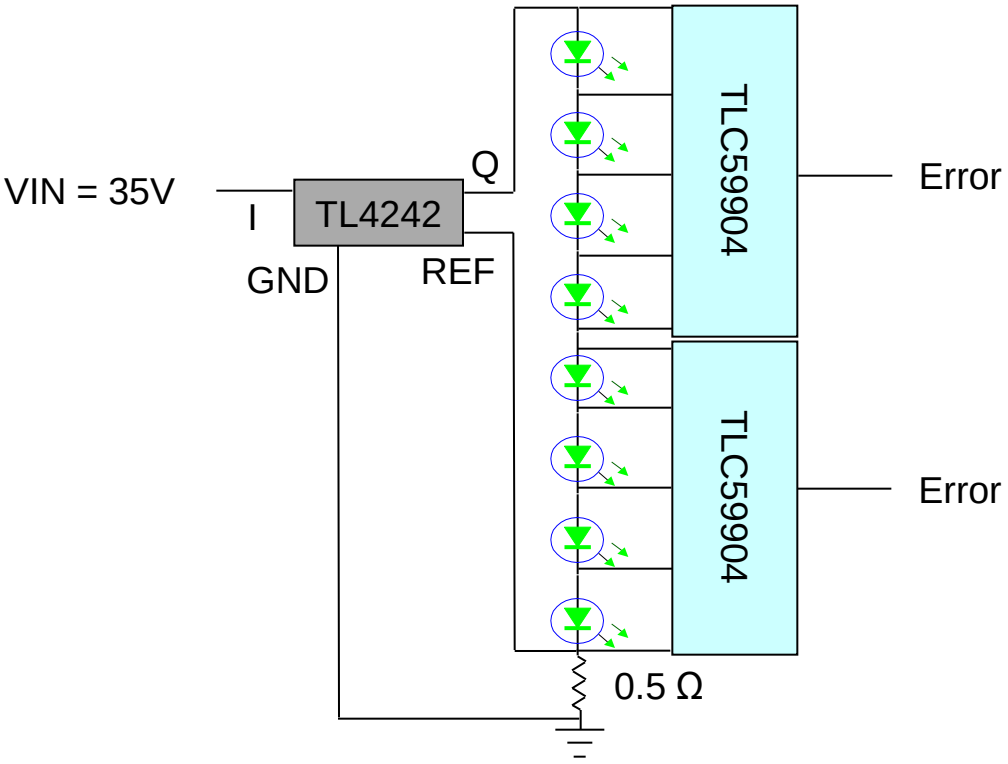


- LED illumination and intensity control
- General Lighting
- Exterior: DRL, Fog light, turn lamp, headlamp
- Interior: vanity, map, courtesy

TL4242EVM-543

1ku Pricing $0.65

LED Open Protector Application Example



1 – TL4242

8 – LEDs with VF = 4 V

VIN = 35V

IOUT = 350mA (R_{REF} = 0.5Ω)

2 – TLC59904 Open Protectors

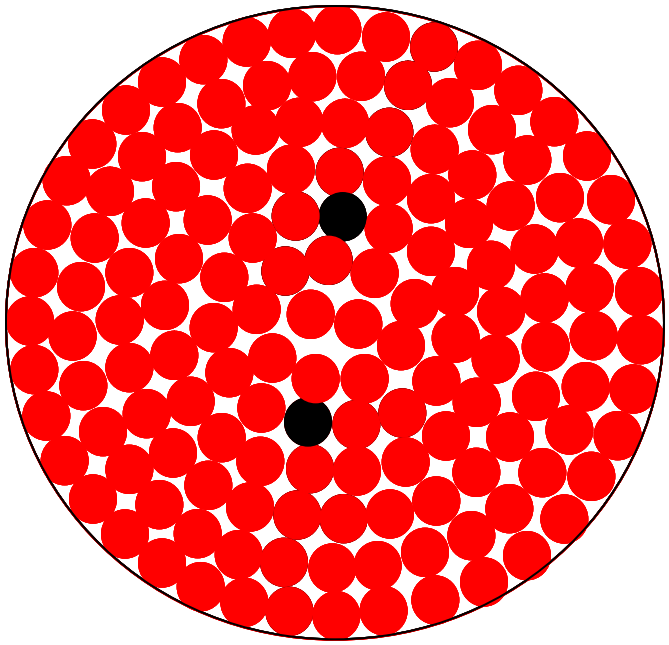
TL4242 supplies constant current

TLC59904 devices protect LED String

Result: 8 sting LED that will function with multiple LEDs open

LED Open Application Example

Typical 8-LED string Traffic Light



One bad LED

turns off full 8-LED string

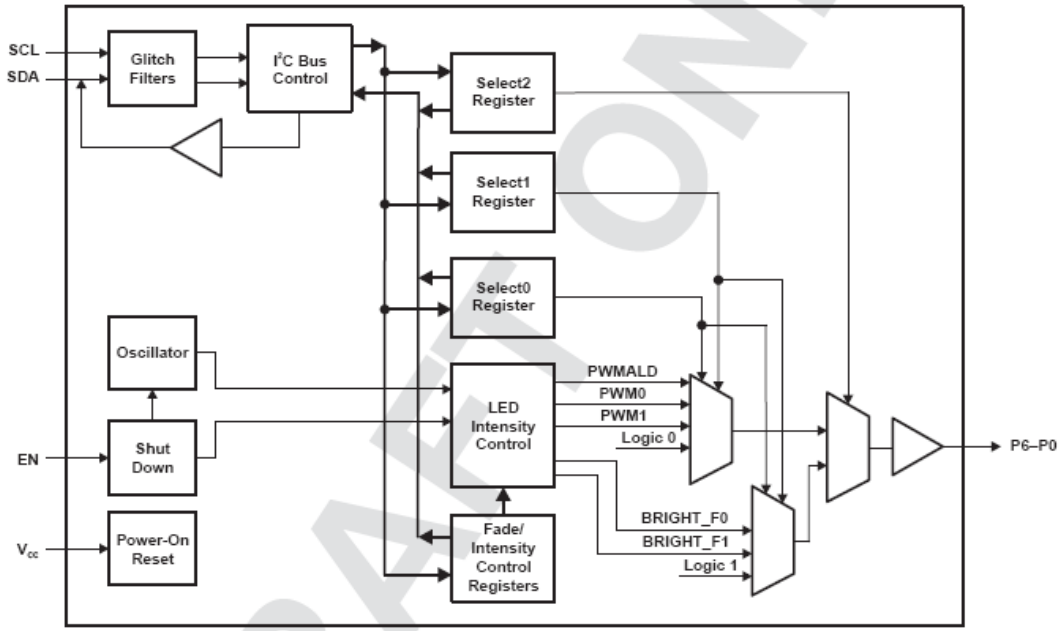
Two bad LEDs

turns off 2 full 8-LED strings

Two bad LEDs

With Open LED Protection

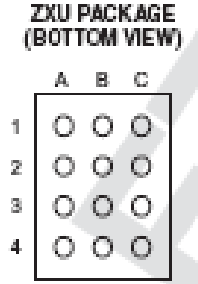
TCA6507 – I²C LED Drivers (7-bit)



Features

- **Frees processor from LED blink operations**
- **7 LED Drivers: On, Off, Flashing at programmable rate**
  - Dual PWMs for 2 different blink-rate selections on any LED
- **16 Intensity control steps from Fully OFF to Fully ON**
  - Each LED driver supports constant intensity over temperature
- **Can support brightness control and blink modes at the same time**
- **1.8V I²C compatible (1.65V to 3.6V on I2C side, 5.5V tolerant on output side)**
- **Internal oscillator – requires no external components**
- **Outputs not used as LED Drivers can be used as regular general purpose outputs**

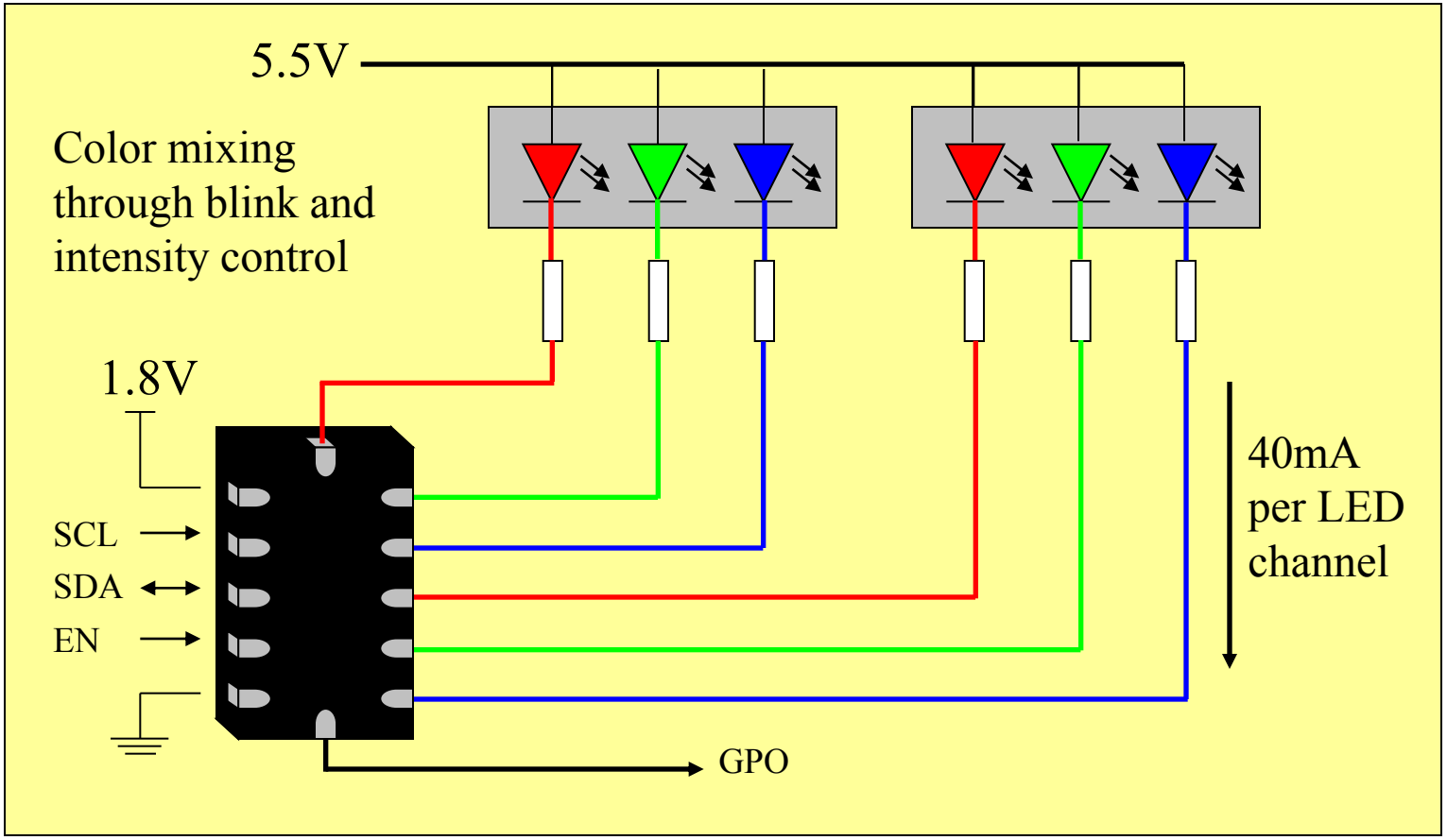
tca6507_demo2.wmv (2 MB)



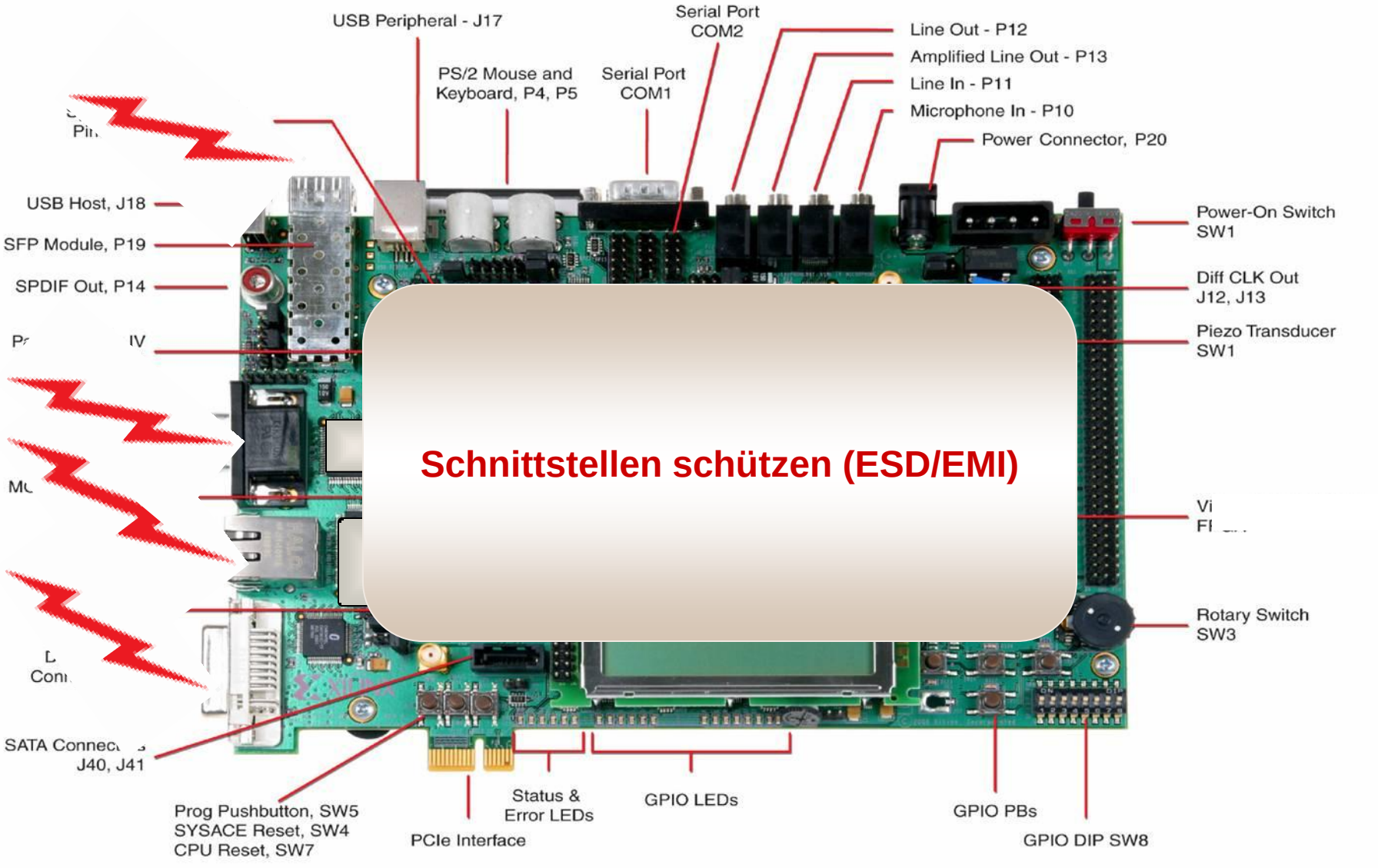
12-ball BGA

2mm x 2.5mm x 0.6mm (max)

TCA6507 Drives 2 RGB LEDs

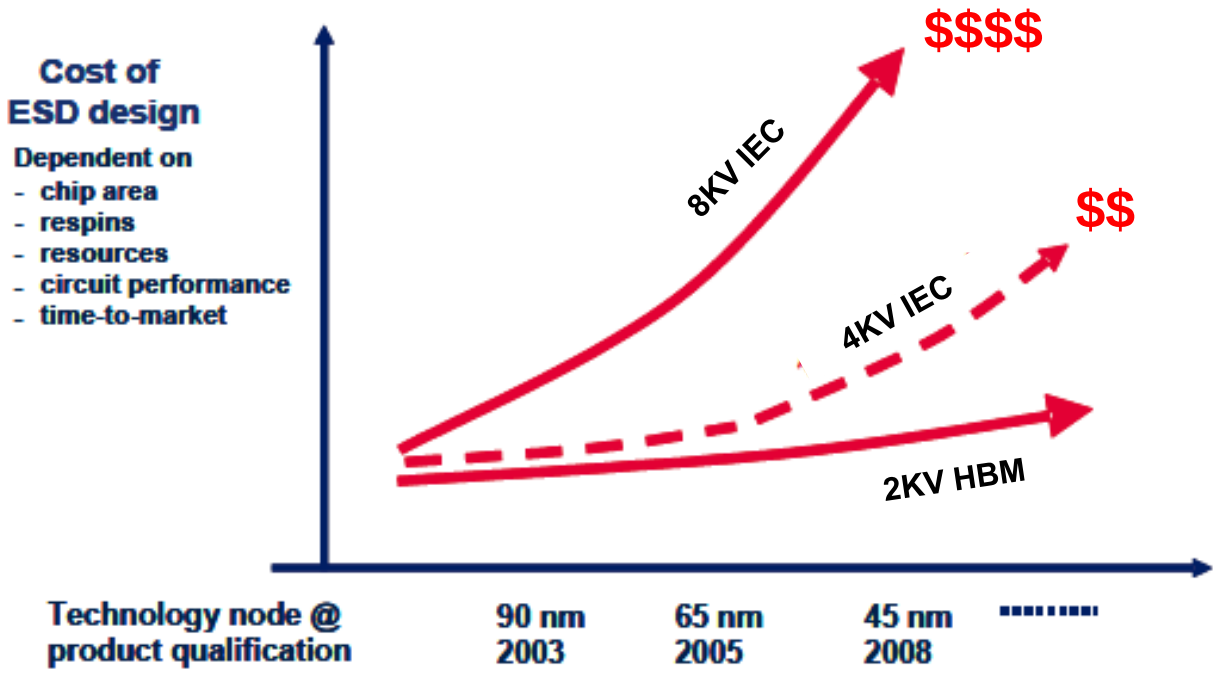


Protect your system



Why External ESD Protection?

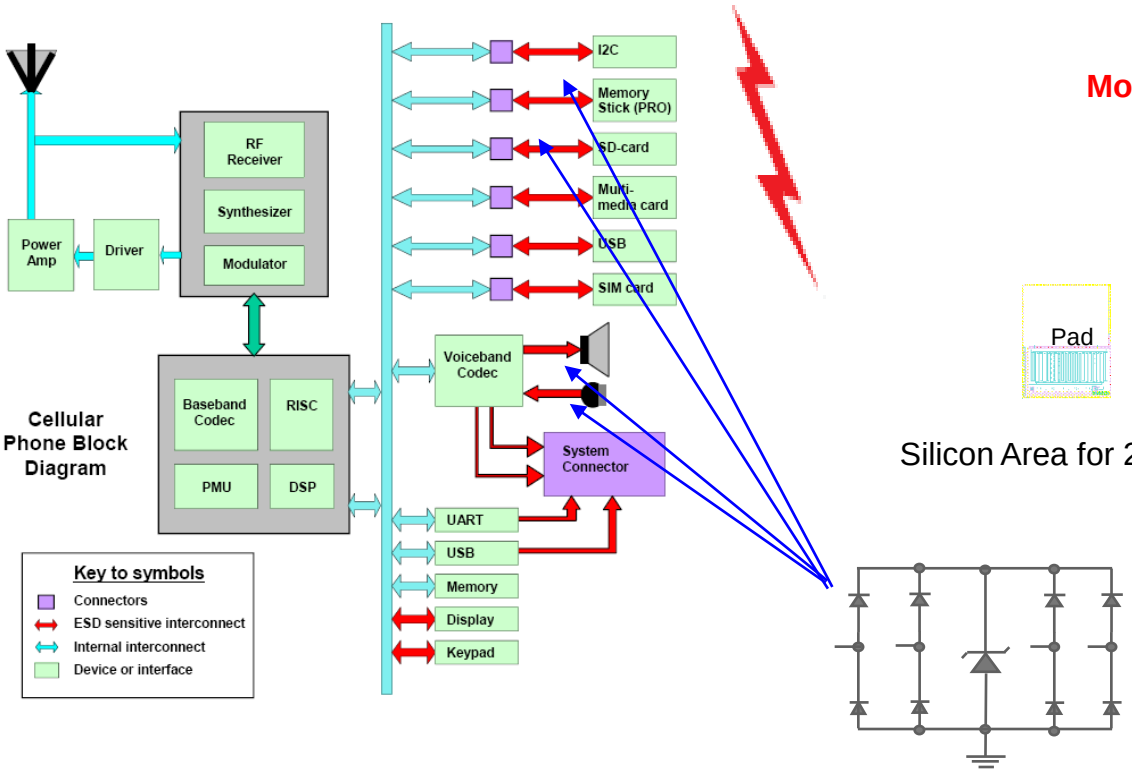
It becomes very expensive to design IEC Clamp at low geometry process



With advanced process we need more die area to design the same IEC Cell
- You can scale down the core design , but you can't scale down the IEC Cell

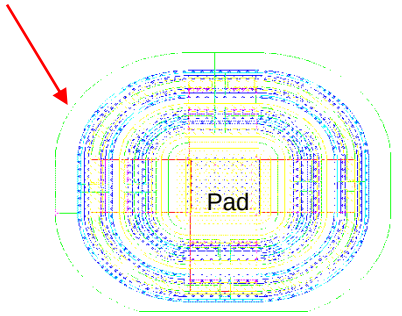
Why External ESD Protection?

- **It is technically and economically challenging to integrate IEC ESD in core ICs based off advanced process nodes**
- **External Connectors, Keypad, Side keys, Audio Jack, etc. are sensitive to system level ESD**
  - **It takes only one ESD stress to damage a system!**



More $$ to design IEC cell in Core Chip

Silicon Area for 2KV HBM

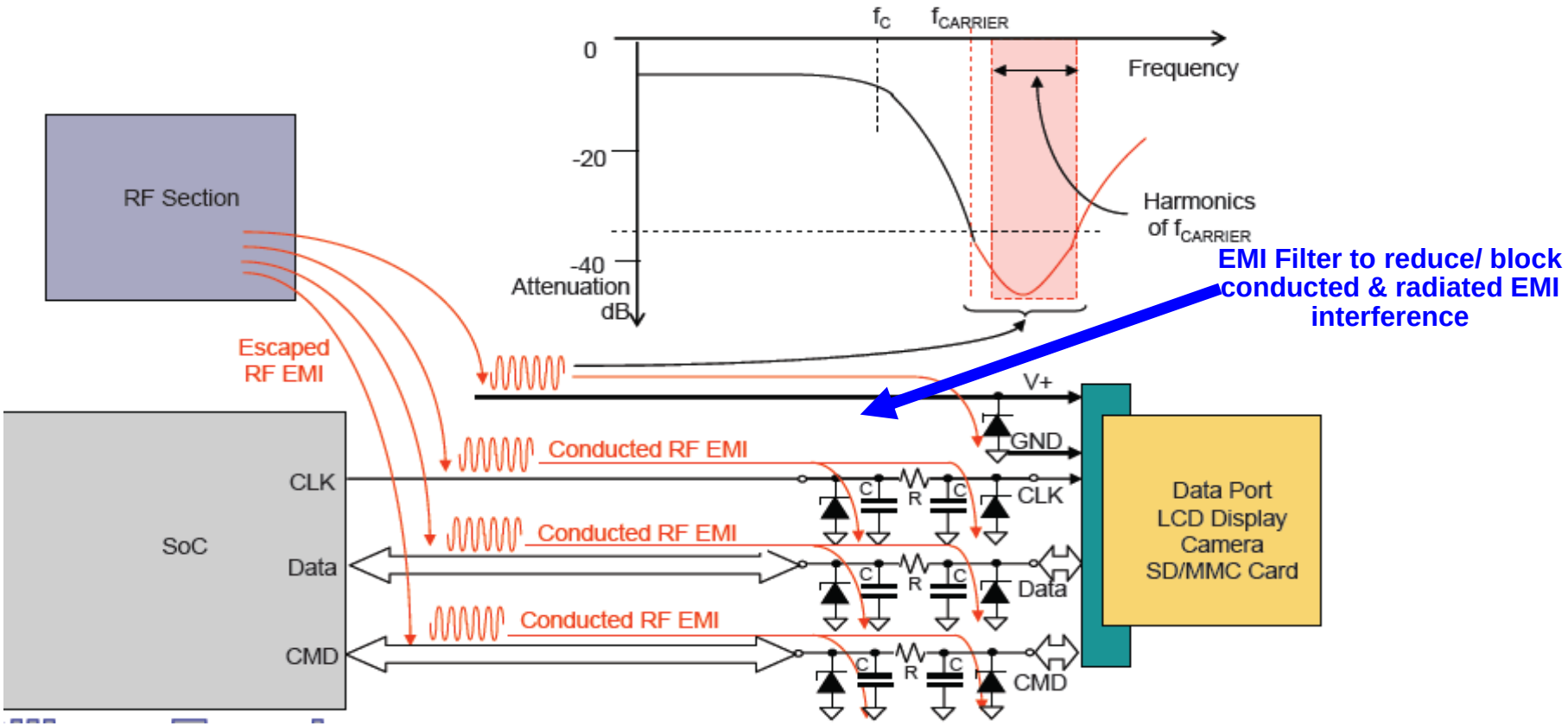


Silicon Area for IEC 8KV Contact ESD

Stand alone ESD protection devices 'cost effectively' saves the system from ESD damage

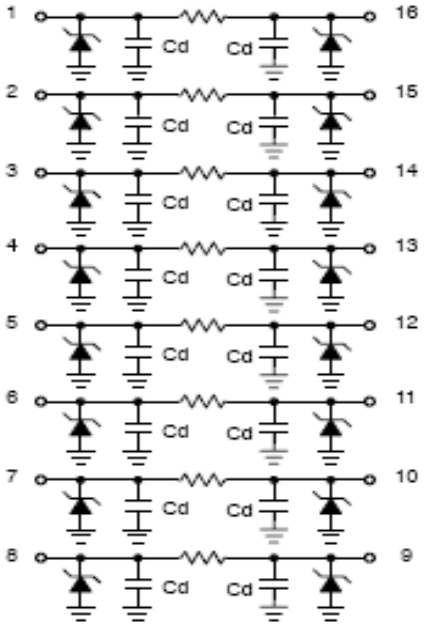
Why EMI Filter?

- RF section of portable equipments generate conducted and radiated EMI interference
- Non-optimized board layout often generates EMI interference among signal lines
- EMI interference can cause both functional and reliability failure

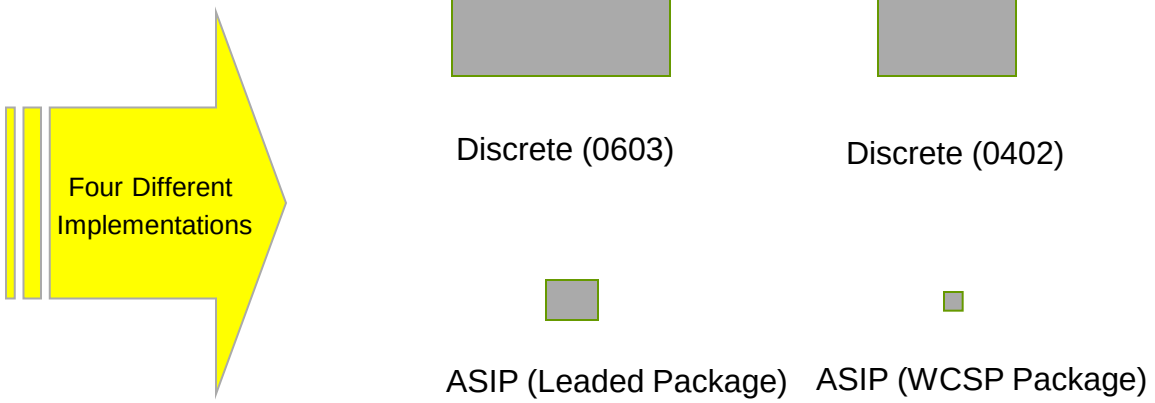


Integrated Protection Devices Vs Discrete Solutions

Board Space Saving



8-Channel EMI Filter



Board Space: Discrete Versus TI IPD Solutions

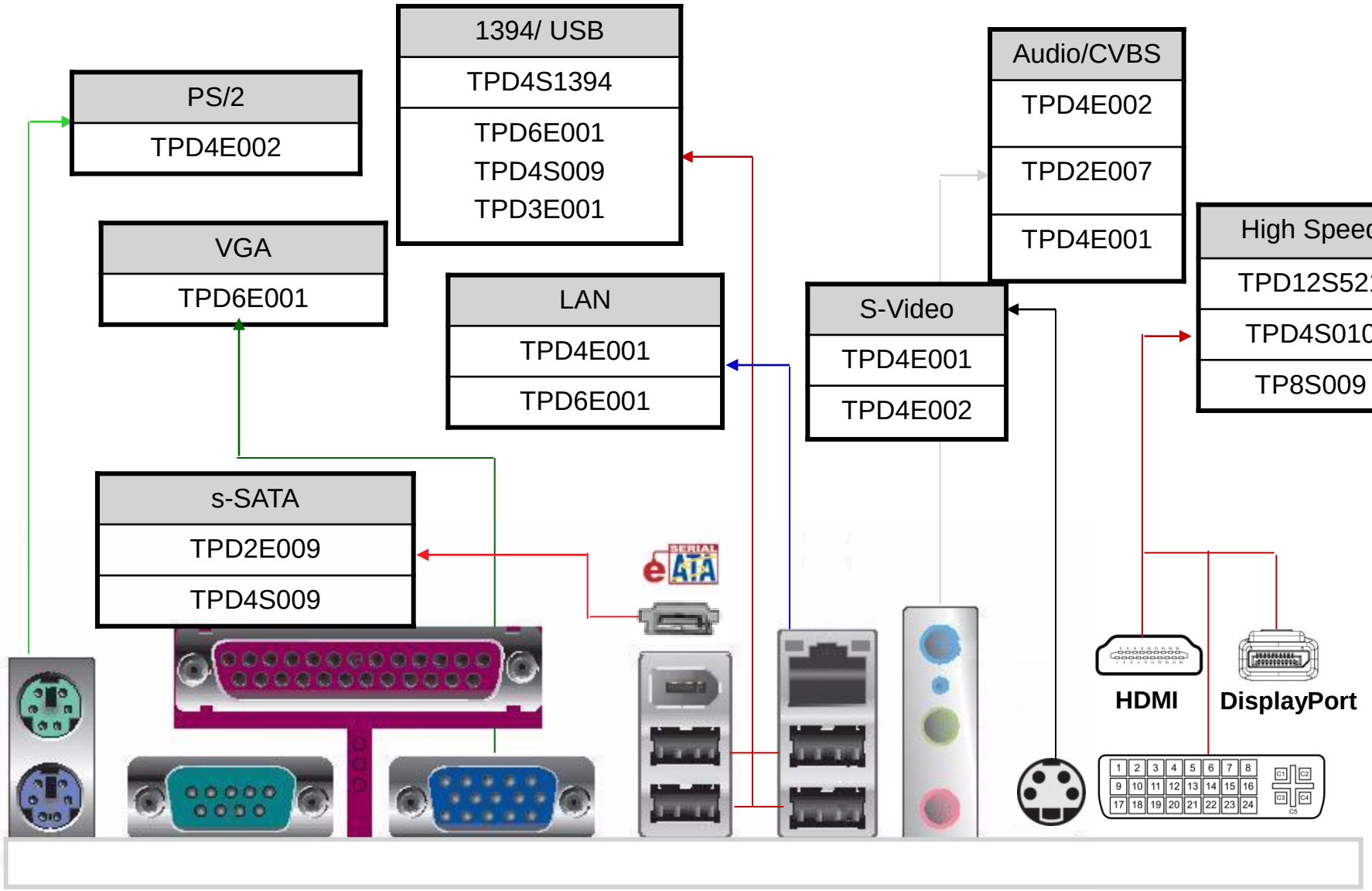
TI's **I**ntegrated **P**rotection **D**evices provide significant board space saving over discrete:

1) Silicon level integration of resistors, capacitors, inductors
2) Eliminate the routing through the board except for filter input, output lines

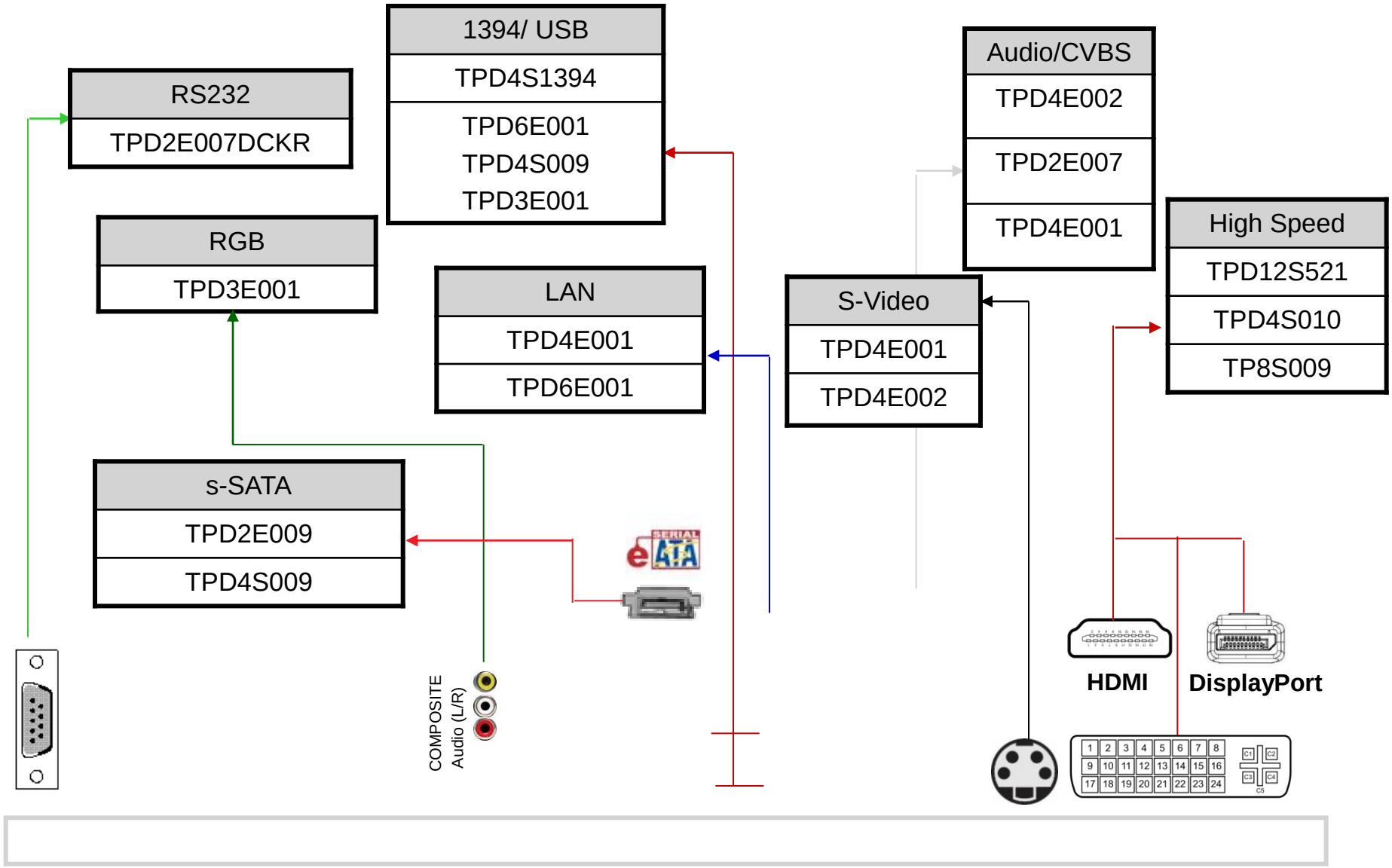
ESD Opportunity By Interface

	Data-Rate	Signal Swing	# of Data Lines	Common Applications	ESD Solutions
USB 2.0	480Mhz	Data swing 0mV to 400mV VBUS = 5V	3 Data lines +1 VBUS	Computing, Portables	TPD3E001 TPD4S012 TPD4S009 TPD2S017
USB3.0	5Gbps	Data swing 0V to 400mV VBUS = 5V	6 Data lines +1 VBUS line/ 7 Data lines +1 VBUS line	Computing, Portables	TPD2E009 TPD4S010
VGA	<50Mbps	Data line 0.7V Control line 5V	5 Line (9-pin connector)/ 9 line (15 pin connector)	Consumer, Computing	TPD4E001 TPD6E001
DVI/ HDMI/ DisplayPort	3.4Gbps	Data Swing 2.7V to 3.3V Control Lines up to 5V	12 Data Lines	Consumer, Computing	TPD8S009 TPD12S520 TPD12S521
LVDS	1.2Gbps	-4V to 5V	2 Line or multiples	Communication, Industrial	TPD2E007
SDIO	<50Mbps	3.3V	7 Lines	Portables	TPD4E001 TPD4E002
RS-485/ RS-422/ RS-232	>200Mbps	-15V to 15V	2 Line or multiples	Communication, Industrial	TPD2E007
‘eSATA	6 Gbps	1V	4 Line	Computing	TPD2E009

IPD @ Computing Interface

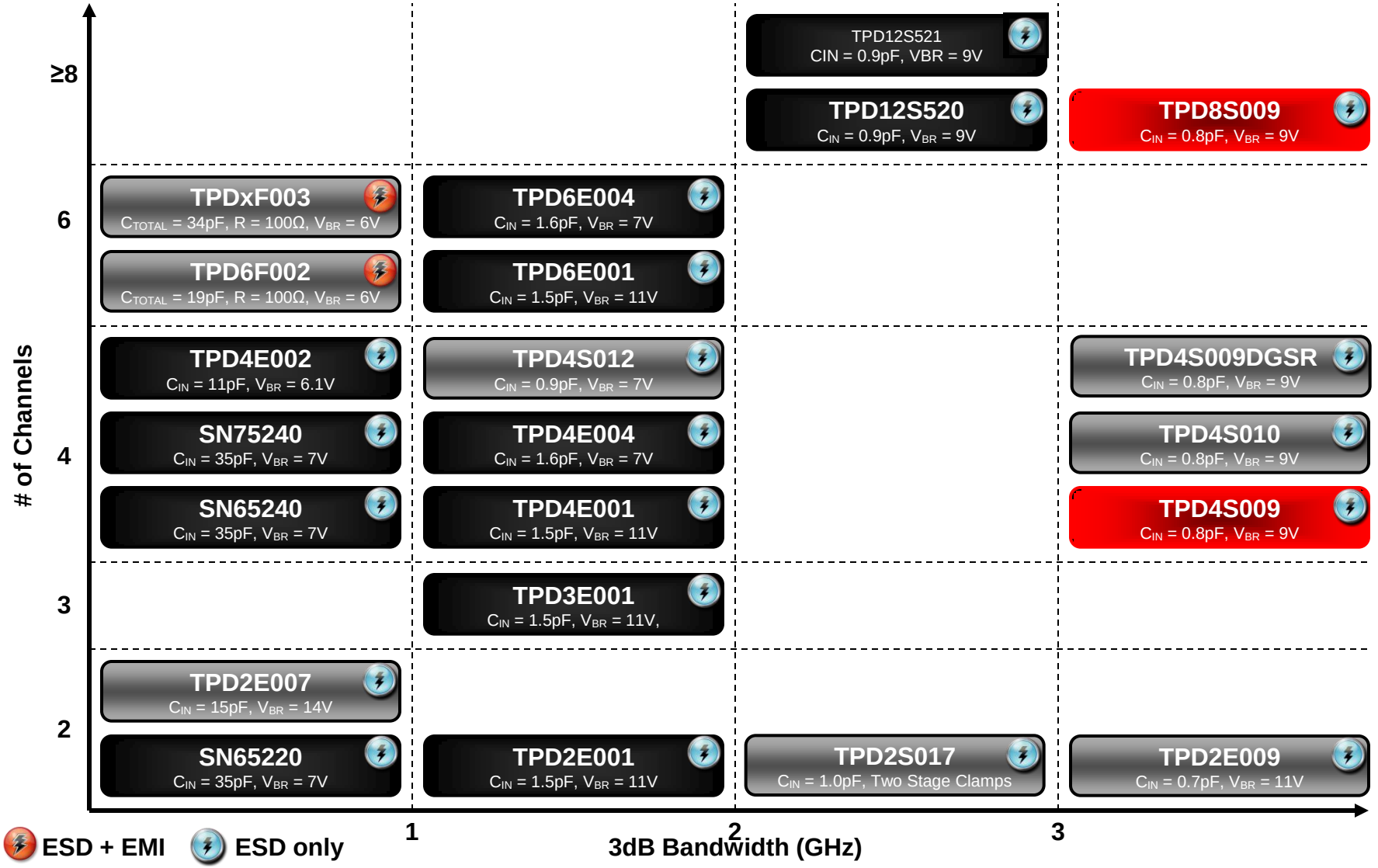


IPD @ LCD TV Interface



ESD / EMI Product Portfolio

(Products Highlighted in RED are New Arrivals, and Gray are 1H,09 Release)



We have Wide Package Solutions for Applications

Package Size

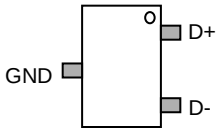
2-Bit PicoStar

TPD2E007YFN
(0.8mm * 0.8mm * 0.15mm)

2-Bit WCSP

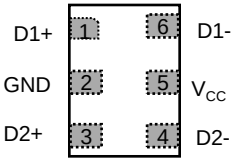
TPD2E004YFP
(0.8mm * 0.8mm * 0.5mm)

2-Bit DRT



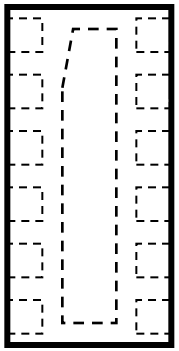
TPD2E009DRT
(1mm * 1mm * 0.5mm)

4-Bit DRY



TPD4S009DRY
(1.45mm * 1mm * 0.6mm)

6-Bit DQD



TPD6F003DSV
(2.5-mm 1.35-mm × 0.75mm)

Bit Width

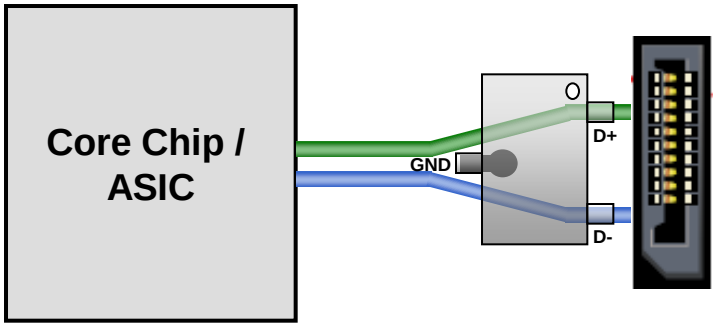
TPD2E009

Samples Now

Two Channel ESD Differential Signal

Key Performance Parameters

- 3-db Bandwidth in excess of **4GHz**
- Optimized package, pin-mapping for high-speed differential lines
- System level ESD protection:
  - ✓ 8kV—Contact
  - ✓ 15kV—Air-gap
- Differential matching less than 0.01pF
- Pin capacitance Less than **0.7pF**
- I_{off}

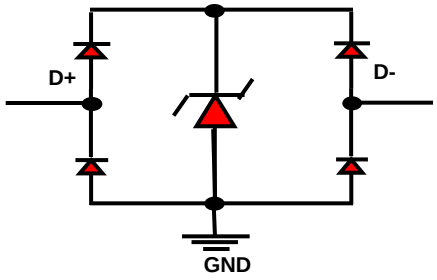


Layout Example at DisplayPort Interface

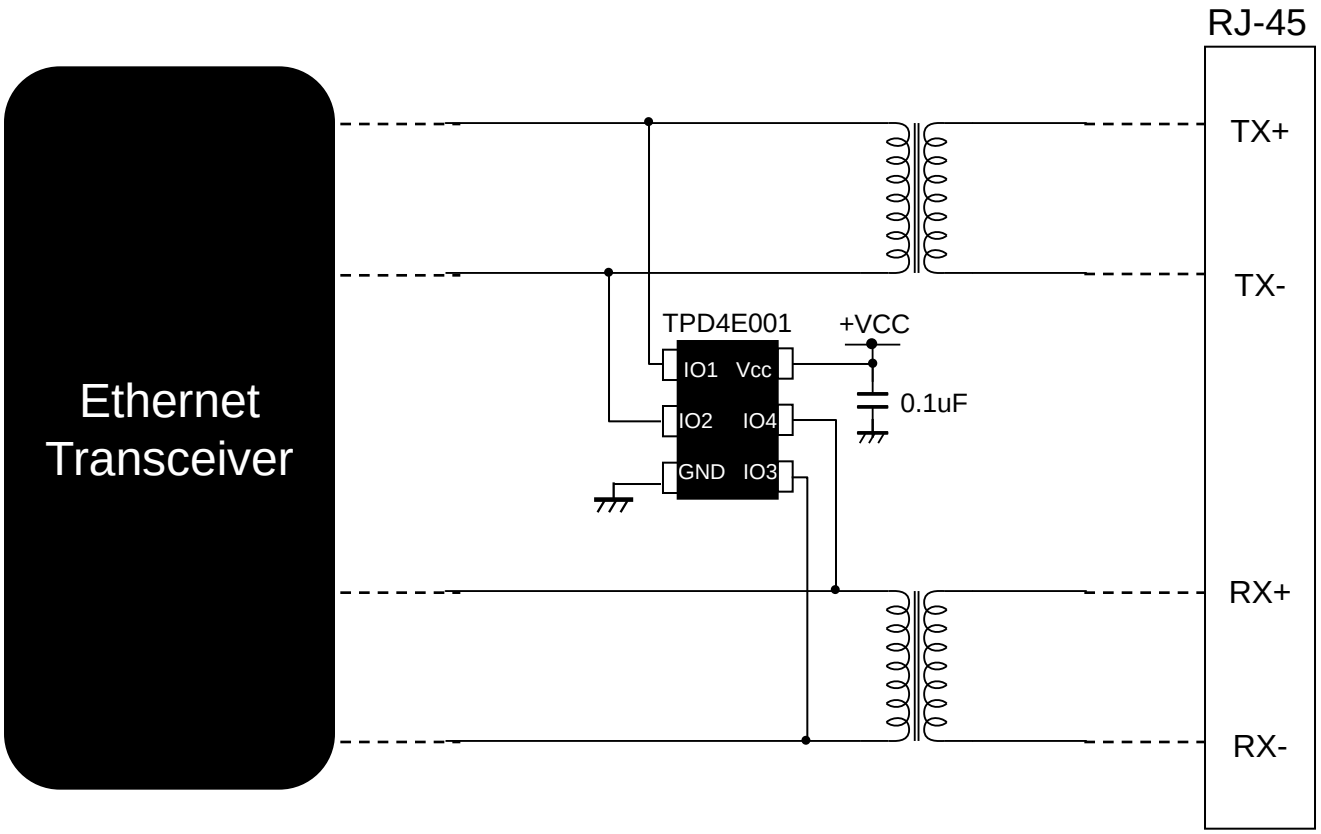
Package	Pitch	Length	Width	Height
3-DBZ	1.9mm	2.9mm	2.37mm	1mm
6-DRY	0.5mm	1.45mm	1.0mm	0.55mm
3-DRT	0.7mm	1.0mm	1.0mm	0.5mm

Benefits

- Flexible layout option to populate ESD chip only if the system ESD is not passing w/o external ESD chip
- No Layout skew for the differential pair
- Minimum distortion in the high-speed lines



TPDxE001: 10/1000BASE-TX PROTECTION

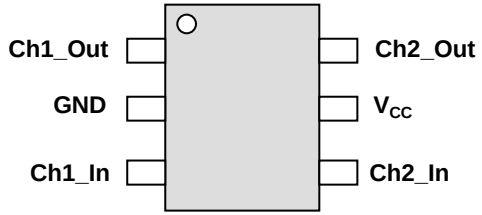


TPD2S017: Dual Channel ESD with Series Resistor Isolation for USB Port

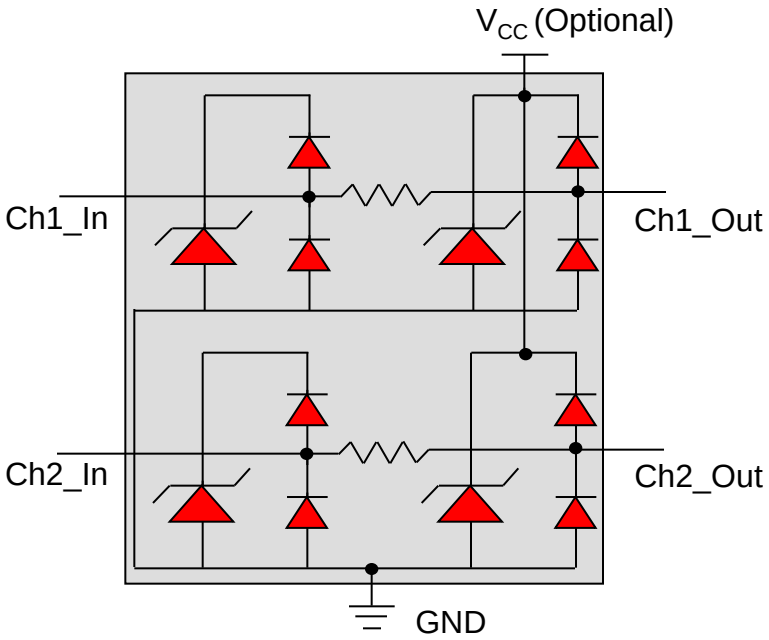
Sample Now

Key Features:

- Ultra low clamp voltage ensures the protection of ultra-low voltage core chipset during ESD events
- Drop-in for the **CM1231**
- Matching-of-series resistor (R =1Ω) of ±10mΩ typical
- Differential channel input capacitance matching of 0.05pF typical.
- High speed data rate and EMI filter action at high frequencies (-3dB bandwidth ~2GHz)
- Available in a 6-pin DBV package
- Flow-through Single-In-Line Pin Mapping for the High-speed Lines Ensures no Additional Board Layout Burden while Placing the ESD Protection Chip near the Connector



6-DBV (Top Side)



Released

TPD8S009

8-Channel ESD Protection for HDMI / DisplayPort

Features

- System-level IEC-61000-4-2 (Level 4) ESD protection
- **Complies with the HDMI 1.3 and Display Port data rate**
- **Differential matching of less than 0.05pF**
- Pin capacitance less than 0.8pF
- I_{off} feature

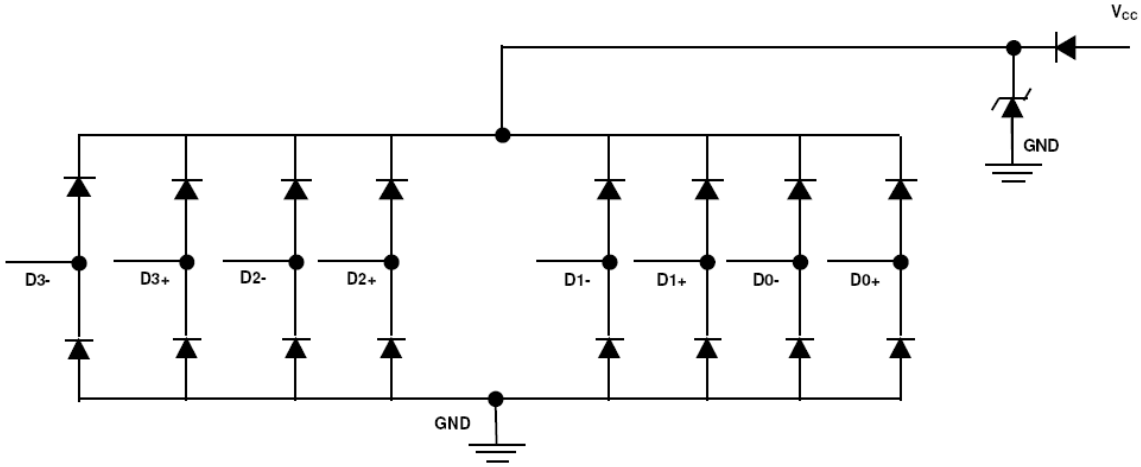
Benefits

- Design allows for line impedance compensation with varying trace widths on-board
- Ultra low capacitance ideal for higher bandwidth applications
- Minimum signal distortion on the high-speed lines
- Optional V_{CC} connection (V_{CC} pin can

Applications

- LVDS signaling lines
- HDMI / DVI
- Display Port
- eSATA interface
- Serial link
- Ethernet port
- PCI Express

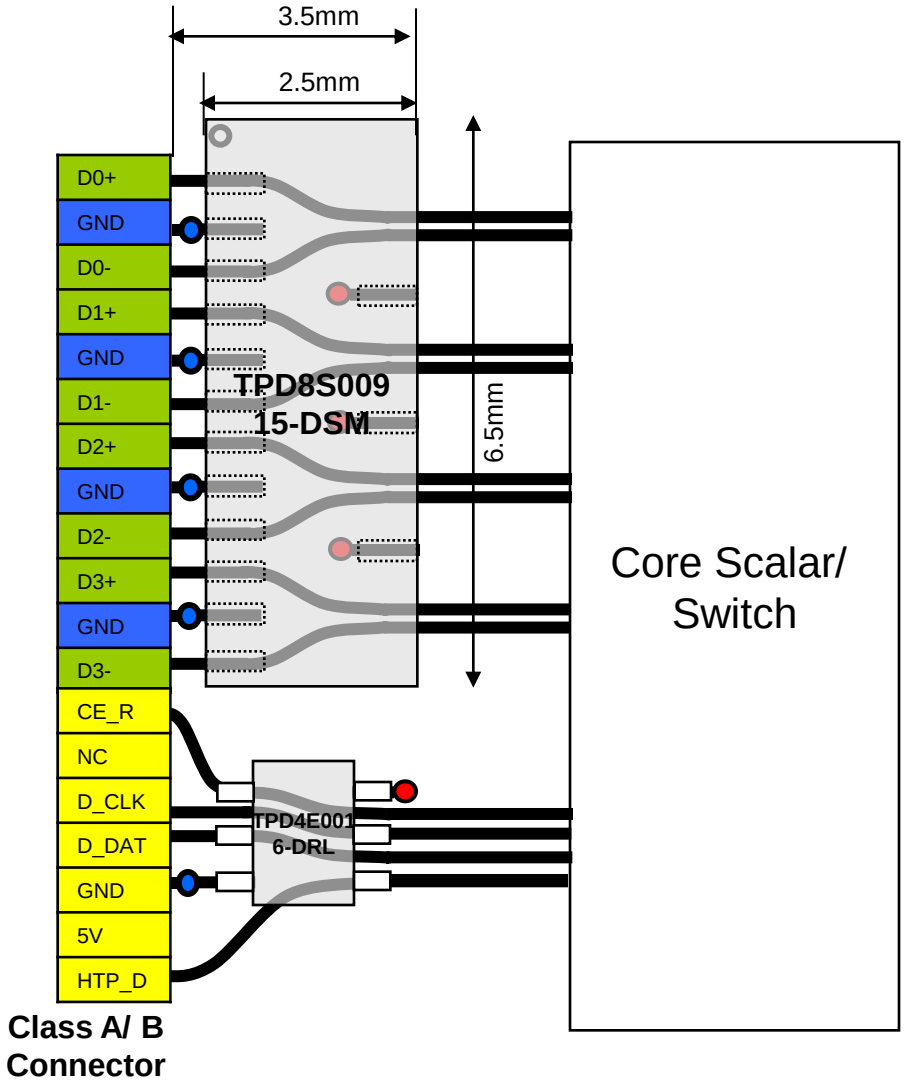
Circuit Diagram



TPD8S009: HDMI/ DisplayPort ESD Solution

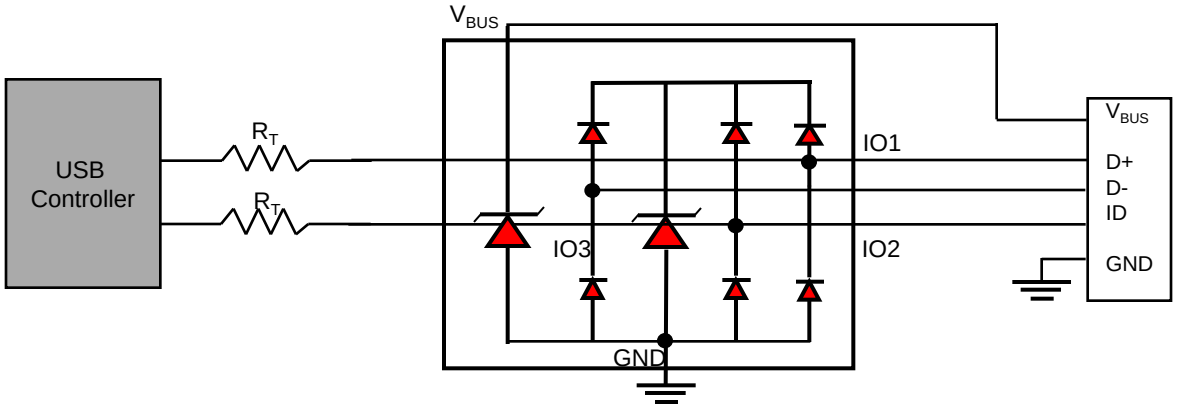
Layout Guidelines for High-speed Differential Lines

- Recommended trace width 10-mills or higher. It is okay to start with ~103-105 ohm differential impedance target (margin of error on the upper side is preferred). When a narrower trace needs to be selected due to board manufacturing cost or other pre-conditions, it is particularly helpful to start with little over 100-ohms and be still within the 15% trace impedance variations with the ESD capacitance effect.
- Minimum separation needs to be same as the trace width. For example, if the trace width is 10 mills, select the trace separation as 10-mills as well
- It is better practice to couple differential traces together as long as possible (as shown in the right layout figure).
- Use shorter stubs to the vias connected to GND, Power supplies, and by-pass capacitors.



Released

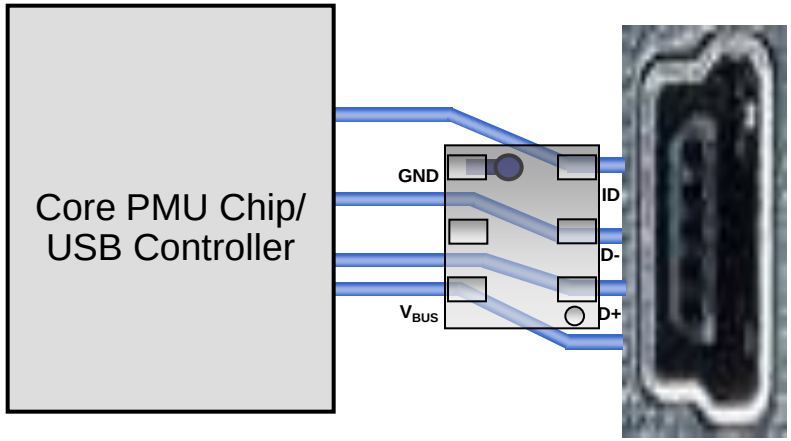
TPD4S012: USB Charger ESD Solution



TPD4S012 in USB2.0 Application

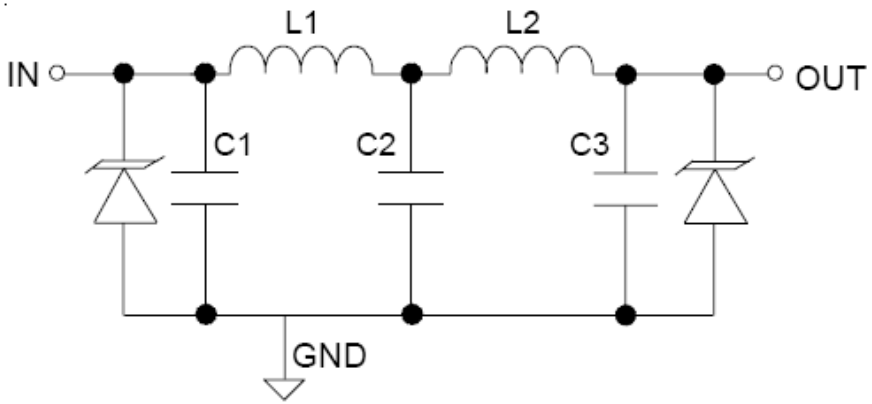
Single-chip ESD solution for USB charger port

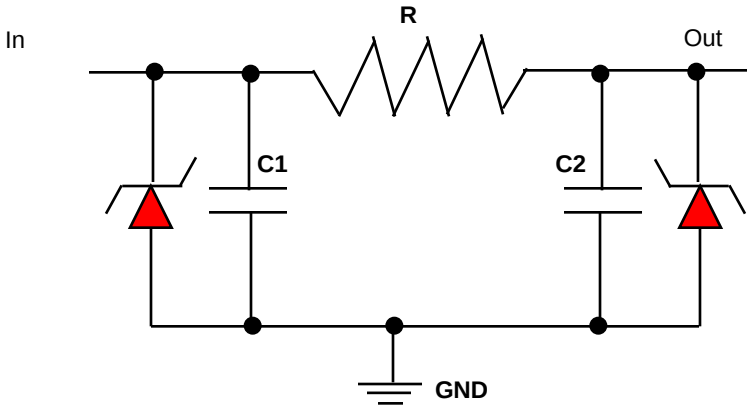
- System level IEC-61000-4-2 (Level 4) ESD protection
- USB HS Lines (D+, D-, ID)
  - ~0.9pF Line Capacitance for
  - 6-V (min) Tolerance
- VBUS Line (V_{BUS})
  - ~9pF Line Capacitance
  - **20-V** (min) Tolerance

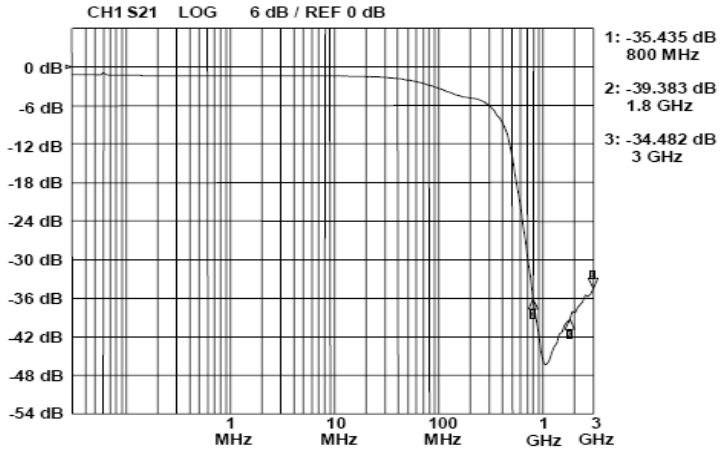


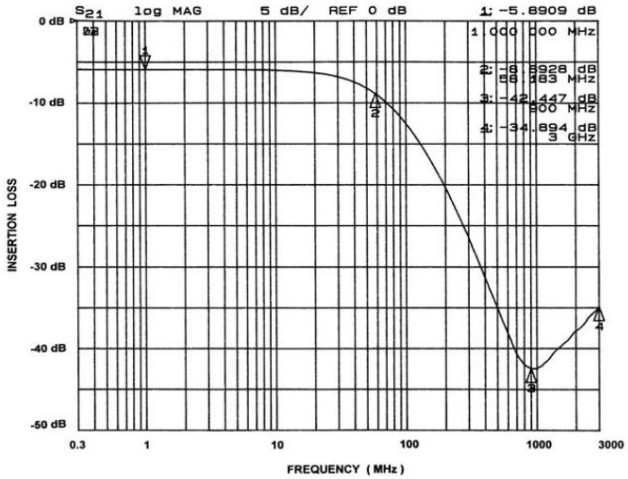
Board Layout with the TPD4S012DRY
DRY (1.45mm 1mm 0.55mm)

EMI Filter: L-C vs R-C?









More challenging to manage series inductor

Less noisy and easy to design with

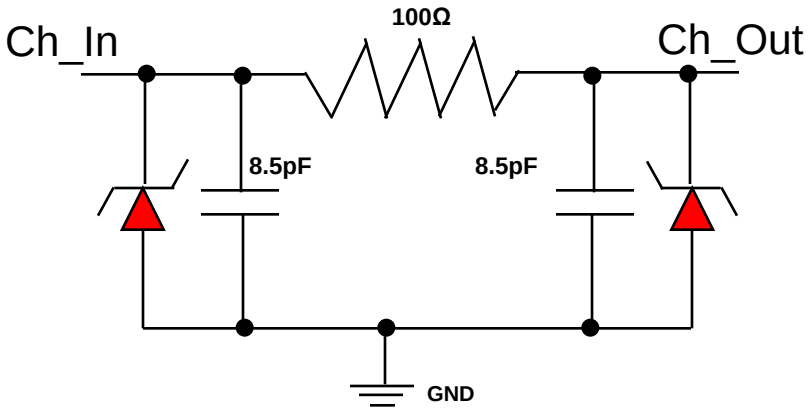
Sample Now

TPD6F003

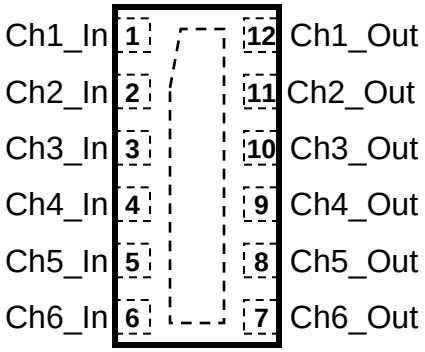
6-Channel EMI Filter for LCD Display Port

Key Performance Parameters

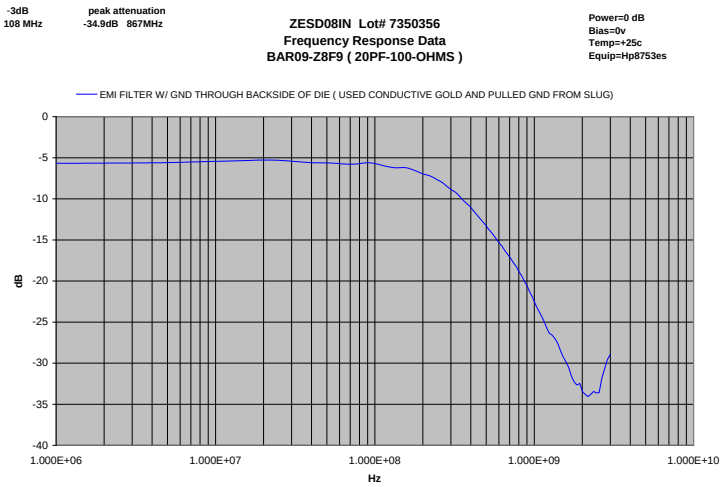
- Six Channel EMI Filtering for Data Ports
- Greater than 32dB attenuation at 1GHz
- -3dB Bandwidth 200MHz
- R-C Topology (R=100Ohm, C=8.5pF)
- System level ESD protection for high speed application:
  - ✓ 15kV—Human Body Model
  - ✓ 8kV—IEC 61000-4-2, Contact Discharge
  - ✓ 15kV—IEC 61000-4-2, Air-Gap Discharge
- Operating IO Voltage Range up to 5.5V
- Space saving package solutions



Schematic Representation



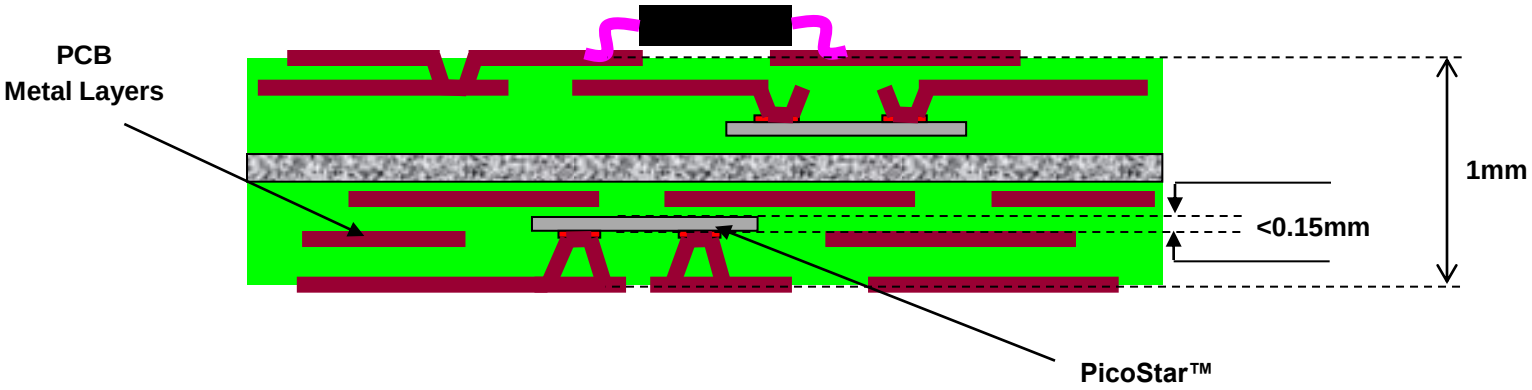
2.5-mm 1.35-mm × 0.75mm DQD

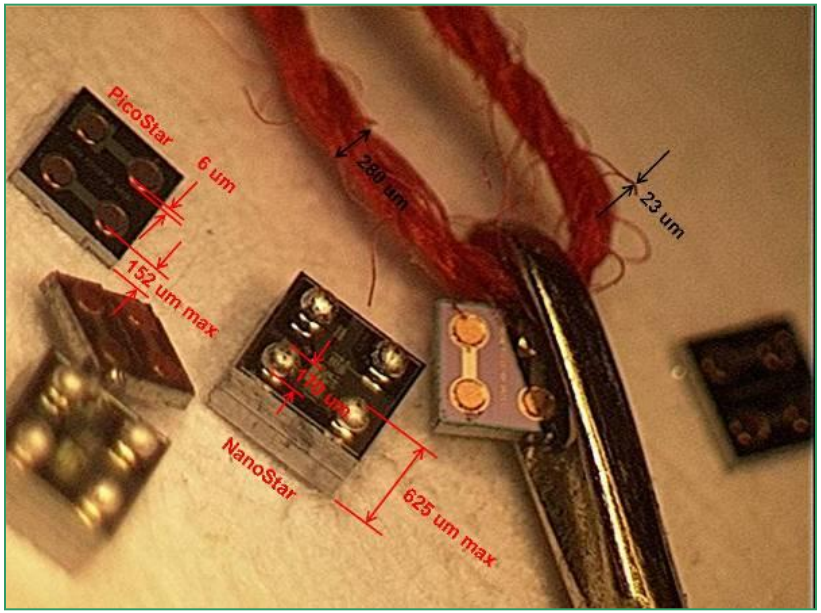


Insertion-loss VS Frequency

PicoStar Embedded Package Technology

Board Cross Section





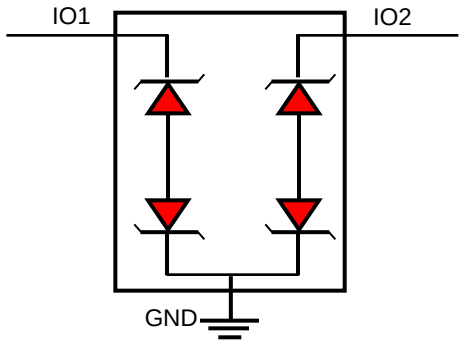
Released

TPD2E007YFMRG4

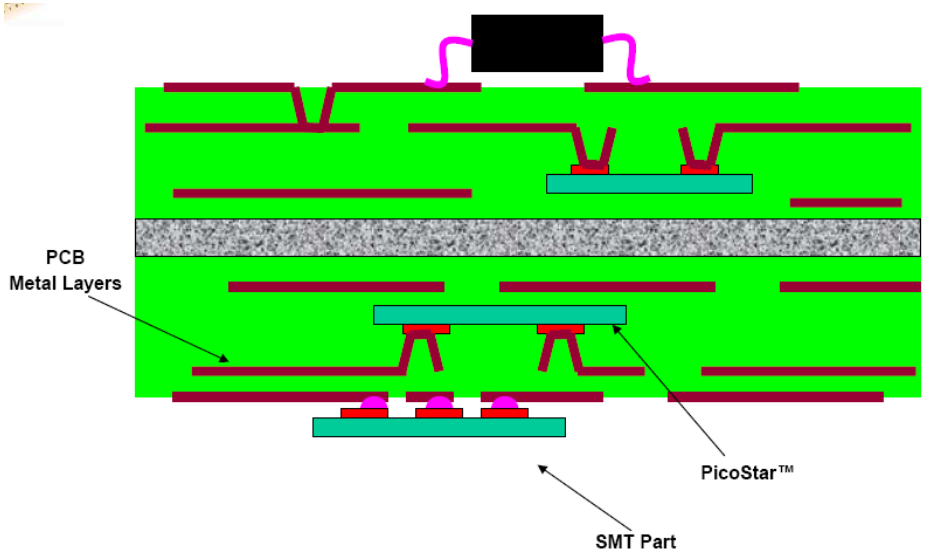
2-Channel ESD in PicoStar Package

Features

- System level ESD protection for high speed application:
  - 8kV—IEC 61000-4-2, Contact Discharge
  - 15kV—IEC 61000-4-2, Air-Gap Discharge
- Breakdown voltage > 14V (@ II=1mA)
- Pin capacitance <15pF (Measured @ VI=2.5V)
- Package height less than 0.15 mm

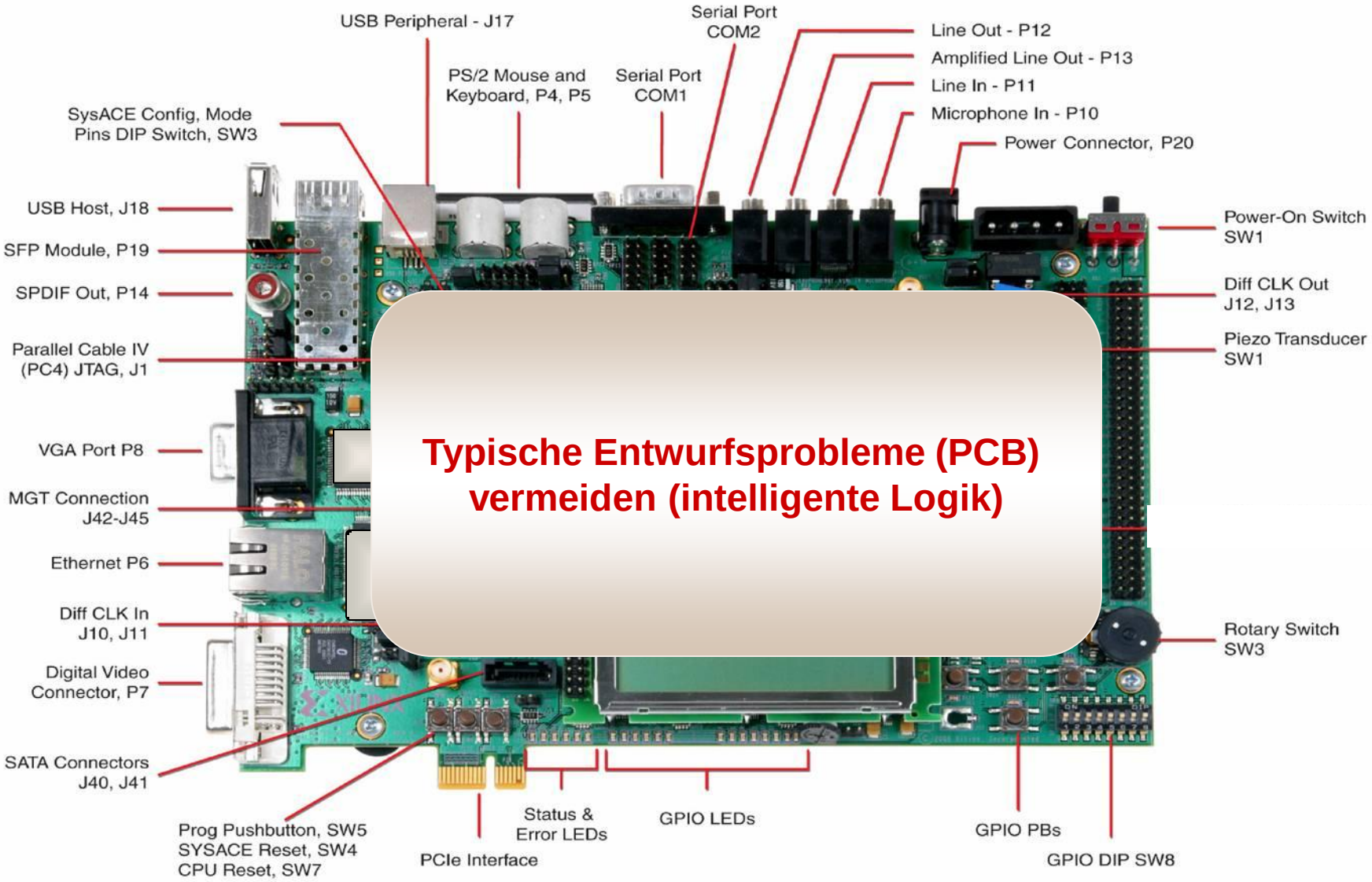


PicoStar Package & Circuit Diagram



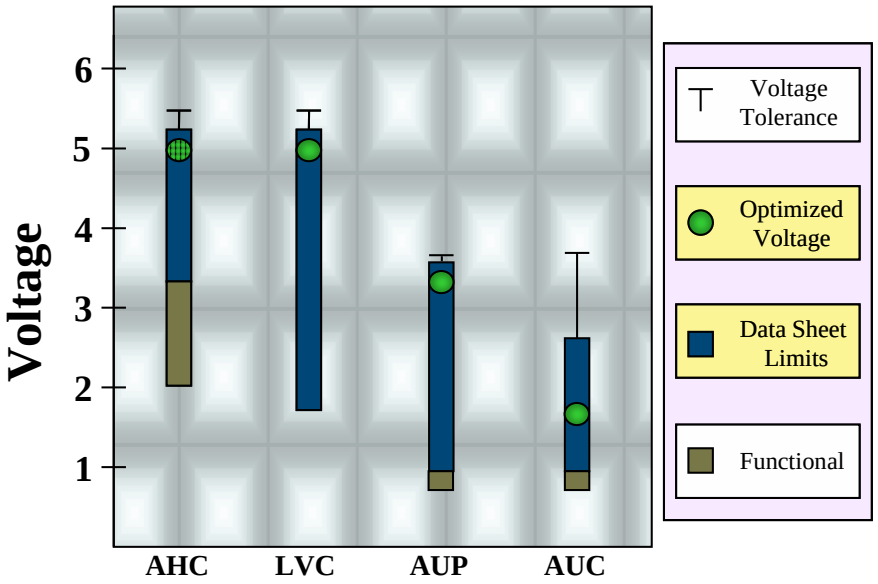
Texas Instruments

Reducing power consumption and noise



Typische Entwurfsprobleme (PCB) vermeiden (intelligente Logik)

Benefits of AUP



	General Purpose	Broadest Portfolio	Lowest Power	Fastest 1.8V Logic
Characteristics	AHC	LVC	AUP	AUC
V_{CC}	2 to 5.5V	1.65 to 5.5V	0.8V to 3.6V	0.8V to 2.7V
I_{CC}	10 uA	10 uA	0.9 uA	10 uA
I_I	1 uA	5 uA	0.5 uA	5 uA
I_{OFF}	N/A	10 uA	0.6 uA	10 uA
I_{OZ}	2.5 uA	5 uA	0.6 uA	10 uA
C_{PD}	18 pF	26 pF	4.3 pF	19 pF
C_{IN}	4 pF	4 pF	1.5 pF	3 pF
C_{OUT}	NS	NS	3 pF	NS
t_{PD} (MAX)	7 ns (15 pF)	3.6 ns (15pF)	4.3 ns (5 pF)	2 ns (30 pF)
I_{OH}/I_{OL}	8 mA	24 mA	4 mA	9 mA

Supports low voltage requirements commonly found in portable devices.

Low static power consumption and leakage current for prolonged battery life.

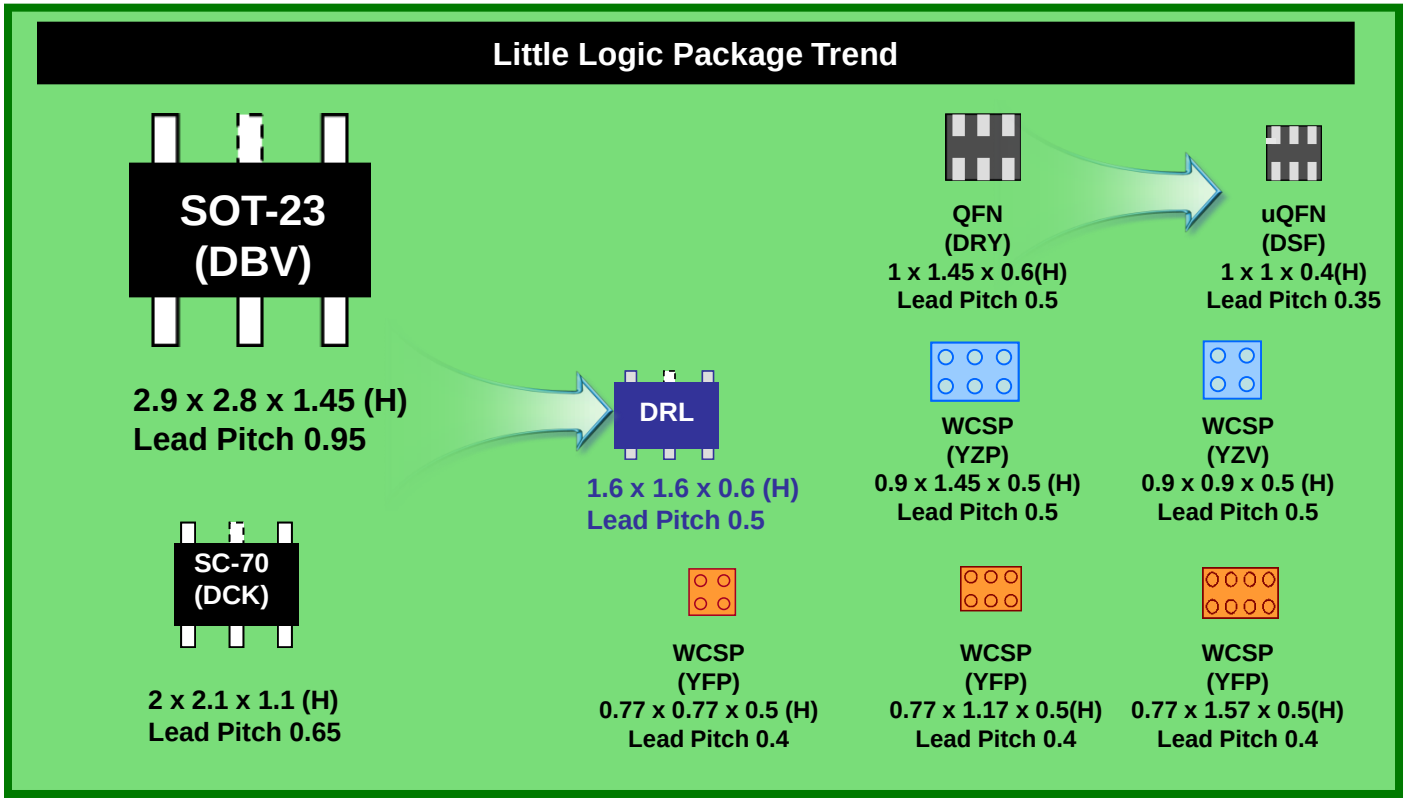
Low dynamic power consumption for minimizing battery drain when the device is toggling.

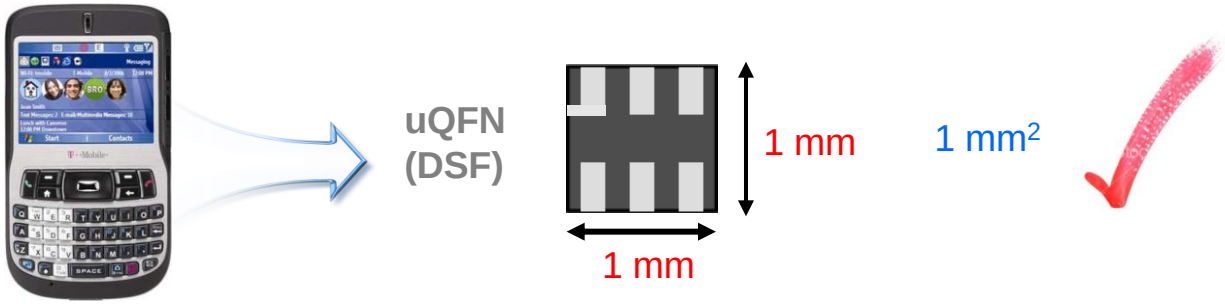
More than adequate speed for most applications.

Reduced drive strength to minimize over / undershoots. Improved signal integrity.

Texas Instruments

Little Logic Technology Overview



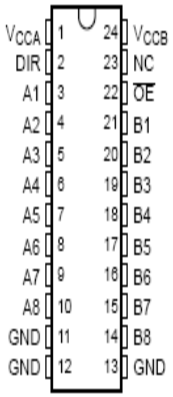


TI Logic special features

Special features of TI standard logic devices are designated in the device number by abbreviation

C – Configurable VCC

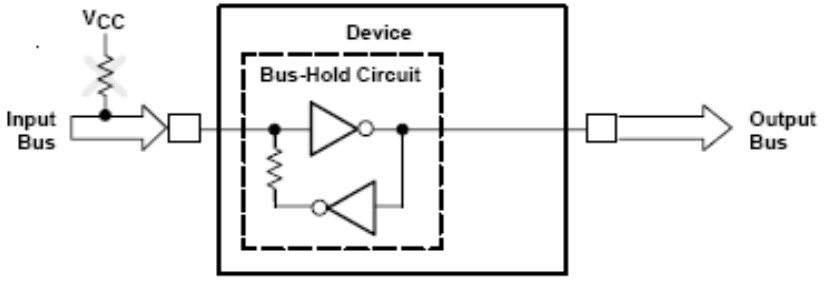
is a feature of devices that are designed as dual-supply level shifters. Using these devices allows selection of the voltage to be applied to VCC on the B-port side (VCCB) and/or A-port side (VCCA)



Designers can use these devices in existing single-voltage systems. When systems become mixed-voltage systems, these devices do not need to be replaced, allowing for quicker time to market.

H – Bus Hold

A bus-hold circuit is implemented in selected logic families to help solve the floating-input problem inherent in all CMOS inputs). The bus-hold circuit maintains the last known input state into the device and, as an additional benefit, pull-up or pull-down resistors no longer are needed.

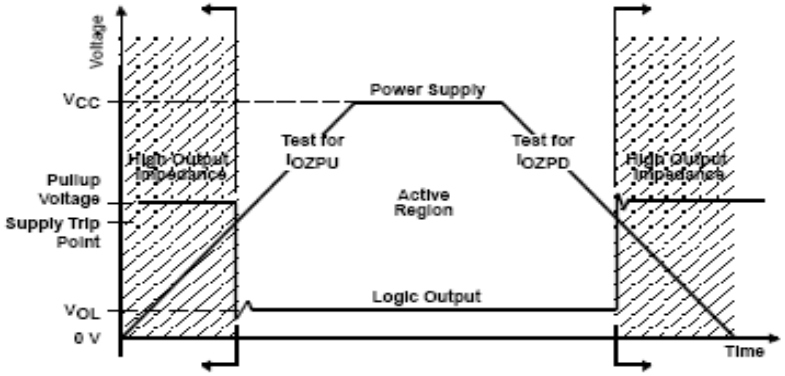


TI Logic special features

Special features of TI standard logic devices are designated in the device number by abbreviations

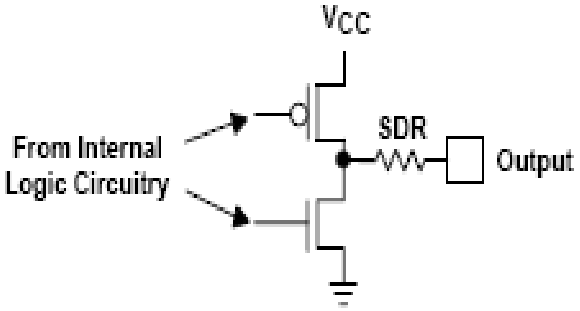
Z- Power- UP 3-State

PU3S is checked dynamically by ramping the power supply from 0 V to its maximum recommended value, then back to 0 V, Δt/ΔVCC the *recommended operating conditions*



R- Damping Resistor on Inputs/Outputs

Series damping resistors (SDR), denoted by R in the device number, are included at all input/output and output ports of designated devices. The SDRs limit the current, thereby reducing signal undershoot and overshoot noise. Additionally, SDRs make line termination easier, which improves signal quality by reducing ringing and line reflections.

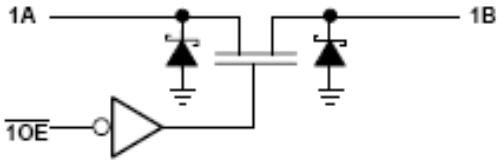


TI Logic special features

Special features of TI standard logic devices are designated in the device number by abbreviations

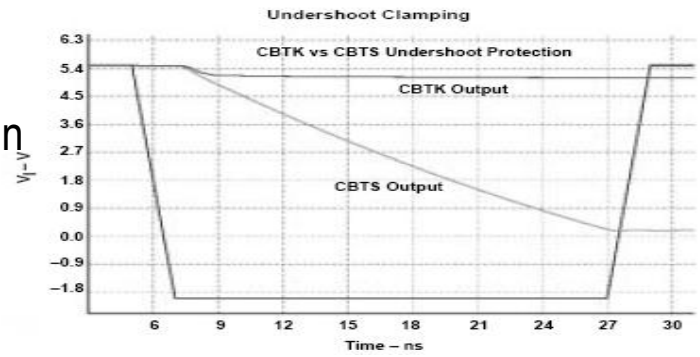
S-Schottky Clamping Diode

Schottky diodes are incorporated in inputs and outputs to clamp undershoot. The Schottky diodes prevent undershoot signals from dropping below a specified level, reducing the possibility of damage to connected devices.



K -Undershoot-Protection Circuitry

TI undershoot-protection circuitry (UPC) functions similarly to Schottky clamping diodes, with one major difference. UPC is an active clamping structure. UPC can greatly reduce undershoot voltage, increasing protection from corrupted data



Logic Families Extra Features

- **Bus Hold – ABT, ALVC, ALVT, AVC, AUC, FCT, GTL, GTLP, LVC, LVT, VME**
  - Bus-hold circuitry in selected logic families helps solve the problem of floating inputs and eliminates the need for pull-up or pull-down resistors by holding the last known state of the input. See $I_{I(HOLD)}$ or I_{BHL}, I_{BHH}, I_{BHLO}, and I_{BHHO} on data sheet.
- **Series Damping Resistors – ABT, ALVC, ALVT, F, GTLP, LVC, LVT, VME**
  - Series damping resistors limit signal overshoot and undershoot by providing better impedance matching and line termination without the need for external resistors.
- **Partial Power Down (Level 1 Isolation - I_{off}) – ABT, ALVT, AVC, AUC, AUP, CBTLV, CBT-C, GTL, GTLP LV-A, LVC, LVT, VME**
  - IOFF circuitry prevents the device from being damaged during hot insertion. See IOFF specifications on data sheet.
- **Hot Insertion (Level 2 Isolation – Ioff and Power-up 3-state) – ABT, ALVT, GTLP, LVCZ, LVT, VME**
  - Power-up 3-state ensures valid output levels during power up and valid Z on the outputs during power down. See IOZPU, IOZPD.
- **Live Insertion (Level 3 Isolation – Ioff, Power-up 3-state, and BIAS VCC) – GTLP, FB, CBT, CBTLV, VME**
  - Precharges I/O capacitance, preventing glitching of active data.
- **Mixed-Voltage-Tolerant I/Os and Level Shifting – AVC, ALVC, ALVT, AUC, AUP, GTL, GTLP, LV-A, LVC, LVT**
  - Systems use mixed supply voltages and TLL or CMOS levels in many designs. Most advanced-logic families allow mixed-signal interfacing and provide level-shifting functions for certain mixed-voltage applications.
- **JTAG – ABT, ACT, BCT, LVT**

(†selected functions)