NexFET™ MOSFETs

How To Design with Highly Efficient MOSFETs

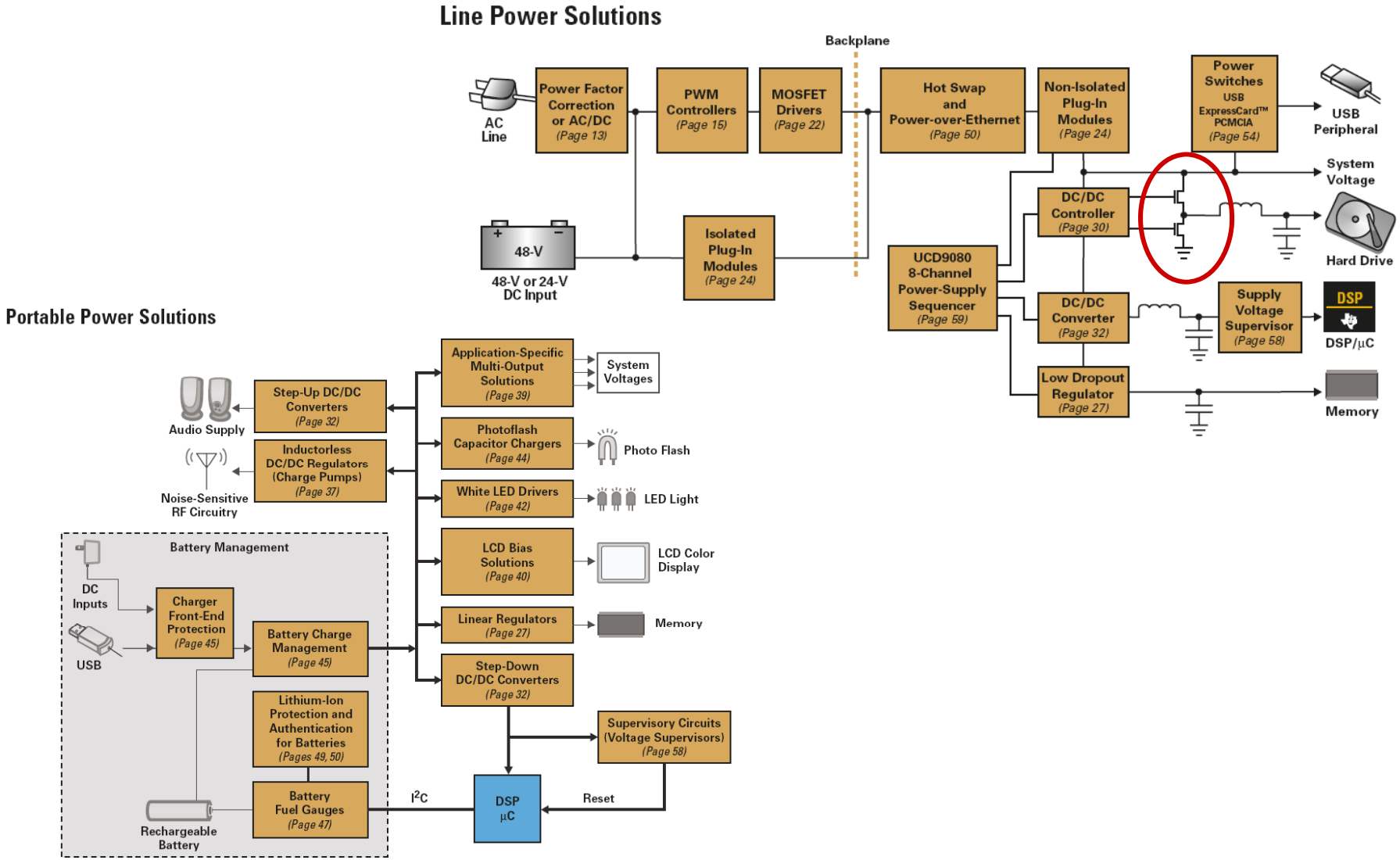
Dirk Gehrke

Texas Instruments

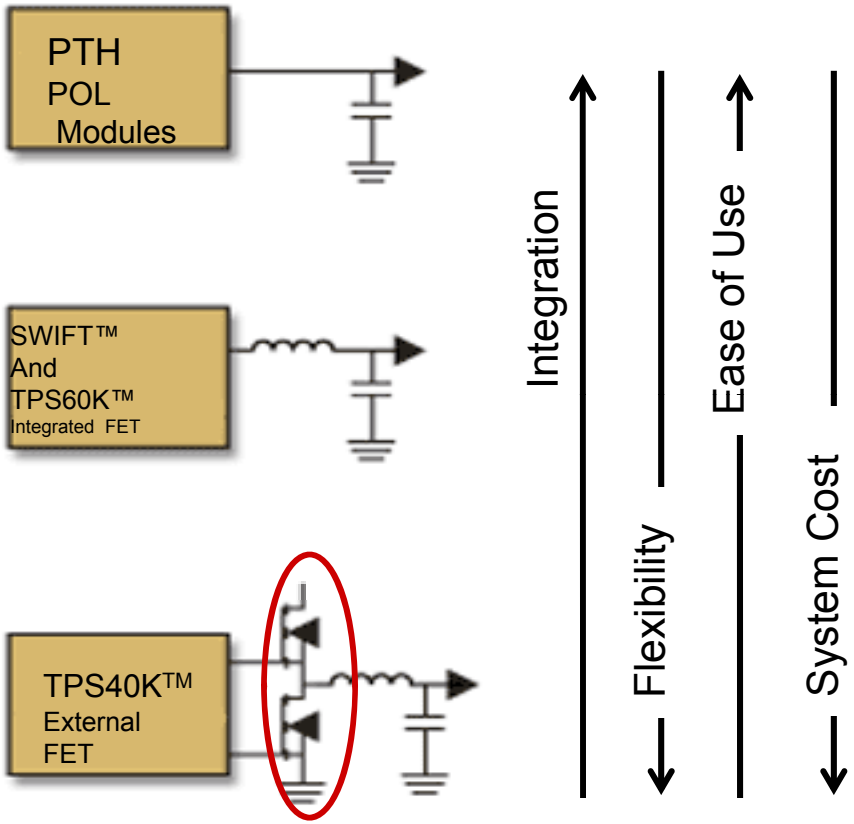
NexFET™ Technology

Texas Instruments

TI Power Products - from Line to Load



POL DC/DC Solutions for Every Need



Plug In Power Modules - PTH series

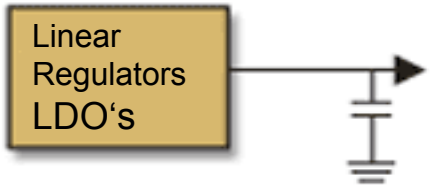
- Complete DC/DC solution
- Second sourced footprint and functionality – POLA alliance
- Fastest time to market

Integrated FET Regulators (SWIFT and TPS60K)

- Integrated power MOSFETs simplify design and consume less board space
- Fewer components reduce bill of material
- Easy-to-use software tool saves development time

External FET Regulators (TPS40K)

- Application and design flexibility available to the user
- Excellent total systems cost/value
- Easy-to-use software tool saves development time



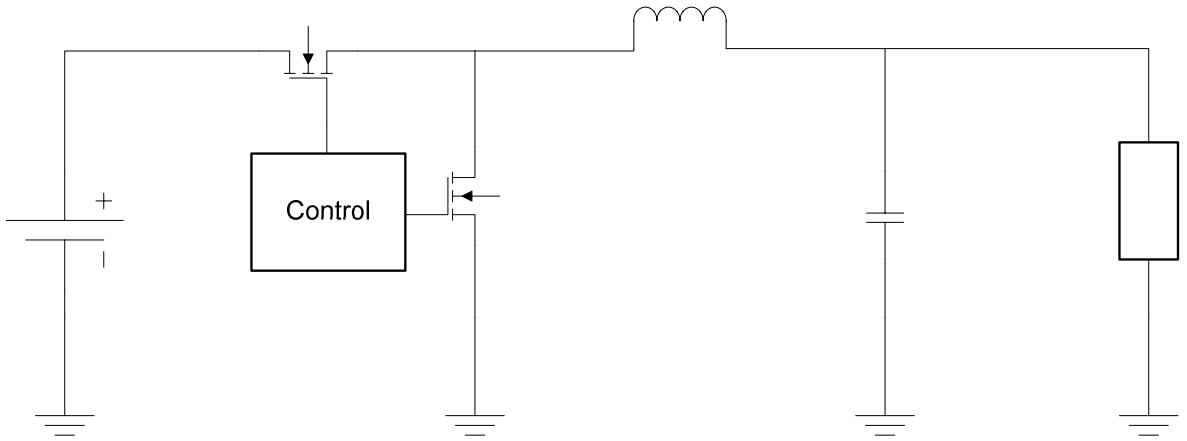
Linear Regulators (TPS7k)

- Simple cost effective implementation
- Depending on the power ratio very efficient

Synchronous Buck Converter – Power Loss Contributors

Conduction Losses
MOSFETs
Inductor
PCB Copper Trace Losses

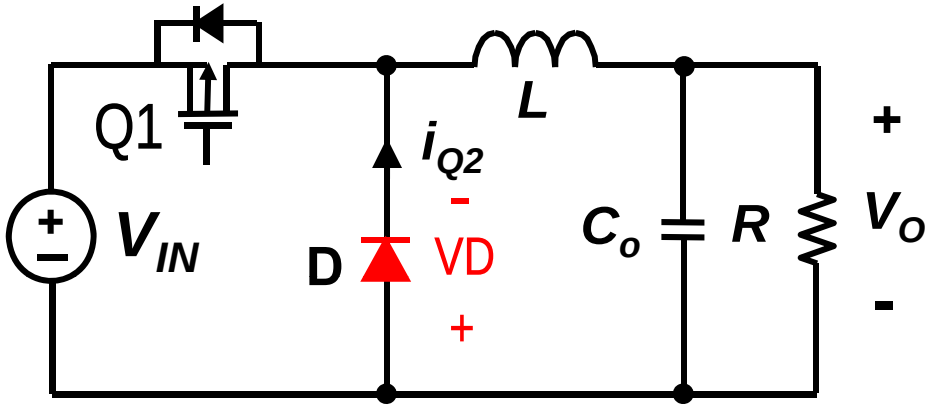
Switching Losses
MOSFETs
Inductor
Gate drive



Static Losses
Control Circuit
Feedback Circuit

Step-Down (Buck) Converter Topologies

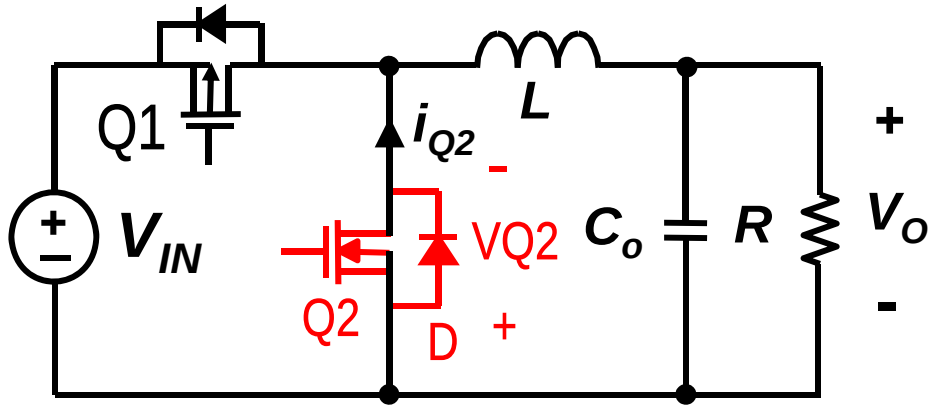
Non-Synchronous Buck



$$i_{Q2} \cdot R_{DSON} < V_D$$

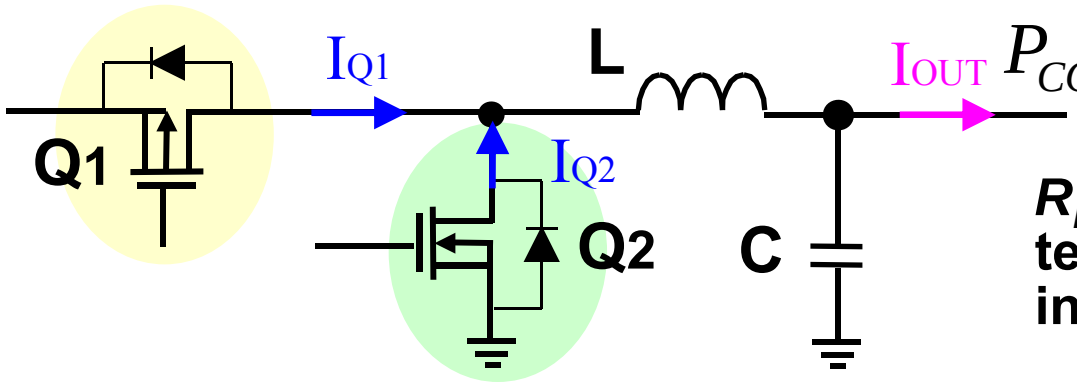
$$P_{Diode} > P_{MOSFET}$$

Synchronous Buck



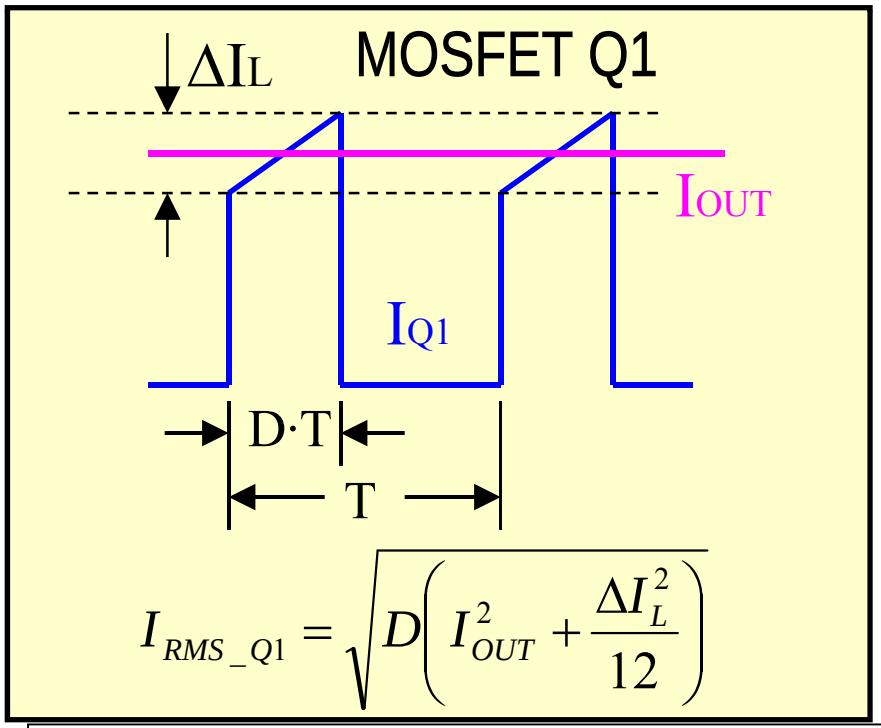
Higher Efficiency:
Parallel Q2 with an external Schottky diode
Longer Battery Run-Time

MOSFET Conduction Losses

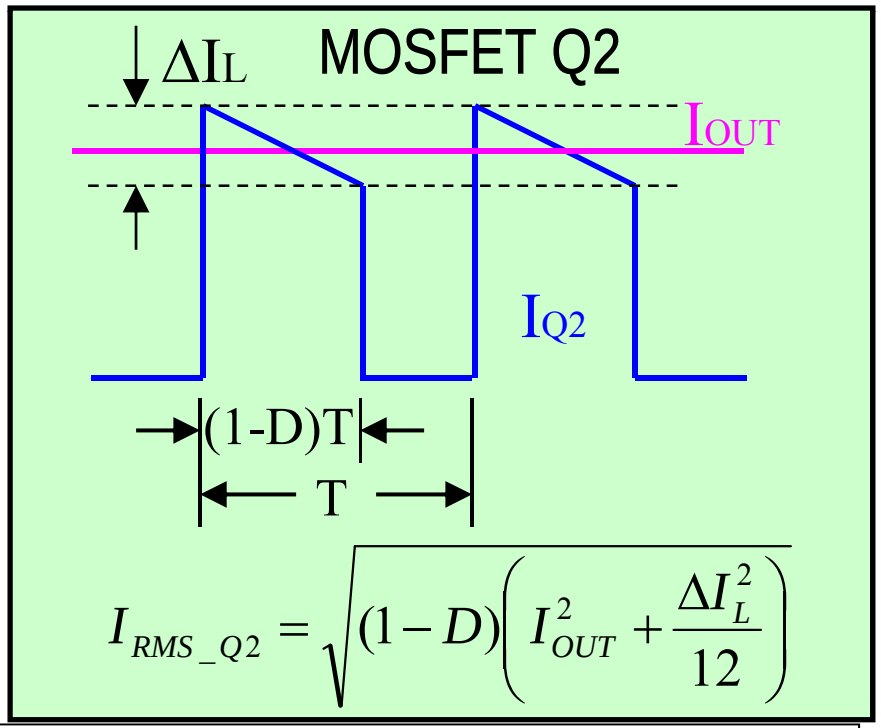


$$P_{COND\_FET} = I_{RMS}^2 \cdot R_{DSON}$$

$R_{DS(ON)}$ is a function of temperature, normally increases by 0.39%/°C



$$I_{RMS\_Q1} = \sqrt{D\left(I_{OUT}^2 + \frac{\Delta I_L^2}{12}\right)}$$



$$I_{RMS\_Q2} = \sqrt{(1-D)\left(I_{OUT}^2 + \frac{\Delta I_L^2}{12}\right)}$$

$$P_{CON} = R_{DS(on)} \times I_{QSW(RMS)}^2 = R_{DS(on)} \times \frac{V_{OUT}}{V_{IN}} \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12}\right)$$

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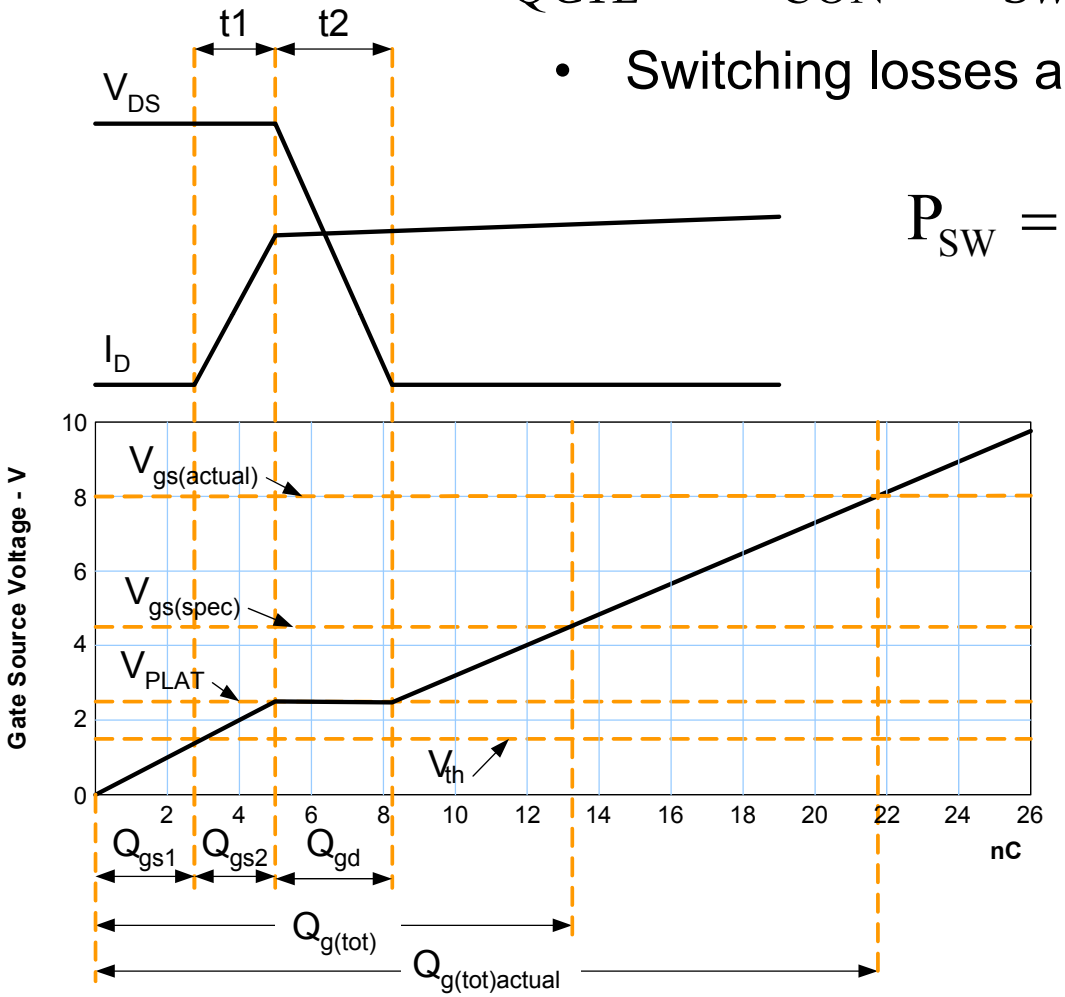
Control FET Losses

$$P_{QCTL} = P_{CON} + P_{SW} + P_{GATE}$$

- Switching losses are more complex

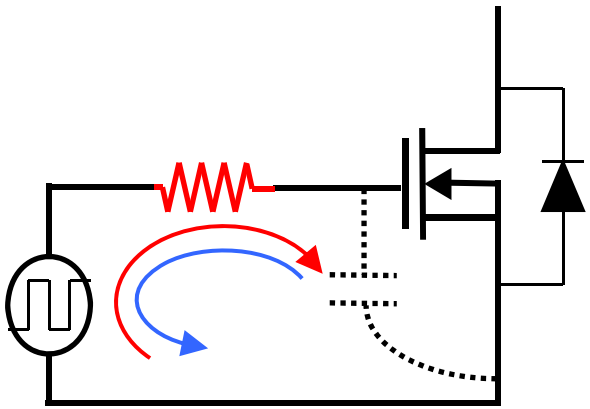
$$P_{SW} = V_{IN} \times I_{OUT} \times F_S \times \frac{(Q_{gs2} + Q_{gd})}{I_g}$$



- Steps to derive loss equation
  - $E_{t1} = (V_{DS} \times I_D/2) \times t1$
  - $E_{t2} = (V_{DS}/2 \times I_D) \times t2$
  - $P_{SW} = 2 \times (E_{t1} + E_{t2}) \times F_S$
  - $t1 = Q_{gs2}/I_g$
  - $t2 = Q_{gd}/I_g$

Control MOSFET Gate Losses

- Gate losses due to energy required to charge the gate. $Q_{g(tot)}$ at the gate voltage of circuit
- Turn on and turn off gate losses
- Most of this power is in the MOSFET gate driver



$$P_{GATE} = Q_{g(tot)} \times V_g \times F_S$$

Rectifier MOSFET Total Losses

$$P_{QSR} = P_{CON} + P_{BD} + P_{GATE}$$

- Conduction losses are simple I^2R losses when the MOSFET channel conducts.
  - R is the $R_{DS(ON)}$ of the selected MOSFET
  - I is the root mean square current through the MOSFET
  - $t_{DLYUpLo}$ is the delay between upper MOSFET turning off and lower MOSFET turning on.
  - $t_{DLYLoUp}$ is the delay between lower MOSFET turning off and upper MOSFET turning on

$$P_{CON} = R_{DS(on)} \times \left(1 - \frac{V_{OUT}}{V_{IN}} - (t_{DLYUpLo} + t_{DLYLoUp}) \times F_S\right) \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12}\right)$$

Rectifier FET Body Diode Losses

Average body diode current should be calculated

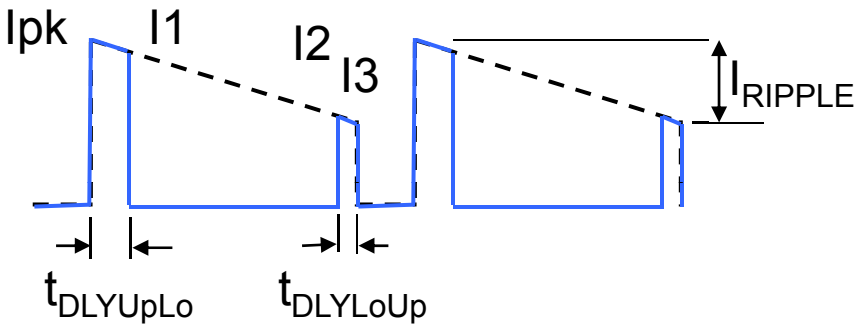
- Derive average current in body diode.

$$I_1 = I_{PK} - \frac{V_O \times t_{DLYUpLo}}{L}$$

$$I_2 = I_{PK} - I_{RIPPLE} + \frac{V_O \times t_{DLYLoUp}}{L}$$

$$I_{AVGUpLo} = I_{PK} - \frac{V_O \times t_{DLYUpLo}}{2 \times L}$$

$$I_{AVGLoUp} = I_{PK} - I_{RIPPLE} + \frac{V_O \times t_{DLYLoUp}}{2 \times L}$$



$$I_{BD(AVG)} = \left(\left(I_{PK} - \frac{V_O \times t_{DLYUpLo}}{2 \times L} \right) \times t_{DLYUpLo} + \left(I_{PK} - I_{RIPPLE} + \frac{V_O \times t_{DLYLoUp}}{2 \times L} \right) \times t_{DLYLoUp} \right) \times F_S$$

- Approximate using:

$$P_{BD} \approx V_f \times I_{OUT} \times \left(t_{DLYUpLo} + t_{DLYLoUp} \right) \times F_S$$

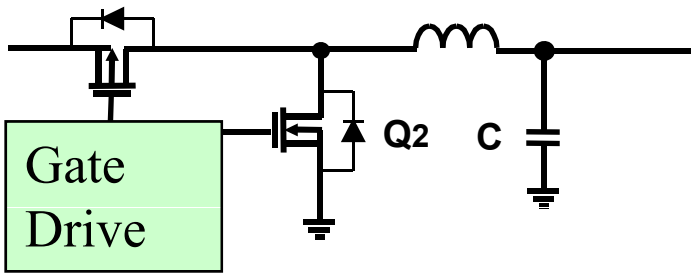
- Reverse Recovery Losses

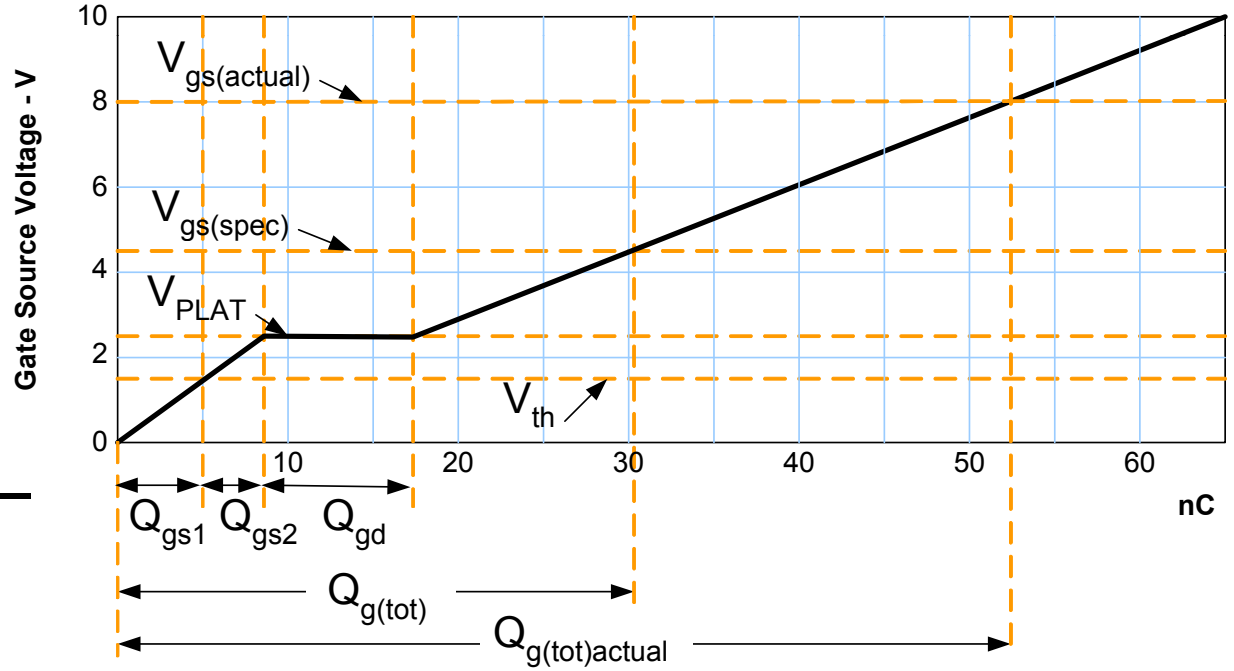
$$P_{RR} = V_{IN} \times Q_{RR} \times F_{SW}$$

Rectifier MOSFET Gate Losses

- Gate losses are calculated in the same manner as switching MOSFET.
- Due to higher gate charge losses can be significant.

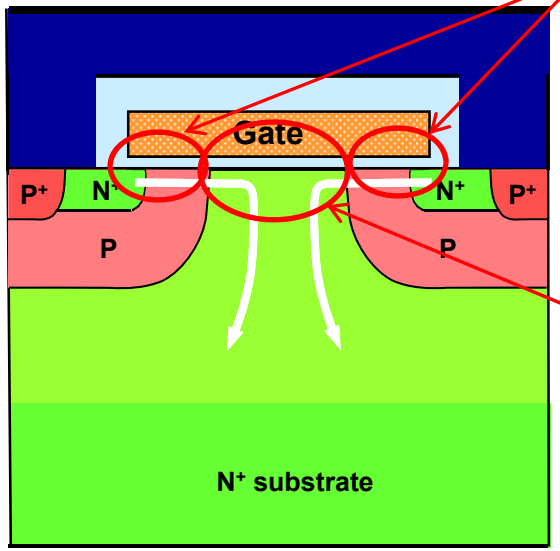
$$P_{GATE} = Q_{g(tot)} \times V_g \times F_S$$



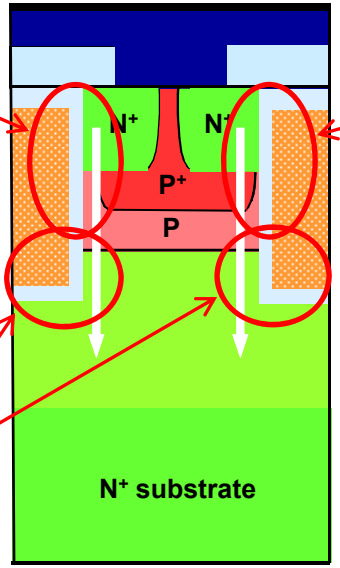


Technology Comparison

Planar
- Commercialized in 1980's
- Lower density structure
- Relative large gate area
- Mid resistance and charge



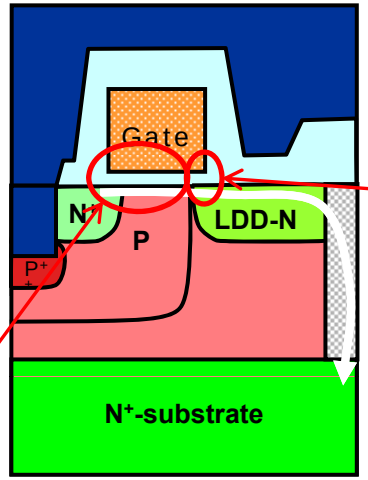
Trench
- Commercialized in the 1990's
- Very High Density structure
- Large gate area
- Low resistance, high charge



C_{GS}

C_{GD}

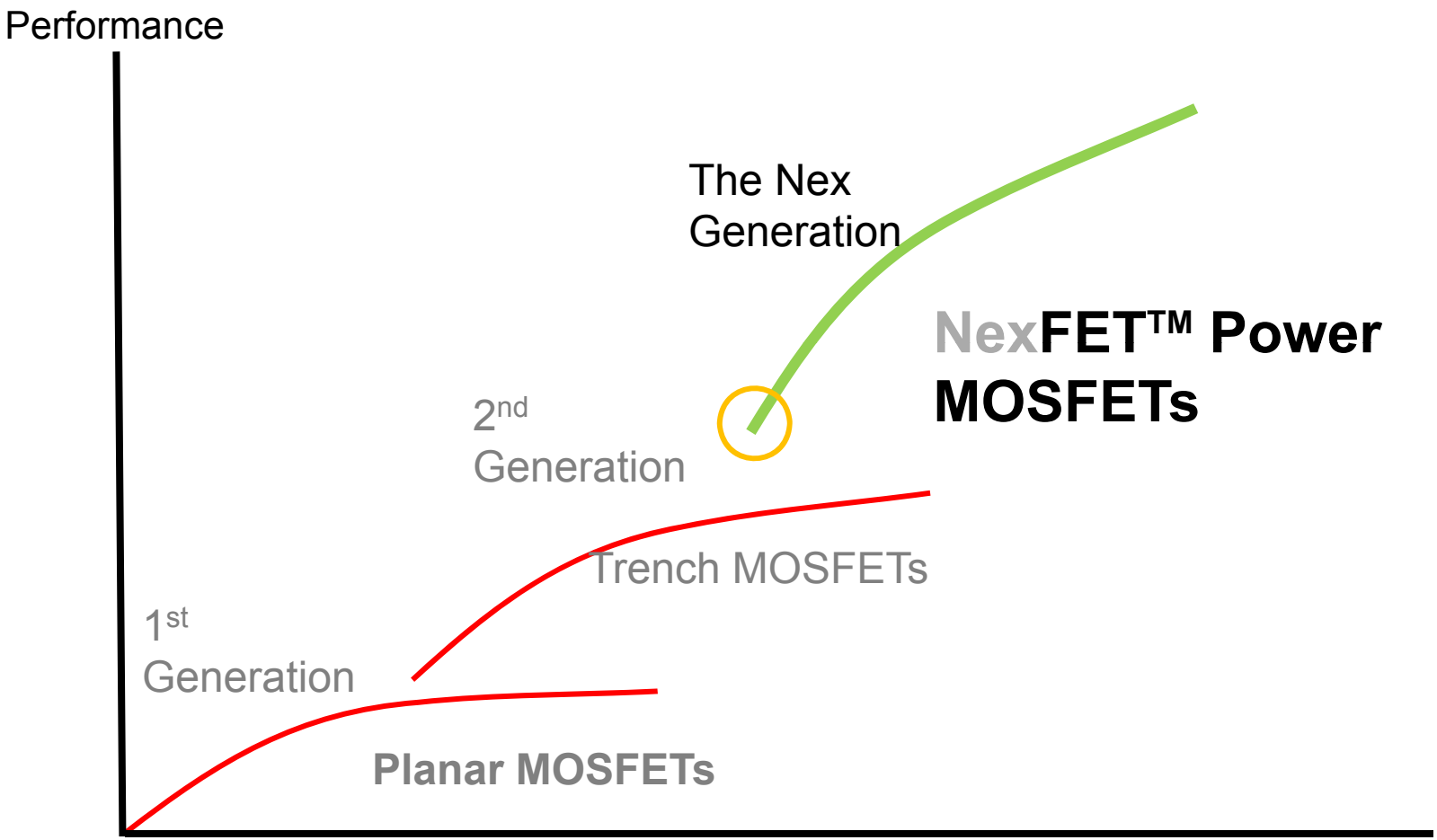
C_{GS}



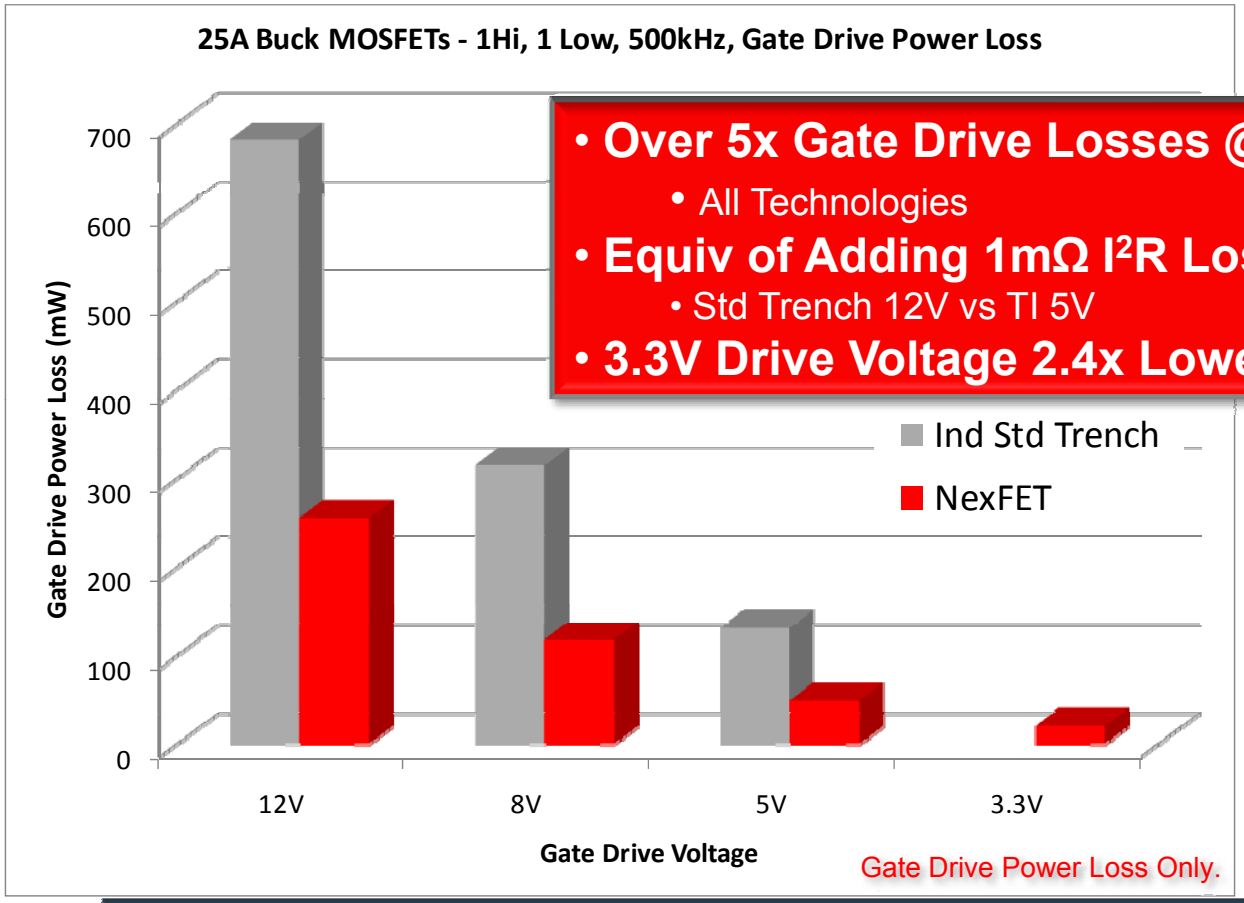
C_{GD}

NexFET™ Technology
- Commercialized in 2007
- High density structure
- Low gate charge
- Low resistance & charge

Just the Beginning



Gate Drive Loss Increase with V_{GS}



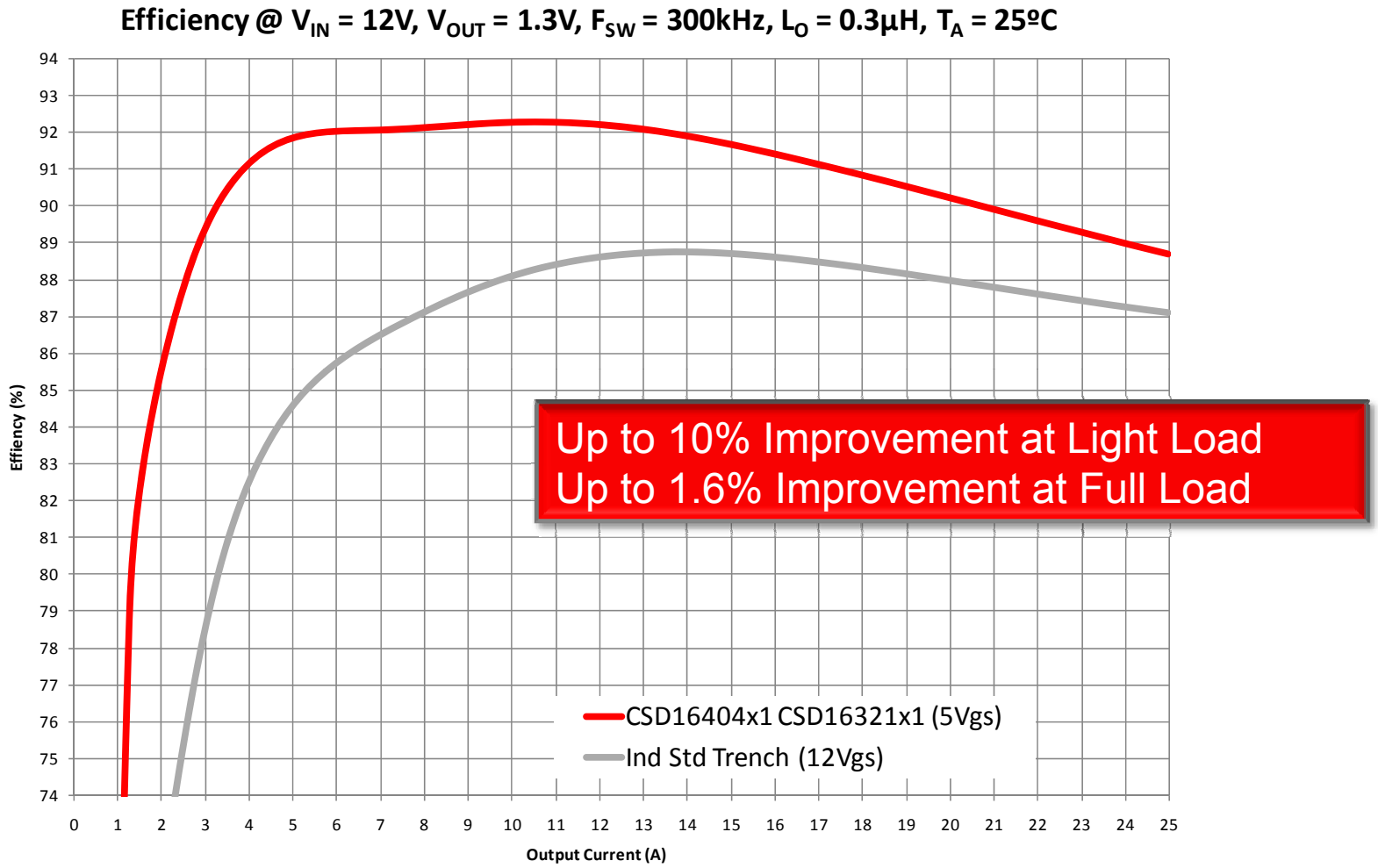
- **Over 5x Gate Drive Losses @ 12V vs. 5V**
  - All Technologies
- **Equiv of Adding 1mΩ I^2R Losses per Phase**
  - Std Trench 12V vs TI 5V
- **3.3V Drive Voltage 2.4x Lower Losses vs. 5V**

V^2 Relationship of Drive Voltage to Energy wasted

$E=CV_{GS}^2$

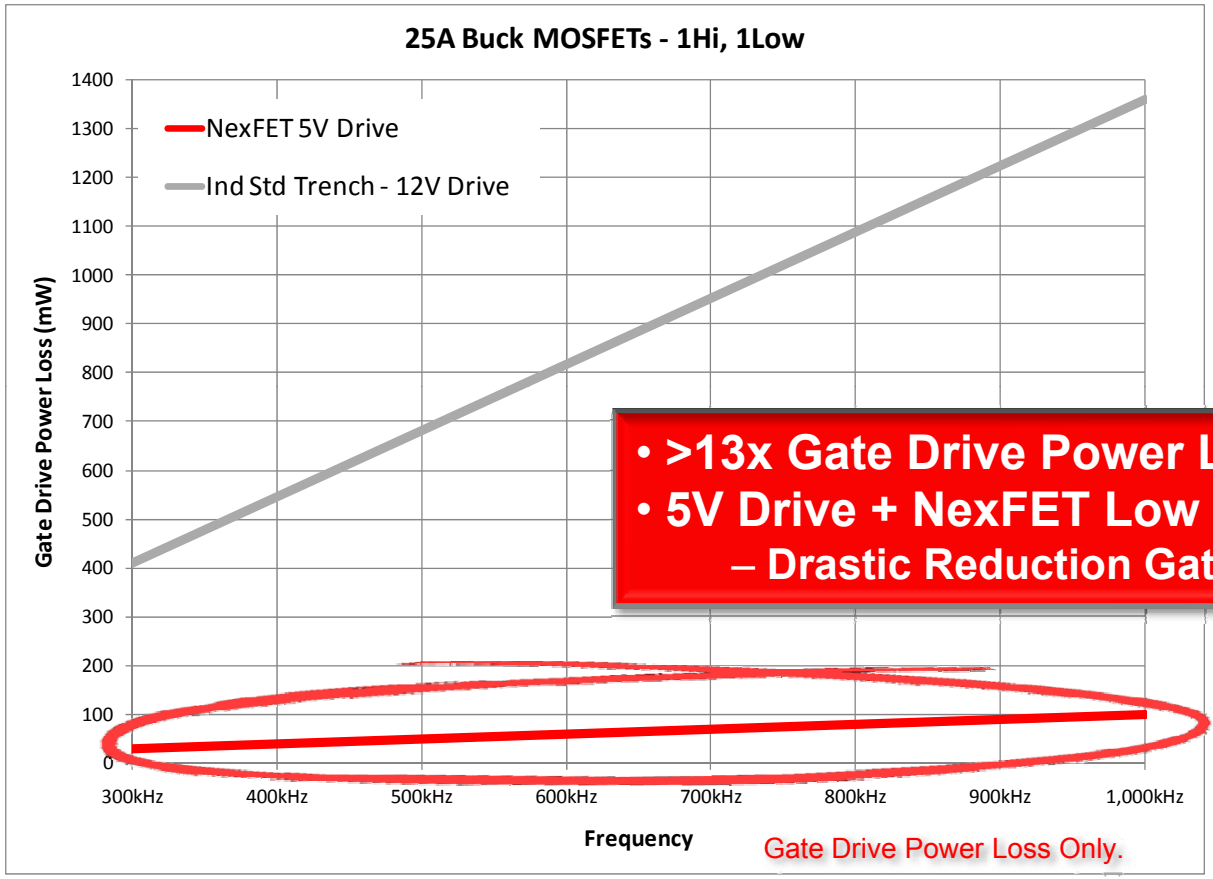
$E=\frac{1}{2}CV_{GS}^2$ for charge and discharge of gate

Improved Efficiency Across the Range



$5V_{GS}$ Better Full Load Even with Comp FET Fully Enhanced @ $12V_{GS}$

Gate Drive Loss Increases with Frequency

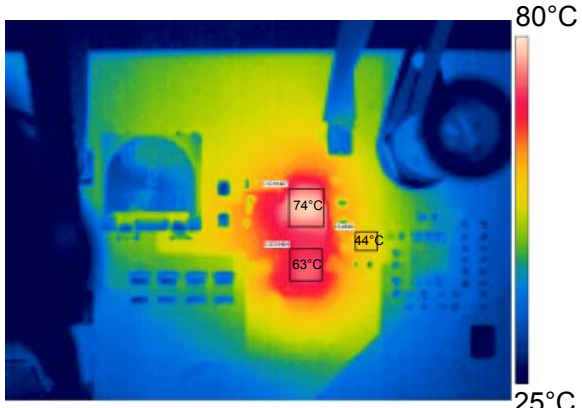


- >13x Gate Drive Power Loss for 12V
- 5V Drive + NexFET Low Q_G
  - Drastic Reduction Gate Drive Losses

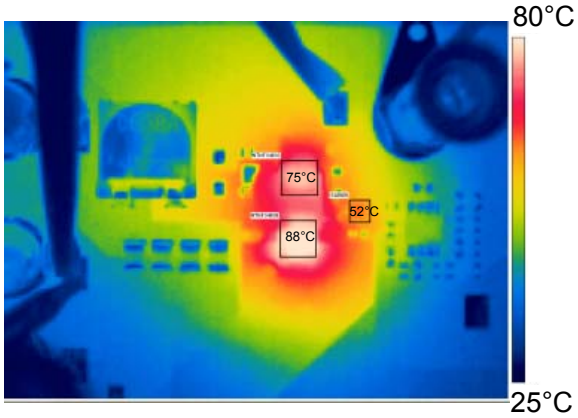
Linear Relationship to Voltage and Charge

Gate Drive Loss = V_{GS} x Freq x Total Q_G

Efficiency Delivering Cooler Systems



NexFET Devices



Industry Standard Devices

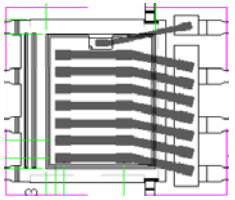
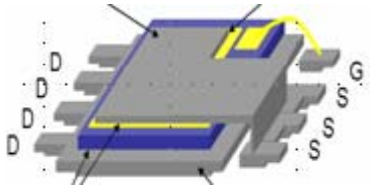
- Up to 30% cooler operation of MOSFET
- Up to 15% cooler driver operation
- Increased Reliability

25A , 500kHz, V_{IN} = 12V, V_{OUT} = 1.3V, V_{GS} = 5V

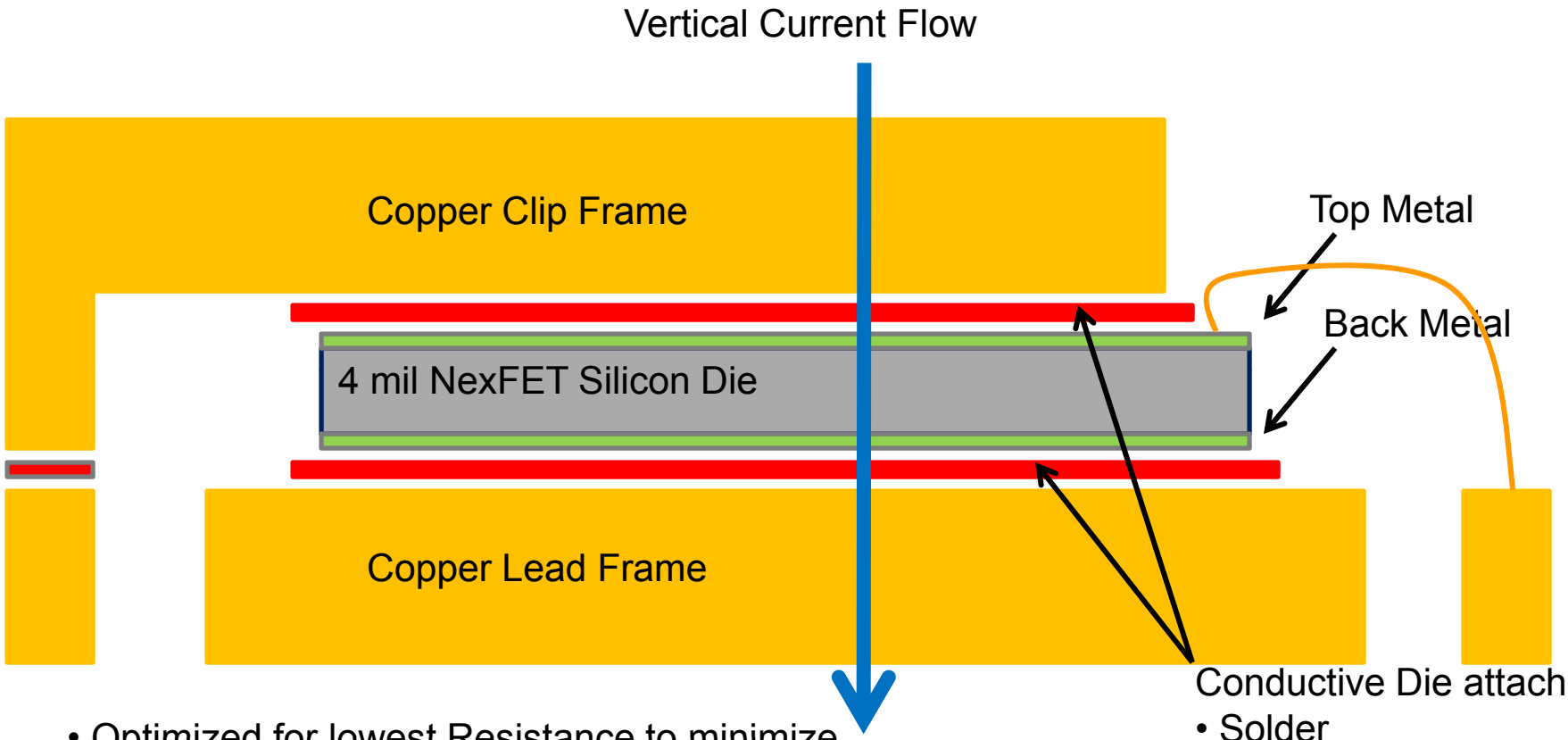
Vgs Summary

- $5V_{GS}$ Systems Delivers Highest Overall Efficiency
- NexFET Devices are Optimized for $5V_{GS}$ Gate Drive Systems
- NexFET Devices Enable Higher System Efficiency or Frequency Running @ $5V_{GS}$ versus @ $12V_{GS}$.
- Gate Drive Losses are Frequently Omitted from Efficiency Measurements.

Current Package Offering

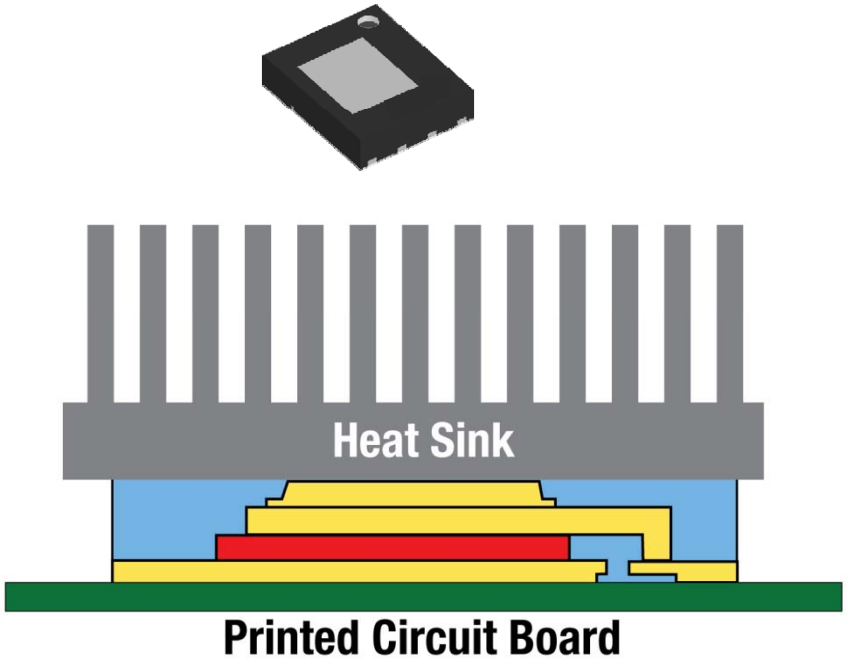
	Q5A Wirebond	Q5 Clip
Construction		
Outline	 5x6	 5x6
Profile	<1mm	<1mm
RoHS Compliant	Yes	Yes
Package Resistance	0.7mΩ	0.3mΩ
Ls	~0.8nH	~0.4nH

Clip Q5 Discrete Power Device

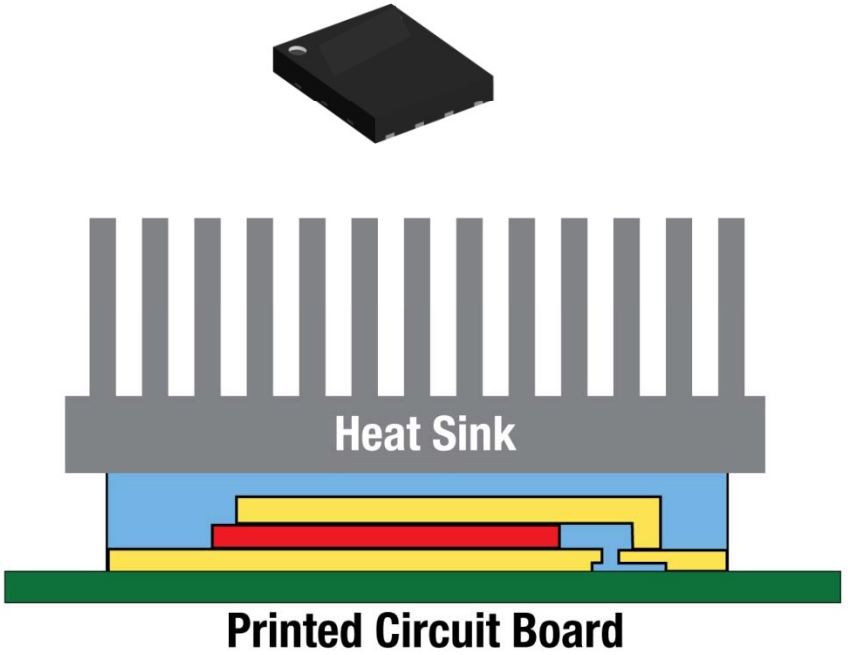


- Optimized for lowest Resistance to minimize package contribution to power loss
- Thermal Engineering critical for reliability
- Production Status

Package comparison highlights top-side cooling capability

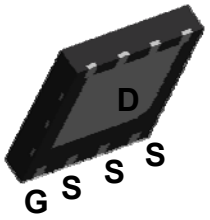


DualCool ™ NexFET™ cross-section view with exposed clip



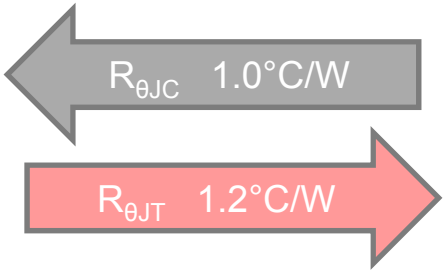
Standard QFN package with non-exposed copper clip

Next Gen: DualCool™ QFN



Exposed DRAIN Pad

Bottom View



Exposed Source Heat Sink

Top View

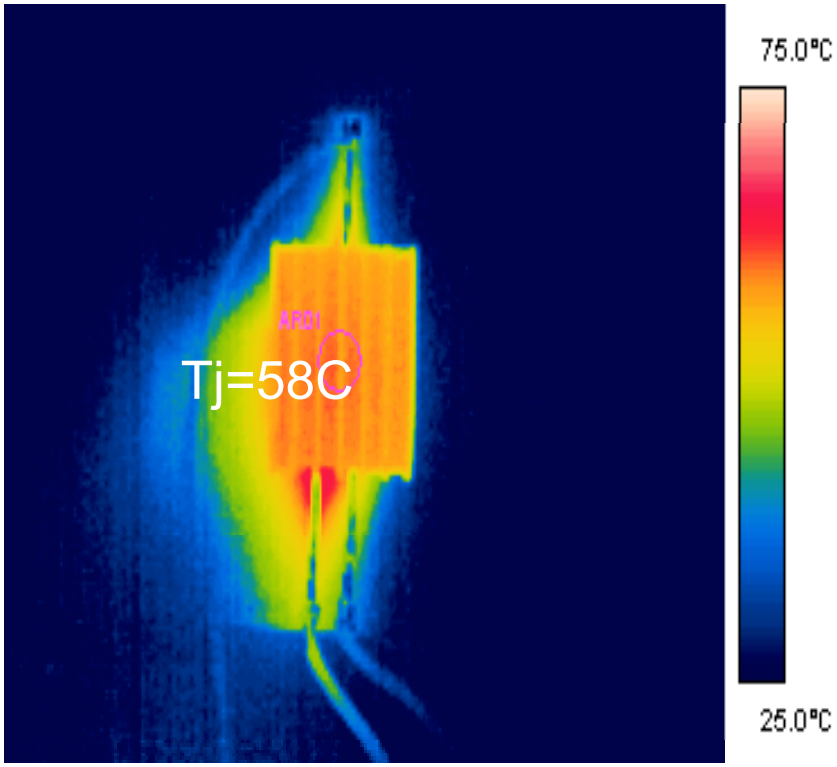
Part No	Size	V_{DS}	V_{GS}	R @ 10V	R@ 4.5V	Qg	Qgd	Sample	Prod
CSD16407Q5C	5x6	25V	16V	1.8mΩ	2.5mΩ	13.3nC	3.5nC	Now	Now
CSD16408Q5C	5x6	25V	16V	3.7mΩ	5.4mΩ	6.5nC	1.9nC	Now	Now
CSD16325Q5C	5x6	25V	10V	-	1.7mΩ	18nC	2.9nC	Now	Now
CSD16321Q5C	5x6	25V	10V	-	2.1mΩ	14nC	2.5nC	Now	Now
CSD16322Q5C	5x6	25V	10V	-	4.5mΩ	6.5nC	1.2nC	Now	Now
CSD16323Q3C	3x3	25V	10V	-	4.4mΩ	6.2nC	1.1nC	Now	Now

Excellent thermal capability through top and bottom of package
Up to 50% Higher Current Capability

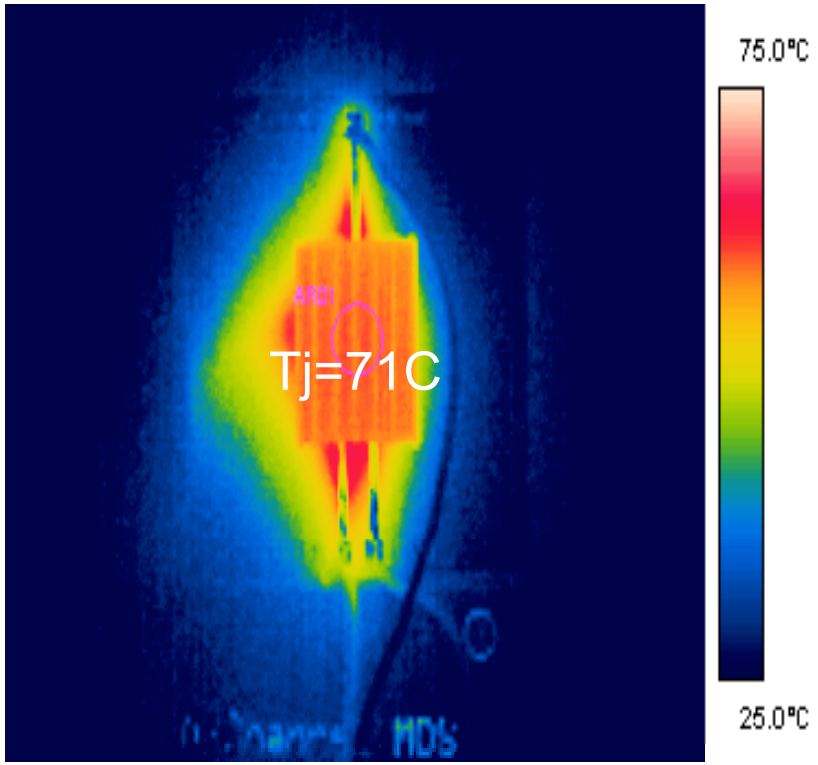
Thermal comparison under actual operating conditions (CSD16321Q5C)

(P_D = 2.1W, Air Flow = 300LFM)

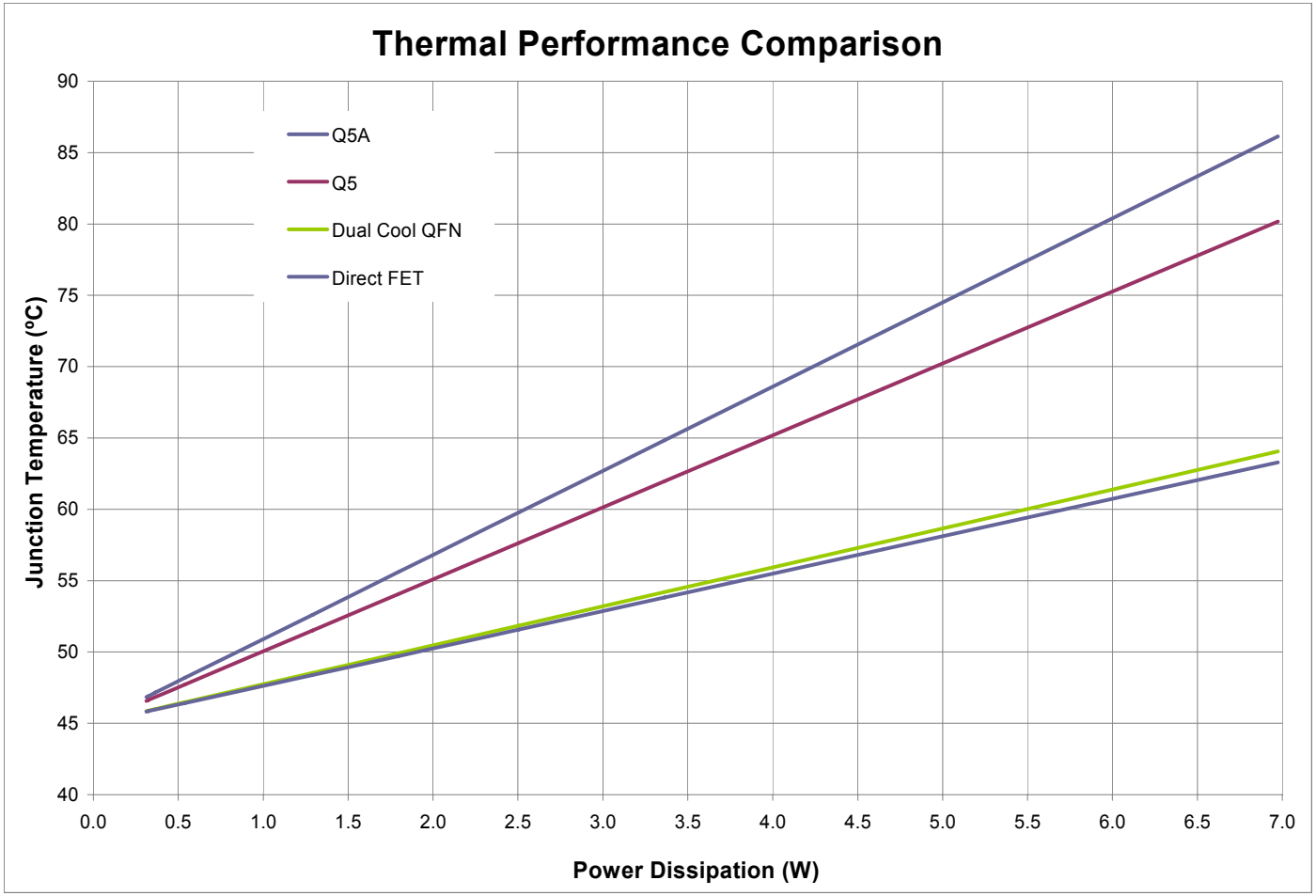
DualCool™ NexFET™



Std package



Excellent Thermal Capability



Same Thermal Performance as DirectFET package

DualCool™ NexFET Summary

- Industry Leading Electrical Performance Now Coupled with Industry Leading Discrete Thermal Performance
- Up to 50% Increase in Current Capability in a standard SON5x6 Footprint
- Up to 50% Reduced Footprint Delivering Increased Power Density
  - Lower Phase Count
  - Less MOSFETs per phase – no need to parallel FETs
  - 2 SON5x6 MOSFETs Replaced by 1
- Ability to Upgrade Existing SON5x6 Designs as Current Requirements Increase without a PCB Change
- Better Thermal Management of the end System as can control amount of Power Dissipated into the PCB with Dual Sided Cooling

NexFET™ MOSFET Ringing

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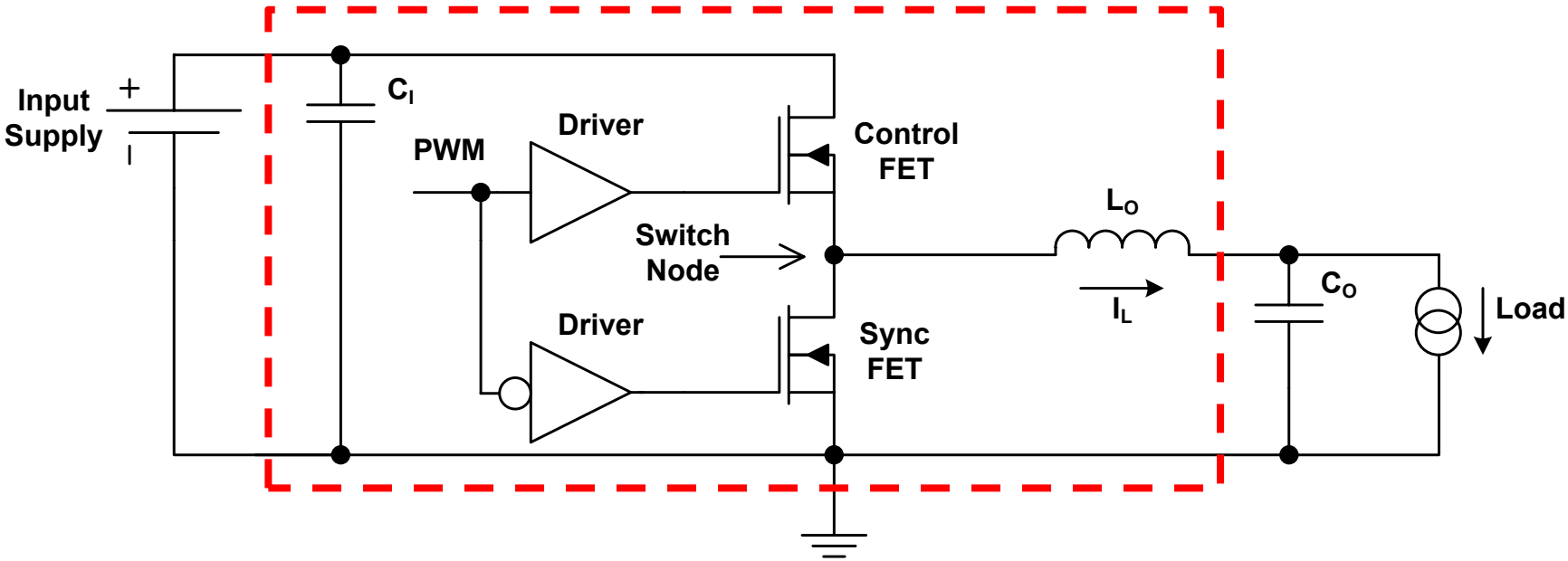
PCB Layout Techniques

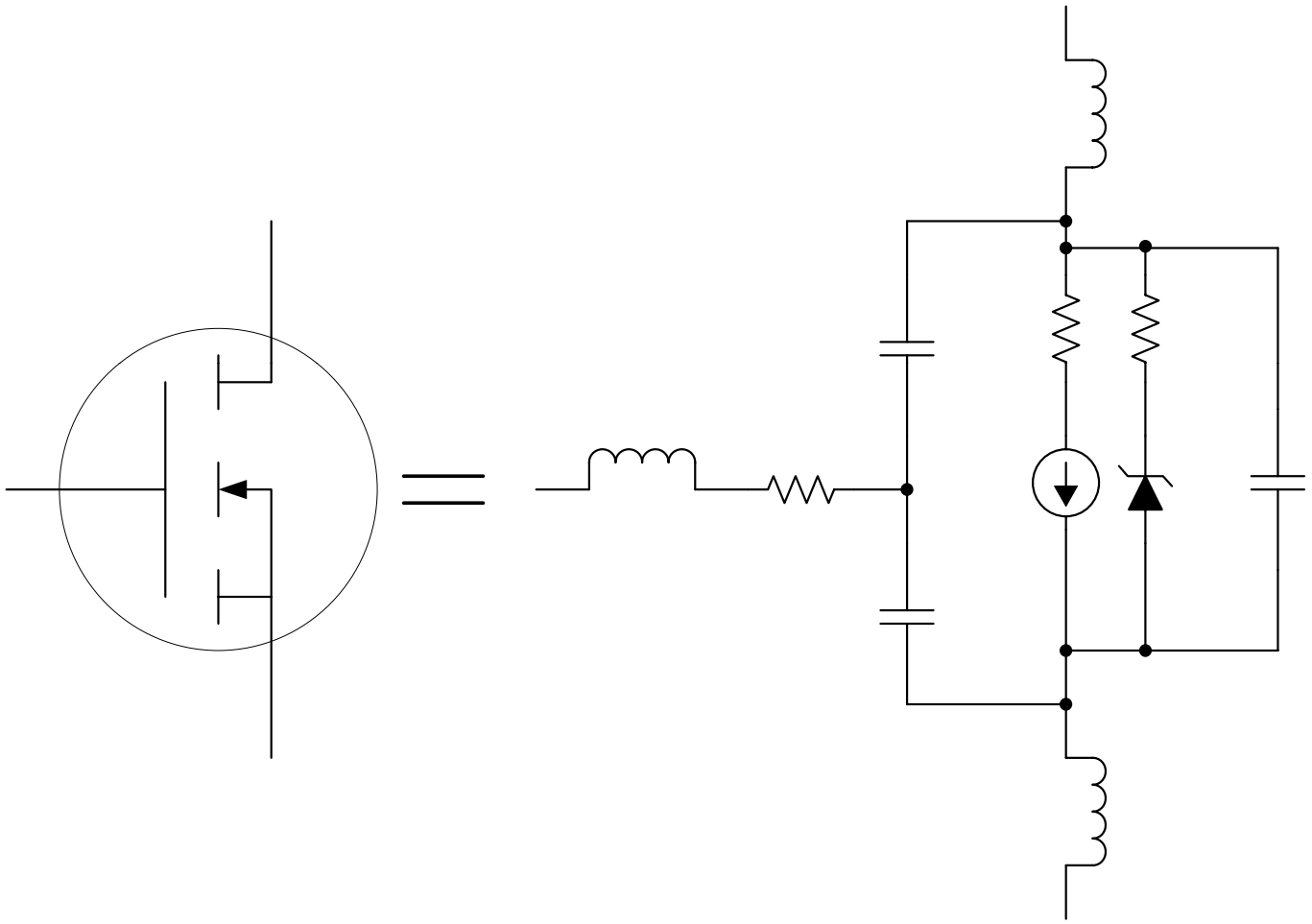


Why Does the Switch Node Ring?

- Simple Answer:
  - Parasitics form L-C tank with very low resistance.
  - L-C Tanks resonate when exposed to a step change.
  - Switch Node is exposed to a step change at Turn_ON and Turn_OFF

The Devil is in the Details

MOSFET Parasitics

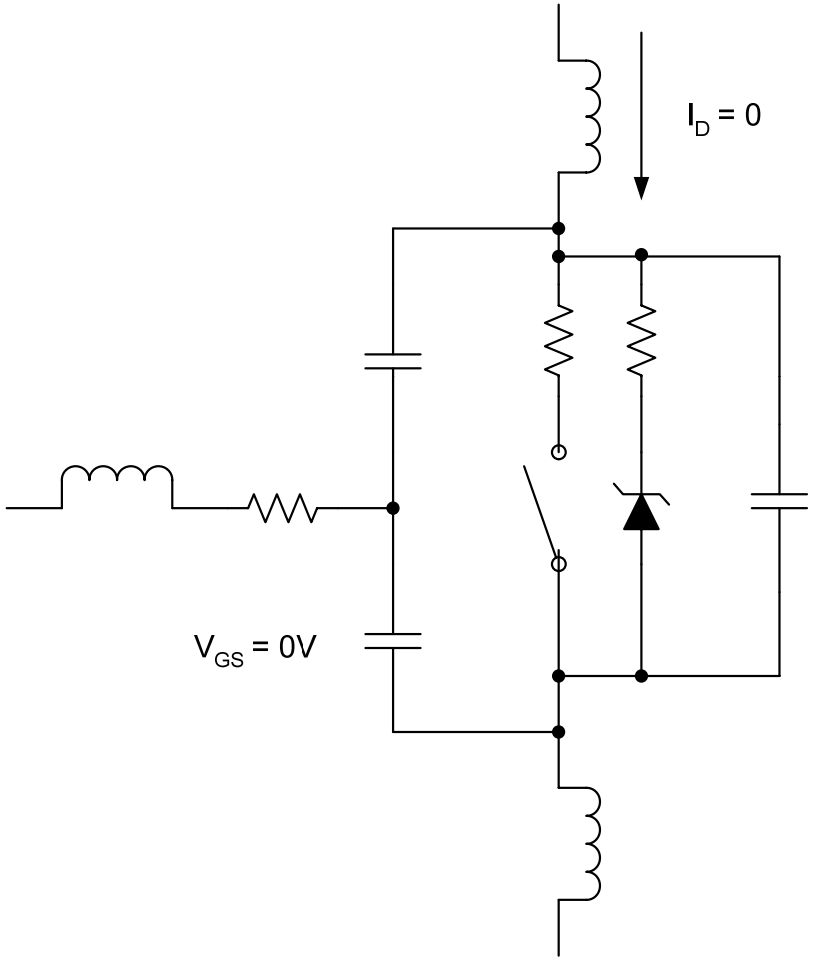


Schematic Symbol

Parasitic Model

When the MOSFET is “OFF”

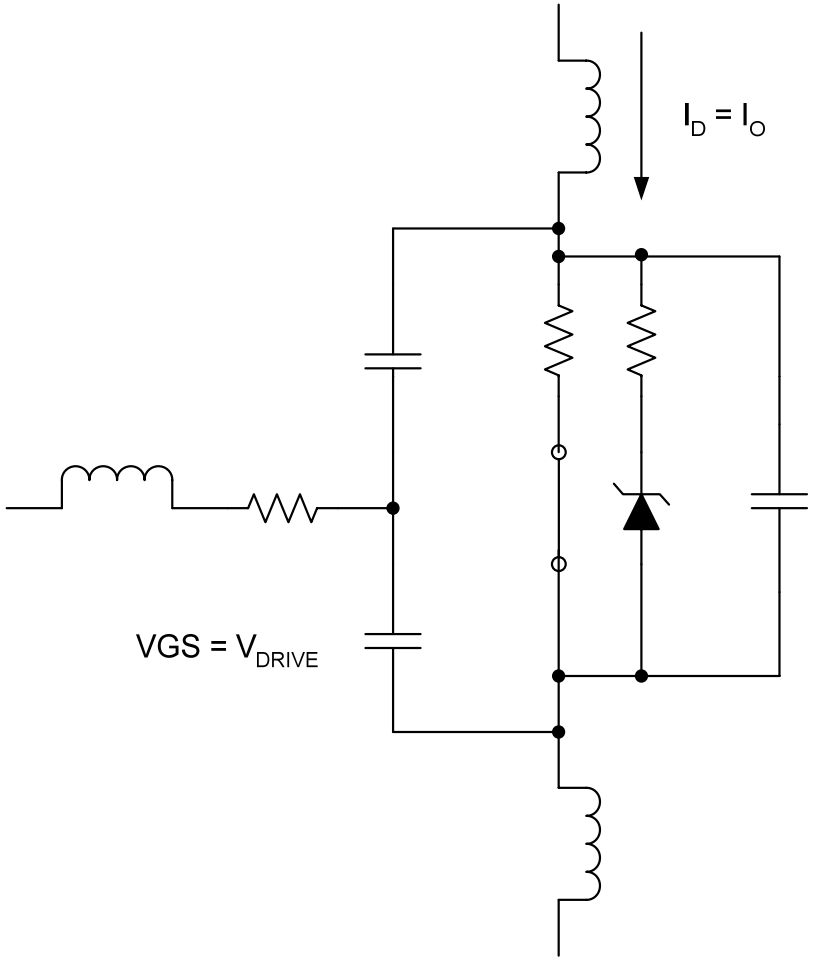
- Drain Current = 0A
- Gate Voltage = 0V
- Parasitics
  - Capacitor from Drain to Source
  - Zener Diode Source to Drain
  - Lead/Trace Inductors
  - Gate Resistance



MOSFET OFF

When the MOSFET is “ON”

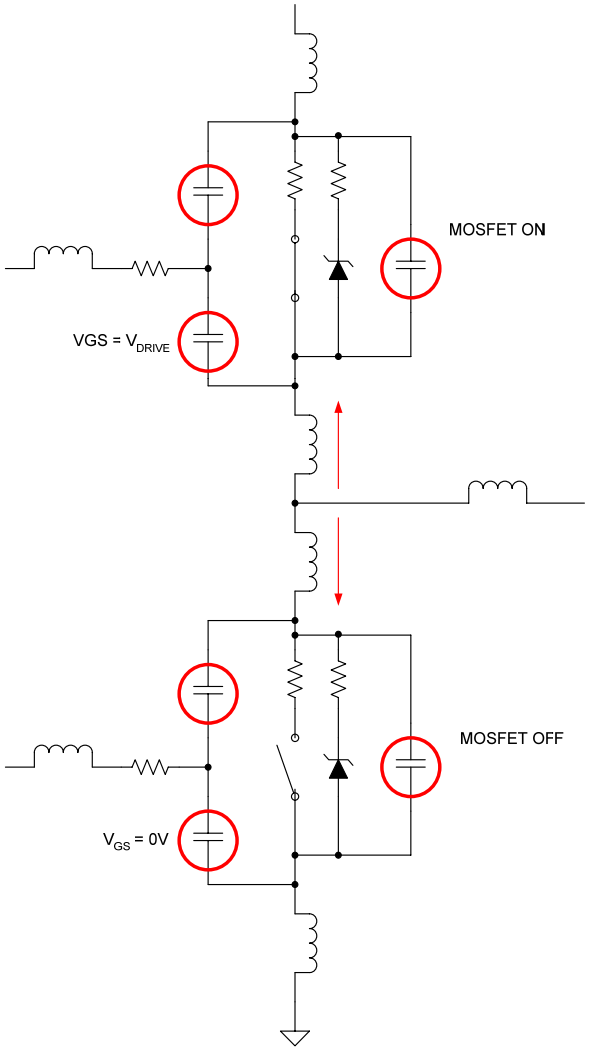
- Drain Carrying Full Current
- Gate Voltage at Drive Voltage
- Parasitics:
  - Drain-Source Capacitor & Zener Diode shorted by Rdson Resistor
  - Lead/Trace Inductance



MOSFET ON

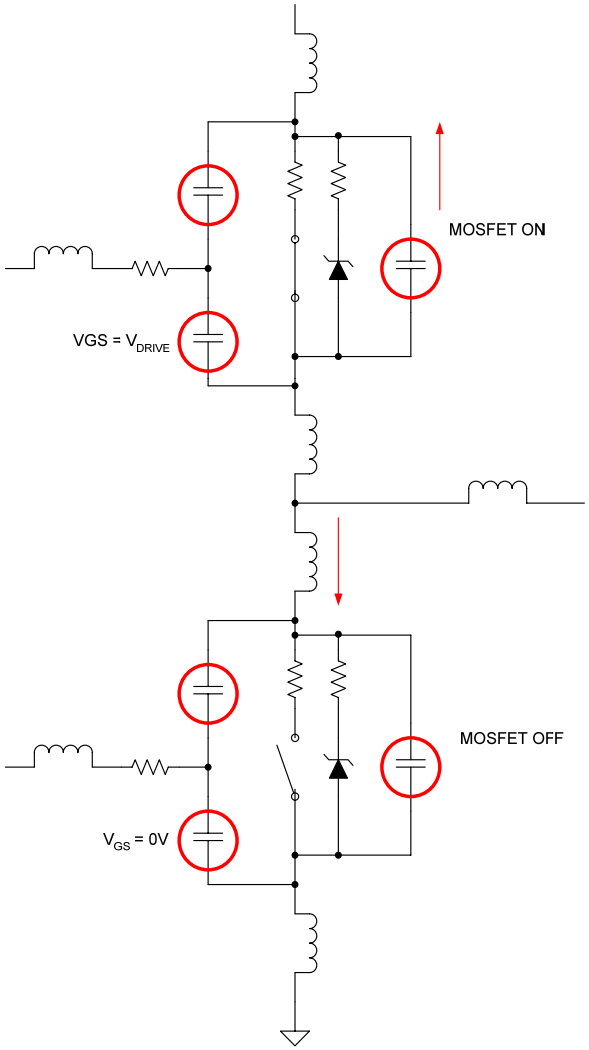
What Happens when we turn “ON”

- High-Side turns “ON”
- Charge Parasitic Capacitance through Inductors
- When:
  - V_L = 0V $I_L \neq$ 0A
  - E = ½ I_L^2 x L
  - Need negative voltage to deflux inductance.



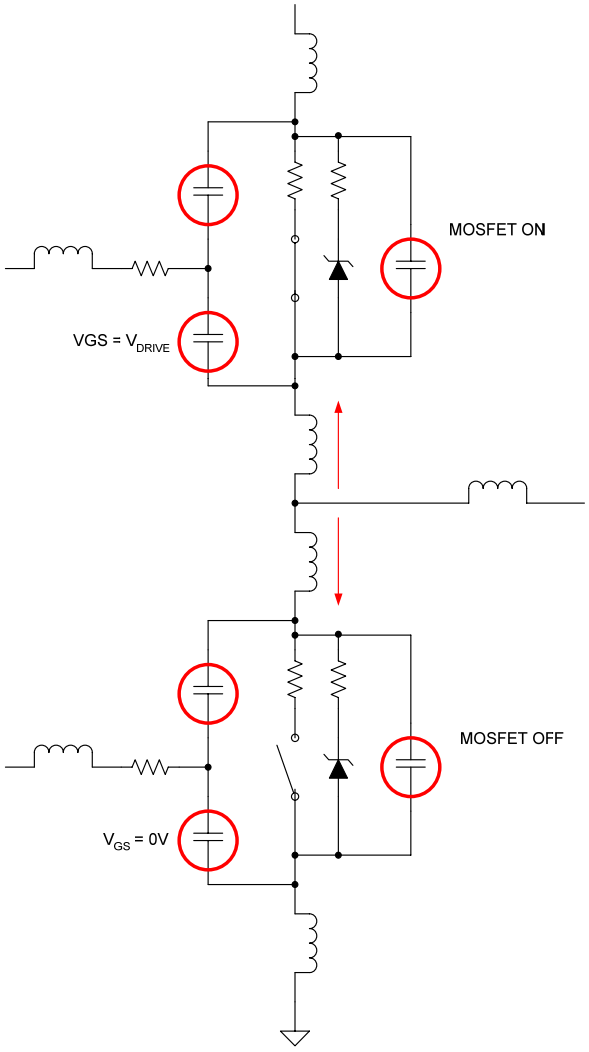
Where Does the Energy Go?

- Current in High-Side
  - Current Reduces V_{DS} of HS FET.
  - Increases V_{SW}
- Current in Low-Side
  - Current Increases V_{DS} of LS FET
  - Increases V_{SW}
- Switch Node Voltage rises above V_{IN}



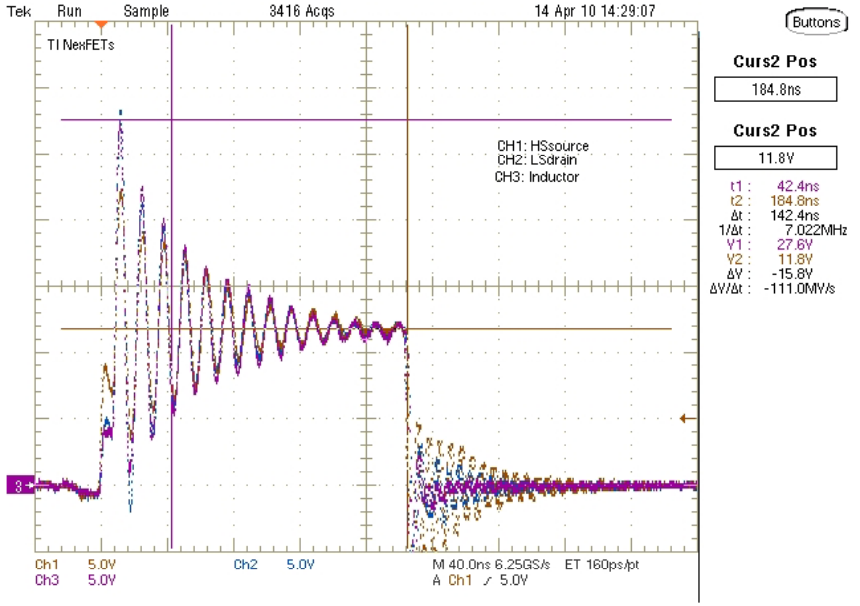
Energy Stored in Capacitors!

- When:
  - I_L = 0A $V_C \neq 0V$
  - $E = ½ V_C^2 \times C$
  - Need negative current to discharge capacitance.
- Process repeats until energy dissipates.



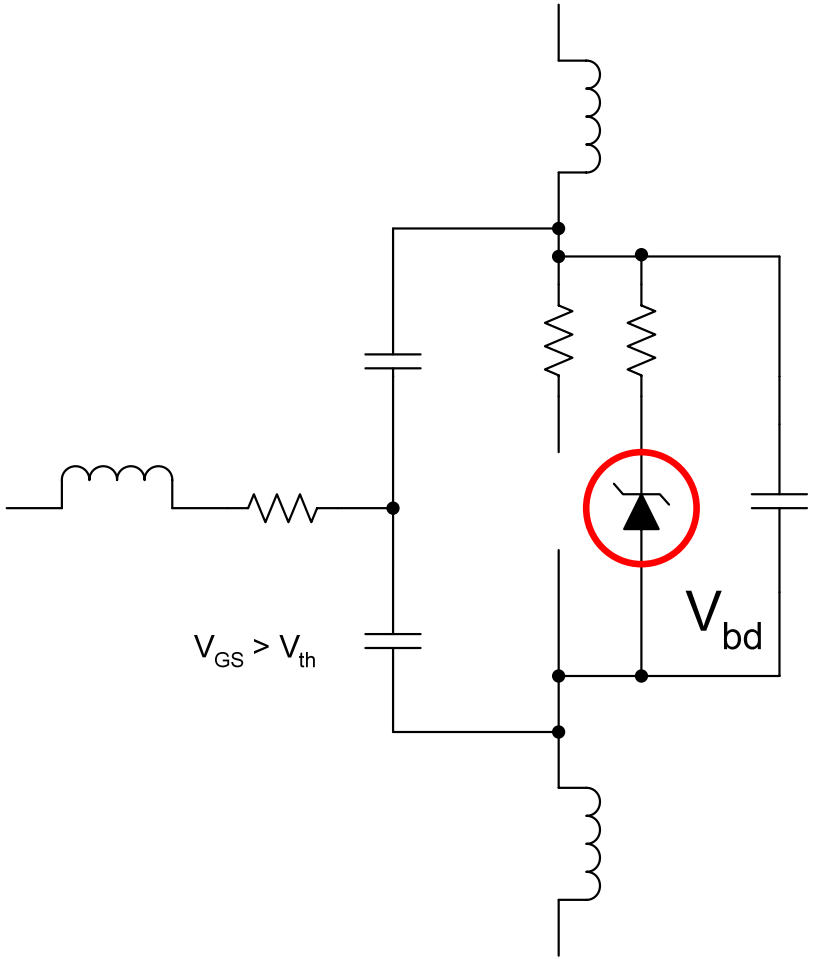
12V to 1.2V @ 20A 600kHz

- 12V Input Voltage
- Rboot = 2W
- Csnub = Open
- Base Layout
  - 27.6V peak rining
  - > 184ns Ring Out
  - 65MHz Frequency



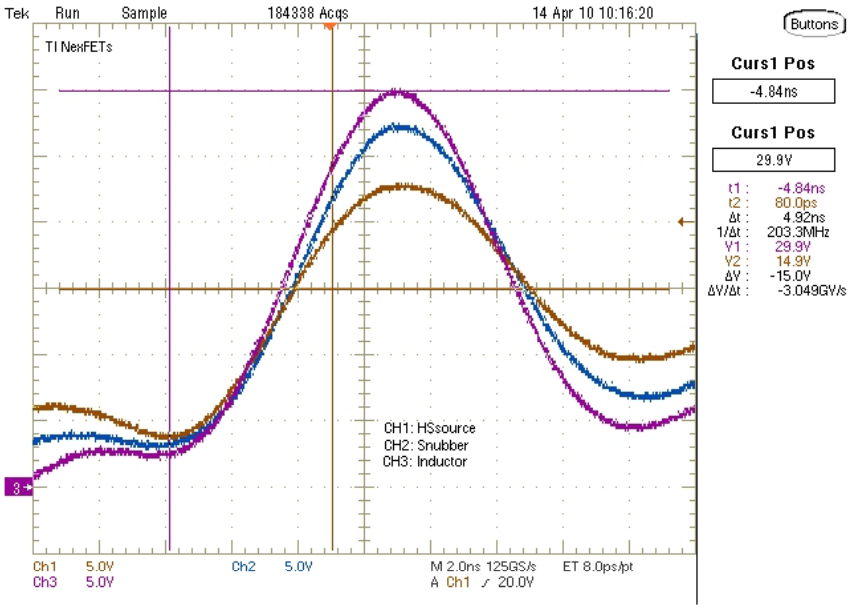
Is Ringing Bad?

- EMI
  - Ringing Adds EMI
    - 50-250MHz
    - Radiated Emissions
    - Near Field
- MOSFET Damage?
  - Avalanche Break-Down
  - Avalanche Rating
    - NexFETs ALL Rated
  - ½ ($V_{PK}^2 - V_{bd}^2$) x C
    - ½ 900V^2-625V^2 x 1nF = 137nJ
    - Lowest Rating:
      - CSD16311Q3 = 11mJ
      - About 0.06%
- Reduced Efficiency
  - 137mW @ 1MHz



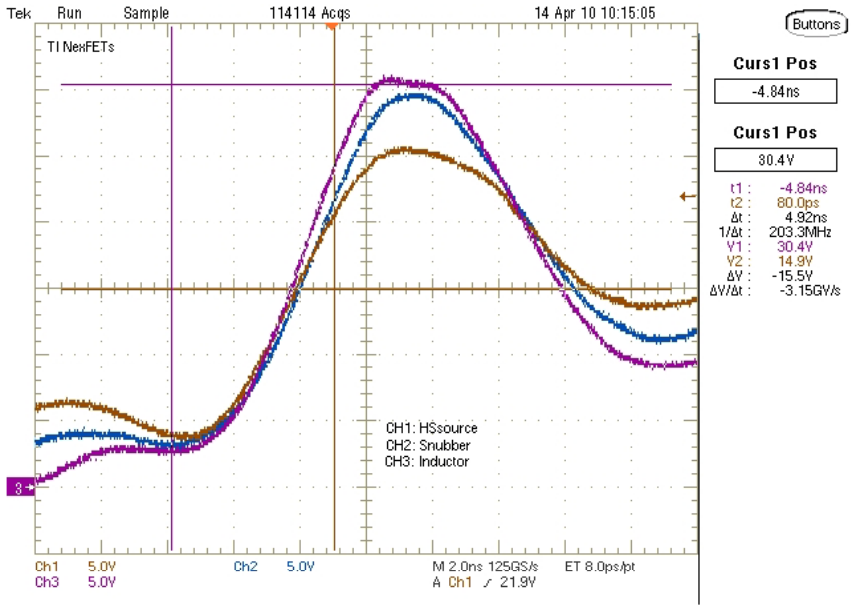
Ring Damage?

Can MOSFET Clamp in 2ns?



V_{IN} = 15V

$V_{SW(peak)}$ = 29.9V



V_{IN} = 18V

$V_{SW(peak)}$ = 30.4V

How High? The Math

- Current in Inductance
  - Rate of charge of C_{SW}
  - When $V_{SW} = V_{IN}$
- Energy Transfers to Capacitor
  - Peak Voltage when $I_{IND} = 0A$
- Assume No Loss
  - $P_{IND} = P_{CAP}$
- What can we learn?
  - Faster Switching = More Ringing
  - Reduce Inductance
  - Reduce Capacitance

$$P_{IND} = \frac{1}{2} L \cdot I^2$$

$$I = C \cdot \frac{dV}{dt}$$

$$P_{IND} = \frac{1}{2} L \cdot \left(C \cdot \frac{dV}{dt}\right)^2$$

$$P_{CAP} = \frac{1}{2} C \cdot V^2$$

$$P_{CAP} = P_{IND}$$

$$\frac{1}{2} C \cdot V^2 = \frac{1}{2} \left(C \cdot \frac{dV}{dt}\right)^2$$

$$V^2 = \frac{L}{C} \cdot \left(C \cdot \frac{dV}{dt}\right)^2$$

$$V^2 = \frac{L}{C} \cdot \left(C \cdot \frac{dV}{dt}\right)^2$$

$$V = \sqrt{\frac{L}{C}} \cdot C \cdot \frac{dV}{dt}$$

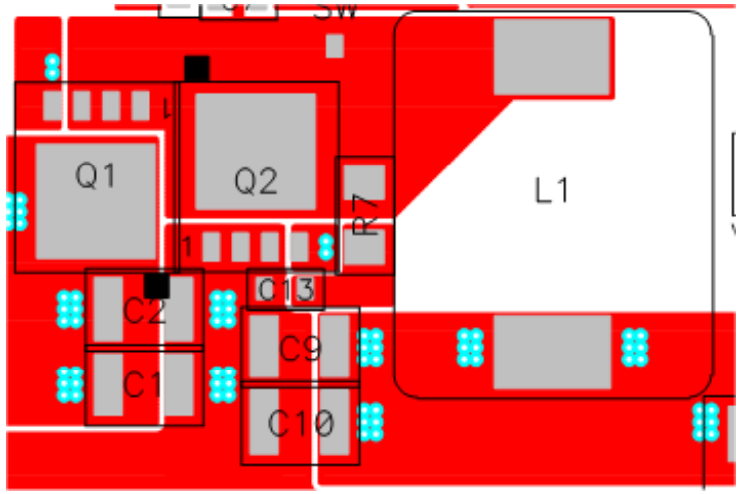
$$V = \sqrt{L \cdot C} \cdot \frac{dV}{dt}$$

How Can We Reduce Ringing?

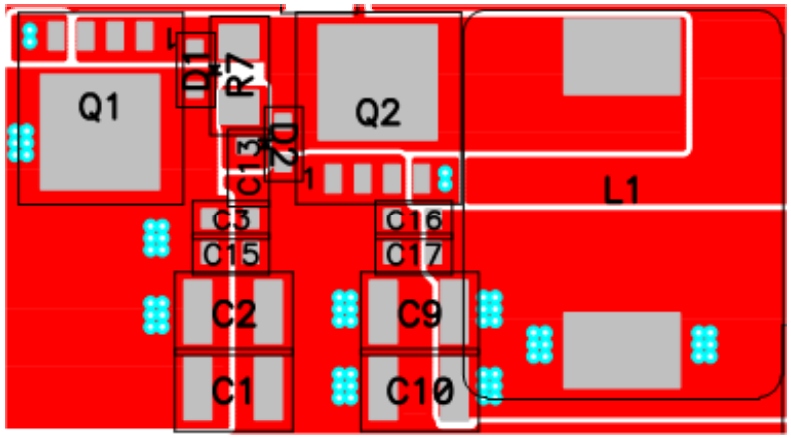
- Layout
  - Reduce Trace Inductance
    - “Common Point” in Switch Node through both FETs and their respective capacitors
      - VIN bypass for High-side
      - VOUT bypass for Low-side
  - Increase Switch to GND capacitance? NO!
    - Reduces Frequency but not Peak
    - Very Low ESR = Longer Ring-out
    - Increases energy! – More Losses
    - Increases High-Frequency GND Noise

Layout Improvements

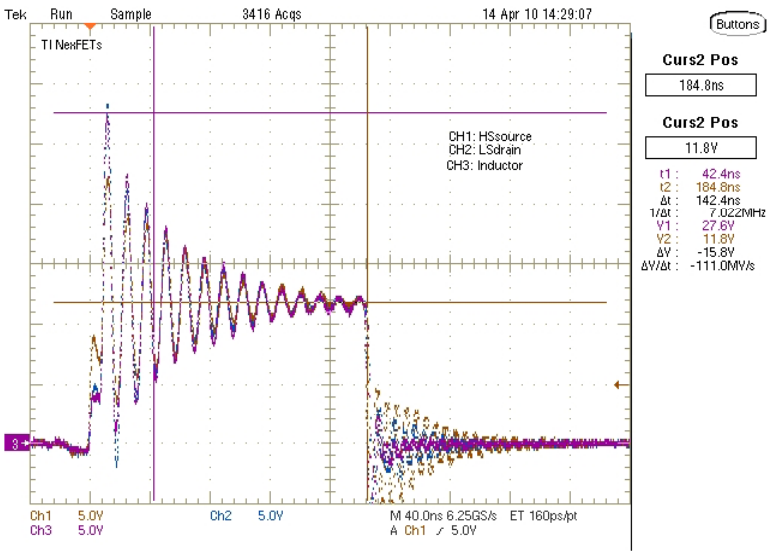
- CSD163CEVM-591
  - Bypass Caps
  - Snubber
  - Tight Snubber Loop
  - V_{IN} & V_{OUT} GND

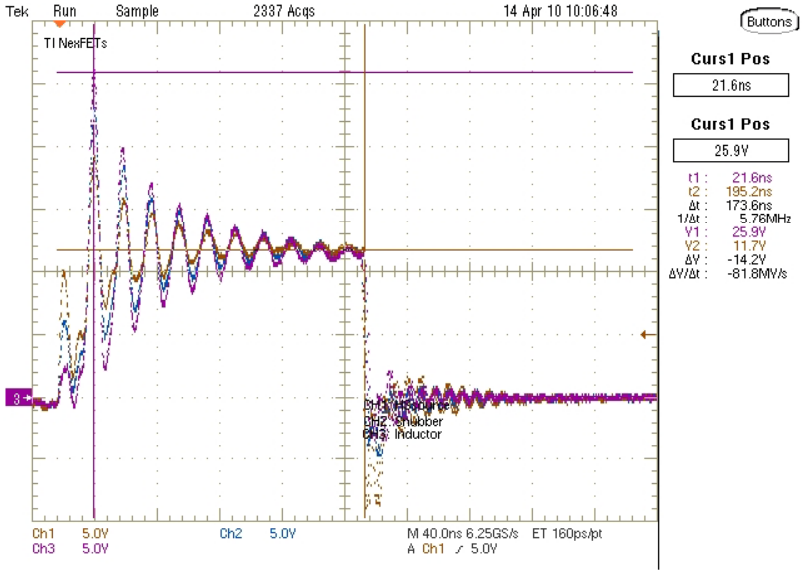


- Improved Layout
  - Snubber between FETs
  - VIN and GND diodes
  - Added 0603 Caps

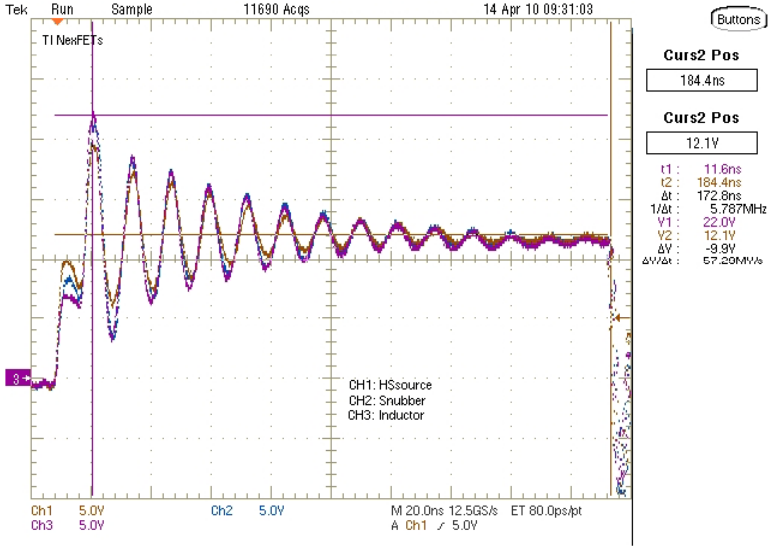


How Effective Is Layout?





10% Reduction!



30% Reduction
Two-sides

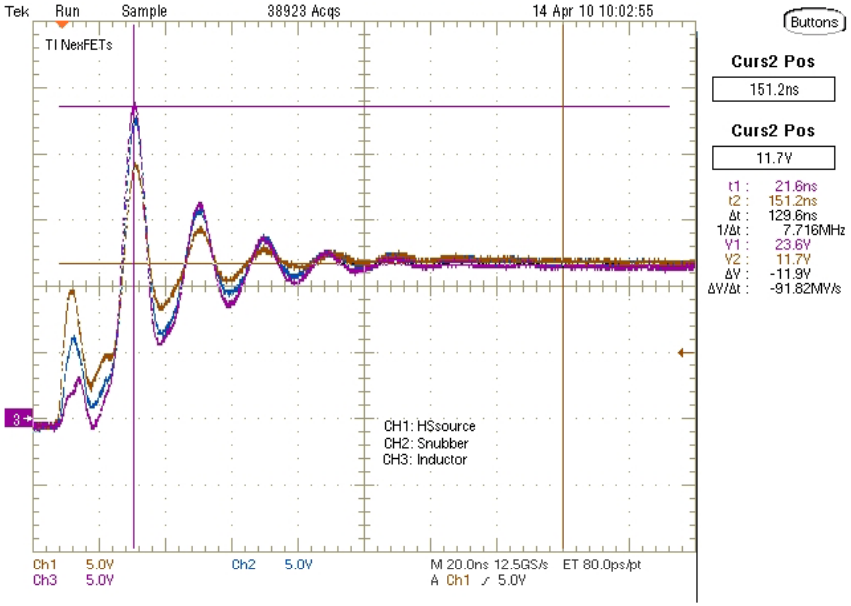
How Can We Reduce Ringing?

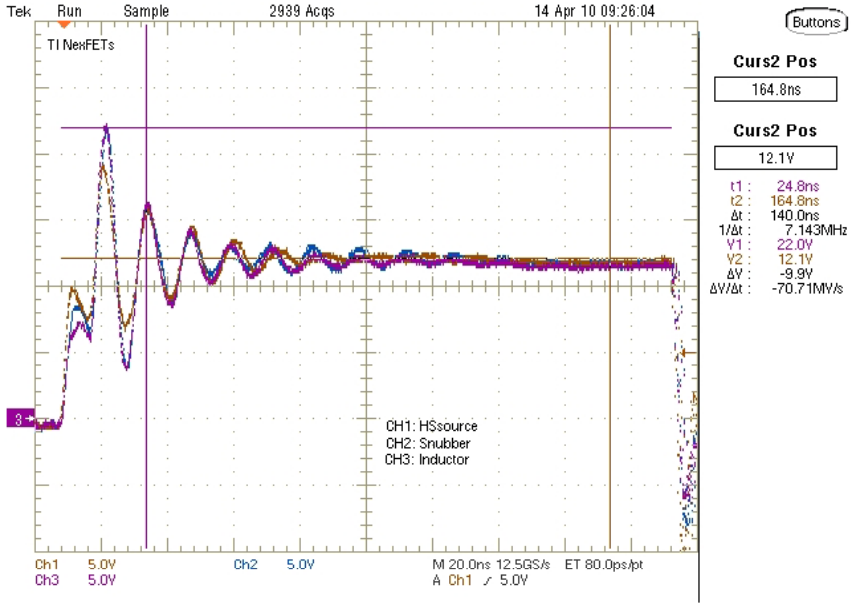
- Slow the Switch Node
  - $I_L = C\ dV/dt$
    - Reduces Energy – Can improve efficiency (to a point)
  - Add Resistors
    - Boot Strap – Only slows Rising Edge
      - Don't Starve Boot Voltage!
      - 1Ω – 3.3Ω typically
    - Gate Drive – Slows both Rising & Falling
      - Can Interfere with dead-time sensing
      - Avoid if possible. 2Ω Max if necessary
    - Switching Node – Slows Falling or Rising & Falling
      - Falling Only if Boot Cap return on IC side of resistor
      - Can also protect IC from negative voltage damage

How Can We Reduce Ringing?

- R-C Snubbers
  - Increase Switch Node Capacitance
    - Reduced Frequency
    - Reduced Peak Voltage
    - Increase ESR for faster ring-out
    - Increased energy dissipation
  - Can Snub to VIN or GND
    - VIN will increase input noise, but recovers some energy.
  - Most Effective when between MOSFETs

Snubbers

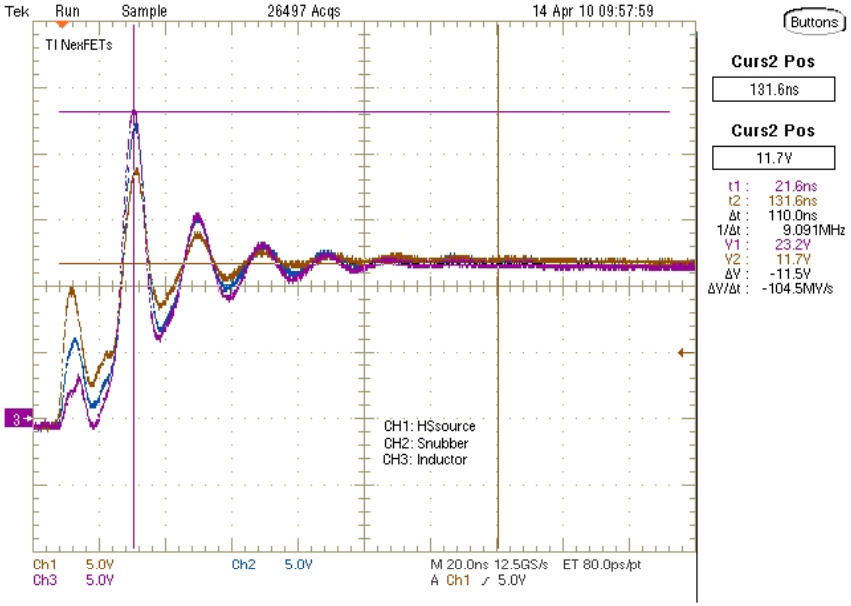

Tek Run Sample 38923 Acqs 14 Apr 10 10:02:55
TI NexFETs
Buttons
Curs2 Pos
151.2ns
Curs2 Pos
11.7V
t1 : 21.6ns
t2 : 151.2ns
Δt : 129.6ns
1/Δt : 7.716MHz
V1 : 23.6V
V2 : 11.7V
ΔV : -11.9V
ΔV/Δt : -91.82MV/s
CH1: HSsource
CH2: Snubber
CH3: Inductor
Ch1 5.0V
Ch3 5.0V
Ch2 5.0V
M 20.0ns 12.5GS/s ET 80.0ps/pt
A Ch1 ⟋ 5.0V

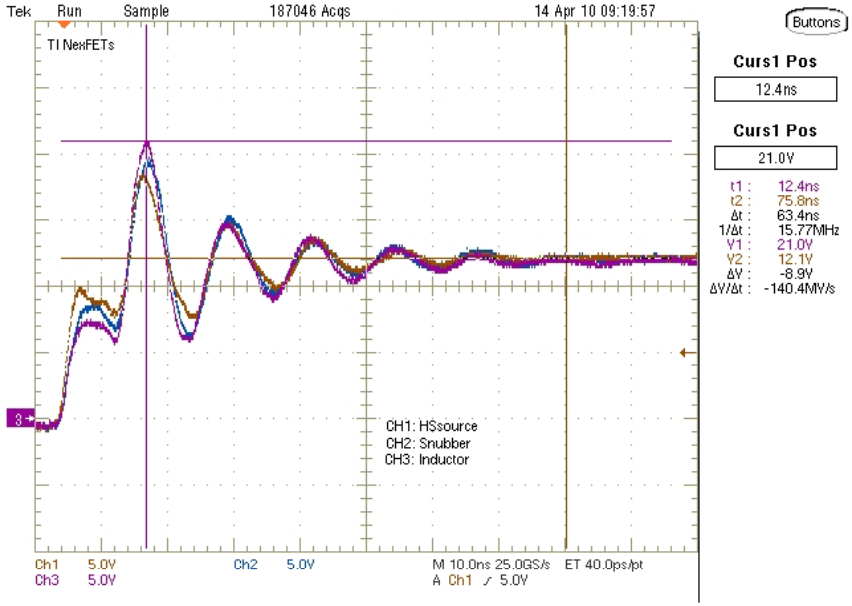

Tek Run Sample 2939 Acqs 14 Apr 10 09:26:04
TI NexFETs
Buttons
Curs2 Pos
164.8ns
Curs2 Pos
12.1V
t1 : 24.8ns
t2 : 164.8ns
Δt : 140.0ns
1/Δt : 7.143MHz
V1 : 22.0V
V2 : 12.1V
ΔV : -9.9V
ΔV/Δt : -70.71MV/s
CH1: HSsource
CH2: Snubber
CH3: Inductor
Ch1 5.0V
Ch3 5.0V
Ch2 5.0V
M 20.0ns 12.5GS/s ET 80.0ps/pt
A Ch1 ⟋ 5.0V

How Can We Reduce Ringing?

- Diode Clamps
  - Very Fast, Small Diodes
    - Adds small capacitance
  - Small loops to small capacitor
    - Needs very low inductance
  - Diode Clamp SW to VIN
    - Little to no impact on Peak
    - Faster ring-out
  - Diode Clamp GND to SW
    - Little to no impact on Negative Peak
    - Faster ring-out

Diodes!


Tek Run Sample 26497 Acqs 14 Apr 10 09:57:59
TI NexFETs
Buttons
Curs2 Pos
131.6ns
Curs2 Pos
11.7V
t1 : 21.6ns
t2 : 131.6ns
Δt : 110.0ns
1/Δt : 9.091MHz
V1 : 23.2V
V2 : 11.7V
ΔV : -11.5V
ΔV/Δt : -104.5MV/s
CH1: HSsource
CH2: Snubber
CH3: Inductor
Ch1 5.0V
Ch3 5.0V
Ch2 5.0V
M 20.0ns 12.5GS/s ET 80.0ps/pt
A Ch1 ⟋ 5.0V


Tek Run Sample 187046 Acqs 14 Apr 10 09:19:57
TI NexFETs
Buttons
Curs1 Pos
12.4ns
Curs1 Pos
21.0V
t1 : 12.4ns
t2 : 75.8ns
Δt : 63.4ns
1/Δt : 15.77MHz
V1 : 21.0V
V2 : 12.1V
ΔV : -8.9V
ΔV/Δt : -140.4MV/s
CH1: HSsource
CH2: Snubber
CH3: Inductor
Ch1 5.0V
Ch3 5.0V
Ch2 5.0V
M 10.0ns 25.0GS/s ET 40.0ps/pt
A Ch1 ⟋ 5.0V

Conclusions

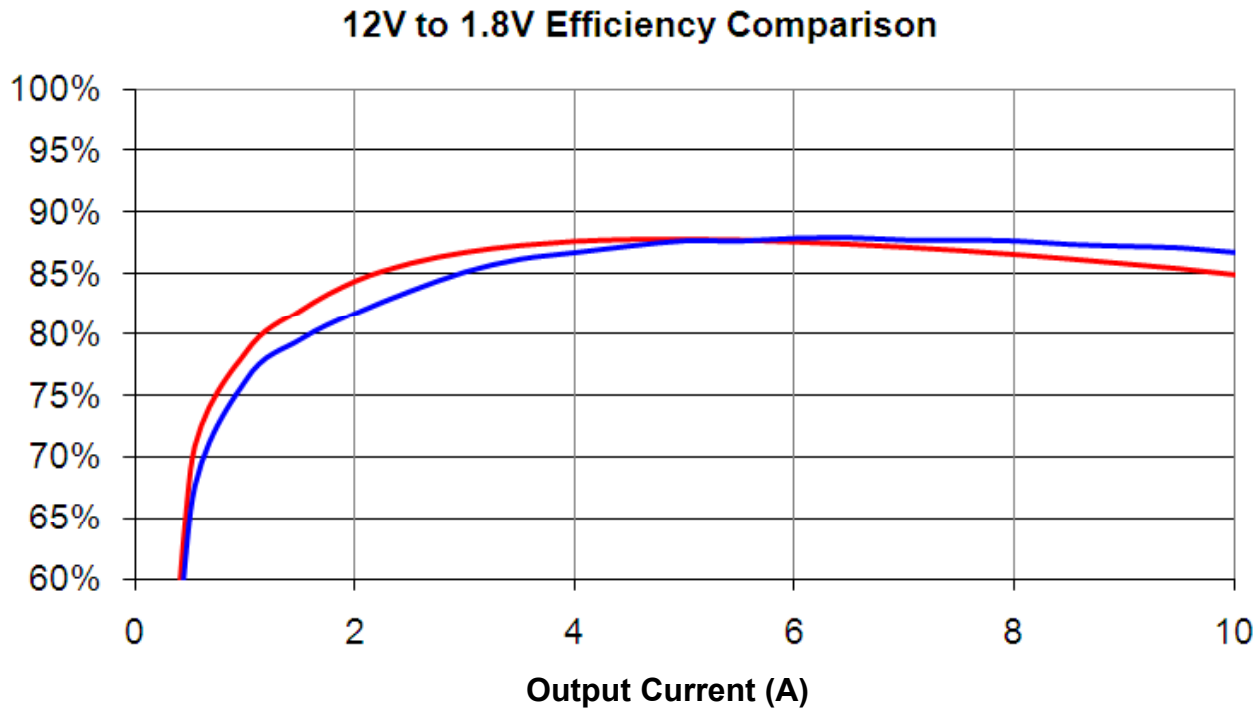
- MOSFET & Board Parasitics Ring
  - Ringing will Generate EMI
  - Ringing is not a MOSFET Failure concern
    - Ringing could contribute to failure of other devices.
- Ringing Can be Reduced
  - Layout, Layout, Layout – Inductive Loops
  - Small, High Frequency Bypass Caps
  - Boot Strap Resistors
  - Snubbers
  - Clamping Diodes

Solutions & Summary

Texas Instruments

Twice the Frequency with Similar Efficiency!

Versus Previous Generation Controller and Competitor's MOSFETs



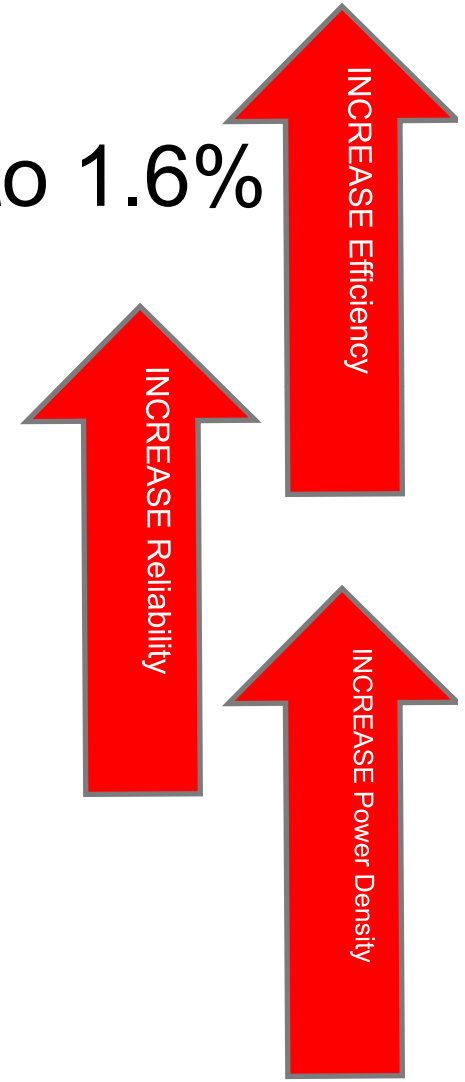
- Blue => TPS40305EVM (1.2MHz) + CSD16410Q5/CSD16322Q5
- Red => TPS40192EVM (600kHz) + Leading Manufacturers MOSFETs

Web-orderable EVMs with NexFETs

- TPS40304EVM-353
  - TPS40304 Controller
  - CSD16410Q5A and CSD16321Q5 NexFETs
  - 12V to 1.2V @ 20A (600kHz)
- CSD163CEVM-591
  - TPS40304 Controller
  - CSD16322Q5C and CSD16325Q5C NexFETs
  - 12V to 1.2V @ 20A (w/ DualCool™ NexFETs)
- TPS40305EVM-488
  - TPS40305 Controller
  - CSD16410Q5A and CSD16322Q5 NexFETs
  - 12V to 1.8V @ 10A (1.2MHz)
- TPS40192EVM-525
  - TPS40192 Controller
  - CSD16410Q5A and CSD16407Q5 NexFETs
  - 12V to 1.8V @ 10A (600kHz)

Lower $R_{DS(ON)}$ & Low Gate Charge Q_{gd} provides:

- Increased Converter Efficiency – up to 1.6%
  - Reduced Gate Drive Power Loss
  - Enables Next Generation “Green” Designs (Energy Star)
  - **Up to 10% Efficiency Increase at light load**
- Increase Reliability
  - **Reduced Temperature – up to 30%**
- Reduced Converter Size & Increased Power Density
  - Up to double the switching frequency
  - **Cut output filter size by 50%**



Current offering…

Stay tuned, there is more to come…

Texas Instruments

N-Channel devices
(small package options)

Part Number	Ch	Vds	Vgs	Typical Rdson (mΩ) @10V	@4.5V	@3V	@2.5V	@1.8V	@1.5V	Qg4.5 Typ.	Qgs Typ.	Qgd Typ.	Rg Typ.	Vth Typ.
WLP1.7x2.3														
Dual														
CSD86311W1723	N	25	10		30.0		35.0			2.8	0.7	0.6		1
SON 2x2														
Single														
CSD16301Q2	N	25	10		23.0	27.0				2.0	0.6	0.4	1.3	1.2
CSD17313Q2	N	30	10		26.0	32.0				1.7	0.5	0.37	1.0	1.2
SON 3x3														
Single														
CSD16411Q3	N	25	16	8.0	12.0					2.9	1.5	0.7	0.8	2
CSD16409Q3	N	25	16	6.2	9.5					4.0	2.1	1	0.9	2
CSD16406Q3	N	25	16	4.2	5.9					5.8	2.5	1.5	1.2	1.8
CSD16323Q3	N	25	10		4.4	5.4				6.2	1.8	1.1	1.4	1.1
CSD16340Q3	N	25	10		4.3		6.1			6.5	2.1	1.2	1.0	0.85
CSD17308Q3	N	30	10		9.2	12.1				3.6	1	0.8	0.6	1.2
CSD17304Q3	N	30	10		6.9	9.3				5.0	1.5	1.1	0.7	1.2
CSD17309Q3	N	30	10		4.8	6.3				7.6	2.3	1.6	1.4	1.2

N-Channel devices
(5x6 SON packages)

Part Number	Ch	Vds	Vgs	Typical Rdson (mΩ) @10V	@4.5V	@3V	@2.5V	@1.8V	@1.5V	Qg4.5 Typ.	Qgs Typ.	Qgd Typ.	Rg Typ.	Vth Typ.
SON 5x6														
Single														
CSD16412Q5A	N	25	16	9.0	13.0					2.9	1.4	0.7	0.7	1.8
CSD16410Q5A	N	25	16	6.8	9.6					3.9	1.8	1.1	0.7	1.9
CSD16404Q5A	N	25	16	4.1	5.7					6.5	3	1.7	0.9	1.8
CSD16408Q5	N	25	16	3.6	5.4					6.7	3.1	1.9	0.8	1.8
CSD16413Q5A	N	25	16	3.1	4.1					9.0	3.5	2.5	0.9	1.6
CSD16403Q5A	N	25	16	2.2	2.9					13.3	5.5	3.5	1.2	1.6
CSD16407Q5	N	25	16	1.8	2.5					13.3	5.3	3.5	1.2	1.6
CSD16414Q5	N	25	16	1.5	2.1					16.6	7.3	4.4	1.4	1.6
CSD16401Q5	N	25	16	1.3	1.8					21.0	8.3	5.2	1.2	1.5
CSD16322Q5	N	25	10		4.6	5.4				6.8	2.4	1.3	1.1	1.1
CSD16321Q5	N	25	10		2.1	2.8				14.0	4	2.5	1.5	1.1
CSD16325Q5	N	25	10		1.7	2.1				18.0	6.6	3.5	1.6	1.1
CSD17307Q5A	N	30	10		9.7	12.8				4.0	1.3	1	0.9	1.3
CSD17302Q5A	N	30	10		7.3	9.5				5.4	1.7	1.2	0.8	1.2
CSD17310Q5A	N	30	10		4.5	5.7				8.9	2.7	2.1	0.9	1.3
CSD17306Q5A	N	30	10		3.3	4.2				11.8	3.5	2.4	1.0	1.1
CSD17305Q5A	N	30	10		2.8	3.9				14.1	4.5	3	1.0	1.1
CSD17301Q5A	N	30	10		2.3	2.9				19.0	5.7	4.3	1.3	1.1
CSD17303Q5	N	30	10		2.0	2.7				18.0	5.6	4	1.4	1.1
CSD17311Q5	N	30	10		1.8	2.3				24.0	6.6	5.2	1.2	1.2
CSD17312Q5	N	30	10		1.4	1.8				28.0	8.4	6	1.1	1.1
Dual Cool 5x6														
Single														
CSD16408Q5C	N	25	16	3.6	5.4					6.7	3.1	1.9	0.8	1.8
CSD16407Q5C	N	25	16	1.8	2.5					13.3	5.3	3.5	1.2	1.6
CSD16322Q5C	N	25	10		4.6	5.4				6.8	2.4	1.3	1.1	1.1
CSD16321Q5C	N	25	10		2.1	2.8				14.0	4	2.5	1.5	1.1
CSD16325Q5C	N	25	10		1.7	2.1				18.0	6.6	3.5	1.6	1.1

P-Channel devices

Part Number	Ch	Vds	Vgs	Typical Rdson (mΩ) @10V	@4.5V	@3V	@2.5V	@1.8V	@1.5V	Qg4.5 Typ.	Qgs Typ.	Qgd Typ.	Rg Typ.	Vth Typ.
WLP 1x1														
Single														
CSD23201W10	P	12	6		66.0		77.0		110.0	1.9	0.28	0.26		0.6
WLP 1x1.5														
Single														
CSD25301W1015	P	20	8		62.0		80.0		175.0	1.9	0.45	0.4		0.75
Common Source														
CSD75301W1015	P	20	8		80.0		105.0	150.0		1.5	0.28	0.3		0.7
CSD75205W1015	P	20	6		72.0		94.0	130.0		1.7	0.3	0.4	30.0	0.7
WLP1.5x1.5														
Single														
CSD25201W15	P	20			33.0		42.0	52.0		4.7	0.8	0.9		0.7
WLP1.5x1.5														
Common Source														
CSD75204W15	P	20	6		50.0		65.0	85.0		2.8	0.5	0.6	30.0	0.7
WLP1.7x2.3														
Dual														
CSD75211W1723	P	20	8		32.0		39.0	50.0		4.8	0.8	1		0.7
SON 2x2														
Single														
CSD25302Q2	P	20	8		39.0		56.0	71.0		2.3	0.45	0.5	0.7	0.7
SON 3x3														
Single														
CSD25401Q3	P	20	12		8.8		13.5			8.8	2.1	2.1	1.2	0.87

Thank You!