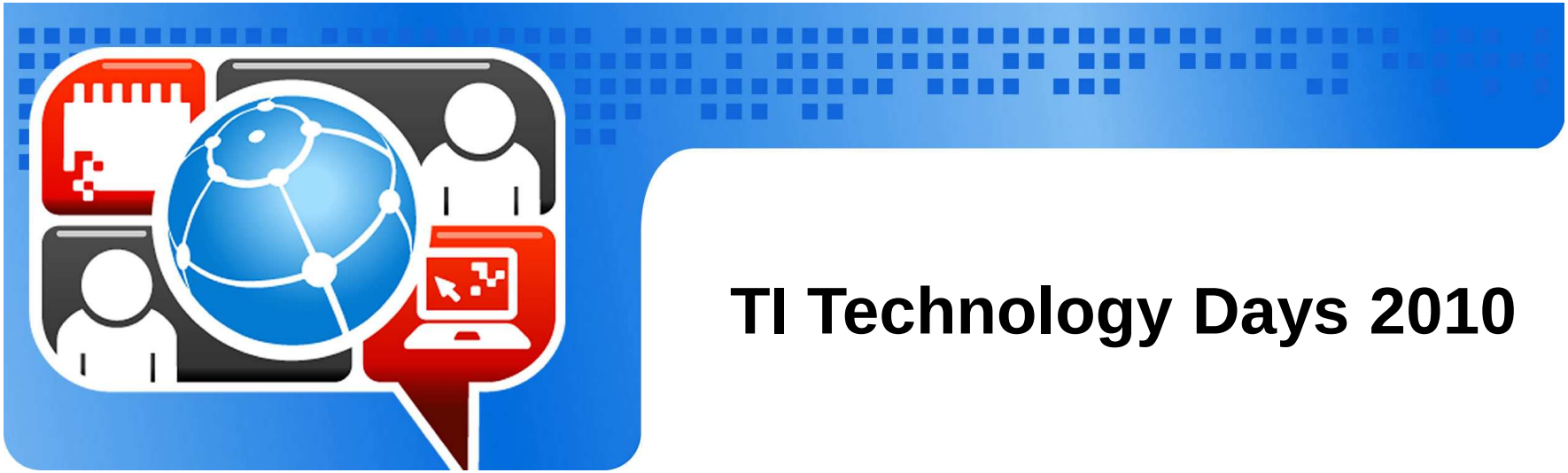


TI Technology Days 2010

Sitara ARM9 and Cortex A8 Processors

Leverage powerful peripherals and low power options

Frank Walzer

Texas Instruments
System Engineer – Industrial Automation Lab

Agenda

- Quick Overview – What is Sitara™?
  - ARM9 based processors (AM1xxx)
  - Cortex A8 based processors (AM35xx and OMAP35xx)
  - Evaluation modules and other boards
- AM18xx differentiating peripherals
  - Internal bus structure
  - UPP – Universal Parallel Port
  - PRU – Programmable Realtime Unit
- Making use of Sitara low power features
  - Comparison AM18xx, AM35xx, OMAP35xx
  - DVFS and Smart Reflex
  - Making use of low power features with Linux

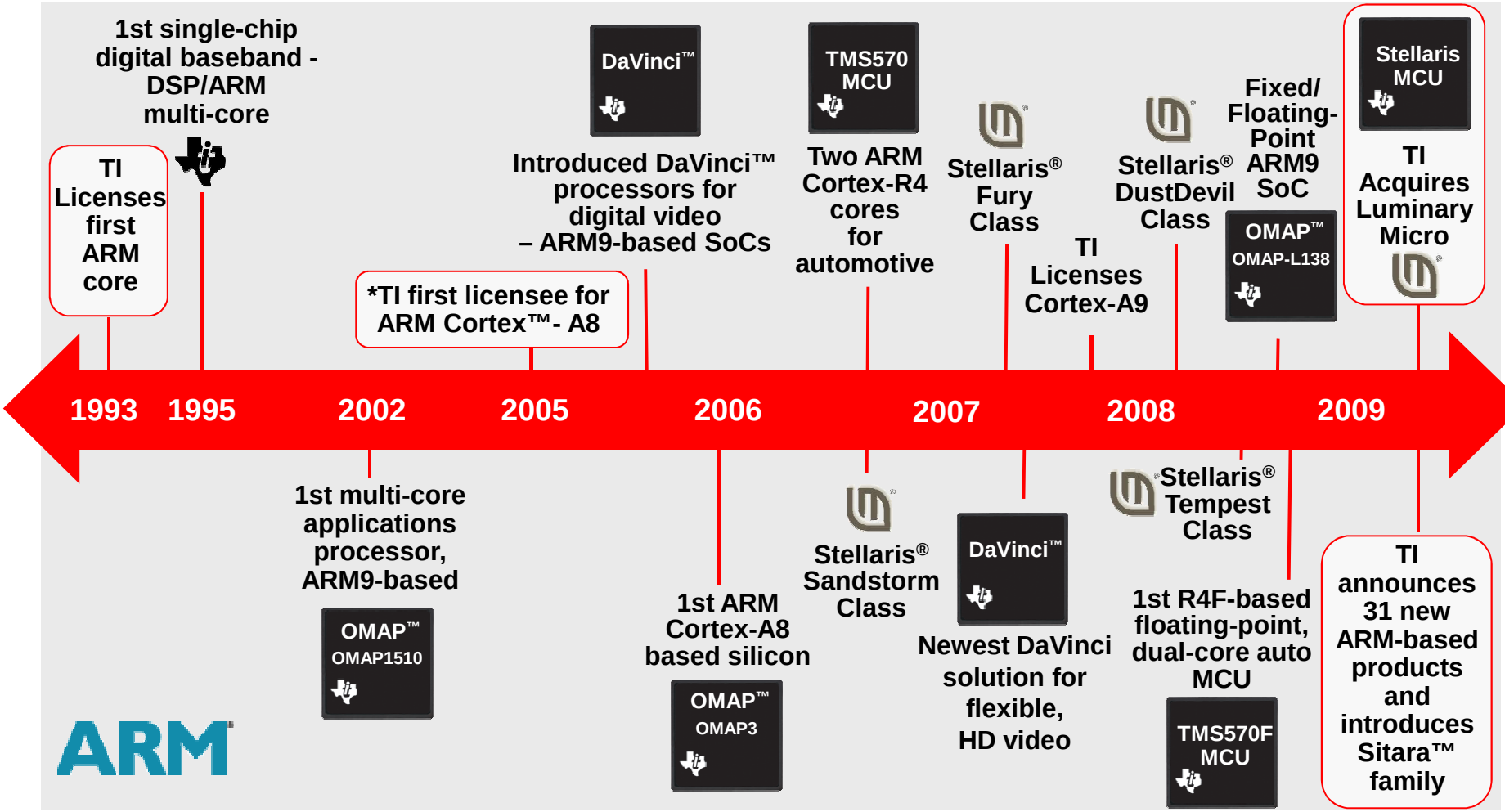
Embedded processing portfolio

TI Embedded Processors

Microcontrollers (MCUs)			ARM®-Based Processors	Digital Signal Processors (DSPs)		
16-bit ultra-low power MCUs	**32-bit real-time MCUs**	**32-bit ARM Cortex™-M3 MCUs**	**ARM Cortex-A8 MPUs**	**DSP DSP+ARM**	**Multi-core DSP**	**Ultra Low power DSP**
MSP430™	**C2000™ Delfino™ Piccolo™**	**Stellaris®** ARM® Cortex™-M3	**Sitara™** ARM® Cortex™-A8 & ARM9	**C6000™ DaVinci™** video processors **OMAP™**	**C6000™**	**C5000™**
Up to 25 MHz	40MHz to 300 MHz	Up to 100 MHz	300MHz to >1GHz	300MHz to >1Ghz +Accelerator	24.000 MMACS	Up to 300 MHz +Accelerator
Flash 1 KB to 256 KB	Flash, RAM 16 KB to 512 KB	Flash 8 KB to 256 KB	Cache, RAM, ROM	Cache RAM, ROM	Cache RAM, ROM	Up to 320KB RAM Up to 128KB ROM
Analog I/O, ADC LCD, USB, RF	PWM, ADC, CAN, SPI, I²C	USB, ENET MAC+PHY CAN, ADC, PWM, SPI	USB, CAN, PCIe, EMAC	USB, ENET, PCIe, SATA, SPI	SRIO, EMAC DMA, PCIe	USB, ADC McBSP, SPI, I²C
Measurement, Sensing, General Purpose	Motor Control, Digital Power, Lighting, Ren. Enrgy	Connectivity, Security, Motion Control, HMI, Industrial Automation	Industrial computing, POS & portable data terminals	Floating/Fixed Point Video, Audio, Voice, Security, Conferencing	Telecom test & meas media gateways, base stations	Audio, Voice Medical, Biometrics
$0.25 to $9.00	$1.50 to $20.00	$1.00 to $8.00	$5.00 to $20.00	$5.00 to $200.00	$40 to $200.00	$3.00 to $10.00

Texas Instruments

TI ARM® Investment and Innovation



TI has shipped over 5 billion ARM-based products and continues to invest in a large portfolio of scalable platforms from $1 to >1GHz

* TI licensed in July 2003, but publicly announced Oct 2005.

Sitara™ ARM® microprocessors

Available Now

ARM9™

AM1808
AM1806
AM1707
AM1705

Low Power ARM9 with flexible peripherals

- Power efficient (down to 7mW standby, 182mW active)
- User configurable interfaces through the programmable real-time unit (PRU)
- Integrated peripherals, 10/100 Ethernet, USB, SATA, CAN, UART and many others

ARM Cortex™-A8

AM3715
AM3703
AM3517
AM3505
OMAP3515
OMAP3503

High-performance Cortex-A8 with system integration

- Up to 1GHz (2000 DMIPS)
- Power efficient (down to 12mW standby, 1W active)
- Integrated graphics for rich user interface functions
- Integrated interfaces to display, USB, 10/100 Ethernet, SD card, Wi-Fi®, CAN, and many others

In Development

ARM Cortex-A8

“AM38x Next” (2010)
“AM33x Next” (2011)

Advanced Cortex-A8 with performance and value options

- Greater than 1GHz core performance
- 1080p display support
- Enhanced graphics for superior user interface functions
- Peripheral integration of 1Gb Ethernet, PCIe, and many others

Support for Linux, Windows® Embedded CE, Android, & RTOS

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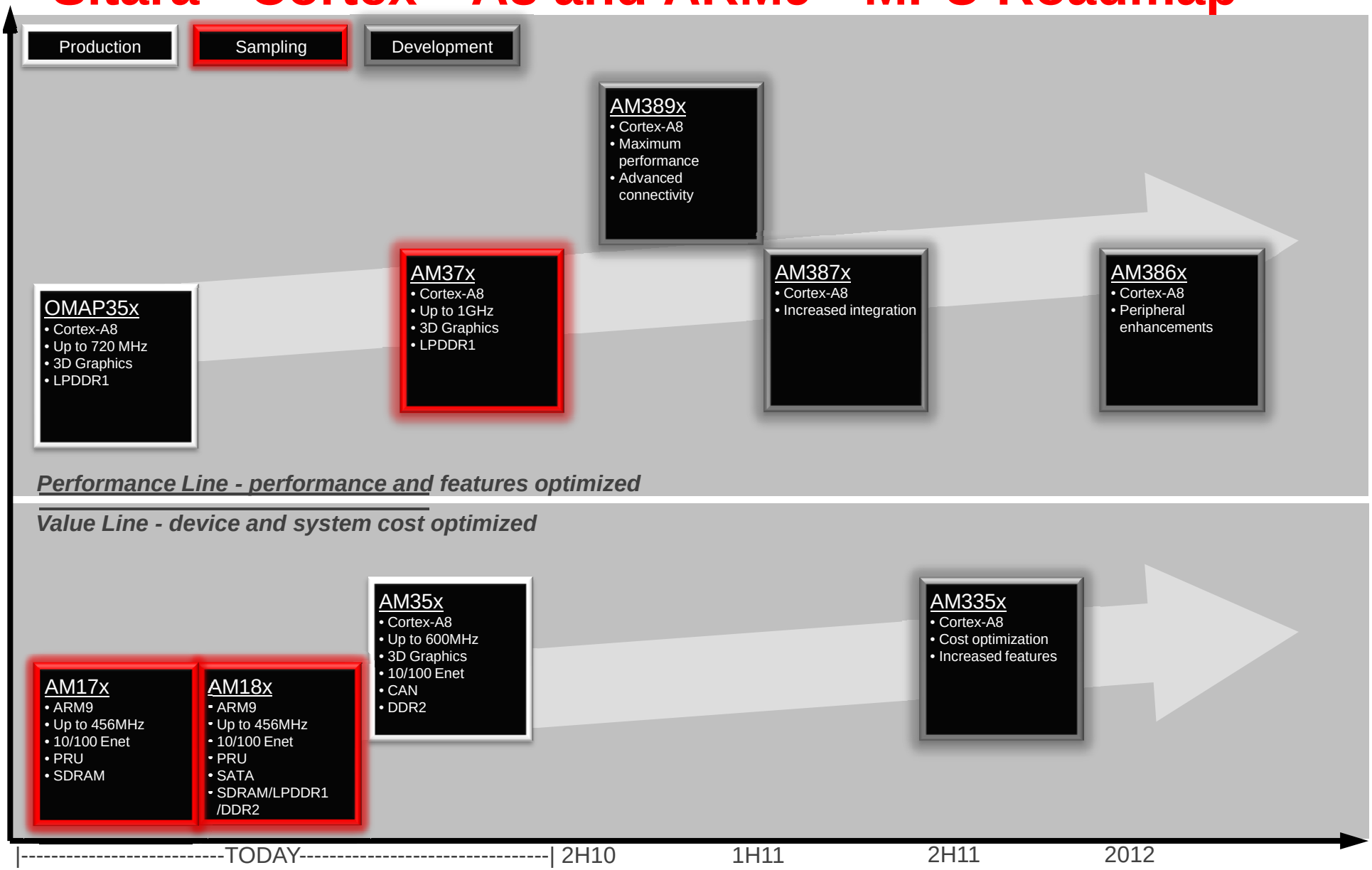
Sitara™ Cortex™-A8 and ARM9™ MPU Roadmap



Speeds shown are for commercial temperature. Dates approximate initial samples. Not all peripherals shown. Limitations apply among package and pin muxing.

Texas Instruments

AM1808/06 Processors

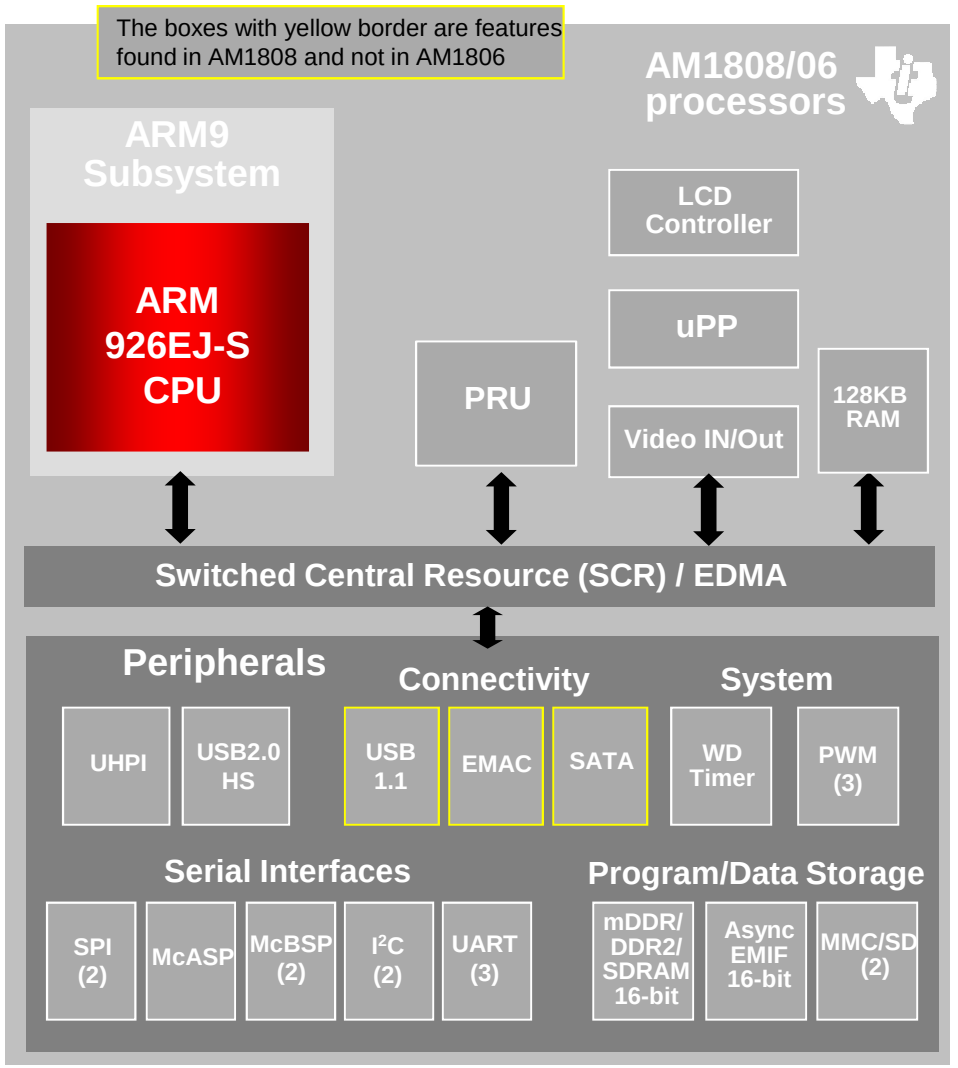
Unmatched Connectivity & Integration for Power-Efficient Processors

Example Applications:

- Industrial Automation
- Home Automation
- Test & Measurement
- Portable Data Terminals

Benefits:

- Multiple connectivity and interface options
- Rich, intuitive user interfaces
- High system integration
- Reduced system cost



AM1808/06 Processors

■CPU Core

−ARM926EJ-S™ (MPU) up to 450 MHz

■Memory

−ARM:
- 16KB – L1 Program Cache
- 16KB – L1 Data Cache

−On-chip
- 128KB RAM

−mDDR, DDR2, SDRAM

■Peripherals (1.8/3.3V IOs)

−10/100 Ethernet MAC
−Video Port I/F – Video In/Out *BT.656)
−SATA, uPP
−EMIFA – DDR (mDDR/DDR2)
−EMIFB – SDRAM/NAND/FLASH

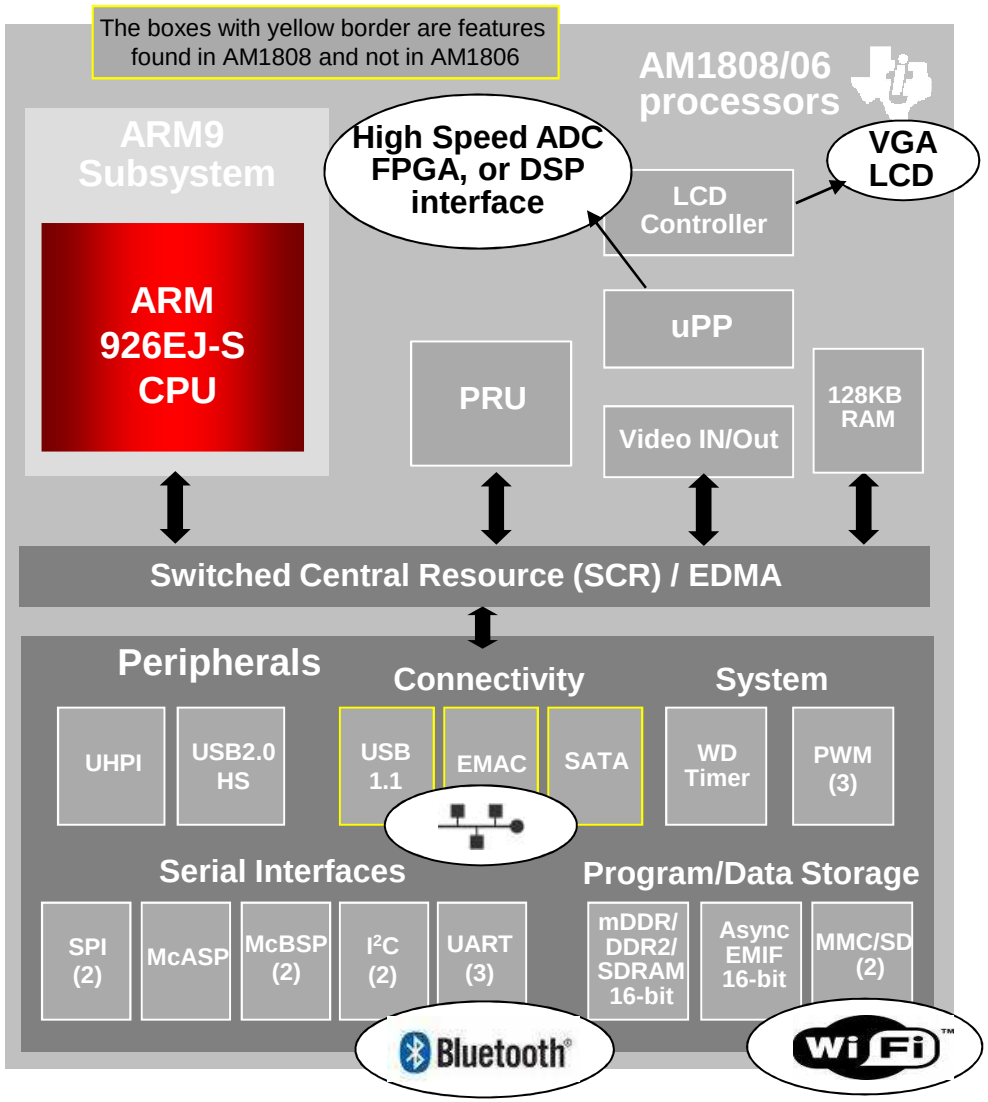
■Power (1.0-1.2V core, 1.8/3.3V IOs)

−Active < 182mW @ 300MHz/1.2V/25C (estimate)
−Standby < 7 mW @ 1.2V/25C (estimate)

■Package

–13 x 13mm nFBGA (0.65mm), ZCE , 361-balls
–16 x 16mm BGA (0.8mm), ZWT, 361-balls
–Extended Temperature Grade Options
- –Commercial (0C to 90C)
- –Industrial (-40C to 105C)

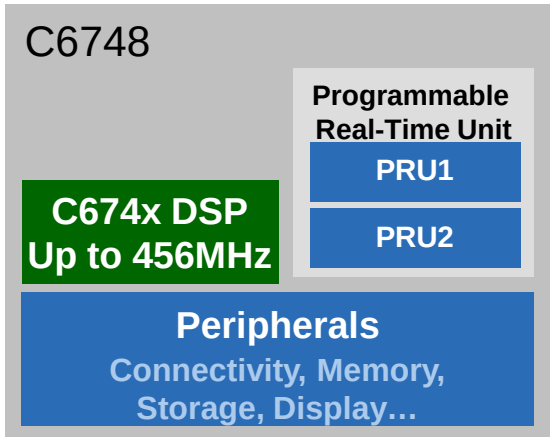
–Pin to pin compatible processors:
- –OMAP-L138/AM1806



Scalability to higher performance

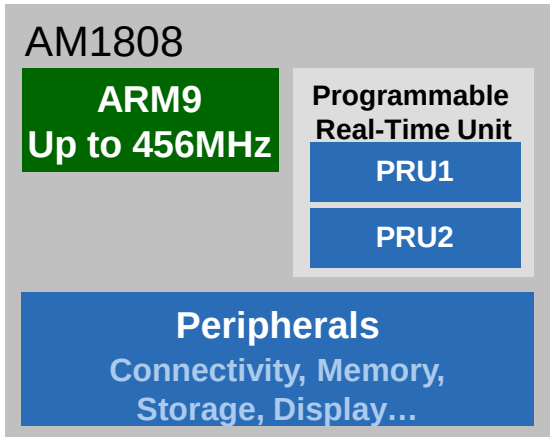
"DSP only" version

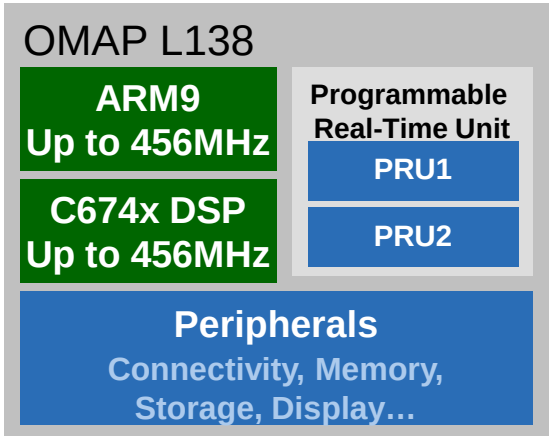
Floating Point DSP and 2 RISC cores (PRU)



"ARM only" version

ARM9 and 2 RISC cores (PRU)





Full featured version

ARM9, DSP and 2 RISC cores (PRU)

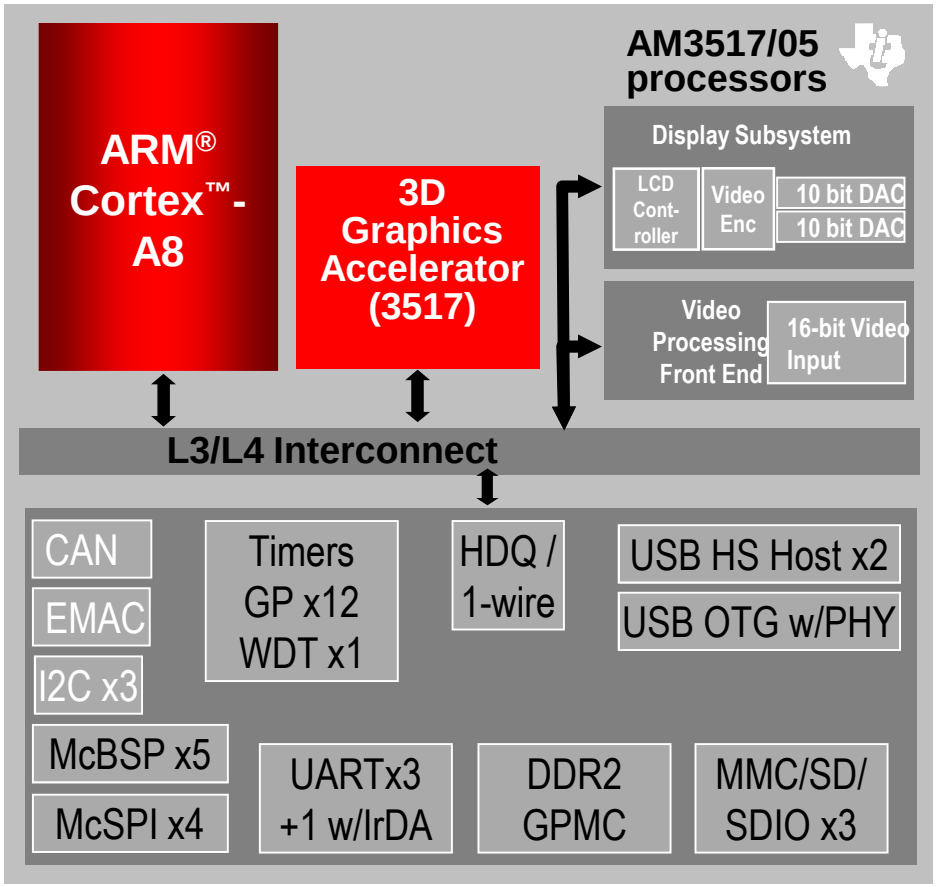
AM3517/05 Cortex™-A8 based processors

Example Applications

- Industrial and Home Automation
- Point of Service Terminals
- Single Board Computers
- Digital Signage
- Portable Industrial products
- Transportation - Navigation

Benefits

- High performance embedded computing
- Rich, intuitive user interfaces
- Native support for large displays
- System integration reduces board complexity

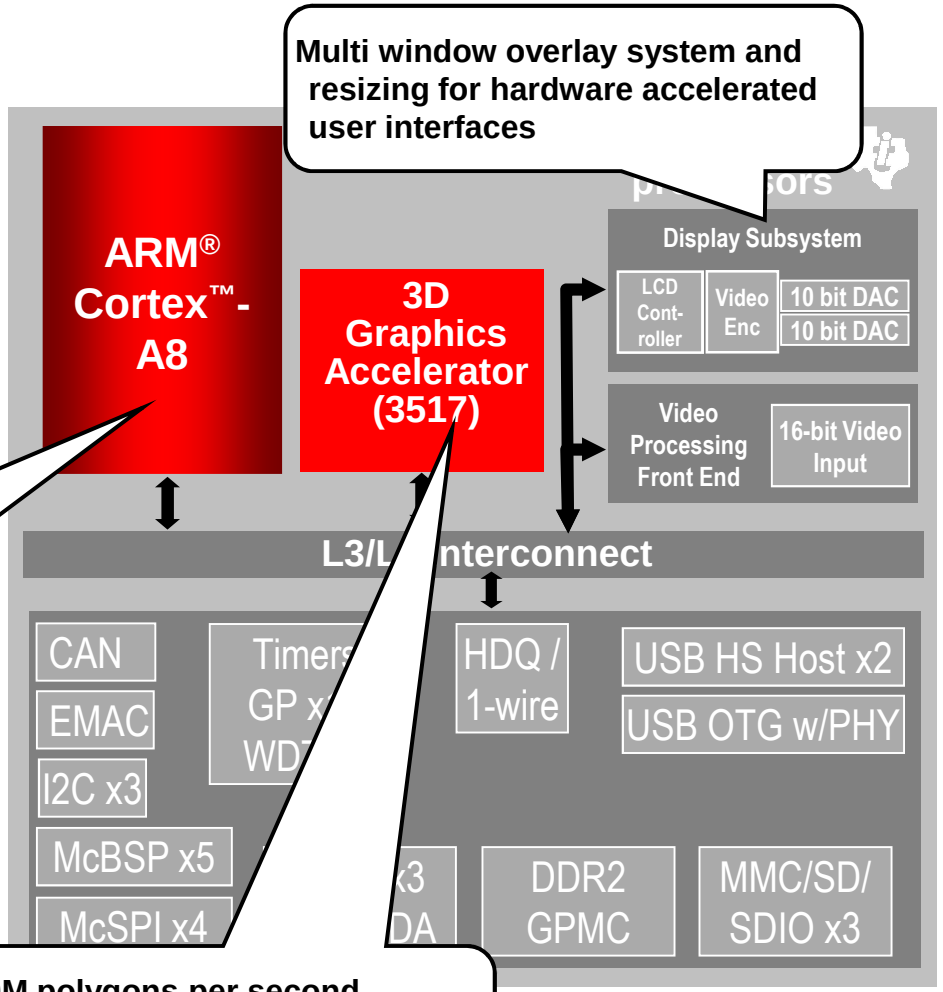


AM3517/05 Core and Accelerators

Features

- **Cores**
  - 500 MHz Cortex A-8 with NEON™ Coprocessor
  - 3D Graphics Engine – up to 10 polygons / second
- **Memory**
  - ARM:
    - 16 kB I-Cache; 16 kB D-Cache; 256kB L2 Cache
  - On Chip: 64kB SRAM; 128kB ROM
  - DDR2 interface
  - GPMC: NAND/NOR
  - interfaces

Up to 1000 Dhrystone MIPS:
- OS's like Linux or WinCE
- Excellent web experience



- Up to 10M polygons per second
- Hardware based on screen display
- Easily create robust GUI's

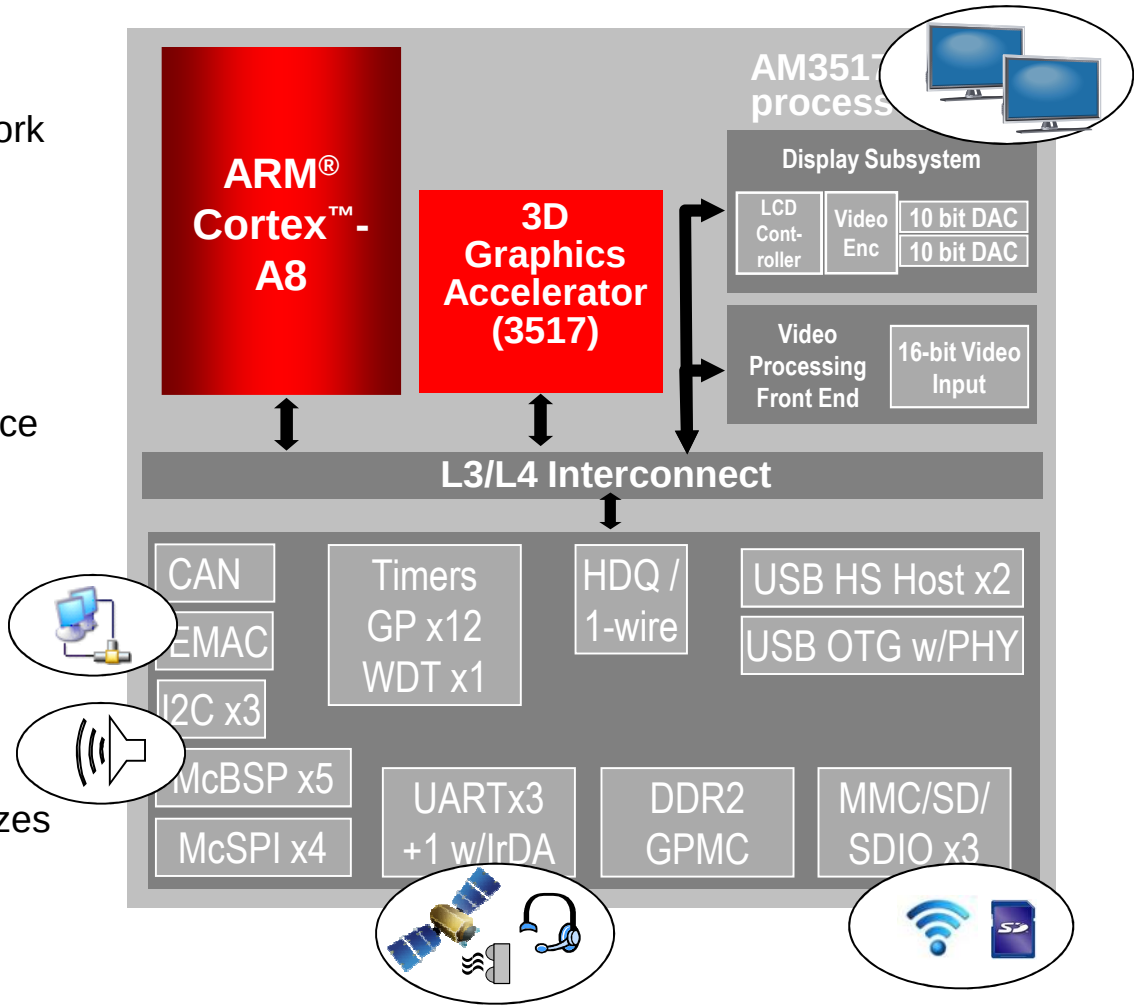
AM3517/05 Peripherals

Features

- **Peripherals**
  - CAN – High End Controller area network Controller (HECC)
  - USB 2.0 OTG w/PHY
  - RMII EMAC controller 10/100
  - USB HS Host x2
  - MMC/SD card interface x3
  - LCD controller and TV out
  - Display subsystem with PIP, color space conversion, rotation, resizing
  - 3.3V IO

- **Power**
  - Total Power: 0.5W – 1.5W
  - Standby Power: 12mW

- **Package**
  - ZCN – 17x17 mm, 0.65 mm pitch Utilizes Via Channel™ Array Technology with 0.8mm pitch plus design rules.
  - ZER – 23x23 mm, 1.0mm pitch



AM3715/03 Cortex™-A8 based processors

Cores
- Up to 1GHz Cortex-A8 with NEON™ coprocessor
- 3D graphics accelerator (3715)

Memory
- ARM: 32kB I-Cache; 32kB D-Cache; 256kB L2
- On Chip: 64kB SRAM
- External interfaces: LPDDR1 and NAND

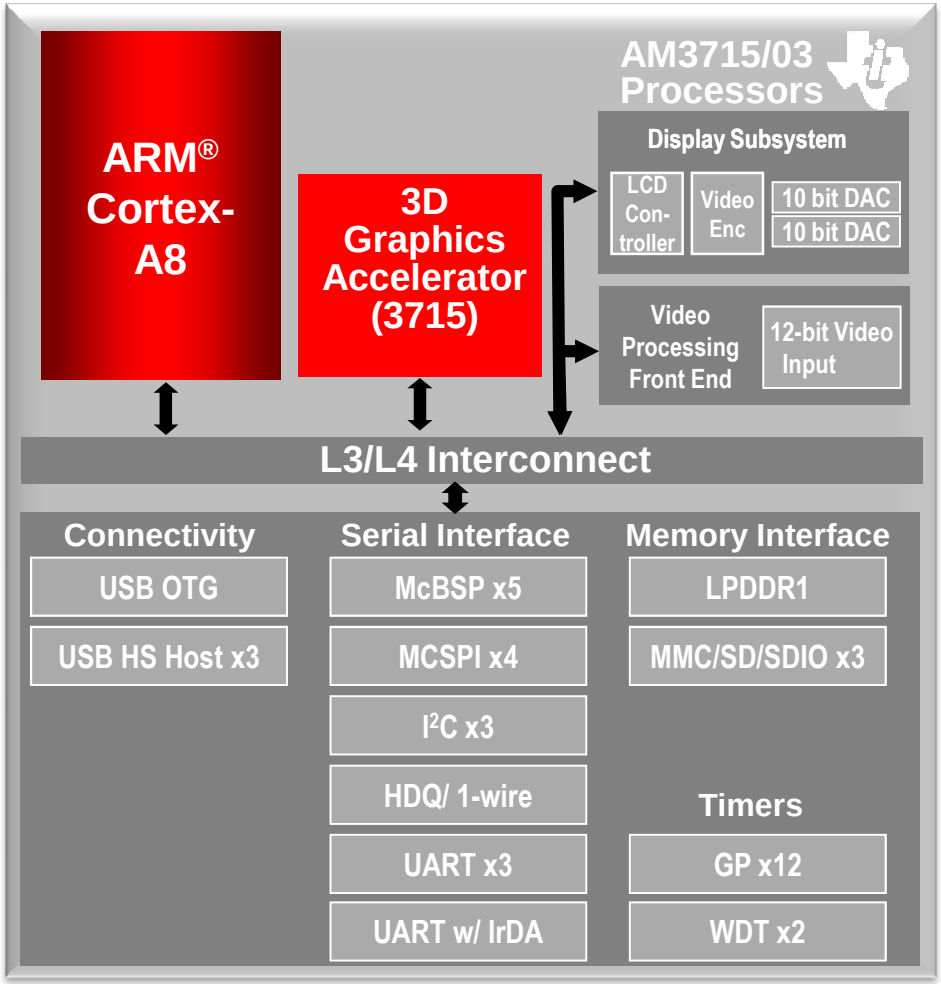
Peripherals
- USB HS Host x3
- USB 2.0 OTG
- MMC/SD card interface x3
- Display subsystem with LCD controller and dual 10 bit DAC's
- 1.8V I/O's

Power
- Dynamic Voltage and Frequency Scaling (DVFS)
- Total Power: 735mW (800MHz)
- Standby Power: 0.1mW (600MHz)

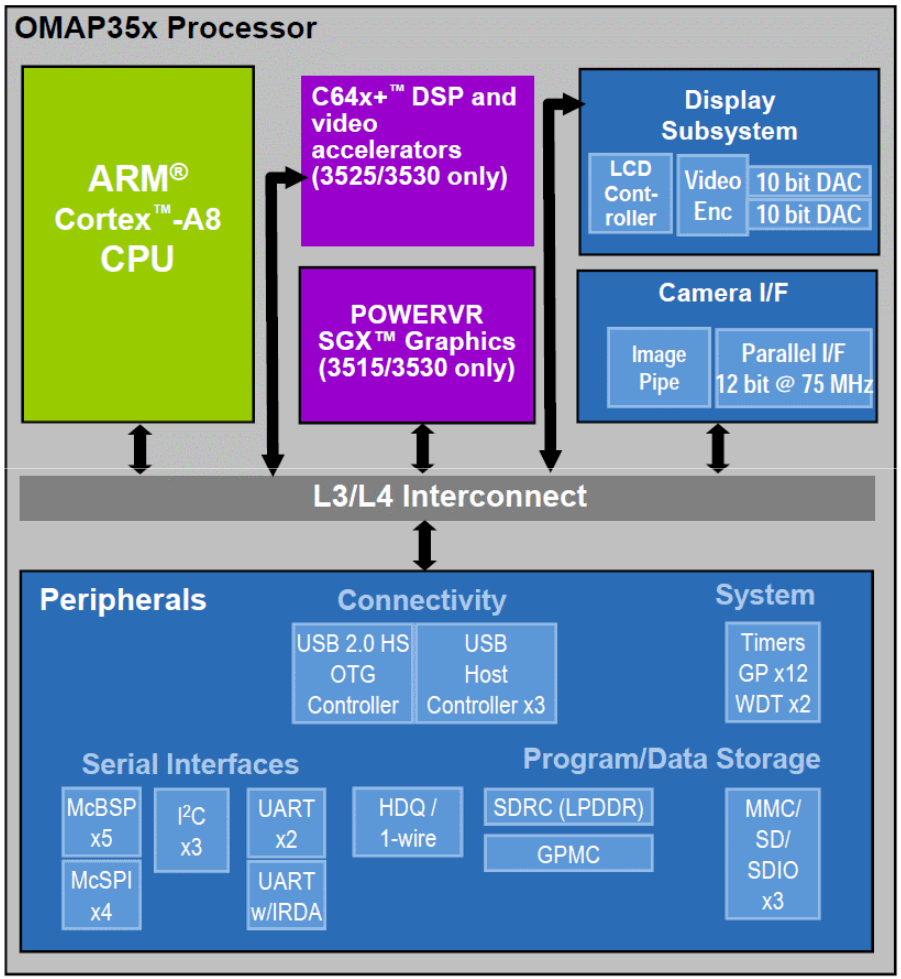
Package
- CBP: 12x12mm PBGA, 0.4mm pitch, 515-ball, Package on Package (PoP)
- CBC: 14x14mm PBGA, 0.5mm pitch, 515-ball, PoP
- CUS: 16x16mm PBGA, 0.65mm pitch. 423-ball. Utilizes Via Channel™ array technology with 0.8mm pitch plus design rules

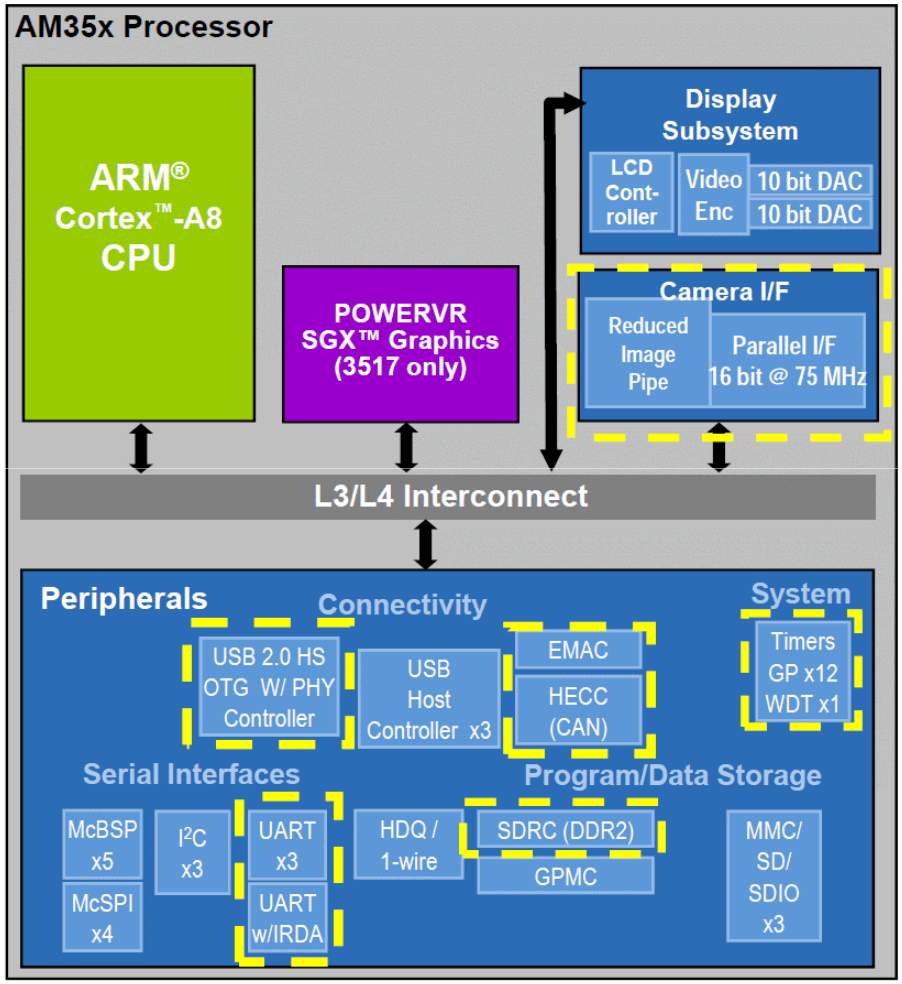
Benefits
- 2000DMIPS for OS's like Linux, Win CE, RTOS
- Up to 30% reduction in power
- 20M polygons per second for robust GUIs

Sample Applications
- Smart connected devices
- Patient monitoring
- Single board computers
- Low power PC

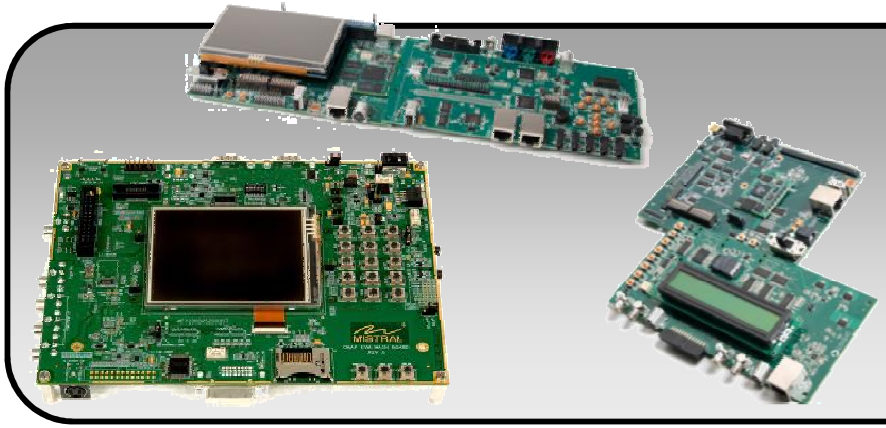


AM35x vs. OMAP35x





Evaluation and Development Kits



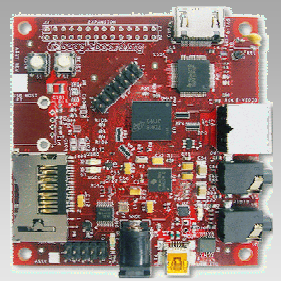
Development Kit Contents:

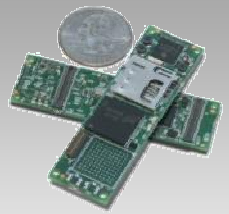
- Eval board & documentation
- BSP
- Development tools

Get Started Today

Tool	Part Number	Price	Availability
OMAP35x EVM	TMDSEVM3530	$1495	TI
AM3517 EVM	TMDXEVM3517	$999	TI
AM18x EVM	TMDXEVM1808L	$1150	TI
AM18x Experimenter Kit	TMDXEXP1808L	$445	TI
Zoom OMAP35x Development Kit	TMDSMEVM3530-L	$995 (subject to change)	Logic
Zoom AM3517 Experimenter Kit	SDK-XAM3517-10-256512R	$199 (subject to change)	Logic
OMAP-L137 (AM1707) Starter Kit	EVMOMAPL137	$415 (subject to change)	Spectrum Digital

Featured Modules





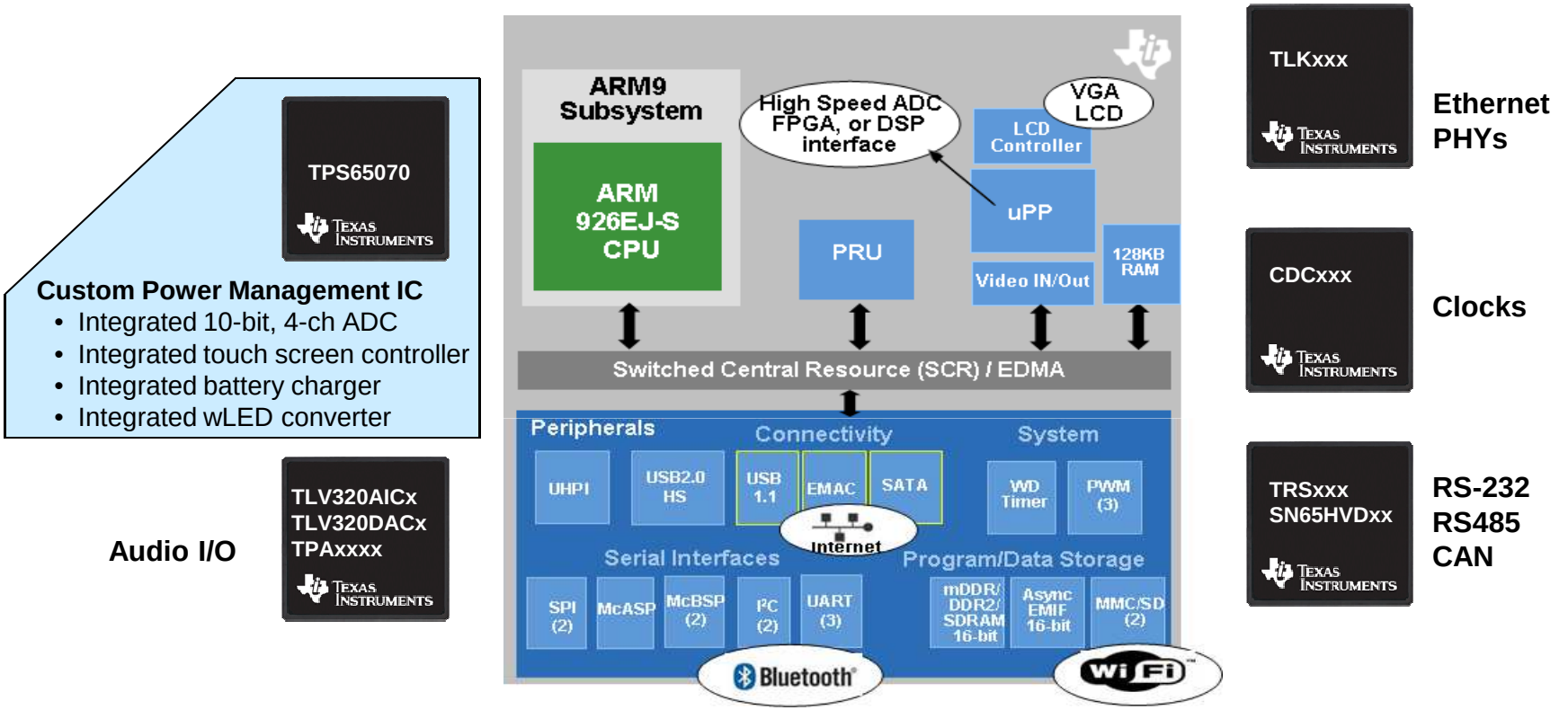
Get Started Today

How to access:

- **Contact TI Partners for more information or click link to buy now**

Tool	Part Number	Price	Availability
Beagle Board (OMAP35x)	Beagle	$149 (subject to change)	Community
Hawkboard (OMAP-L138)	ISSPLHawk	$89 (subject to change)	Community
OMAP35x System on Module	OMAP35x SOM-LV	$99 (subject to change)	Logic
Overo OMAP35x Computer on Module	Overo	$149-$219 (subject to change)	Gumstix
KBOC OMAP35x System on Module	KBOC	$139 (subject to change)	KwikByte

Analog & Power Attach for AM1x

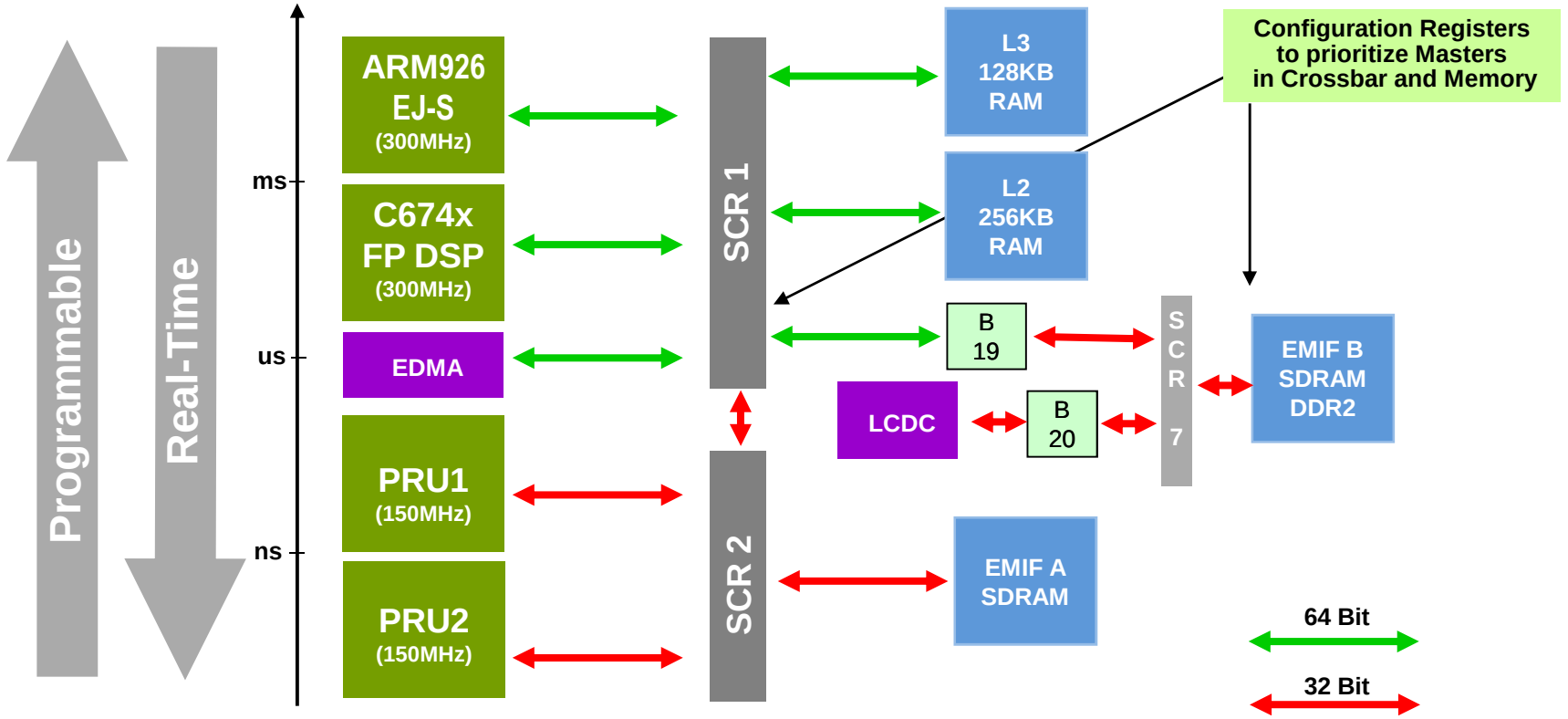


Power for Processors website: www.ti.com/processorpower

For AM18x specifically:
http://processors.wiki.ti.com/index.php/Analog_and_Power_for_AM18x

Technical Details – AM18x Key Peripherals

OMAP-L1 Multi-Core Architecture



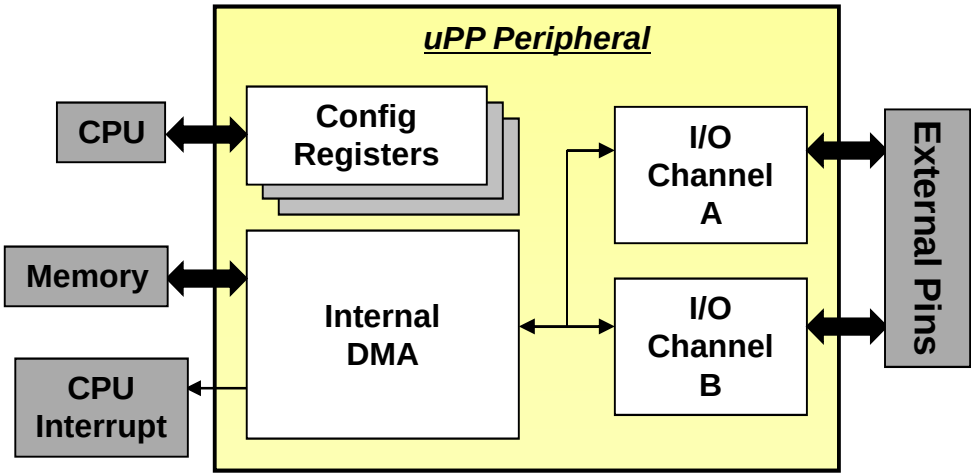
"Multi-Issue" Switched Central Resource 1 has 12x4 crossbar with 64 bit path at 150MHz.

With concurrent operation of up to 4 slaves the peak throughput is 4,8 GB/s!

Universal Parallel Port (uPP)
Extends System Interconnect Options (AM18x, OMAP L138 only)

What Is uPP?

- High Speed parallel data port
- Two Bidirectional and Independent 16bit channels
- Internal dedicated DMA to streamline data I/O
- Simple I/O Protocol



Value of uPP

- Efficient Processor to FPGA communication enabled by high speed data I/O
- Enable multi-processor system design in various topologies
- Interface with high speed ADCs and DACs

Configuration	Throughput (MB/s)
1 Ch, 16-bit	120
2 Ch, 1 Way, 8-bit	120
2 Ch, 1 Way, 16-bit	160
2 Ch, 2 Way, 16-bit	240
HPI (16-bit)	50

PRU Introduction
(available on OMAP L1x, AM1xxx and C674x)

- What is PRU?
  - **P**rogrammable **R**eal-time **U**nit Subsystem
  - Dual 32bit RISC processors running at ½ CPU freq.
  - Local instruction and data RAM. Access to chip-level resources

- Why PRU?
  - Full programmability allows adding customer differentiation
  - Efficient in performing embedded tasks that require manipulation of packed memory mapped data structures
  - Efficient in handling of system events that have tight real-time constraints.

PRU Value

- Extend Connectivity and Peripheral capability
  - Implement special peripherals and bus interfaces (e.g. UARTs)
  - Implement smart data movement schemes. Especially useful for Audio algorithms (e.g. Reverb, Room Correction)
- Reduce System Power Consumption
  - Allows switching off the ARM clocks
  - Implement smart power controller by evaluating events before waking up ARM. Maximized power-down time.
- Accelerate System Performance
  - Full programmability allows custom interface implementation
  - Specialized custom data handling to offload ARM for innovative signal processing algorithm implementation

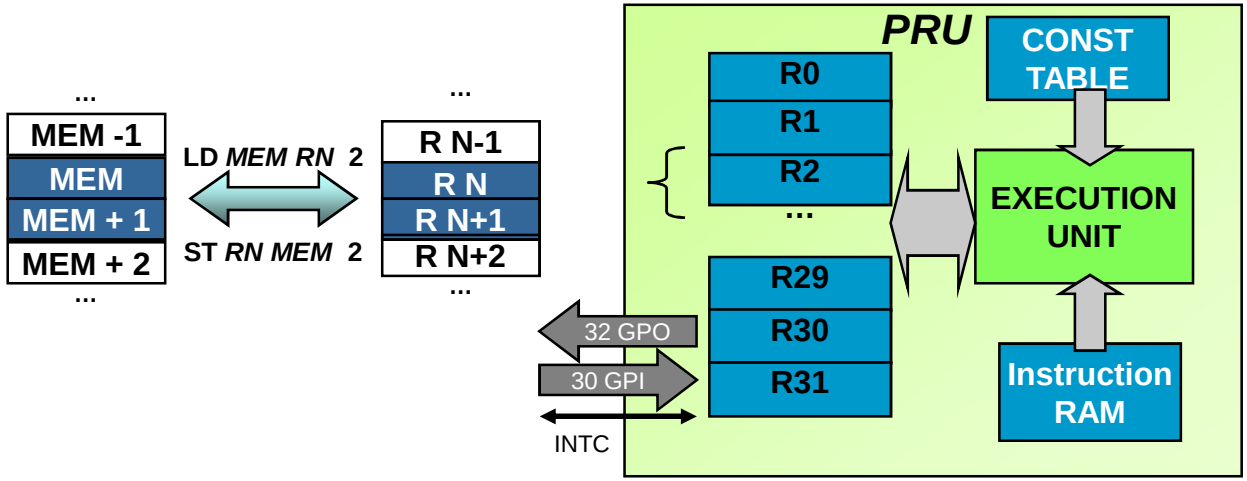
PRU Functional Block Diagram

General Purpose Registers

- All instructions are performed on registers and complete in a single cycle
- Register file appears as linear block for all register to memory operations

Constant Table

- Ease SW development by providing freq used constants
- Peripheral base addresses
- Few entries programmable



Execution Unit

- Logical, arithmetic, and flow control instructions
- Scalar, no Pipeline, Little Endian
- Register-to-register data flow
- Addressing modes: Ld Immediate & Ld/St to Mem

Special Registers (R30 and R31)

- R30
  - Write: 32 GPO
- R31
  - Read: 30 GPI + 2 Host Int status
  - Write: Generate INTC Event

Instruction RAM

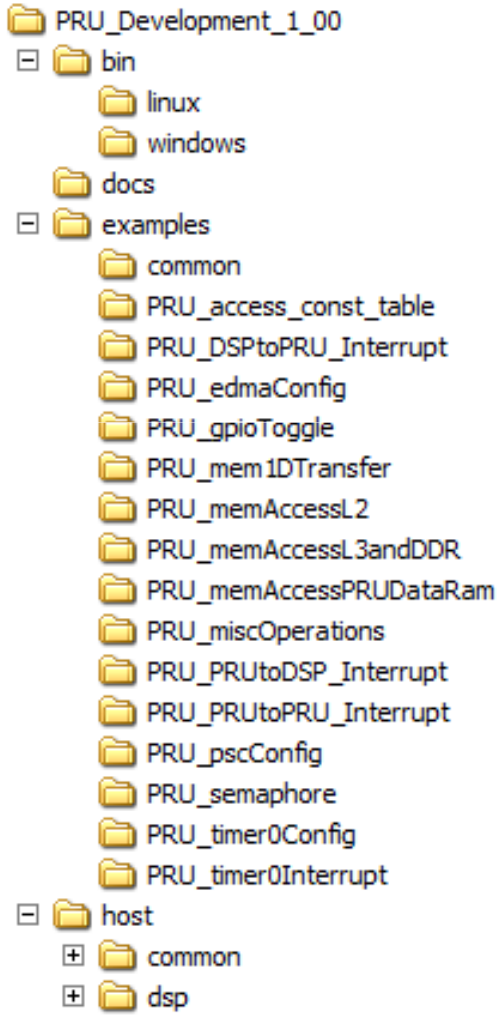
- 4KB in size; 1K Instructions
- Can be updated with PRU reset

PRU Instruction Set

Arithmetic Operations	Logic Operations	IO Operations	Program Flow Control
ADD	LSL	*MOV*	JAL
ADC	LSR	LDI	JMP
SUB	AND	LBBO	QBGT
SUC	OR	SBBO	QBGE
RSB	XOR	LBCO	QBLT
RSC	NOT	SBCO	QBLE
	MIN	*ZERO*	QBEQ
	MAX	*MVIB*	QBNE
	CLR	*MVIW*	QBA
	SET	*MVID*	QBBS
	SCAN		QBBC
	LMBD		*WBS*
			WBC
			HALT
			SLP
			CALL
			RET

Pseudo Op-code (Italic)

Basic Software Package Contents (Today)



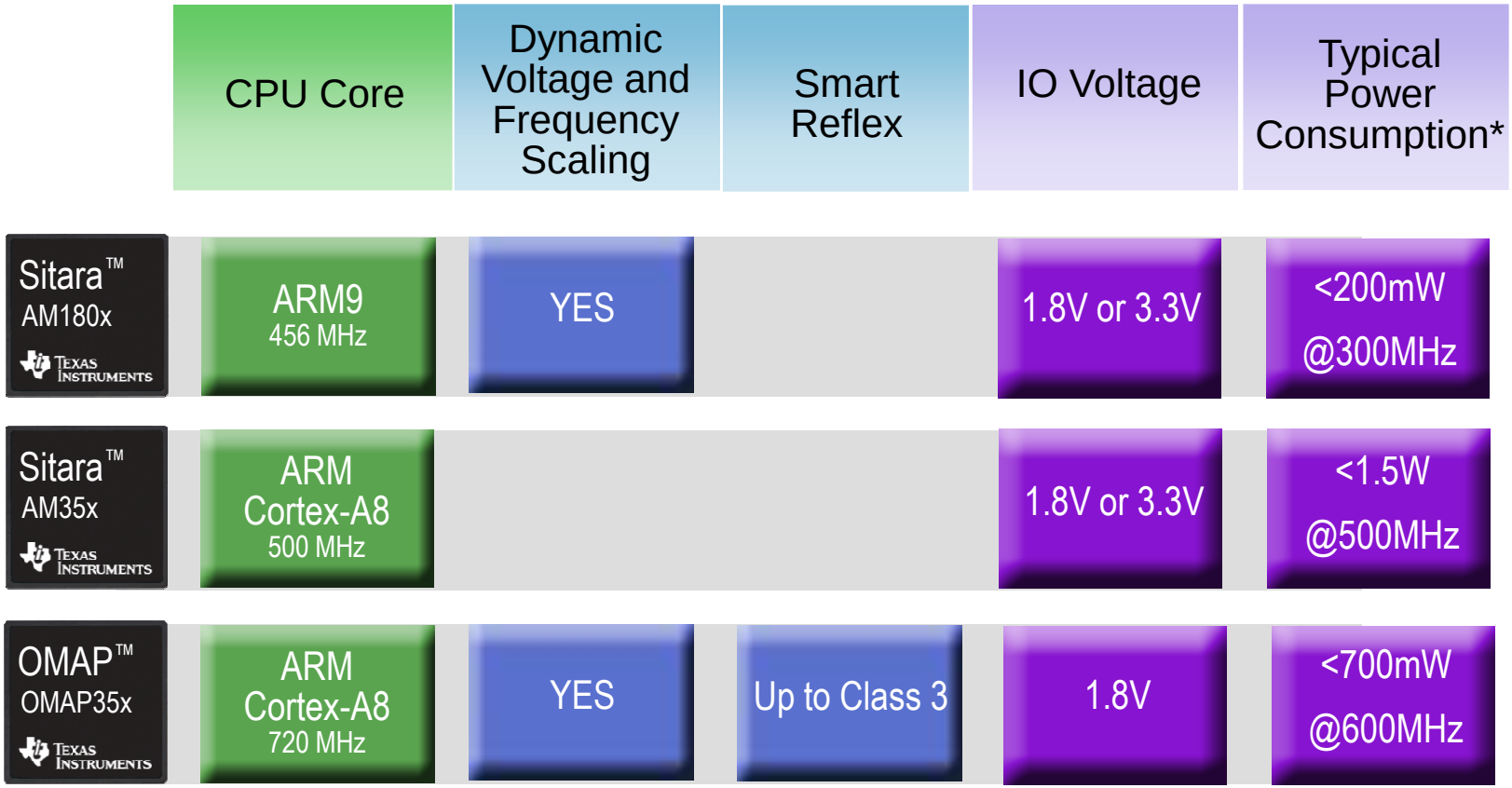
- http://focus.ti.com/docs/toolsw/folders/print/sprc940.html
- Bin directory
  - PASM binary tool
- Doc
  - Current documentation
  - Reference to online documentation
- Examples
  - Collection of CCSv3 DSP projects and associated PRU code
- Host
  - Common: rCSL, PRU APIs, various helper functions used by examples
  - DSP: CCSv3 loader examples for C674x DSP core

Advanced Software Package

- Development to be done by Mistral
  - Free download from Mistral
  - http://www.mistralsolutions.com/assets/downloads/L13x.php
- Full soft IP deliverables (CCS based)
  - Multichannel UART, utilizing McASP (proof of concept demo) - done
  - CAN interface - done
  - Profibus, RTE - TBD
  - Specialized timers/schedulers -TBD
  - Smartcard IF -TBD
  - DMA framework for specialized audio algorithms -TBD
- Daughtercards for OMAP L138 and AM1808 EVM
  - UART: http://www.mistralsolutions.com/products/amdm1x_evm_uart.php
  - CAN: http://www.mistralsolutions.com/products/amdm1x_evm_can.php

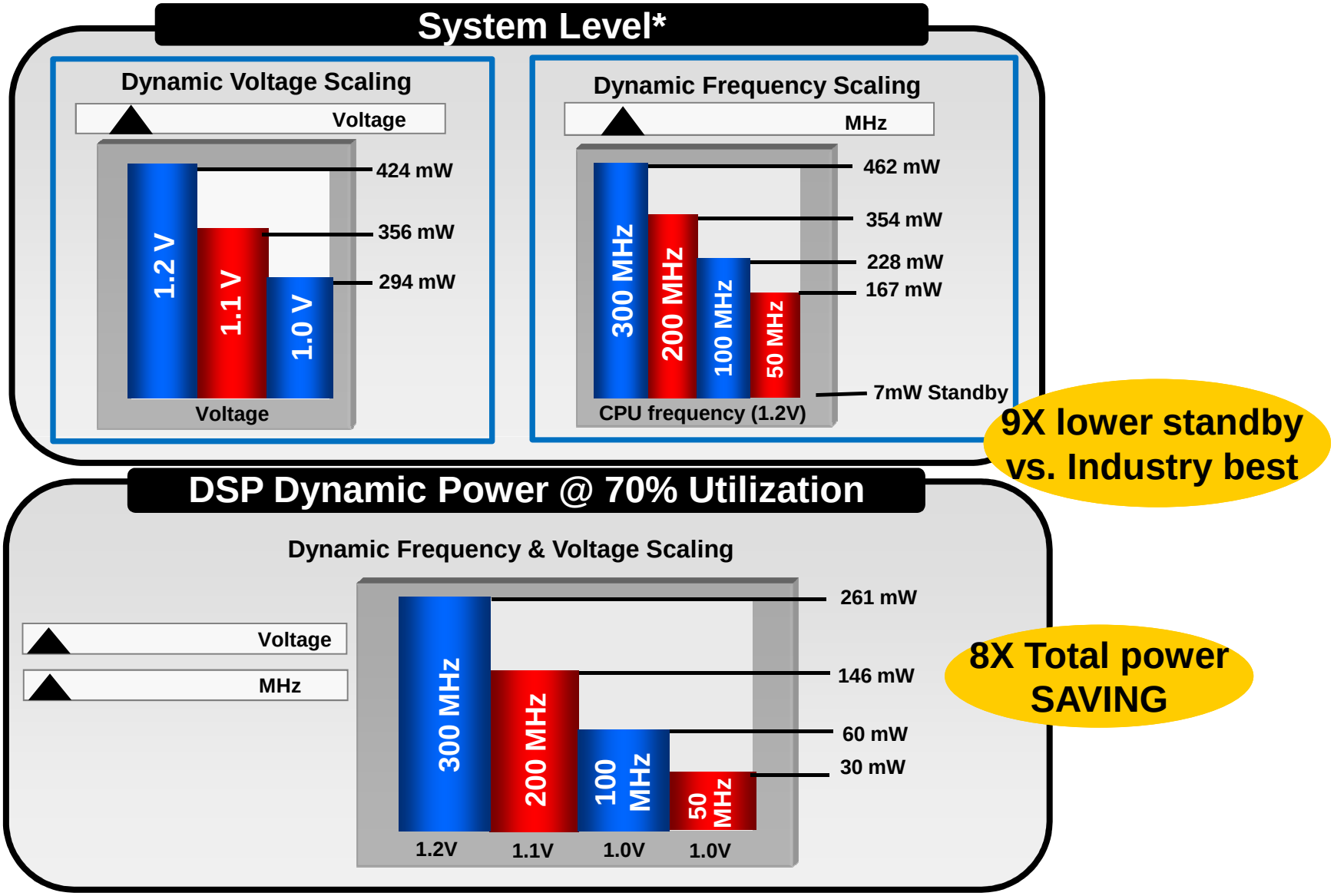
Making Use of Sitara Low Power Features

Comparison of Low Power Features



* Estimated values at 25C

Dynamic Voltage Frequency Scaling and Standby Power savings



OMAP-L138/C6748/6/2
*Use case: 70% DSP (300MHz), 50% EMIF (133MHz), 50% McBSP (25 MHz), Timer at 100%, CVdd= 1.2V, @ 25C, ARM (300MHz) typical activity

Texas Instruments

Smart Reflex on OMAP35x™

Dynamic Voltage & Frequency Scaling (DVFS)

Consume less energy/power in low performance modes by lowering the voltage

	IVA MHz	ARM MHz	VDD_MPU_IVA
OMAP 3530	430	600	1.35
	400	550	1.27
	360	500	1.20
	180	250	1.00
	90	125	0.95

L3 MHz	VDD_CORE
166	1.15
100	1
41.5	0.95

Adaptive Voltage Scaling (SmartReflex)

Lower voltages when the chip process and temperature allow it

Optimizing for process variations gives majority of power savings and optimizing for temperature and silicon degradation provides incremental power savings.

	IVA MHz	ARM MHz	VDD_MPU_IVA
OMAP 3530	430	600	1.35 - 1.12
	400	550	1.27 - 1.07
	360	500	1.20 - 1.00
	180	250	1.00 - 0.90
	90	125	0.95 - 0.80

L3 MHz	VDD_CORE
166	1.15 - 0.95
100	1.00 - 0.85
41.5	0.95 - 0.80

Operating points subject to change prior to TMS

AM18x Runtime Power Management Techniques

- Clock gating (modules, infrastructure)
- CPU idle/sleep modes
- Deep Sleep Mode
- Dynamic frequency scaling (PLL)
- Dynamic voltage scaling (PMIC)
- PHY power down (SATA, USB, DDR)

Power Management - Linux View

Dynamic Power Management (cpufreq)

- This technique is used when the processor is active.
- DVFS
  - Changes between OPPs
  - Pre & Post OPP change notification.

AM18xx & OMAPL138 Linux Power Management

All features already available & demonstrable

Idle Power Management (cpuidle)

- This technique is used when the processor is idle.
- Select optimal sleep state
  - Considers time available for sleep
  - State entry/exit latency
- Dynamic Tick Suppression helps extend sleep duration

User Initiated Power Management (suspend-to-RAM)

- User asks device to suspend
- Implemented using Deep Sleep mode of AM18xx/OMAPL1x8
- Linux device model used to suspend registered devices
- Wakeup based on
  - RTC Alarm
  - External event
- On resume re-activates running processes

Linux Power Management on OMAPL138 & AM18xx

AM18xx Power Management Feature	AM18xx Linux Support
PSC Clock Gating	Clock Framework* clk_get clk_enable clk_disable
ARM WFI	cpuidle state 0 state 1
mDDR self-refresh	cpuidle state 1
Dynamic Voltage and Frequency Scaling (DVFS)	cpufreq
Deep Sleep	suspend-to-RAM

*The kernel keeps ARM, ARM ROM, EDMA, AINTC and EMIF3 always enabled.

Demo Power : DVFS & CPUFreq

Legend

User command

Result

Set of scripts available to test DVFS

```
root@omapl138:~# cd /home/
root@omapl138:/home# ./list_available_freq
456000 372000 348000 300000 200000 96000
root@omapl138:/home# ./list_available_governors
conservative ondemand userspace powersave performance
root@omapl138:/home# ./display_current_frequency
456000
root@omapl138:/home# ./select_speed 96000
root@omapl138:/home# ./display_current_frequency
96000
```

details on next slide

Linux governors for setting CPU Speed

```
root@omapl138:/home# ./list_available_governors
conservative ondemand userspace powersave performance
```

Conservative

Adjusts frequencies based on processor utilization, gradual change of frequency

Ondemand

Based on proc utilization, but faster switch to max speed (compared to “Conservative”)

Userspace

User manually selects CPU speed

Powersave

CPU runs at slowest speed (lowest performance, lowest power consumption)

Performance

CPU runs at max speed (highest performance, highest power consumption)

Demo Power : Regulators

Legend

`User command`

`Result`

Set of scripts available to test Regulators info

```
root@omapl138:/home# ./display_current_frequency
456000
root@omapl138:/home# ./display_regulator_info
VDCDC1 / enabled / 3300000
VDCDC2 / enabled / 3300000
VDCDC3 / enabled / 1325000
LDO1 / enabled / 1800000
LDO2 / enabled / 1200000
root@omapl138:/home# ./select_speed 96000
root@omapl138:/home# ./display_current_frequency
96000
root@omapl138:/home# ./display_regulator_info
VDCDC1 / enabled / 3300000
VDCDC2 / enabled / 3300000
VDCDC3 / enabled / 1000000
LDO1 / enabled / 1800000
LDO2 / enabled / 1200000
```

Power Consumption Optimization

ARM MPU Speed decrease enables the Power Management scripts to automatically reduce the Regulator voltage & then reduce system power consumption

Demo Power : Suspend to RAM

Legend

User command

Result

On PMDC watch Channel 4 : ARM power consumption ➔ from 80mW to 0mW

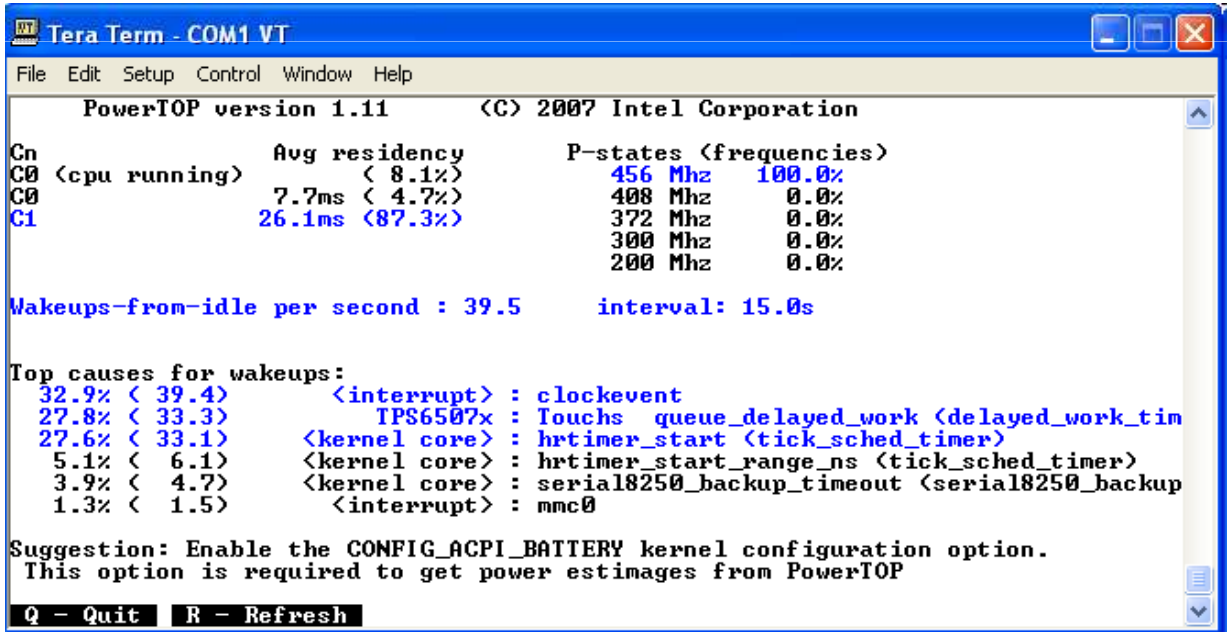
```
root@omapl138:/home# ./sleep 10
wakeup from "mem" at Tue Dec 15 10:23:16 2009
PM: Syncing filesystems ... done.
Freezing user space processes ... (elapsed 0.01 seconds) done.
Freezing remaining freezable tasks ... (elapsed 0.01 seconds) done.
Suspending console(s) (use no_console_suspend to debug)
```

…wait 10 s …

```
PM: suspend of devices complete after 207.924 msecs
PM: late suspend of devices complete after 0.215 msecs
PM: early resume of devices complete after 0.071 msecs
PM: resume of devices complete after 367.441 msecs
Restarting tasks ... done.
```

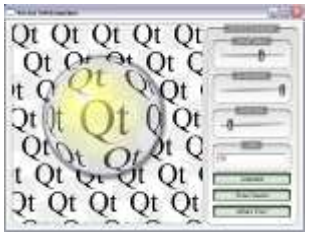
Power Top

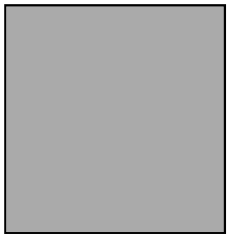
- PowerTOP is a Linux tool that helps you find those programs that are misbehaving while your computer is idle . PowerTOP has these four basic goals:
  - Show how well your system is using the various hardware power-saving features
  - Show you the culprit software components that are preventing optimal usage of your hardware power savings
  - Provide you with tuning suggestions to achieve low power consumption
- `root@omapl138:~#` **`powertop`**



Demo: Qt/e Fluidlauncher

- Fluidlauncher is “Smart Menu” Interface to launch different applications with your finger
  - SVG Viewer
  - StyleSheets
  - Vector Deformation
  - Path Strokin
  - Exit Embedded Demo





- If No action after 6 seconds : Slideshow of AM1xxx Value proposal
  - Touch the screen to come back to
  - Watch Power consumption
    - Channel 4 : ARM – 80mW @ 456MHz

Thank You!