



TI Technology Days 2010

Low-power Embedded Processing Solutions for Industrial Automation

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System Engineer - Industrial Automation Lab






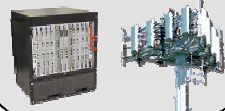







Agenda

- Embedded Processing Portfolio
- Industrial Automation Architecture
- Industrial Communication
- Programmable Logic Control
- Human Machine Interface
- TI Solutions - Roadmap

Problem Definition

- Common challenges in electronic industry
 - Smaller
 - Cheaper
 - Reduce power consumption
 - Shorter time-to-market
- Industrial Automation specific
 - Wide operating conditions
 - Long-term availability
 - Deterministic and safe
 - Special standards and features

Embedded processing portfolio

TI Embedded Processors						
Microcontrollers (MCUs)		ARM®-Based Processors		Digital Signal Processors (DSPs)		
16-bit ultra-low power MCUs	32-bit real-time MCUs	32-bit ARM Cortex™-M3 MCUs	ARM Cortex-A8 & ARM9™ MPUs	DSP DSP+ARM	Multi-core DSP	Ultra Low power DSP
MSP430™ Up to 25 MHz Flash 1 KB to 256 KB Analog I/O, ADC, LCD, USB, RF Measurement, Sensing, General Purpose \$0.25 to \$9.00 	C2000™ Delfino™ Piccolo™ 40MHz to 300 MHz Flash, RAM 16 KB to 512 KB PWM, ADC, CAN, SPI, I²C Motor Control, Digital Power, Lighting, Ren. Energy \$1.50 to \$20.00 	Stellaris® ARM Cortex-M3 Up to 100 MHz Flash 8 KB to 256 KB USB, ENET, MAC+PHY, CAN, ADC, PWM, SPI Connectivity, Security, Motion Control, HMI, Industrial Automation \$1.00 to \$8.00 	Sitara™ ARM Cortex-A8 & ARM9 375MHz to >1GHz Cache, RAM, ROM USB, CAN, SATA, SPI, PCIe, EMAC Industrial automation, POS & portable data terminals \$5.00 to \$25.00 	C6000™ DaVinci™ video processors OMAP™ 300MHz to >1Ghz +Accelerator Cache, RAM, ROM USB, ENET, PCIe, SATA, SPI Floating/Fixed Point, Video, Audio, Voice, Security, Conferencing \$5.00 to \$200.00 	C6000™ 24,000 MMACS Cache, RAM, ROM SRIO, EMAC, DMA, PCIe Telecom test & meas, media gateways, base stations \$40.00 to \$200.00 	C5000™ Up to 300 MHz +Accelerator Up to 320KB RAM, Up to 128KB ROM USB, ADC, McBSP, SPI, I²C Audio, Voice, Medical, Biometrics \$3.00 to \$10.00 
<div>    Software & Dev. Tools    </div>						

Sitara™ ARM® microprocessors

Available Now

In Development

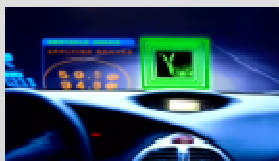
ARM9™

AM1808

AM1806

AM1707

AM1705



Low Power ARM9 with flexible peripherals

- Power efficient (down to 7mW standby, 182mW active)
- User configurable interfaces through the programmable real-time unit (PRU)
- Integrated peripherals, 10/100 Ethernet, USB, SATA, CAN, UART and many others

ARM Cortex™-A8

AM3715

AM3703

AM3517

AM3505

OMAP3515

OMAP3503



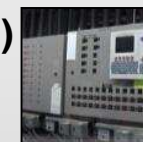
High-performance Cortex-A8 with system integration

- Up to 1GHz (2000 DMIPS)
- Power efficient (down to 12mW standby, 1W active)
- Integrated graphics for rich user interface functions
- Integrated interfaces to display, USB, 10/100 Ethernet, SD card, Wi-Fi®, CAN, and many others

ARM Cortex-A8

“AM38x Next” (2011)

“AM33x Next” (2011)

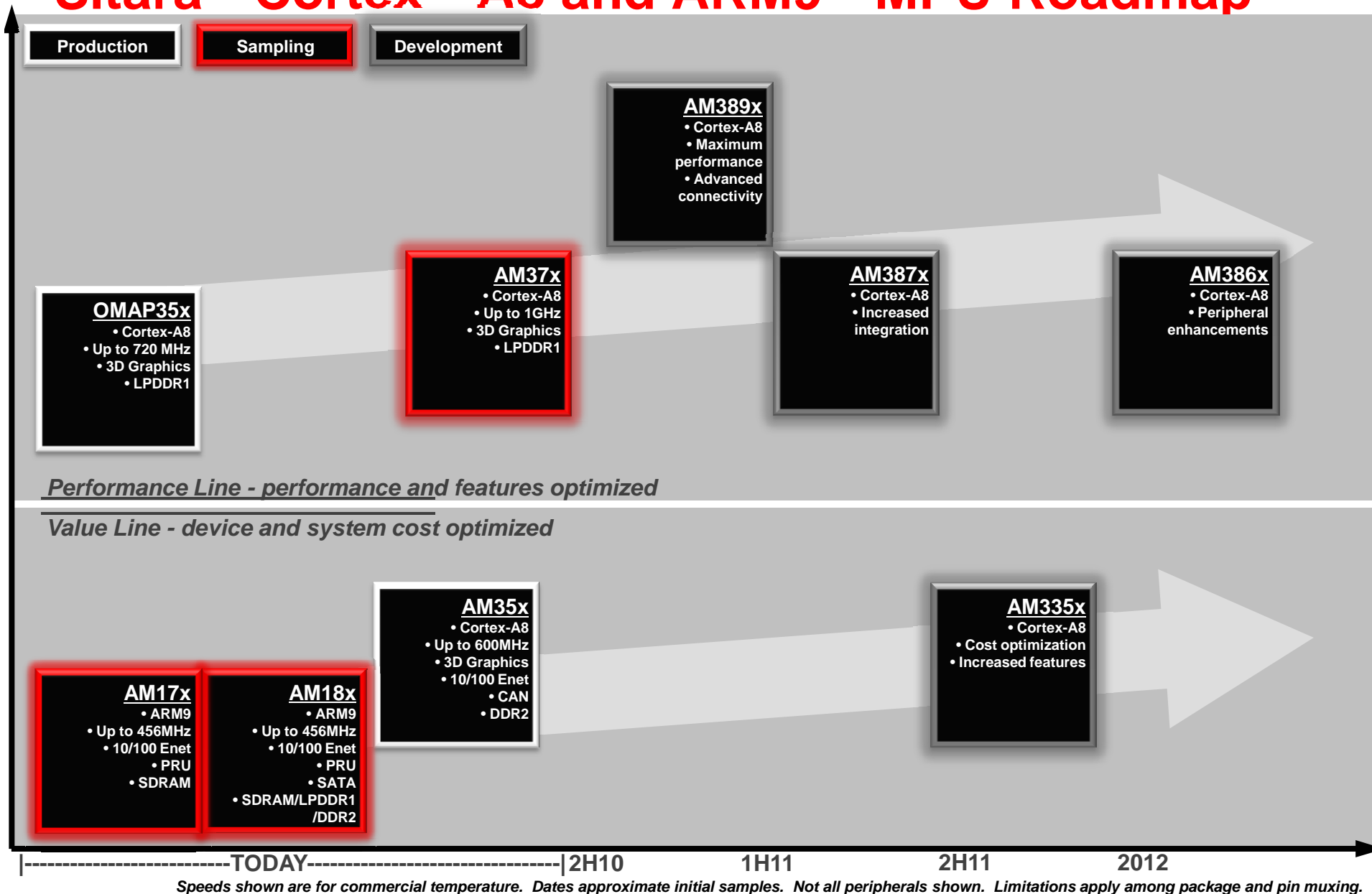


Advanced Cortex-A8 with performance and value options

- Greater than 1GHz core performance
- 1080p display support
- Enhanced graphics for superior user interface functions
- Peripheral integration of 1Gb Ethernet, PCIe, and many others

Support for Linux, Windows® Embedded CE, Android, & RTOS

Sitara™ Cortex™-A8 and ARM9™ MPU Roadmap



AM3517/05 Core and Accelerators

Features

■ Cores

- 500 MHz Cortex A-8 with NEON™ Coprocessor
- 3D Graphics Engine – up to 10 polygons / second

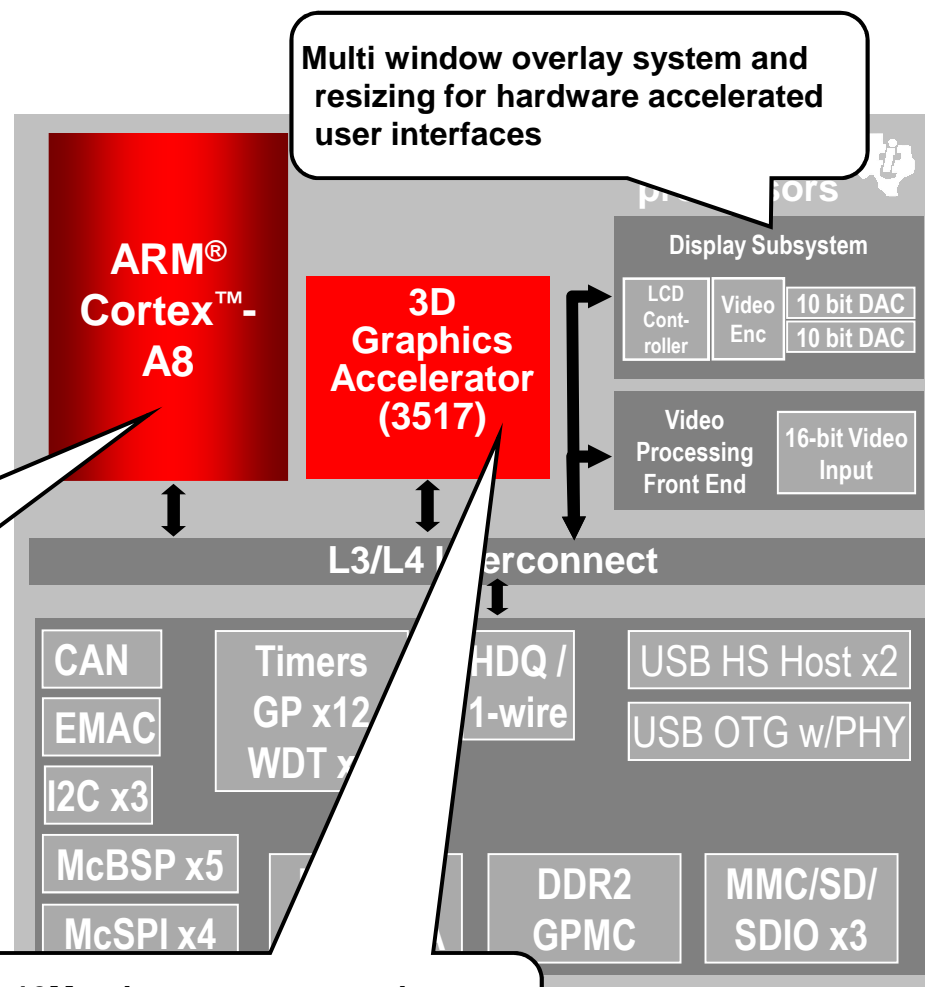
Up to 1000 Dhrystone MIPS:

- OS's like Linux or WinCE
- Excellent web experience

■ Memory

- ARM:
 - 16 kB I-Cache; 16 kB D-Cache; 256kB L2 Cache
- On Chip: 64kB SRAM; 128kB ROM
- DDR2 interface
- GPMC: NAND/NOR
- interfaces

- Up to 10M polygons per second
- Hardware based on screen display
- Easily create robust GUI's



OMAP-L138 (ARM9 + C674x DSP)

■ CPU Cores

- ARM926EJ-S™ (MPU) 300MHz+
- C674x DSP Core 300MHz+
- 2 PRU Cores upto 150 MHz each

■ Peripherals (1.8/ 3.3V IOs)

- 10/100 Ethernet MAC
- EMIFA - SDRAM/NAND Flash
- EMIFB – DDR (mDDR/DDR2)
- Video Port I/F, SATA, uPP, LCDC

■ Power (1.0-1.2V Core, 1.8/3.3V IOs)

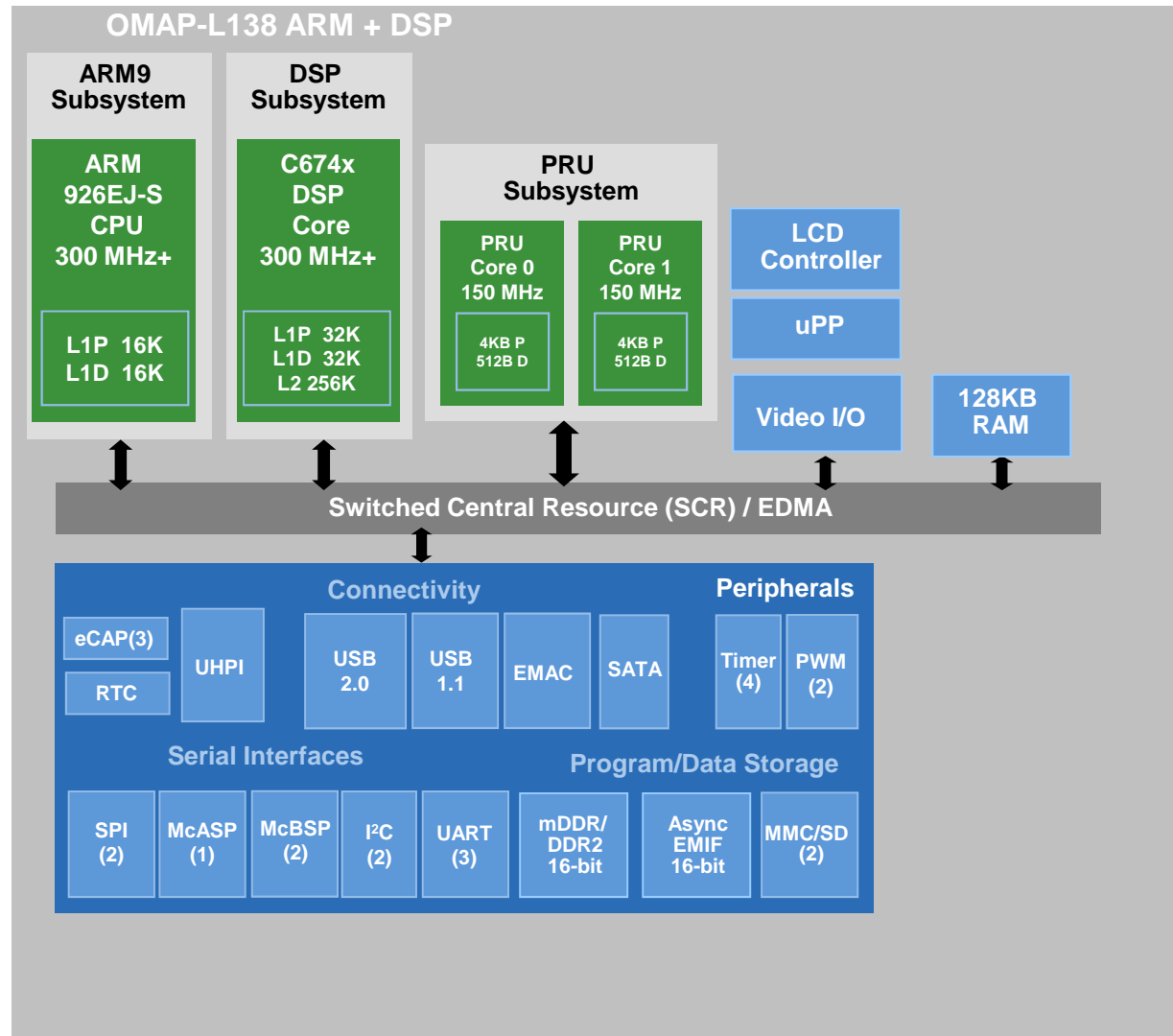
- Total Power < 440 mW @ 300MHz, 1.2V, 25C
- For DSP at 70% loading, ARM at 50% loading; mDDR 50% active at 135MHz
- Standby Power < 9mW @ 1.2V/ 25C

■ Package

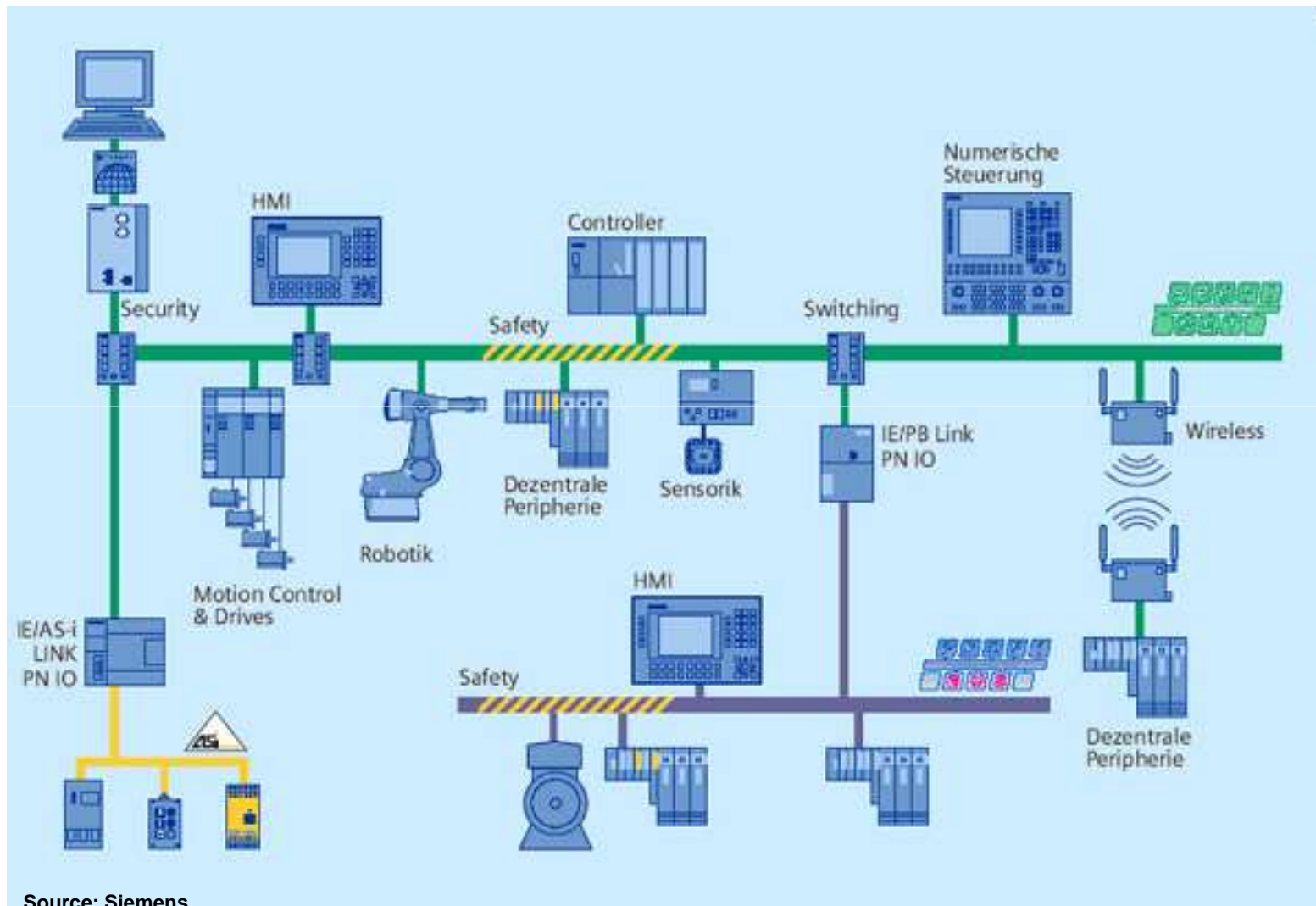
- 13 x13mm nFBGA (0.65mm), 16x16mm BGA (0.8mm)
- Pin to pin compatible with C6748/6/2, AM1808/6

■ Applications

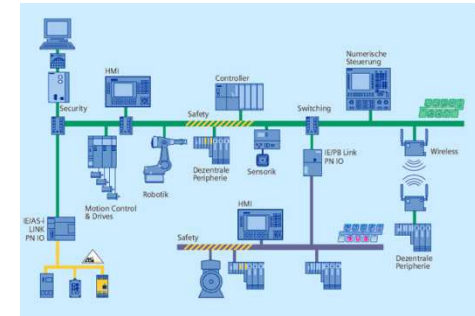
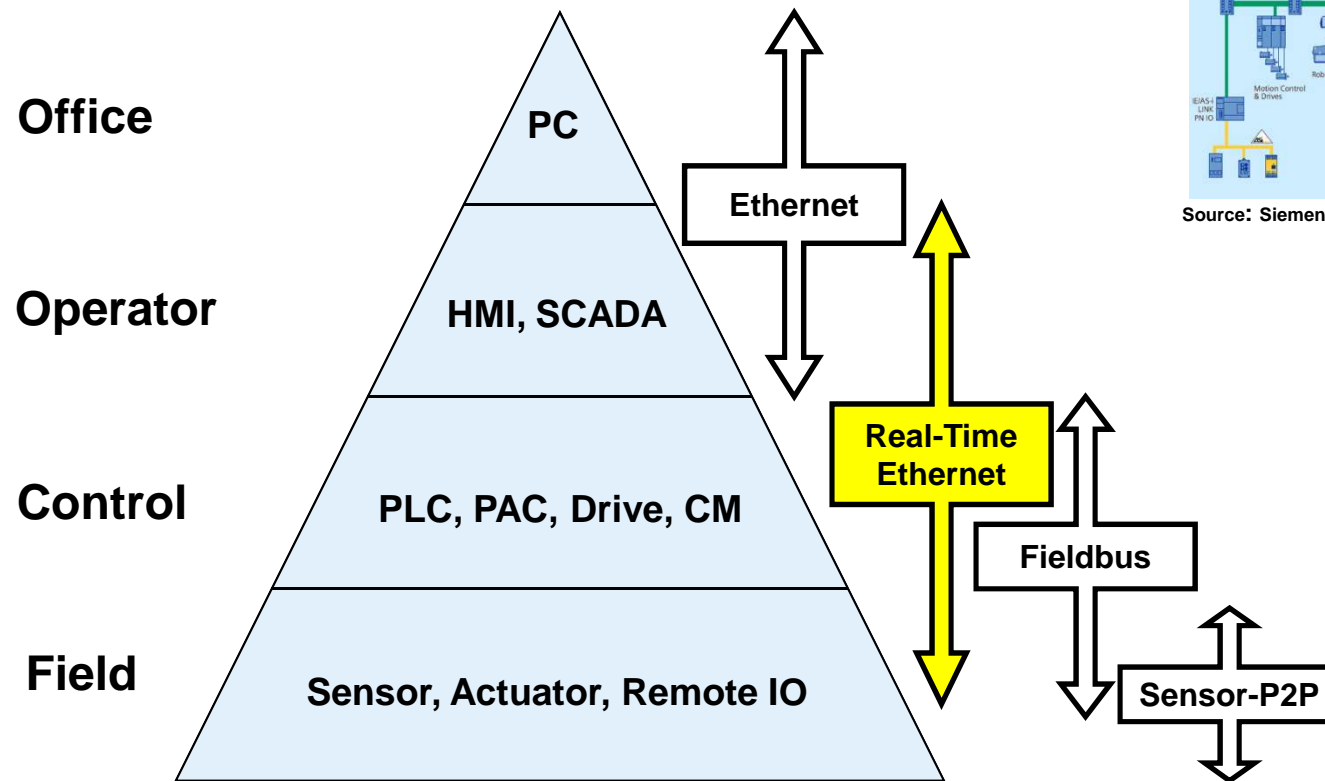
- Power Protection Systems, Test & Measurement, SDR, Bar Code Scanners, Portable Communications, Portable Medical, Portable Audio



Industrial Automation Architecture

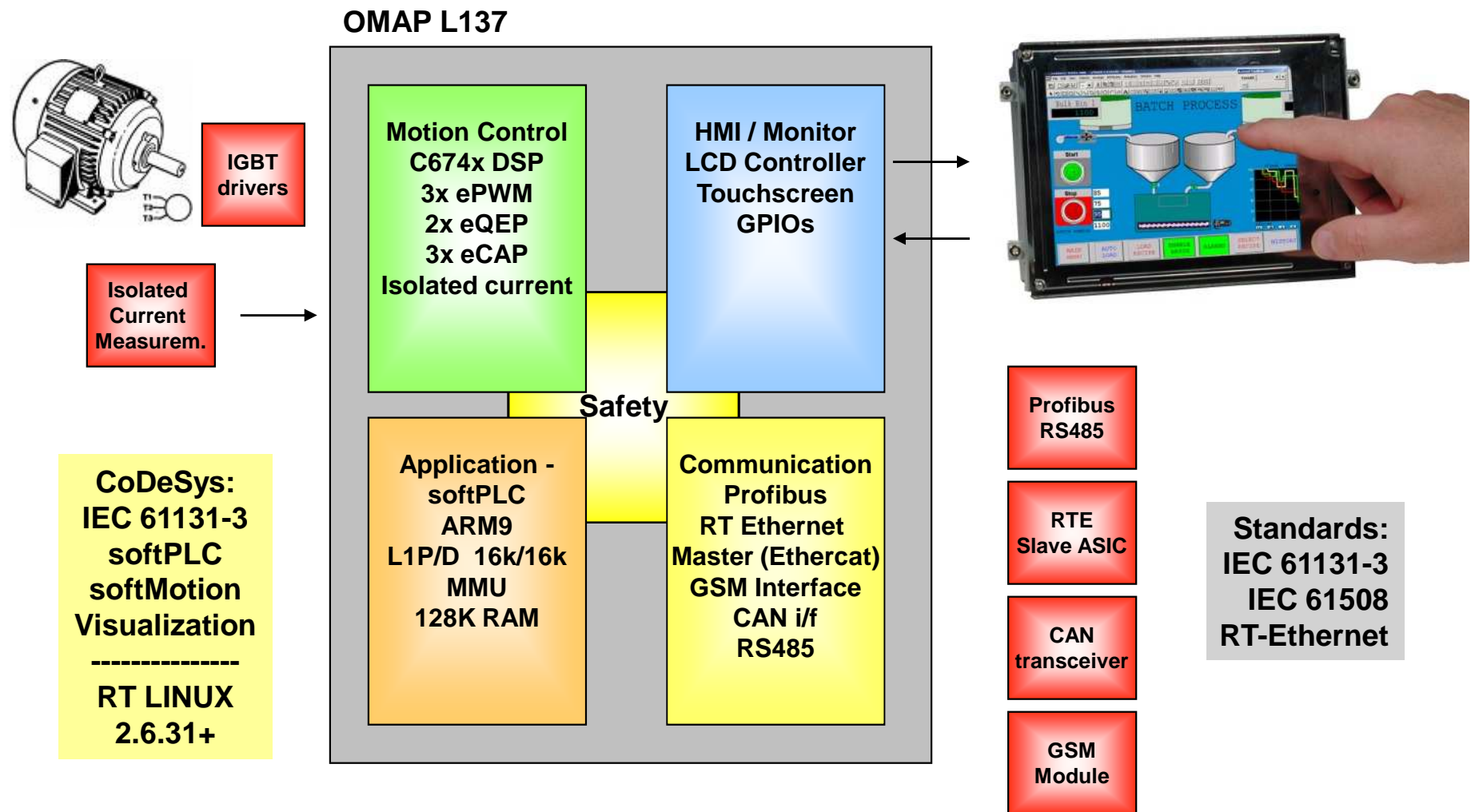


Industrial Automation Pyramid

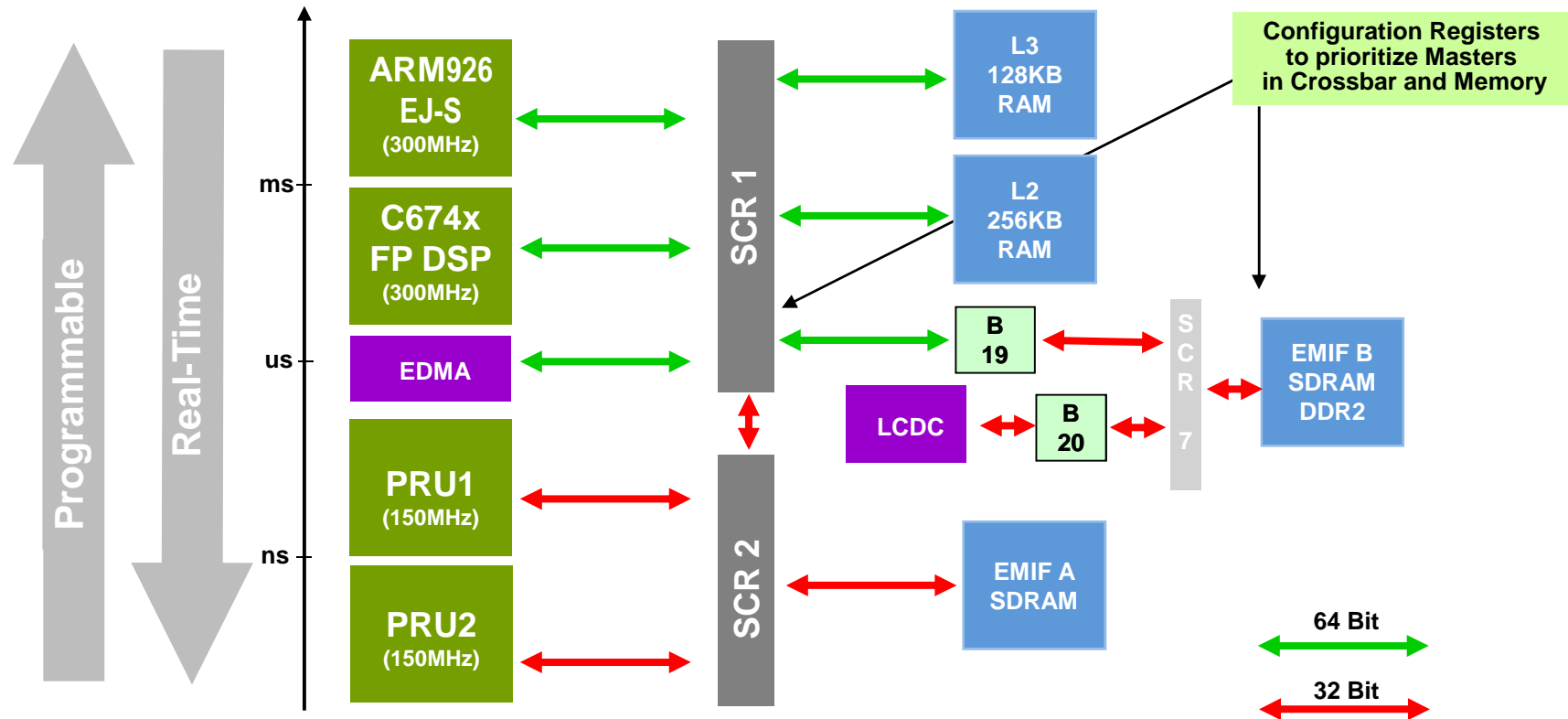


Source: Siemens

Programmable Automation Controller



OMAP L1 Multi-Core Architecture



“Multi-Issue” Switched Central Resource 1 has 12x4 crossbar with 64 bit path at 150MHz.

With concurrent operation of up to 4 slaves the peak throughput is 4,8 GB/s!

OMAP L1 vs x86

Core SoC	ARM926 OMAP L1	C674x OMAP L1	PRU1 OMAP L1	PRU2 OMAP L1	x86 + “Northbridge”
MHZ	300	300	150	150	1600
Cache, Local Memory	16k I, 16k D, 8K RAM, 64 K ROM	32 k I, 32 k D 256k L2 1M L2 ROM	4K I, 512 D	4k I, 512 D	24k I, 32k D 512k L2
Multiscalar	1	8, 2.4 GMAC, 1.8 GFLOPS	1	1	2 HT SSE3
Pipeline	5	13	0	0	16
Interconnect	“multi issue” SCR1 4,8 GB/s		“single issue” SCR2		FSB 3,2 GB/s
Power Consumption	SoC < 500 mW				Incl. Chip Set < 5 W
Form Factor	13x13 mm (0.65 pitch) 16x16 mm (0.8 pitch)				13x14 mm + 22x22 mm (NB)

OMAP L1 competes against x86 through flexibility, high level of integration and Interconnect

Industrial Communication

IA-COM



Industrial Communication Standards

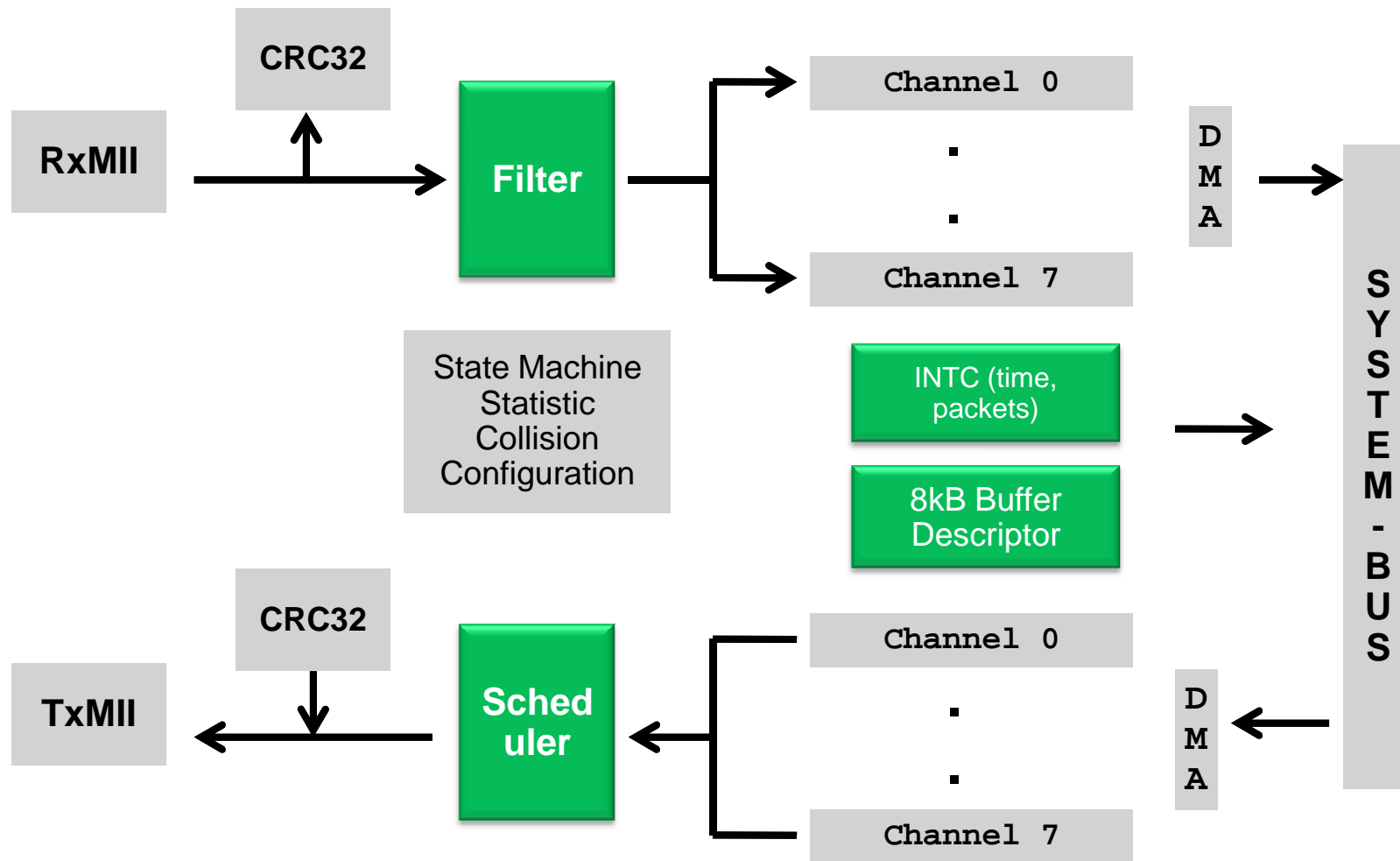
- Industrial Ethernet
 - **EtherCAT**
 - Ethernet/IP
 - ProfiNet
 - ... (28 standards)
- “Serial Fieldbus”
 - **ProfiBus**
 - Interbus
 - Controller Area Network (CAN)
 - Modbus
 - ...
- Sensor Interface
 - ASi Bus
 - **IO-Link**
 - HART

Industrial Ethernet - Overview

Features	Ethernet (IEEE)	Industrial Ethernet
Standard	IEEE802.3 (Cisco) CSMA/CD (EMAC) 10Mbit-10Gbit Half/Full duplex Unicast, multicast, broadcast VLAN, Rapid Spanning tree (QoS)	Profinet (PNO/Siemens) Ethernet/IP (ODVA/Rockwell) EtherCAT (ETG/Beckhoff) Powerlink (EPSG/ B&R) Sercos III (Sercos/Bosch Rexroth) Modbus TCP (Modbus-IDA/Schneider)
Time Sync	IEEE 1588	IEEE 1588 PTP, Distributed clocks
Min Cycle Time (PLC application)	> 10ms	31 us, 62us, 250us, 1ms
Jitter (>100 nodes)	>1 ms (MAC Fifo, stack software)	+/- 20ns (timer resolution, phy jitter)
Latency per node (line 2 line)	10us (switch)	700ns, 1 us, 3.5us (cut through switch)
Throughput RTE	< 100 Mbit (limited by host performance)	100 Mbit (hardware supported)

16

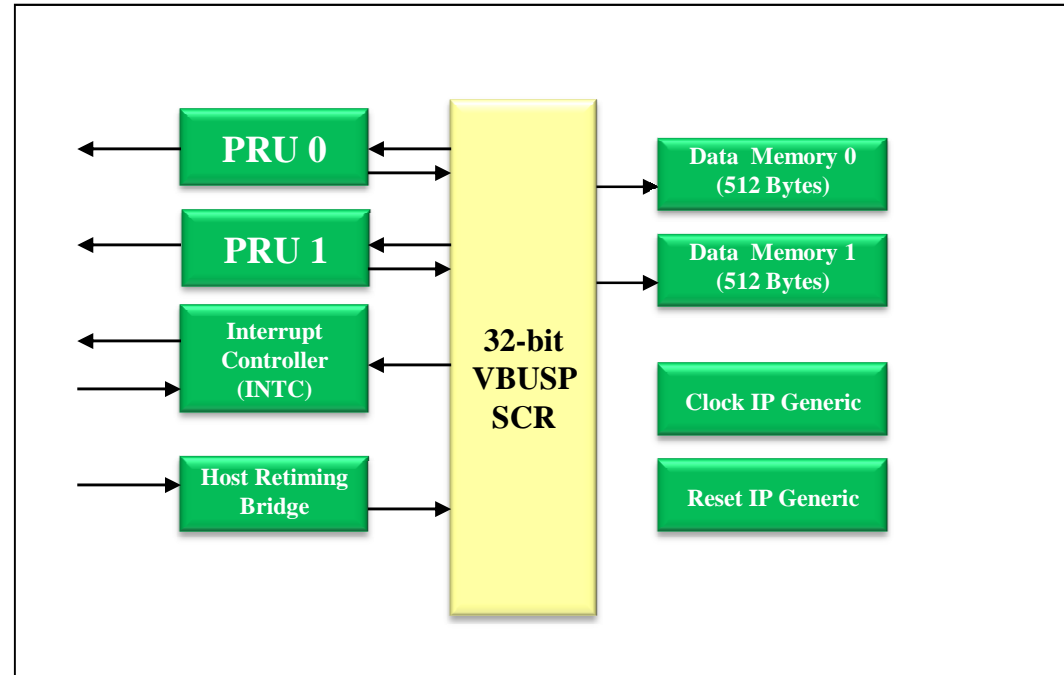
TI Ethernet MAC – MultiChannel QoS



PRU Subsystem on OMAP L1/AM1x

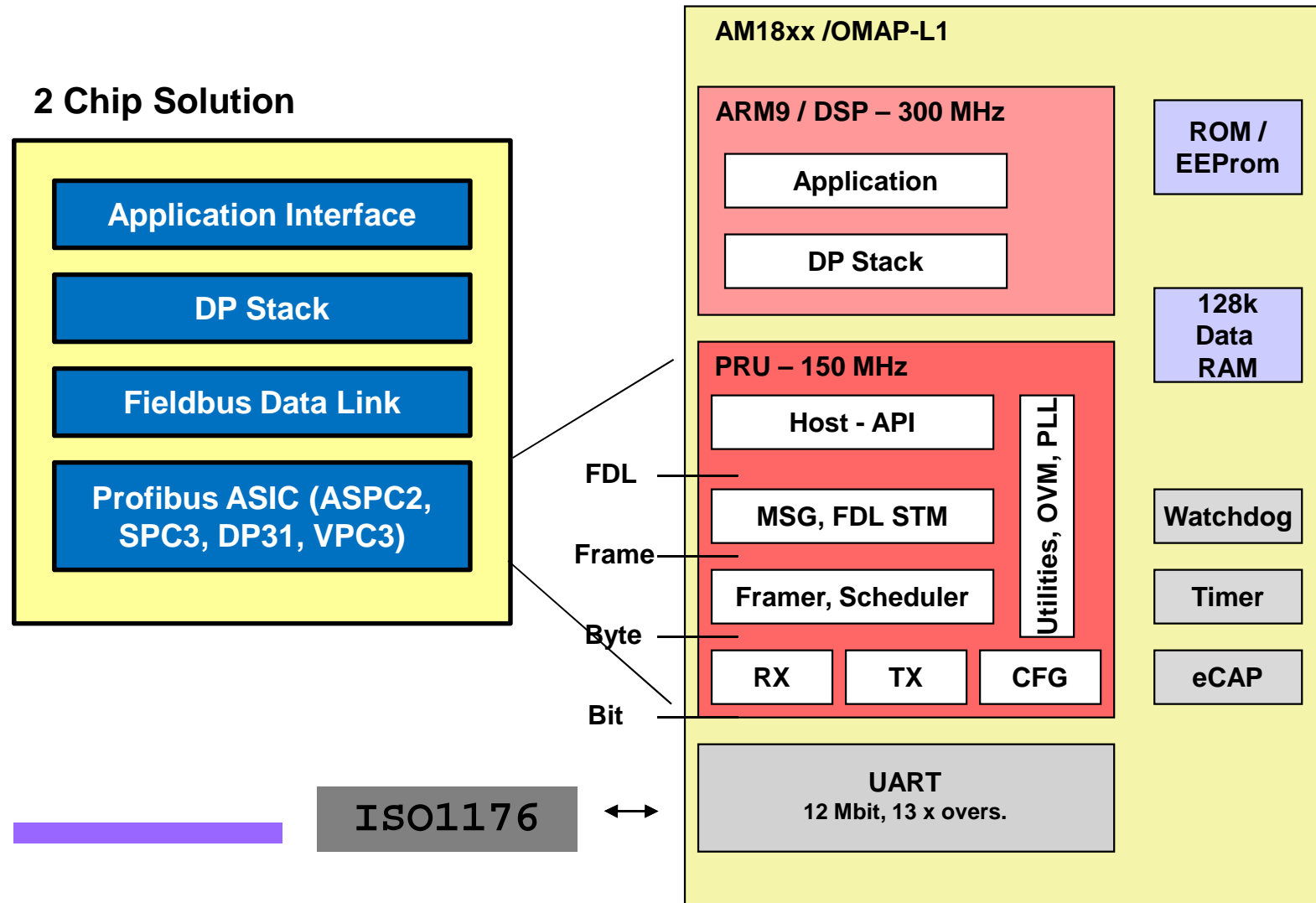
➤ Provides 2 Independent Programmable Realtime Units (PRU)

- ❑ 32-Bit Load/Store RISC architecture
- ❑ 4K Byte instruction RAM per core
- ❑ 512 Bytes data RAM per core
- ❑ Register 30 of each PRU is exported from the subsystem in addition to the normal R31 output of the PRU cores.
- ❑ Each core runs at half of main processor speed (150MHz)

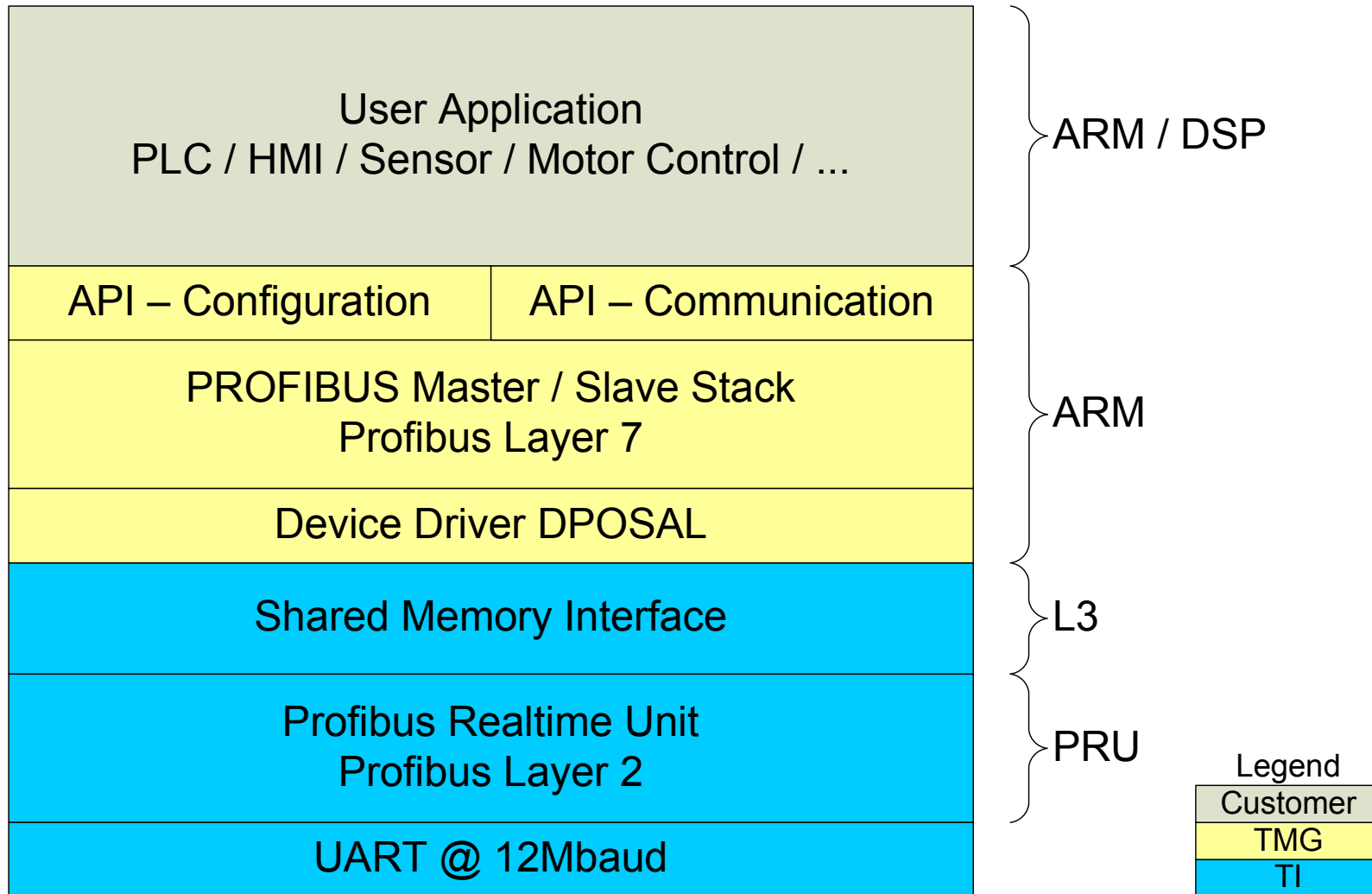


- PRU intended operation is little endian similar to ARM and DSP processors.
- Provides standard power management mechanism
- ❑ PRU can be disabled via software to save power
 - ❑ Entire subsystem under a single PSC clock gating domain
- Provides interrupt controller for system events handling(No vectorization supported)

Profibus DP Integration with PRU



SW Layer Architecture Block Diagram

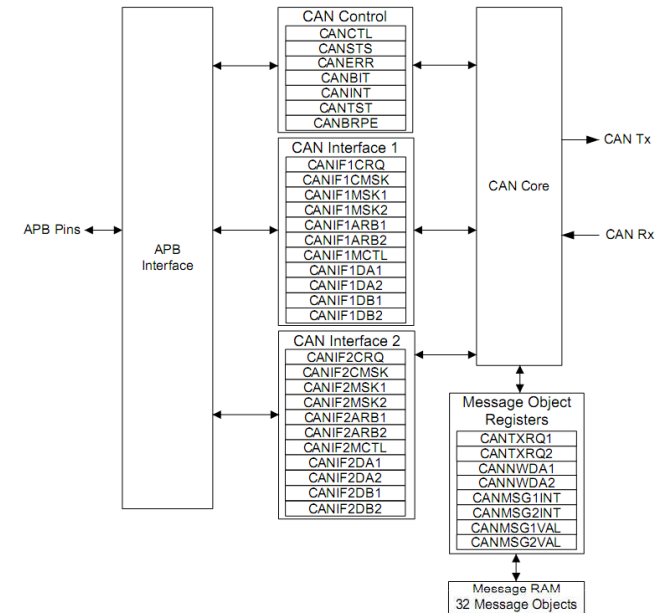


PROFIBUS Solutions in the Market

SoC	AM1810	Hilscher NetX50	Siemens SPC3	ProfiChip VPC3+S
Description	Profibus DP (v0, v1, v2(TBD)) Slave and Master; 12Mbps	PROFIBUS, Master, Slave	Profibus DP (v0, v1, v2) Slave; 12Mbps	Profibus DP (v0, v1, v2) Slave; 12Mbps
Processor	385/312MHz ARM926E	200MHz ARM966E	NA	NA
Host Interface	seamless integrated (SCR)	integrated	parallel	SPI, IIC, parallel
Power Consumption Profibus only	20mW (PRU, eCAP, UART)	NA	NA	160mW 48mA @ 3.3V
System	<182mW @ 300MHz, 1.2V, 25C	800 to 1200mW		
Form Factor	13x13mm	19x19	10x10mm (TQFP 44pin)	6x8mm (BGA 48pin)

CAN Integration

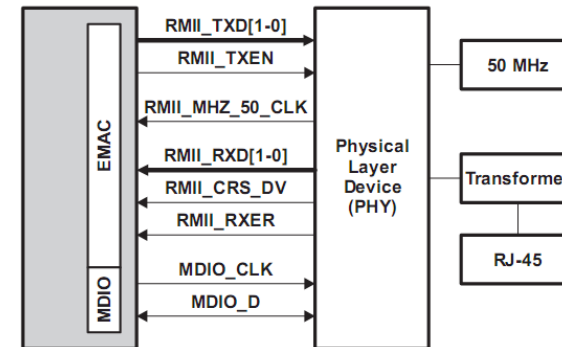
- HW:
 - Dedicated CAN Controller(s)
 - CAN 2.0A/B support
 - CAN transceiver
- SW:
 - Device driver for OS
 - CANopen, DeviceNet – highlevel stack
- Devices:
 - AM3505/17
 - Stellaris family with Cortex-M3 cores
 - C2800 family of MCUs
 - ISO 1050 CAN transceiver



EtherCat Master Integration



- HW:
 - Standard Ethernet port(s)
 - Integrated EMAC/Phy
- SW:
 - Standard Ethernet driver – silicon vendor/open source
 - EtherCAT master stack – SW third party
 - 3S/CoDeSys
 - OSADL
- Devices:
 - AM3505/17
 - AM18xx/17xx
 - TLK100 Industrial Ethernet PHY



EtherCAT Master & CoDeSys

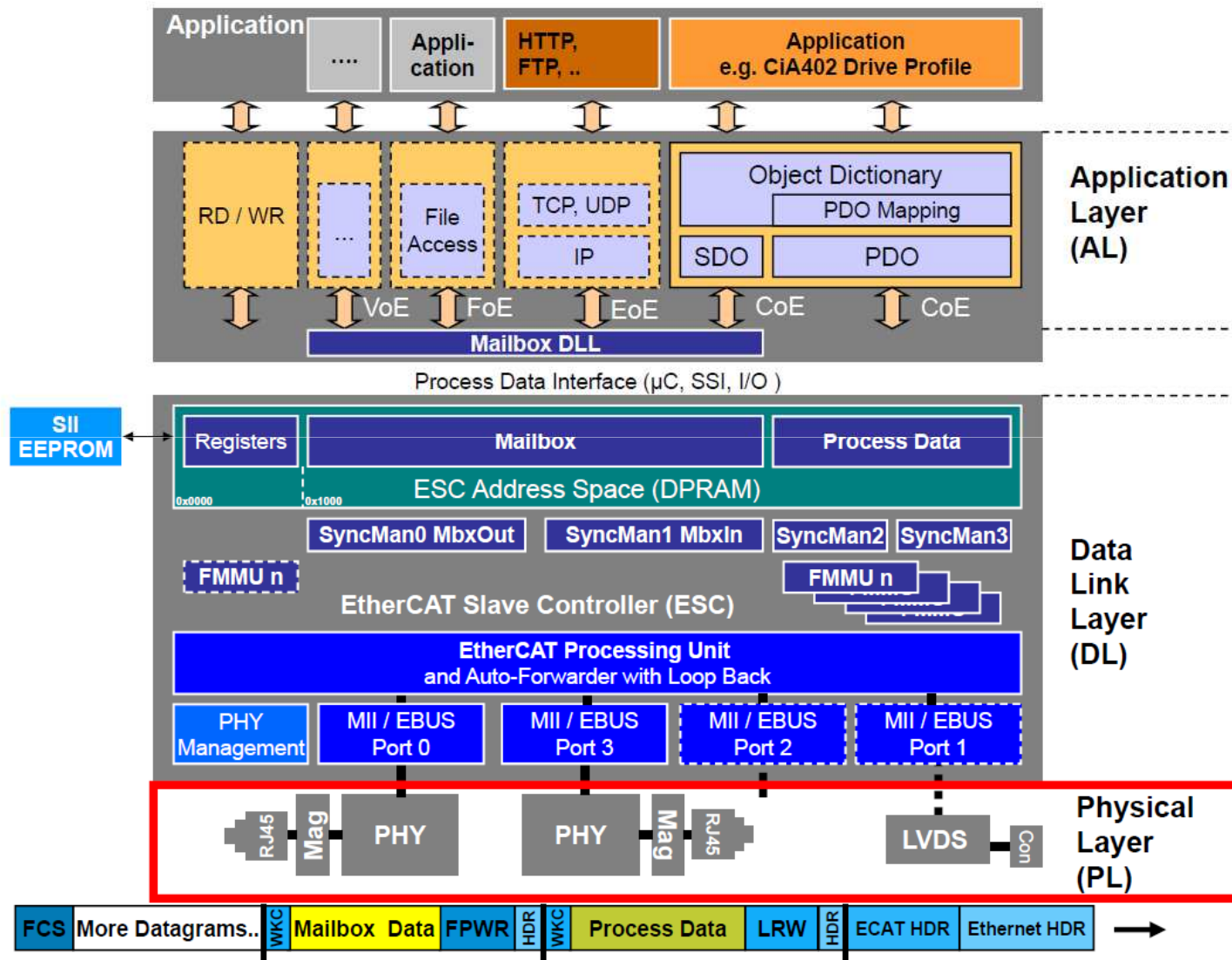
The screenshot displays the CoDeSys IDE interface for a project named "EthCatLinu_eval.project". The left pane shows the project tree with the following structure:

- EthCatLinu_eval
 - Device (CoDeSys SP Lin V3 - TI)
 - PLC Logic
 - Application
 - Library Manager
 - PLC_PRG (PRG)
 - Task Configuration
 - EtherCAT_Master
 - MainTask
 - EtherCAT_Master (EtherCAT Master)
 - EK1100 (EK1100 EtherCAT Coupler (2A E-Bus))
 - EL1004 (EL1004 4Ch. Dig. Input 24V, 3ms)
 - EL2004 (EL2004 4Ch. Dig. Output 24V, 0.5A)
 - EK1100_1 (EK1100 EtherCAT Coupler (2A E-Bus))
 - EL3001 (EL3001 1Ch. Ana. Input +/-10V)
 - EL4001 (EL4001 1Ch. Ana. Output 0-10V, 12bit)

The right pane shows the PLC Logic for the "Application" task, with tabs for "EL1004" and "EL3001". The logic is as follows:

```
1 PROGRAM PLC_PRG
2 VAR
3     IN1: BOOL;
4     IN2: BOOL;
5     IN3: BOOL;
6     IN4: BOOL;
7
8 cycle := cycle + 1;
9 OUT1 := NOT(IN1);
10 IF IN1 THEN
11     OUT2 := state2;
12     state2 := NOT(state2);
13 END_IF;
14 IF state2 THEN
15     OUT3 := state3;
16     state3 := NOT(state3);
17 END_IF;
```


EtherCAT Slave - Architecture



EtherCat Slave Integration



- HW:
 - EtherCAT unit with 2 ports, FMMU and SyncManager
 - Distributed Clocks and Shared Memory support
- SW:
 - EtherCAT driver
 - Data Link Layer implementation
 - Provided by silicon vendor
 - EtherCAT slave stack
 - Application layer implementation
 - Provided by SW third party/user
- Devices:
 - TLK100 (listed in Beckhoff application note)
 - Future C2000, Stellaris and Sitara devices

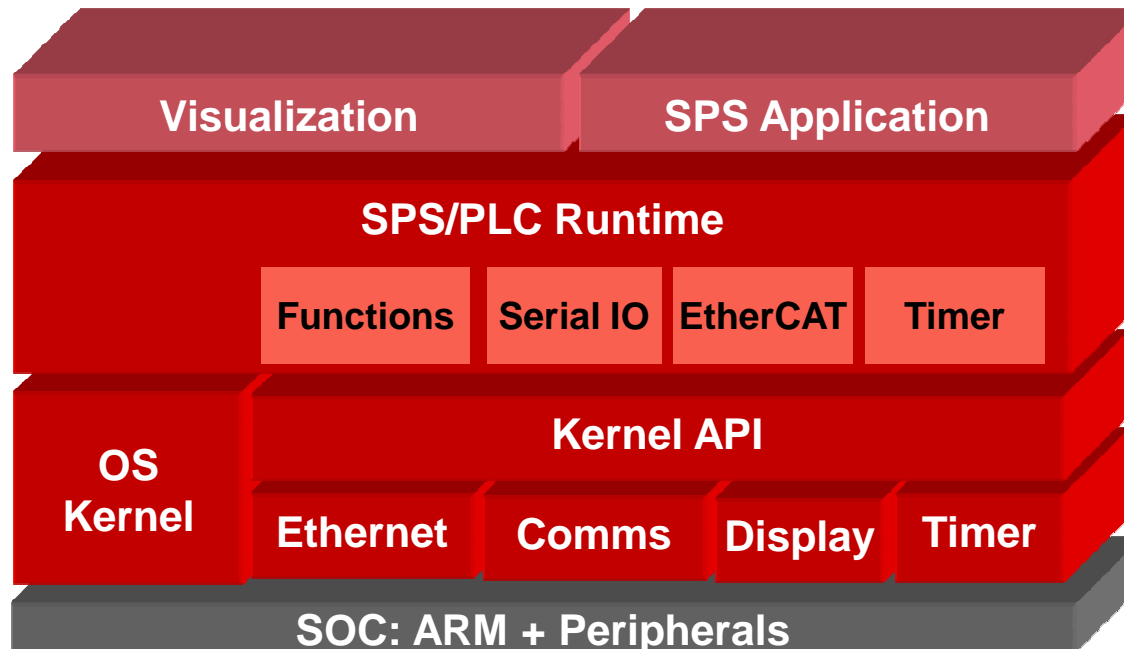
Programmable Logic Controller

SPS/PLC



Source: 3S

SPS/PLC Architecture

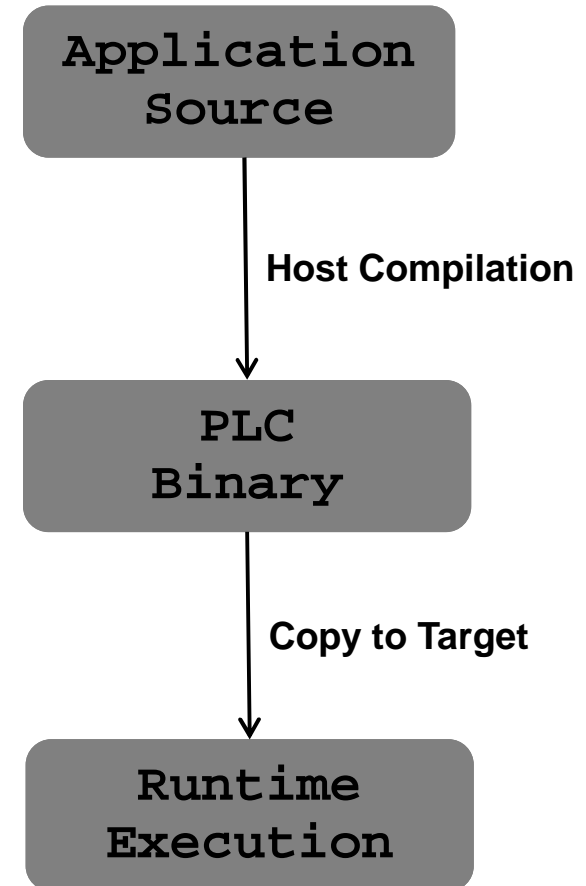


Performance Criteria

- Master Cycle Time
- Interrupt Latency
- SPS Performance - Integer/Float/LD+ST Operations

PLC Application Development Flow

- IEC 61131-3
 - 7 graphical and textual programming languages
- CoDeSys by 3S
 - Host development and debug tool
 - ARM runtimes & compiler
- Communication stacks
 - CAN
 - EtherCAT



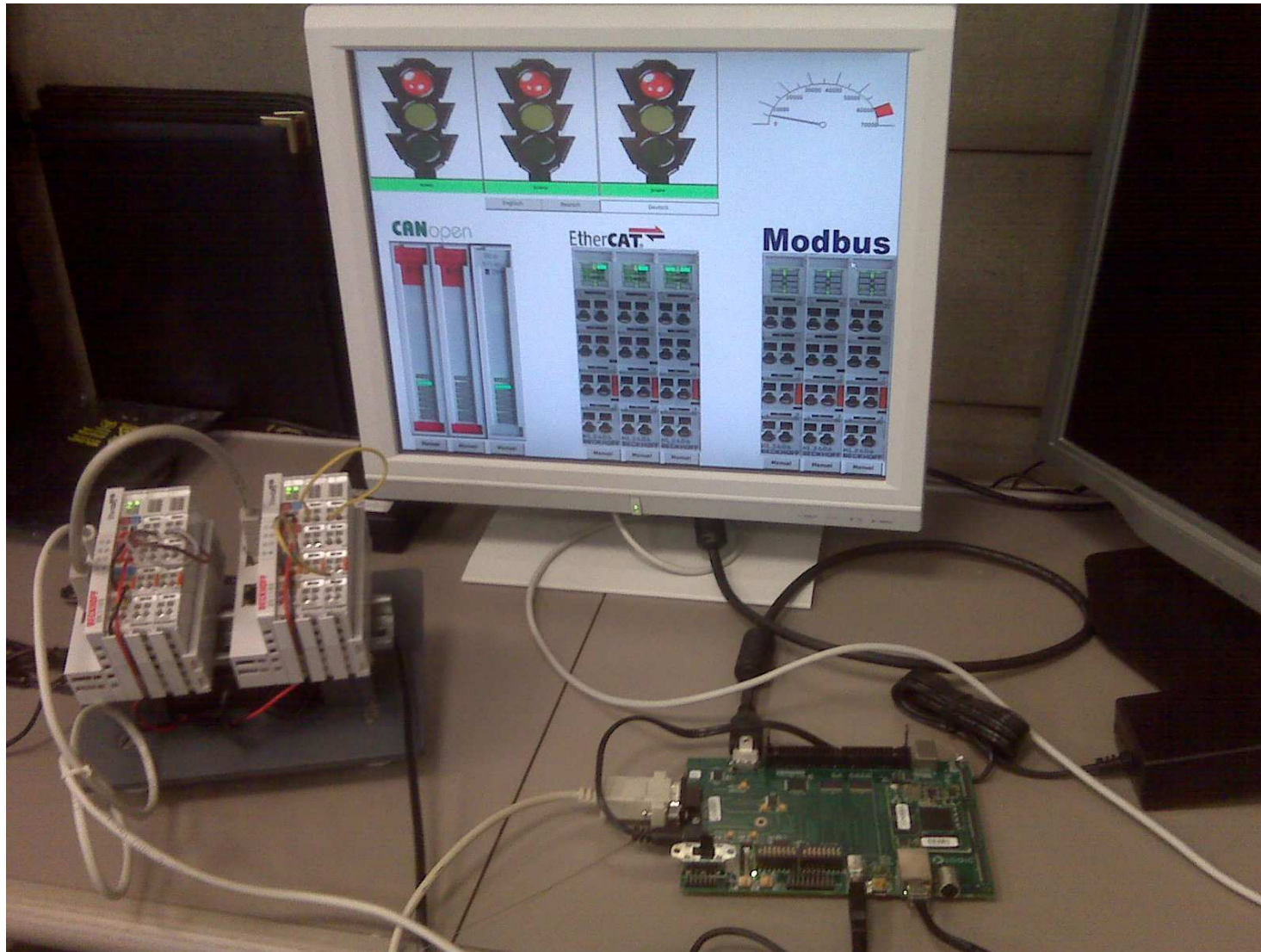
CoDeSysSP on TI devices

- Demonstrator or System packages
 - E.g. AM3517 EVM based demo for evaluation
 - Board vendor packages
- Customer integration
 - TI: hardware support
 - 3S: CoDeSys licensing & support
 - Third party: integration support
- CoDeSysSP v3.4 runtime availability:
 - Cortex-A8 (OMAP3/AM35xx)
 - ARM9 (AM17xx/18xx/OMAP-L1xx)
 - Cortex-M3 (Stellaris family)
 - C28xx (Digital Signal Controller)


CoDeSysSP on Stellaris-M3



CoDeSysSP on AM3517

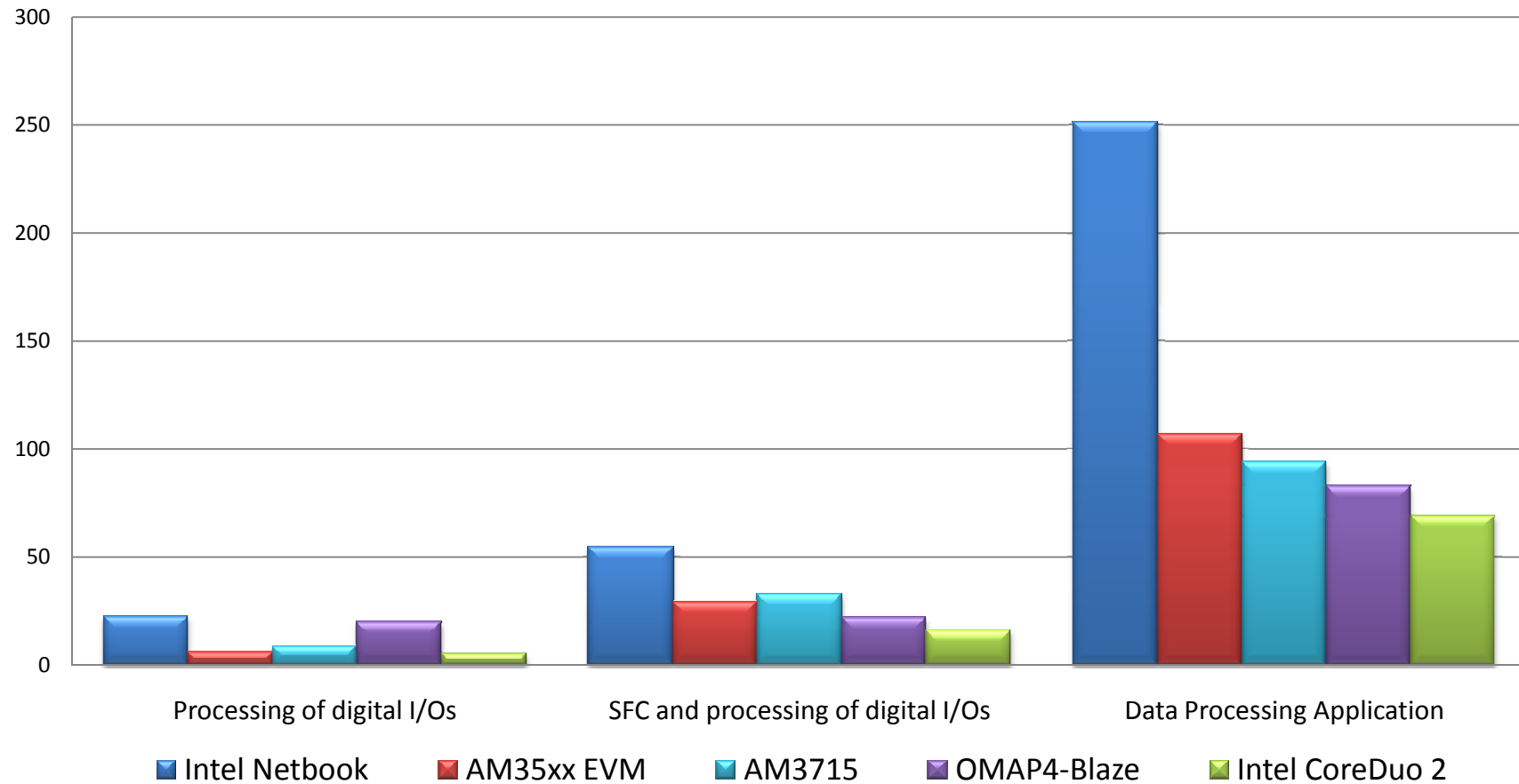


CoDeSys Benchmark

PLC Benchmarking Report									
TI Information - Selective Disclosure					 TEXAS INSTRUMENTS				
AM35xx EVM				CoDeSys runtime v 3.4 SP1					
Tested by:		Frank Walzer			Test date:		25.09.2009		
Results Table									
		AM35xx EVM					AM3715		
Execution time [us] Benchmark		Min.	Max.	Average	Size [bytes]	Min.	Max.	Average	Size [bytes]
Application oriented									
Processing of digital I/Os		0	122	12		0	30	9	
SFC and processing of digital I/Os		30	213	59		0	92	33	
Data Processing Application		183	306	214		91	122	94	
Language oriented									
POU calls		244	457	284		122	213	158	
Function block		152	275	174		61	92	64	
Function		122	275	147		61	91	64	
ST Control Statements		2349	2960	2506		1159	1465	1251	
CASE		30	213	57		30	61	33	
FOR		91	396	141		61	214	82	
IF		30	183	36		0	91	18	

Benchmark Results – Example Graph

CoDeSys V3.4 Execution Time [μ s]
(scaled to 1GHz, 10000 runs average)

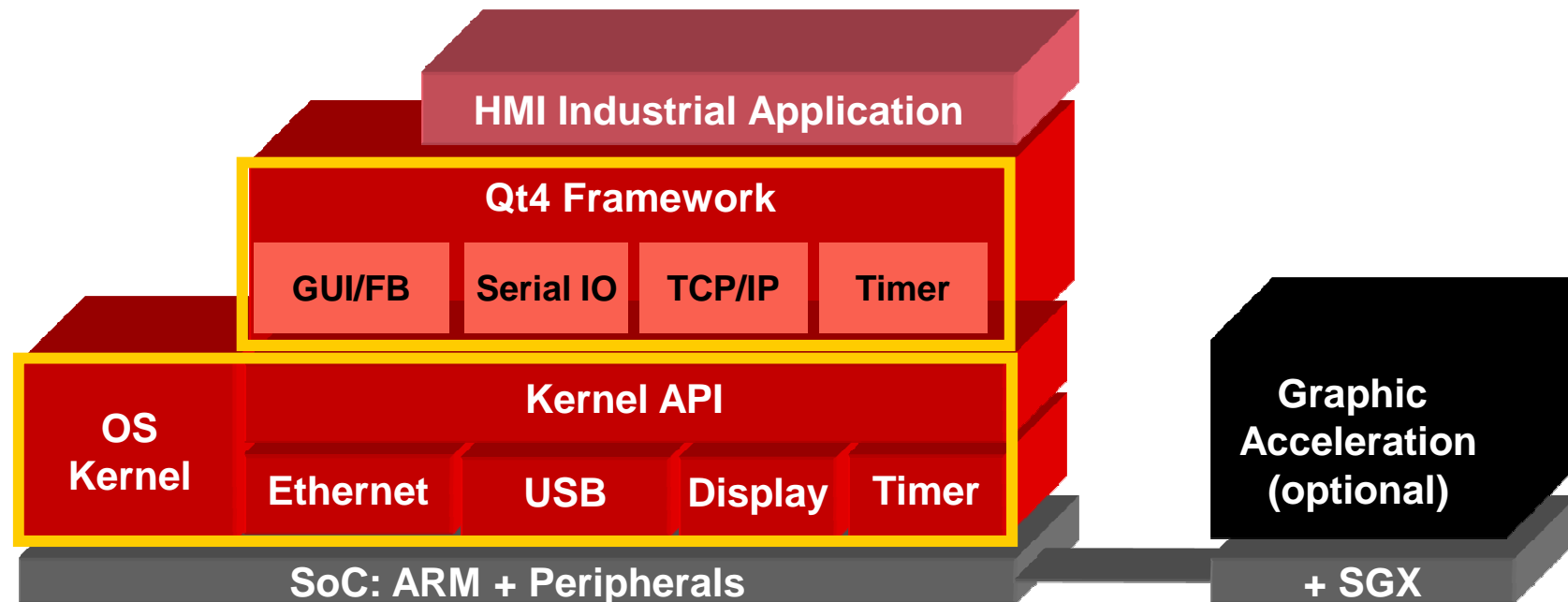


HMI

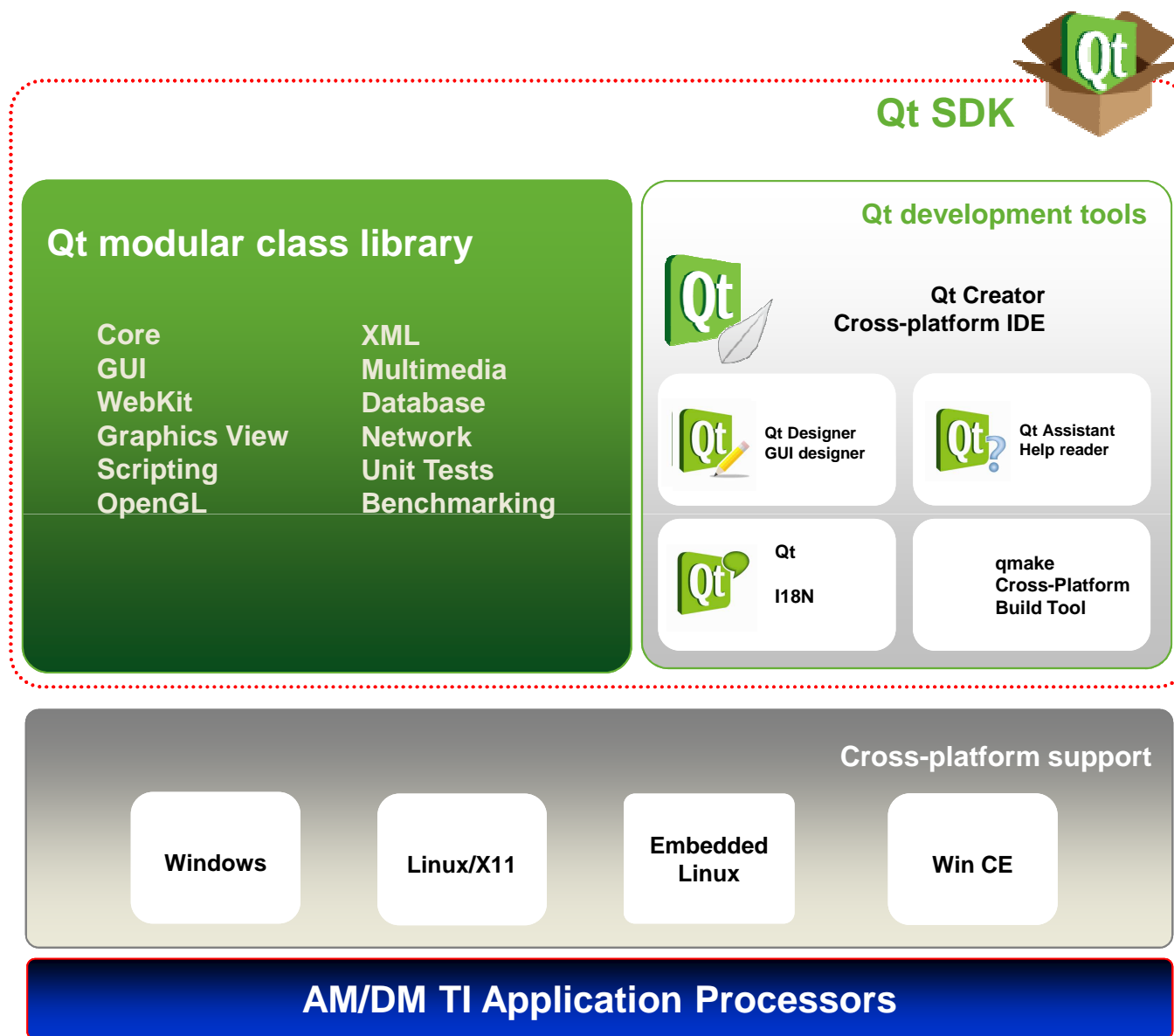


HMI Applications

- ▶ OS: Embedded Linux Kernel 2.6.xx or Microsoft Windows CE 6.0 R3
- ▶ Qt 4.6.x framework abstracts OS API
- ▶ Application program using C++ Object Oriented Programming
- ▶ Debug on other platforms due to Qt4 cross-platform support
- ▶ High abstraction on application level leads to fast development



Qt SDK

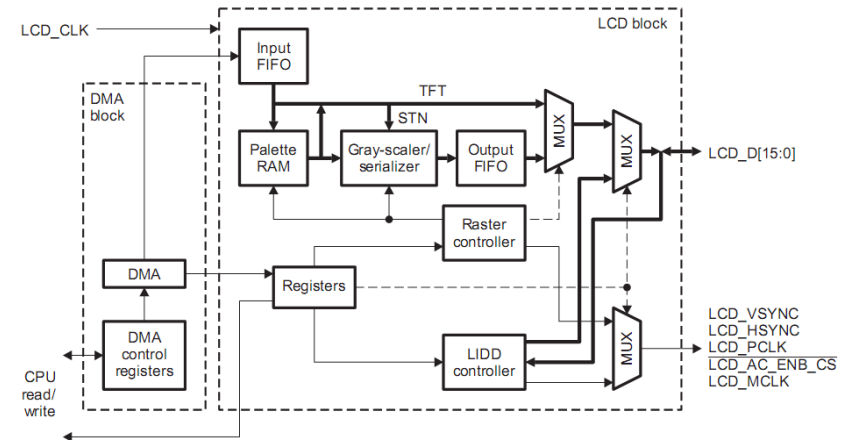


Qt Application Framework

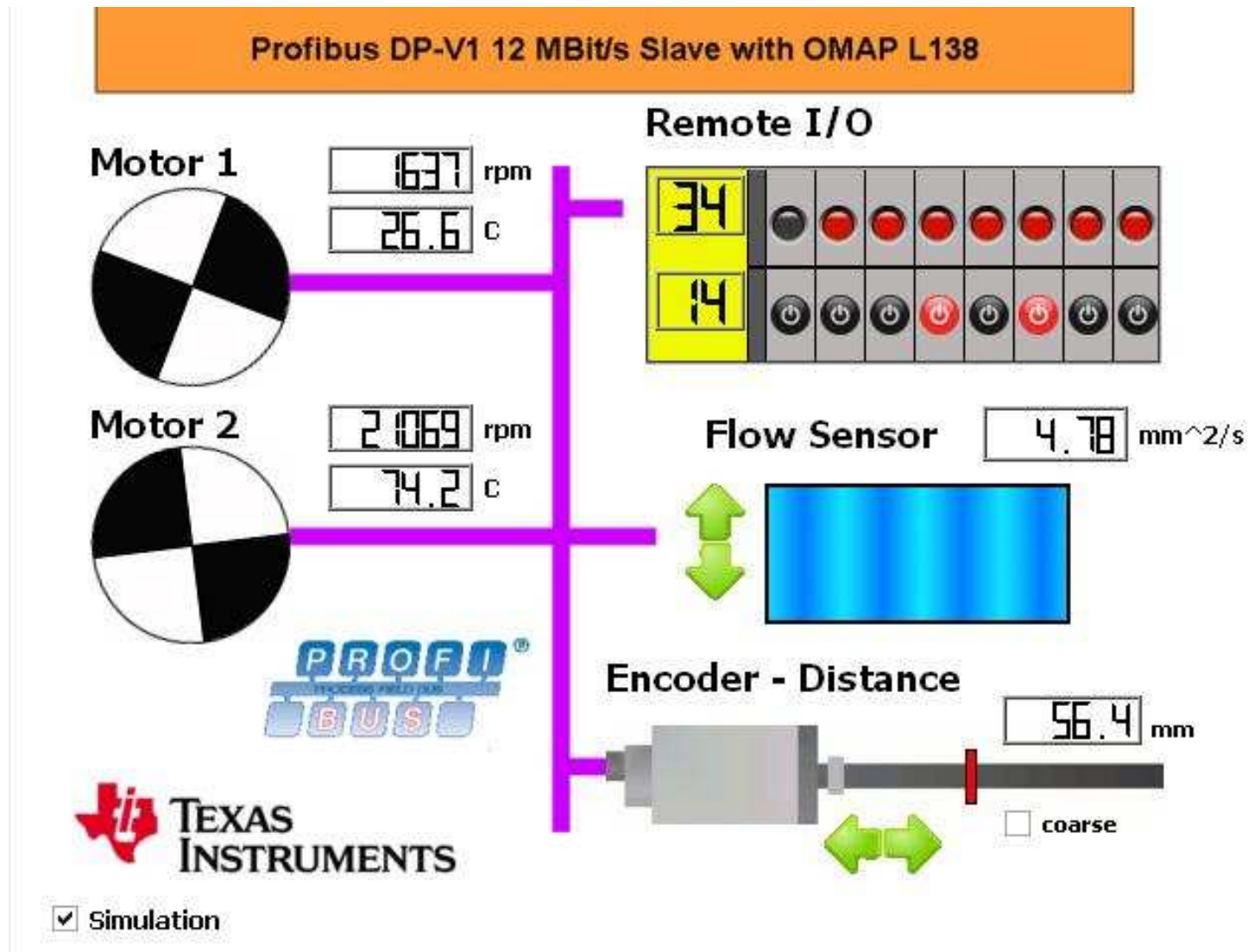
- Rich feature set due to ~800 C++ classes
 - Windows, widgets, buttons,...
 - Ethernet, Web browser, animation,...
- Embedded Linux support
 - Ported to all TI embedded processors
 - Easily configurable for custom targets
 - Well documented process
- Free dedicated development tools
 - Qt Creator – full featured IDE
 - Qt Designer – graphical GUI design
 - Eclipse & Visual Studio plugins – standard tools integration
 - Build process support
- Open Source – LGPLv2

HMI Integration

- HW:
 - LCD Controller
 - DMA support
- SW:
 - Device driver for OS
 - High-Level Graphics – open source
 - Possible combination with SPS/PLC
- Devices:
 - AM3505/17 – 24 bit color, high resolution
 - AM17xx/18xx – 16 bit color, medium resolution
 - Stellaris family with Cortex-M3 cores - small displays

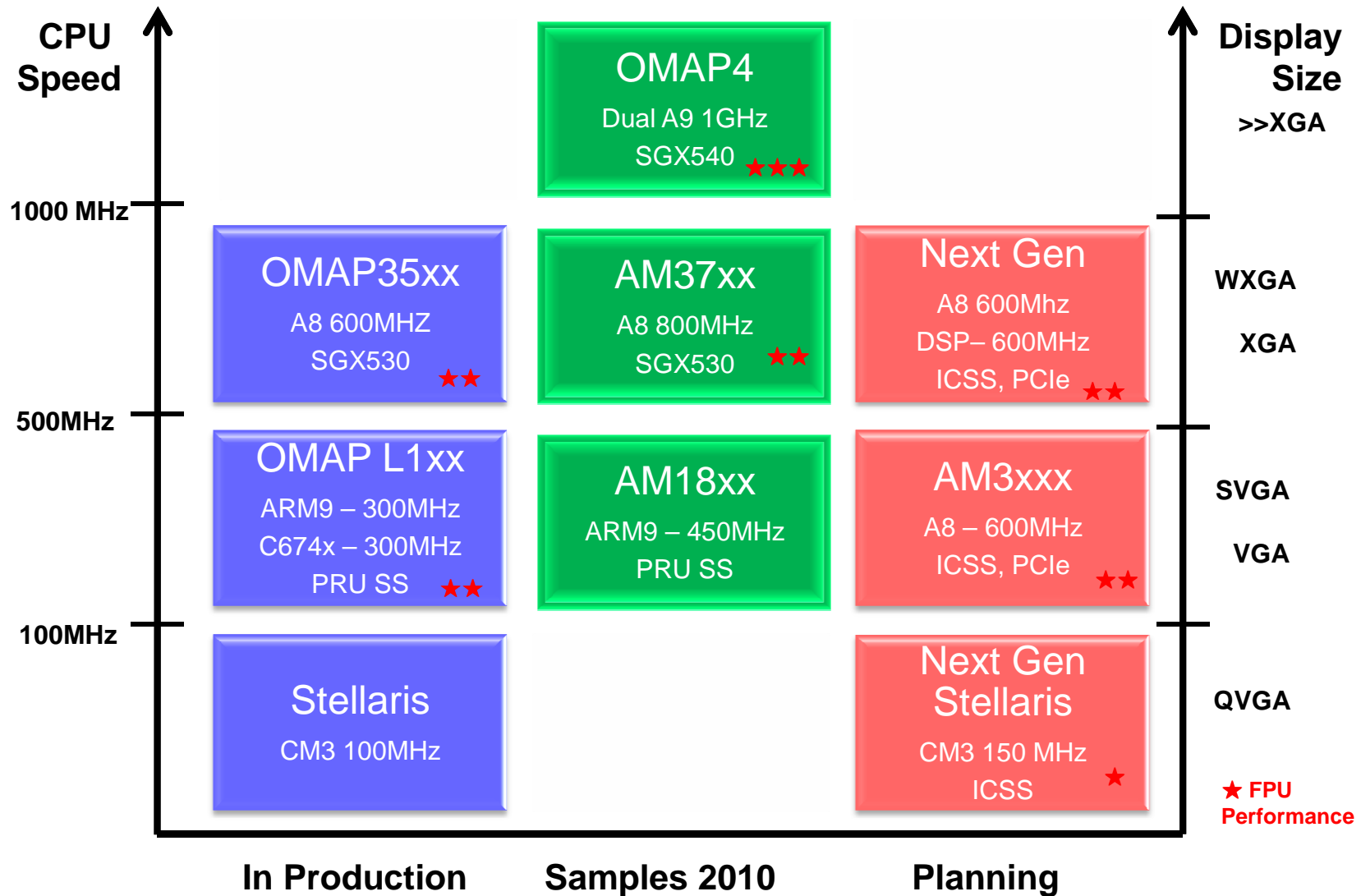


ProfiBus Demo



ROADMAP

Industrial Control/HMI Roadmap



Industrial Automation Software Solutions

Operating System

Linux
WinCE
QNX
VxWorks
Integrity
freeRTOS
eCos
DSP BIOS
custom

Applications Level Software

Sensor

Drive

Remote
IO

PLC /
PAC

HMI

Gateway

Middleware

Virtual
Machine
(PLC, Java)

Graphics
Framework
(Stellarisware,
Qt, X11)

Communication
Stacks
(TCP/IP,
CANopen,
Profibus,..)

Control
Libraries
(DMC, Digital
Power, ..)

Device Driver

Memory

Serial
Interfaces

Fieldbus
(CAN,
Profibus)

Industrial
Ethernet

Control
(PWM,
CAP,QEP)

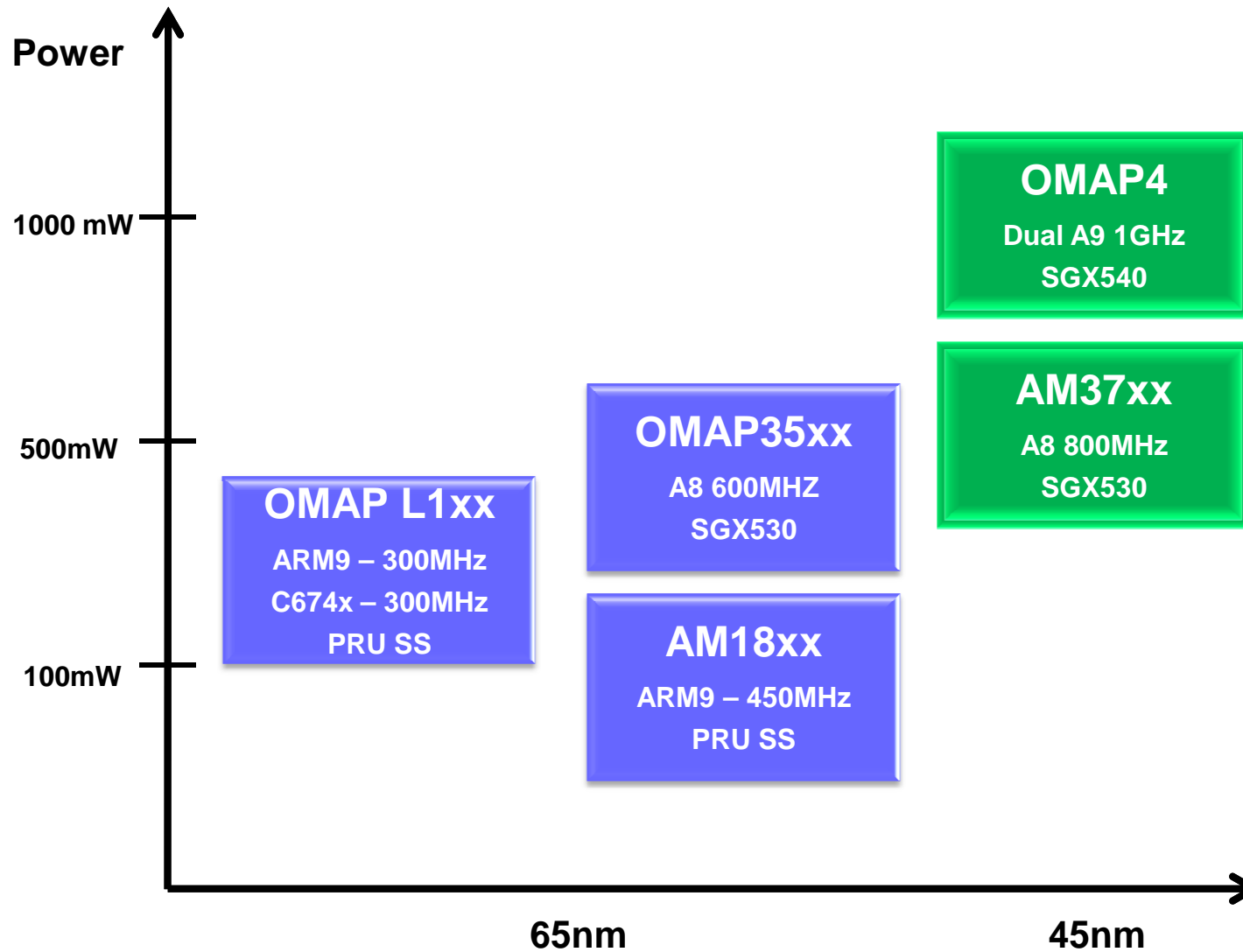
Display
(framebuf,
DSS)

 TI Base
Support
Package

 Open Source / 3rd
Party / TI

 3rd party /
Customer

ARM MPU - Power Consumption



THANK YOU!