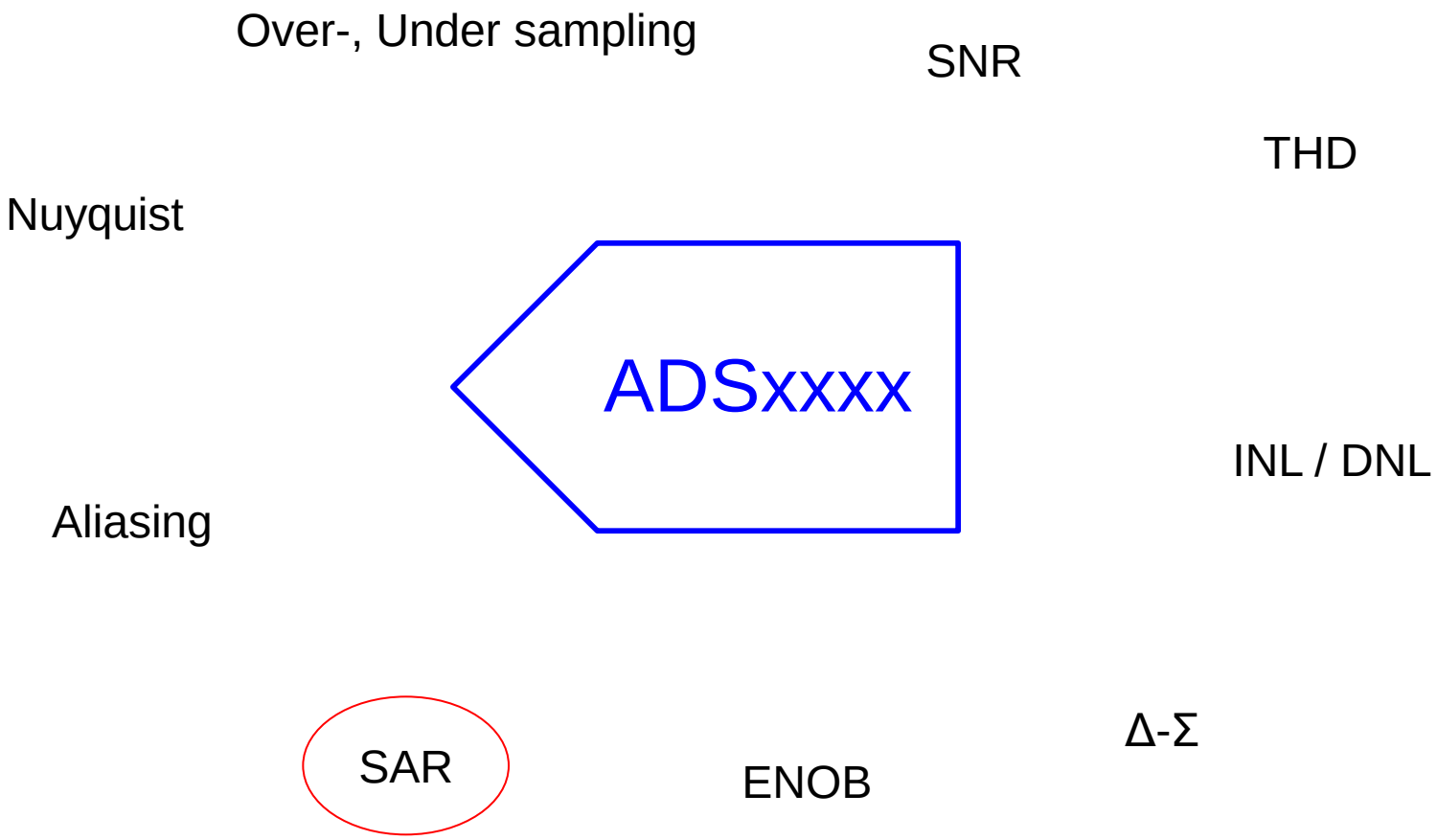
TI Technology Days 2010

How to drive your AD-Converter?

Katharina Berberich

Carsten Schlegel

Analog to Digital Conversion



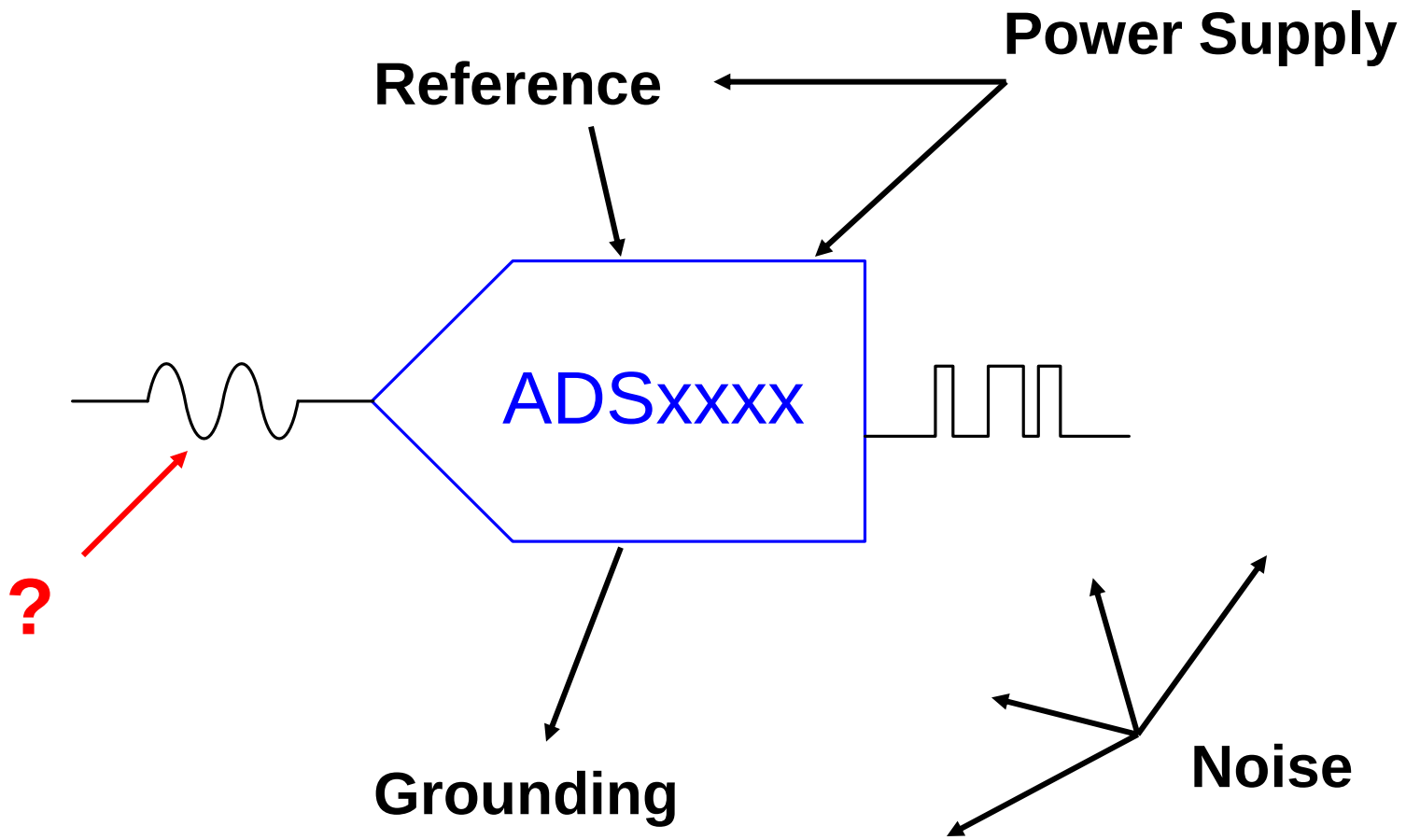
The Size of the Least Significant Bit (LSB)

RESOLUTION N	2^N	VOLTAGE of LSB (10V FS)	ppm FS	% FS	dB FS
2-bit	4	2.5 V	250,000	25	-12
4-bit	16	625 mV	62,500	6.25	-24
6-bit	64	156 mV	15,625	1.56	-36
8-bit	256	39.1 mV	3,906	0.39	-48
10-bit	1,024	9.77 mV (10 mV)	977	0.098	-60
12-bit	4,096	2.44 mV	244	0.024	-72
14-bit	16,384	610 µV	61	0.0061	-84
16-bit	65,536	153 µV	15	0.0015	-96
18-bit	262,144	38 µV	4	0.0004	-108
20-bit	1,048,576	9.54 µV (10 µV)	1	0.0001	-120
22-bit	4,194,304	2.38 µV	0.24	0.000024	-132
24-bit	16,777,216	596 nV*	0.06	0.000006	-144

*600nV is the Johnson Noise in a 10kHz BW of a 2.2kΩ Resistor @ 25 C

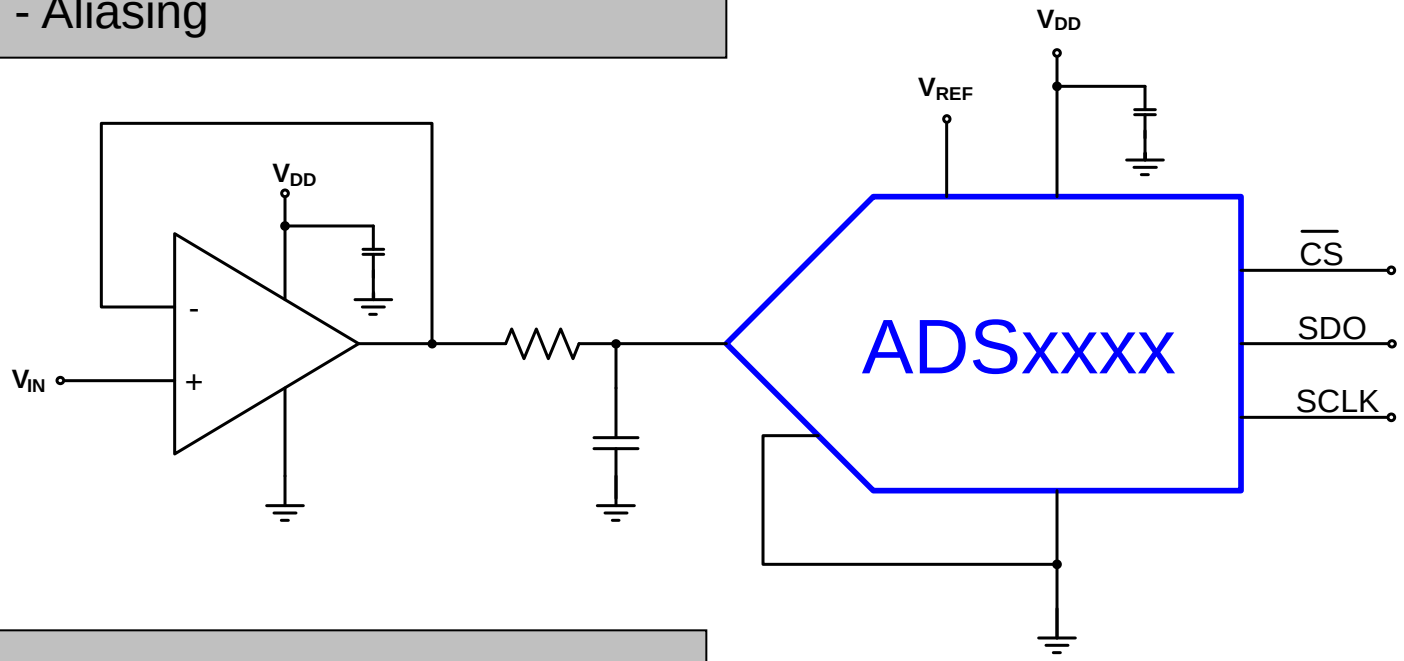
Remember: 10-bits and 10V FS yields an LSB of 10mV, 1000ppm, or 0.1%.
All other values may be calculated by powers of 2.

Analog to Digital Conversion



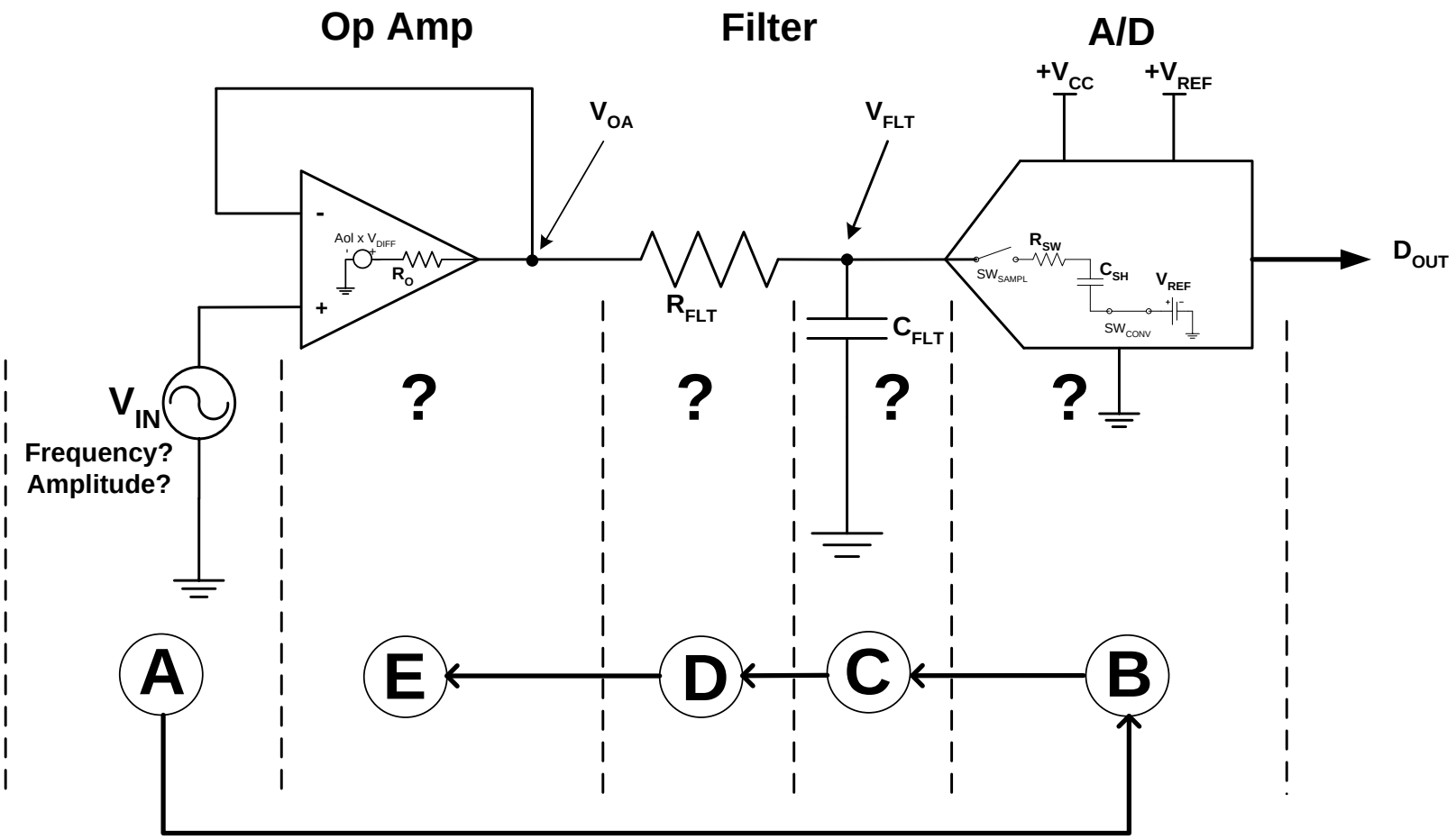
Typical ADC Input Drive Circuit

- Signal conditioning
- Adaptation to ADC input range
- MUX, Range extension
- Anti - Aliasing

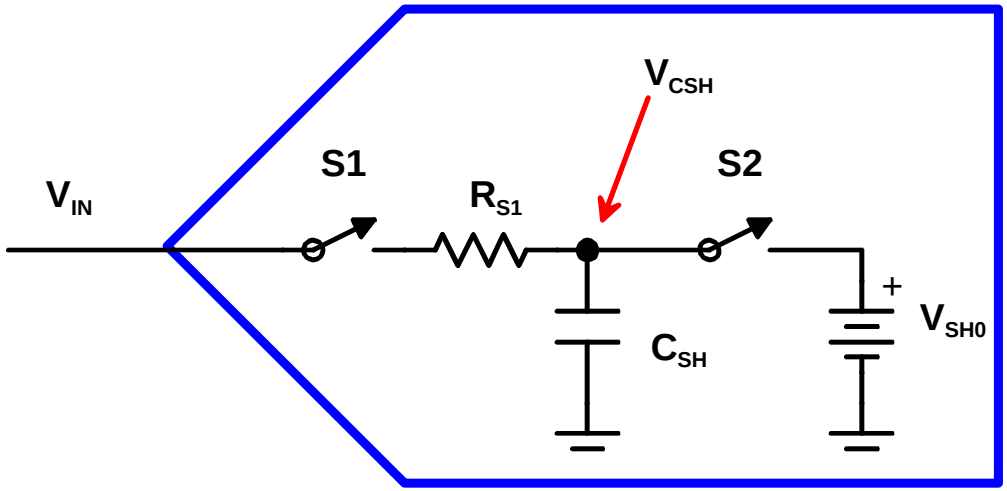


- Buffer for Impedance Matching
- Dynamic Load (Switched Capacitor)
- Acquisition Time

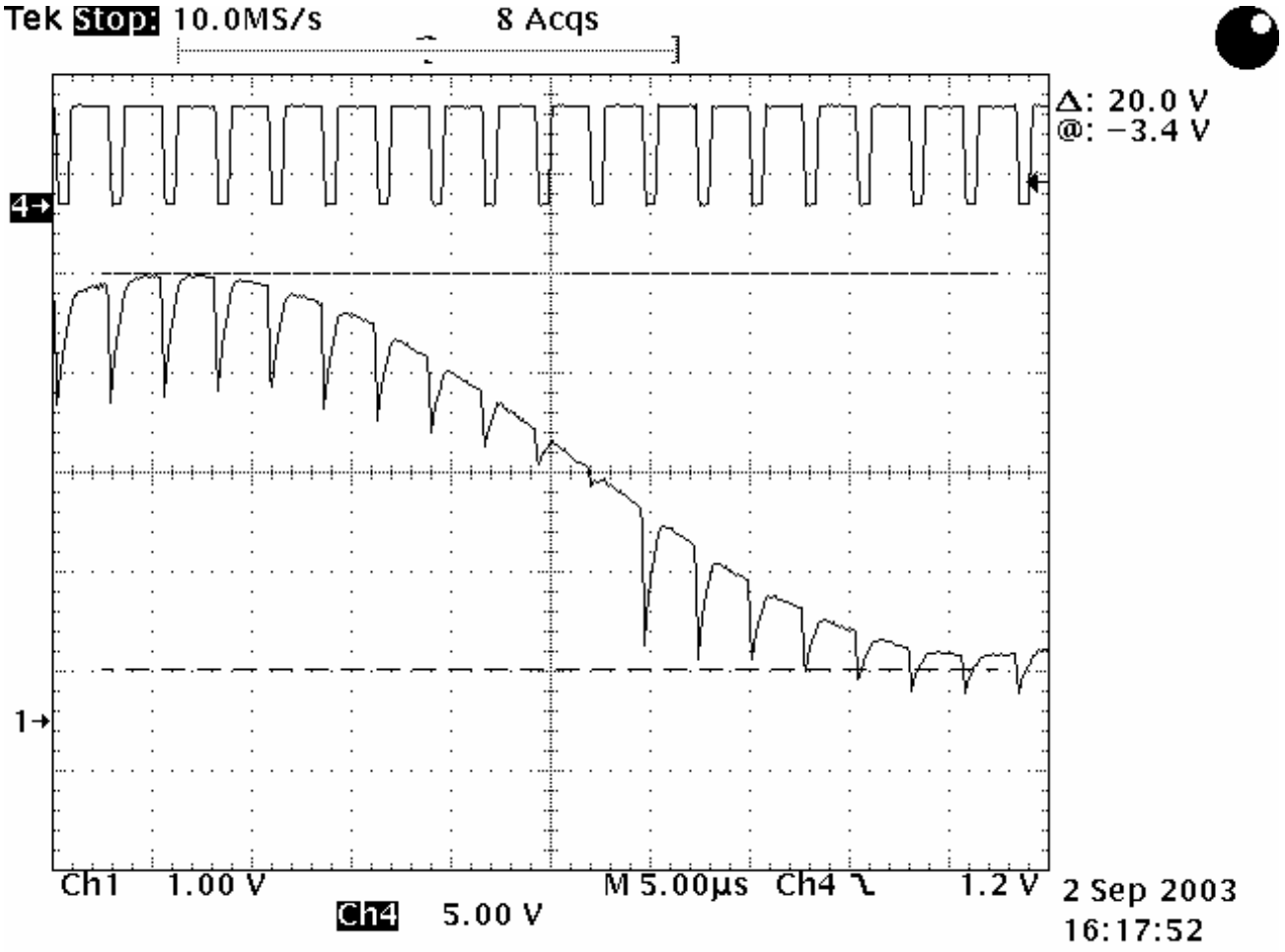
CDAC SAR ADC Input Buffer and Filter Selection



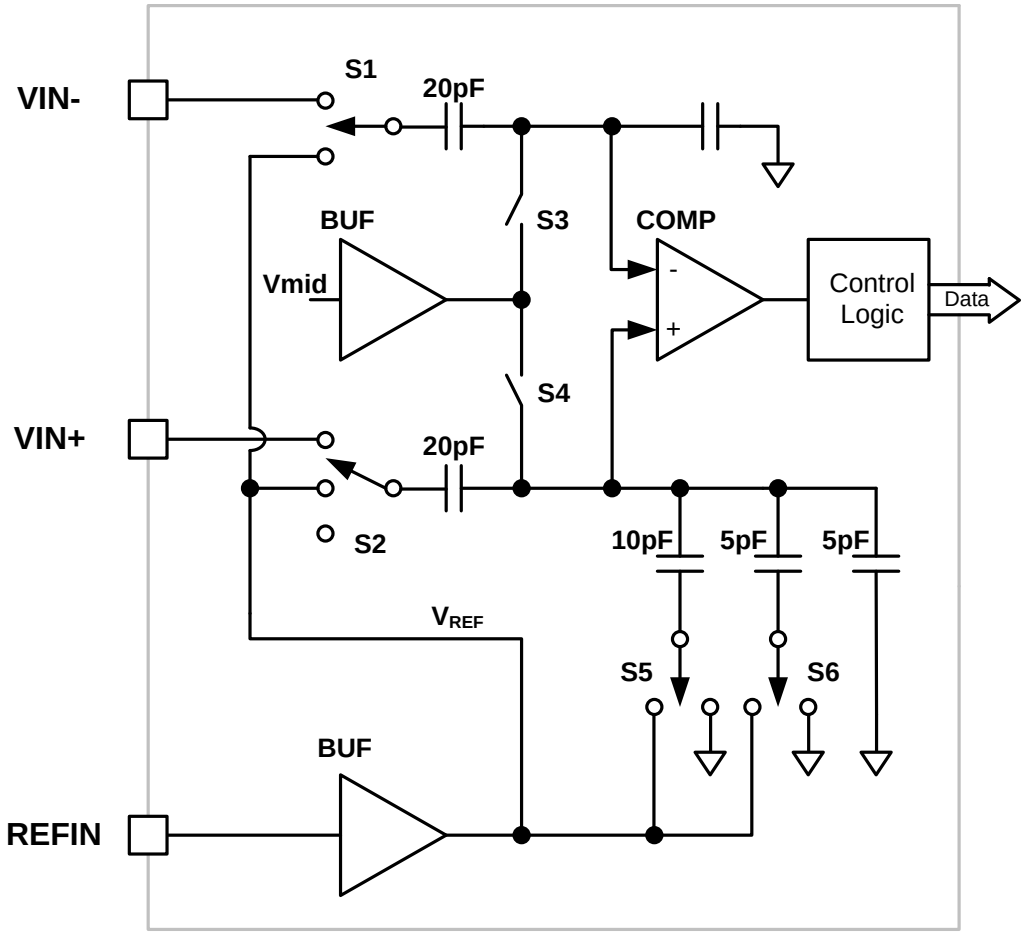
Simplified Model of SAR-ADC Input Stage



SAR ADC Input Voltage during Sampling

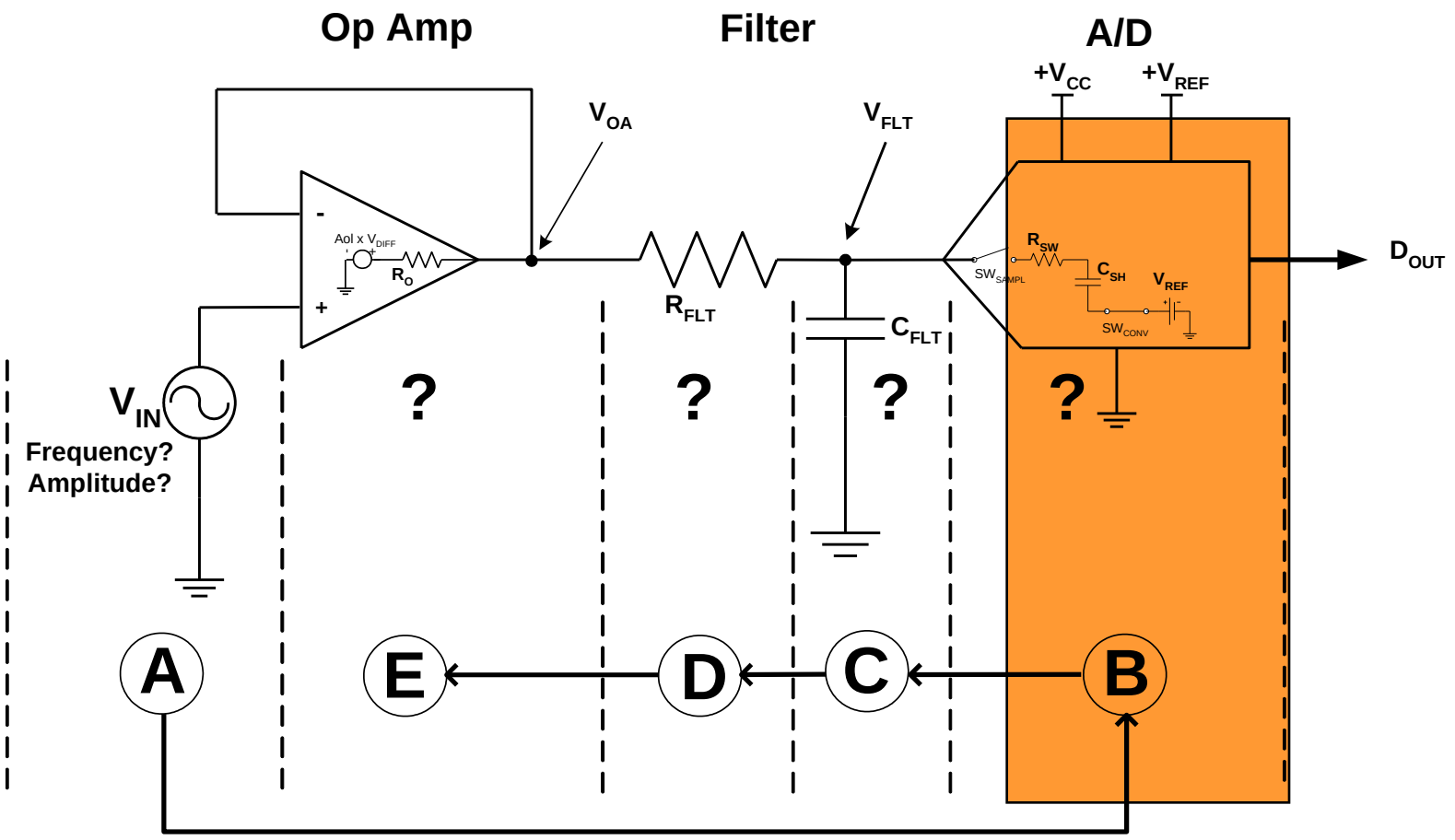


More detailed SAR Input Stage

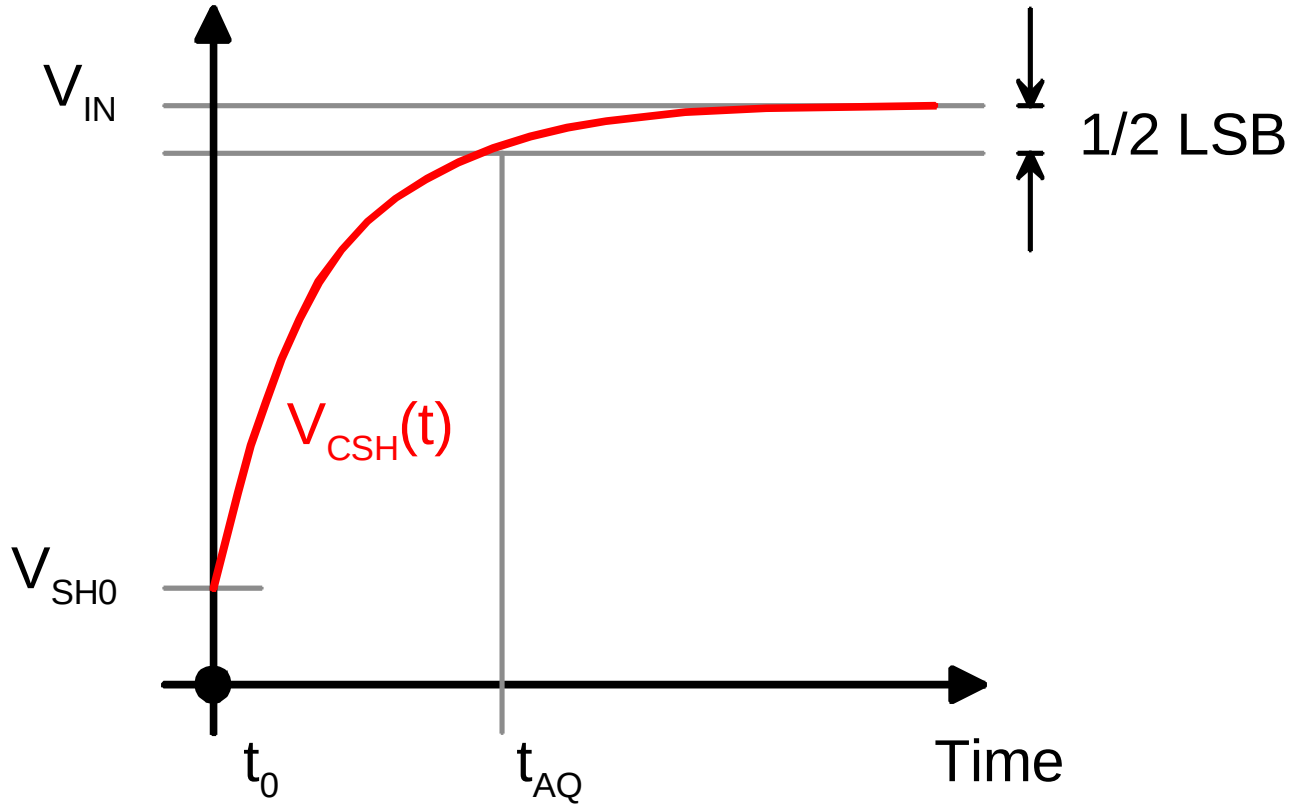


3 bits of ADS8361

CDAC SAR ADC Input Buffer and Filter Selection



Voltage Across the Sampling Capacitor



Voltage Across Sampling Capacitor

$$V_{CSH}(t) = V_{CSH}(t_0) + (V_{IN} - V_{CSH}(t_0)) \times (1 - e^{-\frac{t}{\tau}})$$

$V_{CSH}(t)$ is voltage in time across the sampling capacitor, C_{SH}

$V_{CSH}(t_0)$ is voltage across the C_{SH}, at beginning of acquisition time

V_{IN} is the input voltage to the ADC

τ is acquisition time constant and equal to $R_{S1} \times C_{SH}$

t is a time variable in seconds

Settling Time as Function of τ

$$V_{IN} - V_{CSH}(t_{AQ}) \leq \tfrac{1}{2} LSB$$

$V_{CSH}(t_{AQ})$ is voltage across the C_{SH}, at the end of the sampling period

t_{AQ} is acquisition time, the time from the beginning of the sampling period (t_0) to the end of the sampling period

$$\frac{1}{2} LSB = \frac{FSR}{2^{N+1}}$$

(LSB = Least Significant Bit, FSR is the full-scale range of the N-Bit converter)

$$t_{AQ} \geq k_1 \times \tau$$

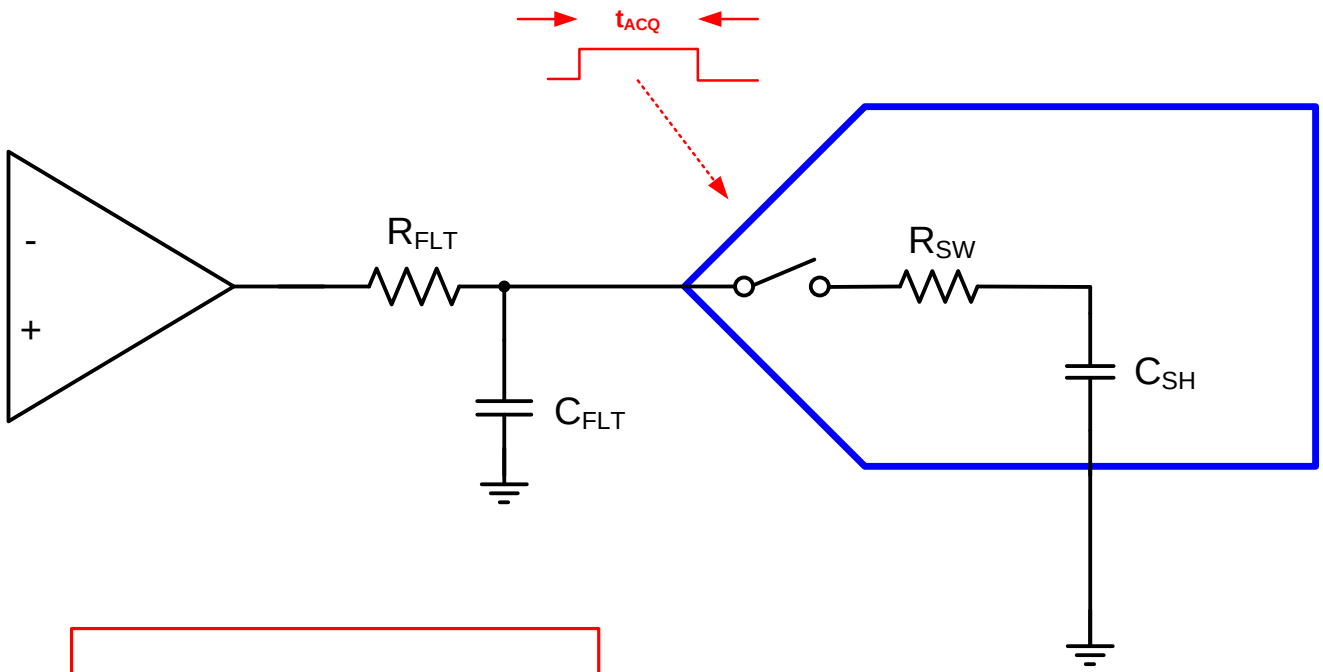
$$k_1 = \ln\left(\frac{V_{IN} - V_{SH0}}{FSR} \cdot 2^{N+1}\right)$$

Time-Constant-Multiplier for SAR ADC

ADC Resolution	k1 time-constant-multiplier 1/2 LSB accuracy, $1/2^{N+1}$
8	6.2
10	7.6
12	**9.0**
14	10.4
16	**11.8**
18	13.2
20	14.6

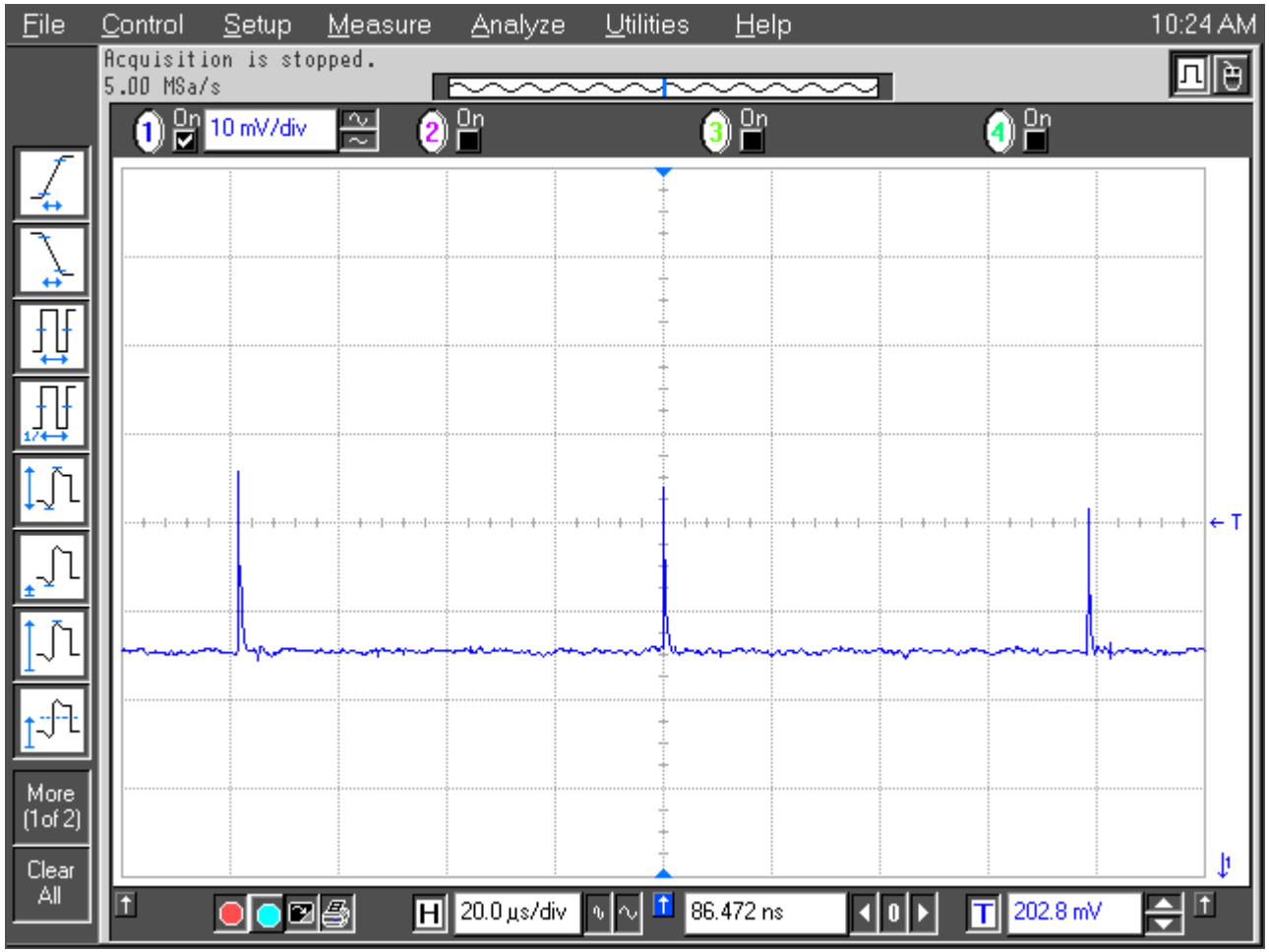
*note – using worst case values: V_{IN} = full-scale voltage or 2^N, V_{SH0} = 0V

Data Acquisition Time

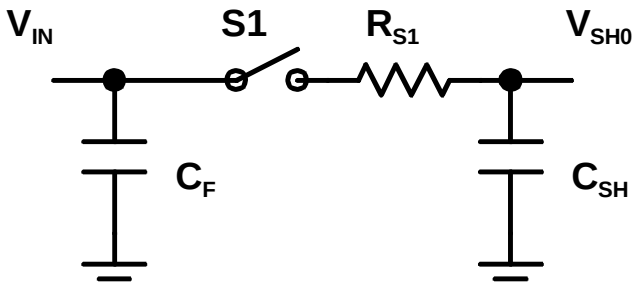


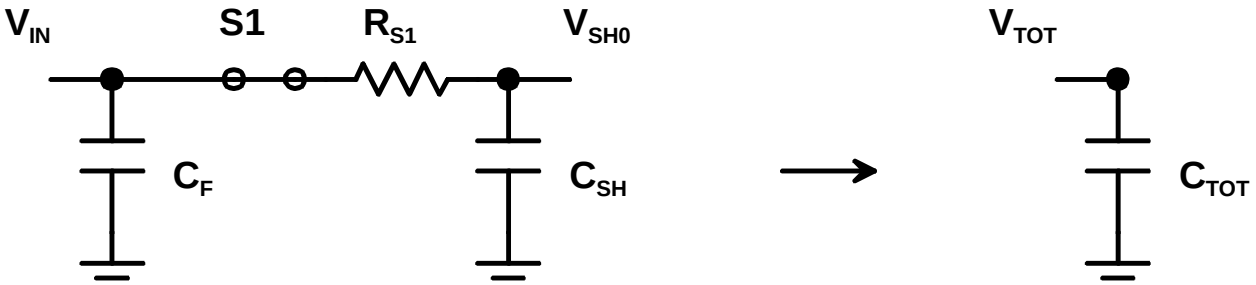
$$t_{AQ} \geq k_1 \times \tau$$

Charge Injection



External and Internal Acquisition Capacitors





Charge Distribution between C_F and C_{SH}

$$Q_{IN} = C_F \times V_{IN} \qquad Q_{SH} = C_{SH} \times V_{SH0}$$

After the closure of S1,the charge on C_F and C_{SH} distributes.

$$C_{TOT} = C_F + C_{SH} \qquad Q_{TOT} = Q_{IN} + Q_{SH}$$

$$V_{TOT} = \frac{C_F}{C_F + C_{SH}} \cdot V_{IN} + \frac{C_{SH}}{C_F + C_{SH}} \cdot V_{SH0}$$

$$V_{TOT} = \frac{a}{a+1} \cdot V_{IN} + \frac{1}{a+1} \cdot V_{SH0} \qquad a = \frac{C_F}{C_{SH}}$$

New Time Constant Multiplier

$$k_2 = \ln\left[\frac{\left(1-\frac{a}{a+1}\right)\cdot V_{IN} - \frac{1}{a+1}\cdot V_{SH0}}{FSR}\cdot 2^{N+1}\right]$$

"*k*" is not only function of the initial charge V_{SH0}, but it is also a function of the value of the applied external capacitor C_F. In the case of the lower frequency input signal (~f_S/10) the calculation of the initial charge V_{SH0} of the C_{SH} is ½ FSR. On the other hand, for the multiplexed signal at the input to the converter, we need to use 0V for V_{SH0}.

$$k_2 = \ln\left(\frac{1}{a+1}\cdot 2^{N+1}\right)$$

New Time-Constant-Multiplier for SAR ADC

ADC Resolution	C_F [pF]	a C_F/C_{SH}	k2 time-constant-multiplie 1 LSB accuracy, $1/2^N$	R_F [Ω]
16	200	8	9.6	1,576
16	400	16	9.0	894
16	1000	40	8.1	411
16	4000	160	6.7	126

*note – using worst case values: V_{IN} = full-scale voltage or 2^N, V_{SH0} = 0V

Assumed: t_{AQ}=3.4us and C_{SH}=25pF

Charge Bucket I

- **Charge Transfer Equation: Q = CV**

- **Charge required to charge C_{SH} to V_{REF}**
  - **$Q_{SH} = C_{SH}V_{REF}$**
  - **Q_{SH} = 25pF·4.096V = 102pC**

- **IDEAL C_{FLT}**
  - **"Charge Bucket" to fill C_{SH} with only a 31.25µV (1/2LSB) droop on C_{FLT}**
  - **$Q_{FLT} = Q_{SH}$**
  - **$Q_{FLT} = C_{FLT}$ (31.35µV)**
  - **102pC = C_{FLT} (31.25µV) → C_{FLT} = 3.3µF**

- **IDEAL C_{FLT} = 3.3µF**
  - **Not a good, small, cheap high frequency capacitor**
  - **Not practical for Op Amp to drive directly (stability, transient current)**
  - **Isolation resistor likely not large enough to help isolate Cload and still meet necessary filter time constant**

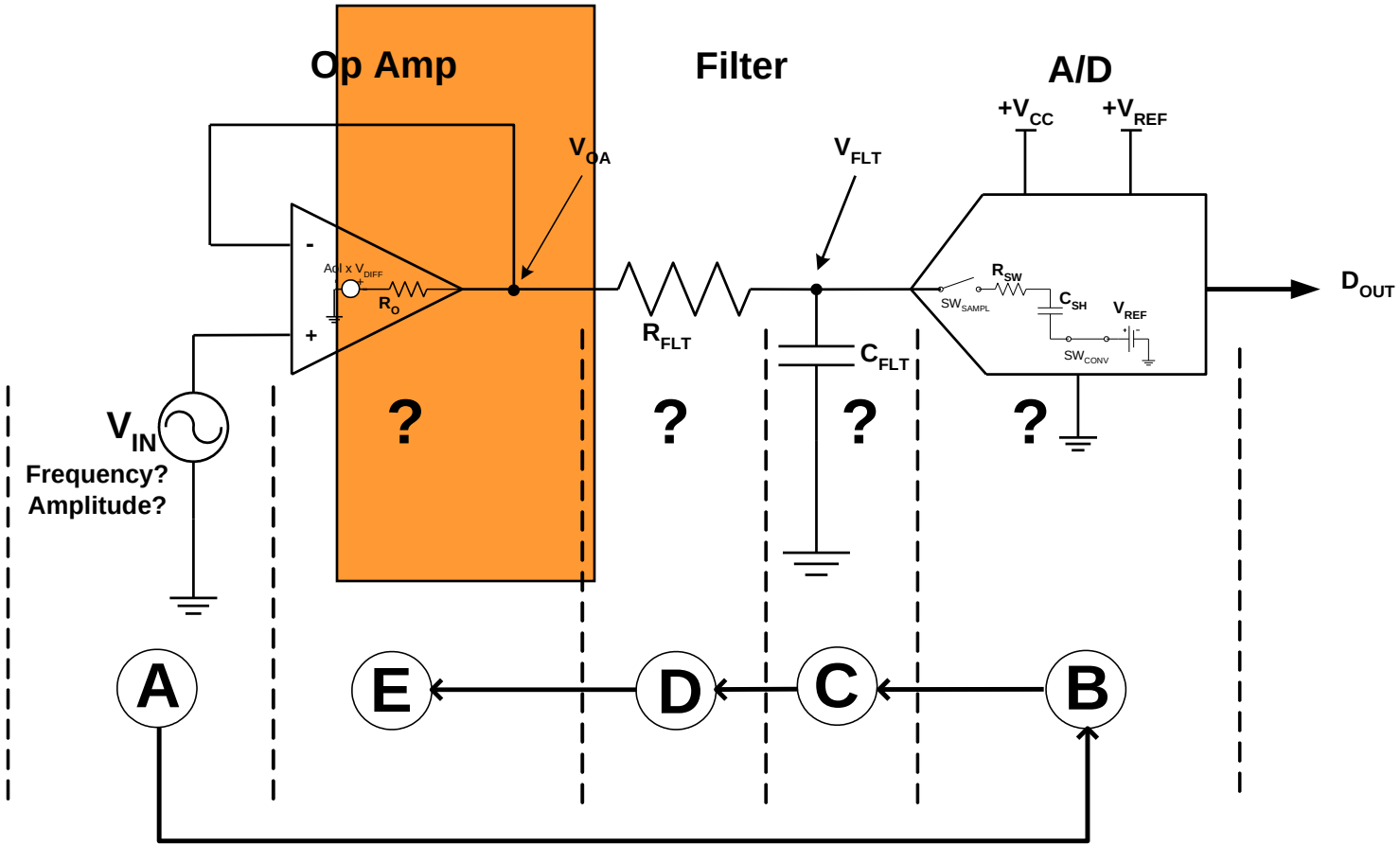
Charge Bucket II

- **Partition the "Charge Bucket"**
  - 95% from C_{FLT}
  - 5% from Op Amp

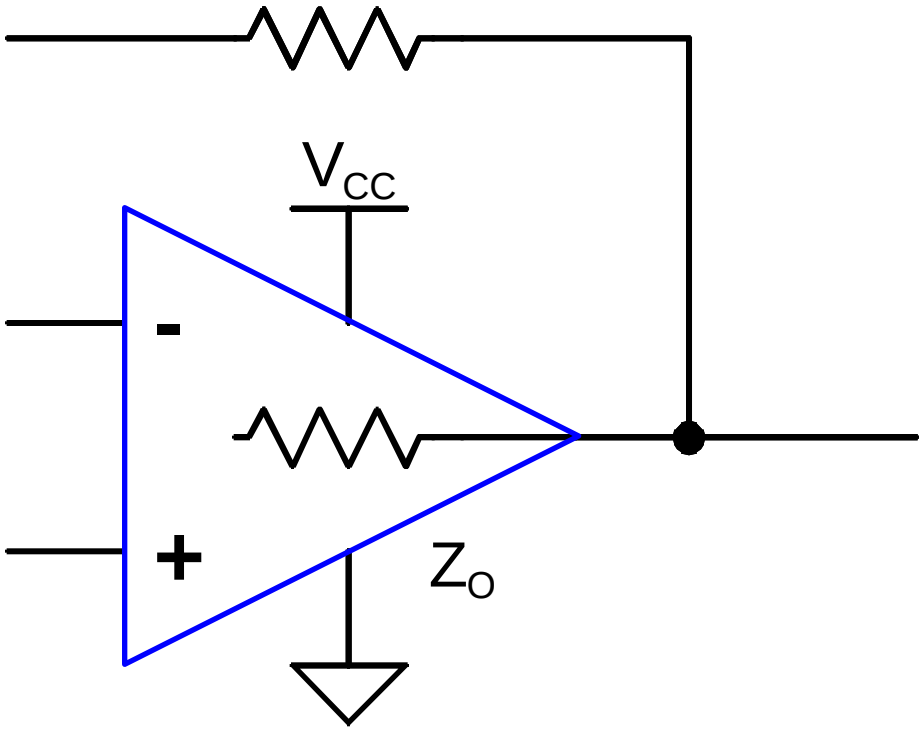
- **C_{FLT} value required to provide Q_{SH} with <5% droop on C_{FLT}**
  - $Q_{FLT} = Q_{SH}$
  - $Q_{FLT} = C_{FLT}$ (0.05VREF)
  - 102pC = C_{FLT} (0.05·4.096V) → C_{FLT} = 500pF

- **During t_{ACQ} the Op Amp must replace 5% V_{REF} on C_{FLT}**
  - Ensure C_{FLT} is at least 10 X > C_{SH}
    - This implies dominant load for Op Amp Buffer is C_{FLT}
    - 500pF = 20 X 25pF → C_{FLT} > 20 X C_{SH}

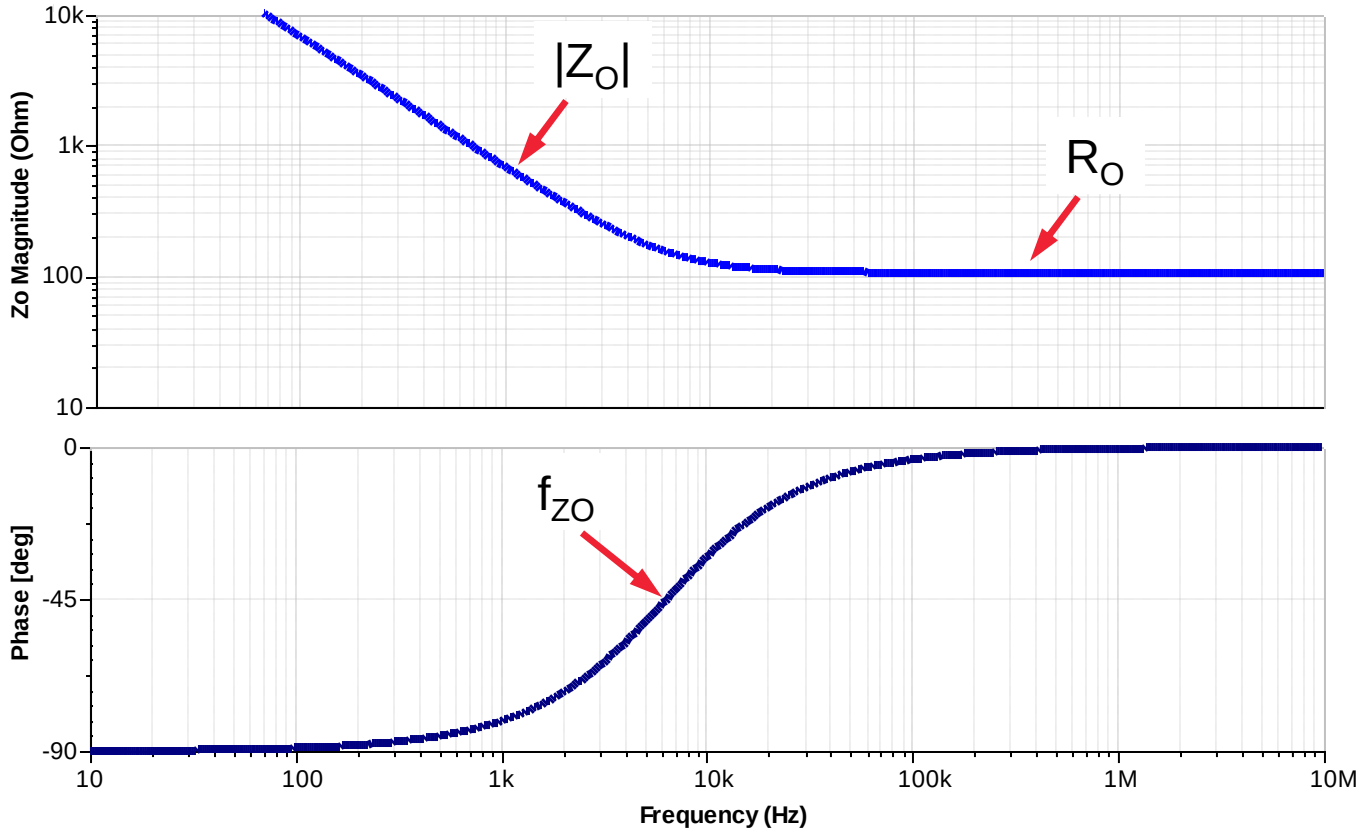
CDAC SAR ADC Input Buffer and Filter Selection



Buffer Output Impedance



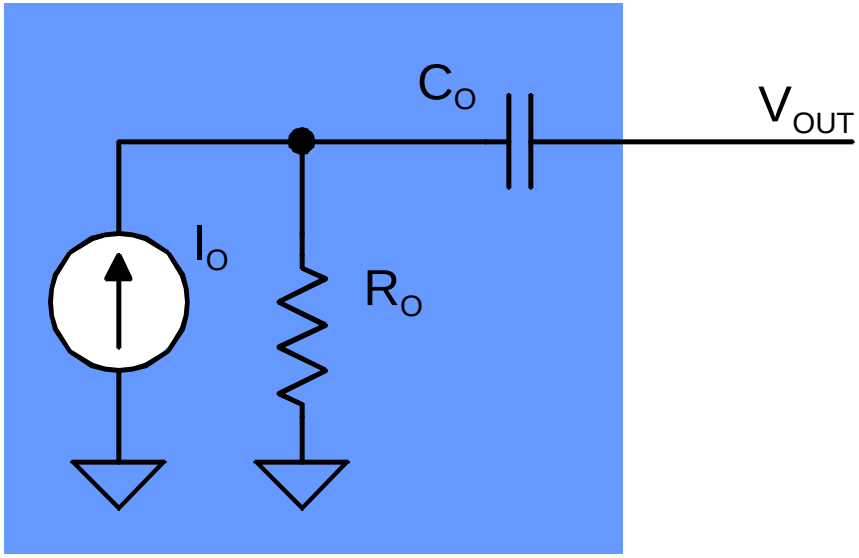
OPA364 Open-Loop Output Impedance



R_O Open-Loop output resistance

f_{ZO} Frequency of Zero in the Open-Loop output impedance

OPA364 Open-Loop Output Impedance



Values from Tina model

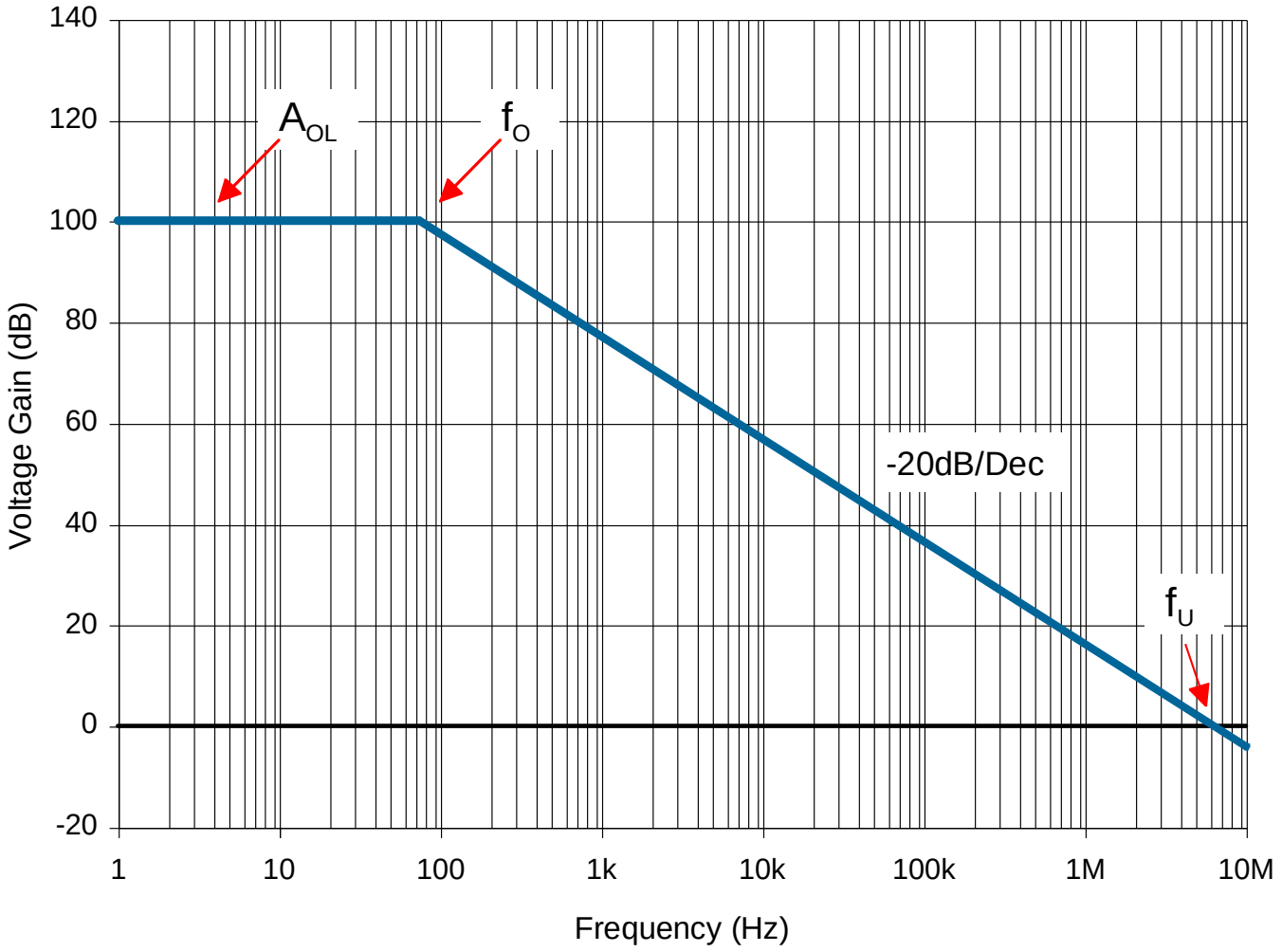
$$R_O = 107.3\Omega$$

$$f_{ZO} = 6.32kHz$$

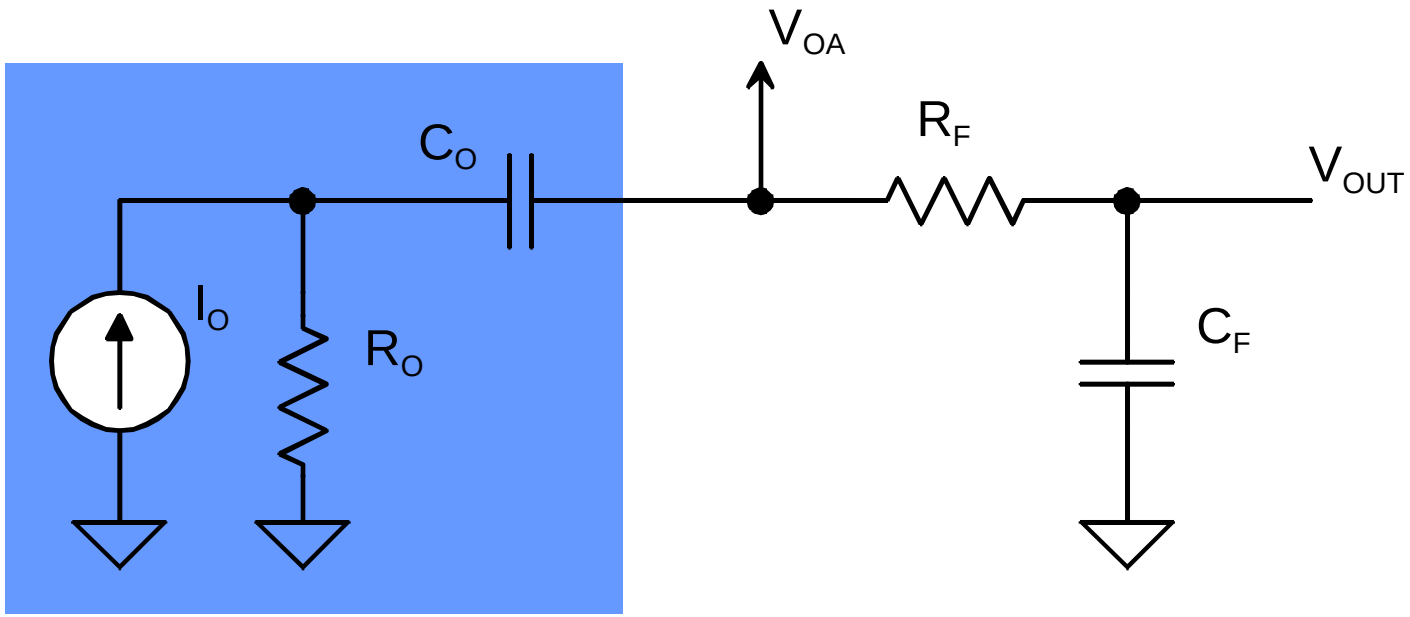
$$f_{ZO} = \frac{1}{2\pi \cdot R_O \cdot C_O}$$

$$C_O = 0.235\mu F$$

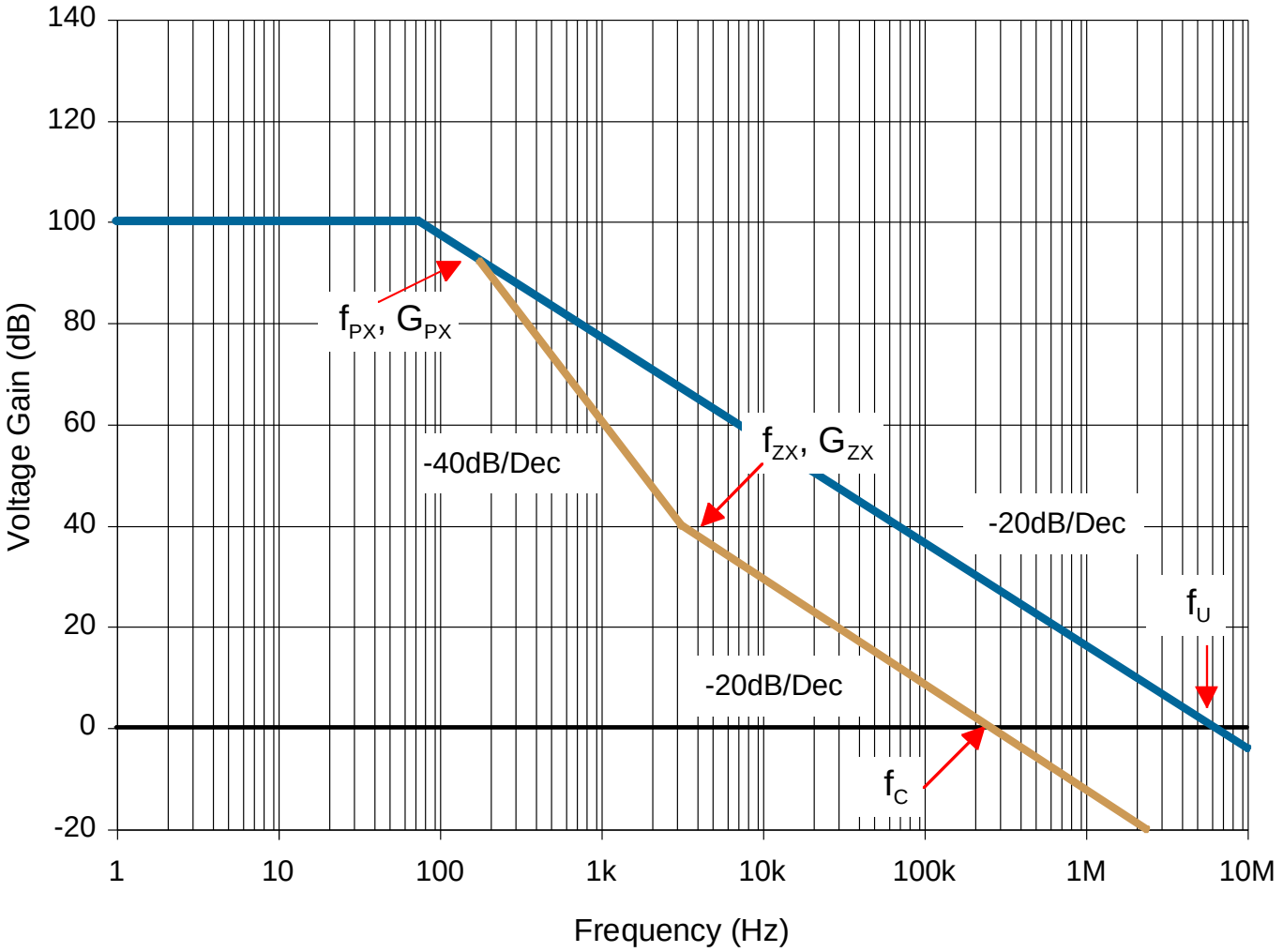
OPA364 Open-Loop Voltage Gain



Op Amp with external RC-Filter



Op Amp with External RC Filter



Added Pole and Zero

BiPOLAR OpAmp

$$f_{PX} = \frac{1}{2\pi \cdot (R_O + R_F) \cdot C_F}$$

$$f_{ZX} = \frac{1}{2\pi \cdot R_F \cdot C_F}$$

2-Stage CMOS RRO OpAmp

$$f_{PX} = \frac{1}{2\pi \cdot (R_O + R_F) \cdot \left[\frac{C_O \cdot C_F}{C_O + C_F} \right]}$$

$$f_{ZX} = \frac{1}{2\pi \cdot R_F \cdot C_F}$$

Gain of Added Pole and Zero

Gain of added pole

$$G_{PX} = -20 \cdot \log\left[\frac{f_{PX}}{f_U}\right]$$

Gain of added zero

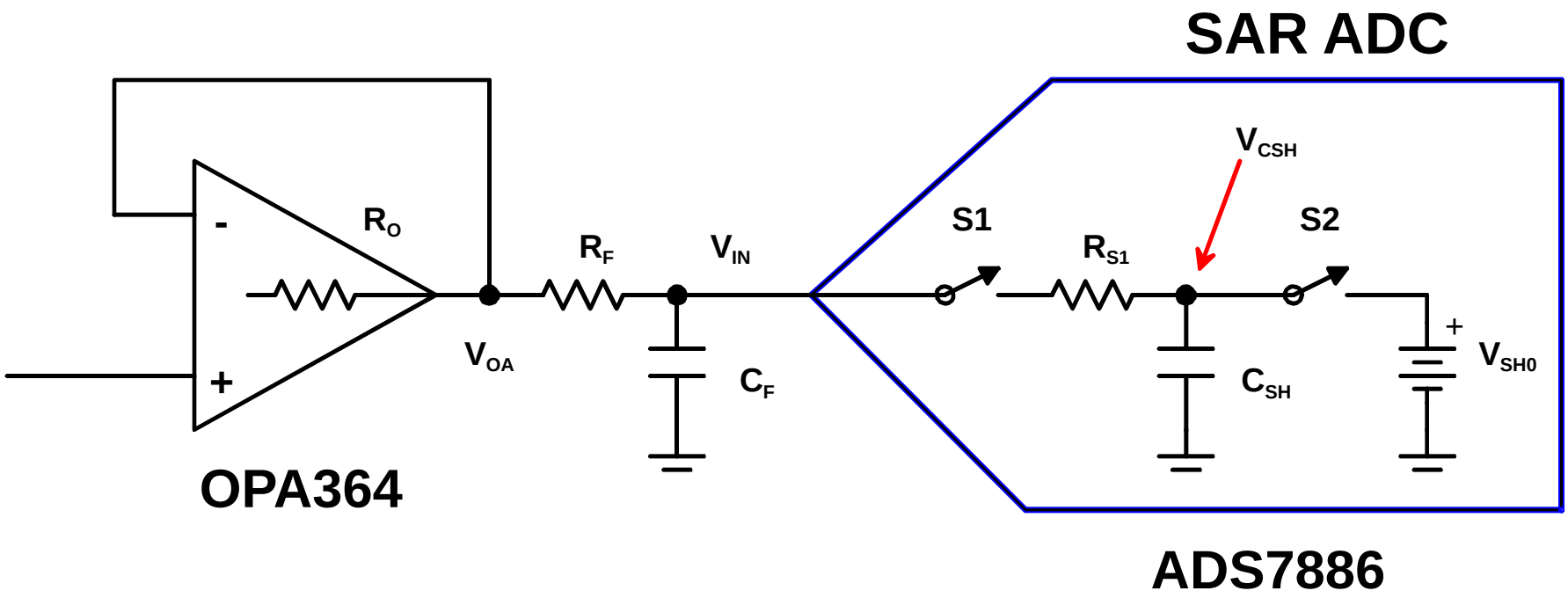
$$G_{ZX} = G_{PX} - 40 \cdot \log\left[\frac{f_{ZX}}{f_{PX}}\right]$$

$$G_C = 0dB = G_{ZX} - 20 \cdot \log\left[\frac{f_C}{f_{ZX}}\right]$$

Modify close-loop unity gain frequency

$$f_C = f_{ZX} \cdot 10^{G_{ZX}/20}$$

Test Circuit



Design Criteria (w/o Phase Margin)

1) Critically stable:

$$f_{ZX} = f_C(-40dB/decade)$$

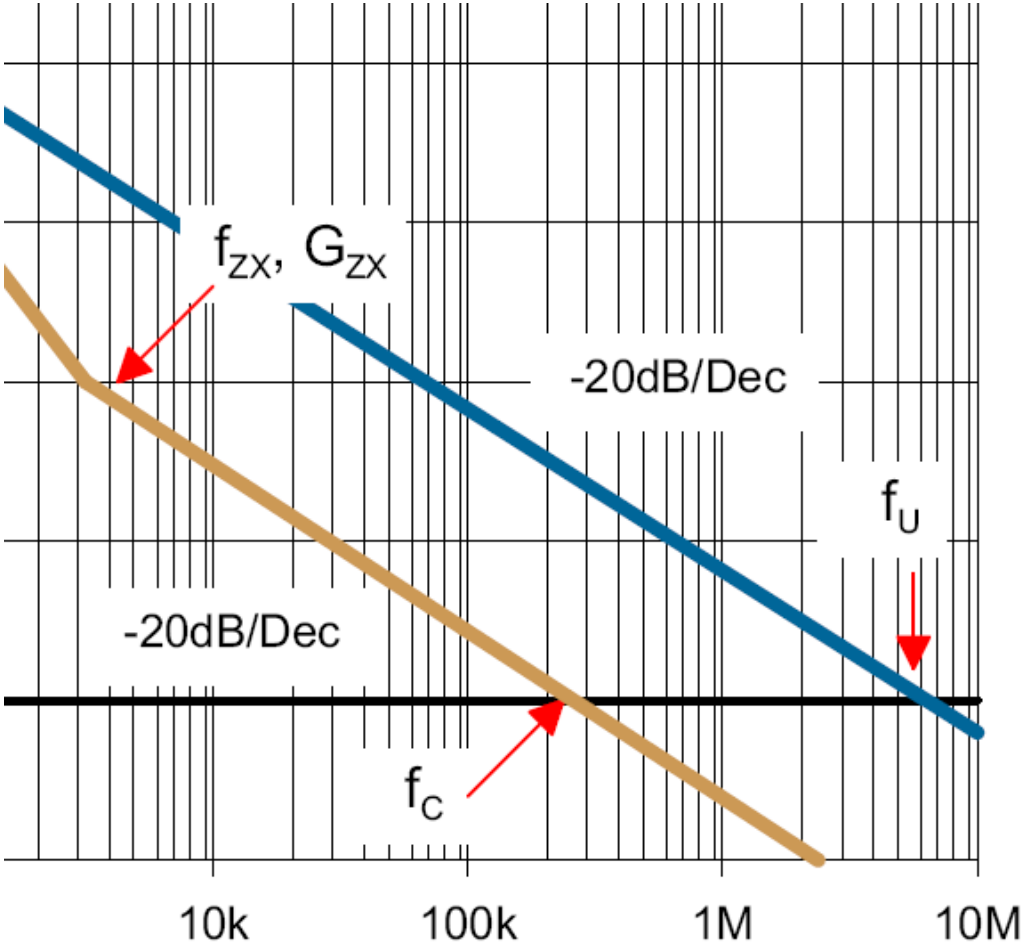
2) Marginally stable:

$$G(f_{ZX}) = 3dB \quad or \quad f_{ZX} = \frac{f_C}{1.41}$$

3) Good design:

$$G(f_{ZX}) = 6dB \quad or \quad f_{ZX} = \frac{f_C}{2}$$

A Good Design Guideline



$$f_C \le \frac{1}{2} f_U$$

$$f_{ZX} \le \frac{1}{2} f_C$$

or

$$f_{ZX} \le \frac{1}{4} f_U$$

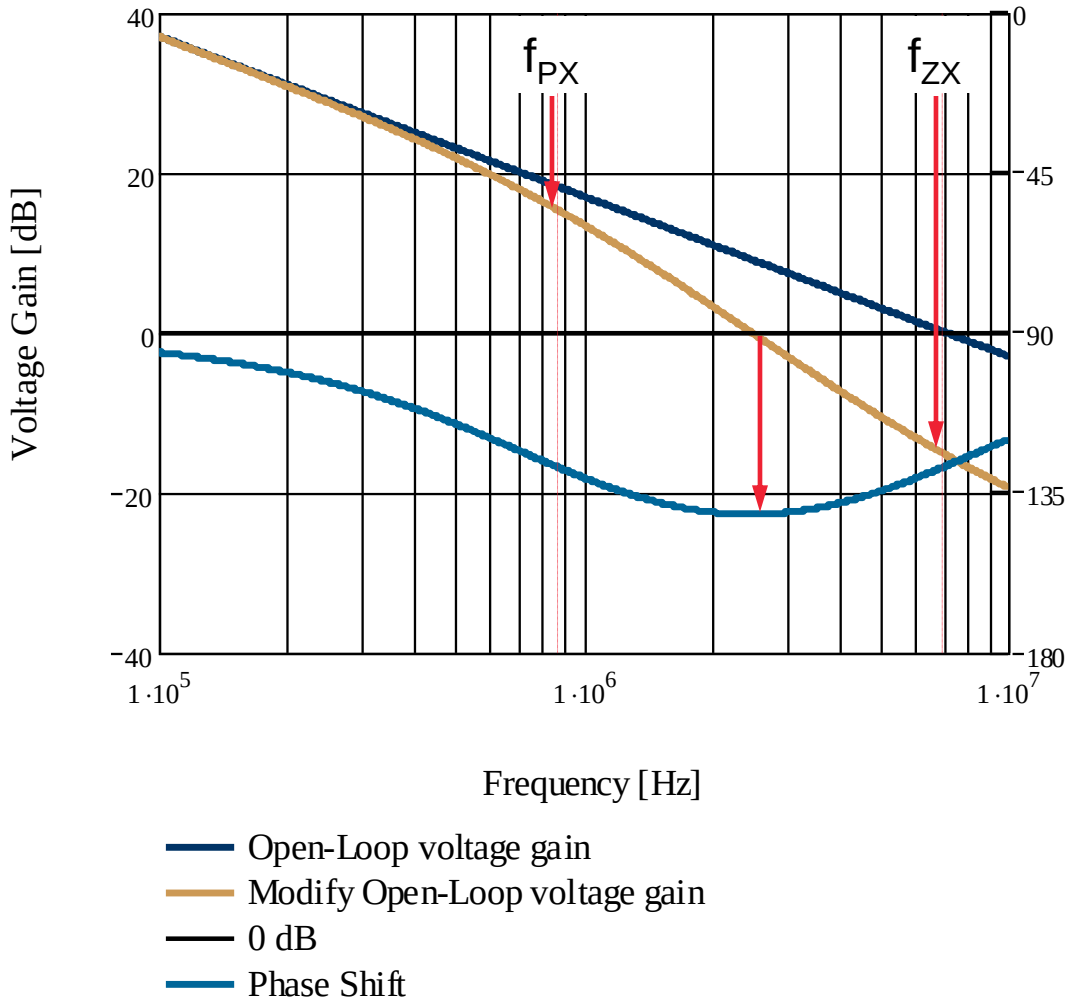
$$G_{ZX} \ge +6dB$$

- Phase Shift -

$$f_{PX} > \frac{1}{10} f_{ZX}$$

$$R_F \ge \frac{R_O}{9}$$

OPA364 with R_F=15Ω and C_F=1,500pF



$$f_{PX} = 873kHz$$
$$G_{PX} = 15.3dB$$
$$f_{ZX} = 7.07MHz$$
$$G_{ZX} = -5.2dB$$
$$f_C = 2.49MHz$$
$$\theta(f_C) = -141.3°$$

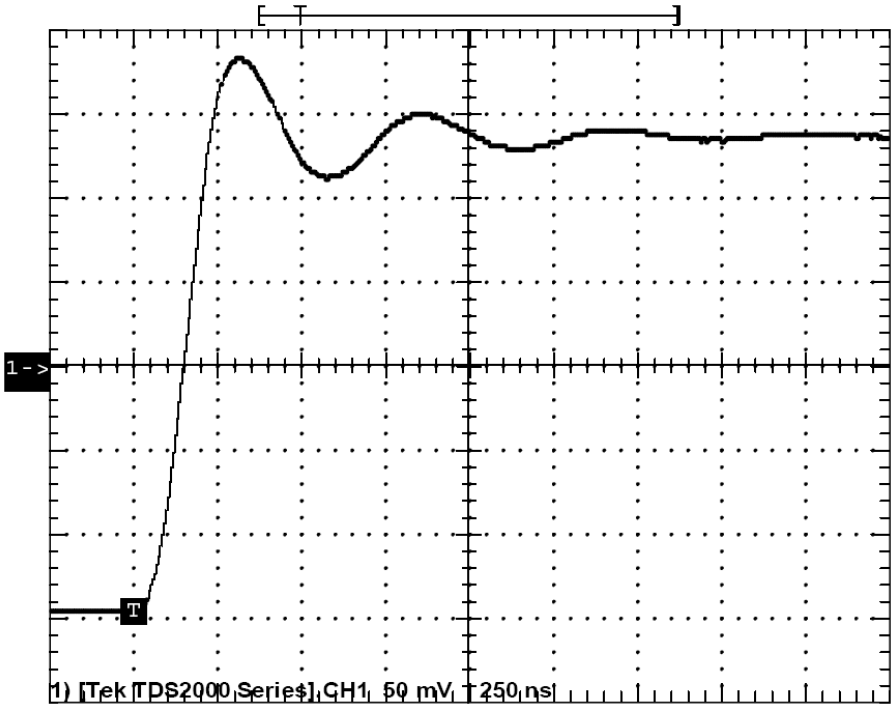
Phase Margin

$$\psi(f_C) = 180° - \theta(f_C)$$

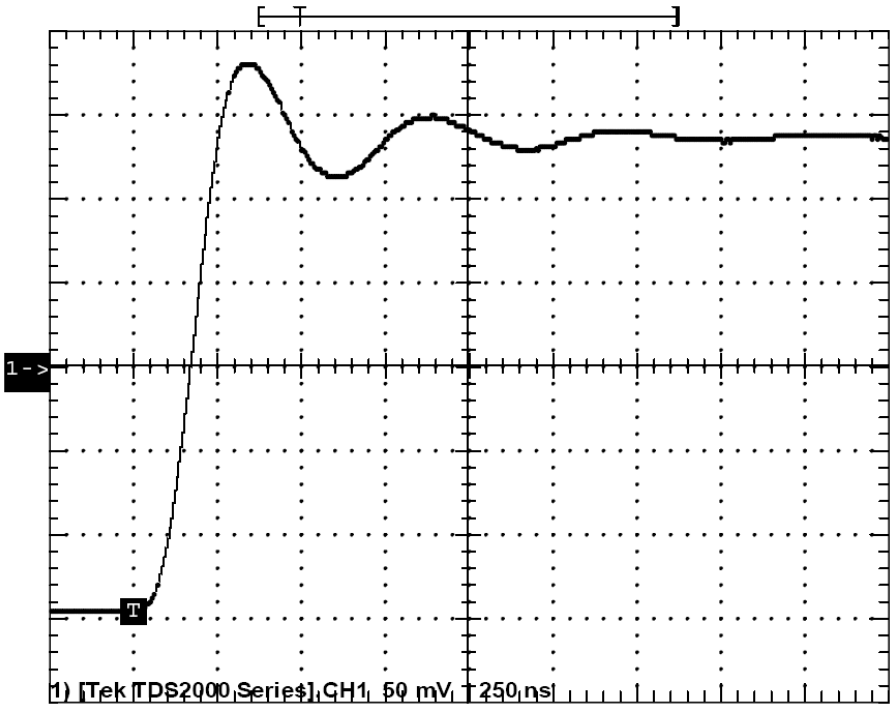
$$\boxed{\psi(f_C) = 38.7°}$$

Small Signal Step Response

R_F=15Ω and C_F=1,500pF
50mV/div 250ns/div

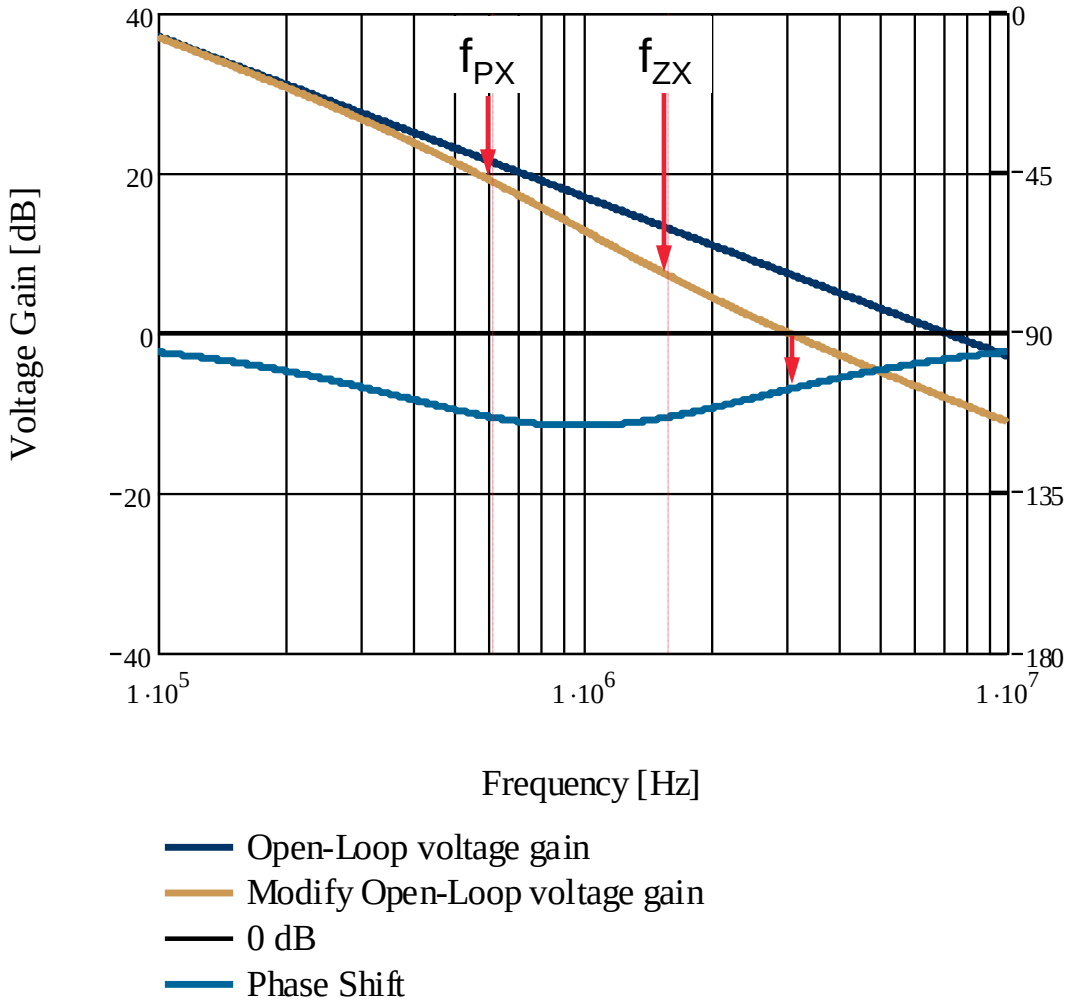


OPA364 Output



ADC Input

OPA364 with R_F=66.5Ω and C_F=1,500pF



$$f_{PX} = 616kHz$$
$$G_{PX} = 18.9dB$$
$$f_{ZX} = 1.59MHz$$
$$G_{ZX} = 7.12dB$$
$$f_C = 3.04MHz$$
$$\theta(f_C) = -106.3°$$

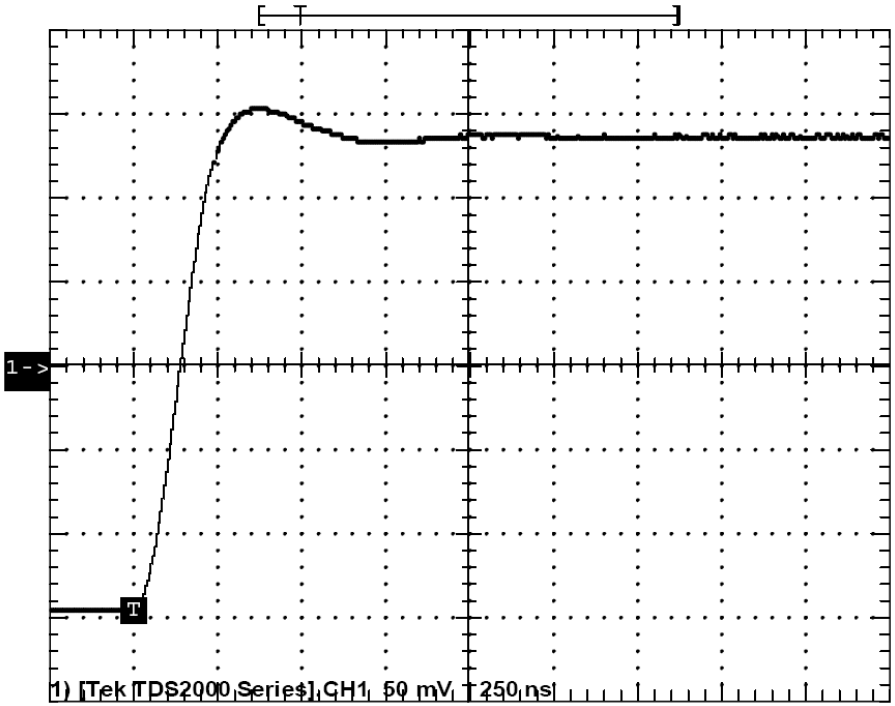
Phase Margin

$$\psi(f_C) = 180° - \theta(f_C)$$

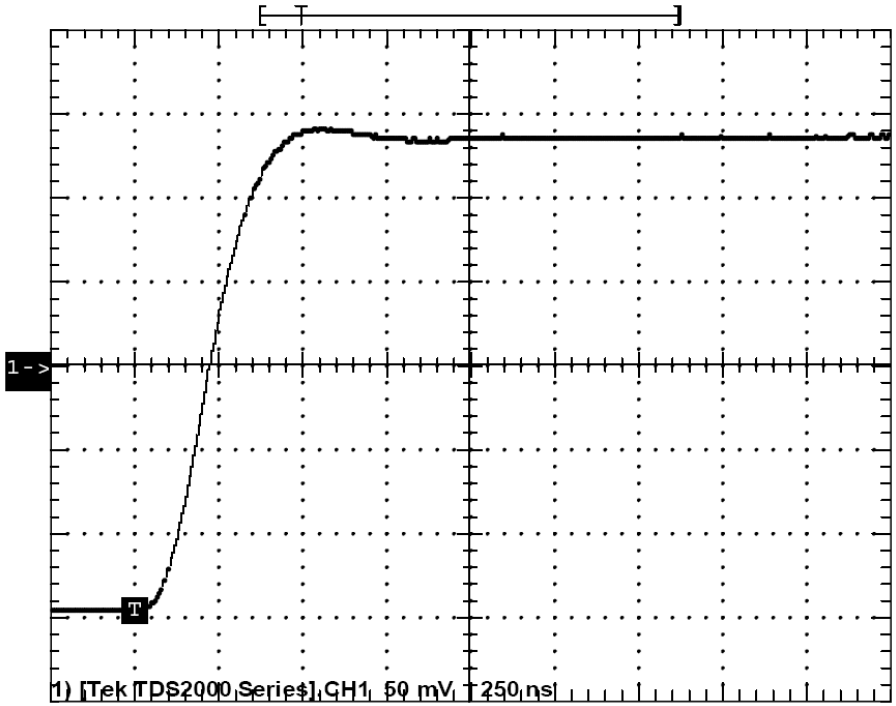
$$\boxed{\psi(f_C) = 73.7°}$$

Small-Signal Step Response

R_F=66.5Ω and C_F=1,500pF
50mV/div 250ns/div

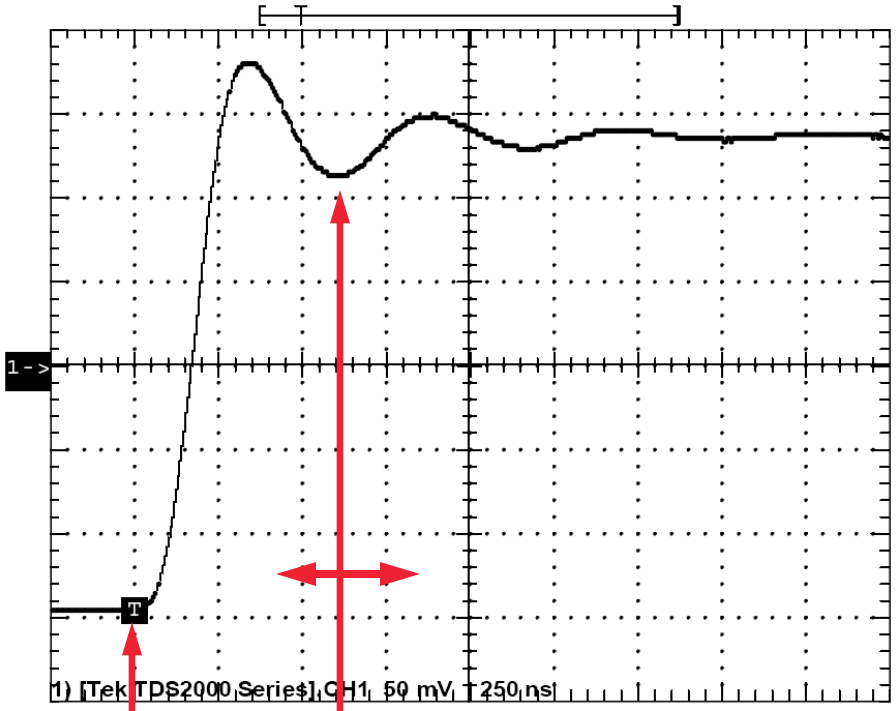


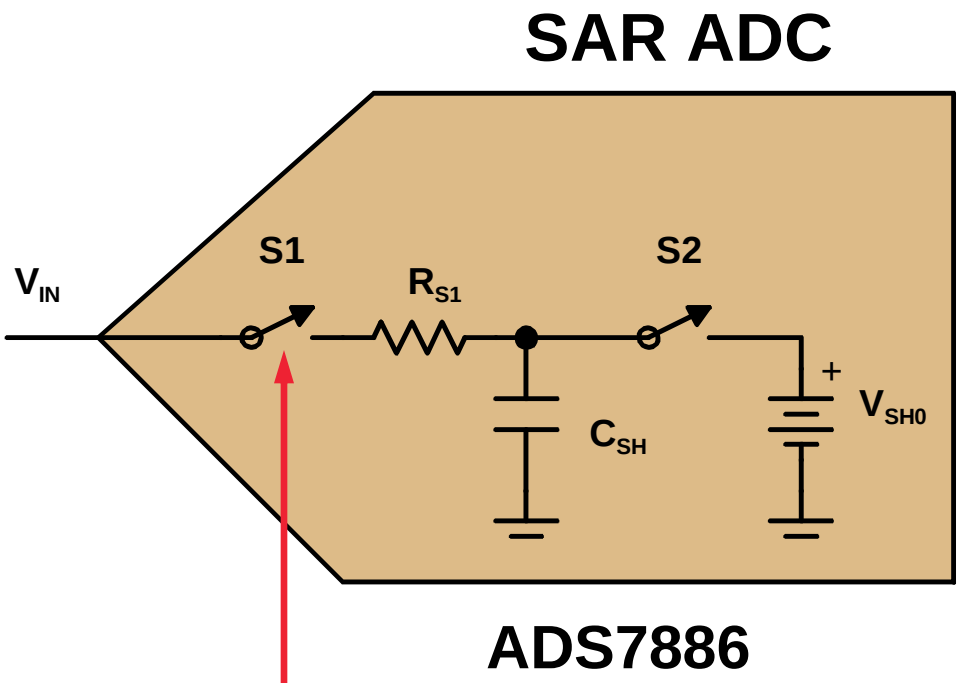
OPA364 Output



ADC Input

Histogram Results for Different t_{AQ}





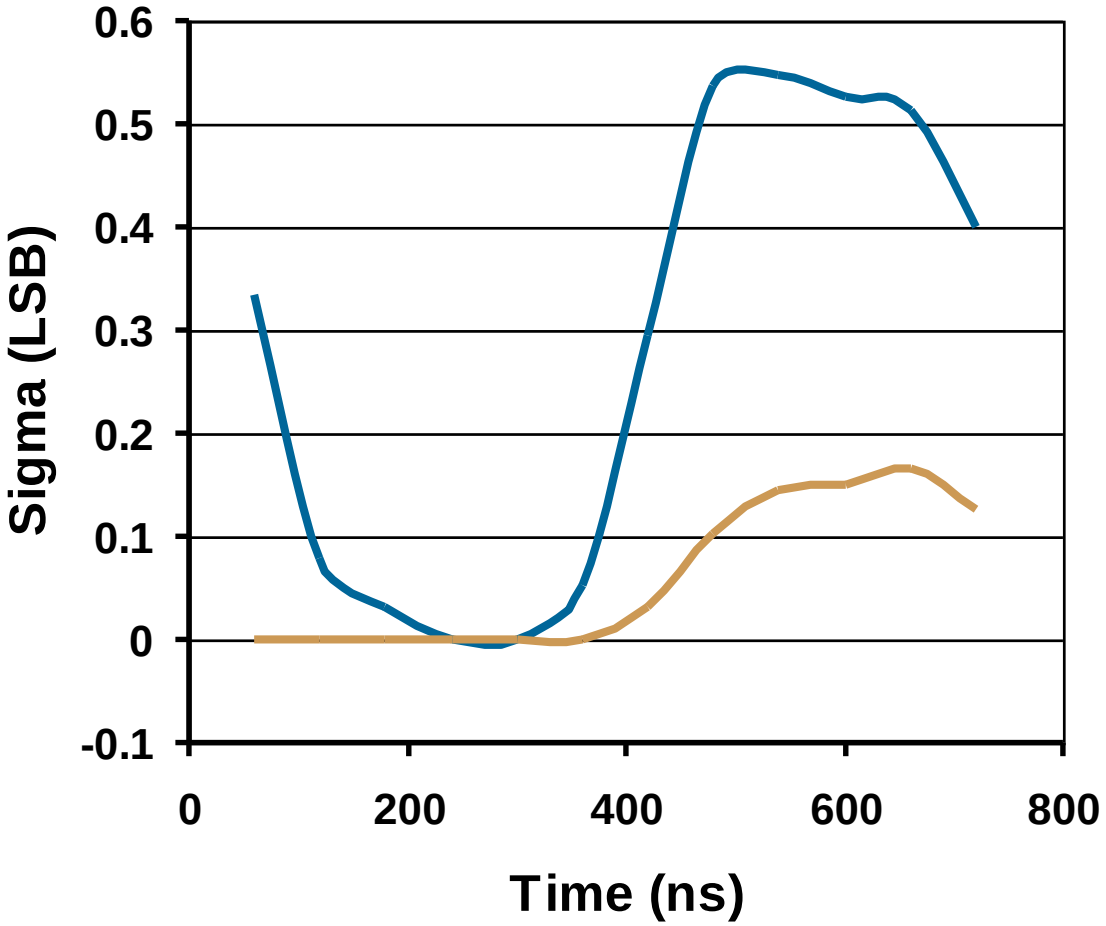
t_{OFF}

t_{ON}

$t_{AQ} = var$

ON/OFF

Histogram Results for Different t_{AQ}



ADS7886
Resolution 12 Bit
FSR 4.096 V
65535 Samples per t_{AQ}

15Ohm 1,500pF

66.5Ohm 1,500pF

σ_{MAX} = 0.55 LSB
Vn_{MAX} = 548 μV_{RMS}

σ_{MAX} = 0.16 LSB
Vn_{MAX} = 164 μV_{RMS}

Minimum Acquisition Time and OpAmp's GBW

1) Find Unity Gain Bandwidth $f_U = GBW$

2) Calculate frequency of added zero $f_{ZX} = \frac{1}{4} f_U$

3) Determine minimum time-constant $\tau = \frac{1}{2\pi \cdot f_{ZX}}$

4) Calculate time-constant multiplier $k = \ln\left(\frac{1}{a+1} \cdot 2^{N+1}\right)$ $a = \frac{C_F}{C_{SH}}$

5) Find minimum acquisition time $t_{AQ} \geq k \cdot \tau$

Minimum Acquisition Time for Some OpAmp's

		GBW (MHz)	f_Z (MHz)	τ (ns)	12 Bit t_{AQ} (ns)	16 Bit t_{AQ} (ns)
INA155	Medium Speed, Precision INA	0.55	0.14	1,157	5,672	8,881
INA128	High Precision, 120dB CMRR	1.3	0.33	490	2,400	3,757
INA331	High Bandwidth, Single Supply	5.0	1.25	127	624	977
OPA340	CMOS, 0.0007% THD+N	5.5	1.38	116	567	888
OPA363	1.8V, High CMRR, SHDN	7.0	1.75	91	446	698
OPA2613	Dual VFB, Low Noise	12.5	3.13	51	250	391
OPA627	Ultra-Low THD+N, Wide BW	16.0	4.00	40	195	305
OPA381	Precision High-Speed Amp	18.0	4.50	35	173	271
OPA727	CMOS, e-trim™, Low Noise	20.0	5.00	32	156	244
OPA228	Precision, Low Noise, G ≥ 5	33.0	8.25	19	95	148
OPA350	Precision ADC Driver	38.0	9.50	17	82	129
OPAy365	High-Speed, Zero-Crossover	50.0	12.50	13	62	98
OPA2889	Dual, Low Power, VFB	75.0	18.75	8	42	65
OPA211	36V, Bipolar Precision	80.0	20.00	8	39	61
THS4281	Very Low Power RRIO	80.0	20.00	8	39	61
OPA358	CMOS, 3V Operation, SC70	80.0	20.00	8	39	61

After selecting ADC and Op Amp

1) Determine C_F $$20 \cdot C_{SH} \le C_F \le 60 \cdot C_{SH}$$

2) Calculate "*a*" $$a = \frac{C_F}{C_{SH}}$$

3) Calculate time-constant multiplier $$k = \ln\left(\frac{1}{a+1} \cdot 2^{N+1}\right)$$

4) Calculate frequency of added zero $$f_{ZX} = \frac{t_{AQ}}{k}$$

5) Verify frequency of added zero $$f_{ZX} \le \tfrac{1}{4} f_U$$

After selecting ADC and OpAmp

1) Calculate R_F

$$R_F = \frac{1}{2\pi \cdot C_F \cdot f_{ZX}}$$

2) Verify value R_F

$$R_F \geq \frac{R_O}{9}$$

3) Calculate frequency of added pole

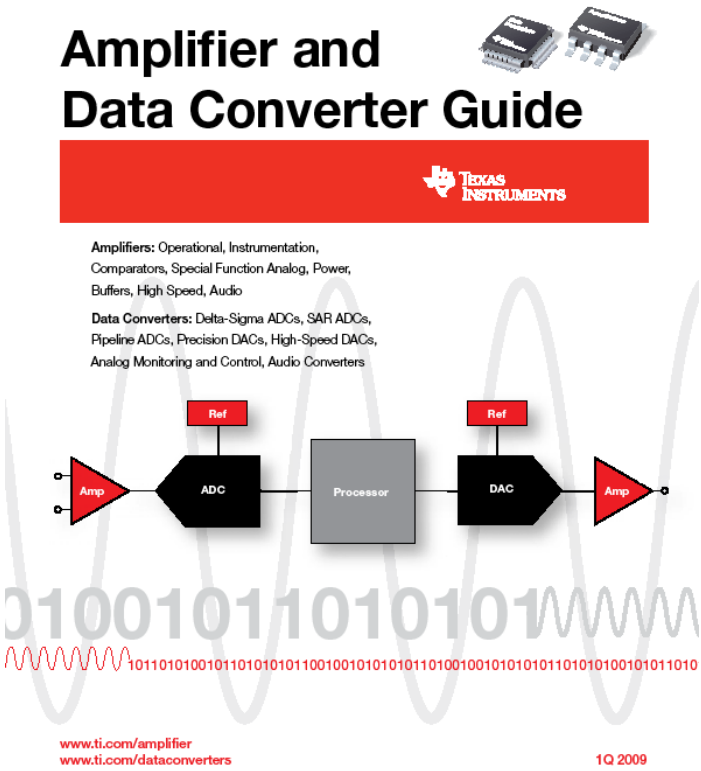
$$f_{PX} = \frac{1}{2\pi \cdot (R_F + R_O) \cdot C_F}$$

4) Keep added pole and zero less then decade a part

$$f_{PX} \geq \tfrac{1}{10} f_{ZX}$$

5) Verify gain of added zero

$$+6dB \leq G_{ZX} = -20 \cdot \log\left[\frac{f_{PX}}{f_U}\right] - 40 \cdot \log\left[\frac{f_{ZX}}{f_{PX}}\right]$$



Thanks !

for your attention