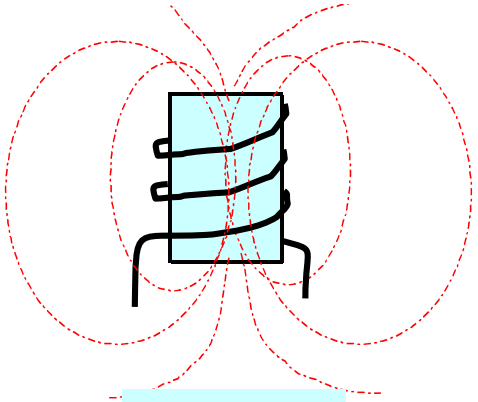
TI Technology Days 2010

Power Supply: Tips & Tricks

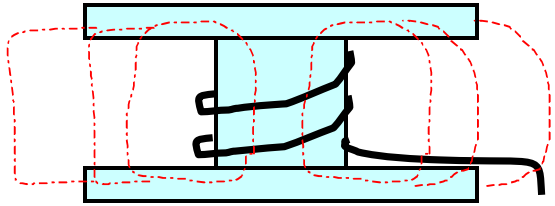
Agenda

- **Characteristic of passive and active components**
  - **Inductors**
  - **Capacitors**
  - **Switching regulators**
  - **Ease your designs challenge**
- **Special circuits**
- **Thermal Design**
- **Improved measurement techniques**
- **Layout**

Inductors – Selection of different core types

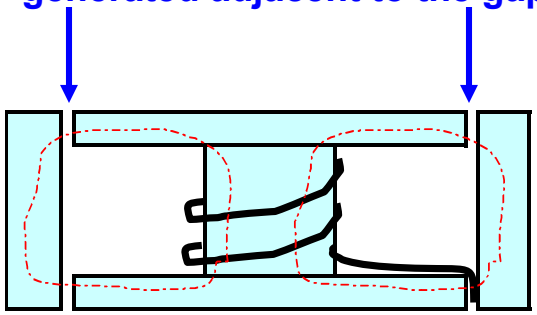


Rod Core

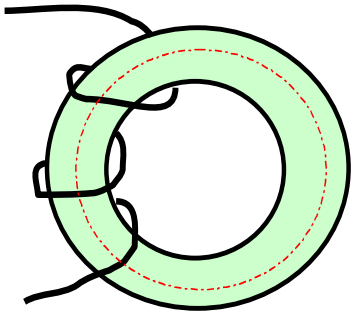


Unshielded Drum Core

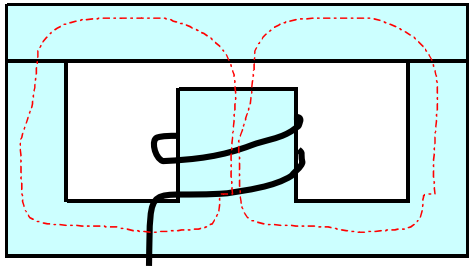
Beware of possible fringing field generated adjacent to the gaps



Shielded Drum



Toroid Core

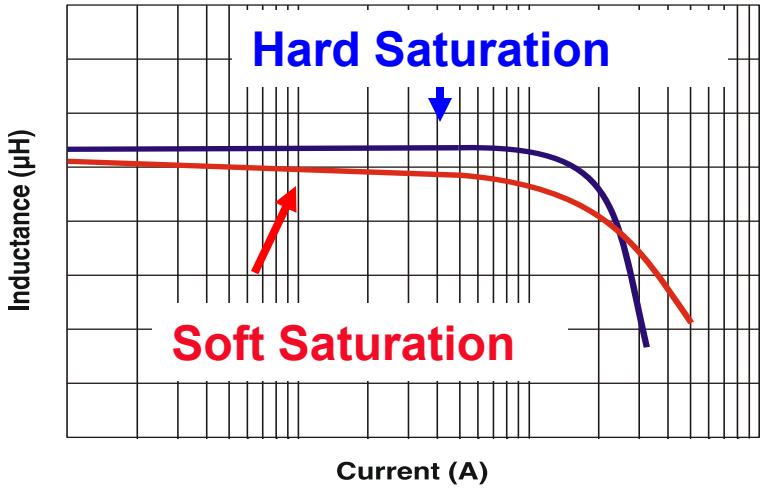


Shape Core

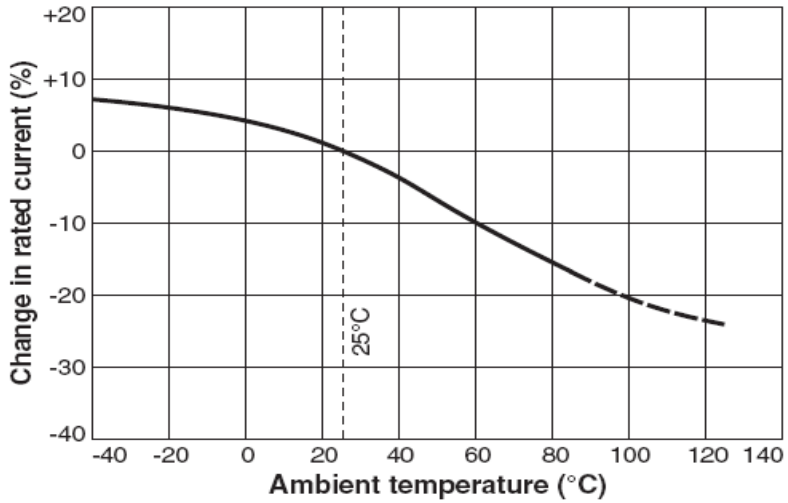
Source: PULSE Power

Inductors - Some characteristics to be aware of

- Saturation

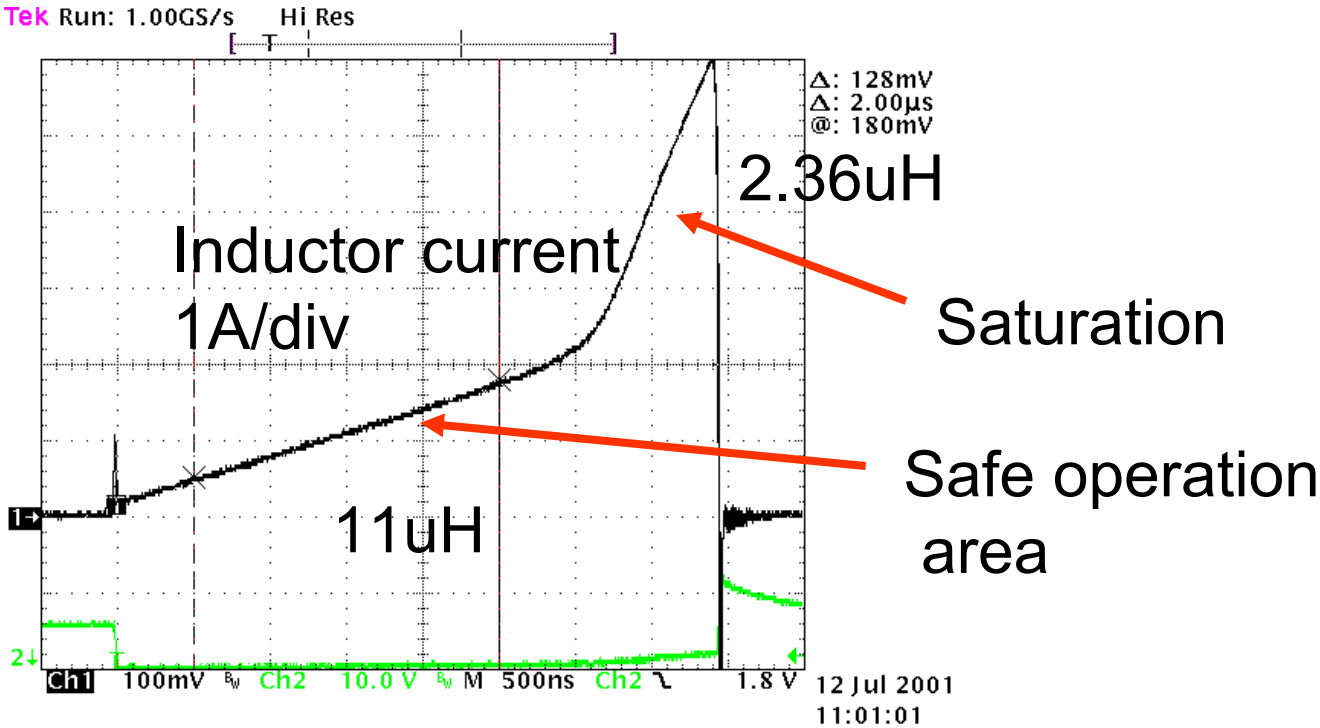


- Temperature Dependency of I_{Sat}
  - Inductor loss will cause temperature rise
  - Saturation current will drop during operation



- **A saturated inductor** is not longer an inductor – it's just a **piece of wire !!!**
- **Each inductor manufacturer has its' own definition for saturation current!**

Effect of core saturation



Saturation causes:

- **drop of inductance**
- **increased ripple current**

Might cause:

- **triggering of over current limit**
- **feedback loop instability (changed L)**
- **thermal run-away (increased I_{L_RMS})**

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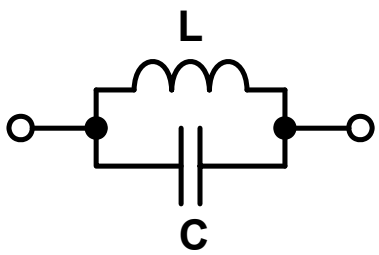
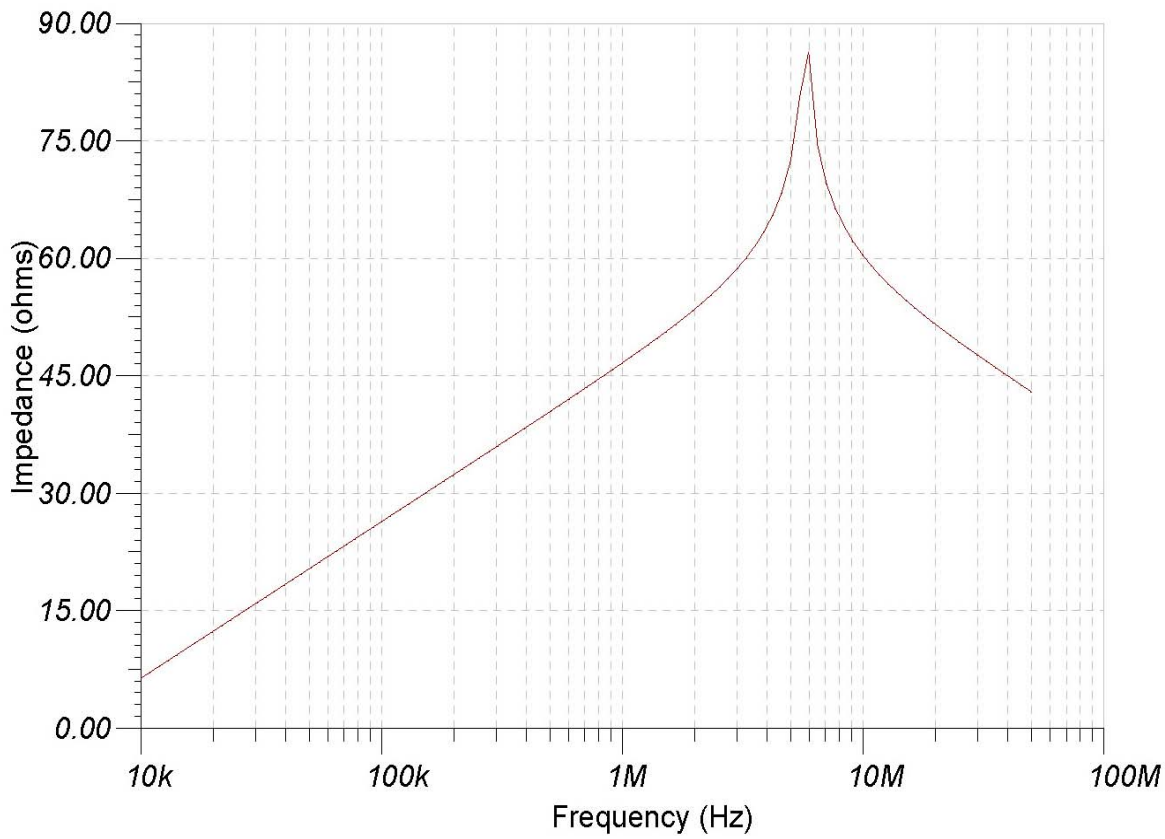
Inductors – Self resonance



- Real-world inductors => parasitic capacitance
- $f_{LC} >> f_{sw}$!!!



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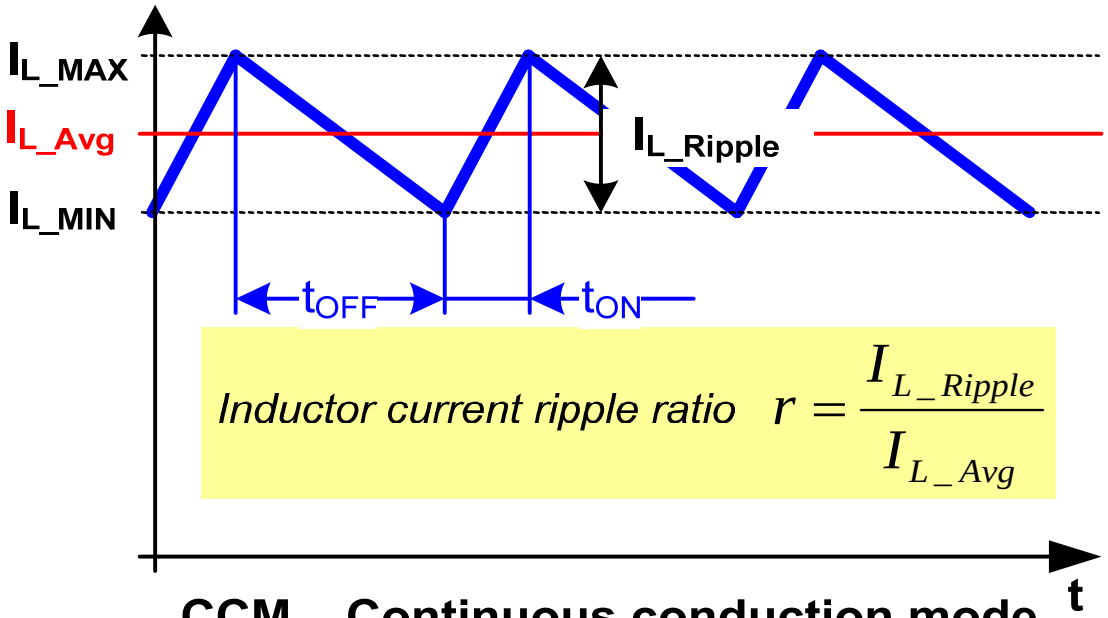
Inductors – Inductor current in CCM



Inductor current ripple ratio $r = \frac{I_{L_Ripple}}{I_{L_Avg}}$

CCM – Continuous conduction mode
(Inductor current is continuous)

CCM Mode	I_{L_Avg}
Buck	I_{OUT}
Boost	$\frac{I_{OUT}}{1-D}$
Buck- Boost	$\frac{I_{OUT}}{1-D}$

$$I_{L_Ripple} = \frac{V}{L}\Delta t$$

$$I_{L_Max} = I_{L_Avg} + \frac{I_{L_Ripple}}{2}$$

$$I_{L_RMS} = I_{L_Avg}\sqrt{1+\frac{r^2}{12}}$$

Inductors – General design guidelines (CCM)

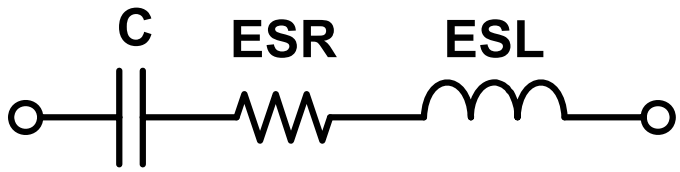
- Design for $r \sim 0.3 \ldots 0.5$; **0.4 is kind of optimum**
- Ensure that:
  - $I_{L_Max} < I_{Sat\ (of\ selected\ Inductor)}$,
  - $I_{L_Max} < I_{RMS(of\ selected\ Inductor)}$ and
  - $I_{L_Max} < I_{Current\ Limit}$ (*of selected* Switching Regulator)
- Apply adequate margin for larger I_{L_Max} under transient
  conditions (increased D to cover sudden load steps)

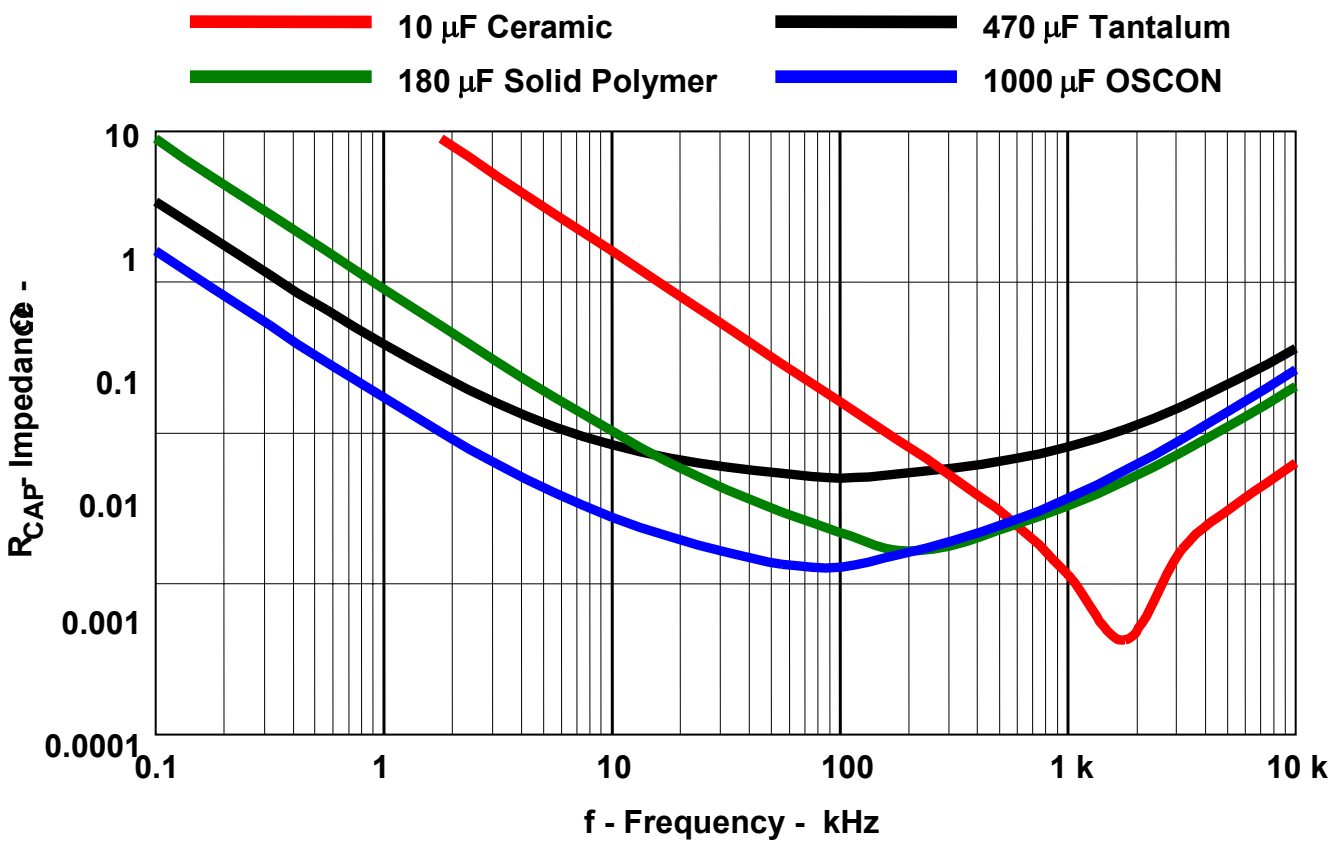
Capacitors (SMD) used as CIN and COUT

	Size	ESR	Cost	Current Rating
Std Al Electrolytic	large	high	lowest	low
OSCON		low	medium	high
Solid Polymer (SP)	medium	medium / low	very high	medium
POSCAP		low	high	medium
Tantalum	medium	medium	medium	medium
Ceramic	small	very low	low … very high	high

- Al Electrolytic:
  - \+ Cheapest
  - \- ESR varies greatly over temp
  - \- Low performance
- Tantalum:
  - \- Short circuit when they fail
- Ceramic:
  - \+ Lowest ESR, ESL → low ripple voltage, fast transient resp.
  - \- Limited by value <= 220uF
  - \- Sensitive to mechanical stress (cracking)
  - \- Microphonic effects (audible noise generation and pick-up)
- SP , OSCON, POSCAP:
  - \- Limited operating voltage

Capacitors – Impedance characteristic





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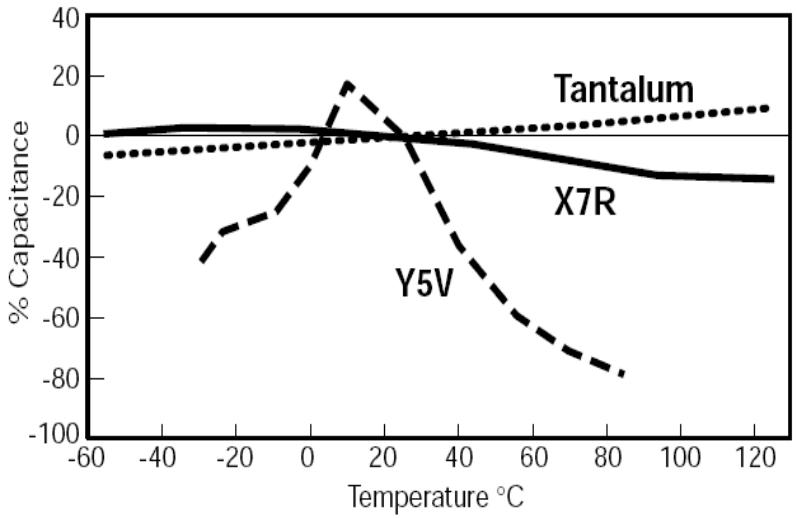
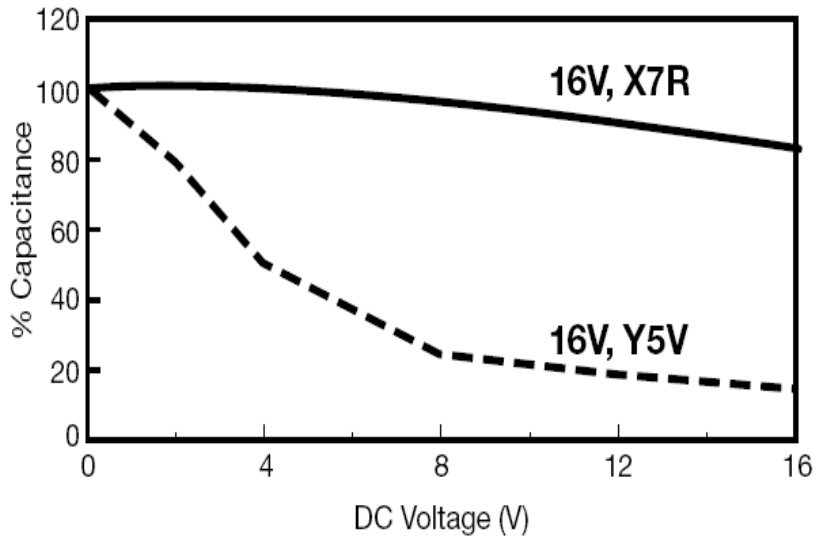
Capacitors – Some effects to be aware of

Temperature Dependency of Capacitance



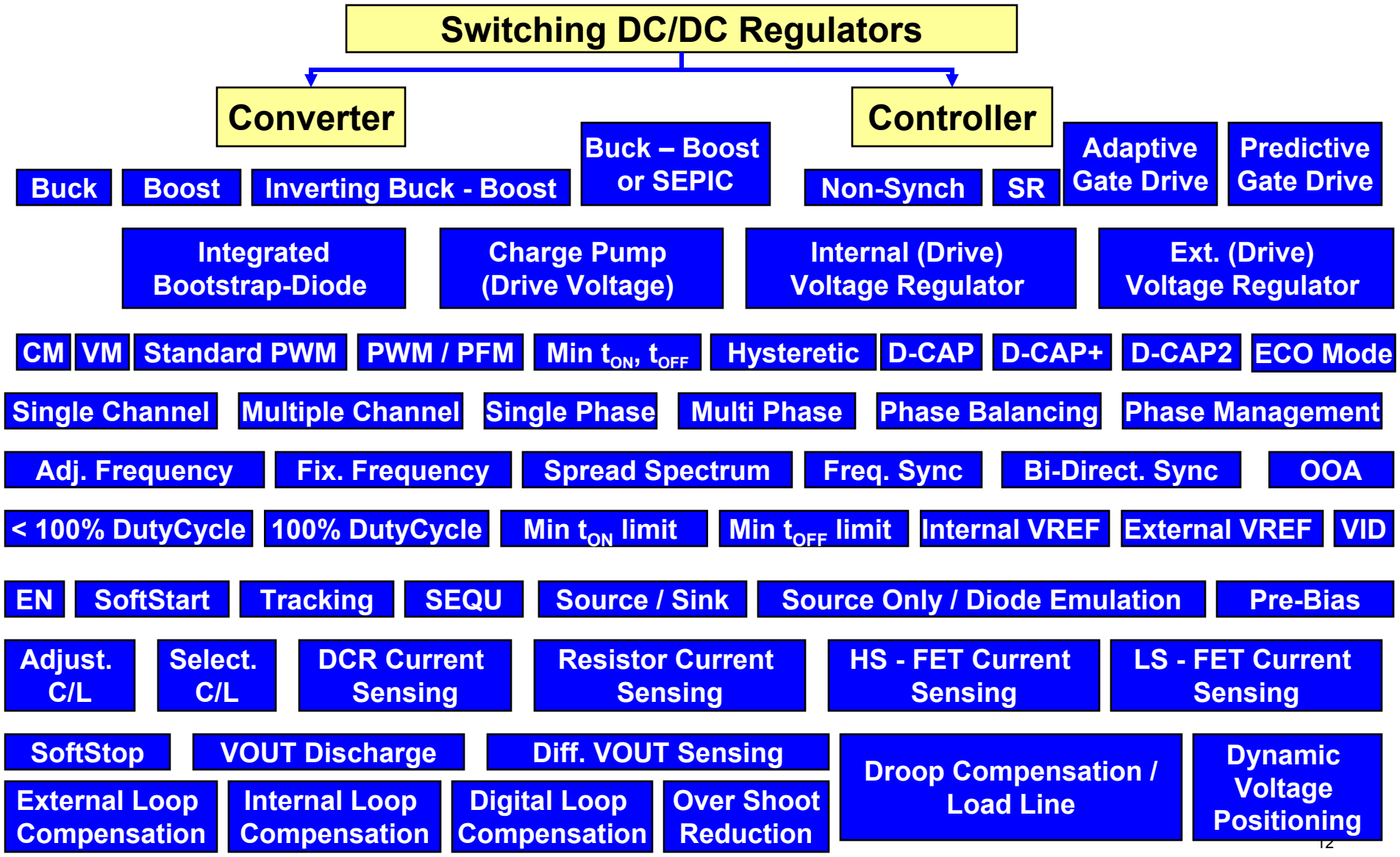
DC Bias Dependency of Capacitance



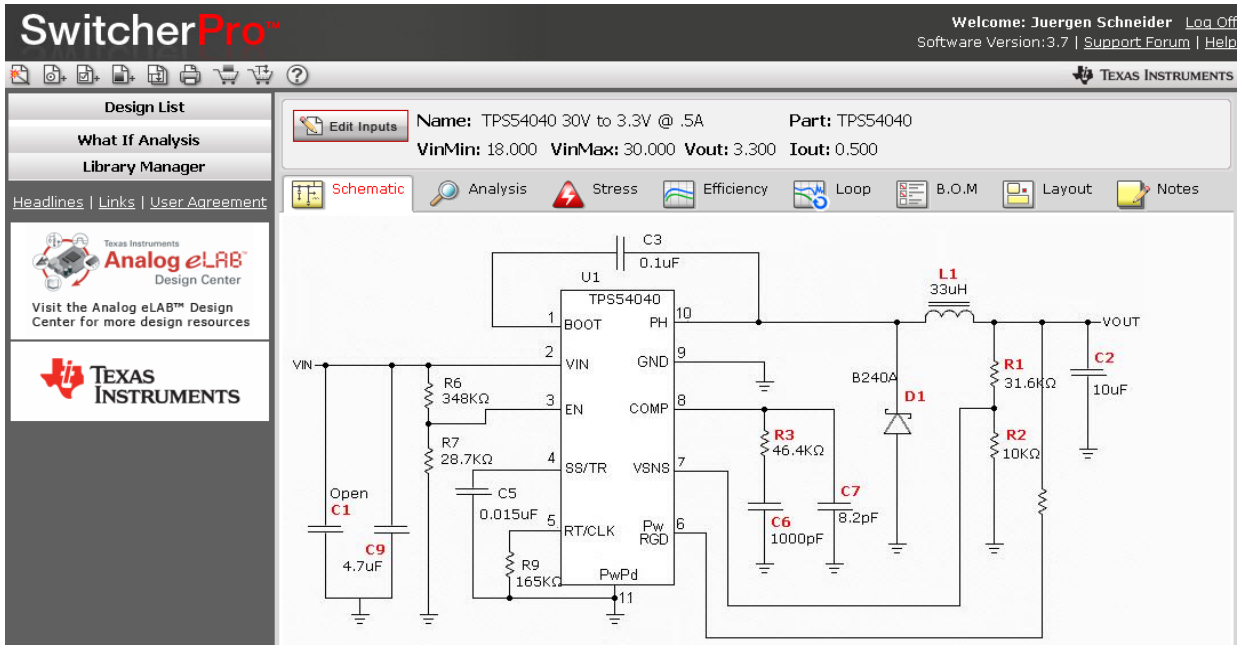
Source: "Comparison of multilayer ceramic and tantalum capacitors"; Jeffrey Cain, Ph.D. AVX Corp.

Further recommended reading: "Capacitors for Switching Power Supplies"; Dr. Ray Ridley, Ridley Engineering

The universe of switching regulators

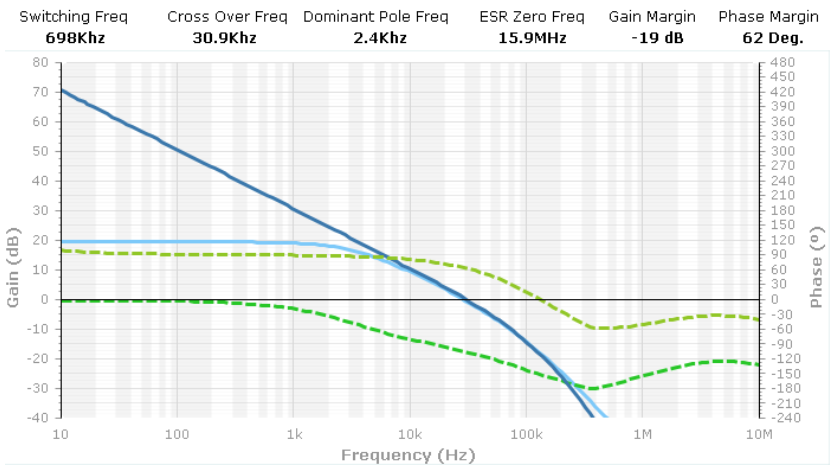


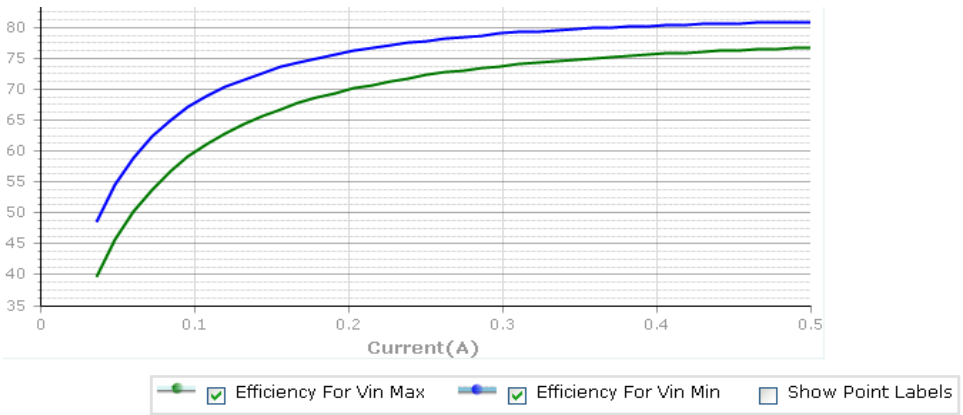
Ease your design challenge - SwitcherPro™



Design and Verification

- Part selection
- Schematic
- BOM
- Loop response
- Efficiency
- What-if analysis
- Stress Analysis
- Extensive library
- Use of own components
- Layout
- …





Agenda

- Characteristic of passive and active components
- **Special circuits**
- Thermal Design
- Improved measurement techniques
- Layout

TPS40200

WIDE INPUT RANGE NON-SYNCHRONOUS VOLTAGE MODE CONTROLLER

FEATURES

- Input Voltage Range 4.5 to 52 V
- 700 mV 1% Reference Voltage
- External Synchronization

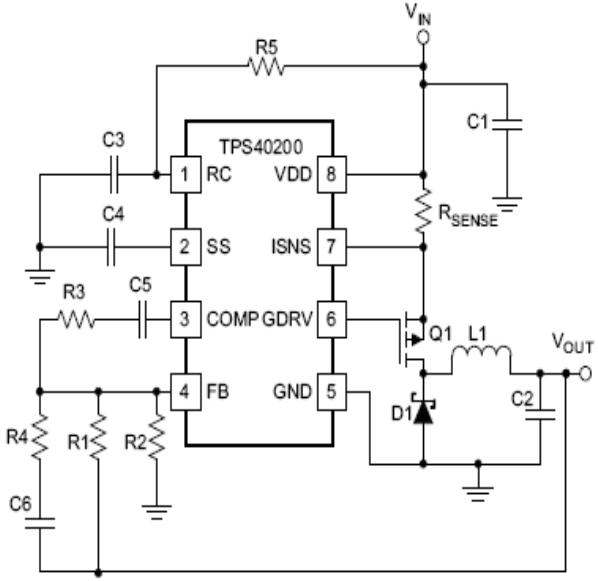
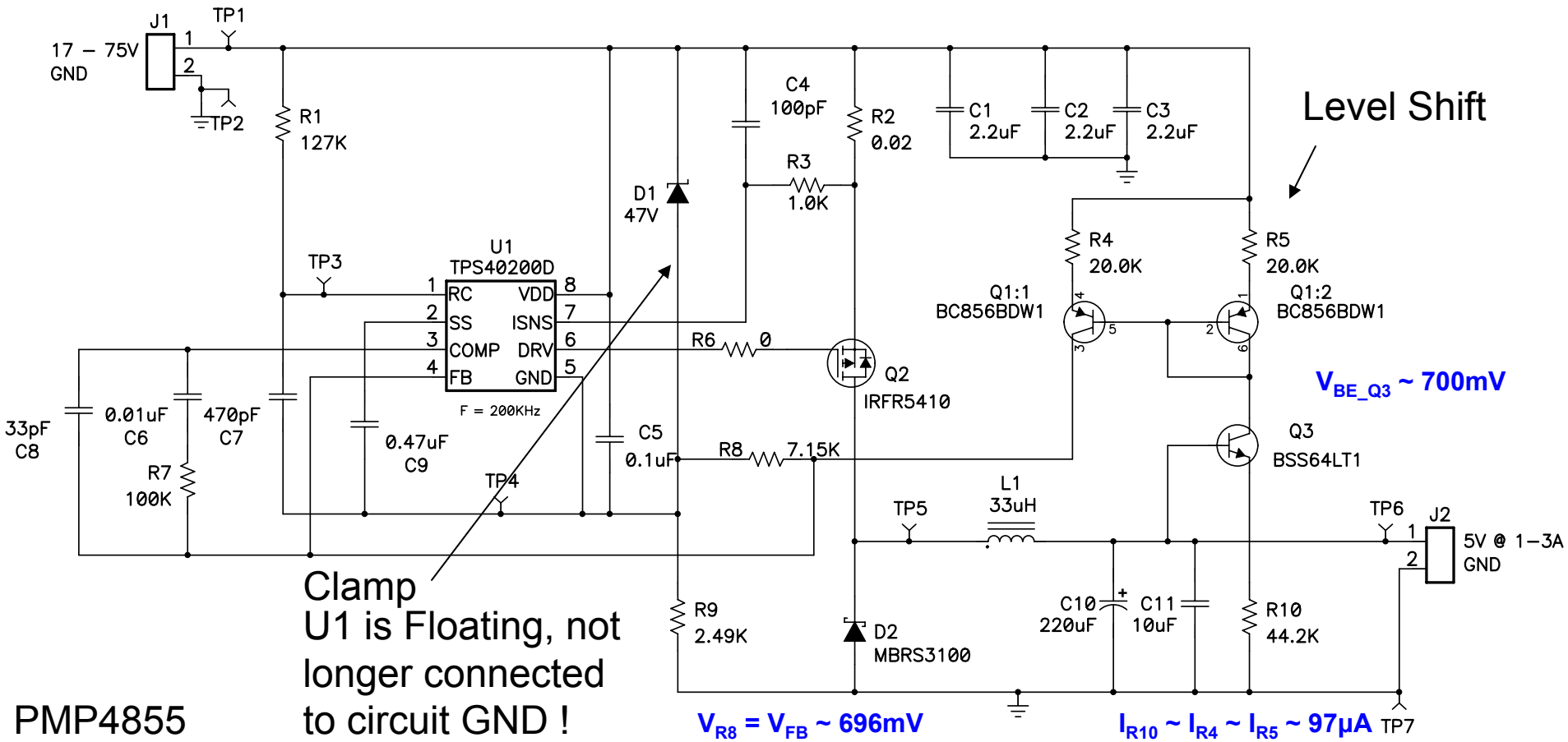


Figure 1. 12 V to 5 V Buck Converter with 94% Efficiency

Extending TPS40200 Vin



PMP4855

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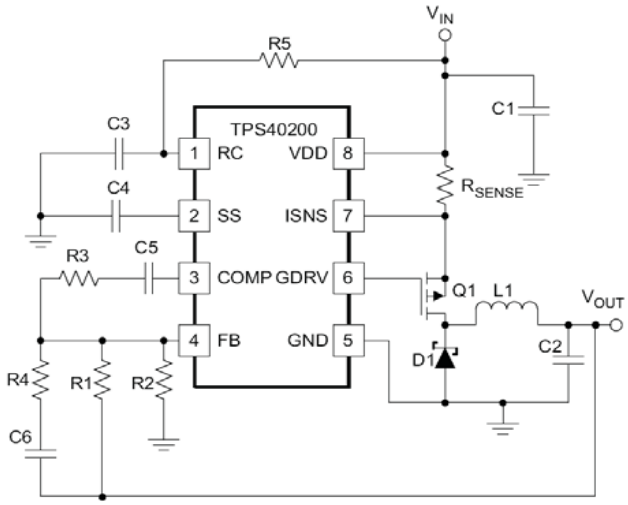
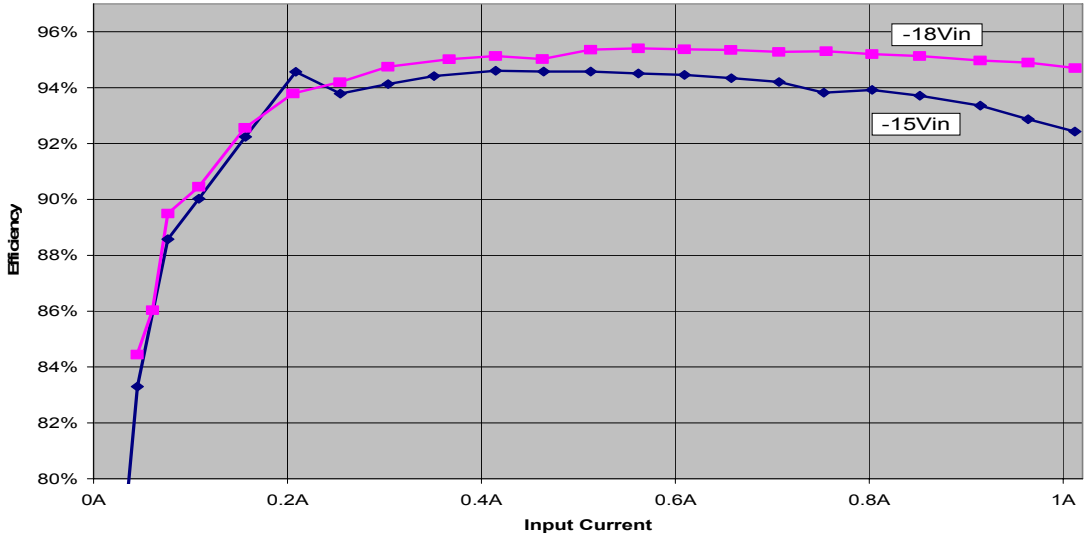
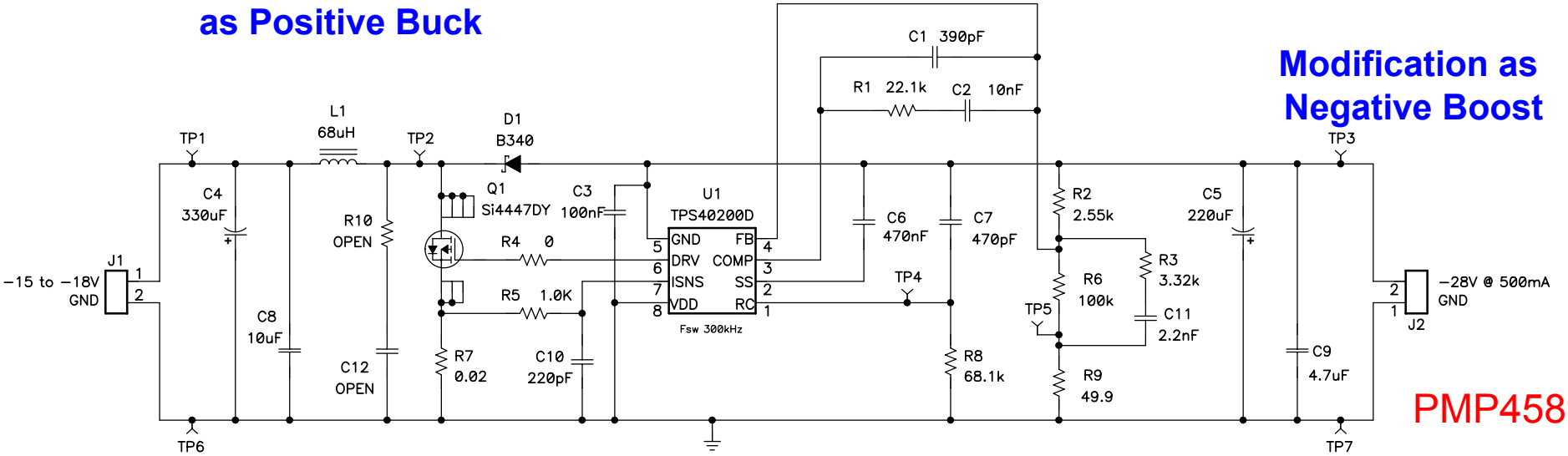
Negative Boost





Standard Use of TPS40200 as Positive Buck

Modification as Negative Boost

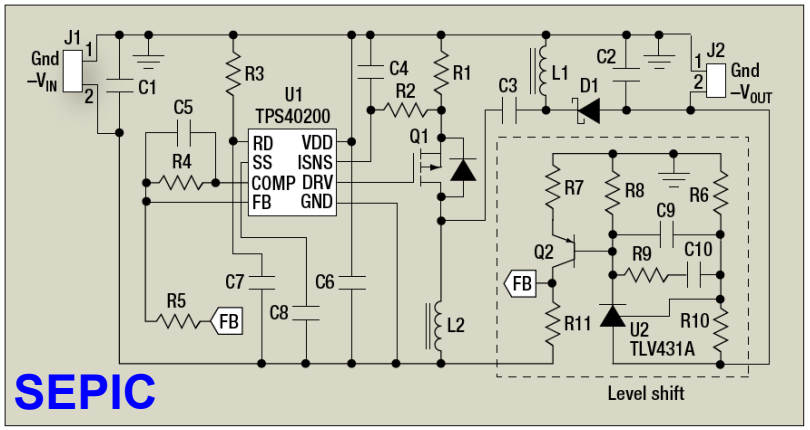


PMP4589

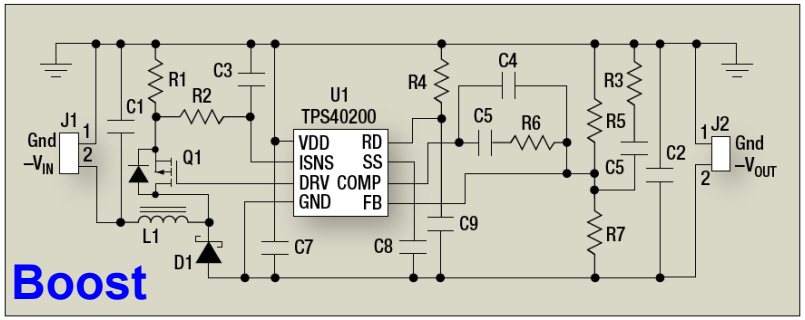
Negative Input Voltage Topologies

The Parallel Universe of Negative-Input Voltages

By John Betten and Brian King, Applications Engineers, Texas Instruments, Dallas



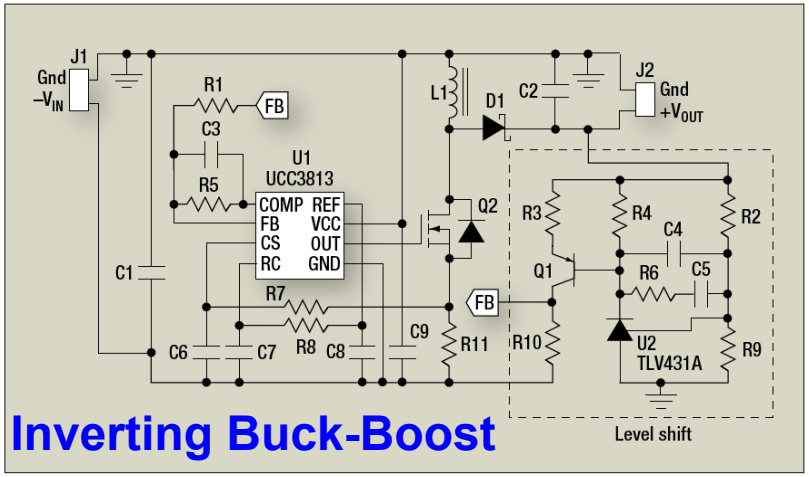
SEPIC



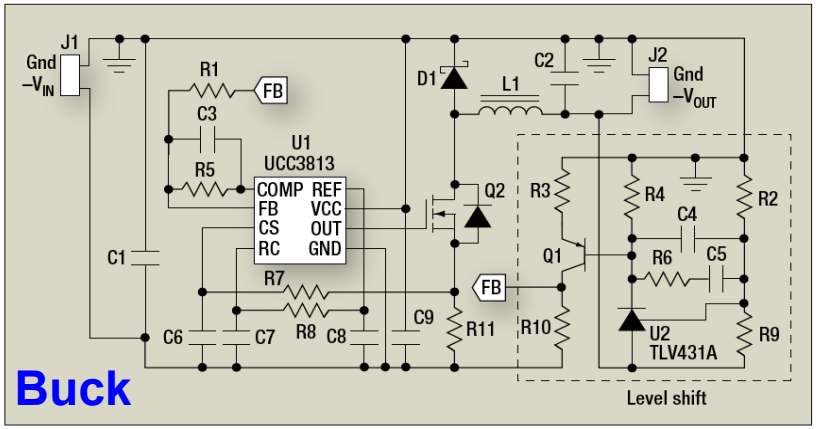
Boost

Article on www.powerelectronics.com:

http://powerelectronics.com/power_management/power_ics/807PET23-negative-input-voltages.pdf

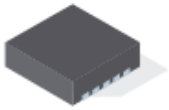


Inverting Buck-Boost



Buck

TPS40210



TPS40210, TPS40211

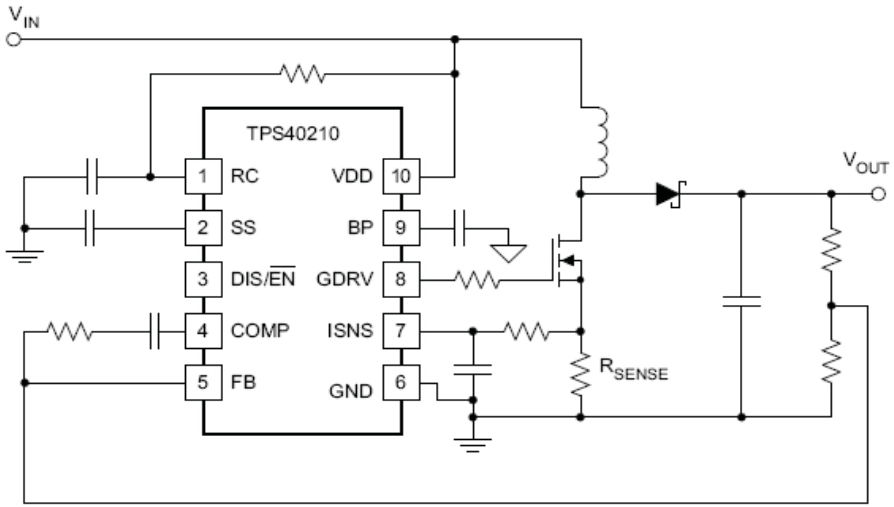
www.ti.com

SLUS772C–MARCH 2008–REVISED OCTOBER 2008

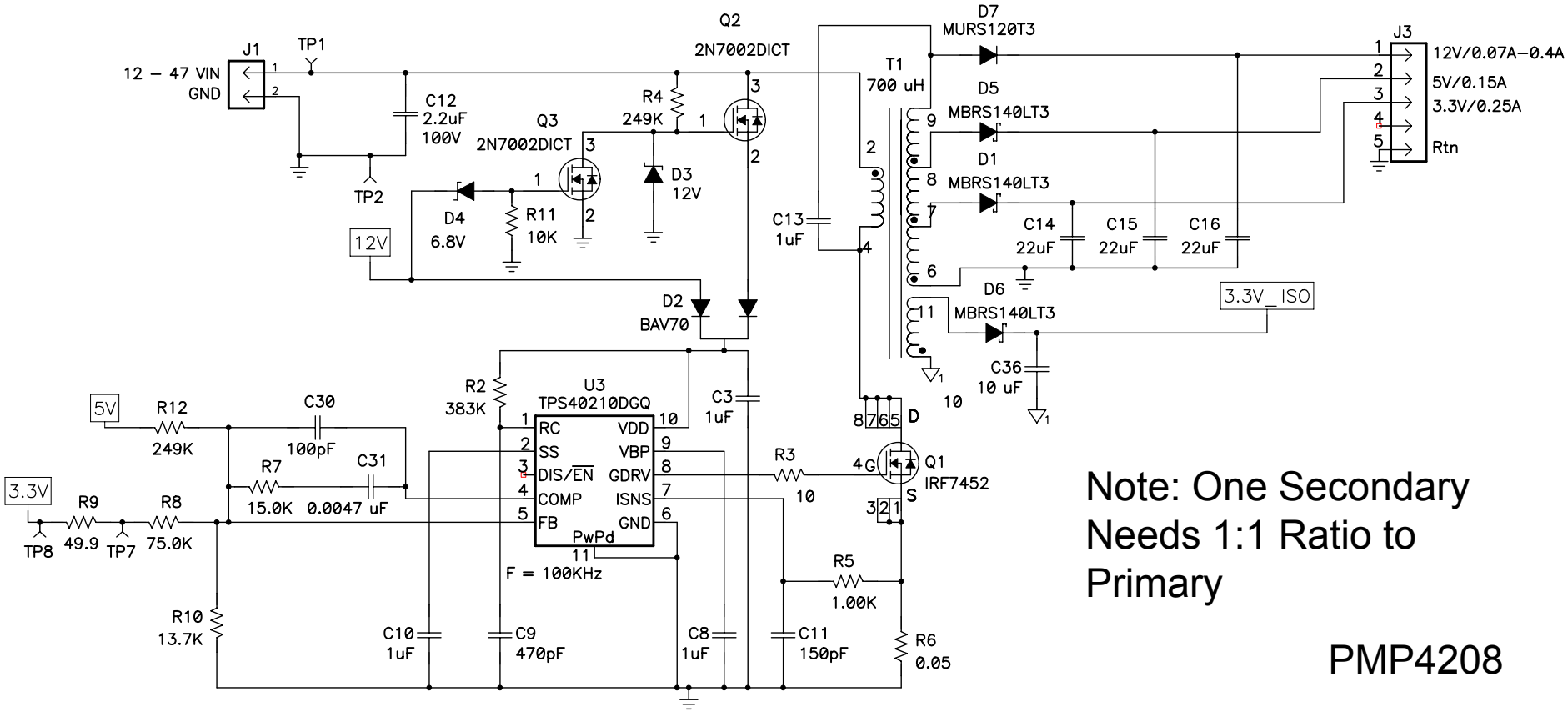
4.5-V TO 52-V INPUT CURRENT MODE BOOST CONTROLLER

FEATURES

- For Boost, Flyback, SEPIC, LED Drive Apps
- Wide Input Operating Voltage: 4.5 V to 52 V



Multi-Output TPS40210 Sepic



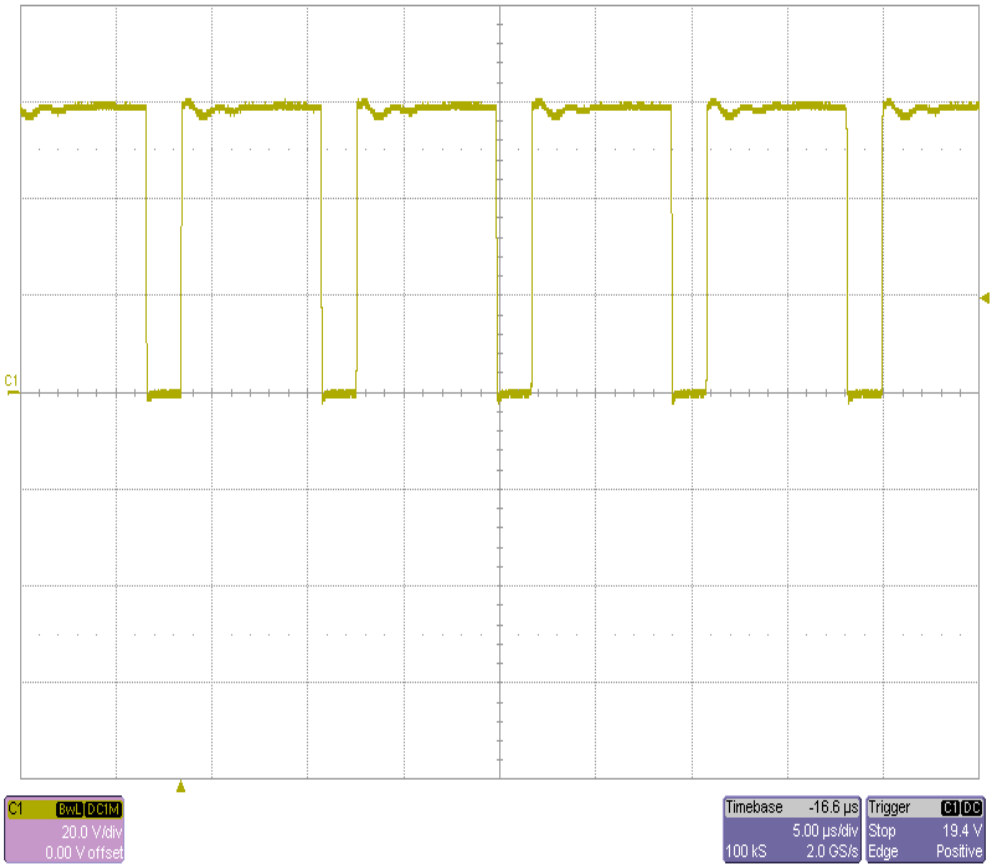
Note: One Secondary Needs 1:1 Ratio to Primary

PMP4208

See also the article “Power Tip: SEPIC converter makes an efficient bias supply” by Robert Kollman (TI) on powermanagement-europe.com:
http://powermanagementdesignline.com/howto/218900164;jsessionid=GH5TVE4AOBIDNQE1GHOSKHWATMY32JVN?pgno=1

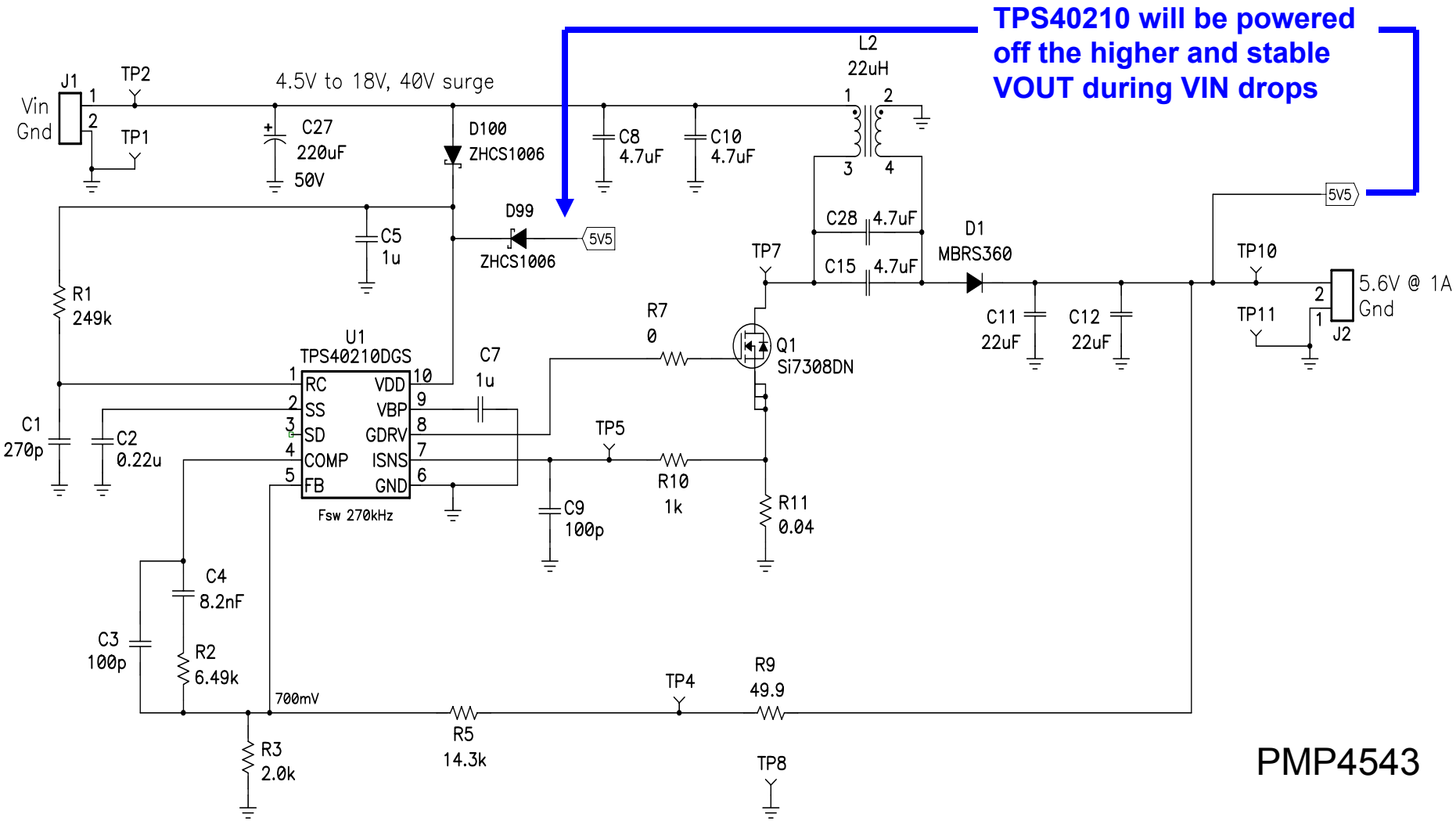
Texas Instruments

Sepic FET Drain With No Ringing



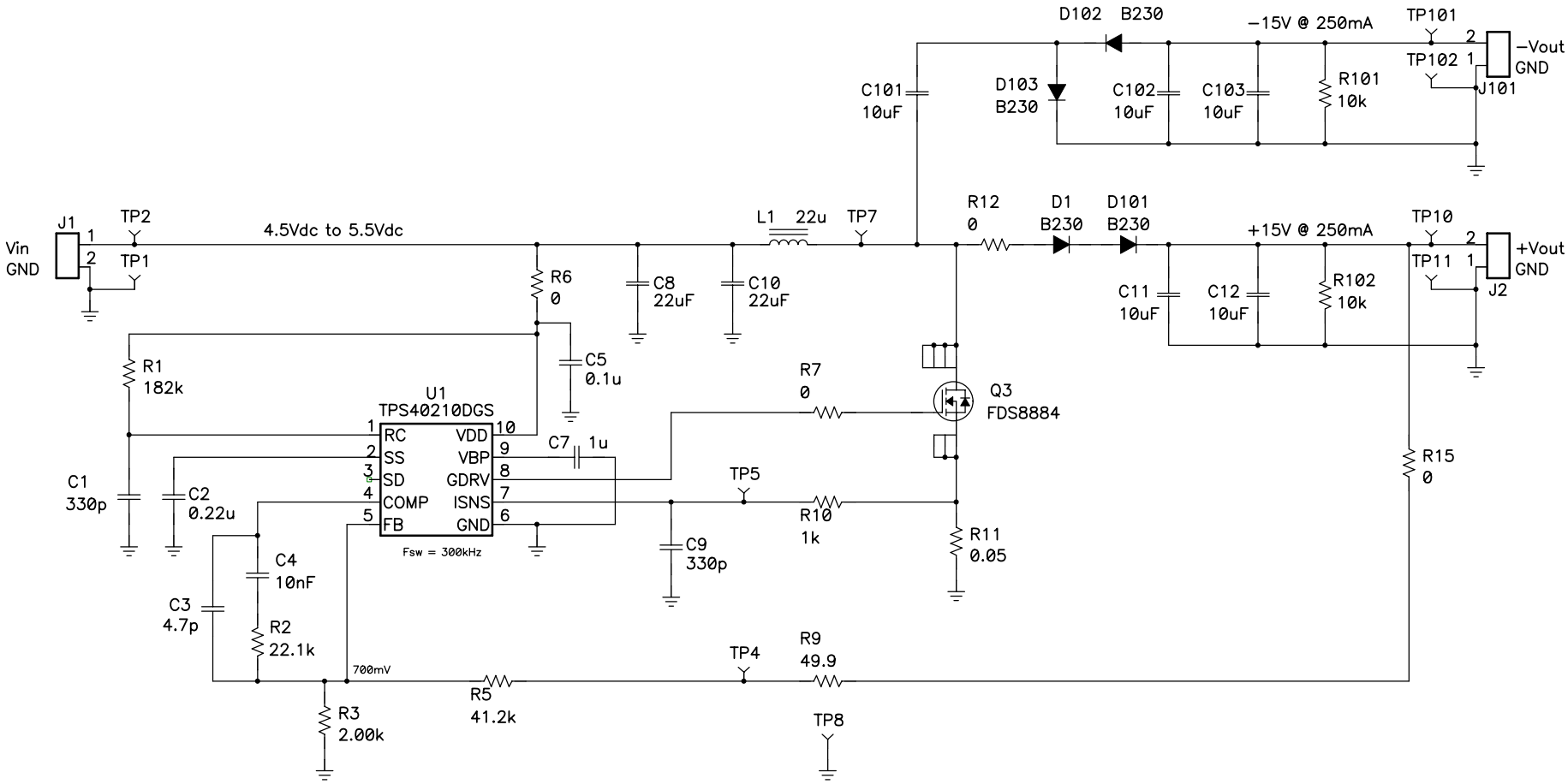
- Low Voltage Stress on Diodes And FET Compared To Flyback
- No Spiking Improves Cross Regulation (+/- 3% for the 3.3 and 5 volts)
- Multi Output Circuit was 85% Efficient

Extended Vin for TPS40210 (Lowered VIN / Cold Crank < 4.5V)



PMP4543

TPS40210 Bipolar Output

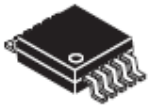


PMP2666

Texas Instruments

TPS54040 / 060

TEXAS INSTRUMENTS

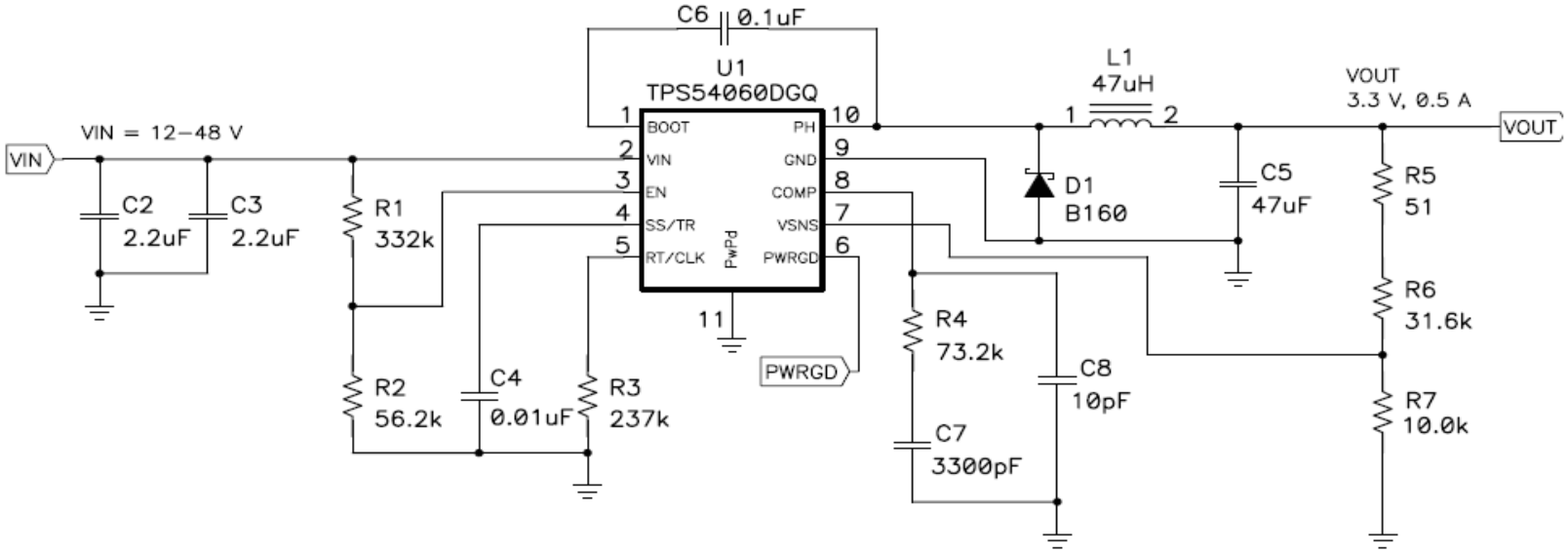


TPS54060

0.5A, 60V STEP DOWN SWIFT™ DC/DC CONVERTER WITH ECO-MODE™

FEATURES

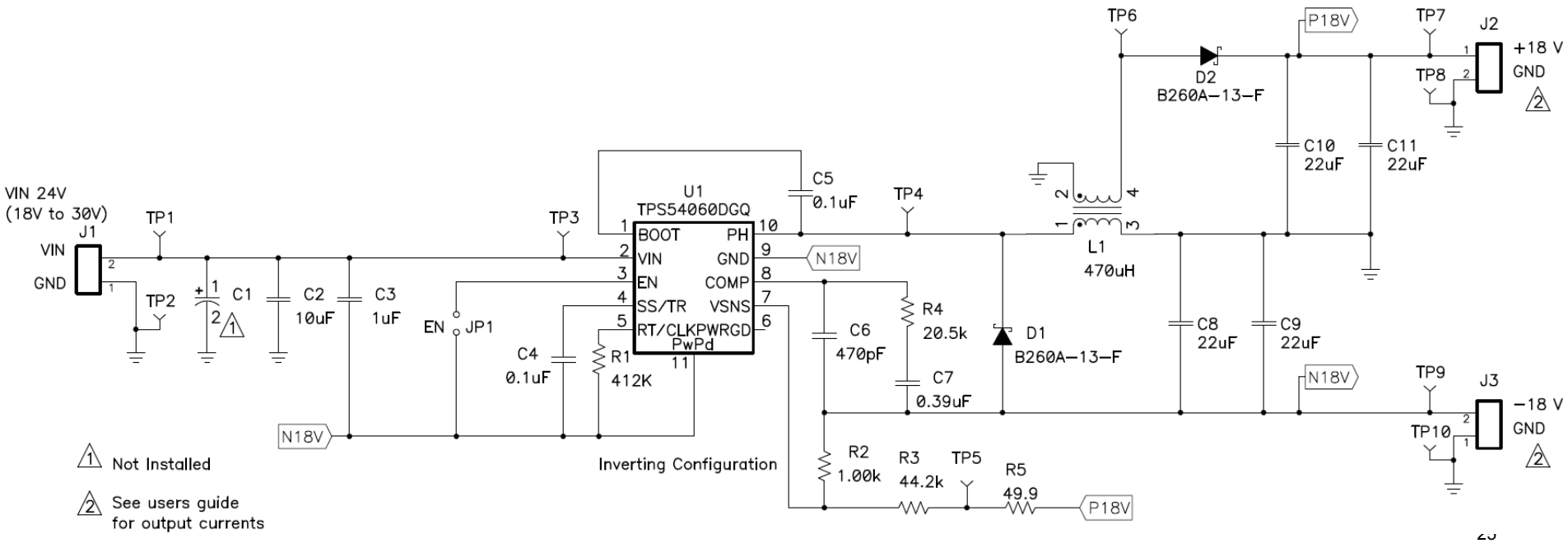
- 3.5V to 60V Input Voltage Range
- 100kHz to 2.5MHz Switching Frequency



TEXAS INSTRUMENTS

TPS54x40 / 60 used for split rail (bipolar) output

- Create a Split-Rail Power Supply with a Wide Input Voltage Buck Regulator (slva369)
- Positive and Negative Output Voltage Split Rail Calculator for SWIFT DC/DC Converters - SWIFTPOSNEG-CALC
- 18 … 30VIN, ±18V / 100 mA Split Rail SWIFT™ Converter Evaluation Module - TPS54060EVM-590 / slvu374



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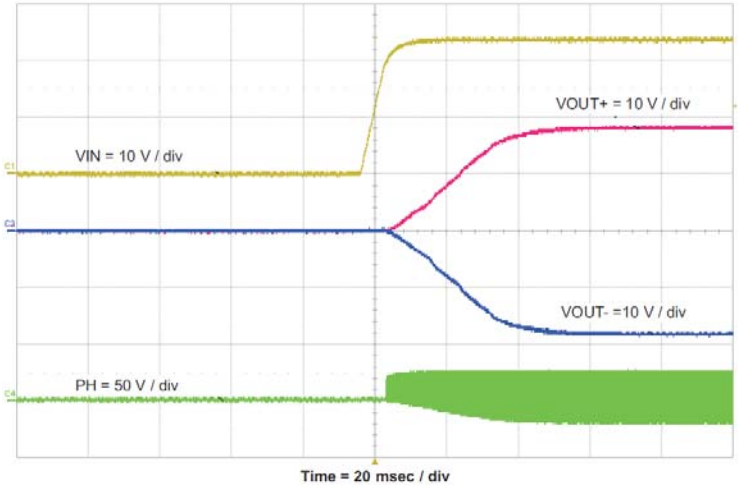
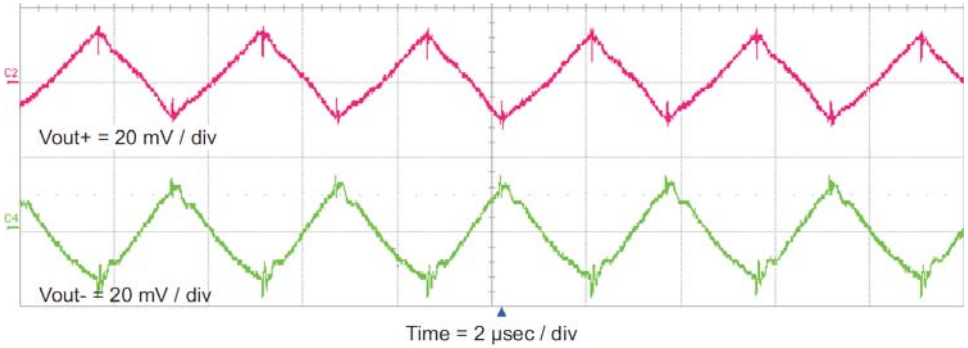
TPS54060 EVM-590: Test results

- **Split Rail (bipolar) output:**
  - Create a Split-Rail Power with a Wide Input Voltage Buck Regulator (slva369)





- **If output ripple is still too large, use additional LC filter or the new upcoming ultra high PSRR LDOs (please ask you TI FAE for more information about upcoming products)**

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TPS61175

TEXAS INSTRUMENTS

TPS61175

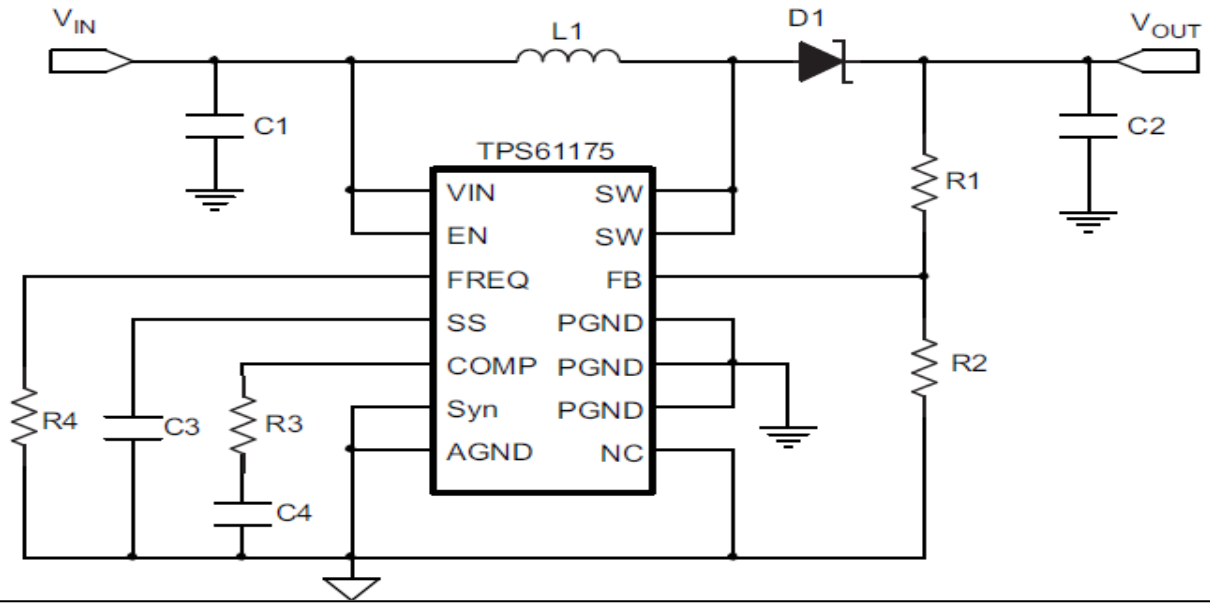
www.ti.com

SLVS892–DECEMBER 2008

3-A High Voltage Boost Converter with Soft-start and Programmable Switching Frequency

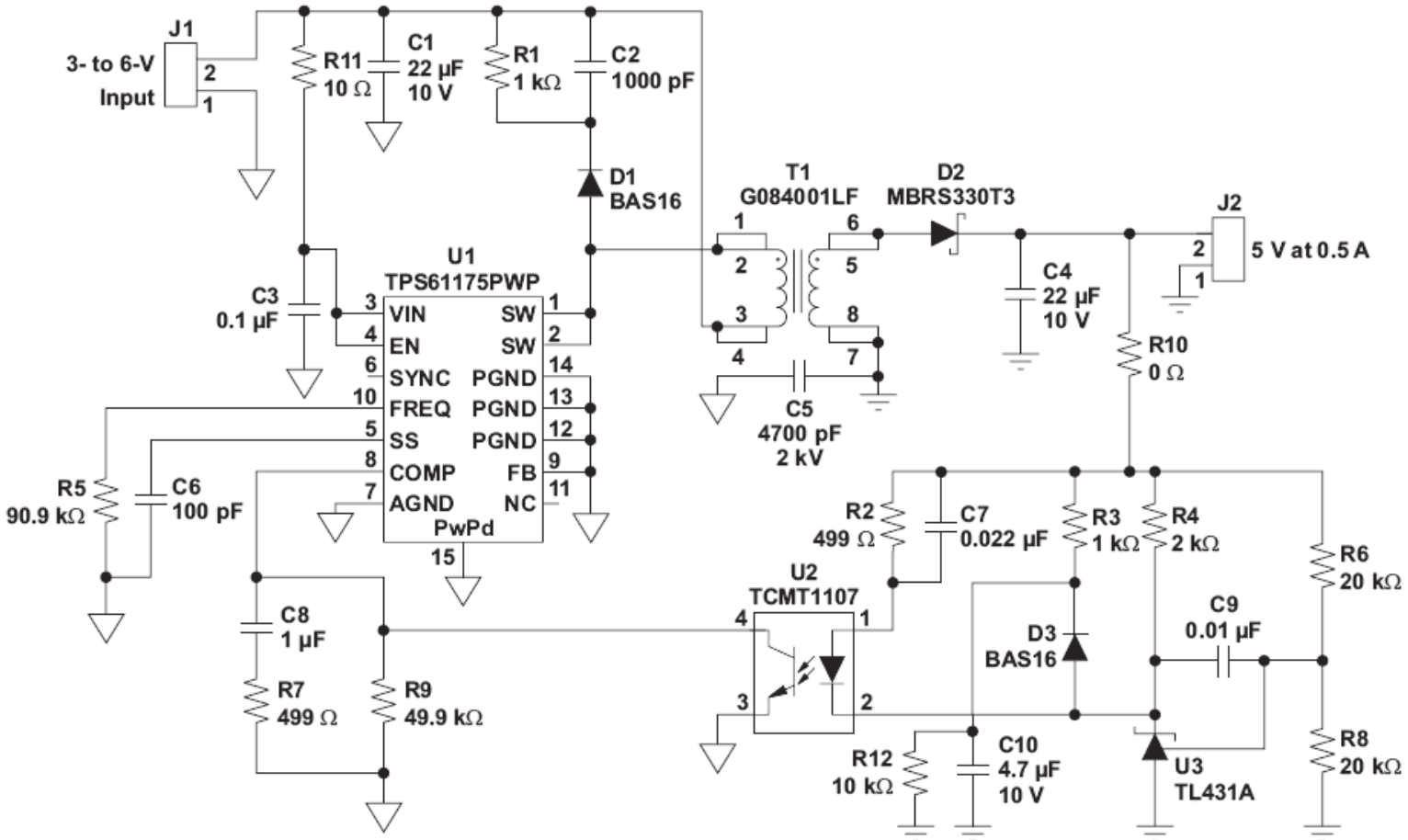
FEATURES

- 2.9-V to 18-V Input Voltage Range
- 3A, 40V Internal Switch
- Frequency Set by External Resistor: 200-kHz to 2.2-MHz



TEXAS INSTRUMENTS

TPS61175 Flyback



PMP4190

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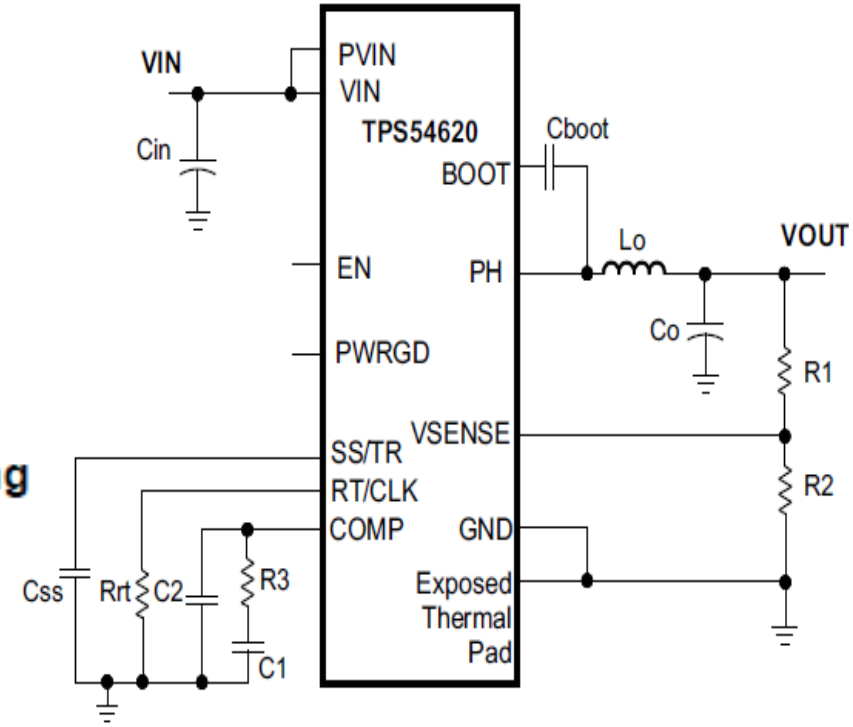
TPS54620

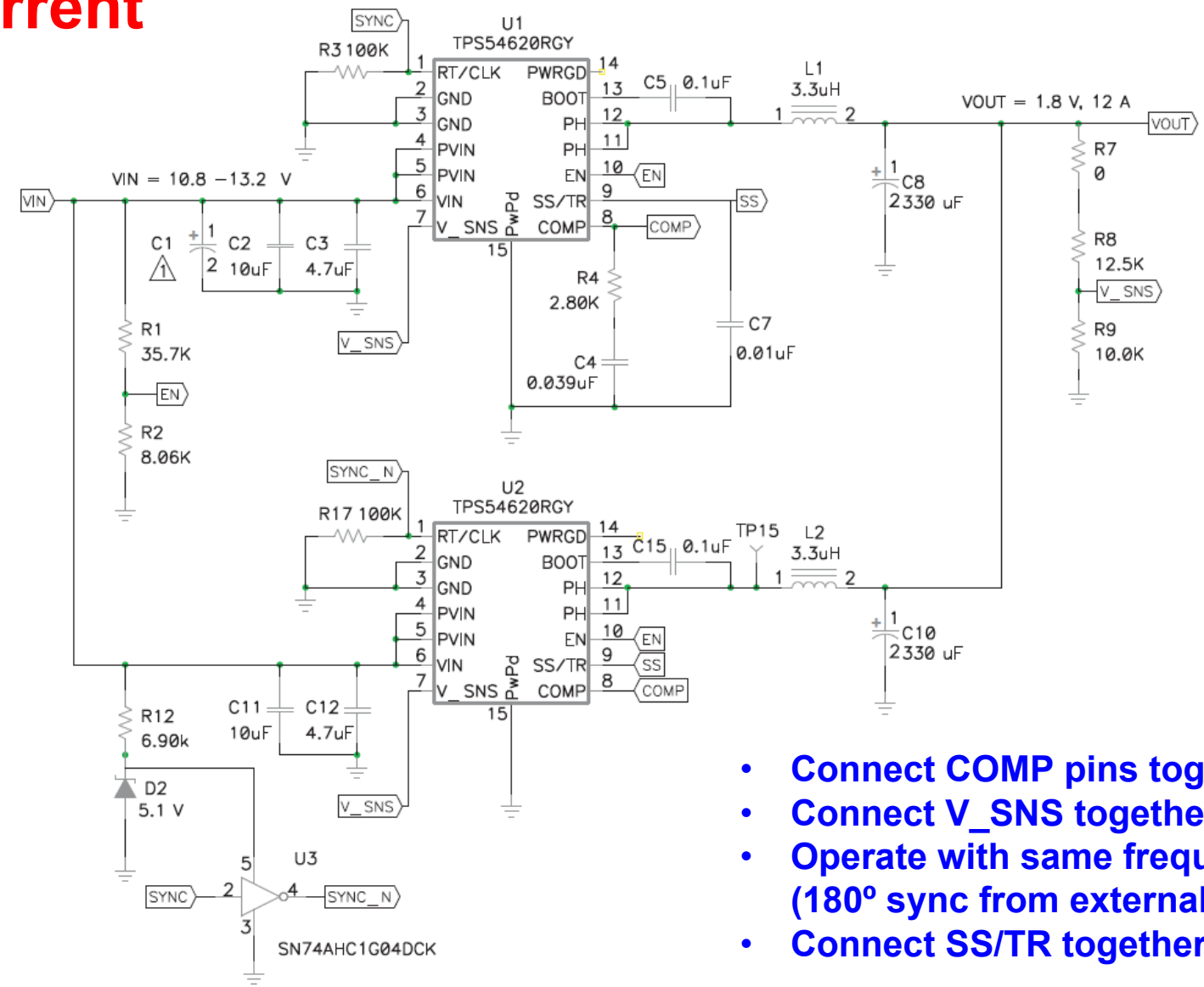
4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter

FEATURES

- Integrated 26mΩ / 19mΩ MOSFETs
- Split Power Rail: 1.6V to 17V on PVIN
- 200kHz to 1.6MHz Switching Frequency
- Synchronizes to External Clock
- –40°C to 150°C Operating Junction Temperature Range
- Adjustable Slow Start/Power Sequencing



Parallel operation of TPS54620 for higher output current



- Connect COMP pins together
- Connect V_SNS together
- Operate with same frequency (180º sync from external source)
- Connect SS/TR together

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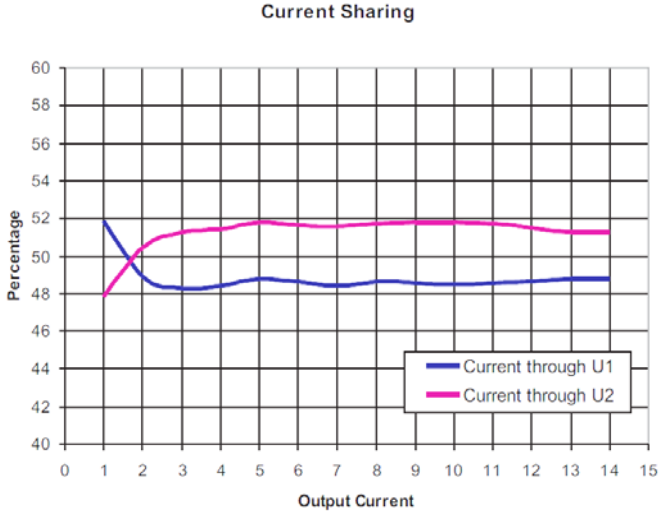
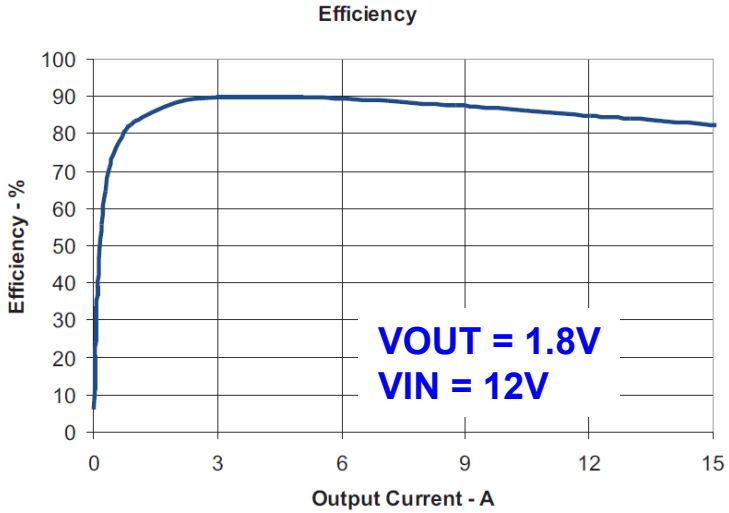
Paralleled TPS54620 - Results

- See App Note “TPS54620 Parallel Operation” (slva389)





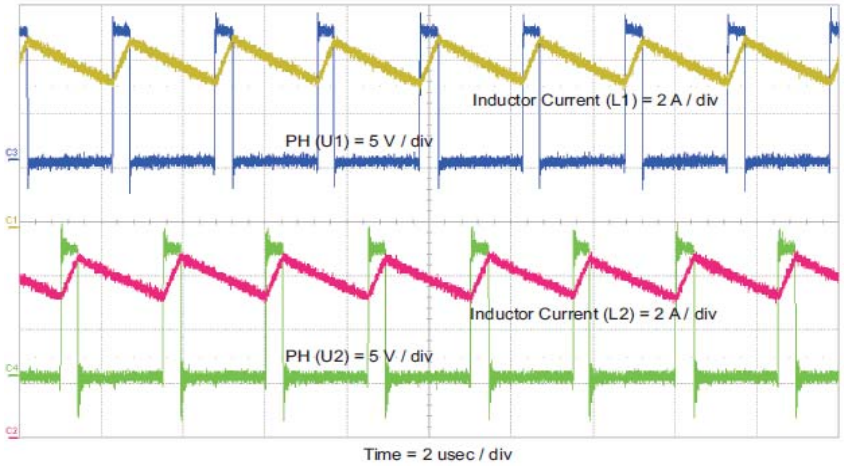
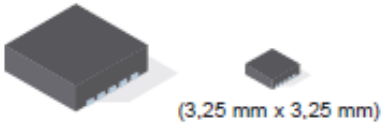


Figure 10. Switching Node and Inductor Current Waveforms

Texas Instruments

TPS6120x

TEXAS INSTRUMENTS
www.ti.com

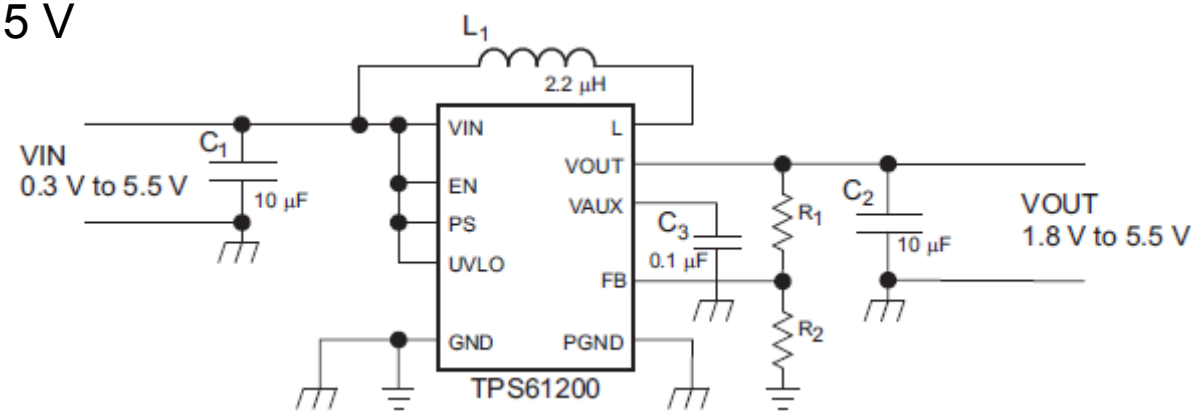


TPS61200
TPS61201
TPS61202

SLVS577B – MARCH 2007 – REVISED FEBRUARY 2008

LOW INPUT VOLTAGE SYNCHRONOUS BOOST CONVERTER WITH 1.3-A SWITCHES

- FEATURES
  - Startup into Full Load at 0.5 V Input Voltage
  - Operating Input Voltage Range from 0.3 V to 5.5 V



TEXAS INSTRUMENTS

Use of TPS61200 in solar cell application

- See App Note “Supplying TPS61200 With a Single Solar Cell” (slva345a)

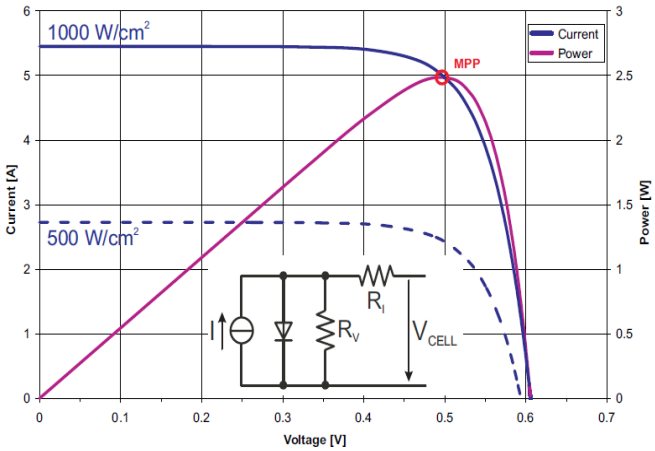
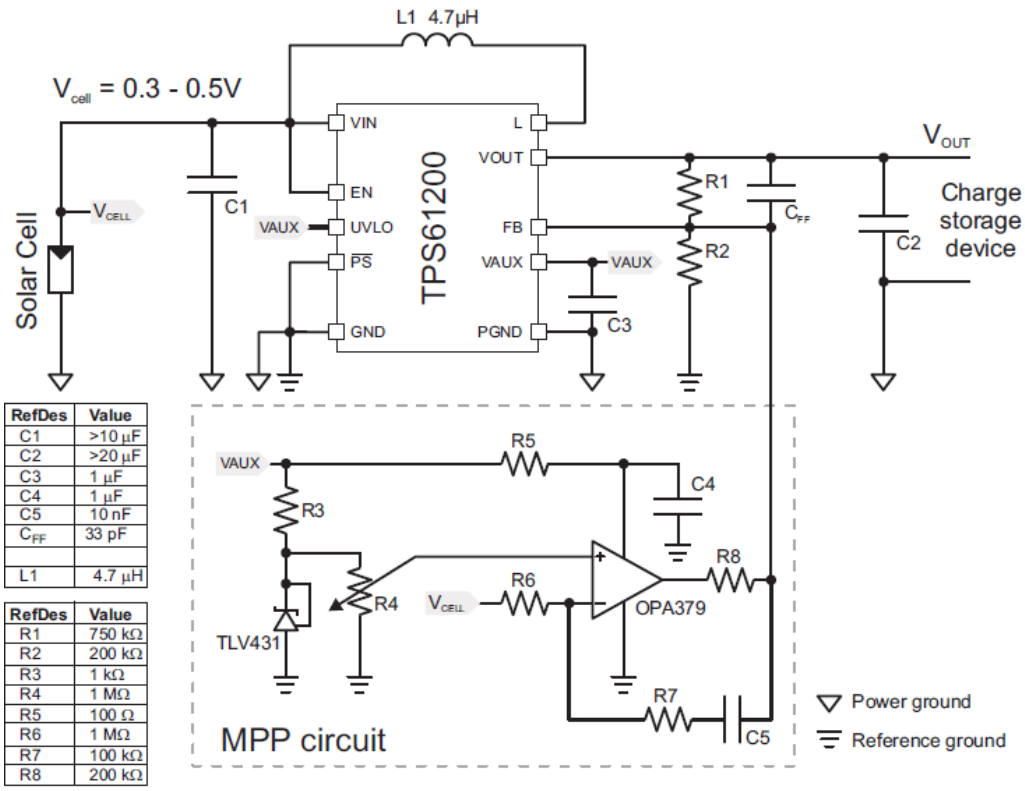


Figure 1. Typical I-V Characteristic of a Solar Cell With Equivalent Circuit Diagram

- Circuit avoids inrush current
- VAUX is active first, powers MPP circuitry
- MPP circuit cheats the boost converter, keeps input current during start-up of converter low, avoiding collaps of the solar cell



RefDes	Value
C1	>10 µF
C2	>20 µF
C3	1 µF
C4	1 µF
C5	10 nF
C_{FF}	33 pF
L1	4.7 µH

RefDes	Value
R1	750 kΩ
R2	200 kΩ
R3	1 kΩ
R4	1 MΩ
R5	100 Ω
R6	1 MΩ
R7	100 kΩ
R8	200 kΩ

Figure 2. TPS61200 Combined With MPP Circuit

Texas Instruments

TPS6420x

TEXAS INSTRUMENTS
www.ti.com

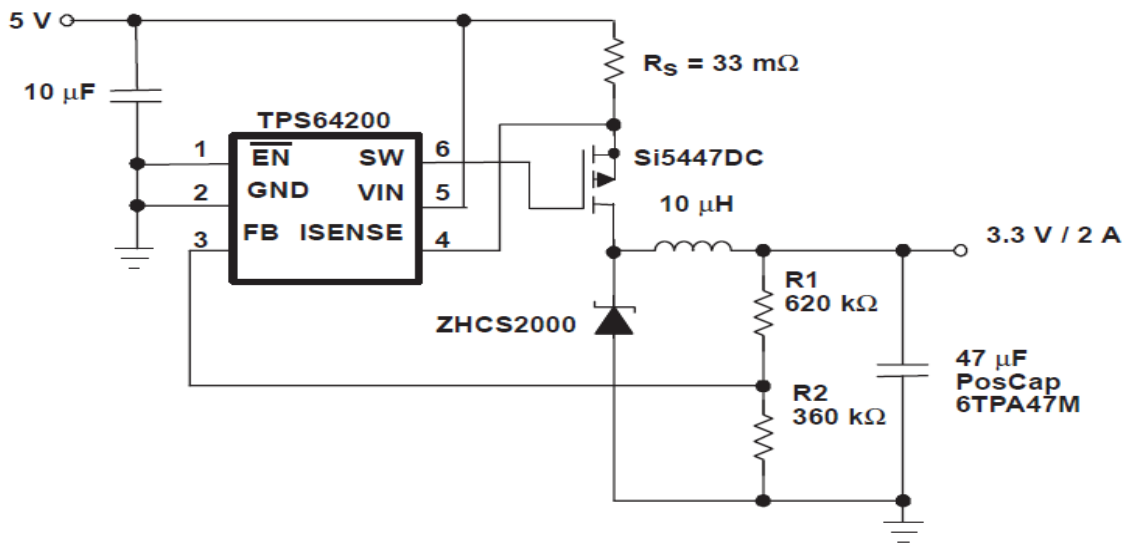
TPS64200, TPS64201
TPS64202, TPS64203

SLVS485 – AUGUST 2003

SOT23 STEP-DOWN CONTROLLER

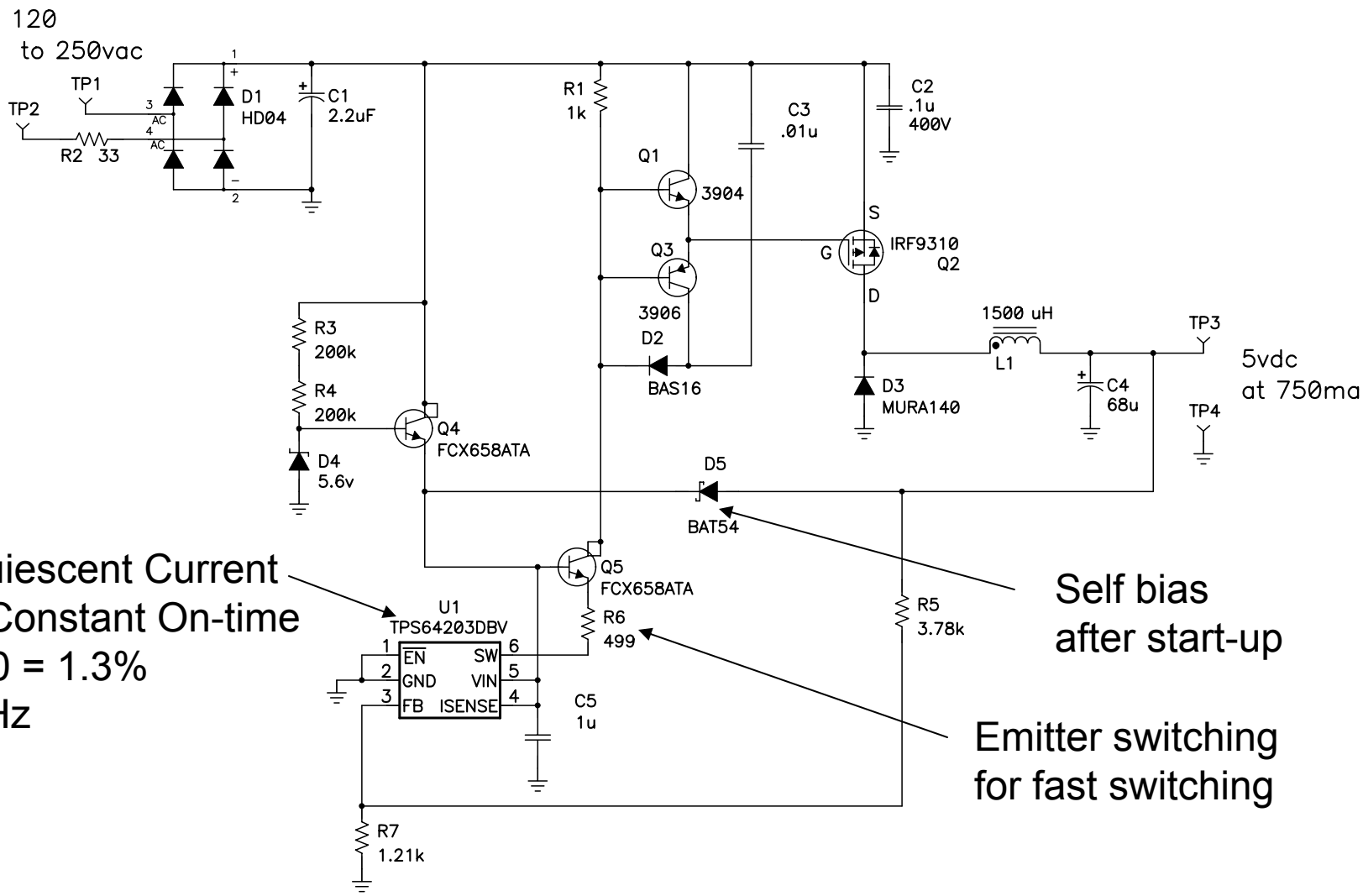
FEATURES

- Step-Down Controller for Applications With up to 95% Efficiency
- 1.8-V to 6.5-V Operating Input Voltage Range
- 20-µA Quiescent Current (Typical)



TEXAS INSTRUMENTS

Offline Buck with TPS6420x

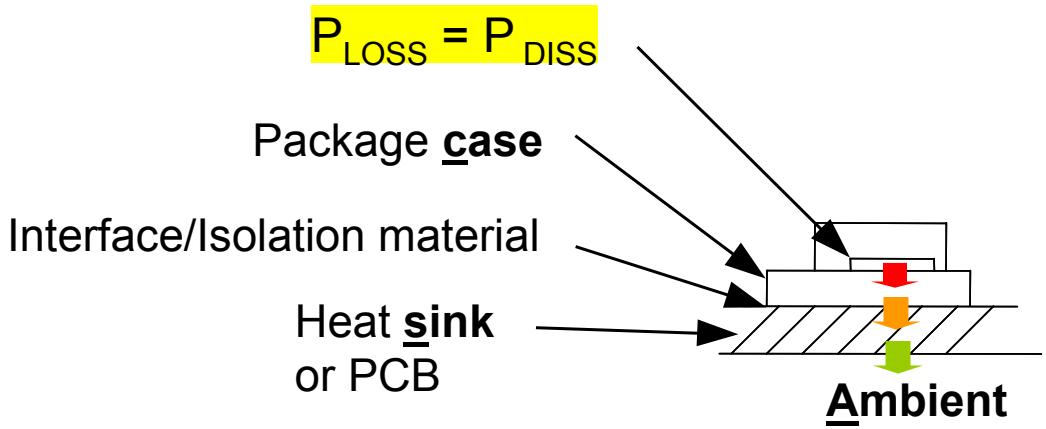


Texas Instruments

Agenda

- Characteristic of passive and active components
- Special circuit
- **Thermal Design**
- Improved measurement techniques
- Layout

Power devices - How to get rid of the heat ?

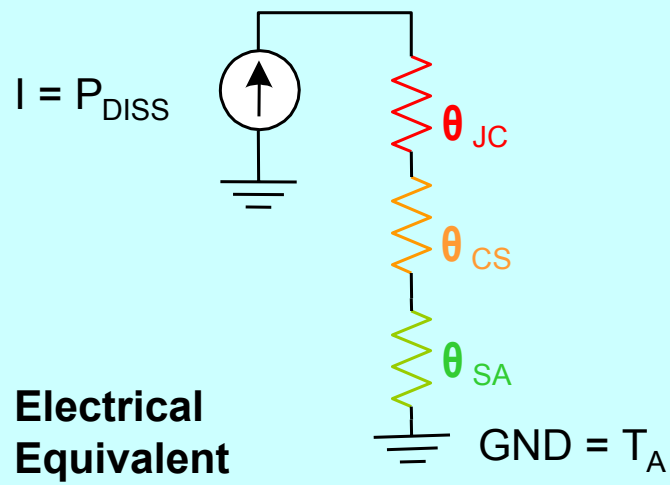


Semiconductor die **(Junction)**
Use max **recommended** junction temperature for calculations

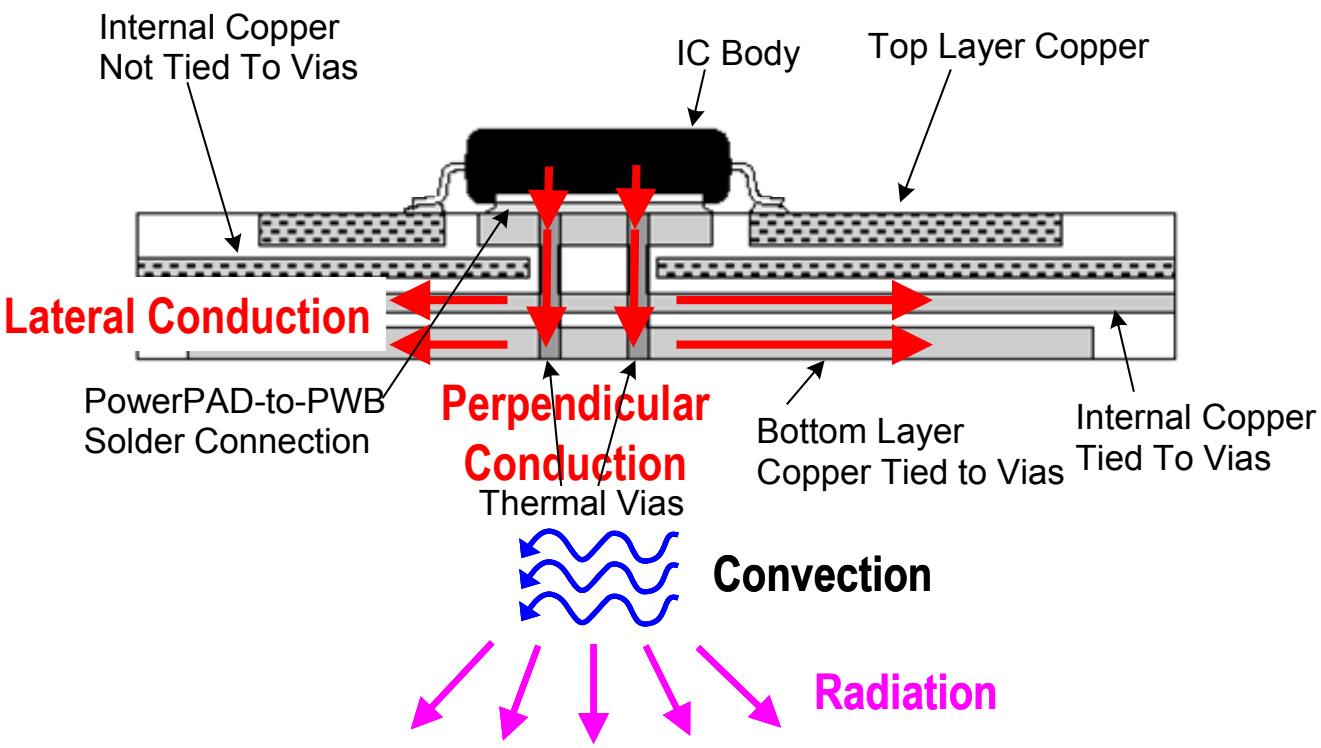
- **θjc**: Junction to case thermal resistance, usually specified
- **θcs**: Interface resistance, specified for heat sink insulators, negligible for solder connections
- **θsa**: Sink to ambient resistance, specified for heatsinks

The different thermal resistances are summed up often as **θja**, applicable for specified board construction only !

$$T_J = P_{DISS} \times (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$



Heat transfer in a surface mount cooling system

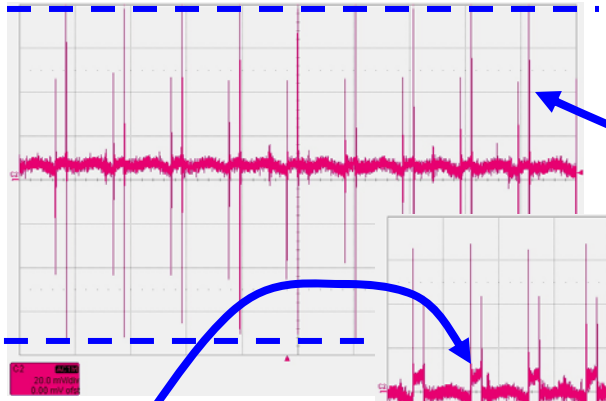


- Use multiple thermal vias
- Copper is excellent thermal conductor,
  use thick copper sheets for copper layers targeted for heat spreading
- FR4 is extremely poor heat conductor, especially in lateral direction,
  use thin FR4 layers

Agenda

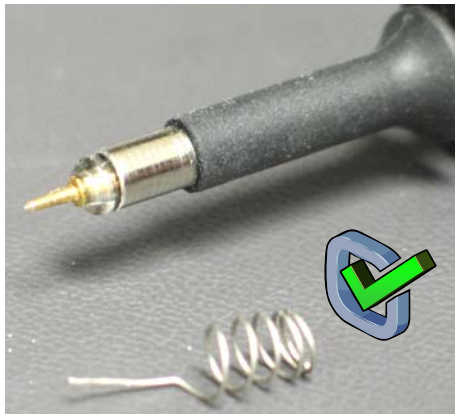
- Characteristic of passive and active components
- Special circuits
- Thermal Design
- **Improved measurement techniques**
- Layout

Oscilloscope probes – Use “tip and Barrel” method

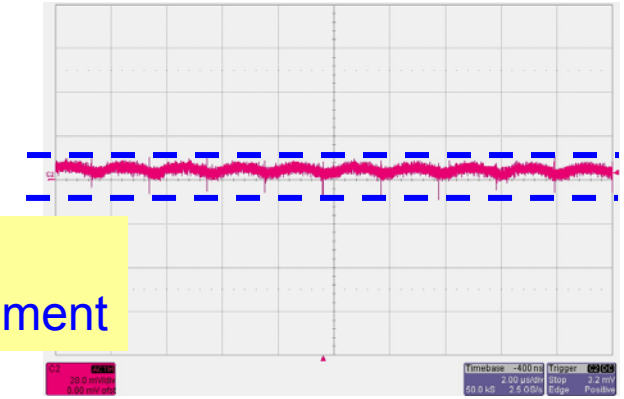


Noise pick-up by probe’s ground lead

Ground lead adjacent to inductor picks-up additional signal



Noise free measurement with “Tip and Barrel” approach

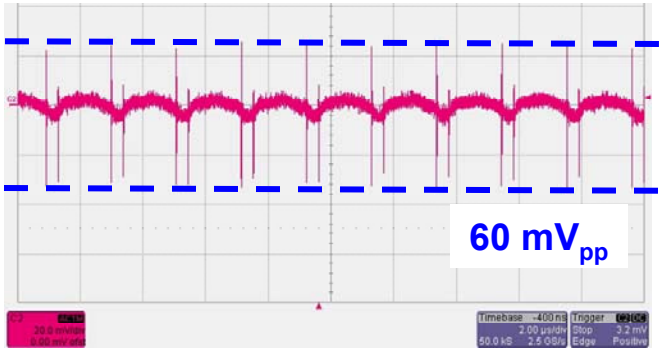


Example:
V_{OUT_Ripple} Measurement

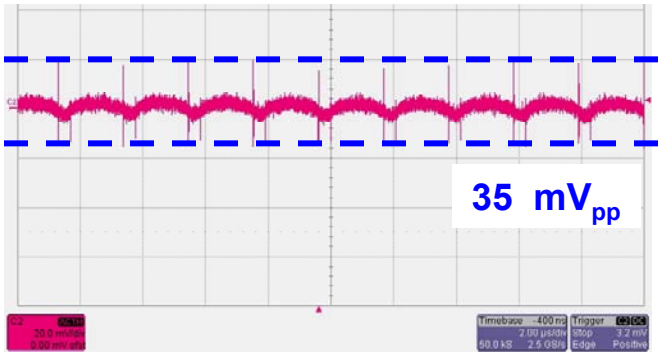
Oscilloscope probes – Suppress CM noise

Self-made common mode choke suppresses any noise coupled into the probe's cable

Example: V_{OUT_Ripple} measurement; probe's cable adjacent to inductor

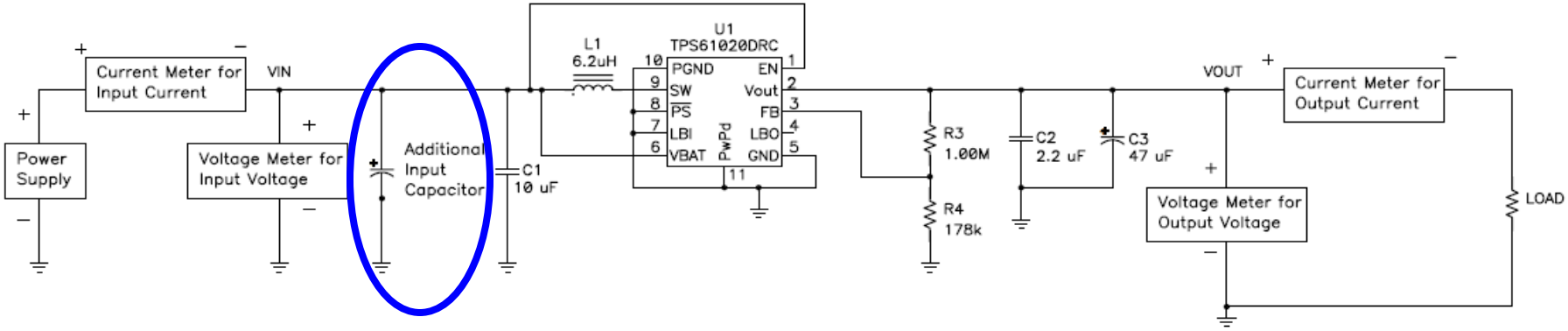


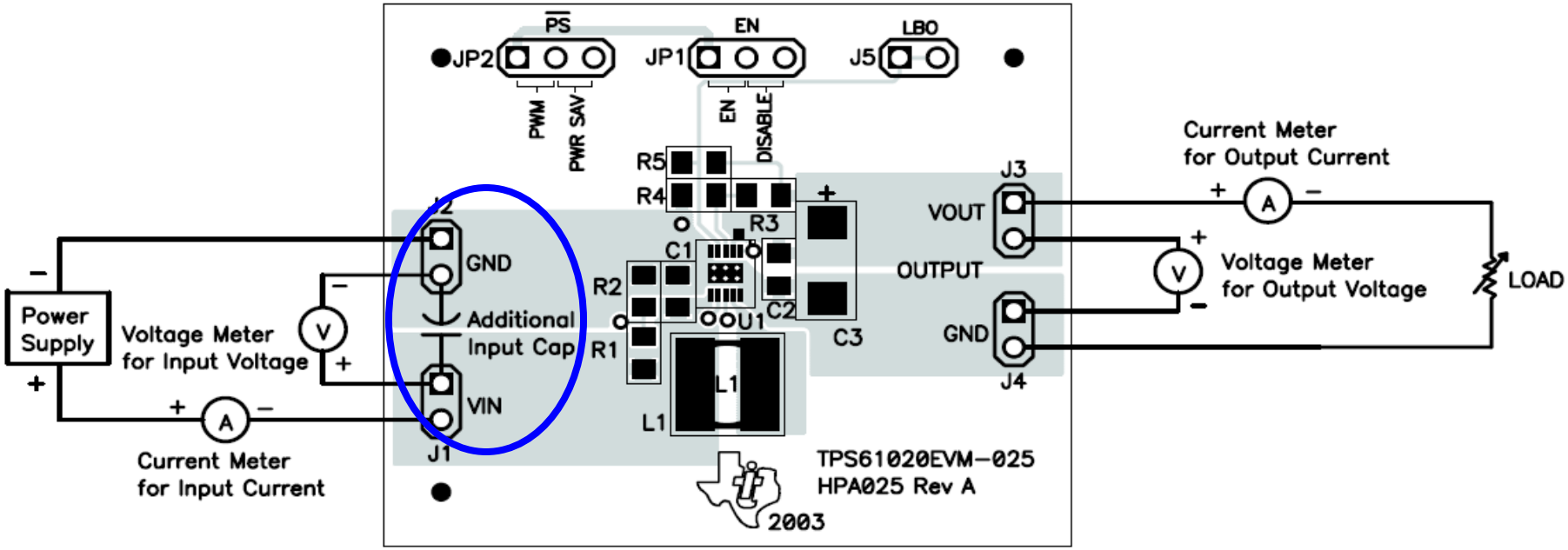
Without common mode choke



With common mode choke

Efficiency measurements – the right approach





- **Use additional input bulk capacitor (>200µF) direct on the board to smooth input current**

Efficiency measurements – results

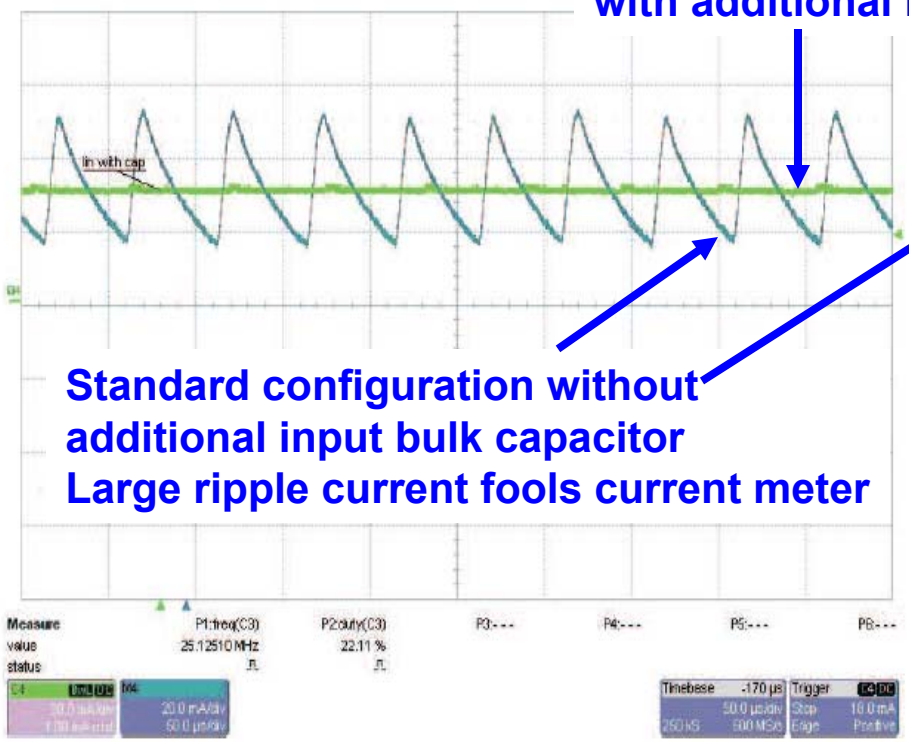


Figure 7. Input Current Waveform

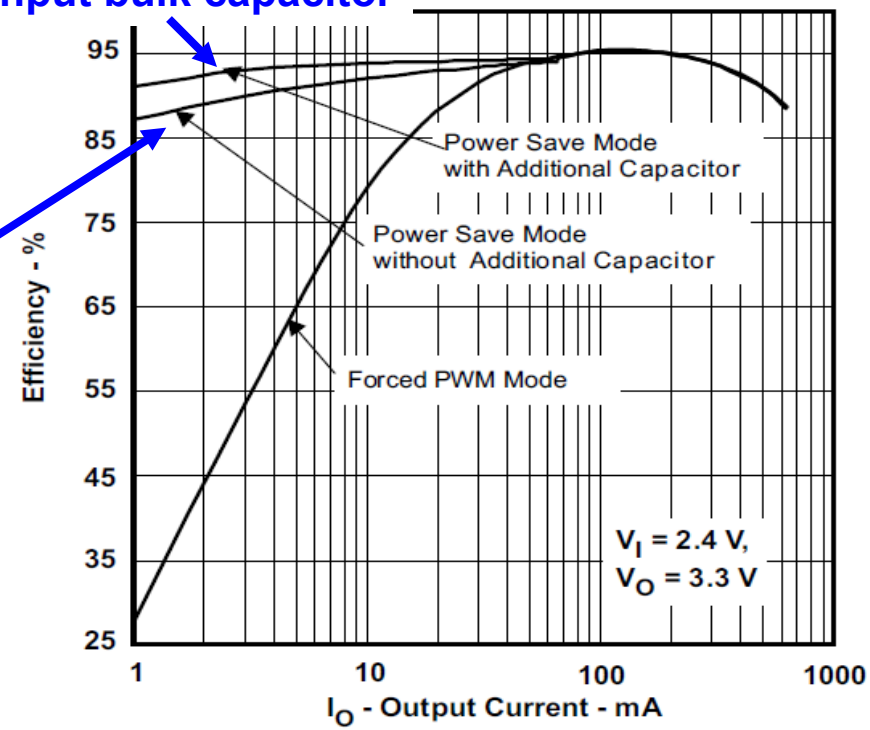


Figure 8. Efficiency Comparison

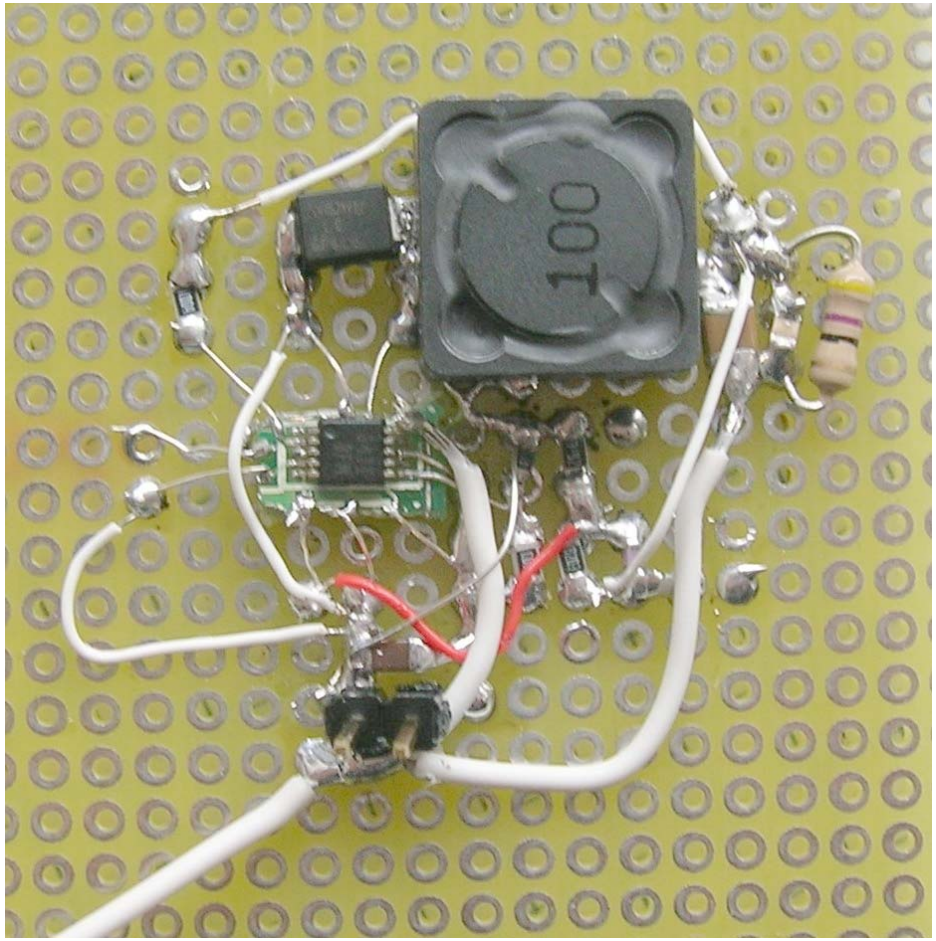
- **Adding additional input bulk capacitor (>200µF) on EVM's input is always a good idea.**
- **Many EVMs are not designed to work off a lab power supply connected via lab cables!**
- **See App Note: "Performing Accurate PFM Mode Efficiency Measurements" (slva236)**

Agenda

- Characteristic of passive and active components
- Special circuits
- Thermal Design
- Improved measurement techniques
- **Layout**

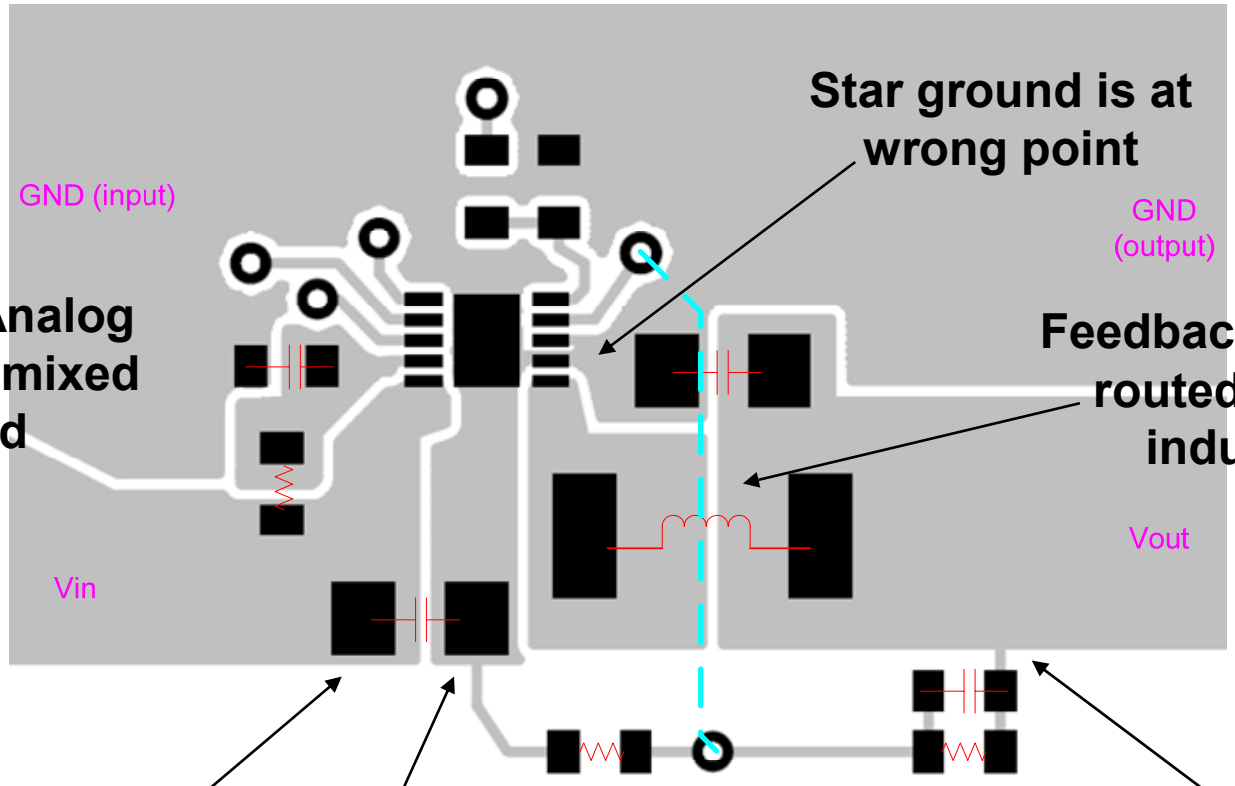
Prototype “layout”

How NOT to Prototype a Power Supply!



Consider Proper Layout Even for Prototypes!

Additional bad layout – Switcher doesn't work at all



Star ground is at wrong point

Power and Analog grounds are mixed on board

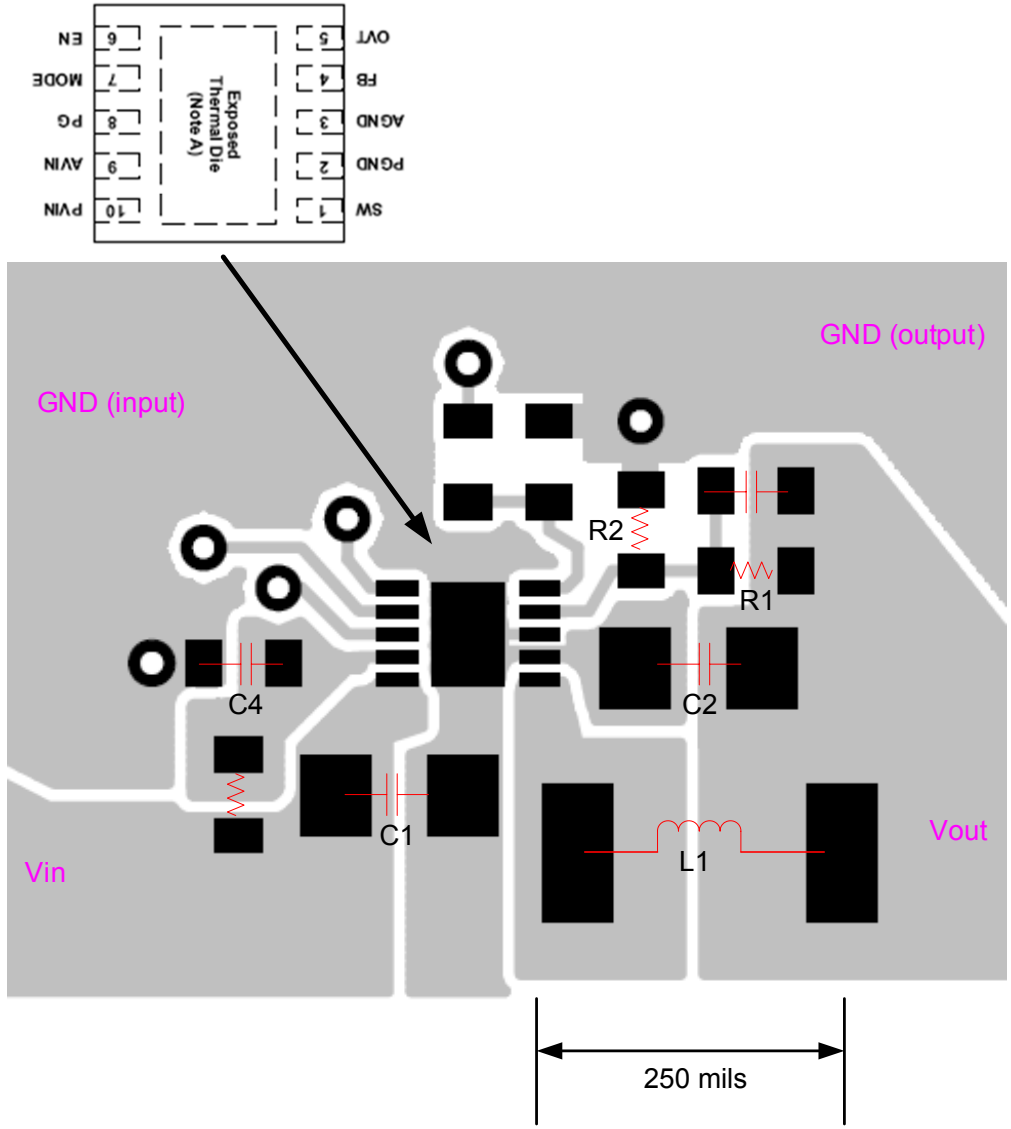
Feedback trace is routed under inductor

Poor input cap. placement

Feedback network grounded to noisy power ground

Feedback sampled at wrong point

Good layout example



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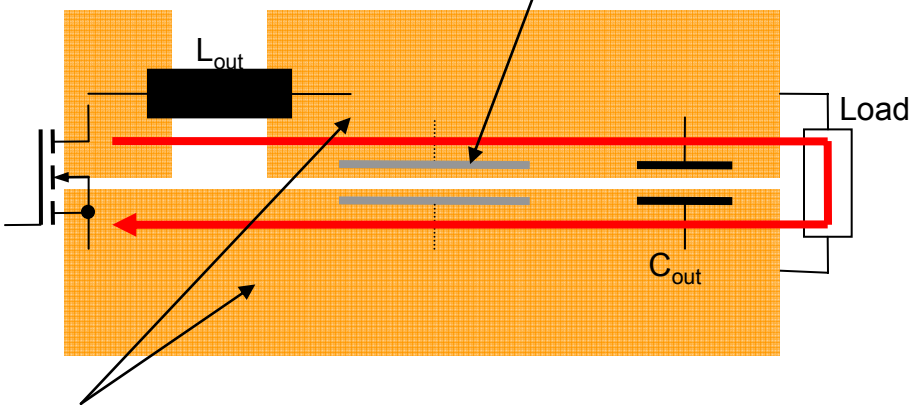
Use parasitic capacitance on Vout

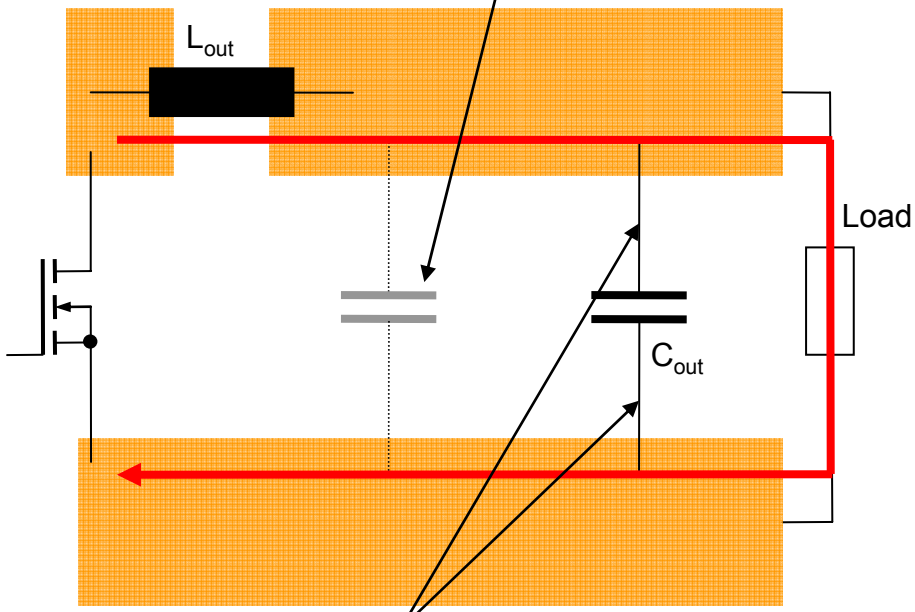
big parasitic capacitance between the traces



parallel traces with narrow gap between traces increase the output capacitance and minimize the loop inductance and therefore the magnetic interference

Do !

small parasitic capacitance between the traces

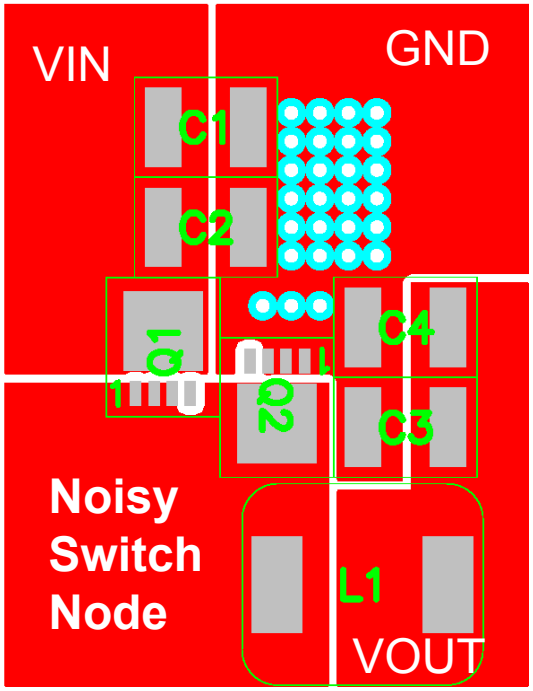


the resistance of long leads to the component will be added to ESR and ESL

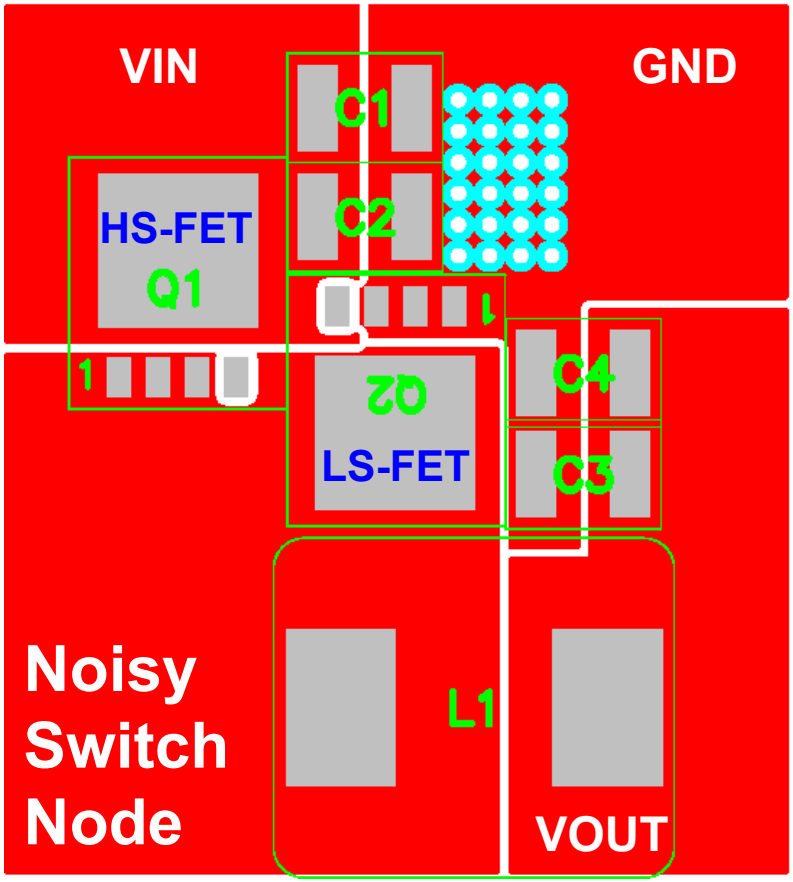
Do not !

Texas Instruments

Optimized Layout for NexFETs

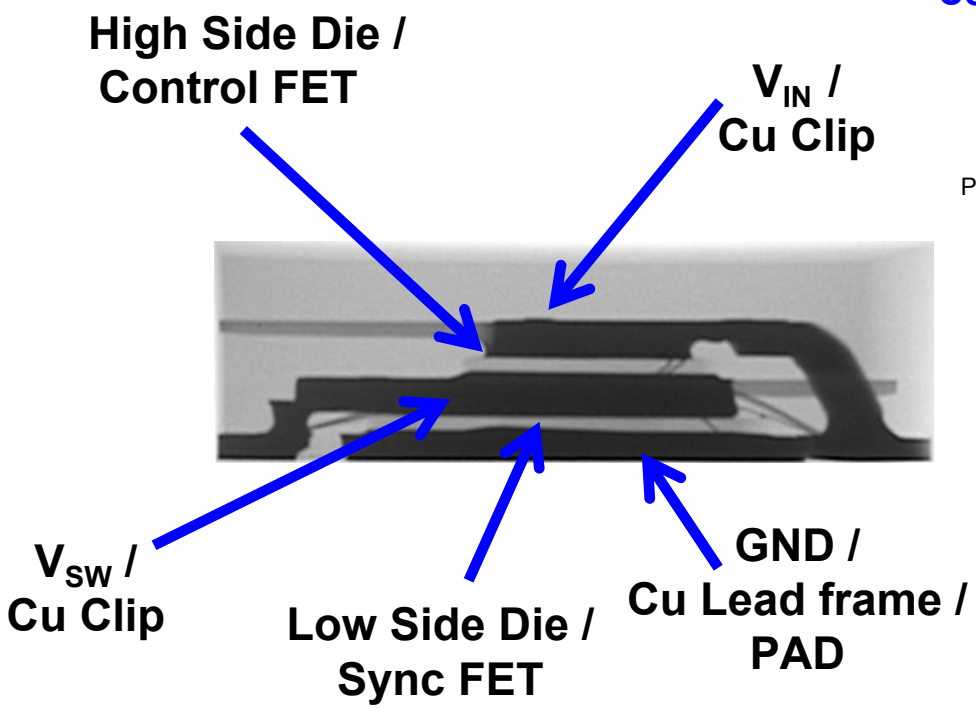


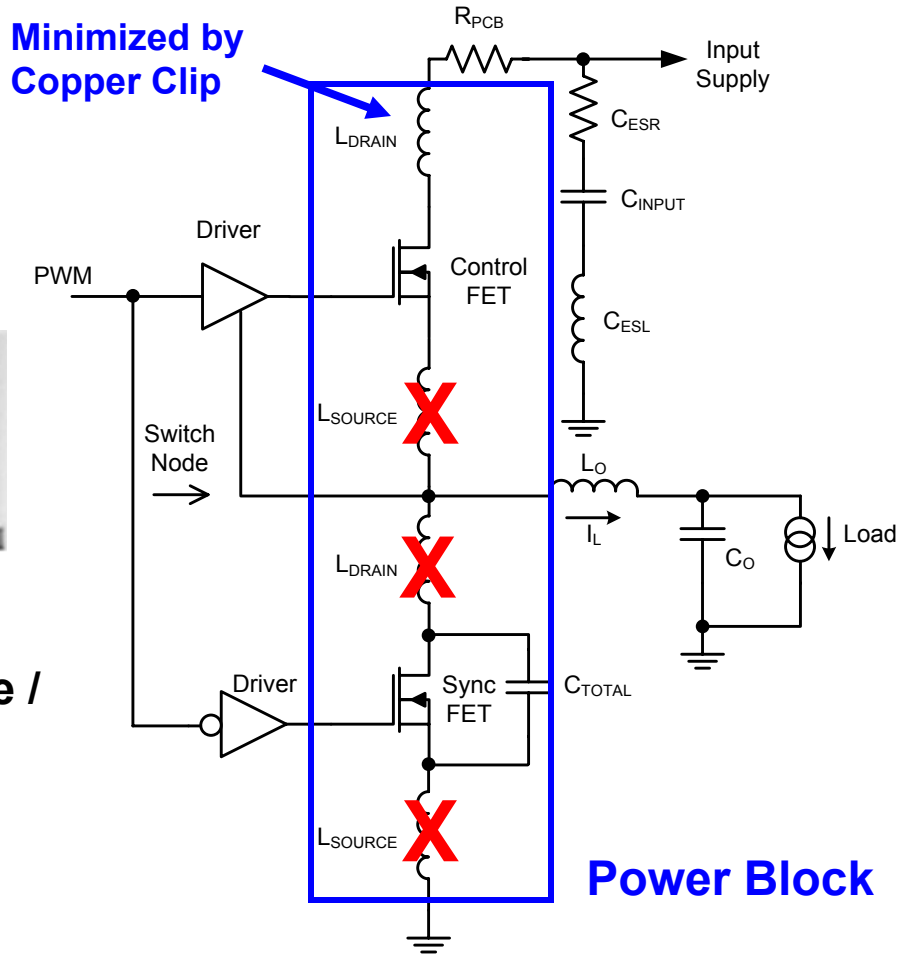
3 x 3 SON Layout



5 x 6 SON Layout

Power Block – Next generation NexFETTM



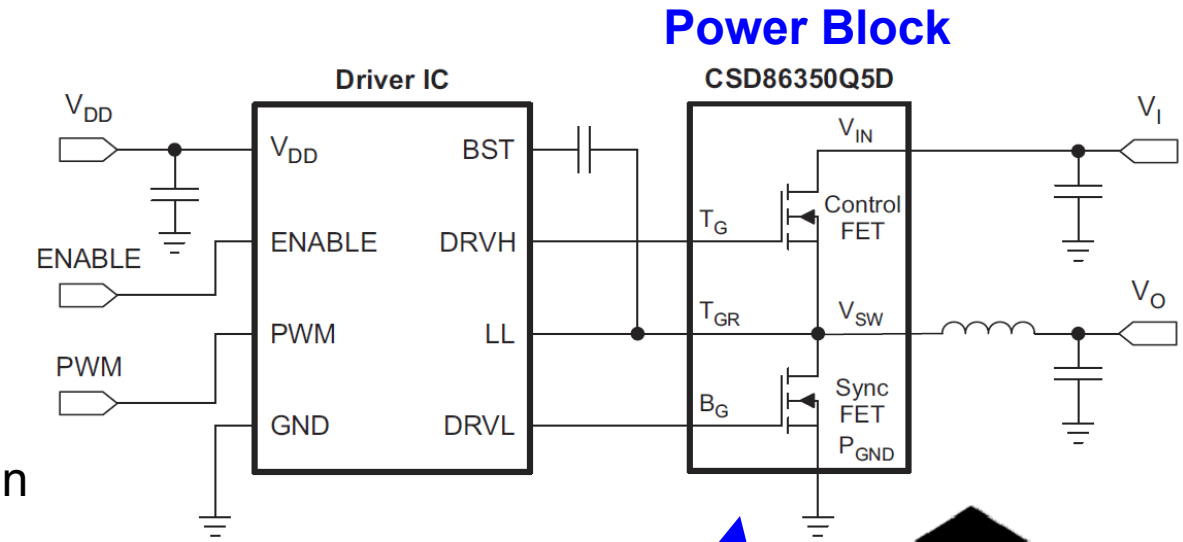


A significant step in reducing package parasitics.

Power Block solves the cooling / EMI challenge

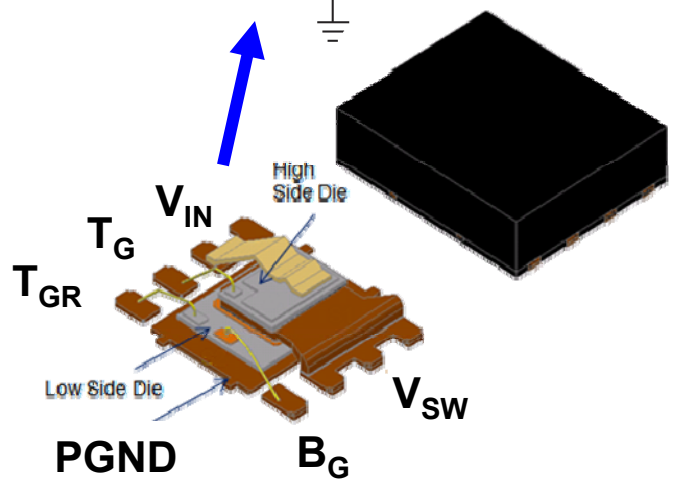
Solution with Power Block

- **Cooling PAD is noise free**, SOURCE of the Sync FET
- Noisy Switch Node not used for cooling,
  Switch Node copper area can be minimized.

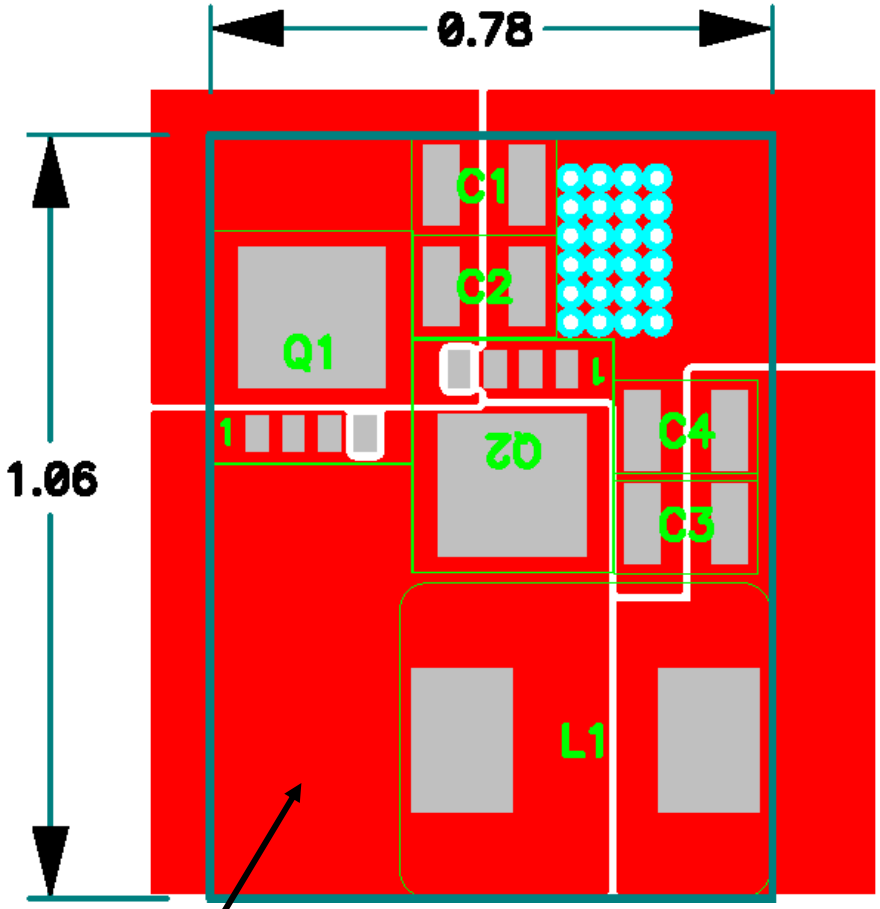


Solution with 2 separate FETs or dual FETs

- DRAINs of both FETs needs cooling.
  DRAIN of Sync FET is noisy switch node, needing maximized copper area on board for cooling !!!



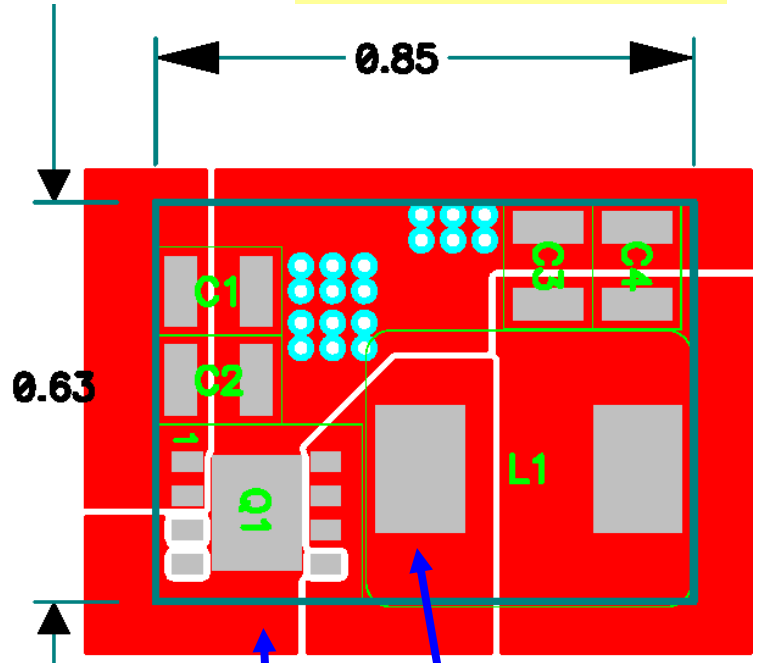
CSD86350 Power Block saves space / eases EMI



0.83 Sq In

20A Power Stage
5 x 6 SON FETs

20A Power Stage
Power Block FET



0.53 Sq In
35% Reduction!

Area for switch node reduced (lower EMI)

Power Block uses GROUND for cooling !

Summary

- Characteristic of passive and active components
- Special circuits
- Thermal Design
- Improved measurement techniques
- Layout

Thanks