TI Technology Days 2010

High Speed Dataconverter Basics

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Agenda

- Introduction
- High Speed ADCs
  - HS ADC parameters
  - Driving HS ADCs
  - Powering HS ADCs
  - Testing HS ADCs
- High Speed DACs

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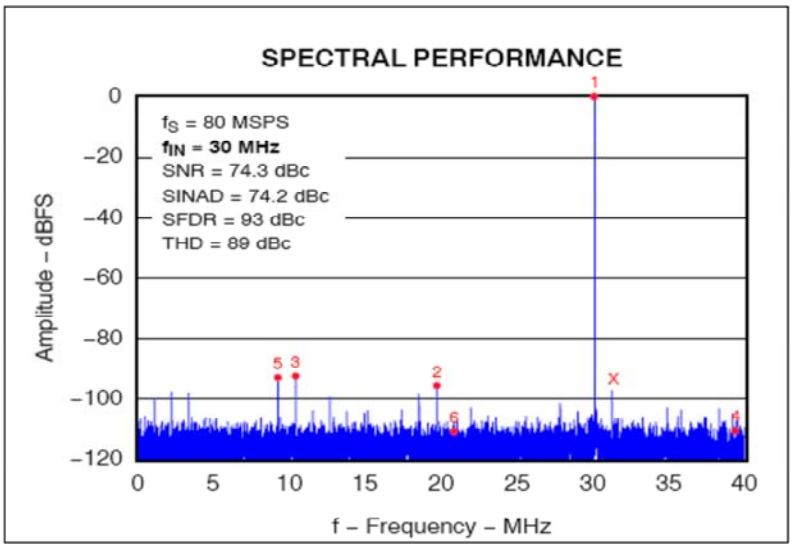
HS ADC parameters

HS ADC parameters



What is:

-SNR?

-SINAD?

-SFDR?

-THD?

-ENOB?

-dBc?

-dBFS?

Typical plots in a HS ADC datasheet

HS ADC parameters

- **SNR (Signal-to-Noise Ratio)**
  Ratio between the power measured in a single tone and the rms sum of the noise (minus harmonics)

- **THD (Total Harmonic Distortion)**
  Ratio between the power measured in a single tone and the sum of the power in harmonics.

- **SFDR (Spurious Free Dynamic Range)**
  Ratio between the power measured in a single tone and the highest spur.

- **SINAD (Signal-to-Noise Ratio and Distortion)**
  Is the ratio of the rms signal amplitude to the mean value of the root-sum-squares of all other spectral components including harmonics, but excluding DC.
  SINAD = THD + SNR.

- **ENOB (Effective Number of Bits)**
  is an overall measure of how perfect the ADC is. SINAD tells us how perfect the ADC is, so ENOB is calculated from SINAD
  ENOB = (SINAD – 1.76)/6.02

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dBc – dBFS – dBm

- dBc – measurement made *relative* to the carrier power
- dBFS – measurement made *relative* to the converter's Full Scale
  - The converter's full scale is 0dBFS, but it is VERY common for recommended full scale to be -1dBFS
  - This is due to the fact that you usually want to allow a little bit of conversion headroom in case there is noise or a slight DC shift in the analog signal…otherwise…you clip.
- dBm is an *absolute* number and is the power of a signal -> PdBm=10*log(PW/1mW)
- Know the difference between dBm, dBc and dBFS!

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THD and THD+N

THD is the ratio between the power measured in a single tone and the sum of the power in harmonics (usually at least the 1st five harmonics, sometimes more)

$$THD = 20\log_{10}\left(\frac{\sqrt{\left(A^2_{HD_2[rms]} + A^2_{HD_3[rms]} + \ldots + A^2_{HD_n[rms]}\right)}}{A_{fin[rms]}}\right)$$

Total harmonic distortion plus noise **(THD + N)** is the ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics plus all noise components (excluding dc). The bandwidth over which the noise is measured must be specified. In the case of an FFT, the bandwidth is dc to fs/2. (If the bandwidth of the measurement is dc to fs/2, THD + N is equal to SINAD)

$$THD + N = 20\log_{10}\left(\frac{\sqrt{\left(A^2_{HD_2[rms]} + A^2_{HD_3[rms]} + \ldots + A^2_{HD_n[rms]} + Noise^2_{[rms]}\right)}}{A_{fin[rms]}}\right)$$

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THD of an ADC is also generally specified with the input signal close to full-scale, although it can be specified at any level.

Harmonic distortion is generally specified with an input signal near full-scale (generally 0.5 to 1 dB below full-scale to prevent clipping), but it can be specified at any level.

For signals much lower than full-scale, other distortion products due to the differential nonlinearity (DNL) of the converter—not direct harmonics—may limit performance.

Signal-to-Noise and Distortion Ratio (SINAD) and ENOB

SINAD is the ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, including harmonics, but excluding DC.

It can be calculated directly by the summation of THD and SNR because that is what it is.

ENOB is an overall measure of how perfect the ADC is, and SINAD tells us how perfect the ADC is, so ENOB is calculated from SINAD

$$\mathrm{ENOB} = \frac{(\mathrm{SINAD} - 1.76)}{6.02}$$

SINAD is a good indication of the overall dynamic performance of an ADC as a function of input frequency because it includes all components which make up noise (including thermal noise) and distortion. It is often plotted for various input amplitudes.

SINAD is equal to THD + N if the bandwidth for the noise measurement is the same.

ENOB generally depends on the **amplitude** and the **frequency** of the applied sinusoidal input tone, and both must be specified for this particular test. This method compares the rms noise produced by the ADC under test to the rms quantization noise of an ideal ADC with the same resolution in bits. If an actual 10-bit ADC with a sine-wave input of a given frequency and amplitude has an ENOB = 9.0 bits, then it produces the same rms noise level for that input as would an ideal 9-bit ADC.

The error of an ideal ADC consists solely of noise. For actual converters, however, the measured error includes quantization noise along with aberrations such as missing output codes, AC/DC nonlinearity, and aperture uncertainty (jitter). Noise on the reference and power-supply lines also degrades the ENOB.

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Signal-to-Noise Ratio (SNR)

$$SNR_{dB} = 20\log_{10}\left(\frac{\text{value of } F_S \text{ input } [rms]}{\text{value of quantizati on noise } [rms]}\right)$$

$$F_S = v(t) = \left[\frac{q2^N}{2}\right]\sin(2\pi mf) \rightarrow F_{S[RMS]} = \frac{q2^N}{2\sqrt{2}};$$

$$Q_{[RMS]} = \frac{q}{\sqrt{12}}$$

$$\Rightarrow SNR_{dB} = 20\log_{10}\left(\frac{\frac{q2^N}{2\sqrt{2}}}{\frac{q}{\sqrt{12}}}\right) = 20\log_{10}\left(\frac{2^{N-1} * \sqrt{3} * 2}{\sqrt{2}}\right) =$$

$$= 20\log_{10}\left(2^N * \frac{\sqrt{3}}{\sqrt{2}}\right) = 20\left(\log 2^N + \log\frac{\sqrt{3}}{\sqrt{2}}\right) = 20 * N * \log 2 + 20 * \log\frac{\sqrt{3}}{\sqrt{2}} \Rightarrow$$

$$\boxed{\Rightarrow SNR = 6.02N + 1{,}76dB}$$

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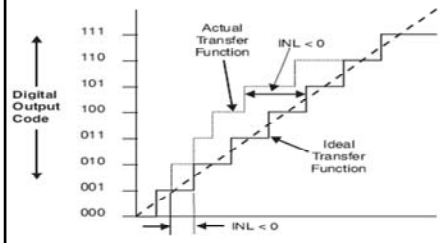
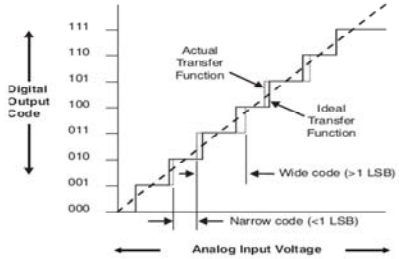
SNR is the signal-to-noise ratio with the distortion components removed (the first six harmonics and dc). SNR reveals where the noise floor of the converter is. There can be a steep decrease in SNR as a function of input frequency, which means the converter was not designed for frequencies near this point.

Integral Nonlinearity INL
Differential Nonlinearity (DNL):





An **INL** error is the maximum deviation of a transition point from the corresponding point of the ideal transfer curve, with the measured offset and gain errors zeroed.

DNL error less or more than +/- 1LSB can cause missing codes.

$$\mathrm{INL}(n) = \sum_{i=0}^{n} \mathrm{DNL}(i)$$

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DNL is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB. Therefore if the step width or height is exactly 1 LSB, then the differential nonlinearity error is zero. If the DNL exceeds 1 LSB, there is a possibility that the converter can become nonmonotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC there is also a possibility that there can be missing codes i.e., one or more of the possible 2^n binary codes are never output.

INL is defined as the integral of the DNL errors, so good INL guarantees good DNL. The INL error tells how far away from the ideal transfer-function value the measured converter result is. The straight line can be either a best straight line which is drawn so as to minimize these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified.

A system with INL error has a non-linear output. The output Y3[n] is not equal to the sum of output Y1[n] +Y2[n] when its input is X3[n] = X1[n] + X2[n]. As a result, the non-linearity error produces additional, unwanted, internally generated sinusoids (intermodulation distortion).

Assuming that we need 0.1% or 10 bits of accuracy (1/(2^10)). Having that in mind a 12 Bit converter gives us enough margin for the design. A 12 bit device with 0.5 LSBs of INL can give 0.0122% -> (0.5/2^12) error or 13 bits (1/2^13) of accuracy, when we remove the gain and offset errors. To calculate best-case accuracy, divide the maximum INL error by 2^N, where N is the number of bits.

Neither INL nor DNL errors can be calibrated or corrected easily.

INL & DNL Diagrams (ADS5474)

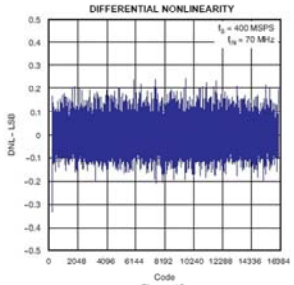


Figure 15.

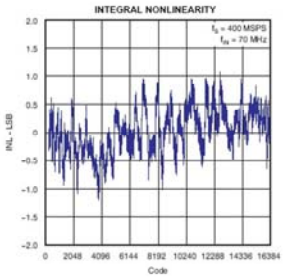


Figure 16.

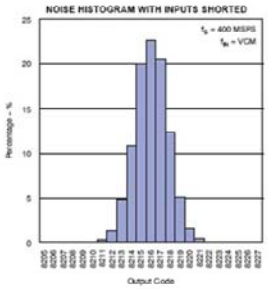


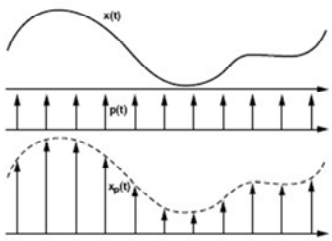
Figure 17.

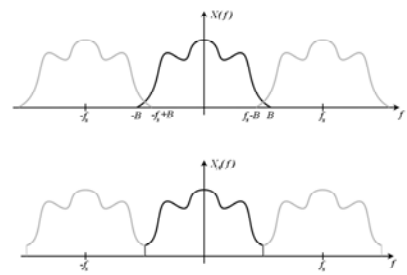
DNL Plot INL Plot Noise Histogram

Only a number about the INL or DNL of a converter without additional information (location, frequency, etc.) is not for a great help.
Although the DNL of the ADC will cause deviations from an ideal Gaussian distribution it should be at least approximately Gaussian. If the code distribution is significantly non-Gaussian, this could be an indication either a poorly designed ADC or bad PC board layout.

Sampling The Signal

Sampling Analog Signals





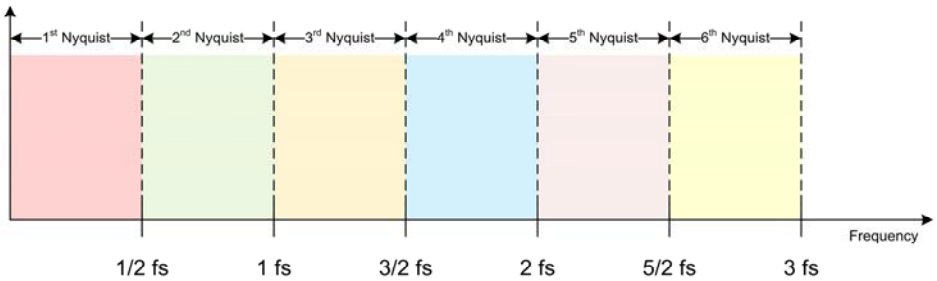
$$x_P(t) = x(t)\cdot p(t) \quad \text{With} \quad p(t) = \sum_{n=-\infty}^{+\infty} \delta(t - nT)$$

In The Frequency Domain:

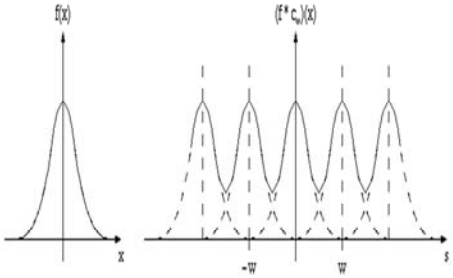
$$\left\{\begin{array}{l} X_p(f) = \dfrac{1}{2\cdot\pi}\left[X(f)\times P(f)\right] \\ P(f) = \dfrac{2\cdot\pi}{T}\displaystyle\sum_{k=-\infty}^{+\infty}\delta(f - kf_s) \end{array}\right\} \Rightarrow X_p(f) = \frac{1}{T}\sum_{k=-\infty}^{+\infty} X(f - kf_s) \rightarrow \text{Multiple Images with sample } f_s$$

Nyquist - Zones

- When talking about High Speed Dataconverter, often the term 'NYQUIST ZONE' is used
- One Nyquist zone has a bandwidth of half the data converters sampling frequency
  - 1st Nyquist zone: DC – 1/2 Fs
  - 2nd Nyquist zone: 1/2 Fs – 1 Fs
  - 3rd Nyquist zone: 1 Fs – 3/2 Fs
  - 4th Nyquist zone: 3/2 Fs – 2 Fs
  - And so on…

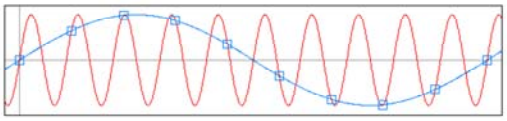


Aliasing

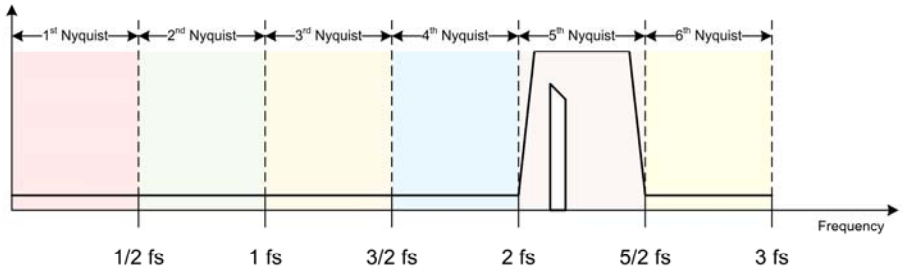


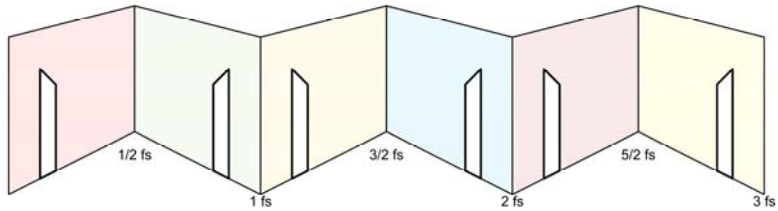
The original spectrum of f and the copies introduced by the sampling process overlap,

The spokes of a wheel may appear to turn backwards if the frame rate of the video input isn't fast enough to capture the motion of the wheel.



Undersampling

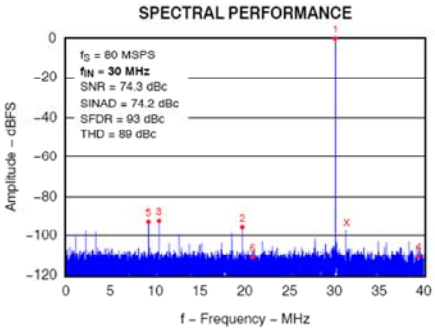




HS ADC parameters

ADS5423 80MSPS 14bit ADC

- **ENOB = (74.2 – 1.76)/6.02=12.03bits**
- **Why do we have only a FFT plot to 40MHz**
- **Harmonics are multiples of the fundamental. Why is e.g. the 2nd harmonic less than the fundamental?**



Can all ADCs Under-sample?

- Pipeline ADCs are usually designed to have Input Bandwidth that exceeds the intended operating range or 'Performance Bandwidth'
- The ADS5463, with a 2GHz Input Bandwidth, could sample input frequencies up to 2GHz (carrier, not BW) at 500MSPS – but the performance is frequency dependent
- There are ADCs that cannot under-sample, which are sometimes called Nyquist Converters, and are usually high precision and a little slower

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12-Bit, 500-MSPS Analog-to-

FEATURES

- 500-MSPS Sample Rate
- 12-Bit Resolution, 10.5 Bits ENOB
- 2-GHz Input Bandwidth
- SFDR = 75 dBc at 450 MHz and 500 MSPS
- SNR = 64.6 dBFS at 450 MHz and 500 MSPS
- 2.2-Vpp Differential Input Voltage
- LVDS-Compatible Outputs
- Total Power Dissipation: 2.2 W
- Offset Binary Output Format
- Output Data Transitions on the Rising and Falling Edges of a Half-Rate Output Clock

DESCRIPTION

The ADS5463 is a 12-bit, 500-MSPS analog-to-digital converter
3.3-V supply, while providing LVDS-compatible digital outputs.
switching of the onboard track and hold (T&H) from dis
high-impedance input. An internal reference generator is also pr

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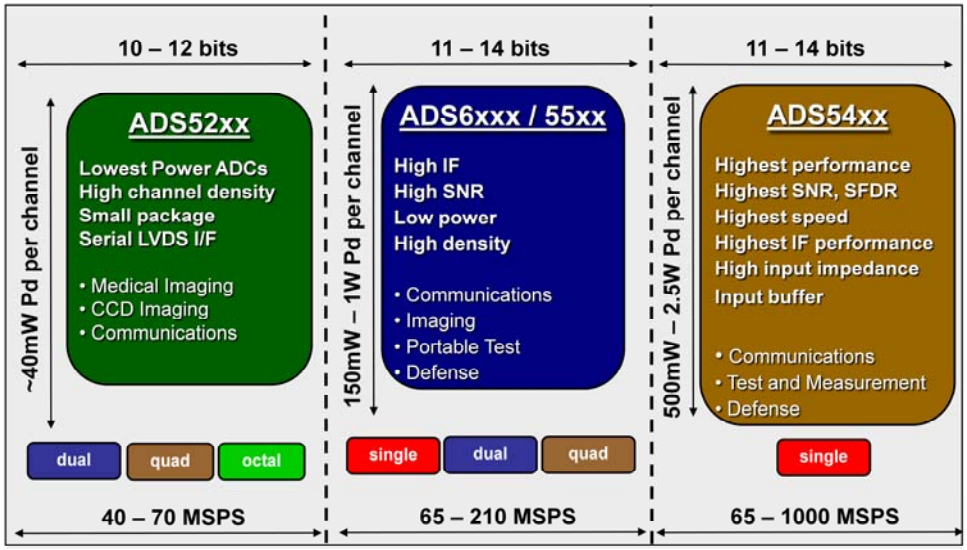
High Speed ADC Families



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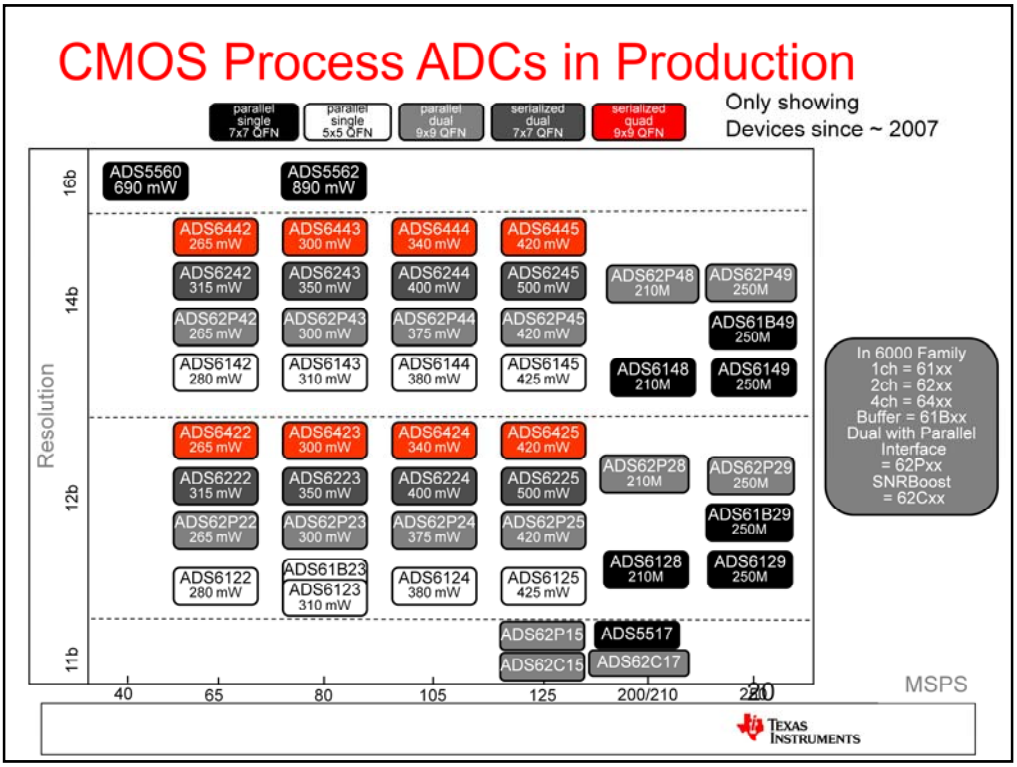
CMOS Process ADCs in Production
parallel single 7x7 QFN
parallel single 5x5 QFN
parallel dual 9x9 QFN
serialized dual 7x7 QFN
serialized quad 9x9 QFN
Only showing Devices since ~ 2007
Resolution
16b
14b
12b
11b
ADS5560 690 mW
ADS5562 890 mW
ADS6442 265 mW
ADS6443 300 mW
ADS6444 340 mW
ADS6445 420 mW
ADS6242 315 mW
ADS6243 350 mW
ADS6244 400 mW
ADS6245 500 mW
ADS62P48 210M
ADS62P49 250M
ADS62P42 265 mW
ADS62P43 300 mW
ADS62P44 375 mW
ADS62P45 420 mW
ADS61B49 250M
ADS6142 280 mW
ADS6143 310 mW
ADS6144 380 mW
ADS6145 425 mW
ADS6148 210M
ADS6149 250M
ADS6422 265 mW
ADS6423 300 mW
ADS6424 340 mW
ADS6425 420 mW
ADS6222 315 mW
ADS6223 350 mW
ADS6224 400 mW
ADS6225 500 mW
ADS62P28 210M
ADS62P29 250M
ADS62P22 265 mW
ADS62P23 300 mW
ADS62P24 375 mW
ADS62P25 420 mW
ADS61B29 250M
ADS6122 280 mW
ADS61B23
ADS6123 310 mW
ADS6124 380 mW
ADS6125 425 mW
ADS6128 210M
ADS6129 250M
ADS62P15
ADS5517
ADS62C15
ADS62C17
In 6000 Family
1ch = 61xx
2ch = 62xx
4ch = 64xx
Buffer = 61Bxx
Dual with Parallel Interface = 62Pxx
SNRBoost = 62Cxx
40
65
80
105
125
200/210
220
MSPS
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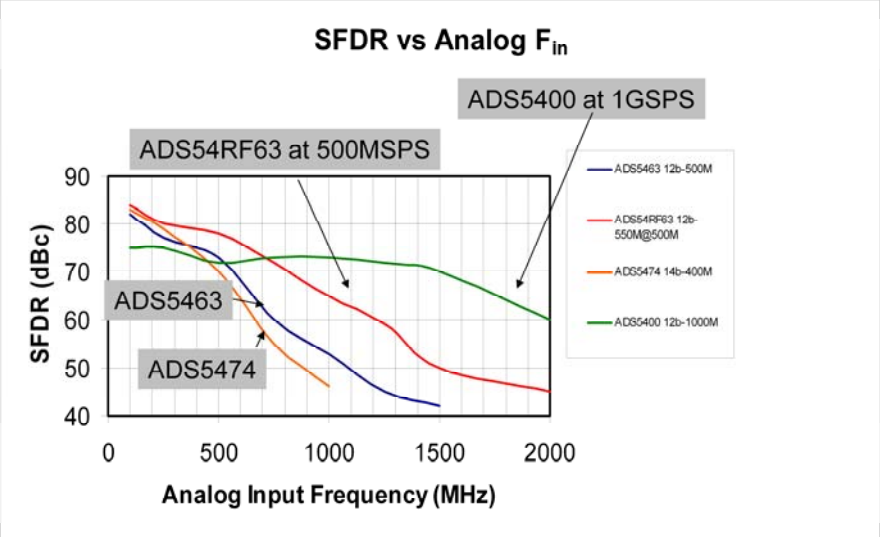
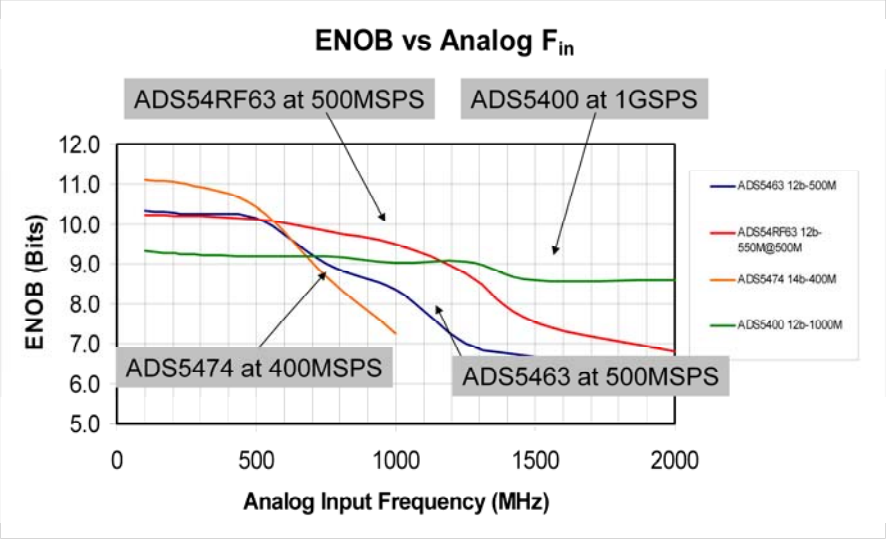
SFDR Comparison of HS TI ADCs



ENOB Comparison of HS TI ADCs



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Sampling Enhancements

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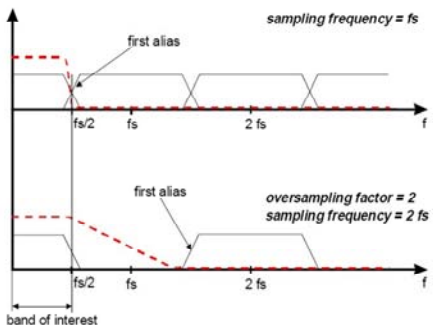
Oversampling

A signal sampled at a frequency higher than the Nyquist frequency is said to be oversampled k times



Oversampling factor k	SNR improvement in dB	extra resolution in number of bits
2	3	0,5
4	6	1,0
8	9	1,5
16	12	2,0
32	15	2,5
64	18	3,0
128	21	3,5
256	24	4,0
512	27	4,5
1024	30	5,0
2048	33	5,5
4096	36	6,0

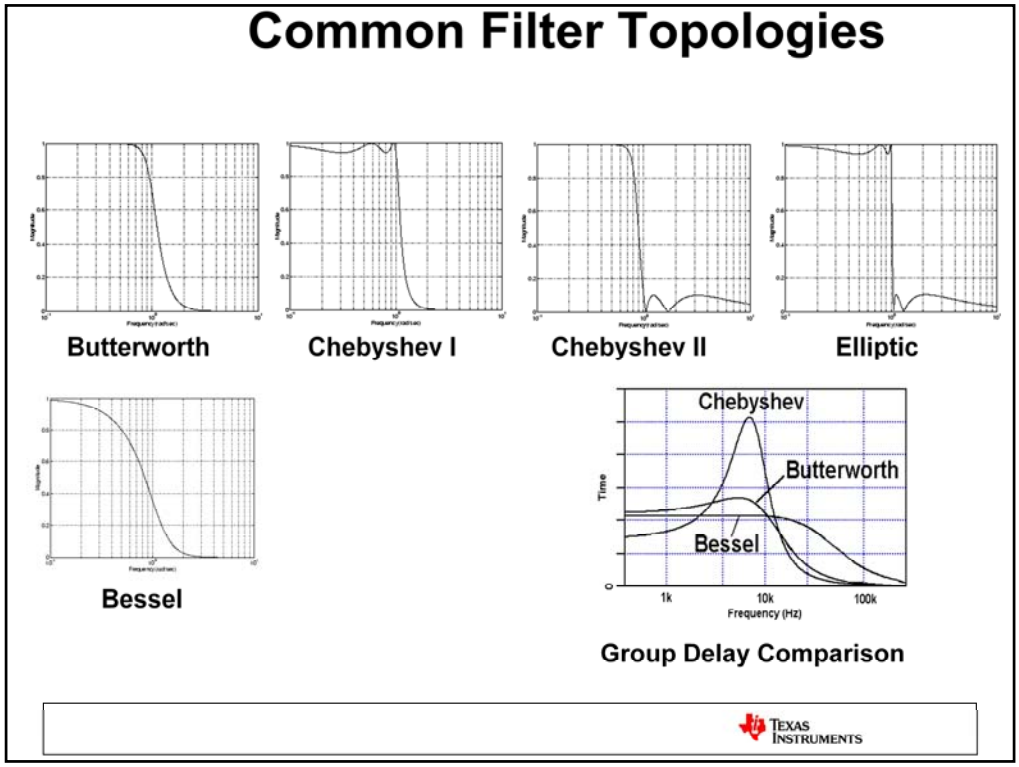
$$SNR_{\max}[dB] \approx 6.02N + 1.76 + 10\log_{10}(k)$$

There are three main reasons for performing oversampling:

a. It aids in anti-aliasing because realizable analog anti-aliasing filters are very difficult to implement with the sharp cutoff necessary to maximize use of the available bandwidth without exceeding the Nyquist limit. By increasing the bandwidth of the sampled signal, the anti-aliasing filter has less complexity and can be made less expensively by relaxing the requirements of the filter at the cost of a faster sampler. Once sampled, the signal can be digitally filtered and downsampled to the desired sampling frequency. In modern IC technology, digital filters are much easier to implement than comparable analog filters of high order.

b. Oversampling is implemented in order to achieve cheaper higher-resolution A/D and D/A conversion. For instance, to implement a 24-bit converter, it is sufficient to use a 20-bit converter that can run at 256 times the target sampling rate. Averaging a group of 256 consecutive 20-bit samples adds 4 bits to the resolution of the average, producing a single sample with 24-bit resolution. Note that this averaging is possible only if the signal contains perfect equally distributed noise (i.e. if the A/D is perfect and the signal's deviation from an A/D result step lies below the threshold , the conversion result will be as inaccurate as if it had been measured by the low-resolution core A/D and the oversampling benefits will not take effect).

c. Noise reduction/cancellation. If multiple samples are taken of the same quantity with a random noise signal, then averaging several samples reduces the noise by a factor of 1/sqrt(k).



Filtering is very important in order to avoid aliasing. The most common (analog) filter structures are the Butterworth, Chebyshev, Inverse Chebyshev, Cauer and Bessel-Thomson filters.

Butterworth Filter: A Butterworth (maximally flat) filter is the most commonly used general purpose filter. It has a monotonic passband with the attenuation increasing up to its 3-dB point which is known as the natural frequency. This frequency is the same regardless of the order of the filter. However, by increasing the order of the filter, the roll-off in the passband moves closer to its natural frequency and the roll-off in the transition region between the natural frequency and the stopband becomes sharper.

Chebyshev I Filter: The Chebyshev equal ripple filter distributes the roll-off across the whole passband. It introduces more ripple in the passband but provides a sharper roll-off in the transition region. This type of filter has poorer transient and step responses due to its higher Q values in the stages of the filter.

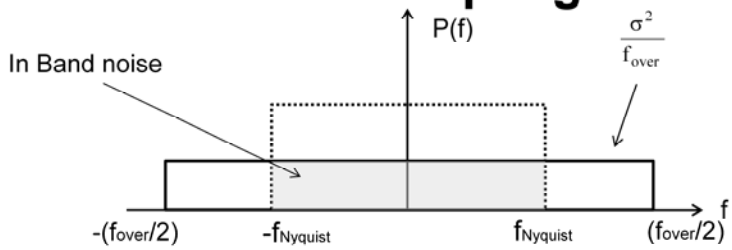
Chebyshev II Filter: Both the Butterworth and Chebyshev filters are monotonic in the transition region and stopband. Since ripple is allowed

in the stopband, it is possible to make the roll-off sharper. This is the principle of the Inverse Chebyshev, based on the reciprocal of the angular frequency in the Chebyshev filter response. This filter is monotonic in the passband and can be flatter than the Butterworth filter while providing a greater initial roll-off than the Chebyshev filter.

Cauer Filter: The Cauer or (Elliptic) filter is nonmonotonic in both the pass and stop bands, but provides the greatest roll-off in any of the standard filter configurations.

Bessel Filter All of the types mentioned above introduce nonlinearities into the phase relationship of the component frequencies of the input spectrum. This can be a problem in some applications when the signal is reconstructed. The Bessel or linear delay filter is designed to introduce no phase distortion but this is achieved at the expense of a poorer amplitude response. Due to the linear delay the filtered signals maintain their waveshapes.

Oversampling



$$\left.\begin{array}{l}\text{Quantisation Noise}: \sigma^2 = \dfrac{q^2}{12} \\ \text{Quantization Step}: q = \dfrac{A}{2^N}\end{array}\right\} \text{Quantisation Noise Power}: \sigma^2 = \frac{A^2}{12} \cdot 2^{-2N}$$

$$\text{Overs. Noise Power} = \int_{-\infty}^{\infty} P(f)\,df = 2 \cdot f_{Nyquist} \cdot \sigma^2 = 2 \cdot f_{Nyquist} \cdot \frac{A^2}{12} \cdot 2^{-2M} =$$

$$= \frac{A^2}{12} \cdot 2^{-2N} = 2 \cdot \frac{f_{Nyquist}}{f_{over}} \cdot \frac{A^2}{12} \cdot 2^{-2M} \Leftrightarrow$$

$$\Leftrightarrow N = M + \frac{1}{2} \cdot \log_2\left(\frac{f_{over}}{2 \cdot f_{Nyquist}}\right) \text{ With } f_{over} = 2 \cdot f_{Nyquist} \cdot 2^{2(N-M)}$$

Source: Digital Signal Processing (Li TAn)

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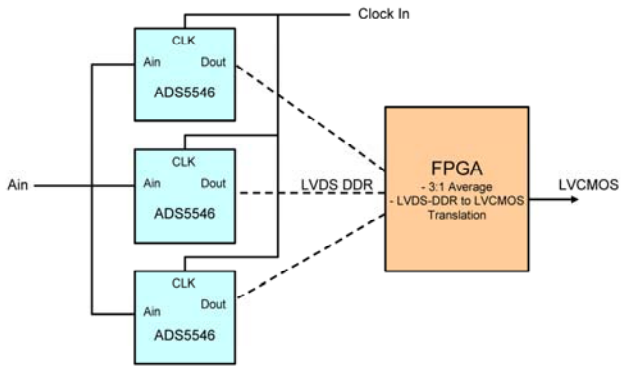
Averaging

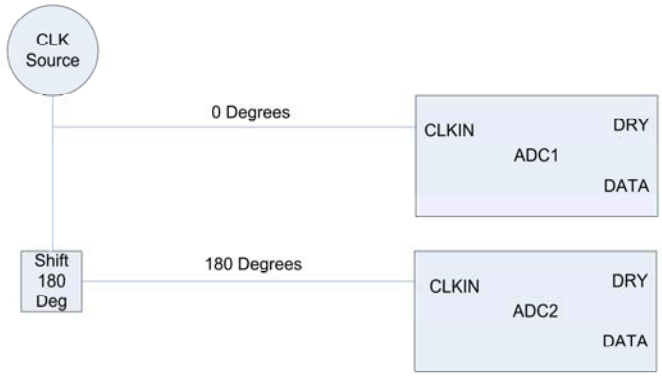
- **Same input signal to multiple ADCs**
- **All ADCs use the same clock**
- **Benefit: Digital outputs from each ADC can be digitally averaged together, increasing the SNR by ~10*log10(N), N=number ADCs**



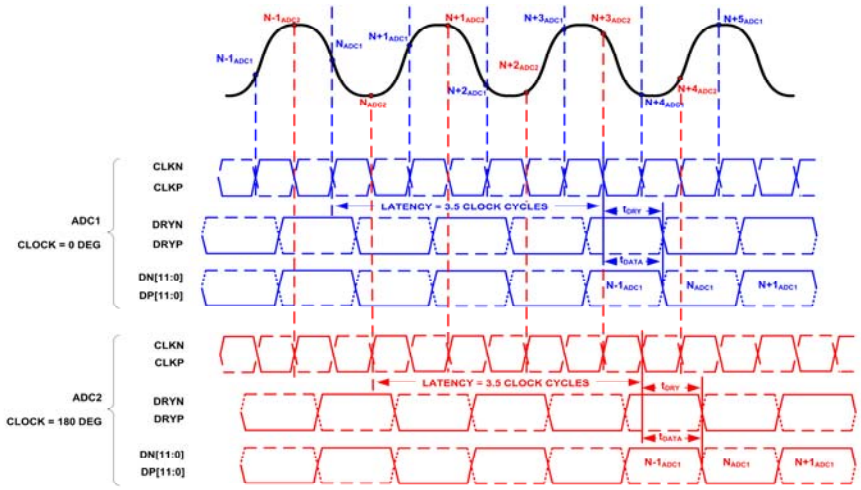
Interleaving

Interleaving ("ping-ponging")

- **Same input signal to multiple ADCs**
- **All ADCs use the same clock, however, the phase is shifted**
- **Benefit: overall sampling frequency is multiplied by the number of ADCs**



Inter-leaving ADCs - Timing Diagram



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Inter-leaving ADCs: Drawbacks

- A phase (clock) or gain mismatch between any of the ADCs will cause a spur at Fs/2 – Fin.
- An offset between the ADCs will cause a spur at Fs/2 if two are inter-leaved and Fs/4 if four are inter-leaved.
  - Not a big deal for 2 but in the middle of the band for 4 converters
- The differences in gain, phase, and offset will have to be calibrated to a sufficient level to reduce the spurs to an acceptable dBc.
- This causes system complexity and a re-calibration is likely required with temperature changes.
- Some ADCs provide the means to adjust some of these internally, but most do not.
- When not provided, the customer has to create methods external to the ADC to adjust for gain, phase, and offset.

**(Fs here is the final effective sample rate of the system)

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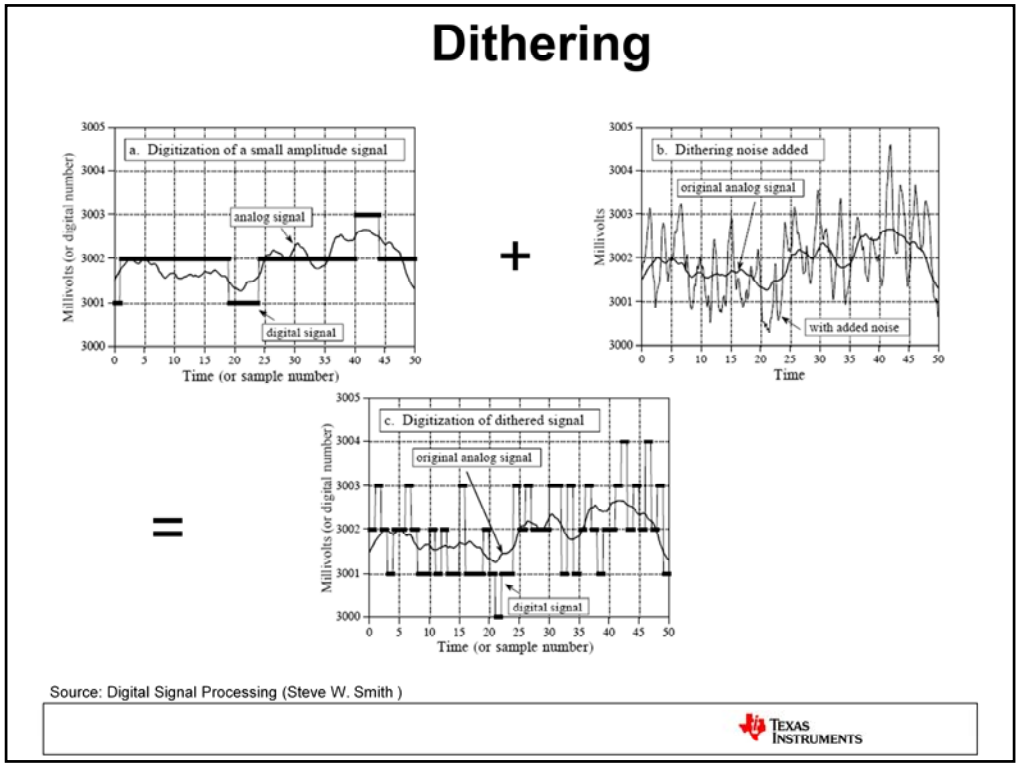

Dithering can be used to improve SFDR of an ADC under certain conditions.

A small amount of random noise is added to the analog signal. An ADC will have deterministic and systematic errors that repeat each time those codes are exercised. Dither (low level noise) can randomize those errors such that they are minimized. The harmonics are still present, but at lower levels. Dither can have the adverse affect of increasing the overall noise floor – acceptable for some applications. Some Dither techniques add the noise in areas of the circuit that need to be randomized and then attempt to subtract the noise later so that the degradation in SNR is minimized or not even noticeable by the user It is a technique used to improve the ADC's distortion beyond its inherent linearity.

The quantization error will not be a function of the input signal but of the instantaneous value of the dither noise. The dither decorrelates the quantization noise and the input signal. The fact that the value of the dither doesn't depend on the input signal and that the quantization noise becomes uncorrelated to the input eliminates the harmonics in the A/D spectrum, but at the cost of an overall increase in the noise floor.

A method is to inject a dither signal with a small bandwidth compared to the bandwidth of the input signal in the range near dc. Most of the times in the high speed applications no signal components are located in this area. An other possible location is slightly below fs/2.

When do you use Oversampling, Averaging, Interleaving and Dithering?

- **Interleaving:** Increase of the Sampling Rate.
- **Averaging**: Increase the SNR of uncorrelated (Not Stationary) noise.
- **Oversampling:** Increase the SNR of uncorrelated (Not Stationary) noise. Relaxation of the filter parameters.
- **Dithering:** Correlation exists always between the quantization noise and the input signal. Dithering is very effective in reducing harmonic distortion for signal levels up to about 10 LSB.

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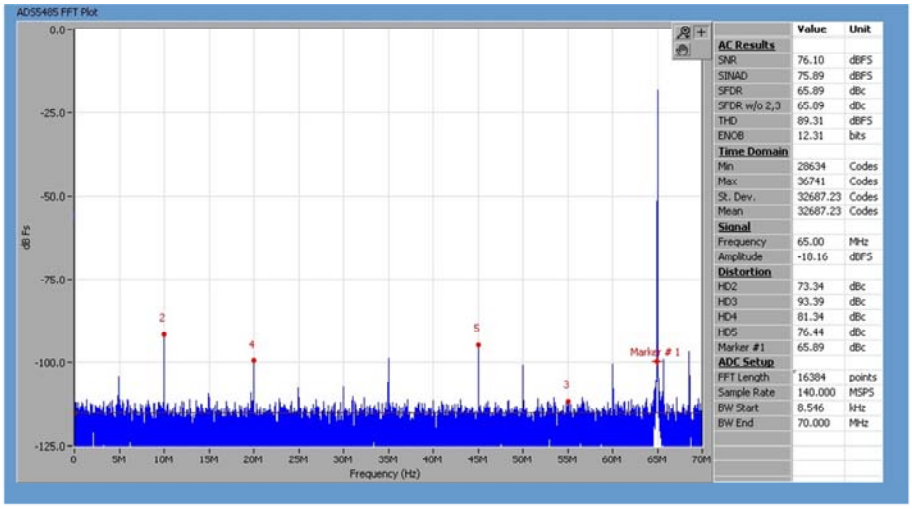

AD5548S FFT Plot
0.0
-25.0
-50.0
-75.0
-100.0
-125.0
dB Fs
0
5M
10M
15M
20M
25M
30M
35M
40M
45M
50M
55M
60M
65M
70M
Frequency (Hz)
2
4
5
3
Marker # 1
Value
Unit
AC Results
SNR 76.10 dBFS
SINAD 75.89 dBFS
SFDR 65.89 dBc
SFDR w/o 2,3 65.09 dBc
THD 89.31 dBFS
ENOB 12.31 bits
Time Domain
Min 28634 Codes
Max 36741 Codes
St. Dev. 32687.23 Codes
Mean 32687.23 Codes
Signal
Frequency 65.00 MHz
Amplitude -10.16 dBFS
Distortion
HD2 73.34 dBc
HD3 93.39 dBc
HD4 81.34 dBc
HD5 76.44 dBc
Marker #1 65.89 dBc
ADC Setup
FFT Length 16384 points
Sample Rate 140.000 MSPS
BW Start 8.546 kHz
BW End 70.000 MHz

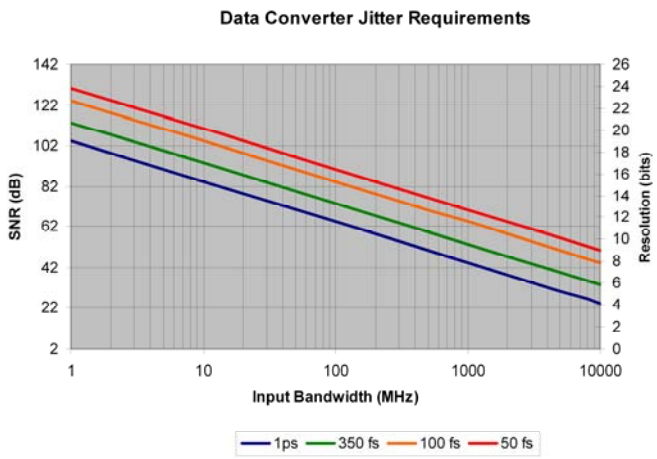
Clocking HS ADCs

Texas Instruments

Data Converter Clocking

$$SNR_{ADC} = 6.02N + 1.76$$

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{max}\tau_{RMS}}\right]$$



- This figure plots SNR vs. input frequency for fixed values of jitter.
- We can note a couple of things about this graph
  - Lower jitter = better SNR
  - For a constant jitter, SNR decreases as the frequency of the sampled signal increases

Signal to Noise Ratio

Assuming a sinusoidal input for V_{in} we have,

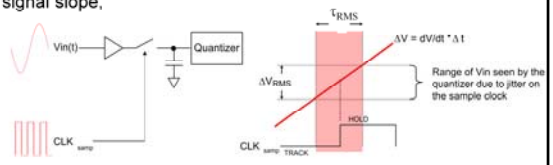
$$v(t) = V_o \sin 2\pi f t$$

Differentiating with respect to time yields the signal slope,

$$\frac{dv}{dt} = 2\pi f V_o \cos 2\pi f t$$

Taking the RMS value,

$$\frac{dv}{dt}_{rms} = \frac{2\pi f V_o}{\sqrt{2}} = \frac{\Delta V_{RMS}}{\tau_{RMS}}$$



Therefore, the RMS error voltage due to jitter is

$$\Delta V_{RMS} = \frac{2\pi f V_0 \tau_{RMS}}{\sqrt{2}}$$

Signal to noise ratio (SNR) is defined by,

$$SNR = 20\log_{10}\left[\frac{signal}{noise}\right] = 20\log_{10}\left[\frac{V_o/\sqrt{2}}{\Delta V_{rms}}\right]$$

Therefore, the SNR component due to jitter is:

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{\max}\tau_{RMS}}\right]$$

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The slide above shows the derivation of theoretical data converter SNR (Signal to Noise Ratio) due to jitter. It provides the following insight:

1. The frequency of the sample clock is not a factor.
2. The sample frequency of the data converter is not a direct factor, the input bandwidth of the data converter is (fmax).
3. The jitter value (tj) in Equation (6) represents total jitter which is the root sum squared of the sample clock jitter and the converter aperture jitter.

For many communications systems the bandwidth of the channel is fixed; however, the channel capacity needs to grow. Why?

1. Multimedia content requires more capacity
2. High definition content requires more capacity
3. Growing populations and an expanding subscriber base requires more capacity.

In fixed bandwidth applications, SNR is the only lever engineers have to control channel capacity? What types of applications have fixed bandwidths?

Calculation for clock jitter requirements

- **Solve for the RMS jitter required of the system in order to get at least 70dB SNR at 100MHz F_{in}**

$$SNR = -20 \cdot \log\left(2\pi \cdot f_{in} \cdot t_{j,total}\right)$$

$$t_{j,total} = \frac{10^{\frac{-SNR}{20}}}{2\pi \cdot f_{in}} \Rightarrow t_{j,total} = 503\,fs$$

- **…now solve for required Clock Jitter with 150fs of internal ADC aperture jitter**

$$t_{j,total}^2 = t_{j,ADC}^2 + t_{j,CLOCK}^2$$

$$t_{j,CLOCK} = \sqrt{t_{j,total}^2 - t_{j,ADC}^2} \Rightarrow t_{j,CLOCK} = 480\,fs$$

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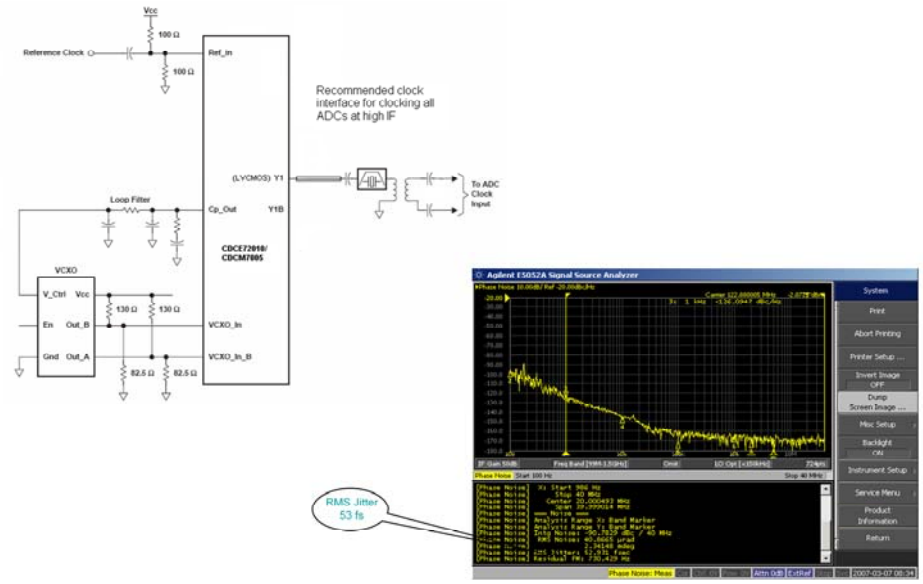
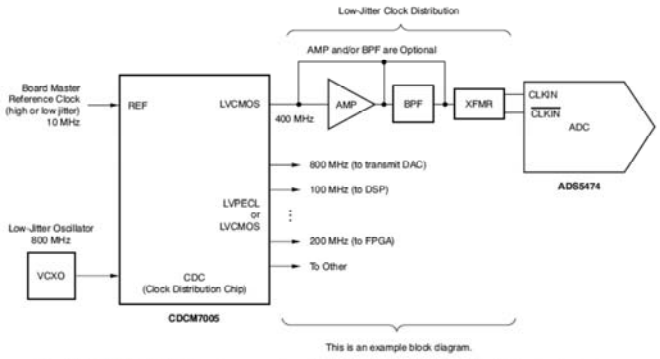
CDCE72010 + BPF Clocking an ADC



TEXAS INSTRUMENTS

How Do I Build the Low Jitter Clock Circuit?



Consult the CDCM7005 data sheet for proper schematic and specifications regarding allowable input and output frequency and amplitude ranges.

Figure 47. Optimum Jitter Clock Circuit

The jitter of this total clock solution at the clock input pins on the ADC will be determined primarily by

1) **The jitter of the VCO/VCXO chosen**
2) **The additive jitter in the CDC chip**
3) **The characteristics of the BPF**

The jitter of this total clock solution at the clock input pins on the ADC will be determined primarily by

1) The jitter of the VCO/VCXO chosen
2) The additive jitter in the CDC chip
3) The characteristics of the BPF

The BPF (bandpass filter) is sometimes required to reject the clock noise that is not near the clock frequency to improve the overall jitter.

The amp is optional if the insertion loss of the BPF (assuming it is required as well) causes the clock amplitude to be too low at the ADC clock pins.

CDCE72010 ADC/Macro BTS Clock
2:10 Ultra Low Jitter Cleaner w/ext. VC(X)O

Features

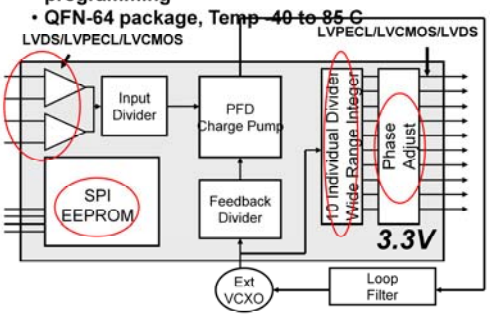
- Input frequencies up to 180MHz SE/500MHz Differential LDVS/LVPECL/LVCMOS
- Output frequencies up to 1.175GHz
- Output up to 10 LVPECL/10 LVDS/20 LVCMOS
- Optional High Swing LVPECL output
- Wide-range integer divide selectable by output
- Individual Phase Adjust
- Ultra low additive jitter (<35fs, RMS)
- Low Output Skew (~ 20ps, typ)
- Provides holdover functionality
- On-chip EEPROM

Applications

- Wireless BTS (Macro, Micro Cells)
- SONET
- Data Communications
- Test Equipment
- Jitter Cleaners

Benefits

- Wide input/output frequency range supports high and low end of frequency standards
- Selectable input/output standards reduces translation logic
- External loop filter provides maximum flexibility
- EEPROM saves default start-up settings
- SPI interface provides in-system programming
- QFN-64 package, Temp -40 to 85 C



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Driving HS ADCs

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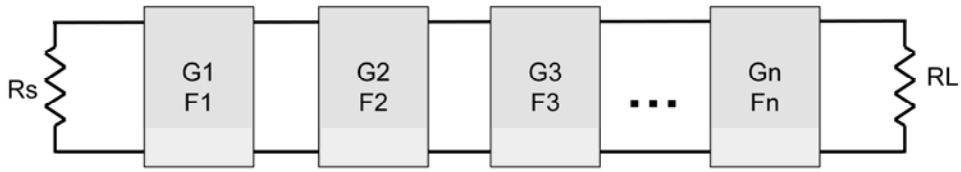
Friis Equation



$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1.G_2} + \frac{F_4 - 1}{G_1.G_2.G_3} + \ldots + \frac{F_n - 1}{G_1.G_2.G_3 \ldots G_{n-1}}$$

Where:

G_n : Gain

F : Noice Factor; $F = \frac{SNR_{in}}{SNR_{out}}$ or $F = 10^{\frac{NF}{10}}$

NF : Noice Figure; $NF = SNR_{in} - SNR_{out}$ in dB or $NF = 10\log(F)$

Source Wikipedia

As such NF represents the degradation in the SNR as the signal passes through the receiving system.

NF of the first stage dominates the total NF

High gain in the first stage reduces the contribution of the NF of the second stage

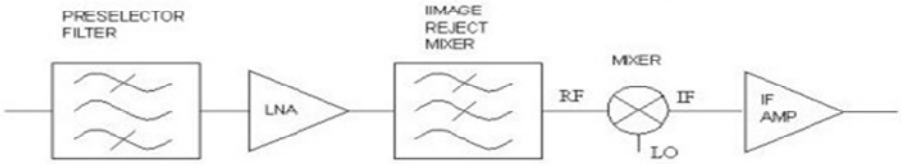
Most of the time the first 3 parts are the major noise contributors and we could neglect the rest.

Transformers vs OpAmps

- **Transformers**
  - Common Mode can be applied to the center tap to bias ADC inputs
  - Only AC coupling
  - Can provide voltage step-up or step down
  - Can provide Single-ended to differential conversion
  - Provides best AC performance, particularly at high-IF
  - They are passive devices, no noise added
- **OpAmps**
  - Opamps can provide the gain needed for driving the ADC at its full dynamic range
  - AC & DC coupling
  - The CM input of the opamp can be used to level shift the signal to the right level for the ADC
  - Opamps like the THS4509 can either be used as differential in to differential out, or as single-ended in to differential out amplifiers
  - Adds noise

Texas Instruments

Friis Equation Example



Gain (dB): -0.5	Gain (dB): 20	Gain (dB): -1	Gain (dB): -6	Gain (dB): 30
NF (dB):0.5	NF (dB):3	NF (dB):1	NF (dB):6	NF (dB):5
Gain (linear): 0.8912	Gain (linear): 100	Gain (linear):0.7943	Gain (linear):0.2511	Gain (linear):1000
F (linear):1.122	F (linear):1.9952	F (linear):1.2589	F (linear):3.981	F (linear):3.1622

$$F_{total} = 1.122 + \frac{1.995 - 1}{0.891} + \frac{1.259 - 1}{89.125} + \frac{3.981 - 1}{70.795} + \frac{3.162 - 1}{17.782} =$$

$$= 1.122 + 1.115 + 0.003 + 0.042 + 0.122 = 2.405$$

$$NF = 10\log(2.405) = 3.81dB$$

$$Linear\ data = 10^{\frac{dB}{10}}$$

The receiver chain has an input filter in front of the LNA to limit the amount of stray signals that might come in and saturate it. Following the LNA is a image rejection filter, to prevent image noise foldover. The mixer and IF amp round out the chain.

As you can see the relative noise contribution of the five stages shows that after the LNA, not much else is added to the noise factor. After the first two stages (F=1.122 and F=1.116), the noise factor at this point is 93% of the entire chain. Whenever your chain has a lot of gain up front, the denominator of subsequent stages in the Friis equation tends to wipe out the noise factor of the numerator.

SNR_{System} from SNR_{ADC} & SNR_{OPA}

$$SNR_{System} = -20 \cdot \log \sqrt{\left(10^{\frac{-SNR_{ADC}}{20}}\right)^2 + \left(10^{\frac{-SNR_{Op-Amp}}{20}}\right)^2}$$

- SNR_{System} is the sum of RMS powers represented by SNR_{ADC} and SNR_{OPA}
- As an example, for an ADC with 75dB SNR_{ADC}, the system SNR is reduced from that as shown here for different SNR's out of the filter.
- An $SNR_{Op\text{-}Amp}$ 5dB greater than SNR_{ADC} results in a SNR_{System} about 1dB less than the ADC by itself.
- At 15dB better than the converter (90dB), we see a 0.14dB degradation.

SNR_{OPA}	SNR_{System}
70 dB	68.8 dB
75 dB	72 dB
80 dB	73.8 dB
85 dB	74.6 dB
90 dB	74.86 dB
95dB	74.96 dB

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The SNR for the system is the RMS addition of SNR for the converter and the op-amp/filter combination. This implies that in order not to add too much noise in the amplifier stage, both filter and amplifier ought to have a very low noise. For example, with a 75dB SNR converter, in order to target a system SNR of 74.9dB, the SNR for the amplifier should be better than 85dB.

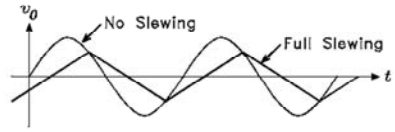
In amplifier terms, the SNR is the integrated output noise through a defined bandwidth. The bandwidth is limited by either:

•Post amplifier filter

•Amplifier small-signal bandwidth

Slew Rate: Sine Wave Input

- When an output sine wave is driven into full slewing, it becomes a **triangle wave**
- The **slew-limited peak** is given by the slope multiplied by ¼ the period
- When the op amp is driven into **full slewing**, an increase in the amplitude of the input signal causes no change in the output amplitude.
- **Slew Rate Limiting:** Distortion in the output signal caused by the slew rate of the device being too slow to allow the device to respond properly to a change in the input signal.
- **Slew Rate** is not related to small signal rise and fall times.



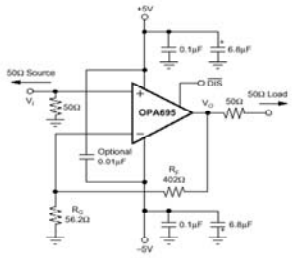
$$V_{Pslew} = SR \cdot \frac{T}{4} = \frac{SR}{4f}$$

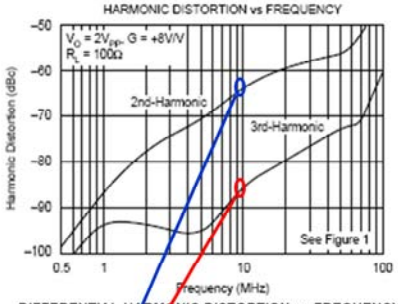
Maximum frequency with no slew rate limiting is given by:

$$f_{max} = \frac{SR\sqrt{2}}{2\pi V_P}$$

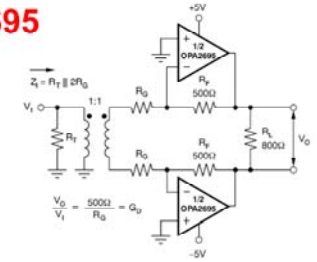
SE-Diff Performance Comparison: Dual Opamp w/Input transformer

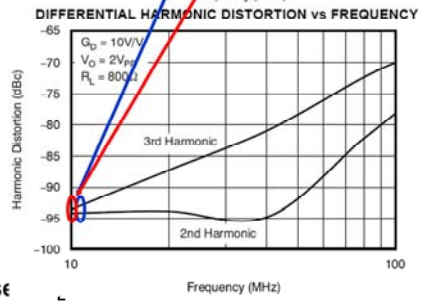
OPA695





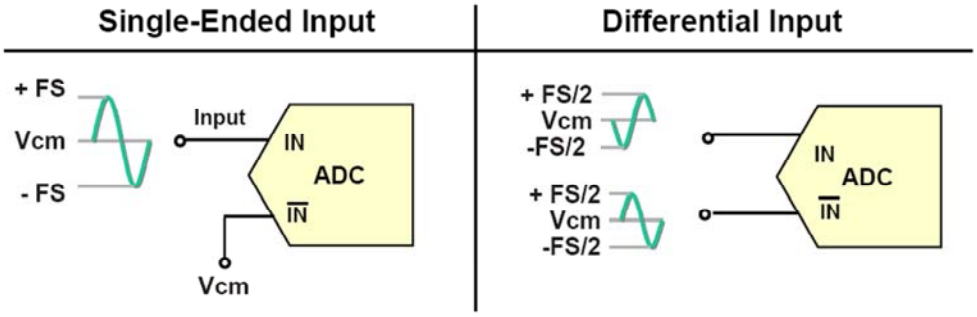
OPA2695





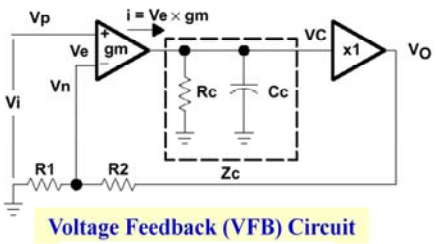
- **30dB improvement in HD2**
- **7dB improvement in HD3 due to increase**

Interfacing to the ADC



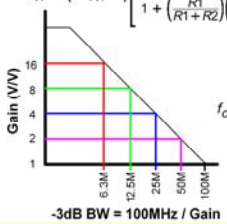
- Theoretically, differential signaling results in cancellation of even-order harmonics
- Reduced signal swing typically reduces the drivers distortion, thereby increasing system performance

VFB vs CFB Amplifiers



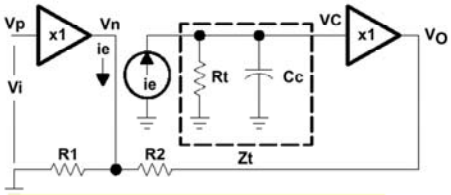
Voltage Feedback (VFB) Circuit

$$\frac{Vo}{Vi} \cong \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{R1}{R1 + R2}\right)\left(\frac{j2\pi fCc}{gm}\right)}\right]$$



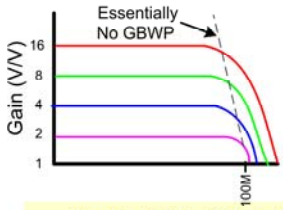
$$f_c = \left(\frac{gm}{2\pi Cc}\right)\left(\frac{R1}{R1 + R2}\right)$$

Bandwidth is Dictated by gm (fixed by design) and Gain – Hence Gain Bandwidth Product



Current Feedback (CFB) Circuit

$$\frac{Vo}{Vi} \cong \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + (j2\pi fR2Cc)}\right]$$



$$f_c = \frac{1}{2\pi R2Cc}$$

Bandwidth is Dictated by R2 (Feedback Resistor)

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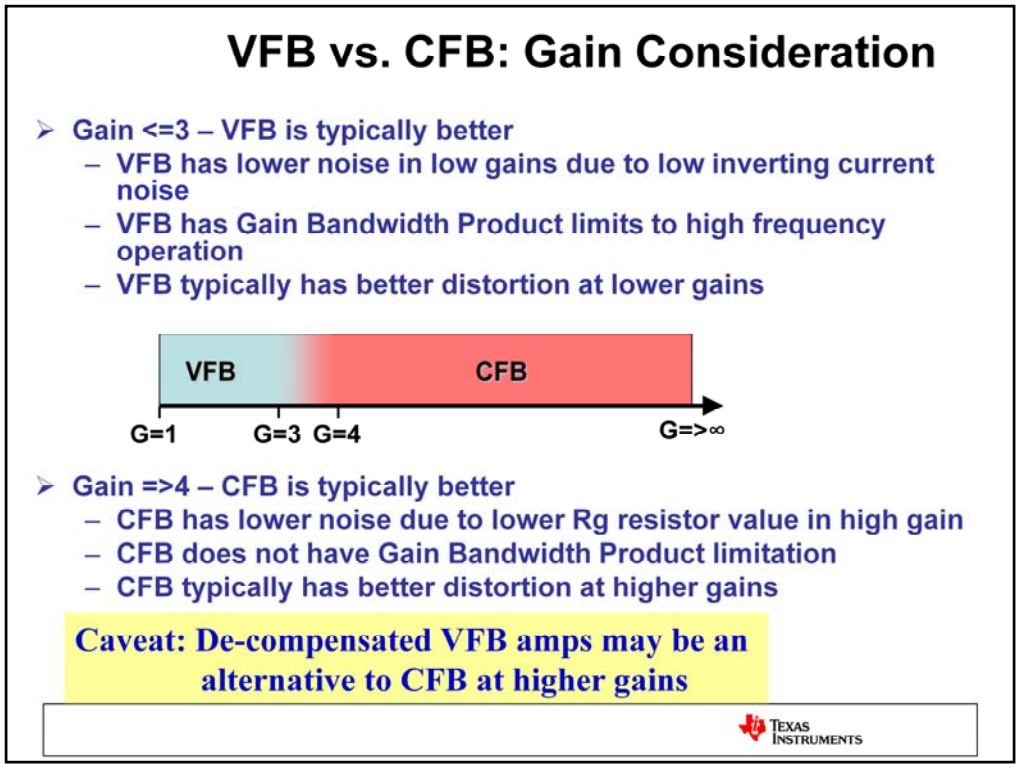


Although there are several attributes that separate a VFB amplifier from a CFB amplifier, there are typically only a few specifications that can be looked at when deciding on what topology is best for a given application. The first specification to look at is gain requirements of the amplifier. There are typically other specifications that go along with gain requirements. All of the key requirements dictate the best amplifier for the socket – not just one. Remember that there are always exceptions to these rules of thumb, but this does give a good starting point.

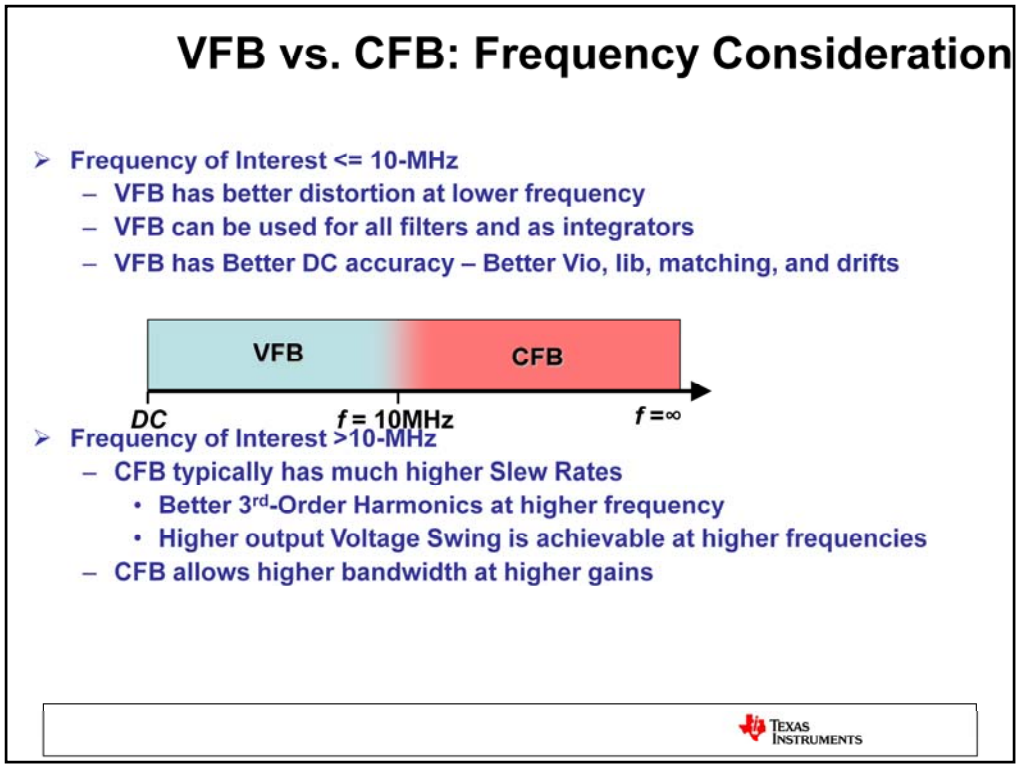
For gains equal to or less than 3, a VFB amplifier generally makes for a very good choice. One of the biggest reasons for this is the output noise of the amplifier. As other slides have shown, a VFB amplifier output noise is dominated by the voltage noise of the amplifier. Thus, the dominant VFB output noise is equal to voltage noise times the gain. Thus, as long as the gain is low, the overall noise will also be low.

A CFB amplifier output noise is generally dictated by the inverting current noise times the feedback resistance. Although this noise is not multiplied by the amplifier gain at the output, this contribution with low gain is generally the dominant noise component in the amplifier.

One other aspect of VFB amplifier working at low gains is their loop gain is very large. This will help keep distortion very low.

For amplifier gains greater than or equal to 4, the CFB amplifier is generally a better amplifier. The main reason for this is the feedback resistor is typically reduced as gain increases. This does two things. The first thing it does is to reduce the main noise contributor as the inverting current noise multiplied by the feedback resistor term is decreased. The other thing reducing the feedback resistor accomplishes is it decompensates the CFB amplifier. This results in a the lack of a gain bandwidth product the VFB amplifier has. Thus, high bandwidths are maintained at high gains with a CFB amplifier. Additionally, this decompensation helps maintain the distortion performance even at higher gains.

An alternative to using a CFB amplifier with high gains is to choose a decompensated VFB amplifier. The only limitation is these decompensated VFB amplifiers must maintain a minimum closed loop gain as dictated by their specifications. Failure to do so can easily result in oscillations. But, if the gain requirement is say 15V/V, and a VFB amplifier is desired, then choosing a decompensated VFB amplifier with a minimum gain of 10V/V or 12V/V – such as the THS4021 or OPA847 - would perform very well in the application.



The next specification to look at is the frequency of interest. This is not necessarily the bandwidth of the amplifier, but rather the frequency range of the signals that are of most importance. If the frequency of interest is 10-MHz or less, a VFB amplifier is typically a very good choice. Again there are exceptions to this rule of thumb, but it is a good starting point. VFB amplifiers work very well with these frequencies due mainly to the architecture of the amplifier. Additionally any type of filter can be constructed with a VFB amplifier including integrators. Couple this with good input offset voltage, matched input bias currents, and low drift, the VFB amplifier makes for an excellent choice for low frequency operation.

As the frequency of interest increases to over 10-MHz, the CFB amplifier generally makes an excellent choice. The ability to work at high gains and high frequencies is an obvious reason for this. But the other key attribute for the CFB amplifier is the exceptionally large slewrates. Third order harmonics are dominated by slewrate limitations. Thus, the higher the slewrate, the better the third order harmonics tend to be.

Coupled with slewrate is the output swing. Using the formula Vout(peak) = SlewRate / (2 Pi f) one can easily see that at high frequencies, to achieve reasonably large output swings requires significantly large slewrates. Thus, even if a VFB amplifier has a very large bandwidth, if it does not have a large slewrate, the output swing will be severely limited.

VFB vs. CFB – General Application Recommendations

	Low Gain	Low Gain/Low Noise	Low Gain/Low THD	High Gain	High Gain/Low Noise	High Gain/Low THD	DC Precision	Low Frequency	High Frequency	ADC driver	Integrator	Active Filter	Line Driver (e.g. DSL)	Buffer	Pulse Amplifier
VFB	x	x	x				x	x		x	x	x		x	
CFB				x	x	x			x	x		x	x		x

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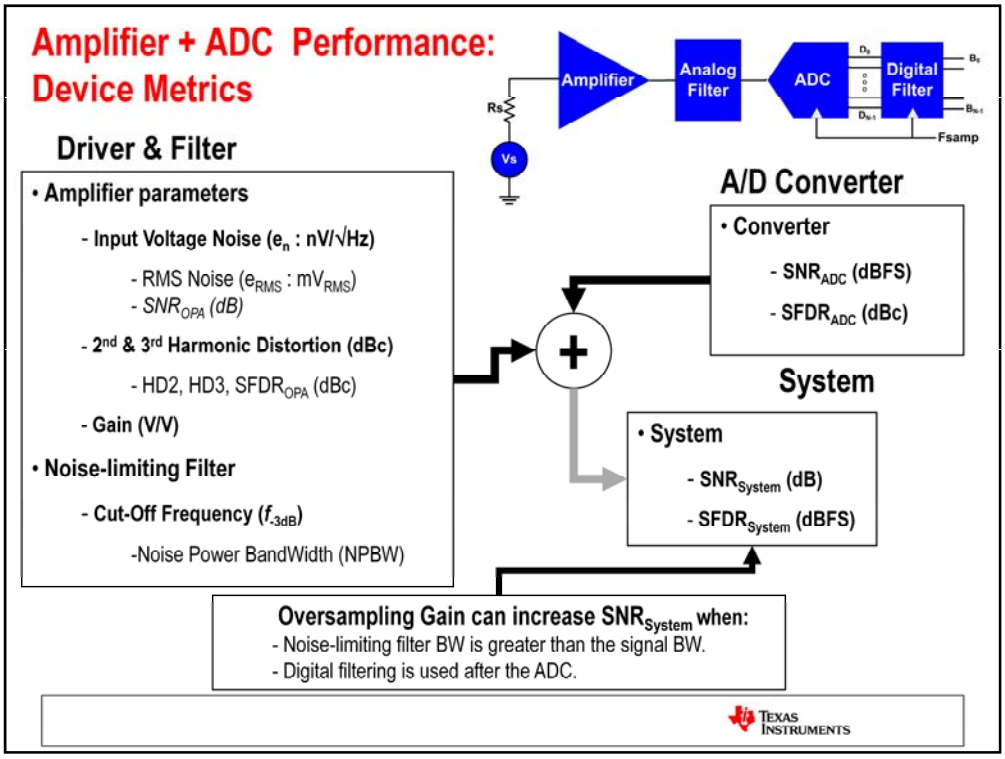
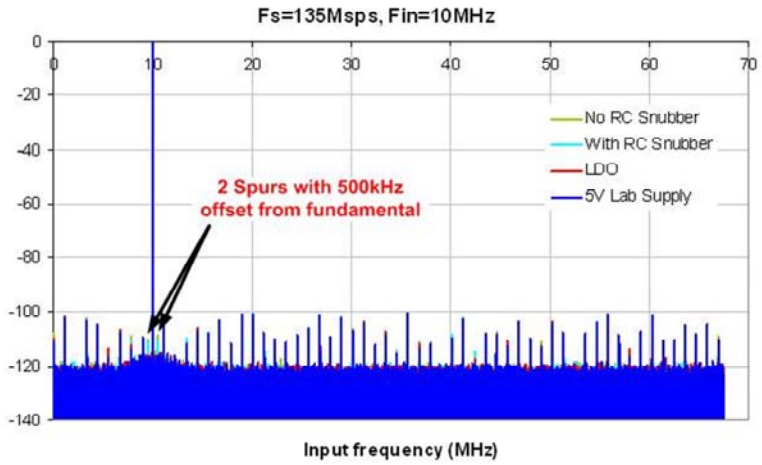


As shown above, amplifiers and converters are defined in different terms.
Amplifier noise is usually referred as spot noise in both current and voltage terms.

Combining the input voltage with the amplifier gain and the filter cut-off frequency, it is possible to derive a signal to noise ratio (SNR_{OPA}) for the amplifier.

In the same manner, using the 2nd and 3rd harmonic distortion, the dominant distortion terms for an amplifier, it is possible to derive an Spurious Free Dynamic Range ($SFDR_{OPA}$) for the amplifier.

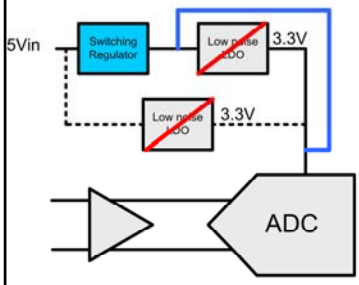
Given these SNR_{OPA} and $SFDR_{OPA}$ numbers, it is possible to combine them with those of the converter and see a predicted combined performance or system performance. This combination will be done at the converter input pins.


Fs=135Msps, Fin=10MHz
0
-20
-40
-60
-80
-100
-120
-140
0
10
20
30
40
50
60
70
No RC Snubber
With RC Snubber
LDO
5V Lab Supply
2 Spurs with 500kHz
offset from fundamental
Input frequency (MHz)

Powering HS ADCs

Texas Instruments

New Power Supply Option



Eliminating the LDO is a huge power saver, especially important for portable and handheld applications.

Customers so far however are skeptical on performance degradation…

Plan is supplemental application note to all new HS ADCs showing performance.

DRAFT Version – Preliminary Information

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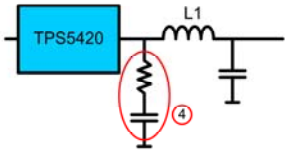
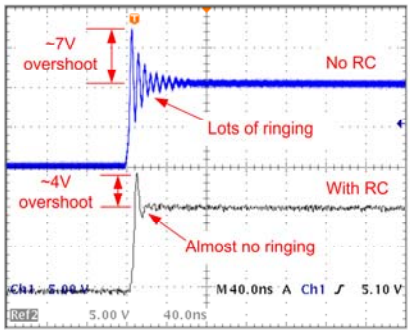
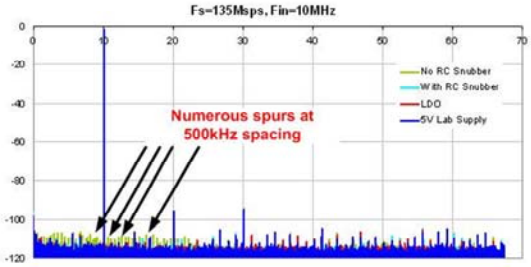
RC Snubber Circuit

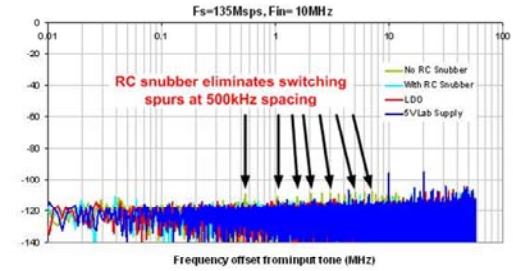


RC snubber reduces the switching spur by removing some of the reactive energy of the LC circuit



FFT Analysis





FFT plot shows a lot of little spurs with 500kHz spacing. However they are below the average spur level of the ADS6148 and don't impact the SFDR but they are going to impact the SNR

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ADS4149 (CMOS) - prelim results

Average of 25 tested EVMs	10MHz IF		170MHz IF	
	SNR (dBFS)	SFDR (dBc)	SNR (dBFS)	SFDR (dBc)
3.3V => LDO => 1.8V	72.76	87.15	71.16	82.7
3.3V => SPS => 1.8V	72.71	87.56	70.92	82.1

=> Hardly any noticeable performance degradation!

	Current from 3.3V Supply	Power Efficiency
LDO	162mA	56.1%
DC/DC	98mA	92.9%

=> LDO Solution requires ~60% more power!!

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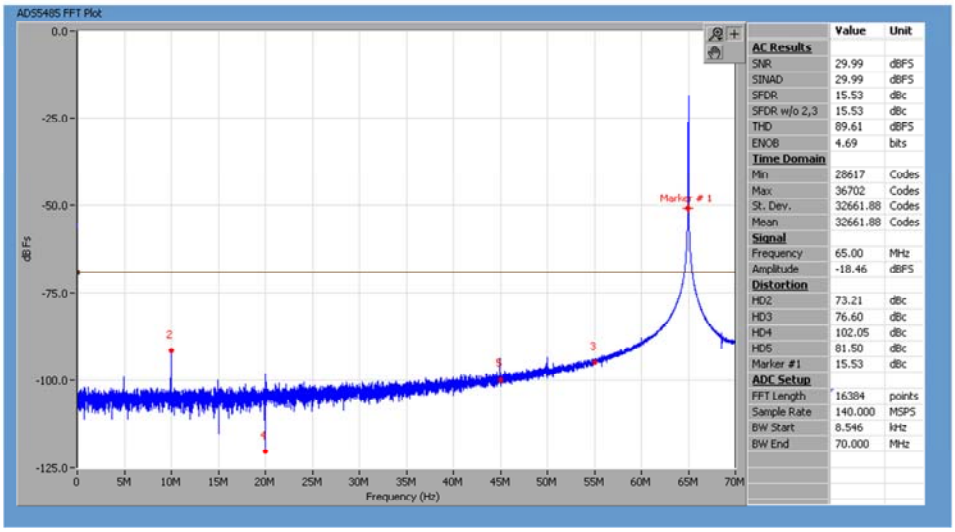

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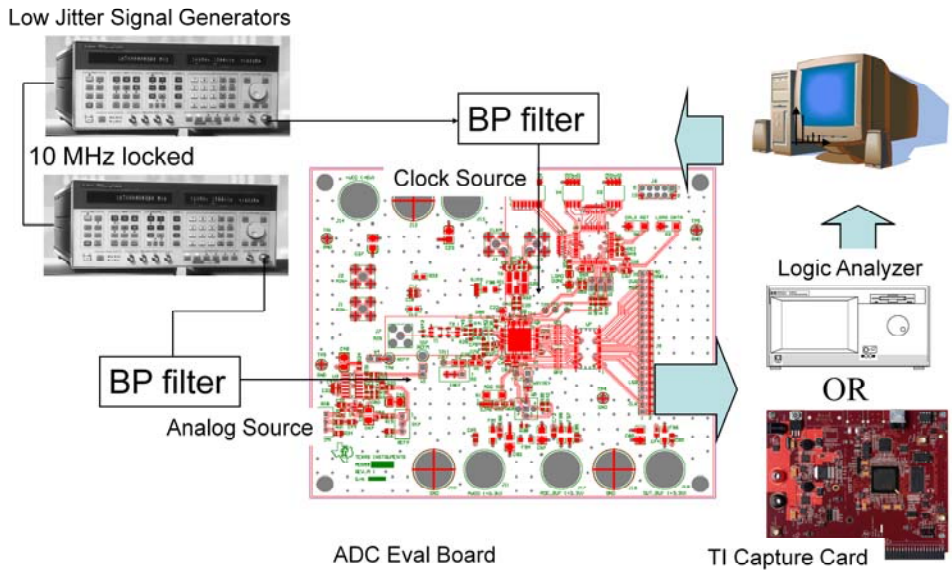
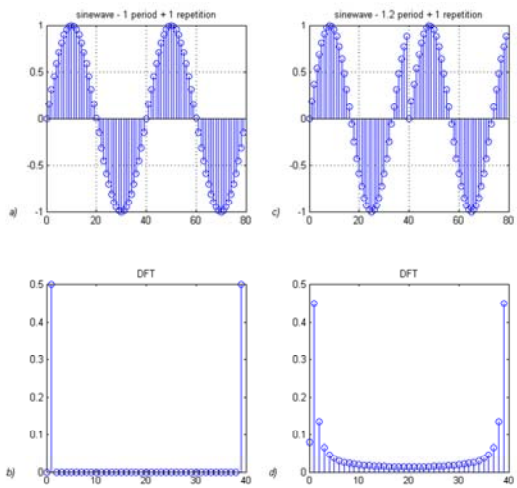
Testing HS ADCs

Testing HS ADCs



Leakage



- Non-integer number of periods within a FFT window causes discontinuity

Coherent Sampling

To avoid leakage in ADC testing, use coherent sampling or Windowing!

$$\frac{f_{signal}}{f_{sample}} = \frac{M}{N}$$

M = number of signal cycles, periods (integer & odd, better a prime number)

N = FFT size (integer)

Example:
Fsignal = 170MHz, Fsample = 110MHz, FFT size = 8192

$$M = \frac{f_{signal}}{f_{sample}} \cdot N = \frac{170MHz}{110MHz} \cdot 8192 = 12660.36$$

With M=12661 (integer and odd), we get for Fsignal:

$$f_{signal} = \frac{M}{N} \cdot f_{sample} = \frac{12661}{8192} \cdot 110MHz = 170.008544922MHz$$

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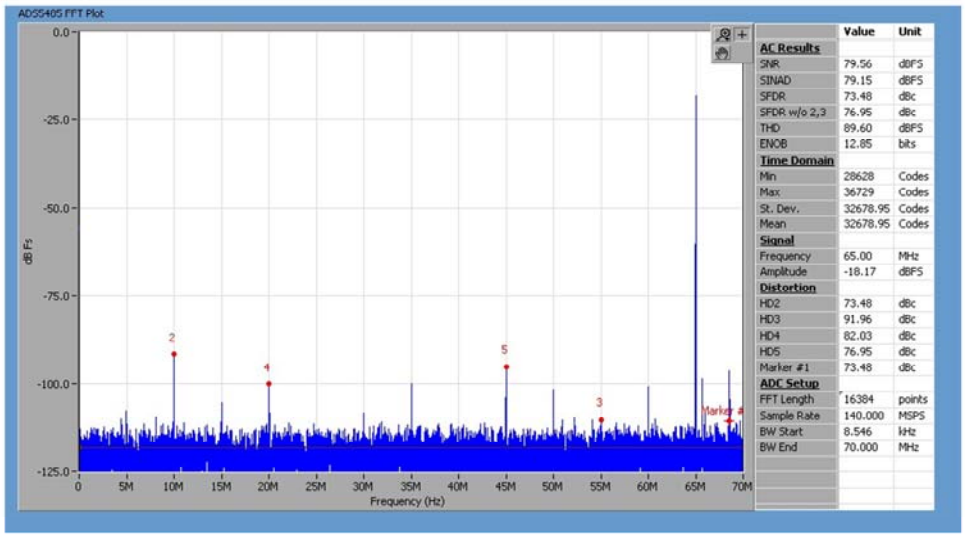
Coherent sampling



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High Speed DACs

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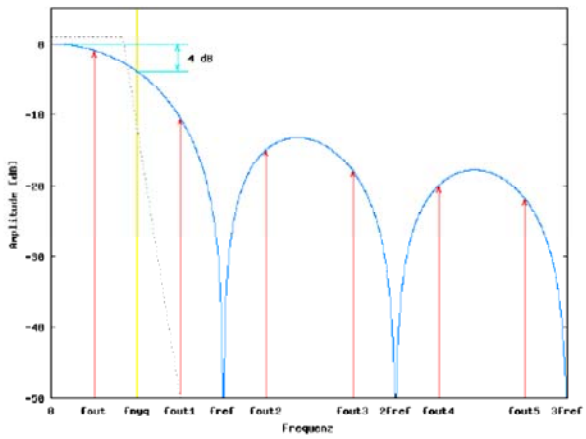
DAC output spectrum



- DAC output spectrum follows a sinc shape
- A signal close to the Nyquist frequency is attenuated by 4dB
- Images are located at multiples of the sampling frequency +/- the signal

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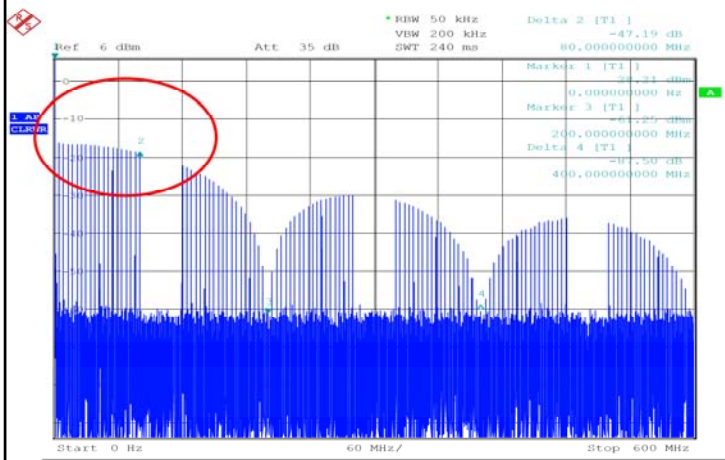
DAC Output Spectrum without ISINC filter



- Fs=200Msps
- Fin=0-80MHz
- SINC shape attenuates the signal at fs/2 by 4dB
- DAC images are located at

$$n \cdot f_{DAC} \pm m \cdot f_{SIG}$$

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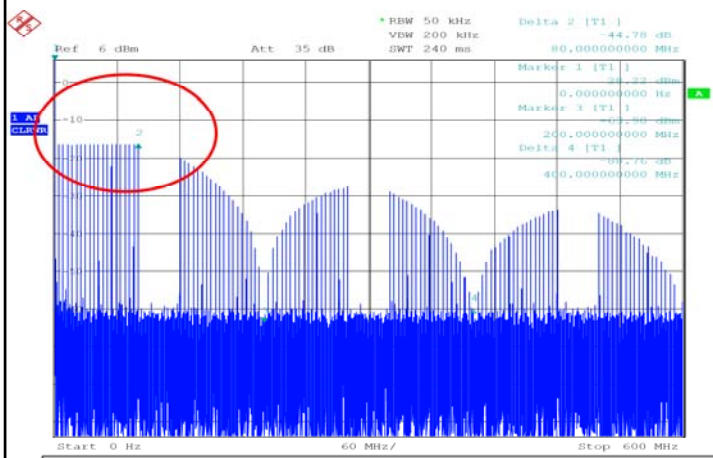
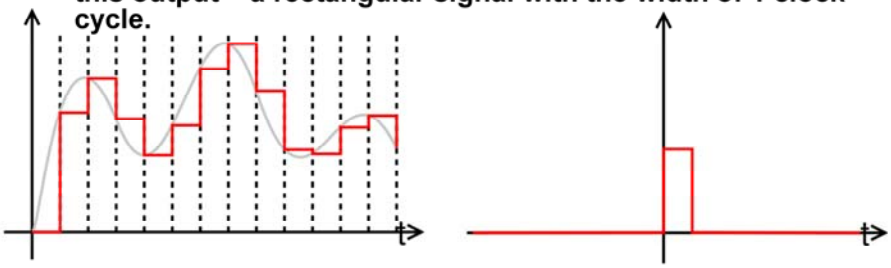
DAC Output Spectrum with ISINC filter



- The inverse SINC filter (ISINC) can compensate for this behavior up to 40% of the sampling rate

Where does this SINC shape come from?

- Ideally, DACs generate a constant value for a complete clock cycle.
- Convolving this impulse response with the original sample sequence will create the ideal DAC output
- In other words, the DAC looks like a filter with this "impulse response"
- Put an impulse into a DAC {0,0,0,…,1,0,0,0,…}, and you'll get this output – a rectangular signal with the width of 1 clock cycle.



SINC / ISINC

$$H(j\omega) = \frac{1 - e^{-j\omega t_{clock}}}{j\omega}$$

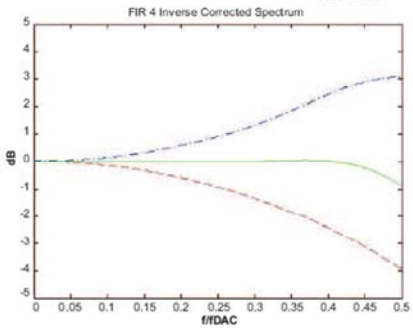
frequency response of the Zero-Order-Hold (ZOH)

$$|H(\omega)| = t_{clock} \bullet \frac{\sin(\frac{\omega t_{clock}}{2})}{\frac{\omega t_{clock}}{2}}$$

after a bunch of trig lookups, its looks like sinx/x

$$|H(2\pi f_{signal})| = \frac{1}{f_{clock}} \bullet \frac{\sin(\frac{\pi f_{signal}}{f_{clock}})}{\frac{\pi f_{signal}}{f_{clock}}}$$

substituting 2*pi*fclock and normalizing to fin/fclock



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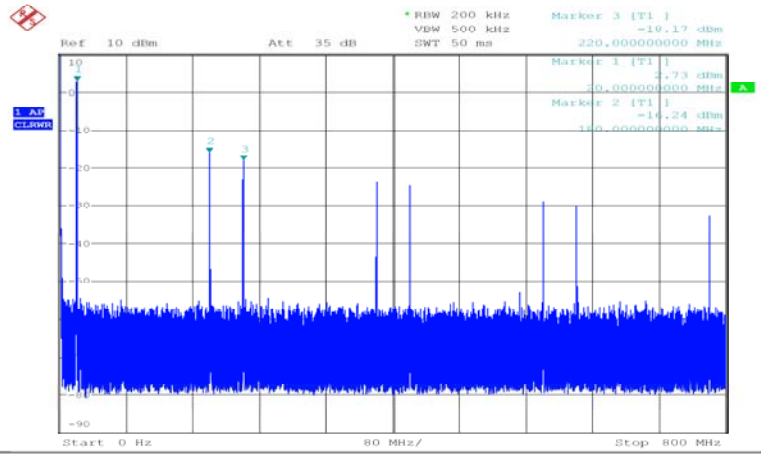
DAC5688 interpolation x2

Samplingrate = 200MSPS; datarate = 100MSPS; signal = 20MHz



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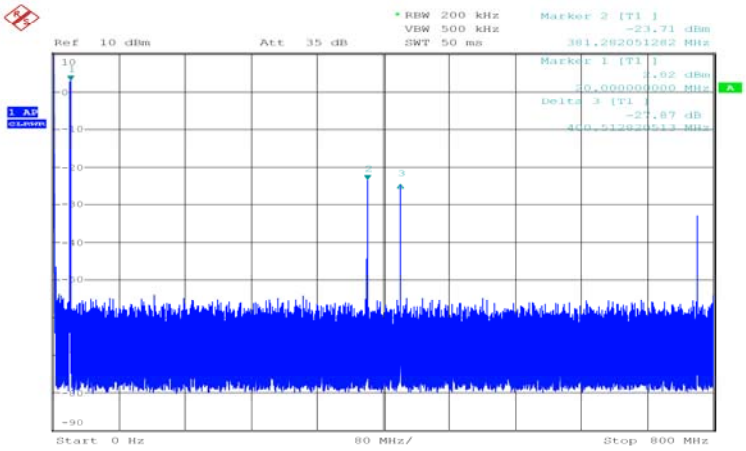
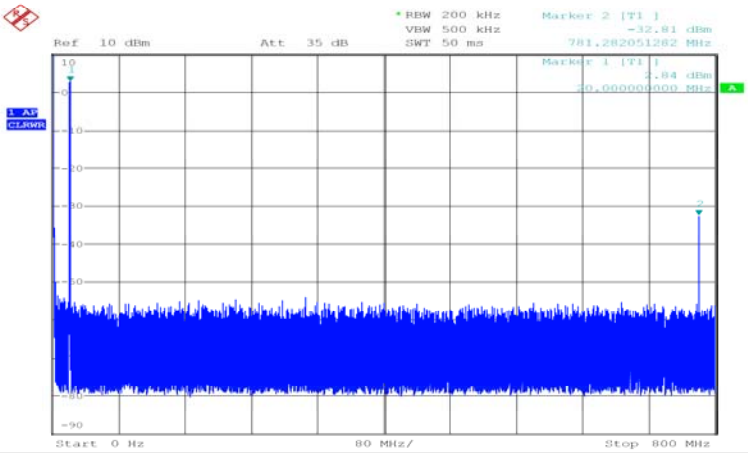
DAC5688 interpolation x4

Samplingrate = 400MSPS; datarate = 100MSPS; signal = 20MHz



DAC5688 interpolation x8

Samplingrate = 800MSPS; datarate = 100MSPS; signal = 20MHz



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Why not clock at 800MSPS without interpolation?

- The datarate needs then to be also at the same speed
  - CMOS outputs generate lots of noise and causes EMI at such high rates, due to fast edges and high voltage swings.
  - Many digital devices can't operate that fast
  - LVDS would double the interface pins
    - Or using LVDS with DDR/QDR

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Benefits of interpolation

- The DAC can run at higher frequencies in order to get more distance between signal of interest and the image → easier filtering
- Interface between DAC and digital device slower → less noise / EMI
- Due to oversampling SNR is improved because of processing gain
- With higher sampling rate, you can output the signal at a higher IF

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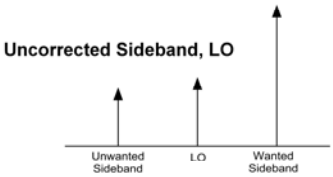
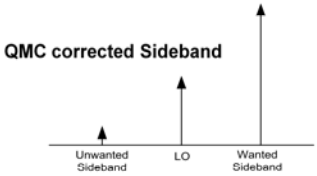
Quadrature Modulator Correction

IQ amplitude and phase correction

- Ideal IQ signal chain
  - Perfect matching of IQ path results in complete sideband rejection
- Realistic IQ signal chain
  - Non ideal matching results in imperfect sideband suppression (typically -40dBc)
- DAC registers allow some adjustment on I and Q to get better sideband suppression (typically -70dBc)





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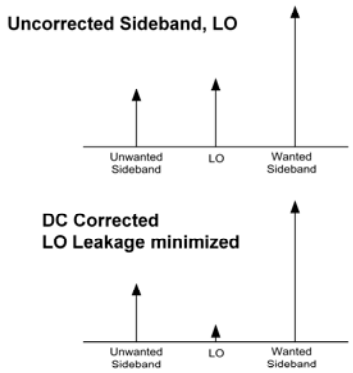
Digital DC Offset Correction

DC offset correction

- Ideal Signal Chain
  - DC offset between I and Q is 0, resulting in 0 DC content at LO carrier frequency (No LO feed through from DC)
- Realistic Signal Chain
  - There is a small mismatch in the DC paths resulting in some LO feed through (typically -40 dBm)
- DAC digital offset registers correct for DC mismatch resulting in reduced LO feed through (typically -70dBm or lower)



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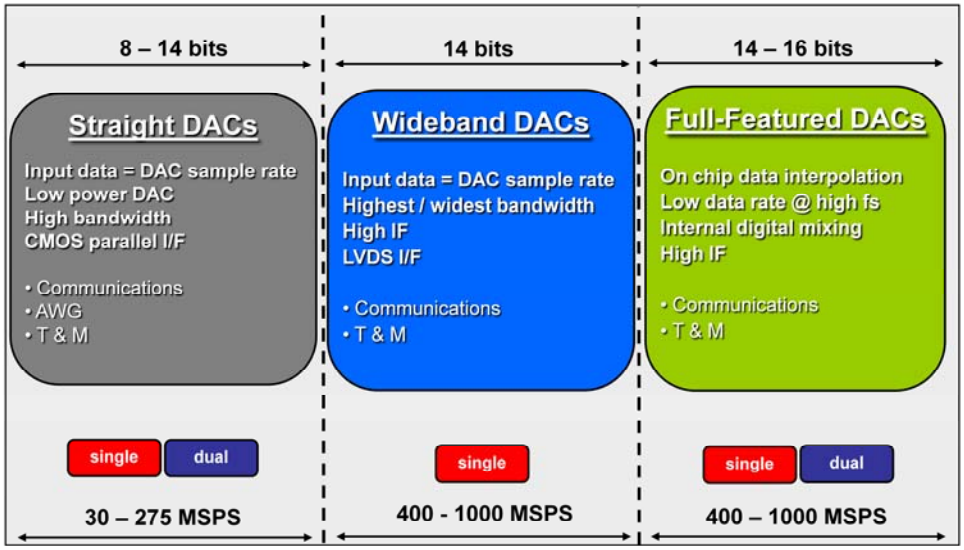
High Speed DAC Families



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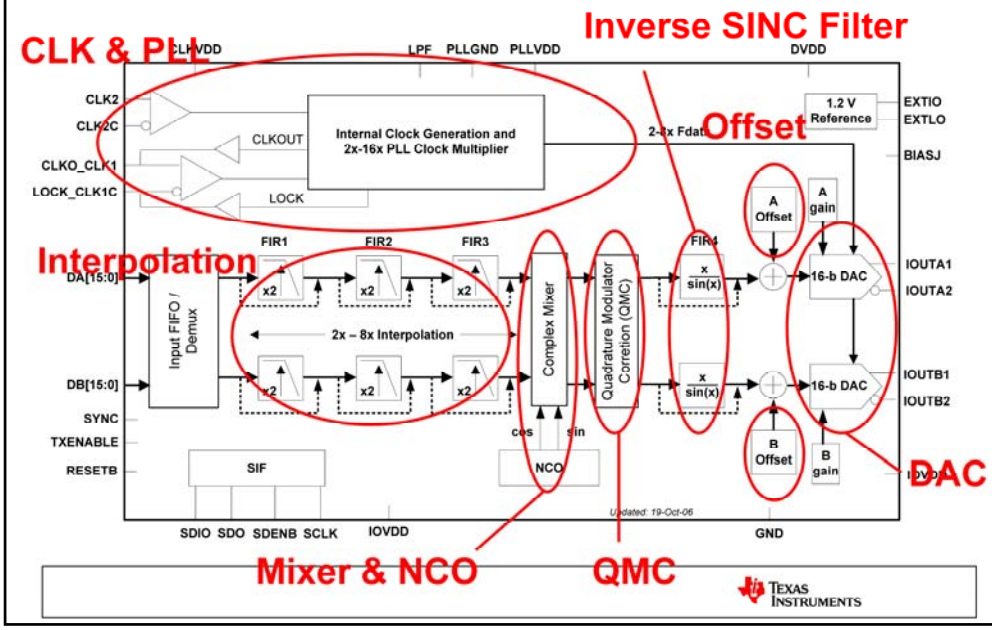
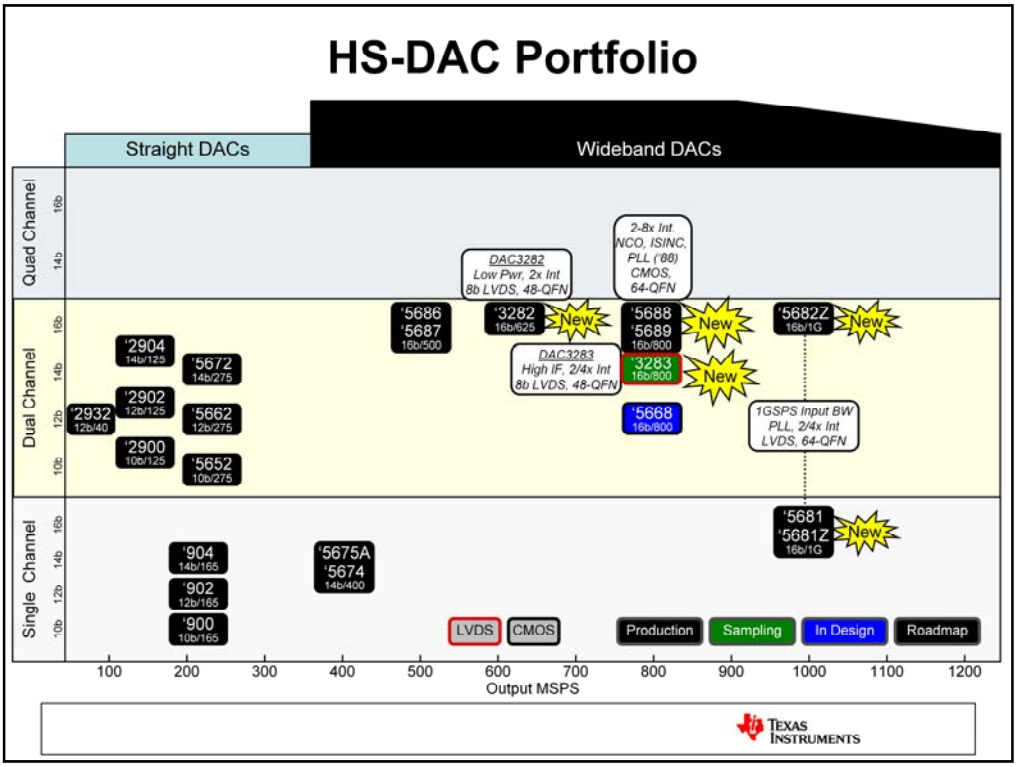
DAC5688 – 800MSPS/16bit




HS-DAC Portfolio
Straight DACs
Wideband DACs
Quad Channel
Dual Channel
Single Channel
16b
14b
12b
10b
'2904 14b/125
'5672 14b/275
'2902 12b/125
'2932 12b/40
'5662 12b/275
'2900 10b/125
'5652 10b/275
'904 14b/165
'902 12b/165
'900 10b/165
'5675A '5674 14b/400
'5686 '5687 16b/500
DAC3282 Low Pwr, 2x Int 8b LVDS, 48-QFN
'3282 16b/625
New
DAC3283 High IF, 2/4x Int 8b LVDS, 48-QFN
2-8x Int. NCO, ISINC, PLL ('88) CMOS, 64-QFN
'5688 '5689 16b/800
New
'3283 16b/800
New
'5668 16b/800
'5682Z 16b/1G
New
1GSPS Input BW PLL, 2/4x Int LVDS, 64-QFN
'5681 '5681Z 16b/1G
New
LVDS
CMOS
Production
Sampling
In Design
Roadmap
100
200
300
400
500
600
700
800
900
1000
1100
1200
Output MSPS
Texas Instruments

Thank you!

Texas Instruments