TI Technology Days 2010

Aero, Defense and High Temperature Industrial

Ioannis Tsikouris-Willgers

Business Development Manager

ioannis@ti.com

Texas Instruments

Agenda

- Market Introduction.
- Reliability Care Abouts
- The Aero, Defense and High Temp Touch

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Part I

Market Introduction

Aerospace & Defense market segments

Traditional markets

Defense

Avionics

Space

New markets For TI HiRel Group

Industrial / Harsh environments

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TI in the Aerospace & Defense Industry

Commitment
- 30+ years of experience in the Aerospace & Defense industry
- Largest dedicated organization in the industry
- Worldwide sales and support infrastructure

Leading-edge technology and manufacturing
- HiRel approved fabs (certified by Defense & Aerospace standards)
- Access to latest process technologies (HPA07, BiCom, etc.)
- Broad packaging capabilities

Market expertise
- Baseline control
- qualification per unique market requirements
- TID, SEU, high-temp, ceramic, QML –Q/V, EP, die solutions…

Extended product life cycles
- Obsolescence mitigation
- Supply beyond commercial availability
- Product resurrection

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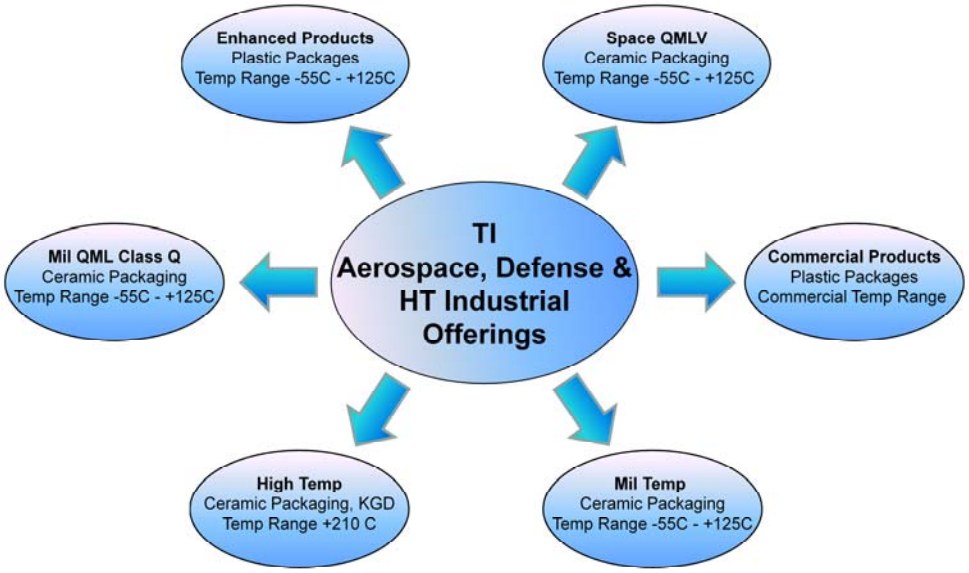
TI Has the Experience to Support Several Specs



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Part II

Aerospace & Defense
Reliability Care abouts

Major Five Care-abouts

- Availability in the right specs.
- Reliability.
- Long Time Support
- Longevity
- Price

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Common Reliability Terms

- EM (Electromigration)
- SM (Stress migration)
- TDDB (Time Dependent Dielectric Breakdown)
- Kirkendall voids
- TID (Total Ionizing Dose)
- SEE
  - SEU — *Single event upset*
  - SEFI — *Single event functional interrupt*
  - SEL — *Single event latch-up*
  - SEGR/SEB — *Single event gate rupture/Burnout*

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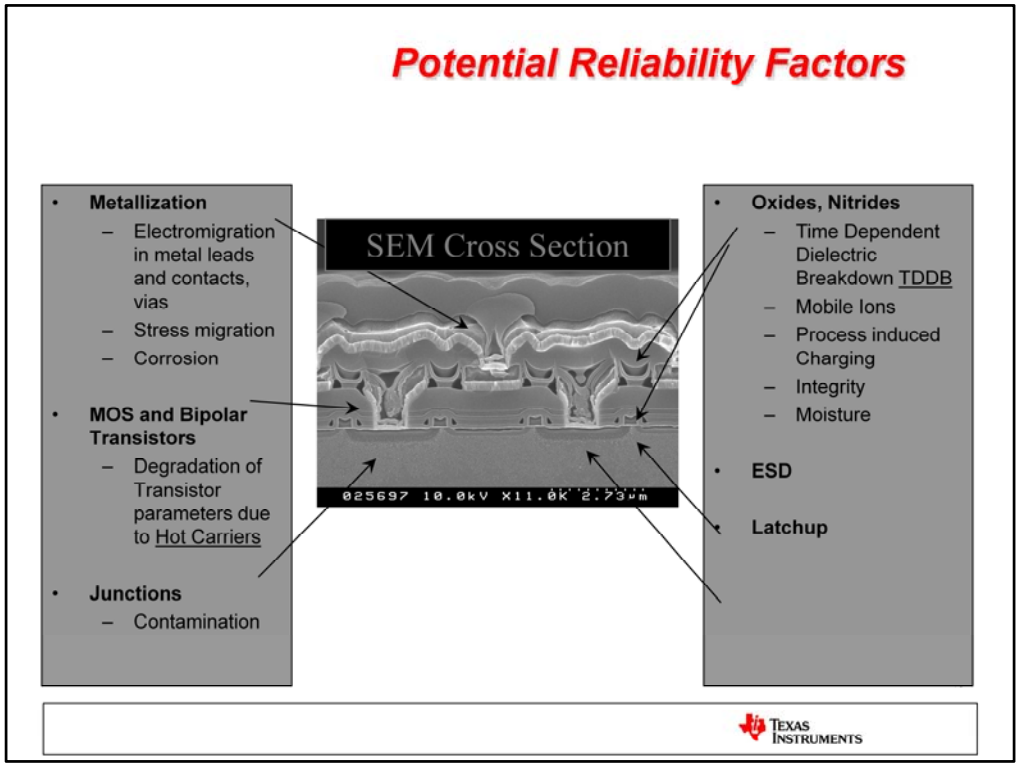


Time-Dependent Dielectric Breakdown (TDDB) is a charge injection mechanism, the process of which may be divided into 2 stages - the build-up stage and the runaway stage.

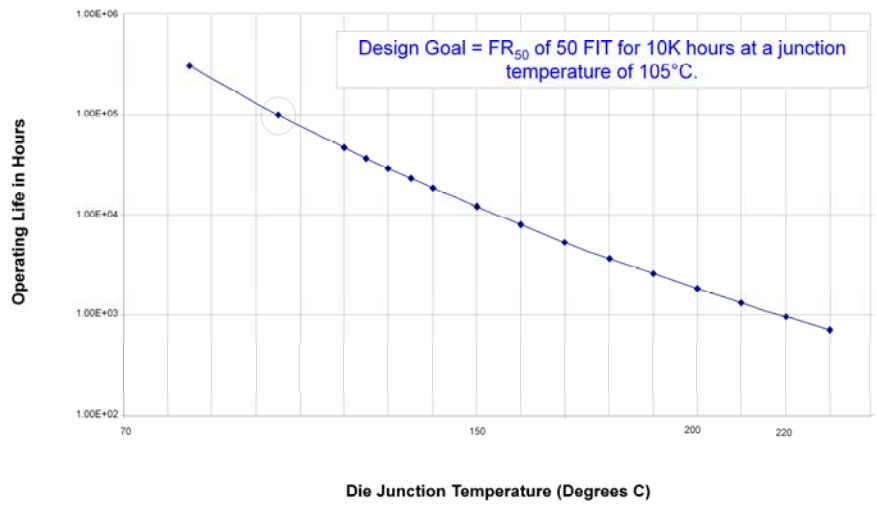
During the build-up stage, charges invariably get trapped in various parts of the oxide as current flows in the oxide. The trapped charges increase in number with time, forming high electric fields (electric field = voltage/oxide thickness) and high current regions along the way. This process of electric field build-up continues until the runaway stage is reached.

During the runaway stage, the sum of the electric field built up by charge injection and the electric fields applied to the device exceeds the dielectric breakdown threshold in some of the weakest points of the dielectric. These points start conducting large currents that further heat up the dielectric, which further increases the current flow. This positive feedback loop eventually results in electrical and thermal runaway, destroying the oxide in the end. The runaway stage happens in a very short period of time.

Stress Migration is a failure mechanism that often occurs in IC metallization (aluminum, copper). Voids form as result of vacancy migration driven by the hydrostatic stress gradient. Large voids may lead to open circuit or unacceptable resistance increase that impededs the IC performance. **Stress Migration** is often referred as **Stress Voiding**, **Stress Induced Voiding**

Hot Carriers injection (HCI) is the phenomenon in solid-state or semiconductor electronic devices where either an electron or a "hole" gains sufficient kinetic energy to overcome a

Derated High Temperature Operating Life



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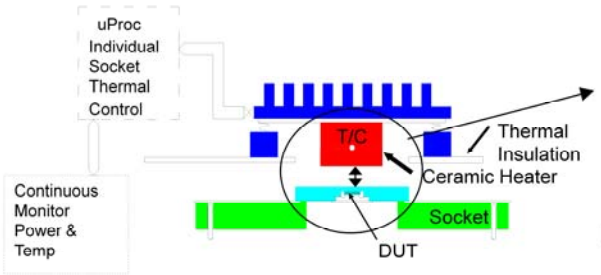
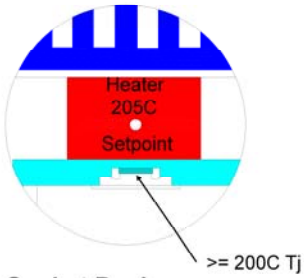
Example Life Test Methodology

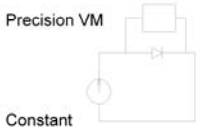




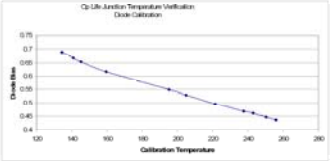
New Socket Design For Hi Temp Op Life Evaluation in Standard Oven

Calibration

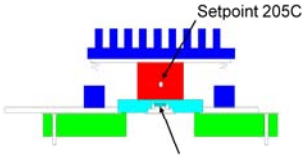
1 Assemble device With Thermal Diode in Equiv Package



2. Place in calibrated oven, unpowered, allow to stabilize at various temperatures & record Vfb



3. Install calibration Device in Op Life test socket with Heater



Read Tj (unpowered) > 200C All Positions

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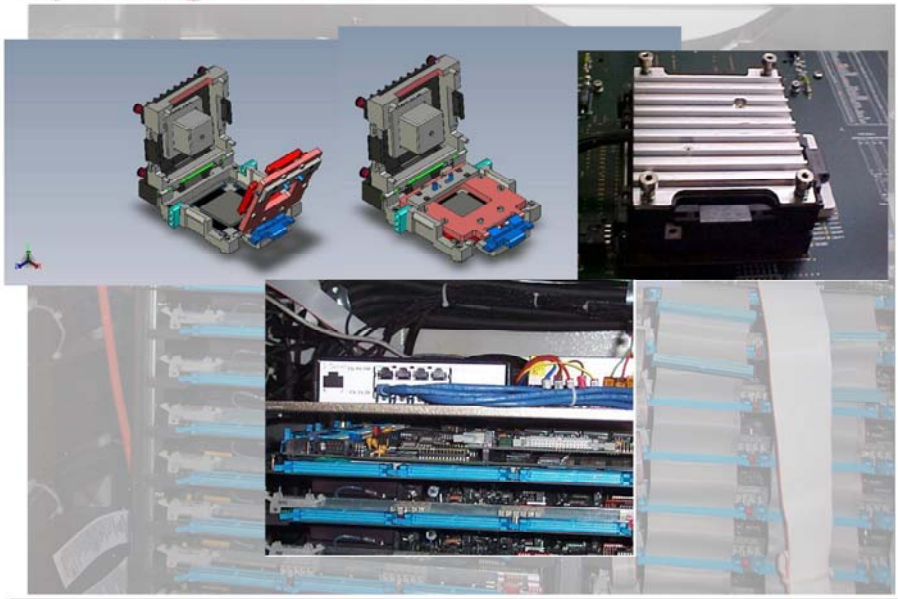
TEXAS INSTRUMENTS

Operating Life Test Boards



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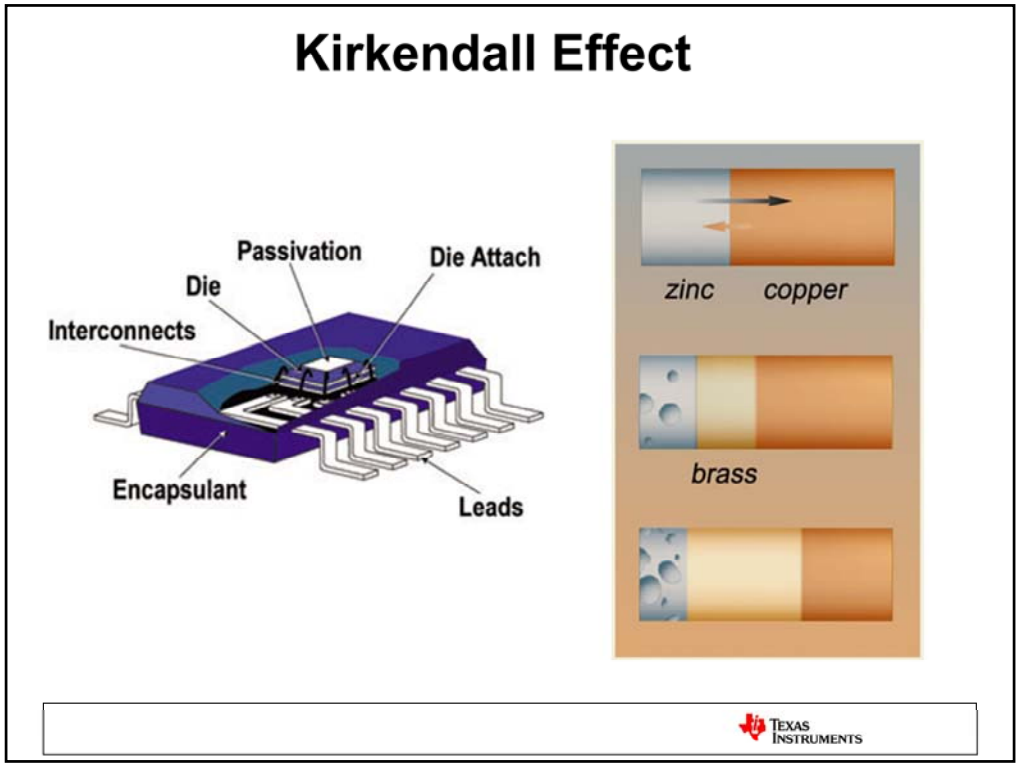
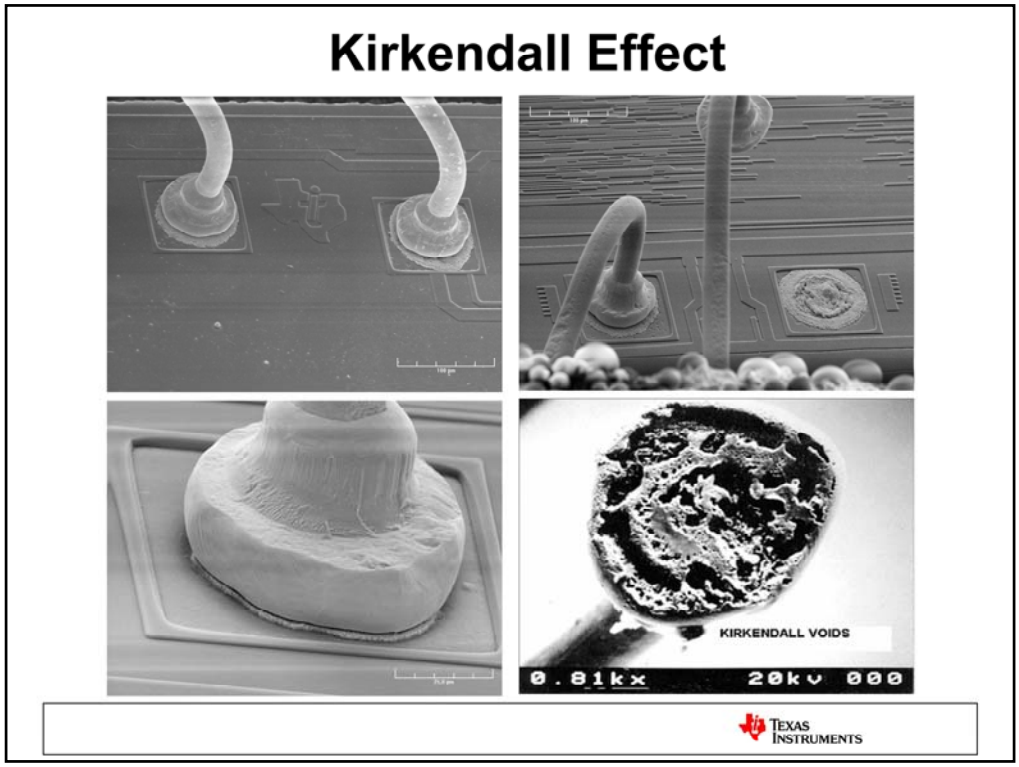
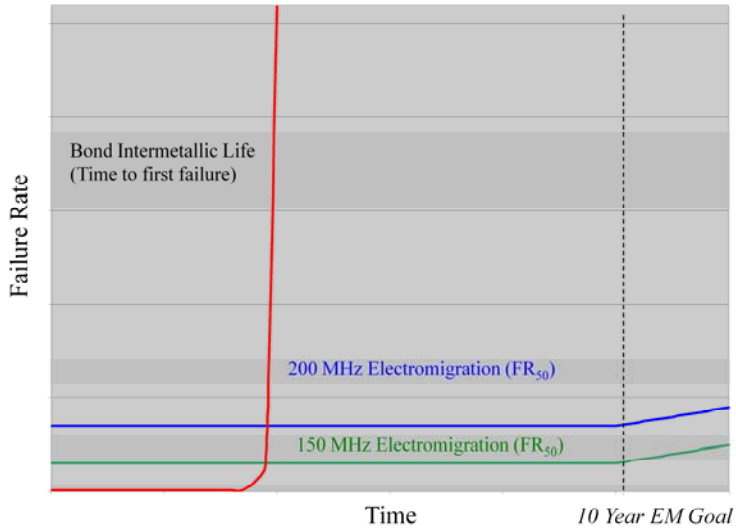


The Kirkendall effect. At the boundary between two solids diffusing into each other at different rates, for example zinc and copper, their alloy (brass) grows in the direction of the faster-moving species (zinc). Unfilled voids are left behind and coalesce into large pores. (After Preston Huey, *Science*)



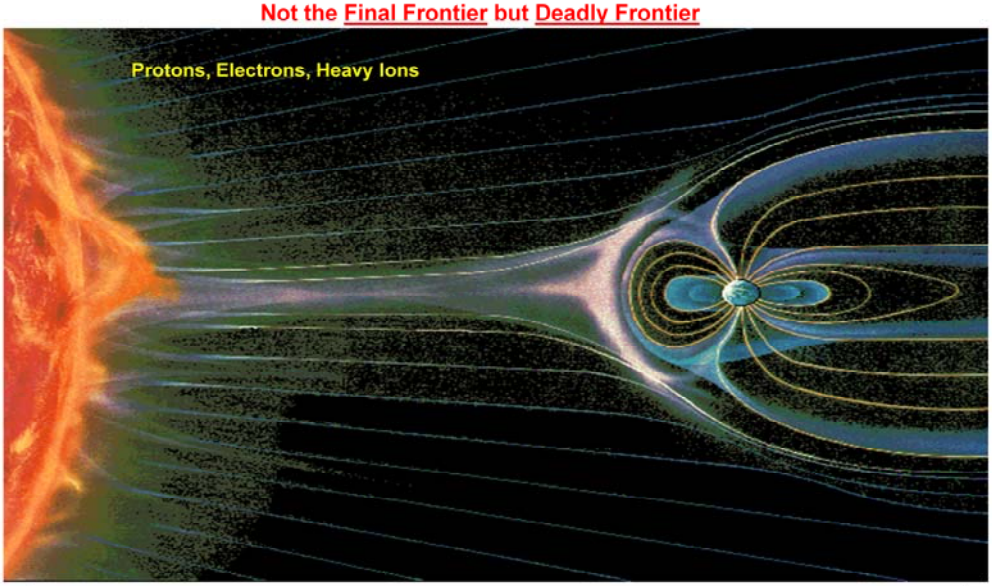
Here are some REAL examples of Kirkendall voids. You can see the intermetallic layer (Here purple plag) between the die and the bond.

Relative Comparison of Failure Mechanisms (Shape of the Curve)



Radiation Effects

Not the Final Frontier but Deadly Frontier



Nikkei Science, Inc. of Japan, by K. Endo

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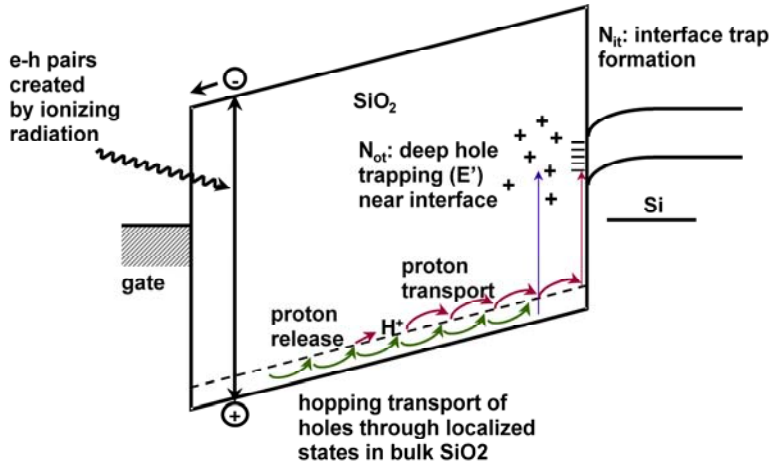
Ionizing Total Dose Radiation Effects

Oxide and Interface-Trap Charge Creation In Oxides and MOS structures



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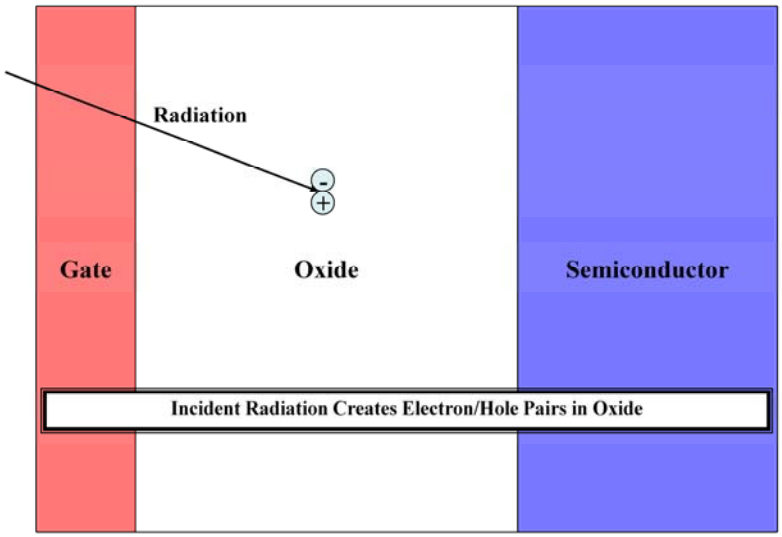
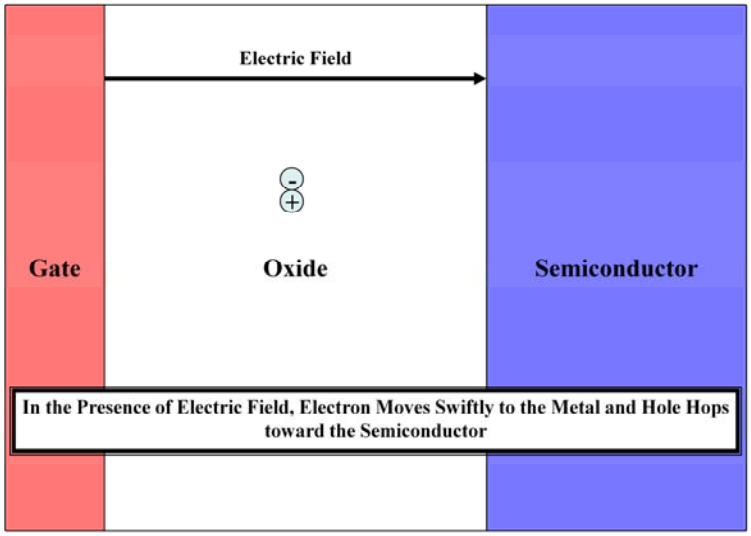
Fundamental TID Mechanisms



Fundamental TID Mechanisms



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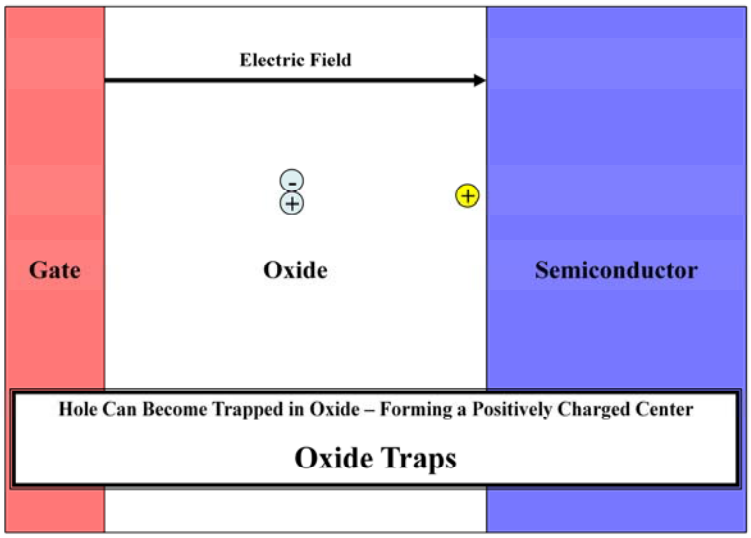
Fundamental TID Mechanisms



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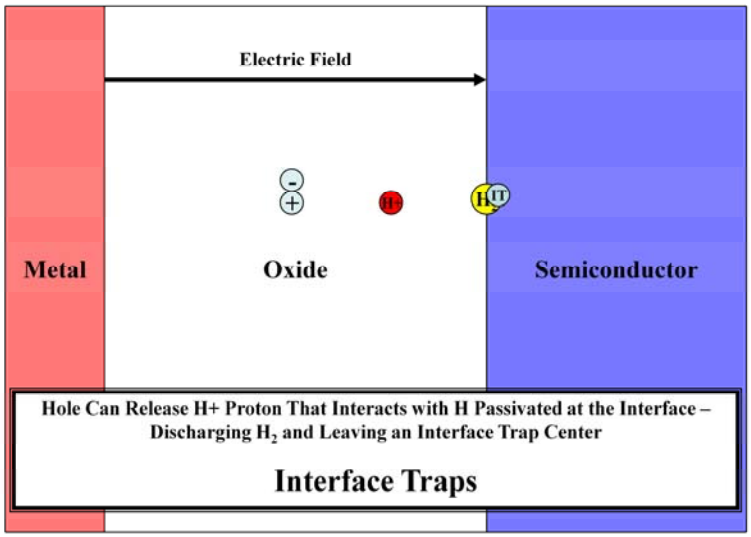
Fundamental TID Mechanisms



Hole Can Release H+ Proton That Interacts with H Passivated at the Interface – Discharging H_2 and Leaving an Interface Trap Center

Interface Traps

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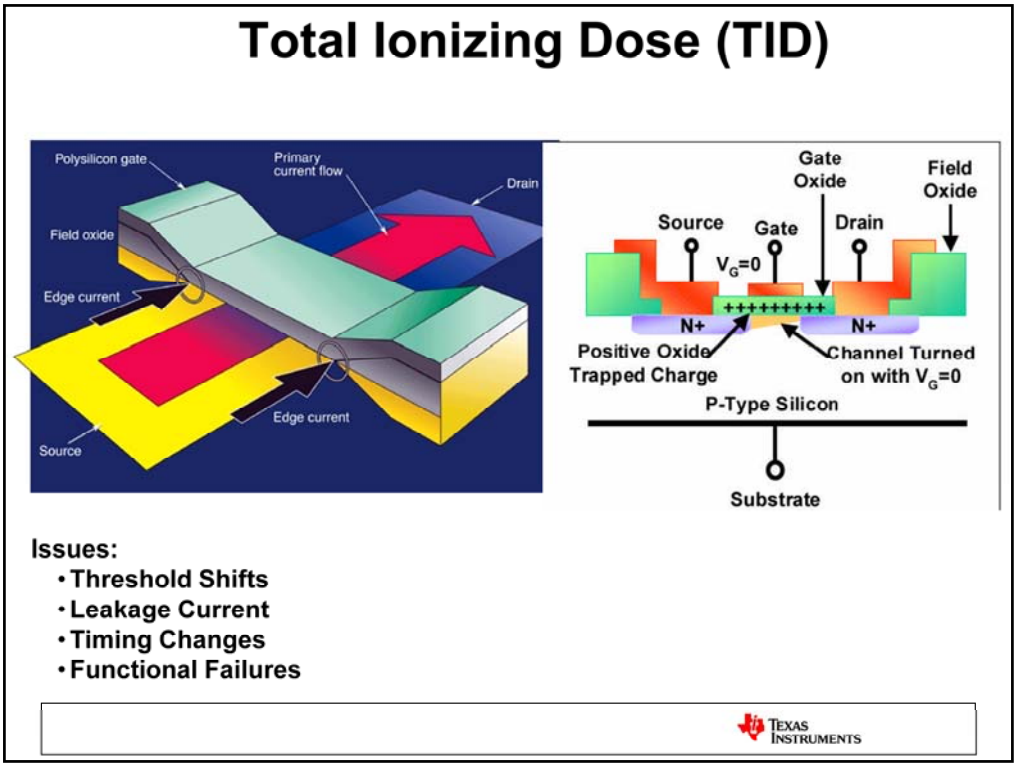


The first satellite failure due to total dose was the Telstar. Telstar was launched a day after the July 9, 1962 Starfish nuclear test. The Starfish, a nuclear weapon of 1.4 Megaton strength, was detonated at an altitude of about 248 mi (~400 km) above Johnston Island in the Pacific Ocean. The explosion produced beta particles (electrons) that were injected into the earth's magnetic field and which formed an artificial radiation belt. This artificial electron belt lasted until the early 1970s. The Telstar experienced a total dose 100 times that expected due to the weapon test. Starfish destroyed seven satellites within 7 months primarily from solar cell damage.

The *total ionizing dose* (TID), mostly due to electrons and protons, can result in device failure (or biological damage to astronauts). In either case, TID can be measured in terms of the *absorbed dose*, which is a measure of the energy absorbed by matter. Absorbed dose is quantified using either a unit called the *rad* (an acronym for **r**adiation **a**bsorbed **d**ose) or the SI unit which is the gray (Gy); 1 Gy = 100 rads = 1 J/kg.

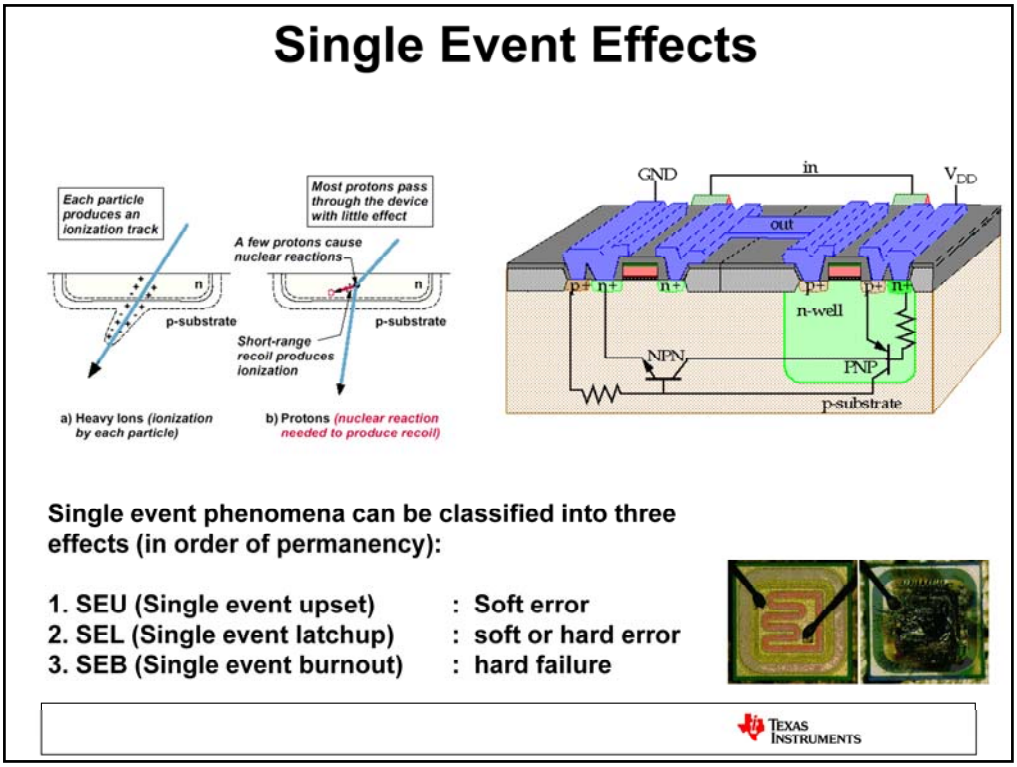
The TID is calculated from the trapped protons and electrons, secondary Bremsstrahlung photons, and solar flare protons (the contribution from galactic cosmic ray ions is negligible in the presence of these other sources). The main sources of the protons and electrons are from solar energetic particle events (from solar flares), and passage through the South Atlantic Anomaly. In low earth orbit (LEO), the main dose source is from electrons and protons (inner belt); and in geostationary earth orbit (GEO), the primary source is from electrons (outer belt) and solar protons.

Charge buildup affects the current-voltage characteristics of the transistors used in semiconductor circuits.

Proper operation of a transistor relies on the ability to switch it from a low-conductance (off) state to a high-conductance (on) state as the gate voltage passes through a threshold. Extended exposure to radiation can shift the threshold voltages (*top image*), making the transistors easier or harder to switch. Radiation may also increase the leakage current (*bottom image*), causing the on and off states of the transistors to become less distinguishable. Either effect can ultimately cause circuit failure.

Edge-current leakage in transistors.

Current should flow only between the source and the drain when the gate receives a proper voltage; however, after extended exposure to ionizing radiation, current can leak through at the edges, where the gate oxide and insulating field oxide meet. When leakage current bypasses the transistor's isolated regions, it degrades the distinguishability of the transistor's "on" and "off" states. Leakage also increases the circuit's background current, or the amount of current flowing when the device is in a quiescent state. Such an increase, multiplied by the tens



Single Event Latchup

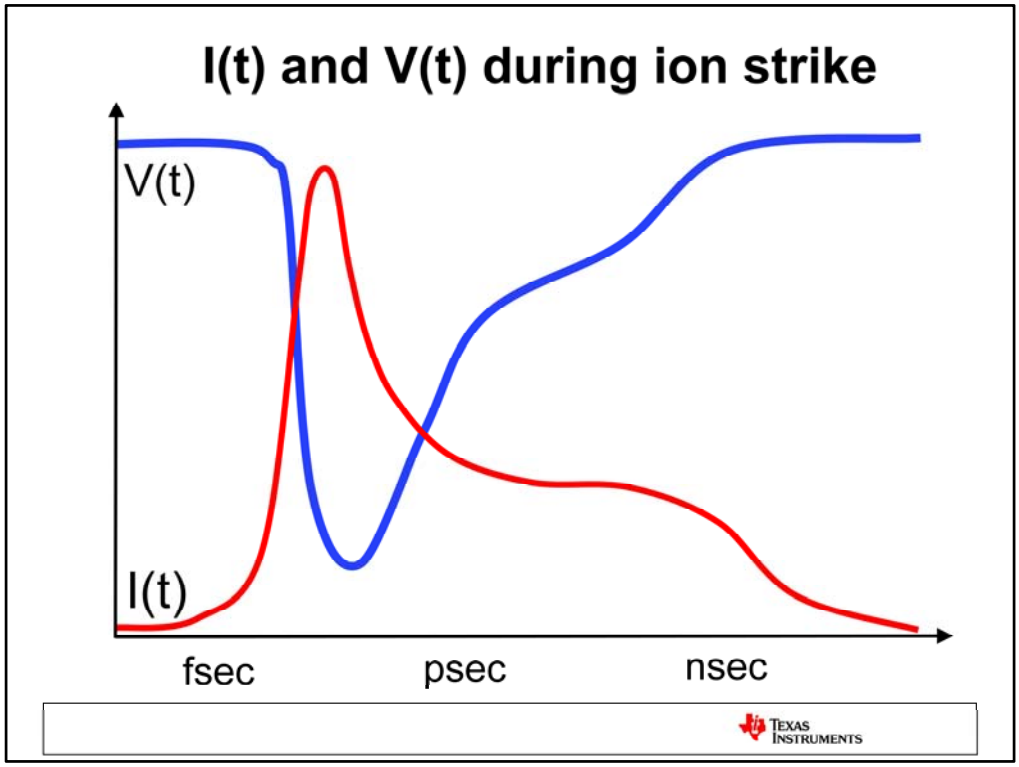
Latchup

Most junction-isolated circuits contain parasitic *bipolar* transistors that can form a four-layer region, similar to that of a silicon-controlled rectifier. These bipolar structures are not involved in normal operation of CMOS devices, but can be triggered by transient currents. On the right hand image you could see the bipolar structures that create a four-layer latchable structure in a p-well CMOS circuit. Latchup disrupts normal operation in the region of the circuit where it occurs, causing partial loss of functionality as well as higher current in the local region where latchup occurs.

Once latchup occurs, the four-region structure will be switched into a conducting mode, and it will remain in that mode until power is removed, or until the voltage across the latched region is reduced to very low values. During latchup currents can be very high. In most circuits, currents of several hundred milliamps or more will flow in the localized region where latchup is triggered, rapidly heating that region to extremely high temperatures. These high temperatures not only introduce the possibility of localized damage to the silicon and metallizations, but the excessive heating may also cause the latchup to spread to other regions.

All CMOS designs use special guardbands and clamp circuits at input/output terminals to prevent latchup from occurring in standard circuit applications. However, in a radiation environment transient signals are no longer confined to I/O terminals, and it is possible for the current pulses from heavy ions or protons to trigger latchup in internal region of a CMOS device, as well as in I/O circuitry.

Because of the potential for catastrophic damage, latchup is a very serious problem for space systems. The most conservative approach rules out use of any latchup susceptible circuit. A number of methods have also been proposed to overcome latchup at the system or subsystem level by sensing excess current, which is a signature of latchup, and temporarily removing power. However, power must be removed within a few milliseconds after latchup occurs to avoid possible catastrophic damage. It is also difficult to make sure that latchup detection circuits will be completely effective because many different latchup paths exist in complex circuits, with different current signatures. Device scaling generally increases susceptibility to latchup, and latchup is expected to be even more important for devices with reduced power supply voltage and operating power.

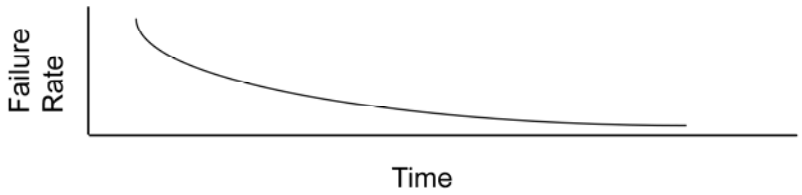


First there is the radiation event itself. In general the event can be imagined as a “roughly” straight line segment (ignoring straggling/channeling) in which a very high degree of ionization takes place. In a region within 1-2um of the node, the actual event itself typically occurs within 10-500 fsec creating a quasi cylindrical track of e-h pairs with a sub-micron radius and a very high carrier concentration. In the junction area carriers are collected immediately by the field. Outside the depletion region e-h pairs are separated by drift and in response to the non-equilibrium charge distribution a funnel shaped potential distortion is formed. A large portion of additional charge is collected by funneling. This leads to an initial current “spike” known as prompt collection. The prompt collection phase is completed within picoseconds. After this point the funnel collapses and diffusion effects begin to occur. Additional charge can be collected as carriers diffuse away from the initial distribution and end up in the sensitive node. Diffusion collection is usually smaller in magnitude but occurs over a longer time scale 1-10s of nanoseconds. In DRAMs with undriven, floating nodes, the diffusion component can add significantly to the total charge - especially in some trench cell designs. However, in nodes that are driven, even weakly, it may be that the drive capability of the transistor providing the current “out matches” the current induced by diffusion collection, and thus this component can be ignored many “static” devices. This diagram illustrates the drop in volatges due to accumulation of electrons on the P+ and the corresponding current. Note that since the node is driven, the voltage eventually recovers once the charge injected by the rad-induced current transient is compensated by the load.

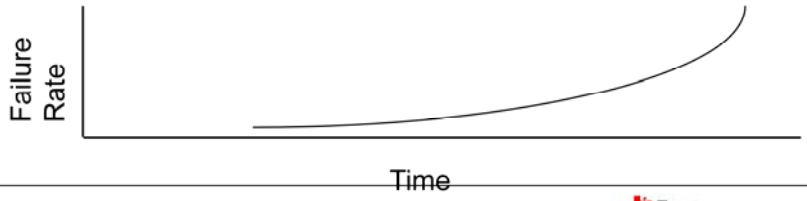
The Reliability Bath Tub Curve

The "bathtub curve" is really the addition of two curves.

Extrinsic failures - caused by some type of processing or material defects



Intrinsic failures - happen as a result of wearout



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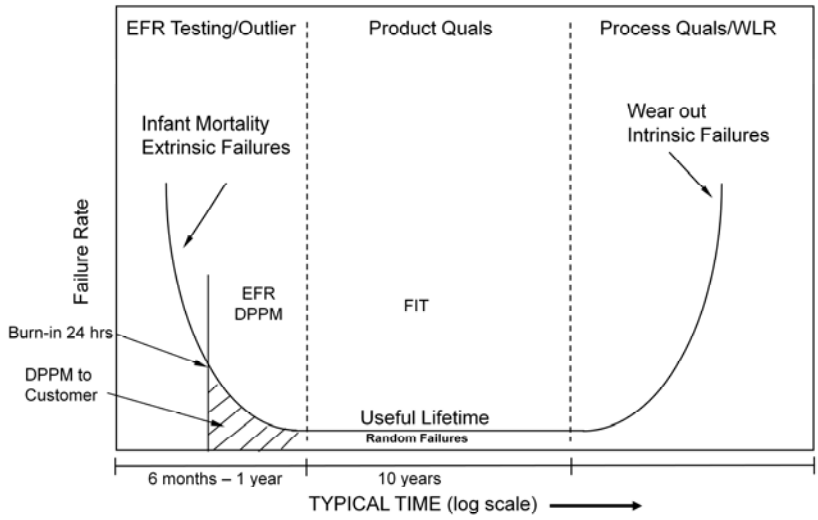
The Reliability Bath Tub Curve

No reliability discussion can be complete without mentioning the bathtub curve.



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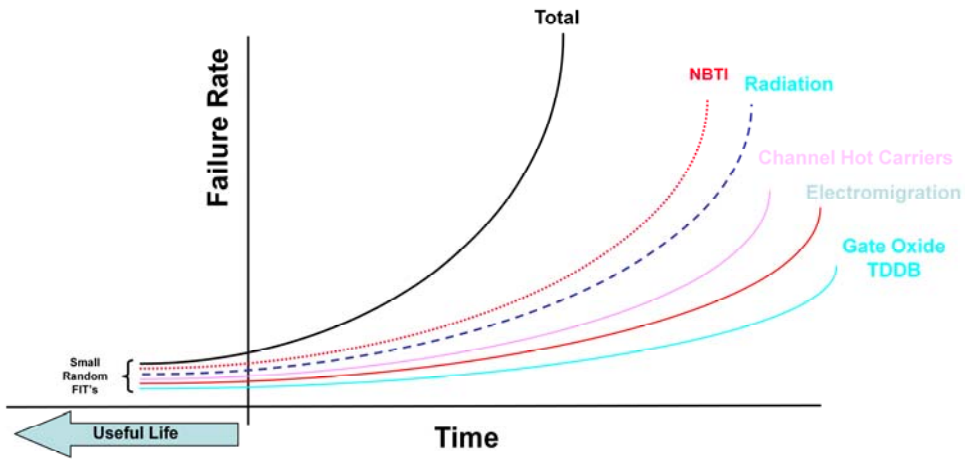
A Closer Look at Intrinsic Failures

The total intrinsic failure curve is the sum of the failure rate of <u>all</u> possible wearout mechanisms.



<u>Radiation is just one of many FIT mechanisms, and often is not the Major mechanism !!!</u>

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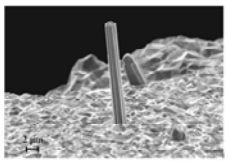
Packaging Reliability

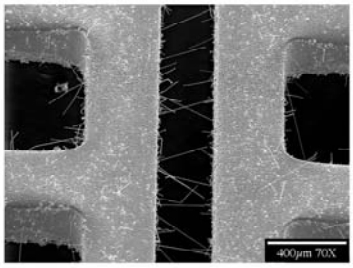
Space Level Reliability – Organic packages reliability concerns remain:

-Residual stresses caused by electroplating
-mechanically induced stresses
-bimetallic stress induced by diffusion
-thermal stresses.

Oh My !!



17 April, 2005 — Millstone Nuclear Generating Station — A single tin whisker created a bridge (short circuit) between a diode and the output trace on a circuit card, causing a partial reactor shutdown. P. Daddona, " New London, CT, July 4, 2005



PB Free - Tin Whiskers

Tin Whiskers growing on a MATTE tin-plated copper lead frame commonly used in the manufacture of 28 pin small outline integrated circuit (SOIC) lead frame after 3 years of ambient storage. From Wikipedia

Photograph of a Tin Whisker Growing through conformal coat.

Tin whiskers caused the failure of the Galaxy IV Satellite in 1998. Wireless Week, 1999-05-17.

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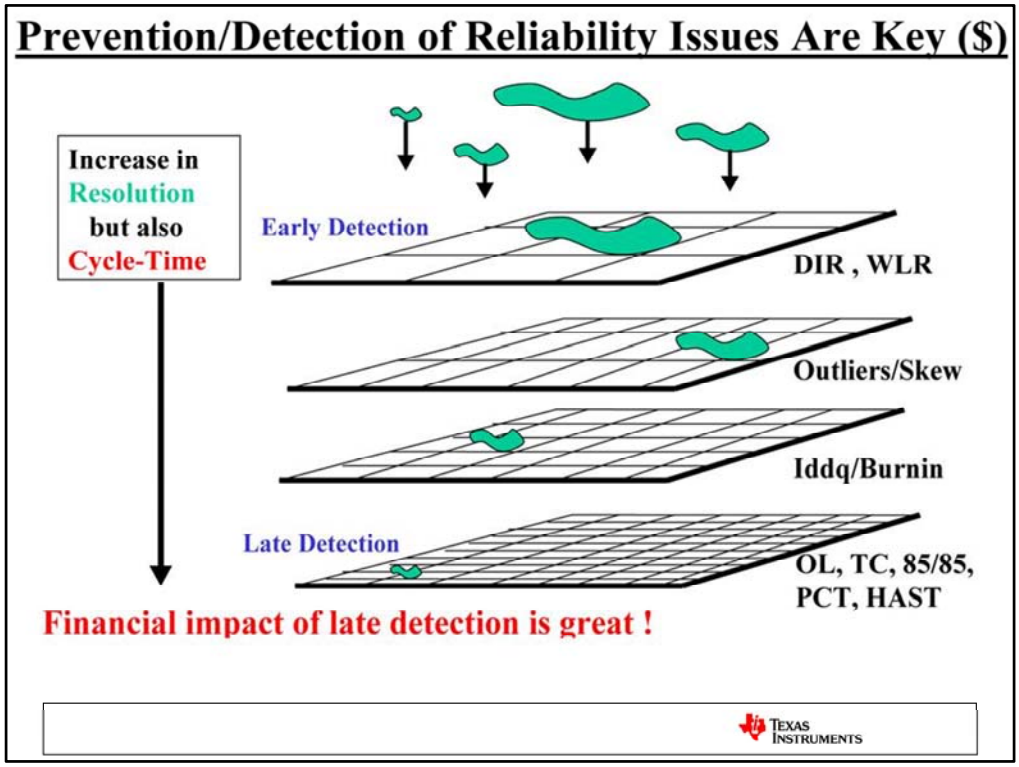
Prevention/Detection of Reliability Issues Are Key ($)
Increase in
Resolution
but also
Cycle-Time
Early Detection
DIR , WLR
Outliers/Skew
Iddq/Burnin
Late Detection
OL, TC, 85/85,
PCT, HAST
Financial impact of late detection is great !
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Reliability Issues & Related Segments

TID	Avionics, Space, Medical
SEE	Avionics, Space
Kirkendall	All of the Aerospace, Defense and HT Applications
SM, EM	All of the Aerospace, Defense and HT Applications
TDDB	All of the Aerospace, Defense and HT Applications

TDDB: Time Dependent Dielectric Breakdown , SM: stress migration (SIV :Stress Induced Voiding)

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Part III

The Aero & Defense and High Temp. Touch

Aerospace Market is not really… "Commercial"

Cost of a satellite mission: 700M$ - 1.5B$

Cost of small plane accident: 150M$

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When do you need HiRel product?

Extreme environments

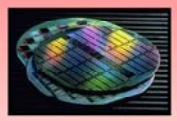
High temperatures

Radiation

Special packaging requirements

Hermetic-Ceramic

Wafer/ Die



Plastic

Regulations/quality requirements

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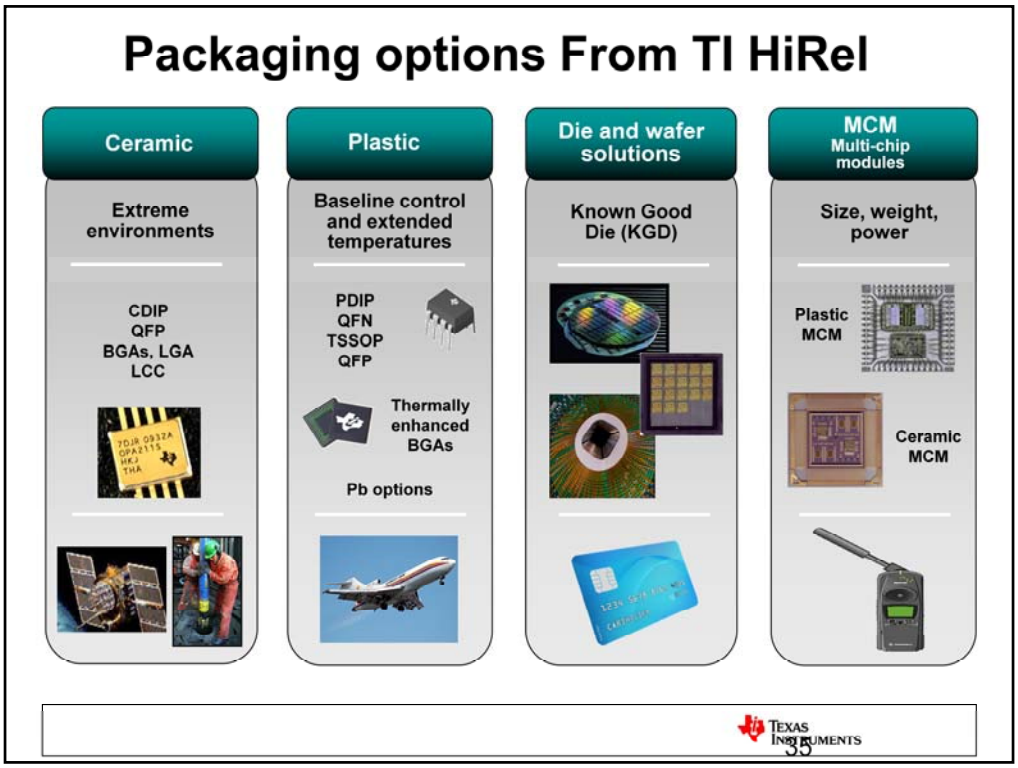

Print 11x17 to MARCOM

Supported Product Specs & Segments

Commercial Products	Plastic Packaging, Commercial Temp Range, Market Segments – Industrial, Medical, Oil Exploration, Aerospace and Defense
Enhanced Products	Plastic Packaging, Wide Temp Range (-55C - +125C), Market Segments – Industrial, Medical, Oil Exploration, Aerospace and Defense
QML Class Q	Ceramic & KGD Packaging, Temp Range (-55C - +125C), Market Segments – Aerospace and Defense, Telecommunications
High Temp	Ceramic & KGD Packaging, Temp Range (+210C), Market Segments– DHD, Aerospace, Automotive
Mil Temp Ceramic	Ceramic Packaging, Temp Range (-55C - +125C), Market Segments– Industrial, Aerospace and Defense
QML Class-V (Space)	Ceramic Packaging, Temp Range (-55C - +125C), Market Segments– Satellite, Telecommunications
Die/Wafer KGD	Bare Die, Various Temp Range (-55C - +210C), Market Segments – Commercial, Industrial, Medical, DHD, Aerospace and Defense

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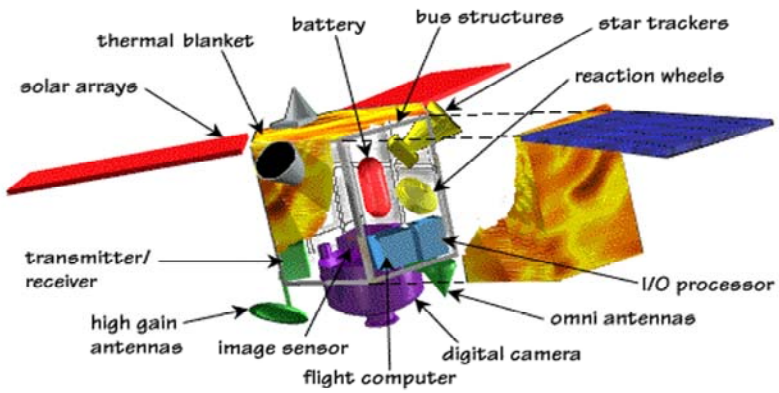
Space Applications



Command & Data
Pointing Control
Communications
Power Supply
Mission Payload
Thermal Control

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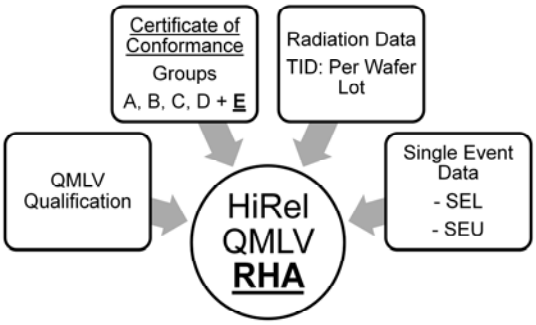
TI RHA QMLV For Space



- Group E Rad conformance report on every RHA Certificate of Conformance (C of C)
- All RHA Plans Approved by DSCC/Aerospace
- TID Radiation Packets Available Per Device

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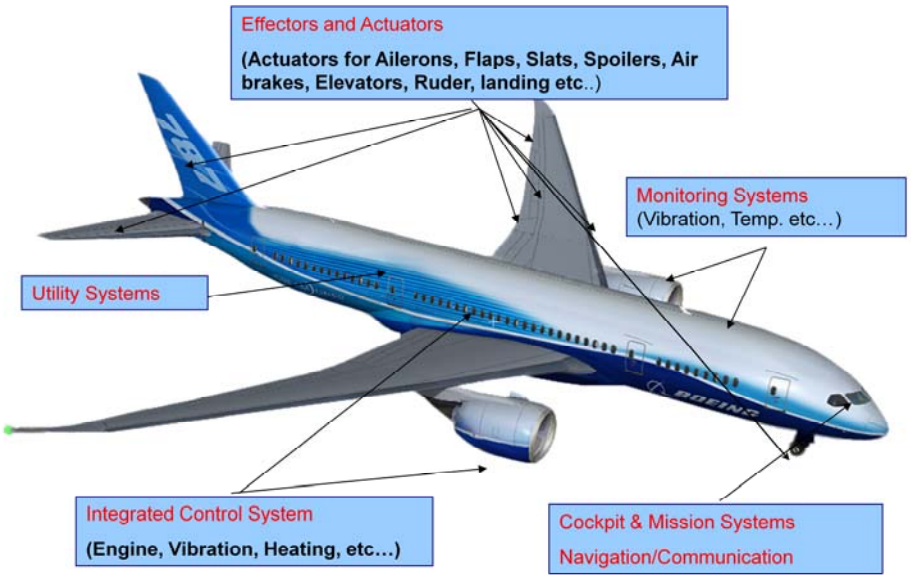
Avionics Applications



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Defense Applications

Avionics

Radar & Com

Missiles

Texas Instruments

EP Enhanced Products

- Fabrication and Assembly Controlled Baseline
- Extended Product Change Notification (PCN)
- Extended Temperature
  - Typically -55°C to +125°C
  - or customer defined
- Qualification pedigree
- Product traceability
- Obsolescence Mitigation
- Access to leading-edge catalog technology
- Widespread of Package offering
- Lead Finishes options

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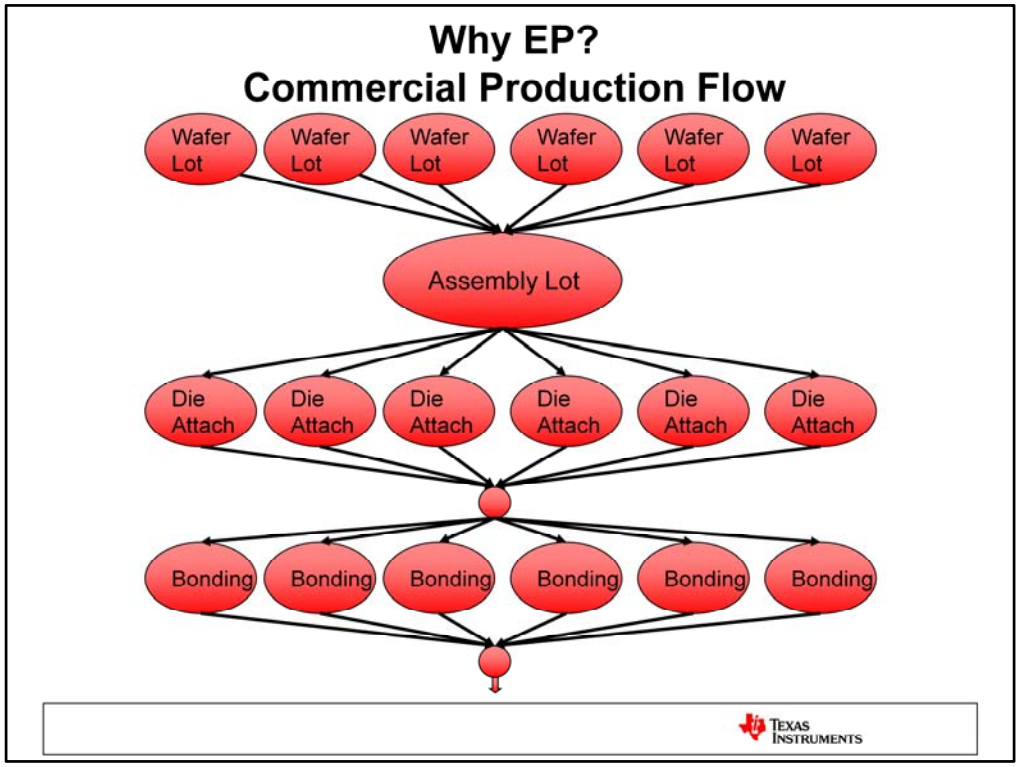

Wafer Run -> Wafer Lot

Example SN74HC138DR Wafer Fabrication Baseline

- **Multiple active wafer fabs**
  - TI SFAB in Sherman, Texas
  - ATC (subcontractor) in Hsinchu, Taiwan
  - ASMC (subcontractor) in Shanghai, China
- **Each wafer fab runs a different baseline**
  - Glassivation (protective overcoat)
  - Base silicon wafers
  - EPI versus non-EPI
  - Diffusion and metal profiles
  - Process equipment

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Over the years the defense community has realized there are multiple obstacles to the effective use of COTS Integrated Circuits.

Military and commercial avionics OEMs currently purchase less than one percent of the total commercial integrated circuits sold. Up to 30% or 40% of COTS devices require uprating or upscreening depending on the OEM and the application. For the purposes of discussion, uprating is defined as use beyond the environment and application for which the part was designed. Upscreening is defined as performing additional testing and/or lot acceptance to use product beyond data sheet conditions. Uprating and upscreening are problematic at best. Very few, if any, manufacturers will support this effort.

Of course some applications, such as ground-based communication systems, are more benign and COTS components may be suitable for use without additional qualification or screening.

Compounding this problem are the short commercial product life cycles that are significantly shorter than military program life cycles. Many COTS products become obsolete before the military program ramps to volume production. With military systems being fielded for 10, 20, or even 50 years, as in the case of the B52 bomber, maintainability and spares become a logistic nightmare.

Example SN74HC138DR SN74HC138DR Assembly Baseline

- **Multiple assembly/test sites**
  - TI Mexico
  - TI Taiwan
  - ALP (subcontractor) in Thailand
- **Each assembly site runs a different baseline**
  - Lead-frame source and geometries
  - Mold compound (encapsulant)
  - Mount Compound (die attach)
  - Wire bonder type and profile
  - Injection mold press type and profile

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Example SN74HC138DR SN74HC138DR Assembly Baseline

Multiple combinations are possible

1. TI Mexico Assembly / SFAB Wafer Fabrication
2. TI Mexico Assembly / ATC Wafer Fabrication
3. TI Mexico Assembly / ASMC Wafer Fabrication
4. TI Taiwan Assembly / SFAB Wafer Fabrication
5. TI Taiwan Assembly / ATC Wafer Fabrication
6. TI Taiwan Assembly / ASMC Wafer Fabrication
7. ALP Assembly / SFAB Wafer Fabrication
8. ALP Assembly / ATC Wafer Fabrication
9. ALP Assembly / ASMC Wafer Fabrication

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High Temperature and Harsh Environments

Downhole
- Drilling
- Logging
- Well monitoring

Avionics
- Jet Engines
- Brakes

Automotive
- Engine compartments
- Brakes

Geothermal
- Drilling
- Well monitoring

Heavy Industrial
- Chemical Processing
- Sensors
- Actuation/Control

Medical
- Autoclave
- Sterilization

Undersea Cabling
- Ceramic
- QML-V like

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High Temp (HT) Roadmap

• Interface		
• SN65HVD233-HT	3.3V CAN Transceiver with Standby Mode, Loop-back	Released
• SN65HVD11-HT	3.3V Differential Transceiver	Released
• Data Converters		
• ADS1278-HT	Octal, 128kHz, Simult. Sampling 24-Bit Delta Sigma	Released
• ADS1282-HT	High Resolution Delta Sigma ADC with PGA	4Q2009
• ADS1243-HT	Low-Noise 24-bit ADC	
• ADS8320-HT	16-Bit, High-Speed, microPower Sampling ADC	
• Power		
• TPS76901-HT	Single Output LDO, 100mA, Adjustable	Released
• TPS62000-HT	Adjustable, 600-mA, 95% Efficient Step-Down Converter	Released
• TPS62110-HT	Adjustable, 1.5-A, 17-V Vin Step-Down Converter	1Q2010
• TPS40200-HT	Wide Input Nonsynchronous Buck DC/DC Controller	4Q2009
• TPS40210-HT	4.5 to 52V Input Current Mode Boost Controller	1H2010
• TPS54362-HT	3A, 60V step down DC/DC converter with low Iq	
• Reference		
• REF5025-HT	Low Noise, Very Low Drift, Precision Voltage Reference	Released
• Amplifiers		
• OPA2333-HT	1.8V, 17uA, 2uV, microPOWER CMOS Op Amp	Released
• OPA211-HT	1.1nV/rtHz Noise, Low Power, Precision Op Amp	Released
• OPA129-HT	Ultra-Low Bias Current Difet Operational Amplifier	1H2010
• INA117-HT	High Common-Mode Voltage Difference Amplifier	1H2010
• INA129-HT	Precision, Low Power Instrumentation Amplifiers	1H2010
• INA333-HT	Low Power, Single Supply Instrumentation Amp	1Q2010
• INA271-HT	Voltage Output High-Side Current Shunt Monitor	1H2010
• THS4524-HT	4 channel rail-to-rail output fully differential amplifier	
• Processors		
• TMS470R1B1M-HT	60 MHz ARM7 uController	Released
• SM320F2812-HT	32-Bit Motor Control DSP	Released
• SM320F28335-HT	32-Bit Floating Point Motor Control DSP	1H2010
• MSP430F2619-HT	16-Bit Ultra-Low-Power MCU (150C EP)	4Q2009
• OMAP-L137-HT	Low-Power Applications Processor (ARM9 + DSP)	1H2010

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175 High Temperature Plastic

- 175C plastic offerings of HT devices
- Standard commercial plastic footprints
- Baseline Control
  - One FAB, Assembly and Test Site
- Extended Temperature (-55C to +175C)
- Nickel-Palladium-Gold lead finishes are standard
- Extended Qualification
- Standard data sheet
  - Extended operating life chart in data sheet
  - 175C data
- Obsolescence Mitigation

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Summary

- Complete portfolio
- Quality and reliability
- Innovative solutions
- Commitment