TI solutions for ESD and EMI problems

Ankara Tech Day 2010

Abstract

TI solutions for ESD and EMI problems

- **ESD issues: explanation of the standard ESD (Electrostatic Discharge) test methods, including IEC61000-4-2, design recommendation and an overview of TI solutions in ESD +EMI filtering.**

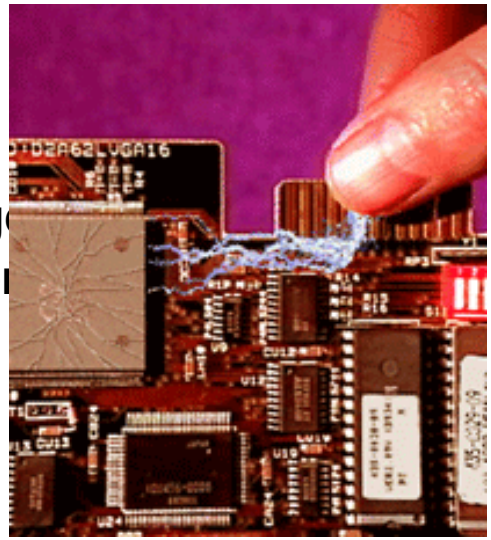
- **EMI issues are becoming the most common cause for redesign nowadays. The certification process of a new electronic device can take more time and money than expected if no EMI consideration was taken into account in the design phase. An early EMI approach of potential problems due to the clocks in your system can minimize the impact of this phenomenon.**

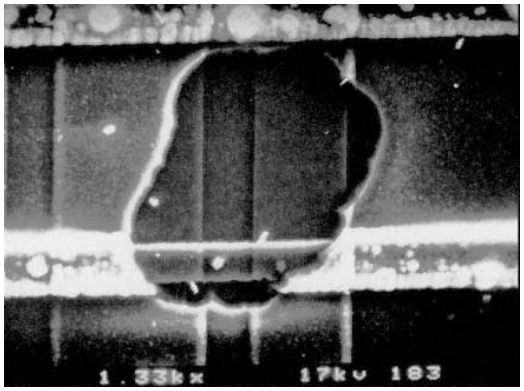
ESD fundamentals

- ESD stands for: **Electrostatic discharge.**
- Cause of ESD: **This occurs when an electrically charg object is placed near a conductive object isolated fro**
- **Type of ESD**: The most spectacular form of ESD is the spark, which occurs when a strong electric field creates an ionized conductive channel in air.

  This can cause minor discomfort to people, severe damage to electronic equipment, and fires and explosions if the air contains combustible gases or particles.

  Many ESD events occur without a visible or audible spark. A person carrying a relatively small electric charge may not feel a discharge that is sufficient to damage sensitive electronic components.
- **ESD industry standard testing:** IEC 61000-4-2

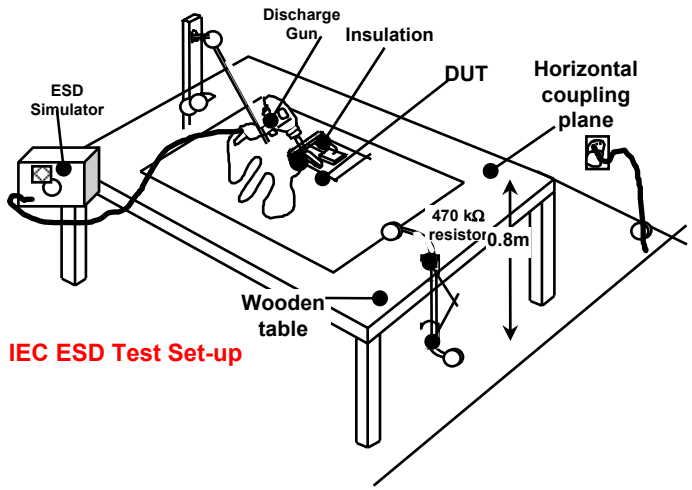




ESD damage to an IC. A “punch through” effect has occurred which exposes lower layers of a circuit.

IEC 61000-4-2: What is it?

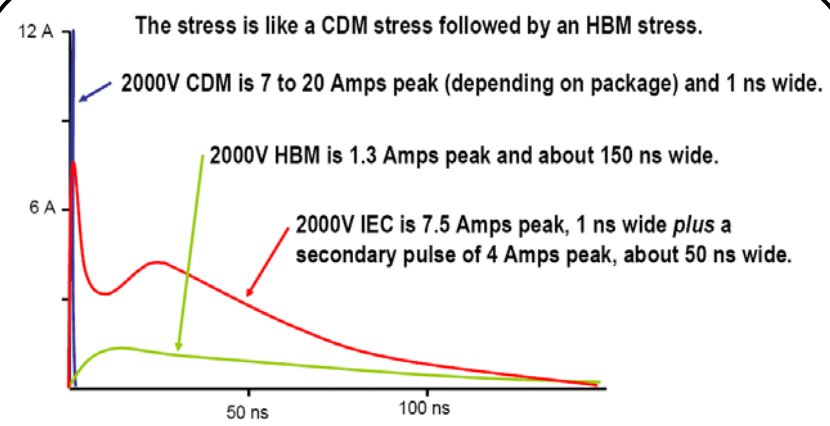
How Does it Differ from HBM*, CDM, MM***?**



IEC ESD Test Set-up

Level	Contact discharge (±KV)	Air discharge (±KV)
1	2	2
2	4	4
3	6	8
4	8	15

Different IEC 6100-4-2 ESD Levels



Comparison is shown with 2kV ESD stress for all the three cases)

HBM, CDM, & MM address device protection requirements during board assembly, part handling.

The IEC ESD specifications address the ESD immunity in 'real world' environment:

- IEC is a system level ESD specifications
- The system is zapped with ESD strike while the device is operating
- IEC is a more stringent ESD requirement compared to HBM, CDM!

*HBM: Human Body Model; **CDM: Contact Discharge model; ***MM: Machine Model

TI Integrated Protection Device

TPD Devices: www.ti.com/interface

TPD xx T nnn PPP

TPD = **TI Protection Device**

xx = **No of Channels**

12 = Twelve Channel
4 = Four Channel

T = **Protection Device Type**

E = ESD Only
F = ESD+EMI
S = Custom ESD (HDMI, DVI etc.)

nnn = **Part Number**

000-999
(depends on feature, parameters)

PPP = **Package Name**

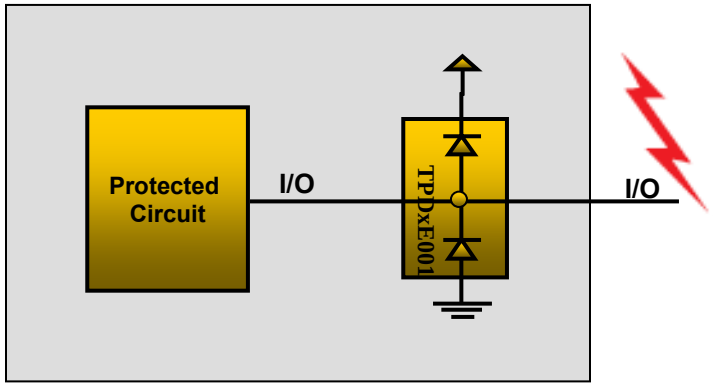
Ex1: TPD**4E**001YFPR: Four Channel ESD
Ex2: TPD**2F**701RSER: Two Channel EMI Filter

TPD2E001, TPD3E001, TPD4E001, TPD6E001

Dual, Triple, Quad, & Hex ESD Array for USB High-speed Applications

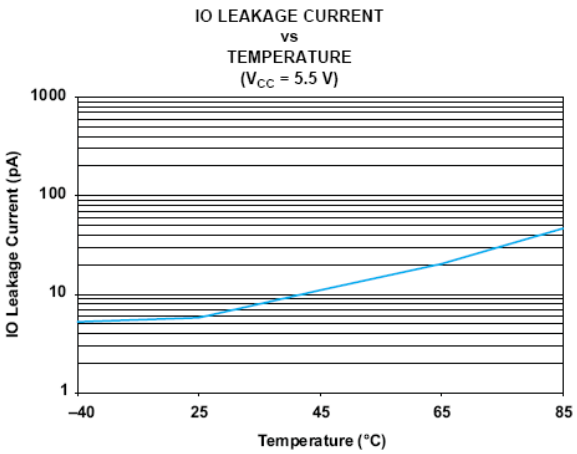
Key Performance Parameters

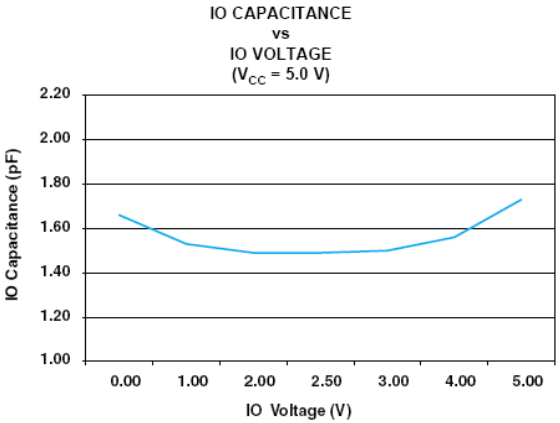
- System level ESD protection for high speed application:
  - ± 8kV—IEC 61000-4-2, Contact Discharge
  - ± 15kV—IEC 61000-4-2, Air-Gap Discharge
- Less than 1.5pF IO pin capacitance
- Ultra low 1pA leakage current
- Operating supply voltage range: +0.9V to +5.5V
- Space saving package solutions: DRY, DRL, DRS, & RSF

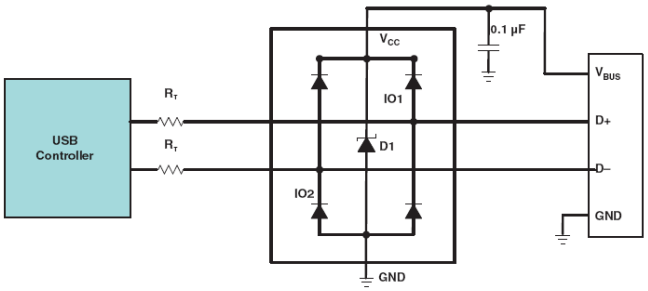


TPDxE001 Application Schematics

TYPICAL OPERATING CHARACTERISTICS

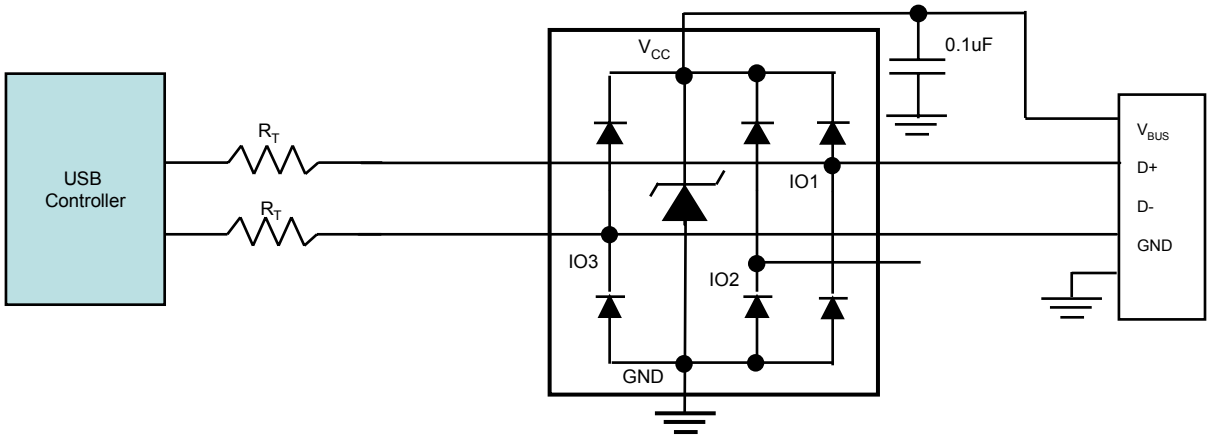




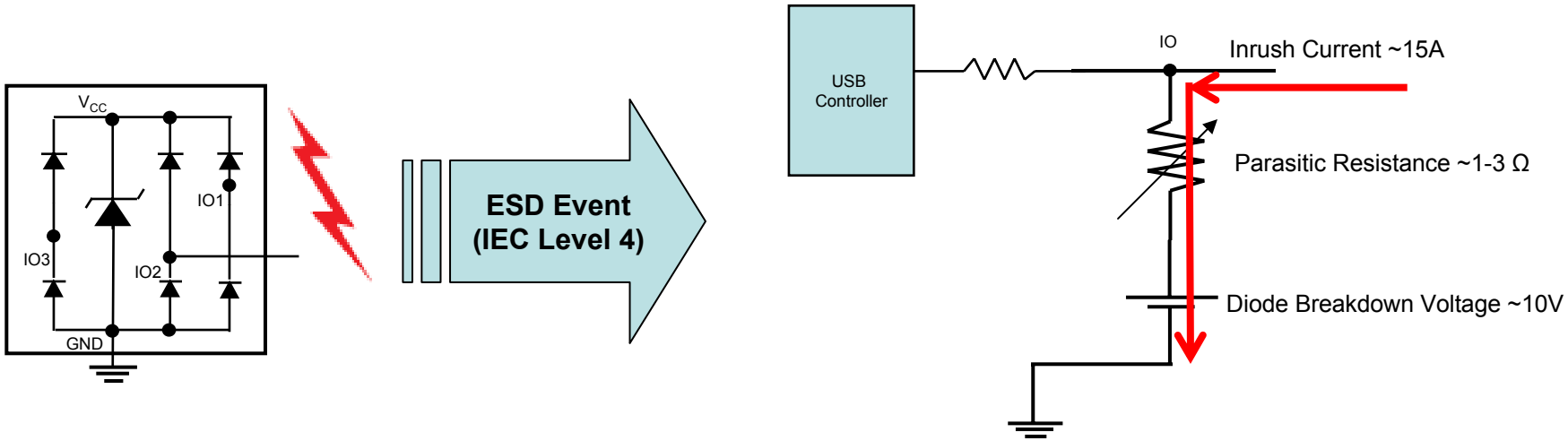


TPD2E001 Data

ESD Event: The Clamp Voltage



TPD3E001 in USB2.0 (480Mbps) Application



ESD Event: Equivalent Circuit Representation

TPDXE001 lay-out tips

1. Place the **TPDxE001** solution **close to the connector** allowing the TPDxE001 device to dissipate the energy associated with ESD strike before it reaches internal circuitry of the system board.

2. Place a **0.1uF** capacitor **very close to the VCC pin** - will help limit any momentary voltage surge at the IO pin during the ESD strike event

3. Make sure that **there is adequate metallization for the VCC and GND loop**. During normal operation, the TPDxE001 will operate in the nA leakage current range; but, during an ESD event the device may see 15-30 amps of current depending on the ESD level. Adequate metallization in current path will enable safe discharge of all the energy associated with the ESD strike

4. Leave the unused IO pins floating

   - The VCC pin can be connected in two different ways:

   - If the VCC pin is connected to the system power supply, the TPDxE001 works as a transient suppressor for any signal swing above VCC + VF. A 0.1uF capacitor on the device VCC pin is recommended for ESD bypass

5. If the VCC pin is not connected to the system power supply, the TPDxE001 can tolerate higher signal swing in the range up to VBR. Please note that a 0.1uF capacitor is still recommended at the VCC pin for ESD bypass.

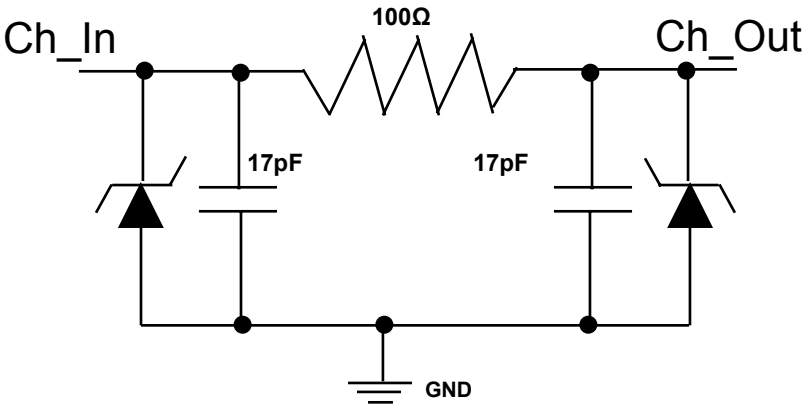
Sample Now

TPD6F002

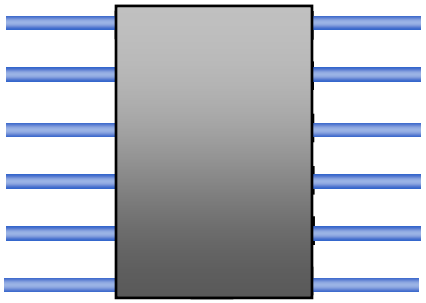
6-Channel EMI Filter for LCD Display Port

Key Performance Parameters

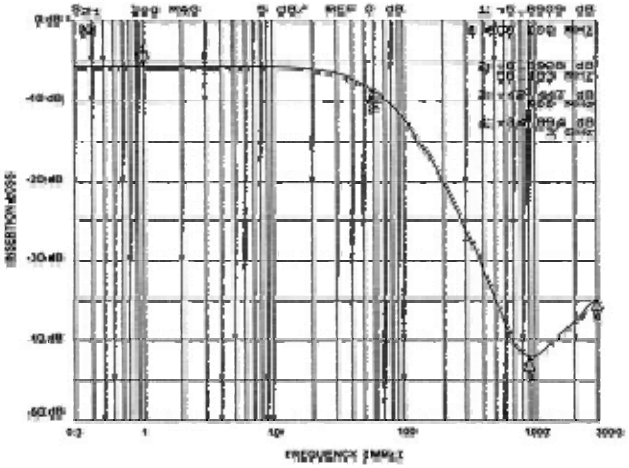
- Six Channel EMI Filtering for Data Ports
- Greater than 32dB attenuation at 1GHz
- R-C Topology (R=100Ohm, C=17pF)
- System level ESD protection for high speed application:
  - ✓ ± 15kV—Human Body Model
  - ✓ ± 8kV—IEC 61000-4-2, Contact Discharge
  - ✓ ± 15kV—IEC 61000-4-2, Air-Gap Discharge
- Operating IO Voltage Range up to 5.5V
- Space saving package solutions



Schematic Representation

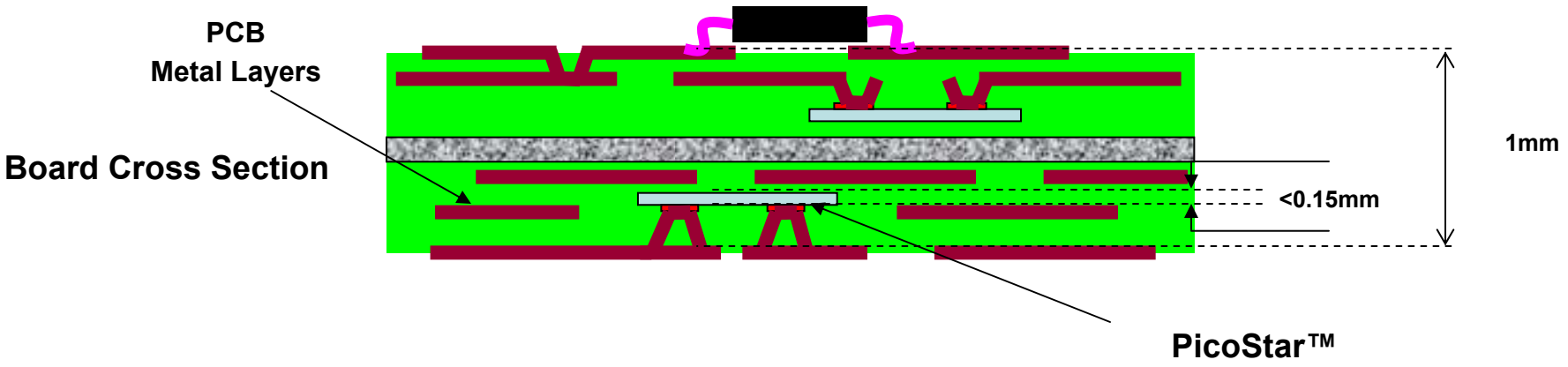


3.0-mm × 1.35-mm DSV Package

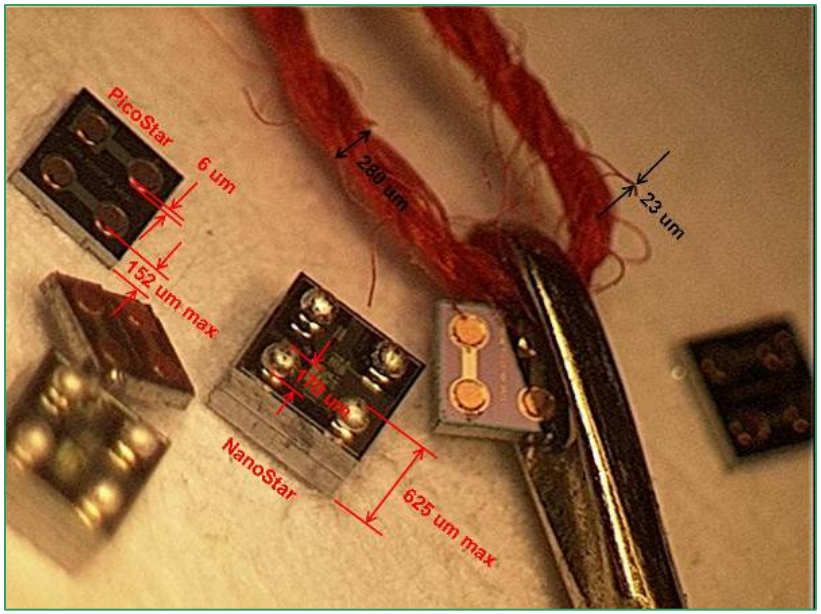


Insertion-loss versus Frequency

PicoStar™ the latest technology: A package that can be embedded in a PCB



0.8mm * 0.8mm * 0.15mm



ESD / EMI Protection Devices

BP	SP	BV	
	✓	✓	**Multi-channel ESD Protection**
	✓		**TPD2E001**: 2-Channel, 1.5pF I/O Cap, 1nA Leakage
			TPD3E001: 3-Channel, 1.5pF I/O Cap, 1nA Leakage
			TPD4E001: 4-Channel, 1.5pF I/O Cap, 1nA Leakage — 1394
			TPD6E001: 6-Channel, 1.5pF I/O Cap, 1nA Leakage
		✓	**TPD4E002**: 4-Channel, 11pF I/O Cap, ±15kV Contact ESD
	✓		**TPD4E004**: 4-Channel, 1.6pF I/O Cap, 6V DC Breakdown — 1394
			TPD6E004: 6-Channel, 1.6pF I/O Cap, 6V DC Breakdown
	✓		**TPD2E007**: 2-Channel, 11pF I/O Cap, PicoStar™ Package
✓	✓		**TPD2E009**: 2-Channel, 0.7pF I/O Cap, >3GHz Bandwidth — 1394
		✓	**Multi-channel ESD+EMI Protection**
		✓	**TPD6F002**: 6-Channel EMI Filter, C_{TOTAL} = 34pF, R = 100Ω
			TPD6F003: 6-Channel EMI Filter, C_{TOTAL} = 19pF, R = 100Ω
	✓		**Custom ESD Protection**
			SN65220: Single-Port USB 2.0 Full-Speed Protection
			SN65240: Dual-Port USB 2.0 Full-Speed Protection
			SN75240: Dual-Port USB 2.0 Full-Speed Protection
✓	✓	✓	**TPD4S009**: 4-Channel ESD Solution for HS Differential Signals
✓			**TPD8S009**: 8-Channel ESD Solution for HDMI / DisplayPort
✓	✓		**TPD4S012**: 4-Channel USB ESD Solution with Power Clamp
			TPD12S520: 12-Channel ESD Solution for HDMI Receiver Port
			TPD12S521: 12-Channel ESD Solution for HDMI Transmitter Port

EMI

- Definitions
- Elements involved
  - Source
  - Coupling
  - Victim
- Signal Integrity
- Layout techniques to reduce EMI
- TI solutions for EMI Reduction:
  - SSC
  - Slew Rate Control

Definitions

EMC – Electromagnetic Compatibility

- It is the capacity of a system, electric or electronic device to work as designed in an electromagnetic area for the one it was designed

- It is EMC compatible when
  - Does not produce interference with other systems
  - Does not suffer from perturbations from another system
  - Does not produce interferences to itself

Definitions

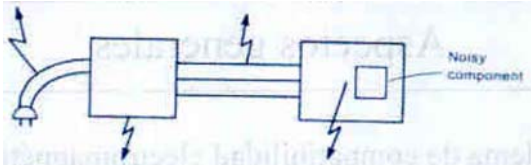
EMI – Electromagnetic Interference

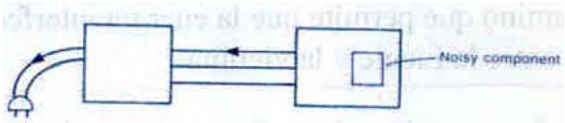
- Every electromagnetic influence of a system, disturbing or disrupting this systems function, is called ElectroMagnetic Interference (EMI)

- There are two different types of EMI:
  - Conducted EMI: unwanted coupling through parasitic inductance, power and ground connections
  - Radiated EMI: unwanted coupling between components through electromagnetic transmition

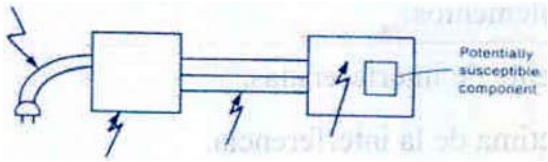
General Aspects

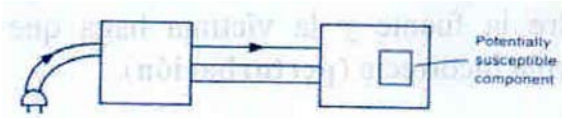
- **Emission:**
  - **Radiated**
  - **Conducted**





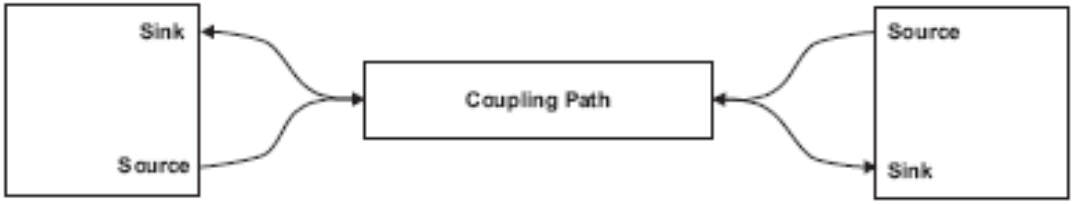
- **Immunity:**
  - **Radiated**
  - **Conducted**





EMI Elements

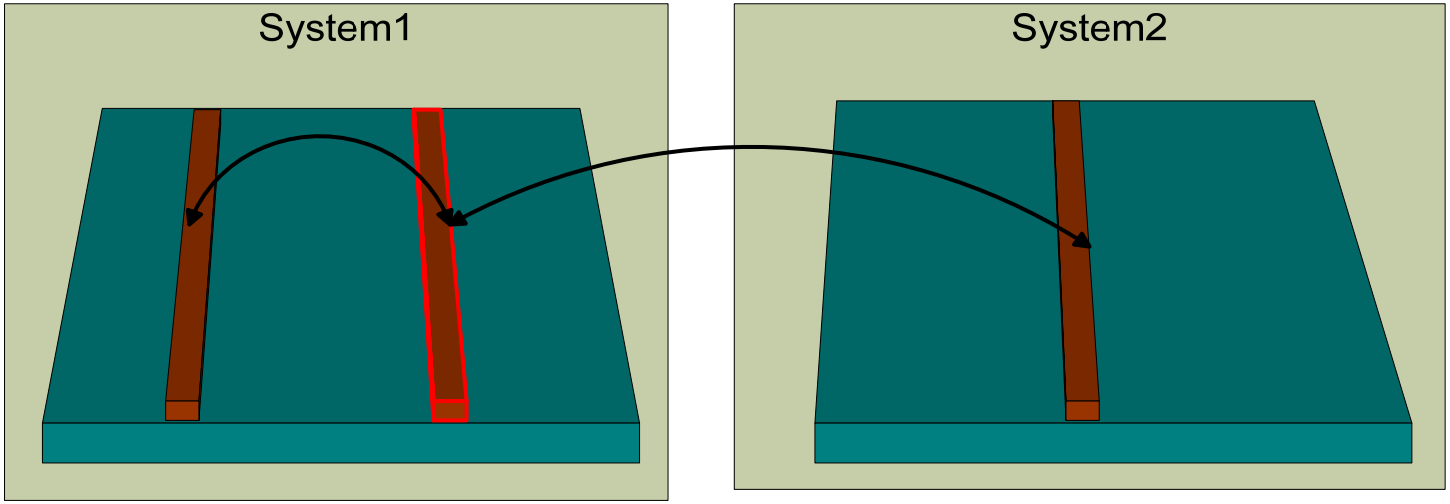
- **Source** of the interference
  - Reduce the perturbation of the source
- **Victim** of the interference
  - Make victim as robust as possible
- **Coupling Path** that allows to interfere the energy of the source with the victim



EMI Source – Coupling - Victim

- An electromagnetic wave, traveling on a line, can radiate part of its energy in the surroundings, depending on the mix of frequency, material and layout

- The wave is loosing energy and somewhere the victim is receiving this energy

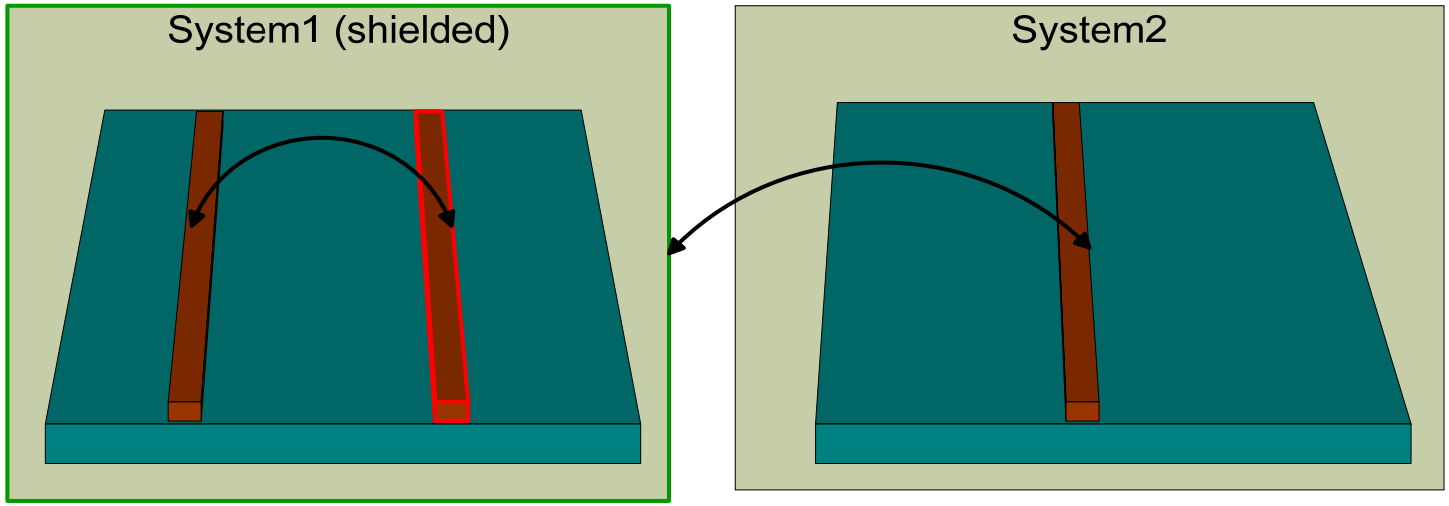


Shielding

- Shielding uses electromagnetic conductible material to “wrap” a system completely

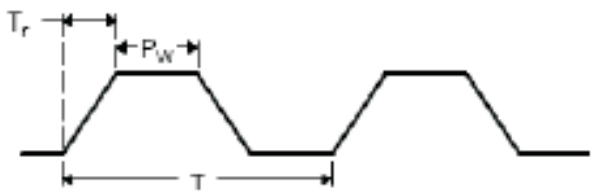
- By this electromagnetic energy will be kept inside the system and it gets harder for a external signal to cause EMI inside the system

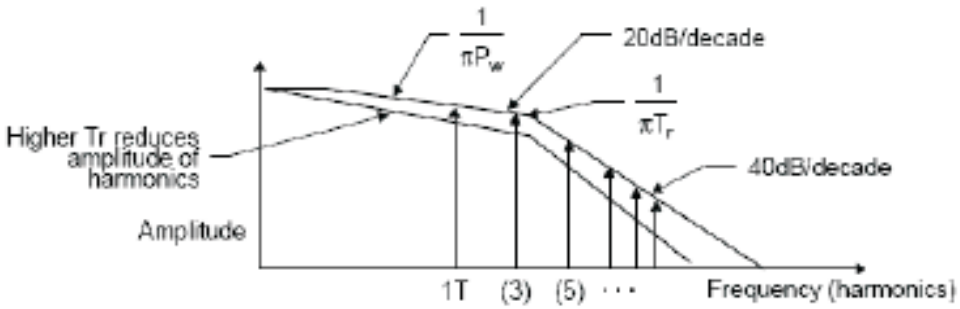
- Easy to use
- Can be heavy and expensive
- Does not help if an EMI source within the system is present



Clocks and EMI

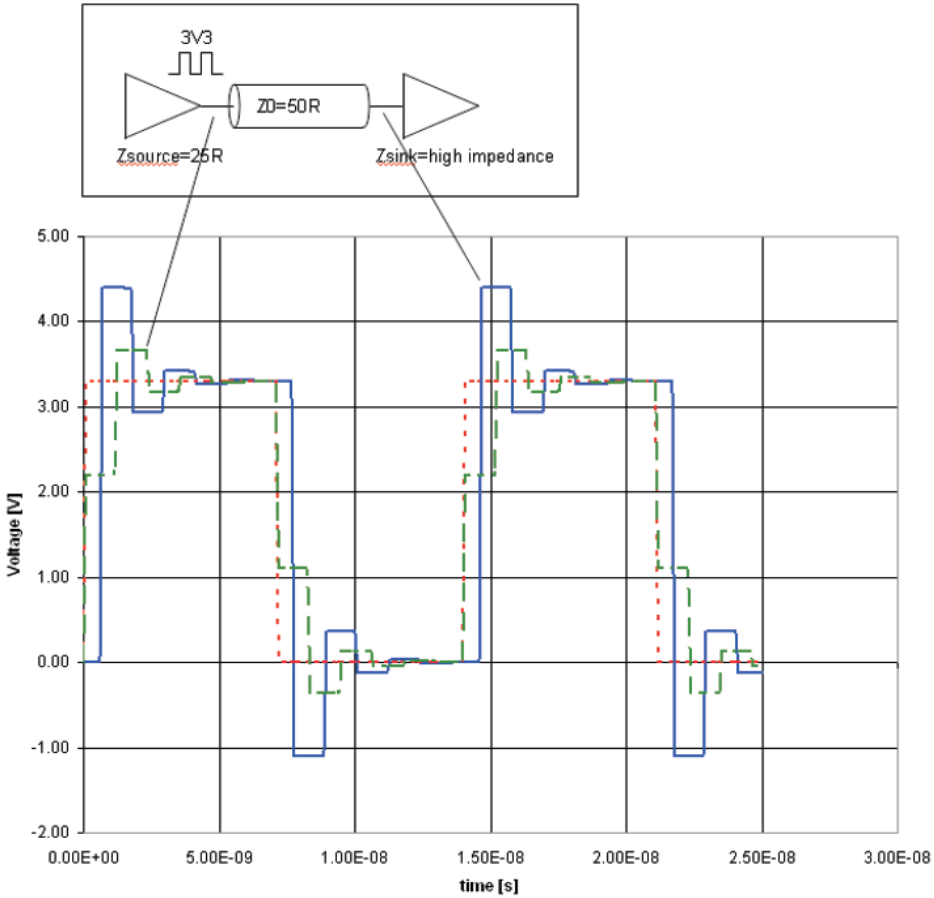
- Ideal Clocks have short rise and fall times to avoid Duty Cycle Distortion and other problems
- For good rise and fall times a greater number of odd harmonics is necessary
- Even low frequency clocks can have components that can cause high frequency EMI

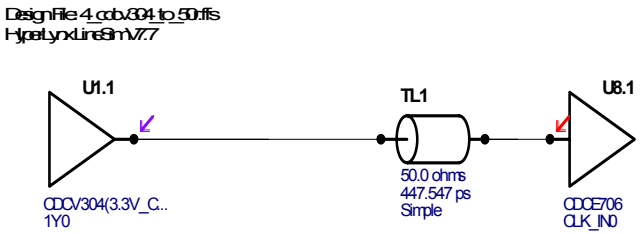


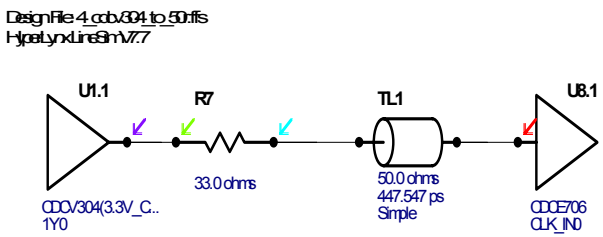


Reflections

- **Problems associated with the reflections**

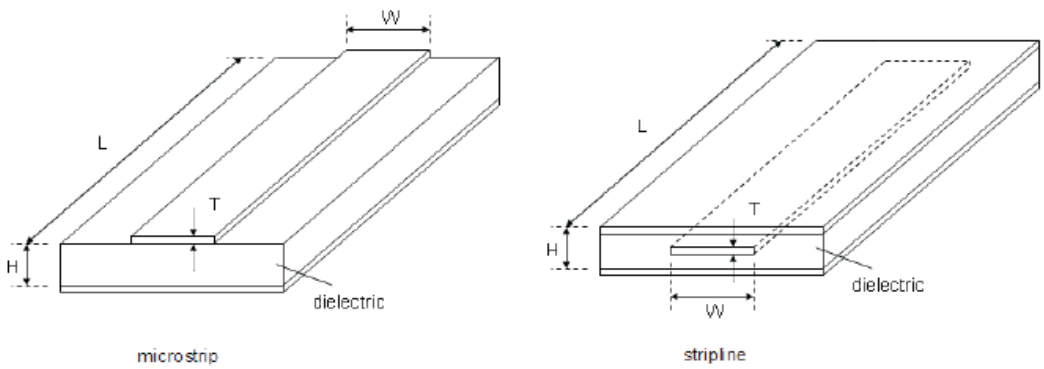






Transmission lines

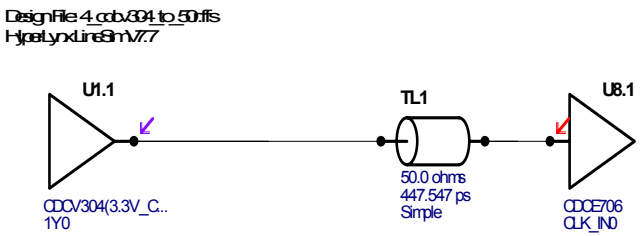
- If the length of traces are in the range of the signal's wavelength, then the user has to consider the effects of transmission lines.
- Formulas are complex and software tools can help to determine the characteristic impedance of the tracks.

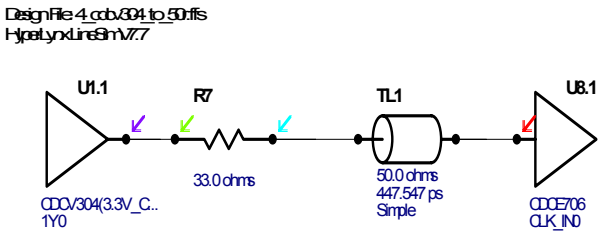


Transmission Lines

- **Reflections are due to changes of the characteristic impedance**
- **The reflection coefficient is the dimension witch expresses the relationship between the impedance of the transmission line and the impedance of the source or sink**

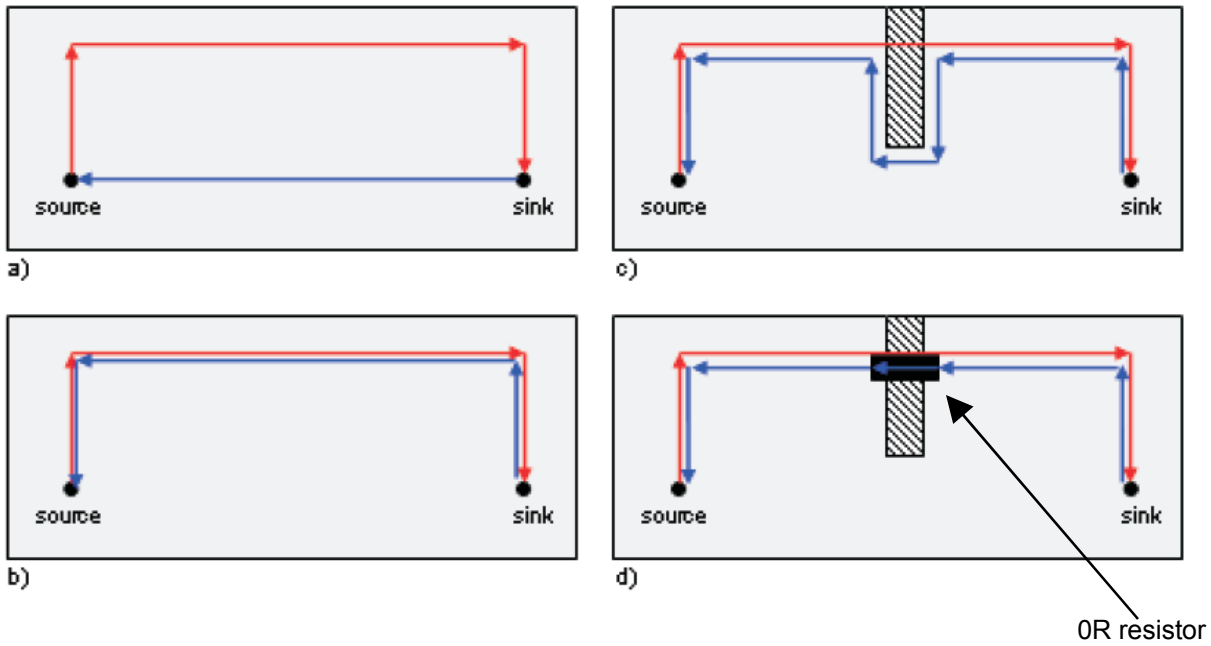
$$\rho = \frac{R - Z_0}{R + Z_0}$$





Return currents and loop areas

- **An electrical circuit must always be a closed loop**



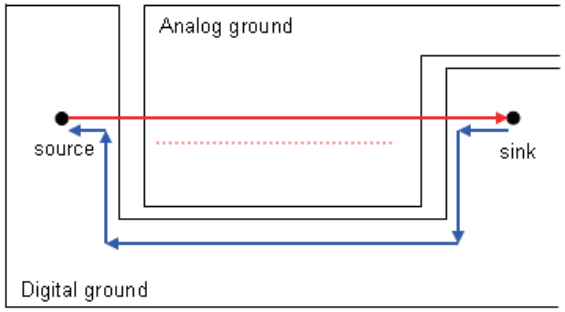
Layout considerations

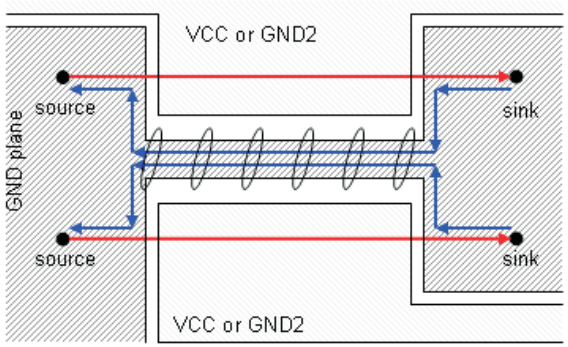
- Define the location of each section on the board by means of the functional diagram. Try to keep the devices together to avoid interaction (crosstalk, influence of noise) between two separate blocks (like transmitter–receiver or analog–digital).
- At which functional block is which supply voltage used?
- It is necessary in high-speed designs to have at least one complete ground plane as a reference for microstrip traces for sensitive signals.
- With a complete power plane as close as possible to the ground plane, it is possible to create capacitive coupling between them to get low impedance at high frequencies. This reduces the amount on small decoupling capacitors at the power pins of the devices. The closer the planes, the less impedance is present

Power and Ground Planes

- **Ground plane in high-speed design is ESSENTIAL**

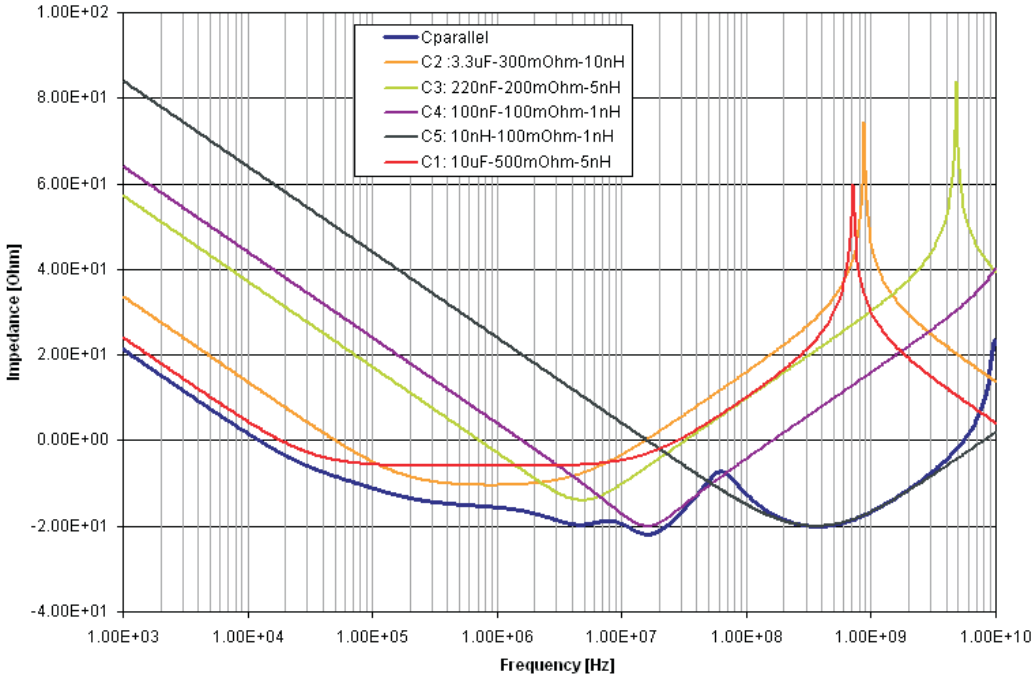
- **Special considerations:**
- Split ground planes act as slot antennas and radiate.
- A routed trace over a gap creates large loop areas, because the return current cannot flow beside the signal, and the signal can induce noise into the nonrelated reference plane.
- With a proper signal routing, crosstalk also can arise in the return current path due to discontinuities in the ground plane. Always take care of the return current





Decoupling capacitors

- **Ensure low ac impedance to reduce noise and to store energy**
- **To reach low impedance over a wide frequency range, several capacitors must be used**



Capacitor placement

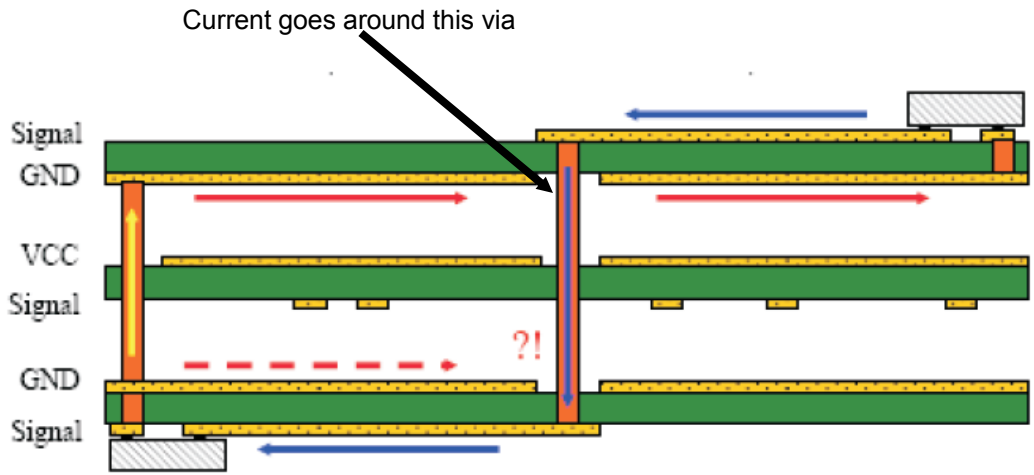
- Place the lowest valued capacitor as close as possible to the device to minimize the inductive influence of the trace. This is especially important for small capacitor values, because the inductive influence of the trace is not negligible anymore.
- Place the lowest valued capacitor as close as possible to the power pin/power trace of the device.
- Connect the pad of the capacitor directly with a via to the ground plane. Use two or three vias to get a low-impedance connection to ground. If the distance to the ground pin of the device is short enough, you can connect it directly.
- Make sure that the signal must flow along the capacitor.

Traces and Vias

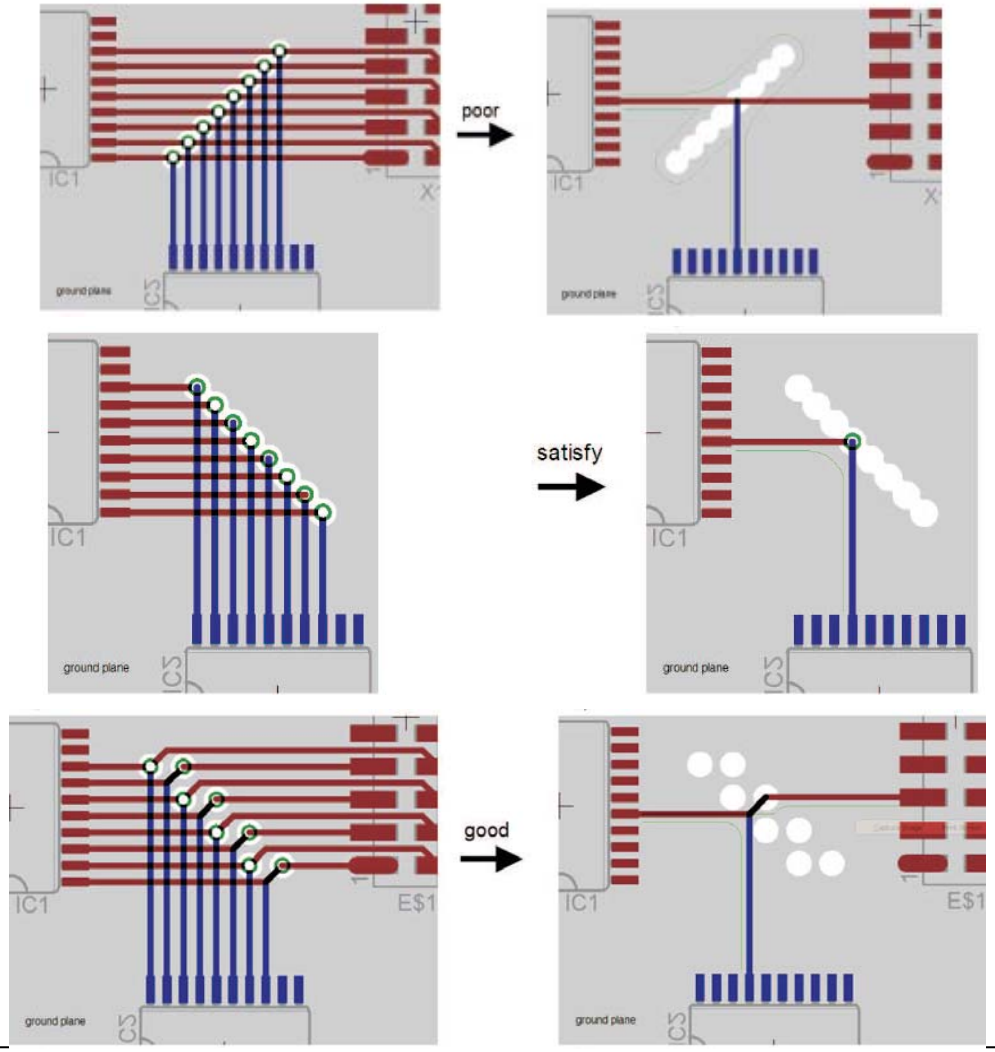
- Avoid right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing would be a round bend.
- Separate high-speed signals (e.g., clock signals) from low-speed signals and digital from analog signals; again, placement is important.
- To minimize crosstalk not only between two signals on one layer but also between adjacent layers, route them with 90° to each other.
- Avoid vias in differential signals

Loop Areas

- **Loop Areas Caused by poor via placement**

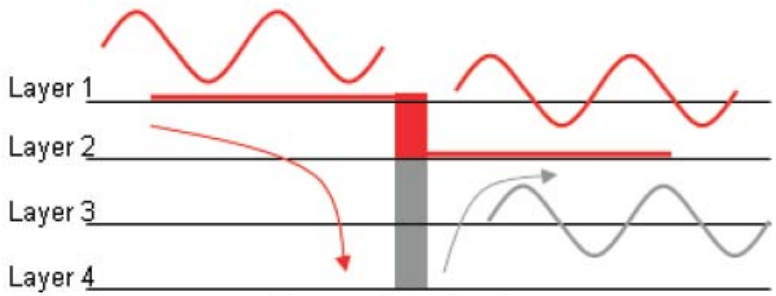


Practical Examples



Practical Examples

- **Reflection Caused by Stubs in a Via**



Open end -> reflection

Tips for traces and vias

- Do **not use right-angle** bends on traces with controlled impedance and fast rise time, respectively.
- Route the traces **orthogonally** to each other on adjacent layers to avoid coupling.
- To minimize crosstalk, the distance between two traces should be approximately **2 to 3 times the width** of the trace.
- **Differential traces should be routed as close** as possible to get a high coupling factor. As a result of this, influenced noise is then a common-mode noise and is not a problem for a differential input stage.
- Do **not use vias** on traces with sensitive signals, if unnecessary.
- Be careful with the return current when changing the layers. Use **ground vias around the signal via** to make sure that the return current can flow as close as possible to the signal.
- Do **not create slots**, for example in the ground plane, by using closely placed vias.

Clock distribution

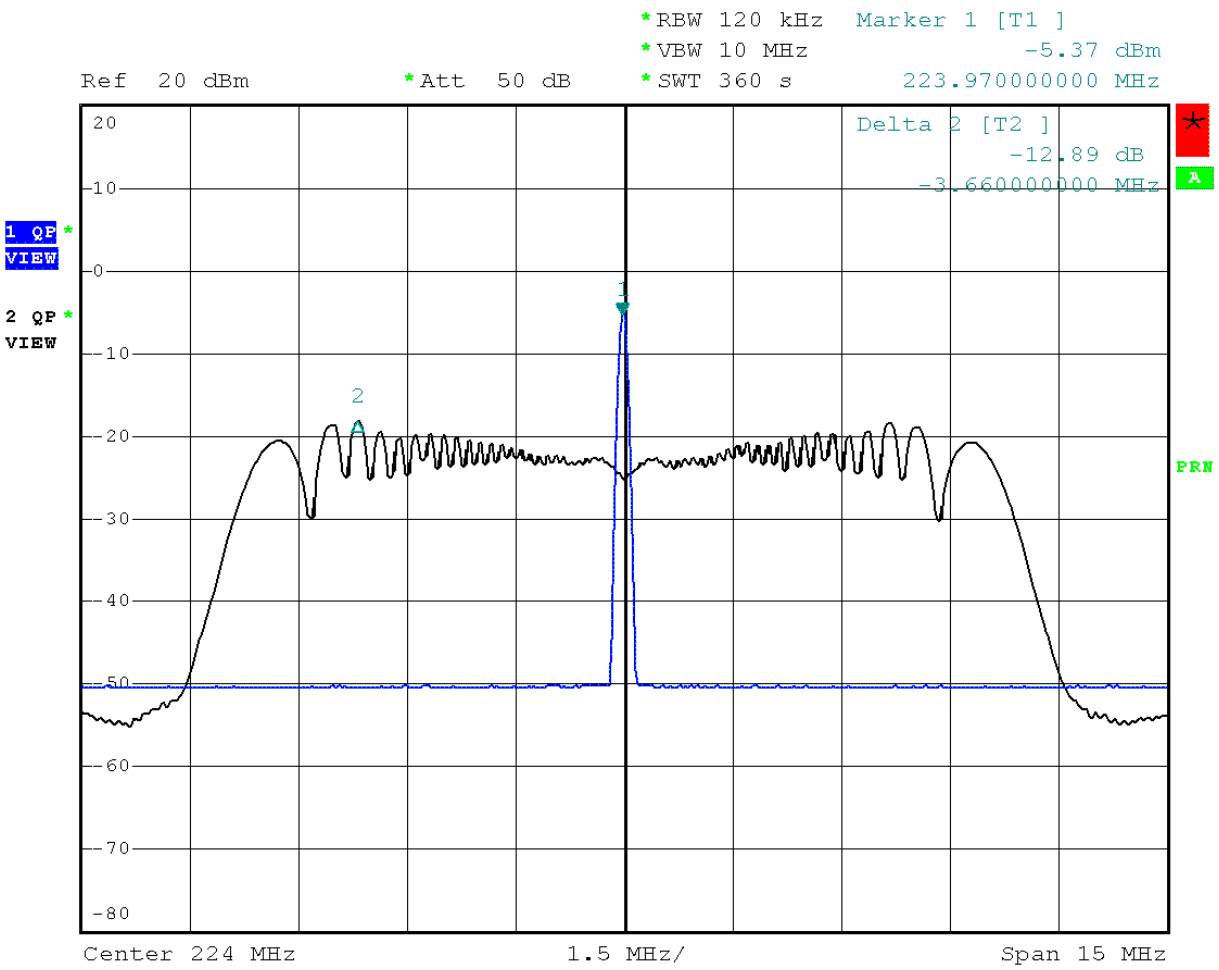
- Consider the delay for each trace. The best solution is to route these signals with the same length.
- Avoid branches to reduce reflections.
- Use a clock driver to distribute the signal to every device and consider a proper termination.

Practical Examples

SSC

- SSC is a way to reduce the emitted energy from a signal
- It simply distributes energy from a single frequency to a frequency band near the original frequency
- If now a part of the signal is emitted, the radiated energy is significantly less
- A welcome side effect is that only a part of the original signal is loosing energy and therefore also most of the original signal is still available

CDCS502 – 7th Harmonic



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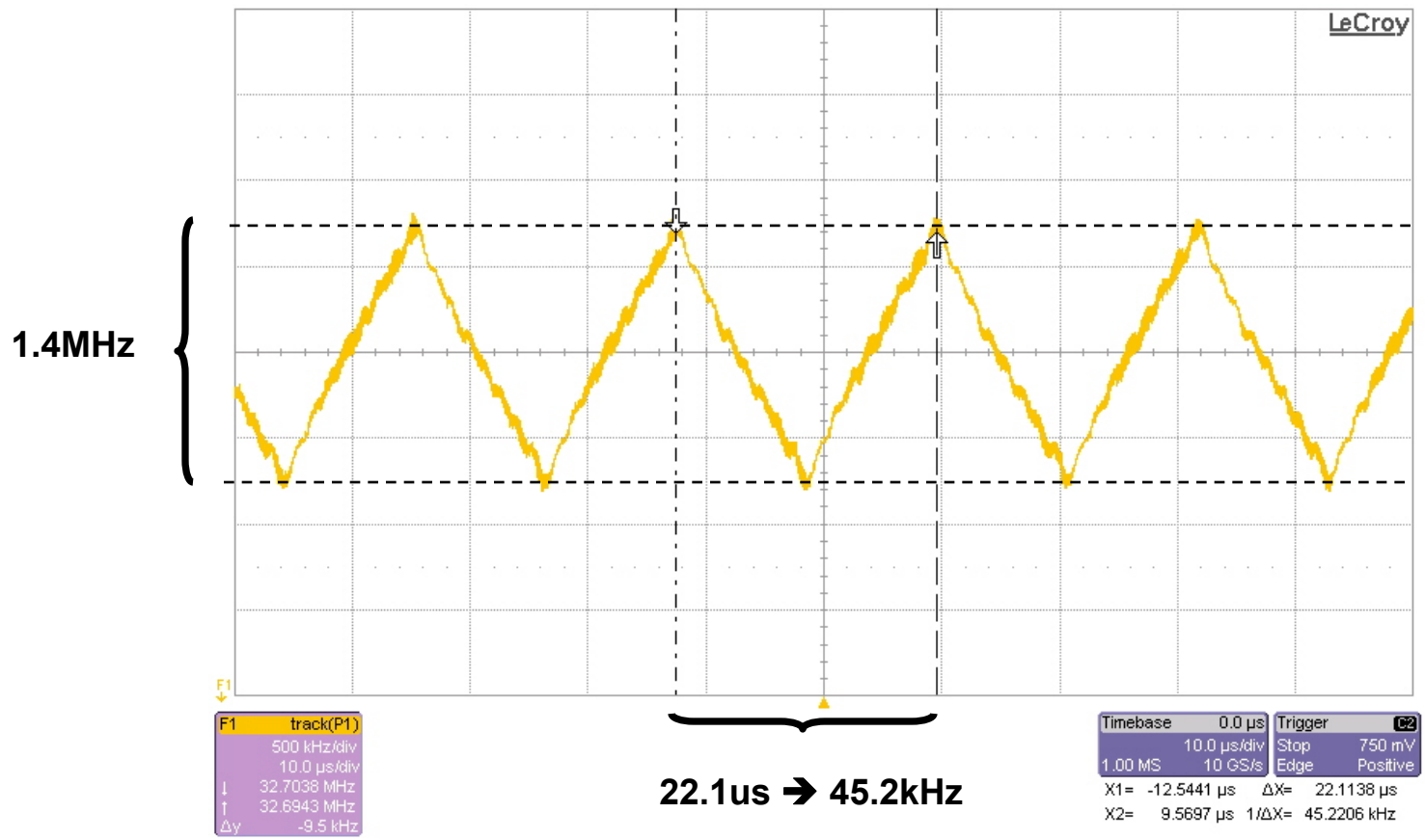
SSC time domain

- **Frequency vs cycles**



CDCS502 jitter x1

- **Fin = 25MHz crystal**
- **Fout = 25MHz**

SSC amount	Cycle – Cycle Jitter (ps)	Period pk-pk Jitter (ps)
0%	36	41
±0.5	93	512
±1	117	1001
±2	195	1990

CDCS502 jitter x4

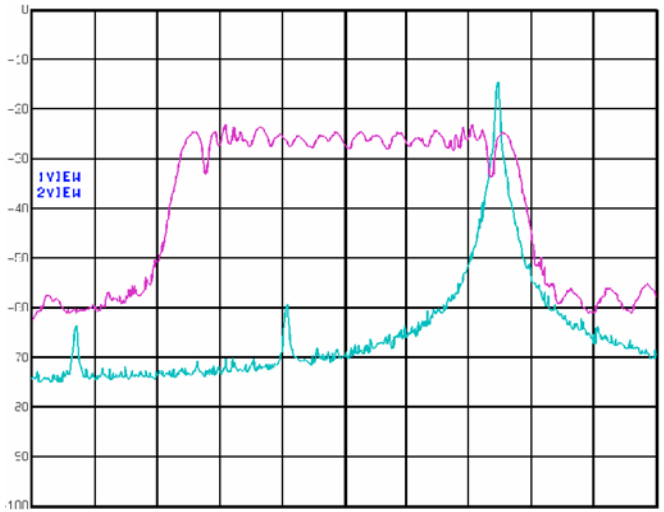
- **Fin = 25MHz crystal**
- **Fout = 125MHz**

SSC amount	Cycle – Cycle Jitter (ps)	Period pk-pk Jitter (ps)
0%	36	41
±0.5	72	178
±1	72	292
±2	78	529

Different methods of SSC

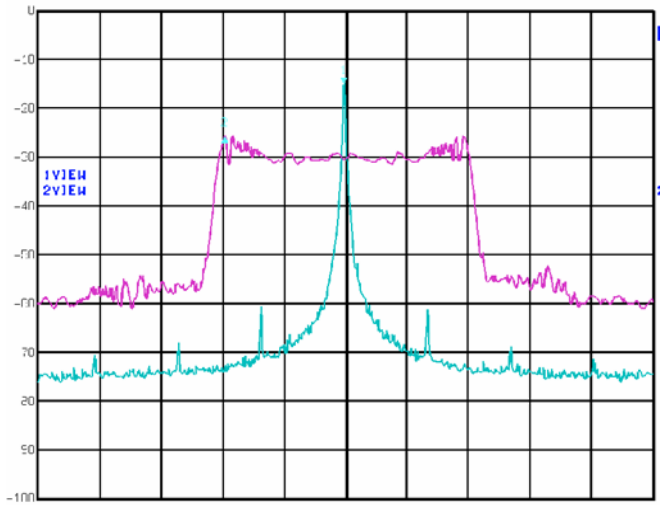
Downspread:

Highest frequency is the one that is programmed into the device



Centerspread:

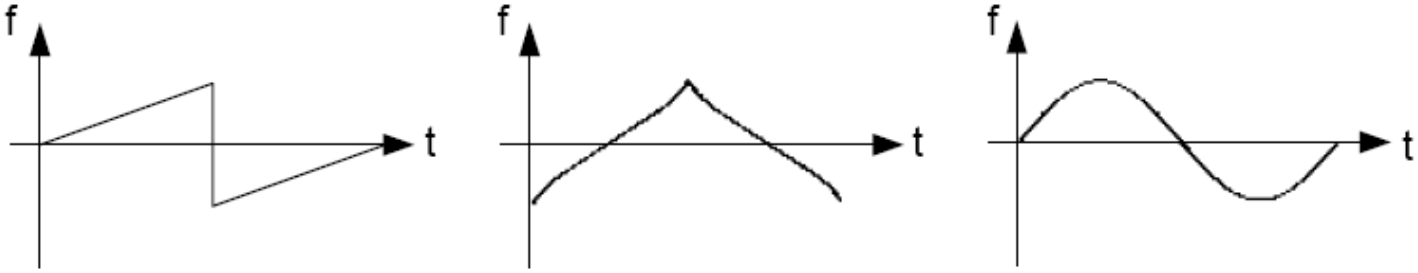
Frequencies are distributed around the desired clock frequency



Important SSC Parameters

- **Spread frequency**
  - Is the frequency the signal gets changed with
  - If too low, its modulation products can interfere with audio frequencies
  - If too high, the follow on system might be influenced (e.g. added jitter, loss of functionality)

- **Spread function**
  - To allow for a even frequency distribution of the spreaded signal, one has to use a special function to sweep through the spread frequency range (see figure below)
  - The best sweep function is called “Hershey Kiss” Profile
  - Since this profile is hard to create, in a lot of designs a triangular profile is used
  - Triangular shape does not create a completely even frequency spectrum, the frequencies at the “end” of the spread are more dominant



sawtooth shape hershey shape sinusoidal shape

SSC and EMI Standards

- The EMI guidelines defining the Spectrum Analyzer settings
  - Amongst others: Filter bandwidth, video bandwidth and detector type
- Since these settings can be close to the commonly used SSC modulation frequency's, a small change in the way the SSC is done can show a different result in the Spectrum Analyzer
- So even two devices with the same amount of spread can appear different in EMI measurements

SSC

- SSC is an easy and cheap way to reduce EMI
- If a clocking device is used that can switch SSC on and off it can even be applied after the system design is done and therefore can safe time and money
- It does not require RF knowledge
- Cheap compared with shielding and special layout needs

Can I use SSC in my application?

- What kind of jitter is critical in my application?

- Cycle-to-cycle
- Period jitter
- RMS
- Phase jitter

Example

- My Microprocessor specs cycle-to-cycle max of 500ps. Can I use the SSC (CDCS502)?
- My Microprocessor specs 50ps peak-peak. Is SSC an option?
- PCIe accepts -0.5% down spread.

TI Solutions

- **CDCS50X Family: EMI expert**
- **CDCE(L)913/925/937/949: Programmable SSC**
- **CDCE906/CDCE706 : Programmable SSC and Slew Rate control outputs**

CDCE(L)949

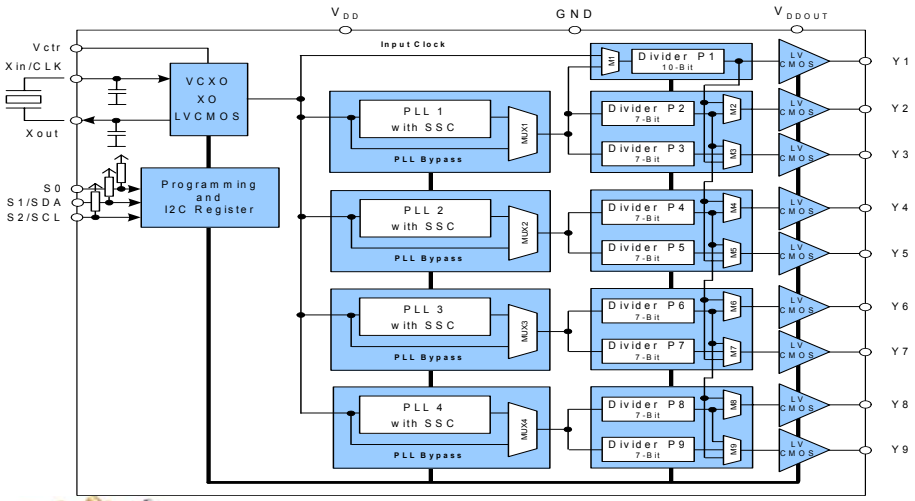
1.8 V Programmable VCXO 4-PLL Clock Synthesizer with 3.3V/2.5V/1.8V I/Os

Features

- Input Clock: LVCMOS (160 MHz) and Crystal (8- 32MHz)
- VCXO input with ±150ppm (typ) pulling range
- Output frequencies up to 230 MHz @ 1.8V, 2.5V and 3.3V
- 9 low-jitter, low-skew high-performance outputs
- Three user-definable control inputs
- Spread-Spectrum Clocking
- On-chip EEPROM
- 1.8V supply voltage, 3.3V or 2.5V I/O for CDCE949 and 1.8V I/O for CDCEL949

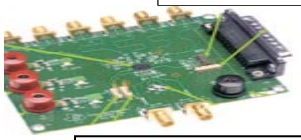
Benefits

- Wide I/O frequency range supports wide frequency ratio for Audio/Video clocking
- Enables Zero PPM clocking generation
- Supports frequency scaling and power saving
- Reduce EMI noise
- Easy to customize by EEPROM-Lock
- 1.8V ready – low power consumption
- 24 Pin TSSOP



Applications

- Digital Media Systems (Audio/Video)
- DSP, DaVinci and OMAP Attached
- IP-STB/TV/Phone
- Streaming Media (i.e. DVD-P/R)
- Automotive Entertainment
- Portable Media
- Print Media



CDCE949EVM

TI Proprietary Information - NDA Protected Material

Texas Instruments

CDCS502 / 503

Spread Spectrum Clock Driver/Multiplier

Features

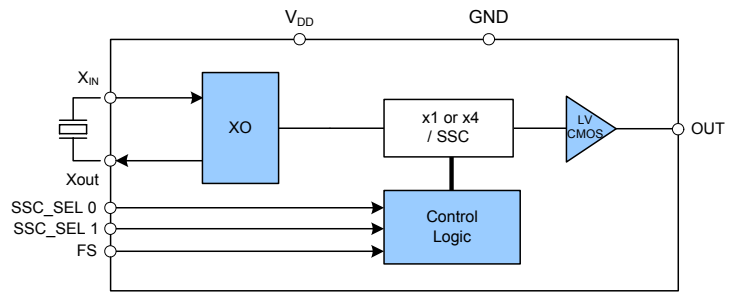
- Member of a family of easy-to-use clock generator with optional SSC.
- Selectable spread-spectrum modulation of ±0.5%, ±1.0%, and ±2.0% center spread
- Crystal (CDCS502) or LVCMOS(CDCS503) input from 8MHz to 32MHz; Generate frequency from 8MHz to 108MHz
- Selectable frequency multiplication rates of 1x and 4x
- Single 3.3V power supply
- 8 pin TSSOP package
- Wide temperature range – 40°C to 85°C

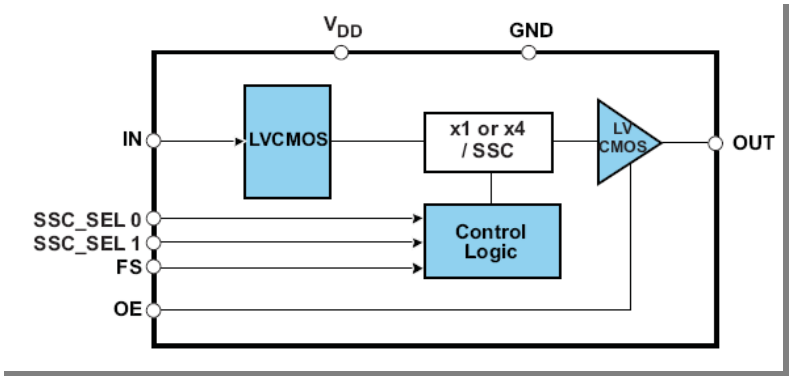
Applications

- **Consumer and Industrial Applications requiring Crystal Oscillator with the possibility of EMI reduction through Spread Spectrum Clocking**
  - •Digital Audio/Video Entertainment: Flat Panel TV; Set-top Boxes; Blu-Ray DVDR
  - •Computer peripherals: Printers
  - •Automotive
  - •Portable devices
  - •Industrial equipment

Benefits

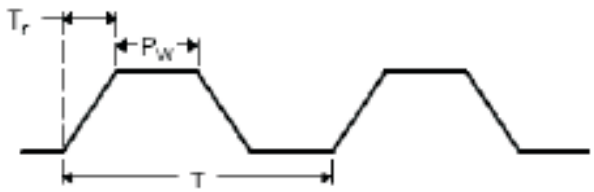
- Reduce EMI thru SSC dithering
- Selectable amount of SSC modulation provides flexibility in EMI reduction
- Wide input/output range supports various applications with single device
- Low board space consumption by 8 pin TSSOP package

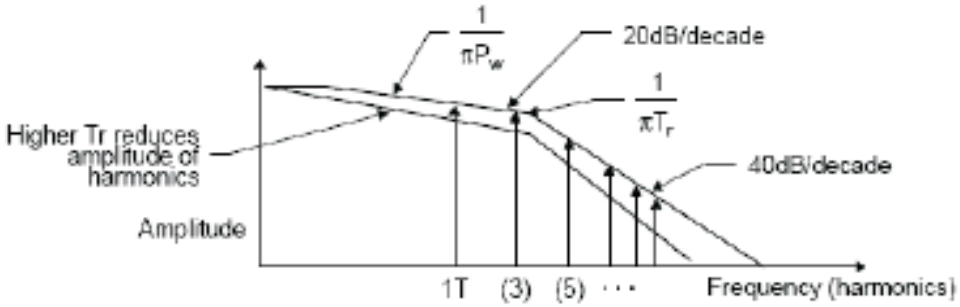




When SSC is not an option

- **Slew Rate Control (SRC)**
  - It smoothes the edges of the clock. This produces less harmonics.
  - Jitter is affected by the slow edges





CDCE906

3-PLL Clock Synthesizer/Multiplier/Divider

Features

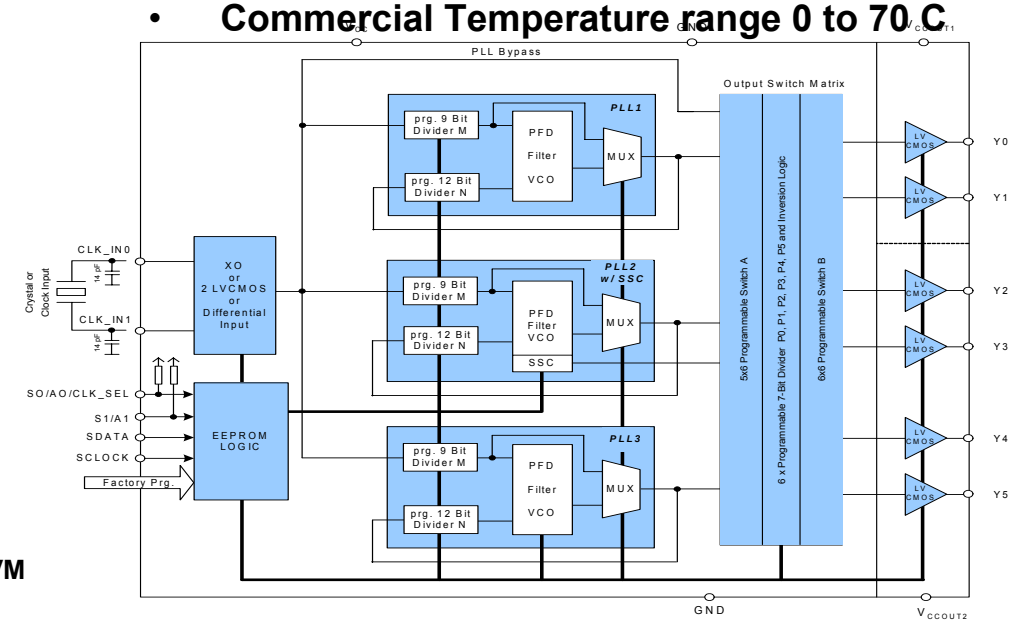
- Input frequencies up to 167 MHz for SE & differential and 54 MHz for crystal
- Output frequencies up to 167 MHz
- Output provides up to 6 LVCMOS/LVTTL
- Low Period Jitter (~ 60ps, pk-pk)
- Provides spread spectrum clocking
- On-chip EEPROM
- 180 degree inverting option

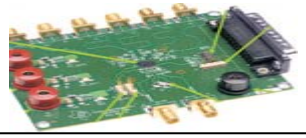
Applications

- Consumer
- DSP clocking
- General purpose frequency synthesizing
- Audio and Video clocking

Benefits

- Wide divider ratio supports fractional multiplication with 0 ppm error
- Universal input supports two single ended clocks, or differential or crystal input
- 3.3 V and 2.5 V output signals from single chip
- SMBus interface provides in-system programming
- TSSOP-20 package
- Commercial Temperature range 0 to 70 C





CDCE906-706PROGEVM

SSC Settings for the CDCE(L)9xx Family

- This is done by choosing the PLL range in every PLL register

- 4 Ranges are implemented:
  - < 125MHz
  - 125MHz<= x <150MHz
  - 150MHz<= x <175MHz
  - >175MHz

- If programmed by hand or with a external controller this has to be done by the programmer

- If the TI ClockPro Software is used the software will automatically set the register values

EMI Summary

- EMI is a problem in most modern electronic systems
- EMI can be countered in several ways
  - PCB (Signal Integrity / Layout)
  - Active components (SSC / SRC)
- Using SSC is a easy, fast and cheap method to reduce EMI
- SSC can be implemented into IC's in different ways
- Different vendors can use different ways to measure their devices THEREFORE:
  - If in doubt, ask!
    - For TI clocking devices: clocks_apps@list.ti.com