High Speed Layout Considerations

Op Amp
ADC
DAC
Clock

Agenda

1) General Considerations
   a) Models: Resistors, Capacitors, Inductors, and Circuit Board
2) High Speed Op Amp Layout
   a) Input and output considerations
   b) Signal routing
   c) Bypass capacitors
   d) Layout examples
3) High Speed ADC/DAC Design and Layout
   a) Input and output considerations
   b) Bypass Capacitors
   c) Splitting the Ground Plane
   d) Filtering clocks to reduce jitter
4) High Speed Clock Layout Guidelines
   a) Coupling (Interference or Cross Talk)
   b) Power Supply Filtering
   c) Power Supply Bypassing & Grounding
   d) Layout Tricks to Reduce EMI

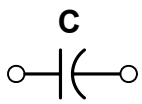
High Speed Layout
Key General Considerations

- **Key points**
  - Use short direct signal routing
  - Control parasitic capacitance
  - Use adequate local bypass capacitors
  - Manage ground planes
  - Avoid ground loops

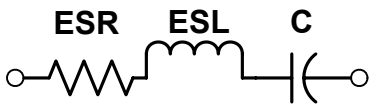
We will discuss each of these with regard to Op Amp, ADC, DAC, and Clock

Capacitor Models

Ideal Model



Better Model



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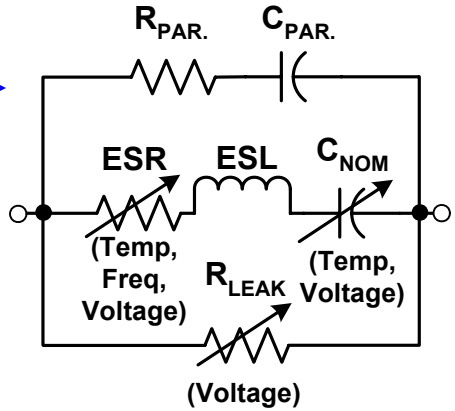
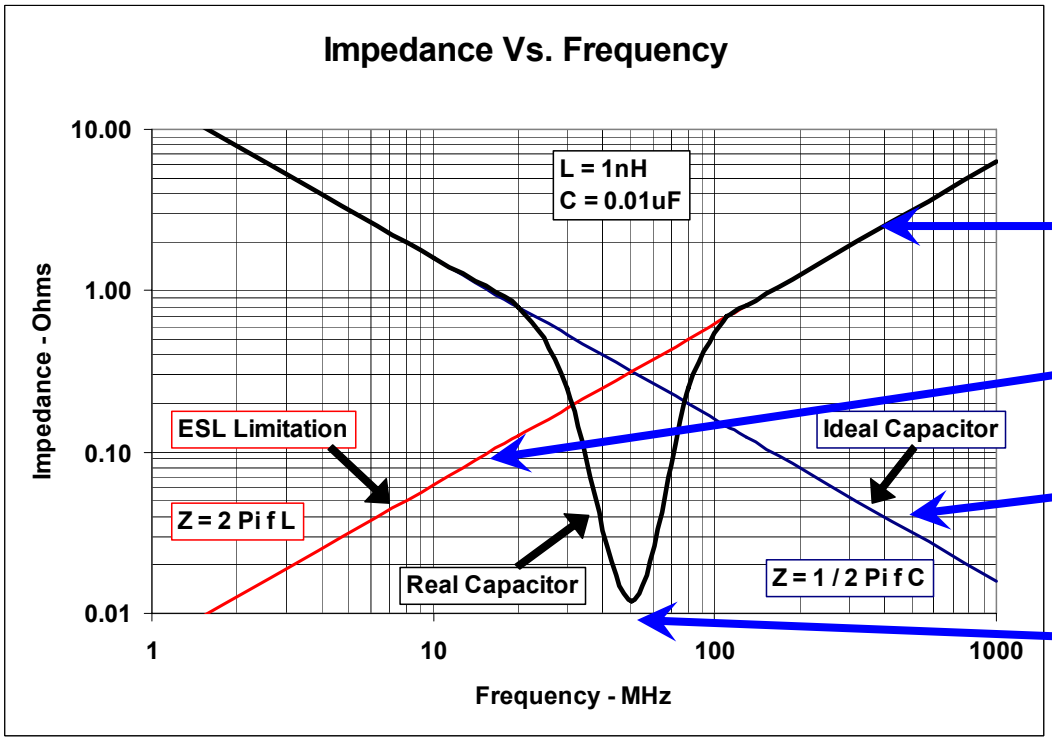




$$Z(\Omega) = \sqrt{(ESR)^2 + (X_{ESL} + X_C)^2}$$

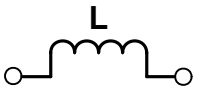
$$X_{ESL}(\Omega) = 2\pi f L$$

$$X_C(\Omega) = \frac{1}{2\pi f C}$$

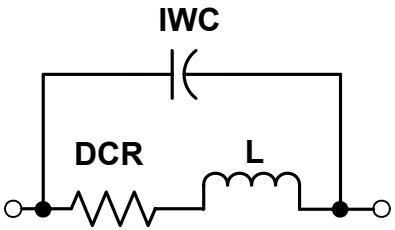
$$f_{RES} = \frac{1}{2\pi\sqrt{LC}}$$

Inductor Models

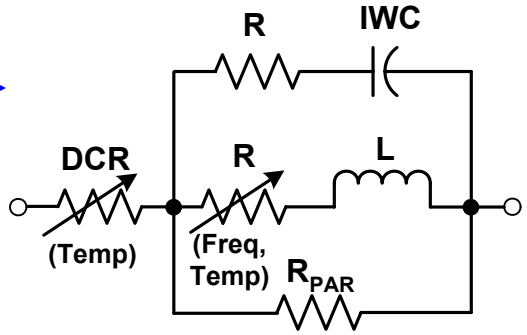
Ideal Model

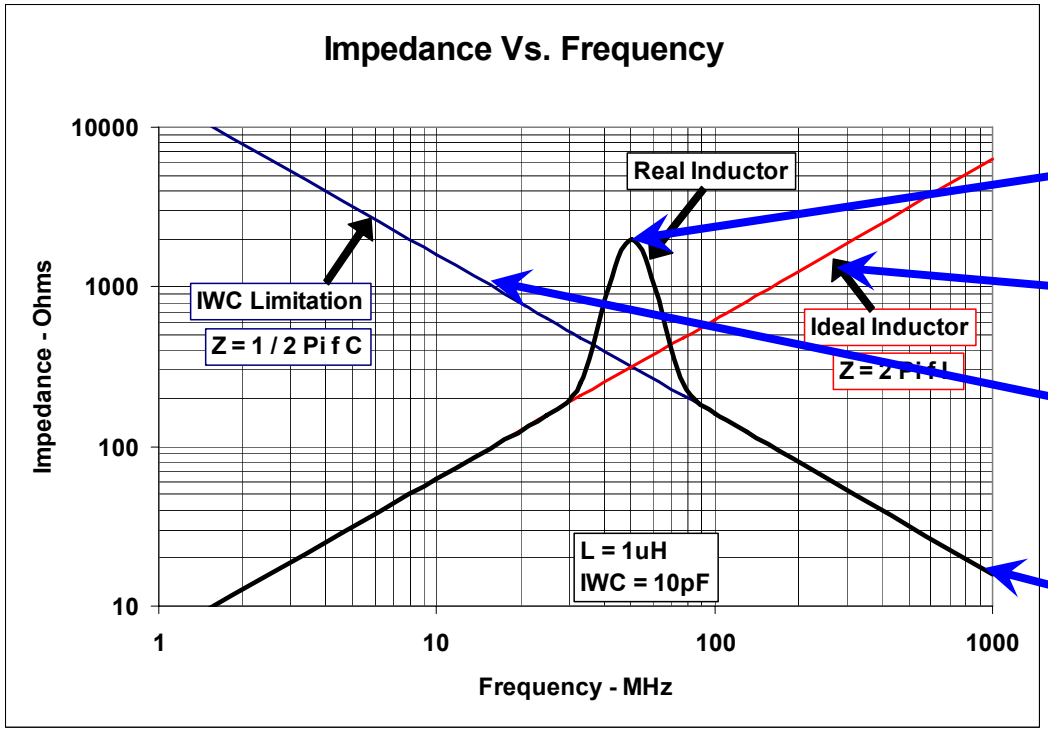


Better Model



Best Model





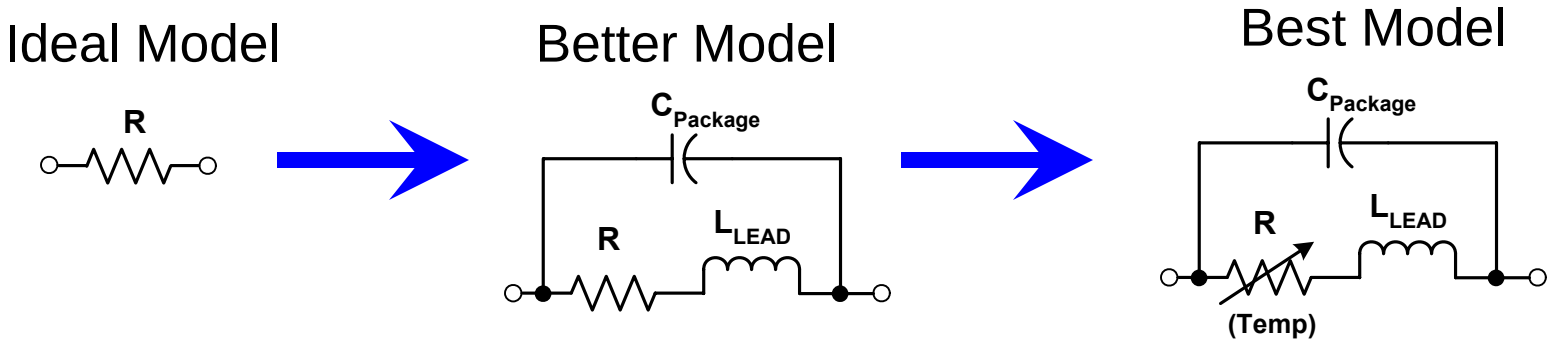
$$f_{RES} = \frac{1}{2\pi\sqrt{LC}}$$

$$X_L(\Omega) = 2\pi\ f\ L$$

$$X_{IWC}(\Omega) = \frac{1}{2\pi\ f\ C}$$

$$Z(\Omega) = DCR + \frac{X_L\ X_{IWC}}{X_L + X_{IWC}}$$

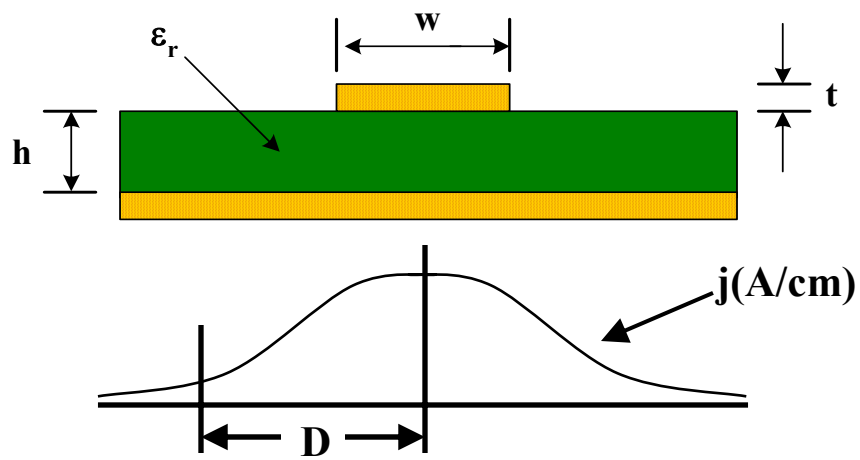
Resistor Models



- **Using SMT resistors minimizes lead inductance to the point that PCB traces are the limiting factor**
- **SMT packages also minimize the capacitance between the leads such that this parasitic is usually insignificant**
- **Note that resistor packs CAN have significant lead inductance and resistor-to-resistor capacitance, so choose wisely based on the application**
- **Resistors will have temperature coefficients, 200PPM is common, but higher precision is available**
- **AVOID Wire-wound resistors and leaded resistors for high speed applications due to their large inductance**

Remember Current Return Path

$$j(A/cm) = \frac{I_o}{\pi h} \times \frac{1}{1 + \left(\frac{D}{h}\right)^2}$$

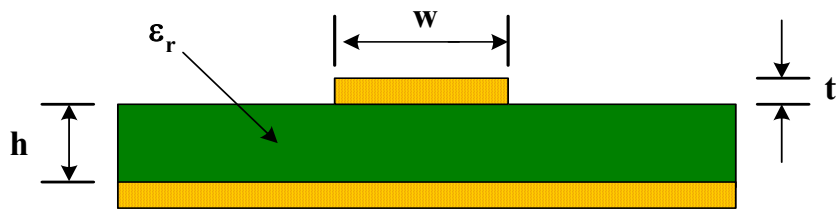


I_O = total signal current (A)
h = PCB thickness (cm)
D = distance from center of trace (cm)

- Return Current Flow is directly below the signal trace
- Must have Solid return path (i.e. Solid Ground Plane) under the signal trace for lowest impedance.
  - Do not route high speed signals near edge of board; especially clocks

PCB Components

Component: Microstrip Copper Traces
Purpose: Interconnect two or more points
Problem: Inductance and Capacitance



x = length of trace (cm)
w = width of trace (cm)
h = thickness of board (cm)
t = thickness of trace (cm)
e_r = PCB dielectric constant (FR-4 ≈ 4.5)

$$L(nH) \approx 2x \ ln\left(\frac{5.98\,h}{0.8\,w + t}\right)$$

$$C(pF) \approx \frac{0.264x\ (\varepsilon_r + 1.41)}{ln\left(\frac{5.98\,h}{0.8\,w + t}\right)}$$

$$T_p(\,ps/cm\,) = 31.6\sqrt{L(nH)C(pF)}$$

0.8mm (0.031”) trace on 0.8mm (0.031”) thick PCB (FR-4) has:

≈ 4nH and 0.8pF per cm

≈ 10nH and 2.0pF per inch

Use Microstrip design to control impedance

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}}$$

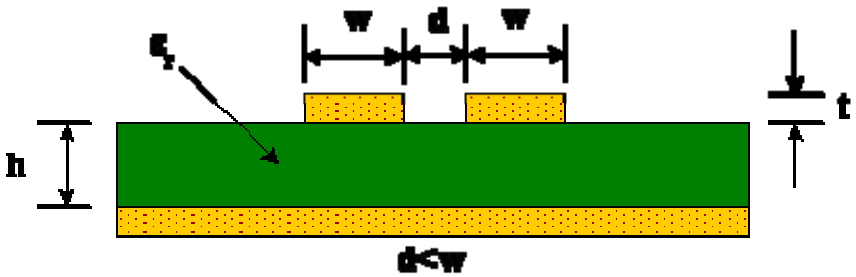
Impedance of Differential Traces

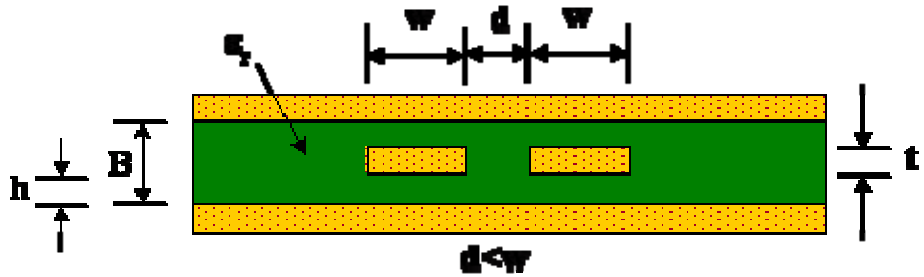
MICROSTRIP

- Most Commonly Used
- Less Propagation Delay
- May Radiate more RF
- Only requires 2 Layers

STRIPLINE

- More Propagation Delay
- Better Noise Immunity/Radiation
- Requires at least 3 Layers
- May be harder to control Z_0





$$Z_{diff}(\Omega) \approx 2 * Z_0 \left(1 - 0.48 e^{-\frac{0.96d}{h}} \right)$$

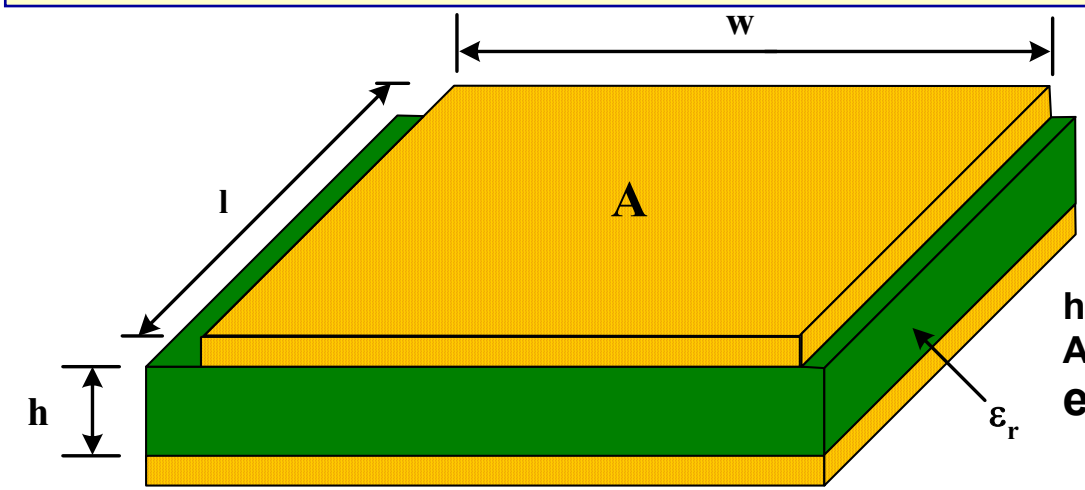
$$Z_{diff}(\Omega) \approx 2 * Z_0 \left(1 - 0.347 e^{-\frac{2.9d}{B}} \right)$$

$$Z_0(\Omega) \approx \frac{60}{\sqrt{0.475\,\varepsilon_r + 0.67}} \ln\left(\frac{4\,h}{0.67(0.8w + t)} \right)$$

$$Z_0(\Omega) \approx \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4\,h}{0.67\pi(0.8w + 1)} \right)$$

PCB Components

Component: Copper Planes
Purpose: Used For Ground Planes and Power Planes
Problem: Stray Capacitance on Signal Traces
Benefit: At high frequencies (1G+) Adds Bypass Capacitance with low Inductance



$$C(pF) \approx \frac{0.0886\ \varepsilon_r\ A}{h}$$

h = separation between planes (cm)
A = area of common planes = l*w (cm²)
e_r = PCB dielectric constant (FR-4 ≈ 4.5)

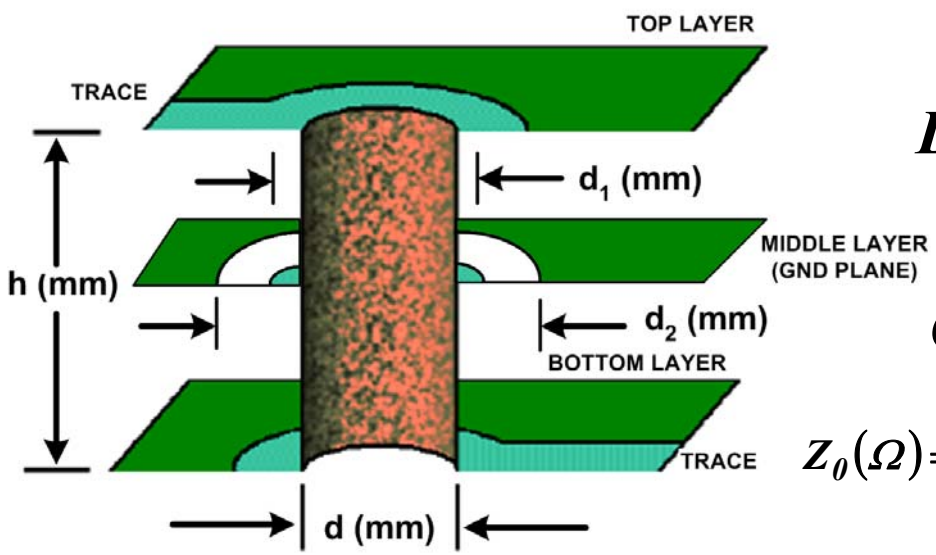
0.8mm (0.031”) thick PCB (FR-4) has:

≈ 0.5pF per cm²

≈ 32.7pF per inch²

PCB Components

Component: Vias
Purpose: Interconnect traces on different layers
Problem: Inductance and Capacitance



$$L(nH) \approx \frac{h}{5}\left[1 + ln\left(\frac{4h}{d}\right)\right]$$

$$C(pF) \approx \frac{0.0555\ \varepsilon_r\ h\ d_1}{d_2 - d_1}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \qquad T_p(ps/cm) = 31.6\sqrt{L(nH)C(pF)}$$

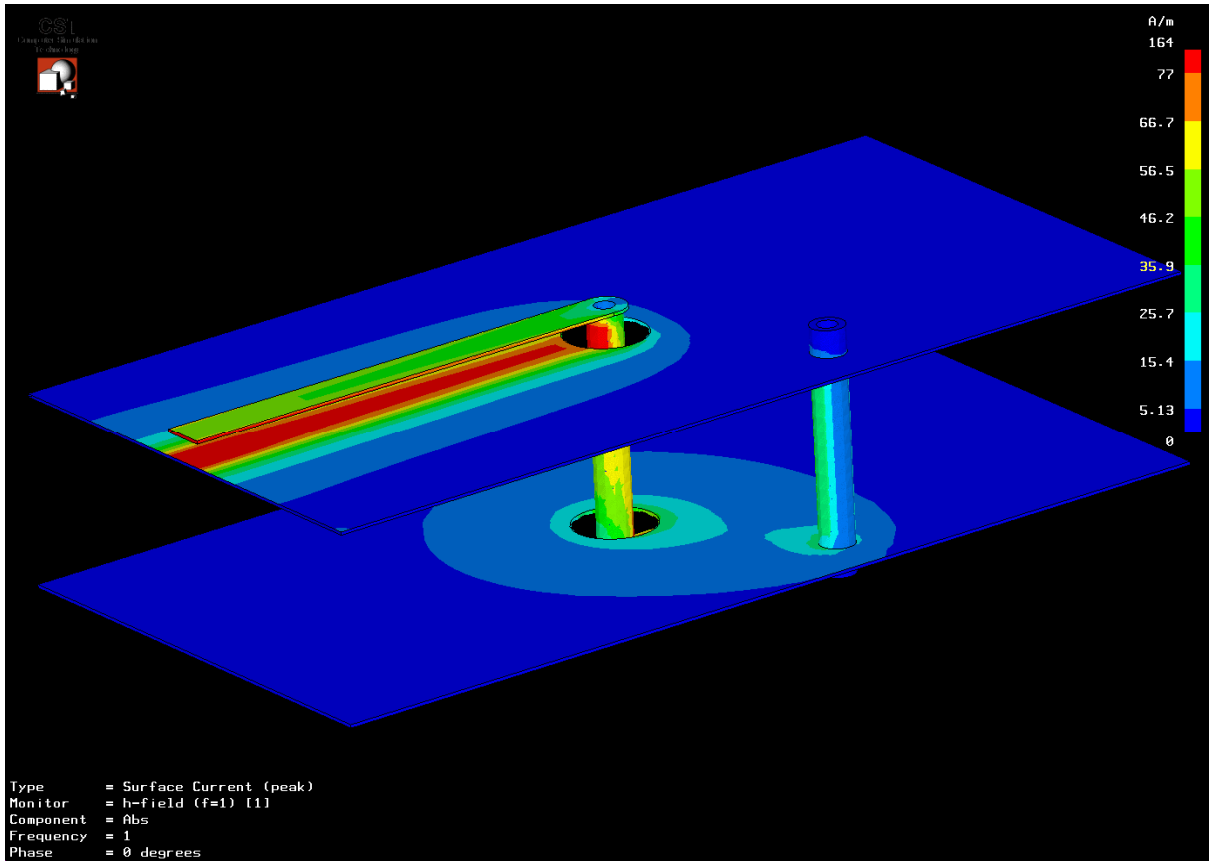
0.4mm (0.0157”) via with 1.6mm (0.063”) thick PCB has ≈ 1.2nH

1.6mm (0.063”) Clearance hole around 0.8mm (0.031”) pad on FR-4 has ≈ 0.4pF

e_r = PCB dielectric constant (FR-4 ≈ 4.5)

Taking a Look at Vias

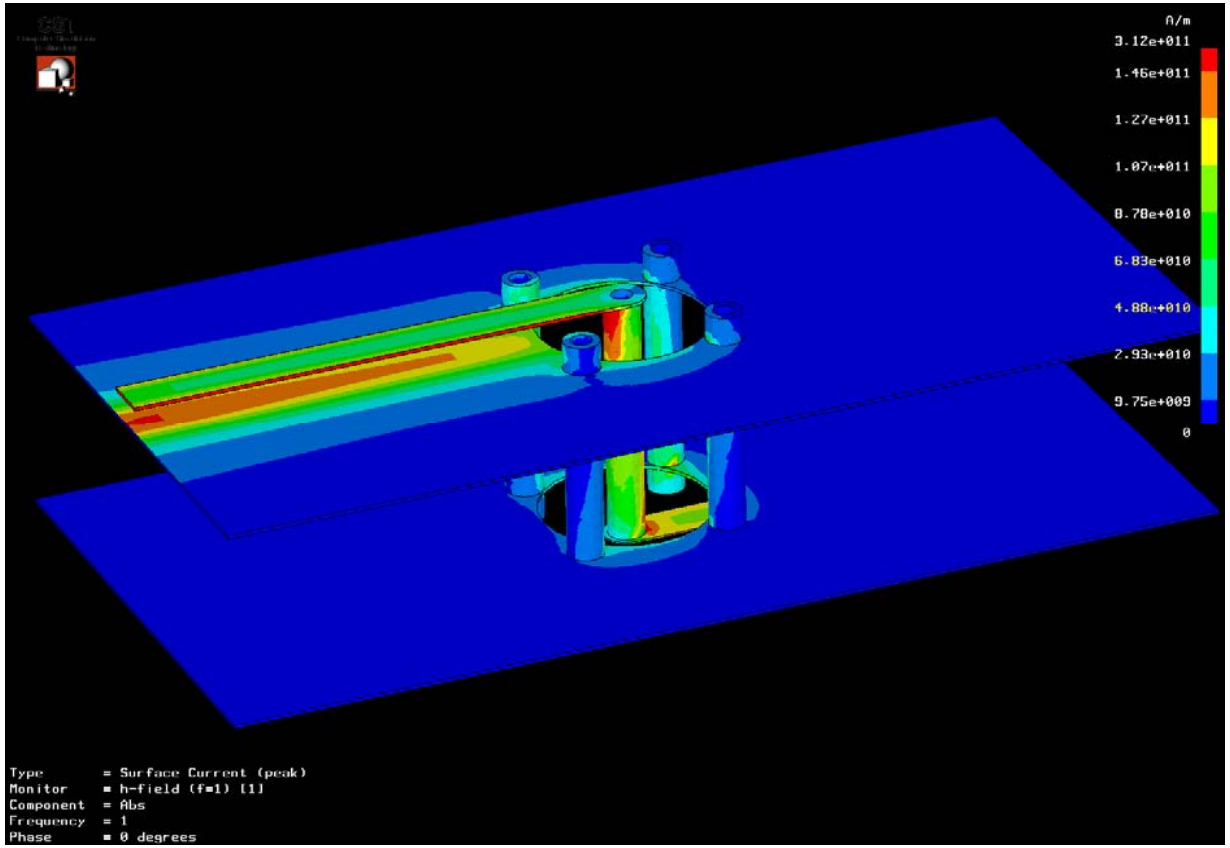
- Must have Return Path Vias next to Signal Path Vias.
- Notice Large Current Density Area flow in return path.
- Will have a change in impedance with this configuration.



2-Layer PCB showing Current Density of PCB trace and Single Return Path Via.

Controlled Impedance Vias

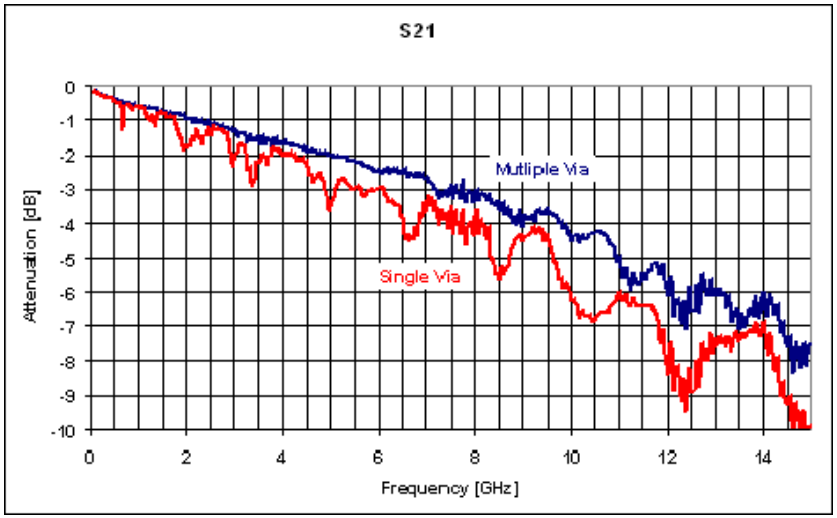
- Better Solution is to add Multiple Return Path Vias.
- Notice minimal Current Density Area Flow at vias.
- Improved impedance – reduces reflections.

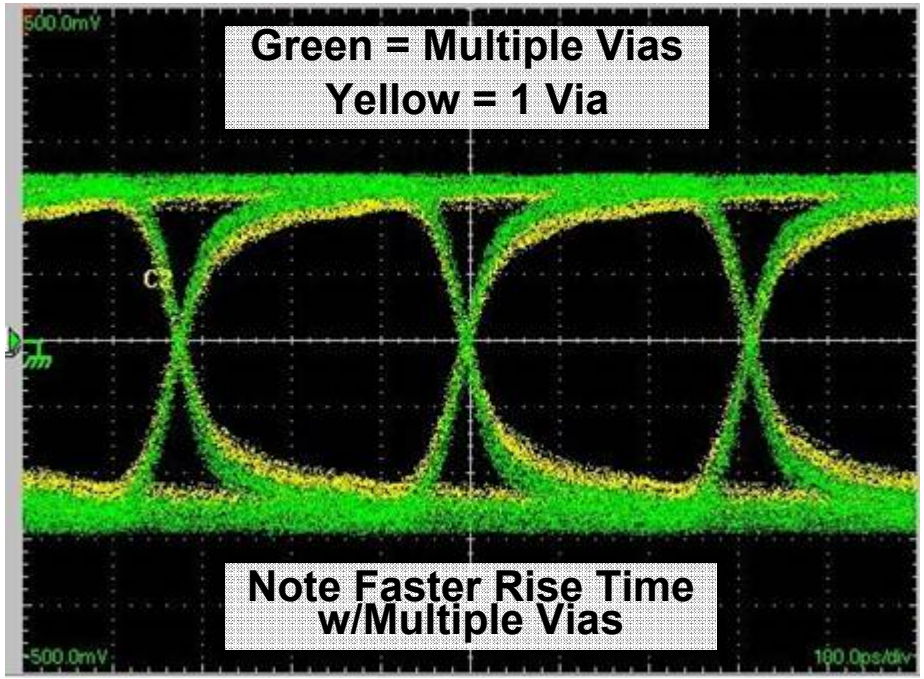


2-Layer PCB showing Current Density of PCB trace and Multiple Return Path Vias.

Controlled Impedance Vias

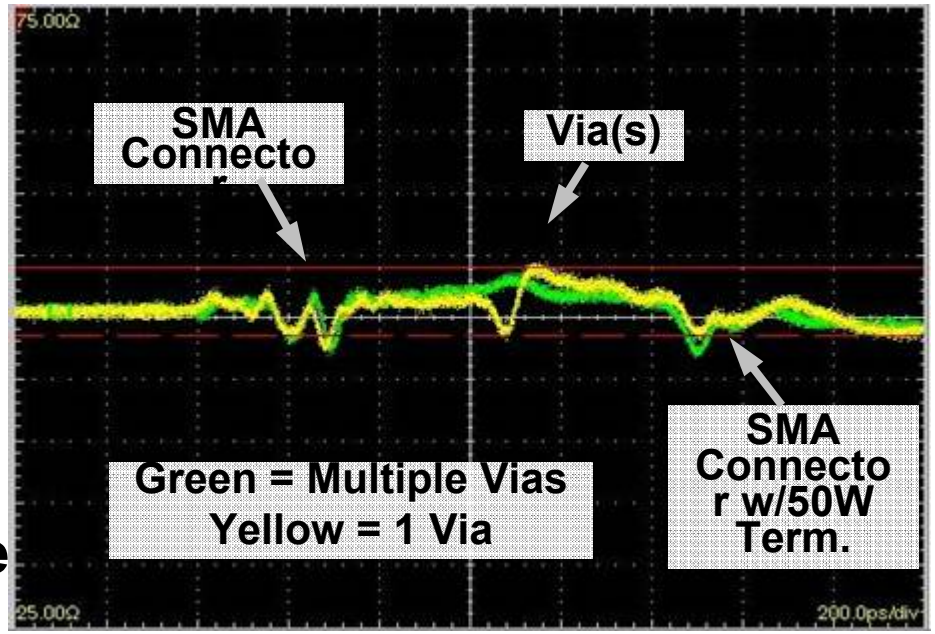
S21 Results





3.125-Gbps PBRS Eye Pattern on 2.8" (7.1cm) PCB trace

TDR Pulse



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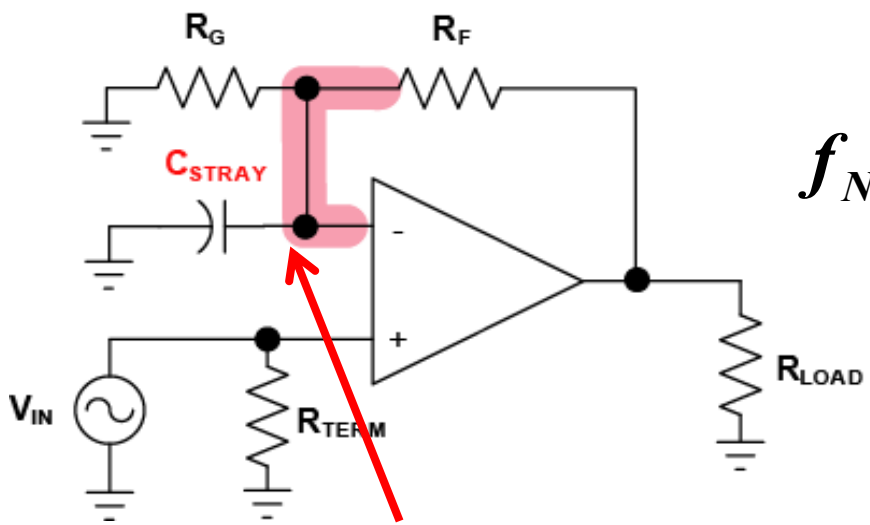
(-) Input Capacitance

- Inverting input node of an op amp is sensitive to stray capacitance (C_{STRAY})
- R_F,R_G and C_{STRAY} add a zero to the noise gain which can lead to instability
- As Little as 1pF of C_{STRAY} can cause stability problems
- inverting input Node includes the entire trace up to the placement of R_F, R_G, and any other component on the inverting input

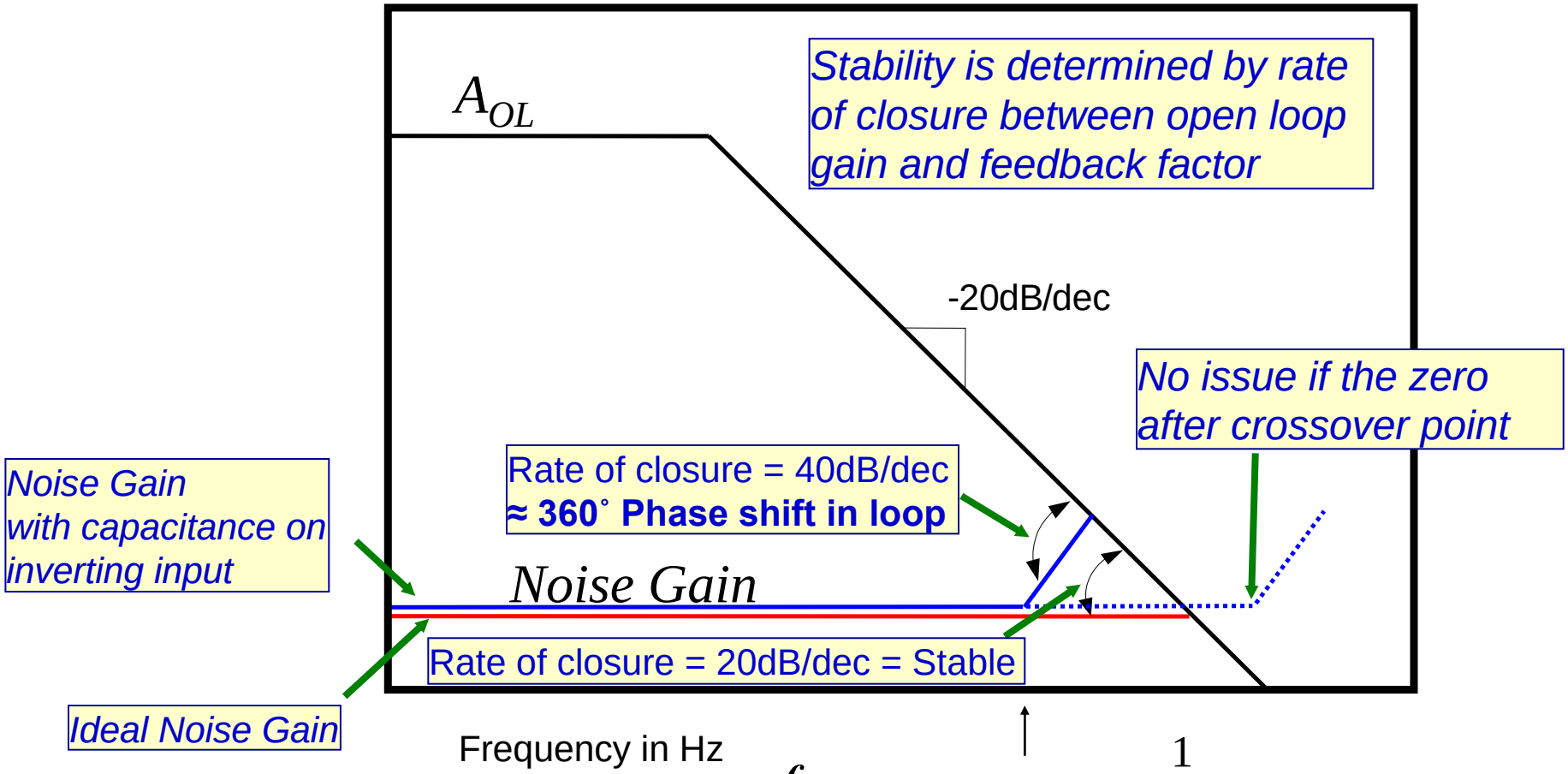


$$f_{NG_ZERO} = \frac{1}{(2\pi C_{STRAY}) \times (R_F \parallel R_G)}$$

C_{STRAY} modifies the noise gain by adding a zero

Inverting Input Capacitance is Bad

Bode Plot

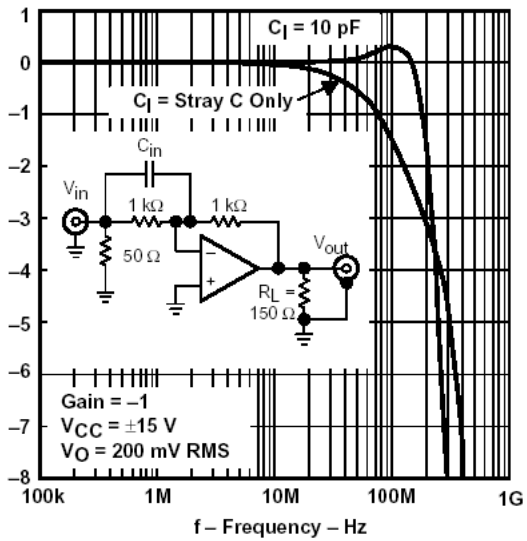


$$f_{NG_ZERO} = \frac{1}{(2\pi\, C_{STRAY}) \times (R_F \parallel R_G)}$$

Minimizing Stray C at (-) Input

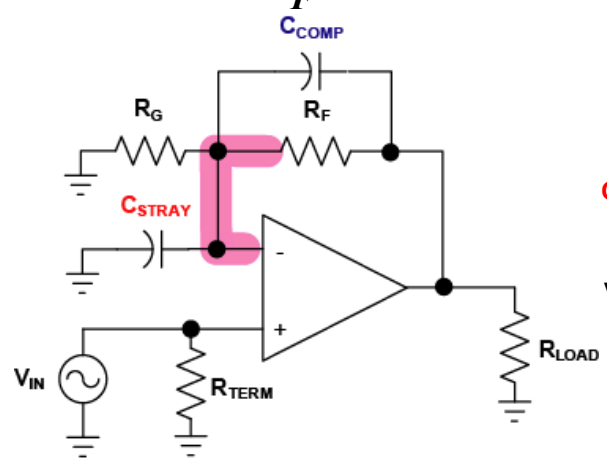
Solutions:

1. Eliminate Ground Planes and Power Planes under and near the inverting input (-)
2. Shorten trace by moving components closer to the inverting input (-)
3. Reduce R_F and R_G values
4. Increase noise gain of op amp
5. Place Compensation Capacitor Across R_F
6. Use Inverting Configuration

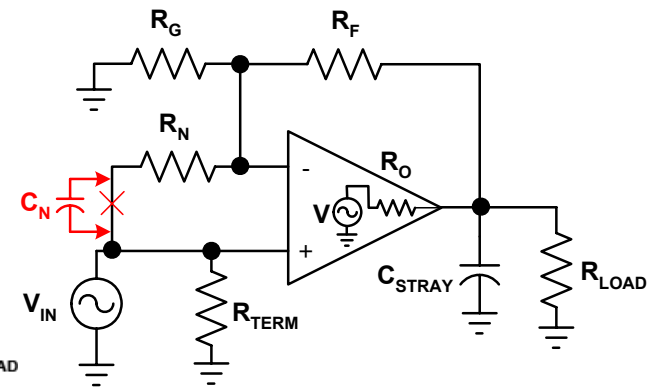


Inverting Configuration

$$C_{COMP} = \frac{R_G}{R_F} C_{STRAY}$$



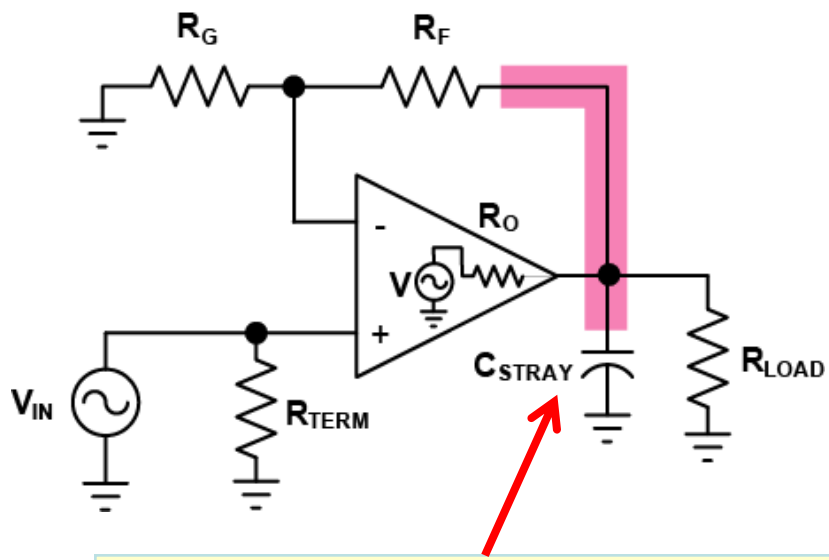
Feedback Cap Compensation



Increase Noise Gain

Output Capacitance

- Op amps are sensitive to capacitance on output (C_{STRAY})
- Real op amps have output Impedance (R_O)
- R_O and C_{STRAY} create another pole in the open loop gain which can lead to instability



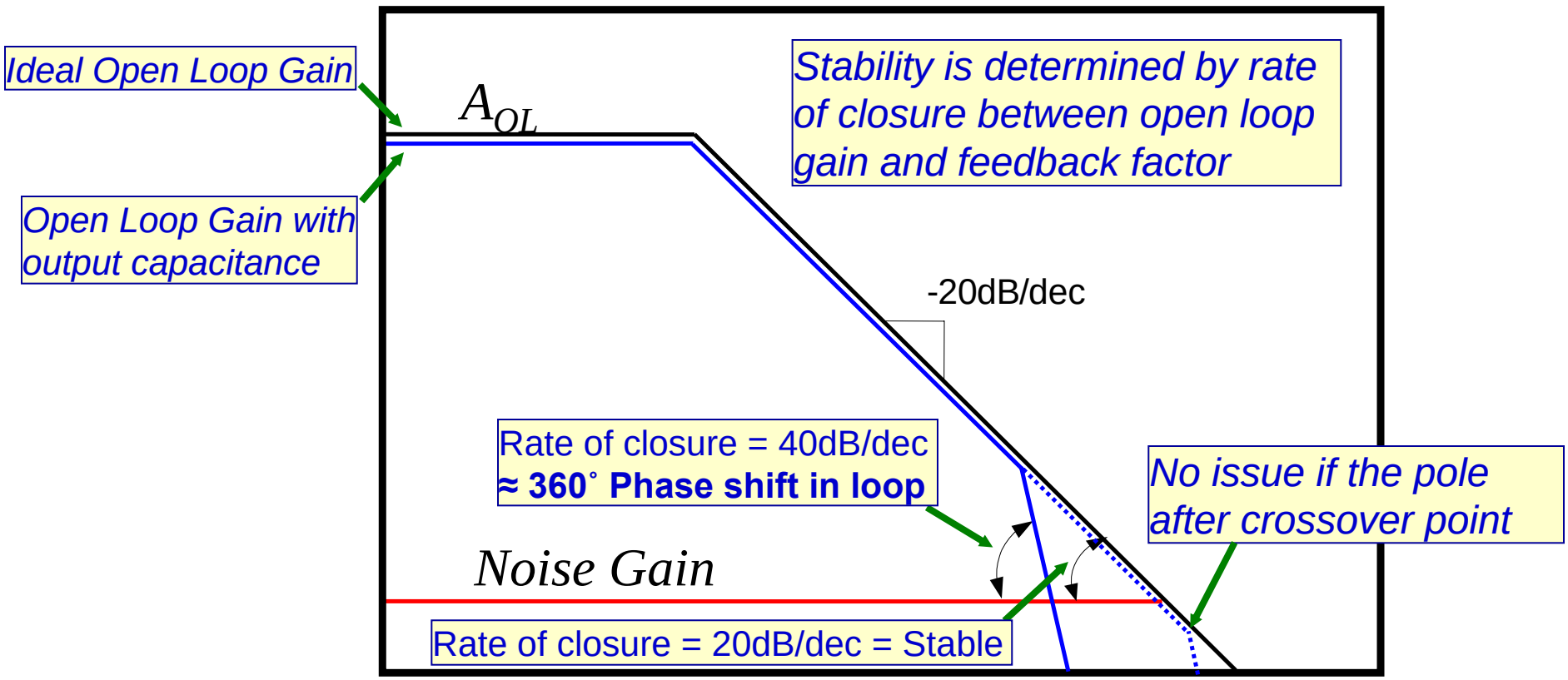
$$f_{A_{OL}_POLE} \approx \frac{1}{2\pi C_{STRAY} R_O}$$

Assuming:
$R_O << R_F, R_{LOAD}$

C_{STRAY} modifies the open loop gain by adding another pole

Output Capacitance is Bad

Bode Plot

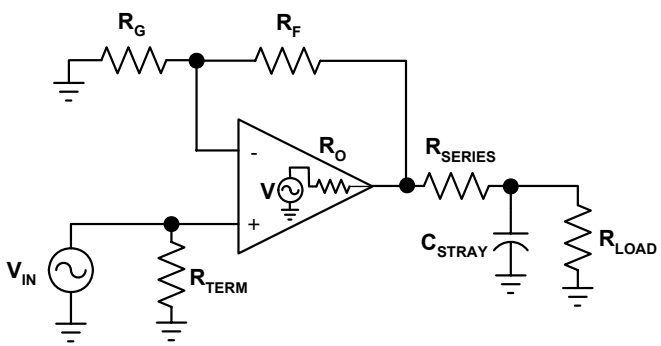


$$f_{A_{OL}_POLE} \approx \frac{1}{2\pi C_{STRAY} R_O}$$

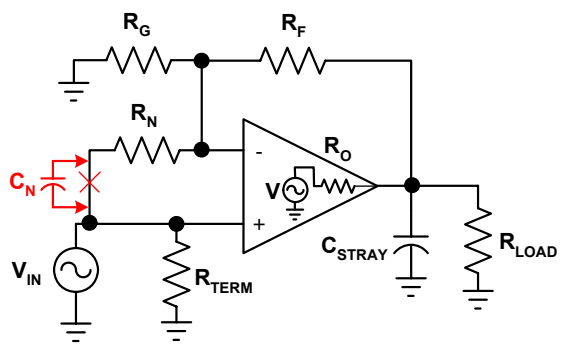
Minimizing Effects of Output Capacitance

Solutions:

1. Eliminate Ground Planes and Power Planes under output node
2. Shorten traces by moving components closer to output pin – especially Series Matching R
3. Use series output resistor
4. Increase Noise Gain of System
5. Use Feedback Compensation

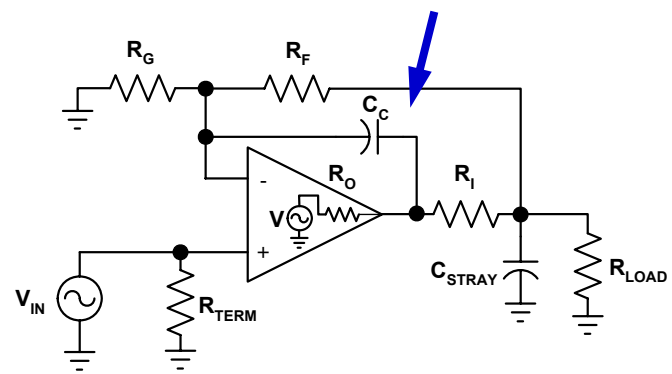


Adding Series R for Isolation



Increasing Noise Gain Only

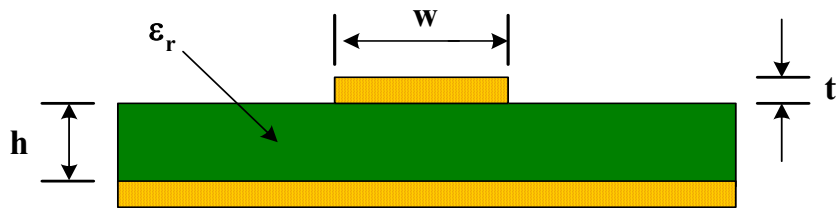
Do not use for CFB



Feedback Compensation

Input and Output Trace Impedance

Match impedance of input transmission line
Match impedance of output transmission line



x = length of trace (cm)
w = width of trace (cm)
h = height of trace (cm)
t = thickness of trace (cm)
e_r = PCB Permeability (FR-4 ≈ 4.5)

$$L(nH) \approx 2x \ ln\left(\frac{5.98\,h}{0.8\,w + t}\right)$$

$$C(pF) \approx \frac{0.264x\ (\varepsilon_r + 1.41)}{ln\left(\frac{5.98\,h}{0.8\,w + t}\right)}$$

$$T_p(\,ps/cm\,) = 31.6\sqrt{L(nH)C(pF)}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}}$$

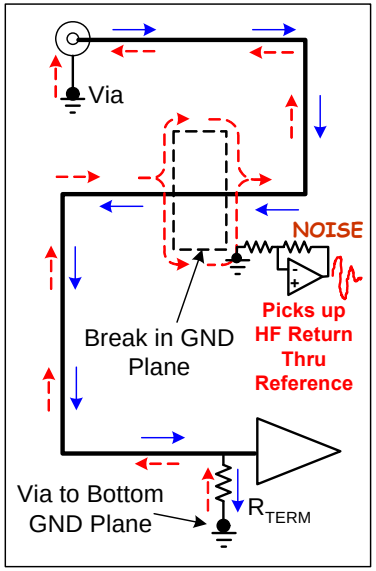
0.8mm (0.031”) trace on 0.8mm (0.031”) thick PCB (FR-4) has:

≈ 4nH and 0.8pF per cm

≈ 10nH and 2.0pF per inch

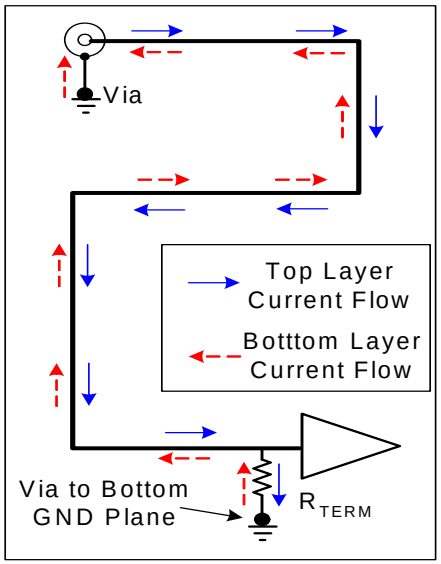
Input Signal Routing

Use direct routing and avoid loops



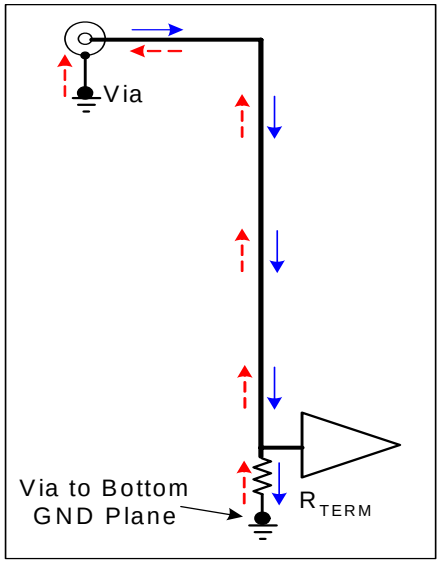
WORST

Large Current Loop + Discontinuous GND Plane



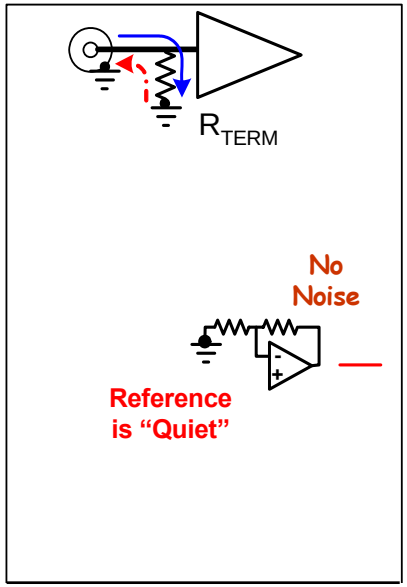
BAD

Large Current Loop



BETTER

Reduced Current Loop



BEST

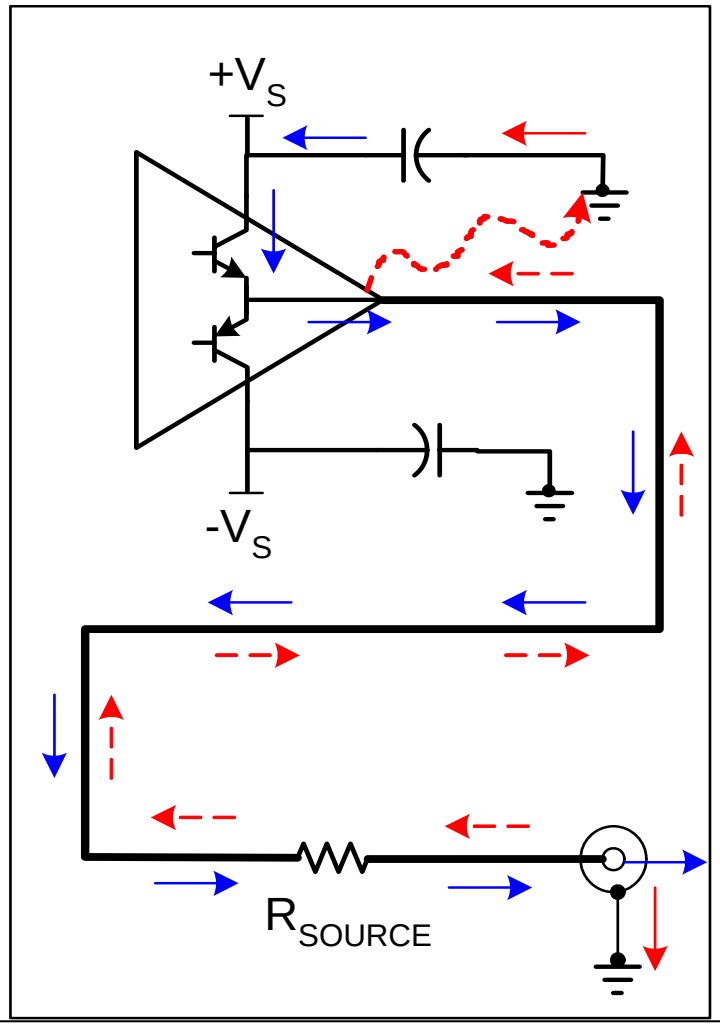
Minimum Current Loop

Output Signal Routing

Use direct routing and avoid loops

Problems:

1. Long winding path causing large current loop area.
2. HF bypass caps are placed too far away from amplifier and GND. Inductance eliminates benefit of bypass caps.
3. GND of bypass caps are too far away from amplifier output.
4. Series Resistor (RSOURCE) is too far away from the amplifier. Causes C-loading on amplifier and lack of a transmission line.
5. Single GND point on connector

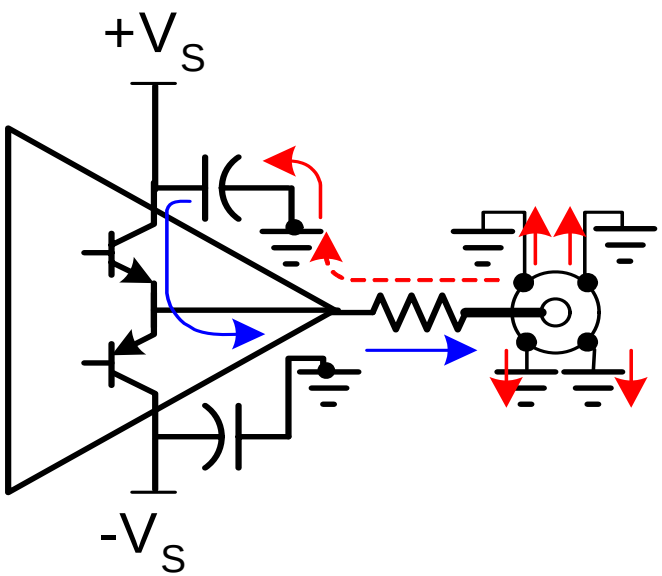


Output Signal Routing

Use direct routing and avoid loops

Solutions:

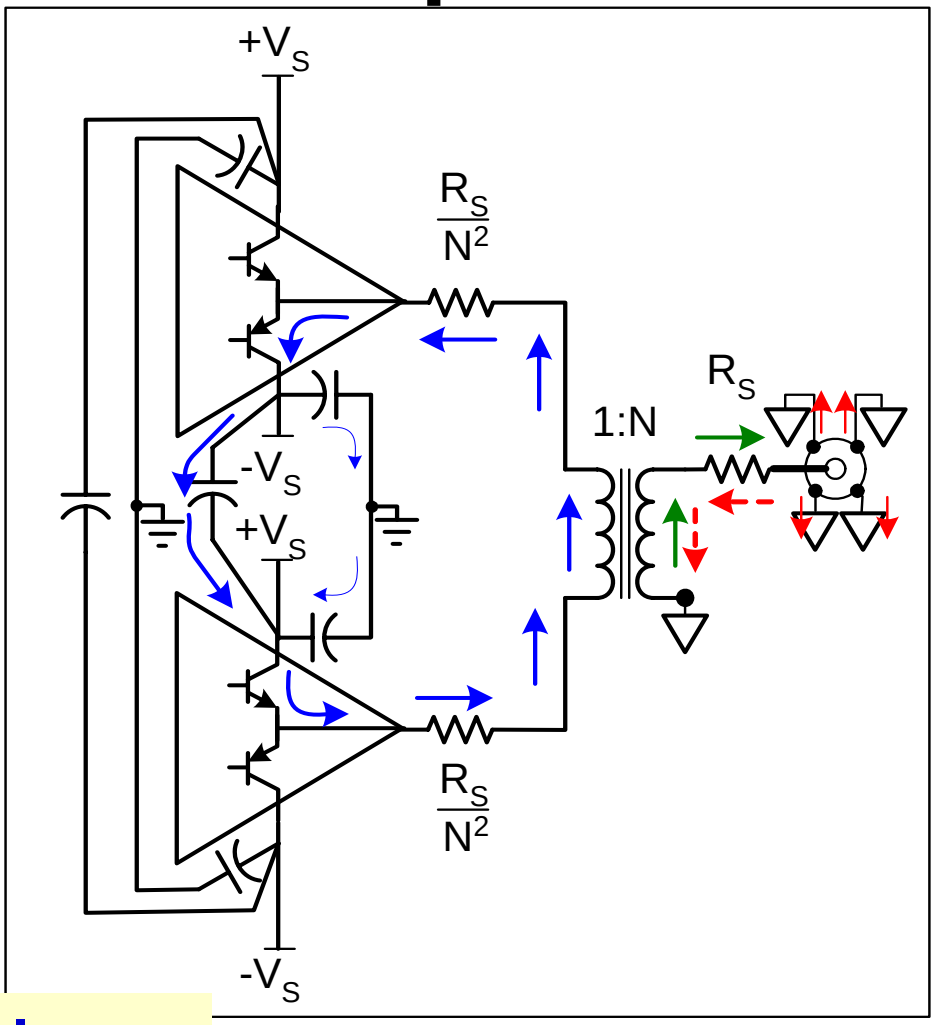
1. Amplifier is next to Connector minimizing loop area.
2. HF bypass caps are now placed next to amplifier power supply pins and has short GND connection.
3. GND of bypass caps near amplifier output – but not too close to cause C-loading issues.
4. Source Resistance is next to amplifier output.
5. Multiple GND points on connector.



Differential Output Signal Routing From 2 Amplifiers

Guidelines

1. **Minimize Loop Area on Driver Side.**
2. **Utilize a single Capacitor between opposite amplifier supplies as this should be the main current flow. Adding this Capacitor can reduce 2nd-Order Distortion by 6 to 10dB!**
3. **Use bypass caps to GND at a mid-point to handle stray-C return path currents but do not disrupt differential current flow.**

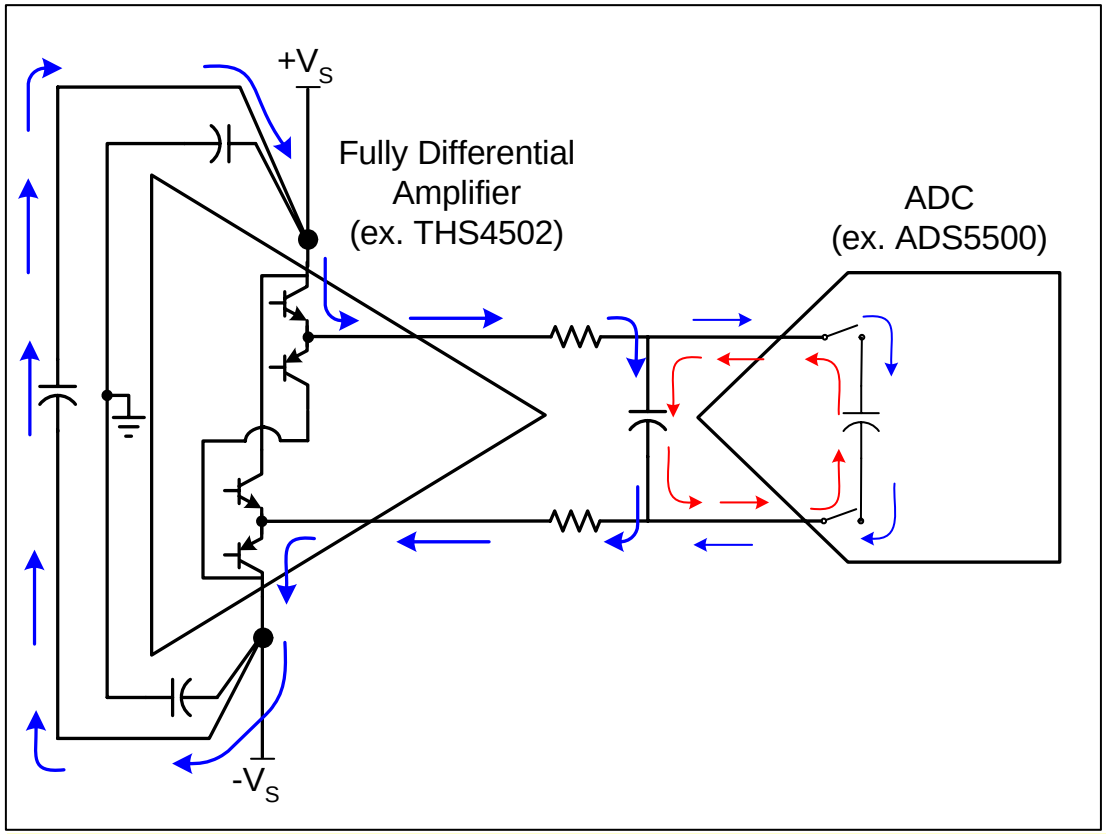


Use direct routing and avoid loops

Differential Output Signal Routing From FDA

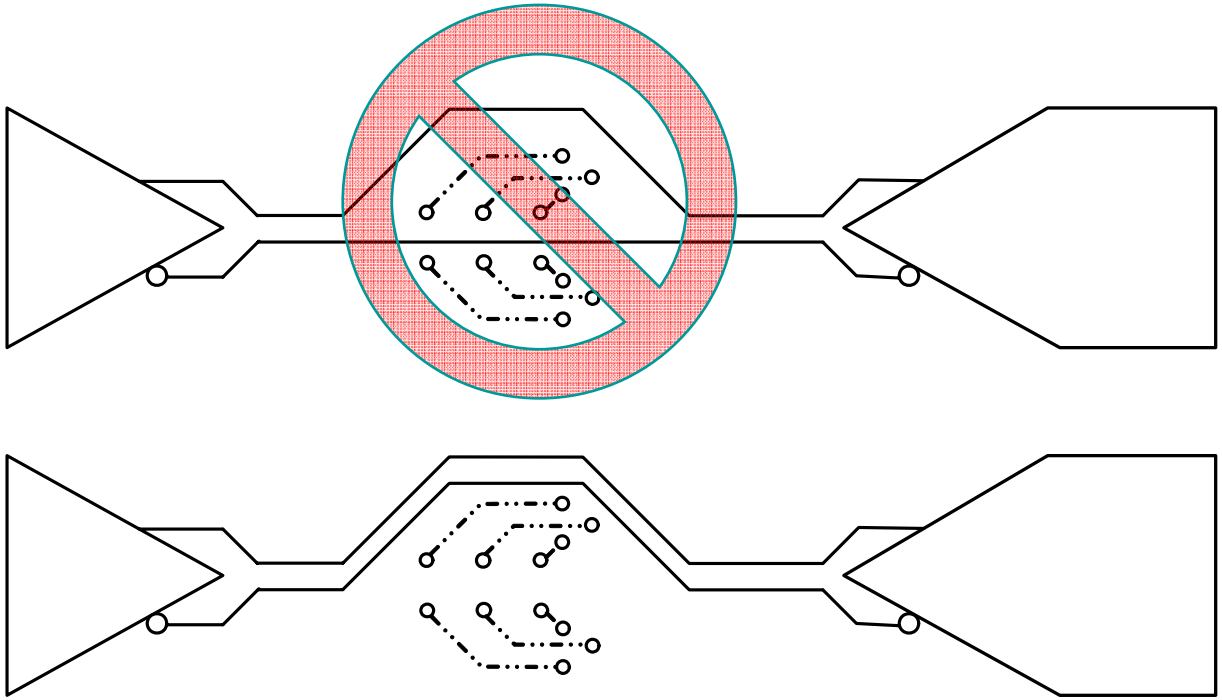
Guidelines

1. **Minimize Loop Area on Driver Side.**
2. **Utilize a single Capacitor between opposite amplifier supplies as this should be the main current flow.**
3. **Use bypass caps to GND at a mid-point to handle stray-C return path currents but do not disrupt differential current flow.**
4. **Filter Cap should allow for small Loop Areas – including "kick-back" current flow.**



Use direct routing and avoid loops

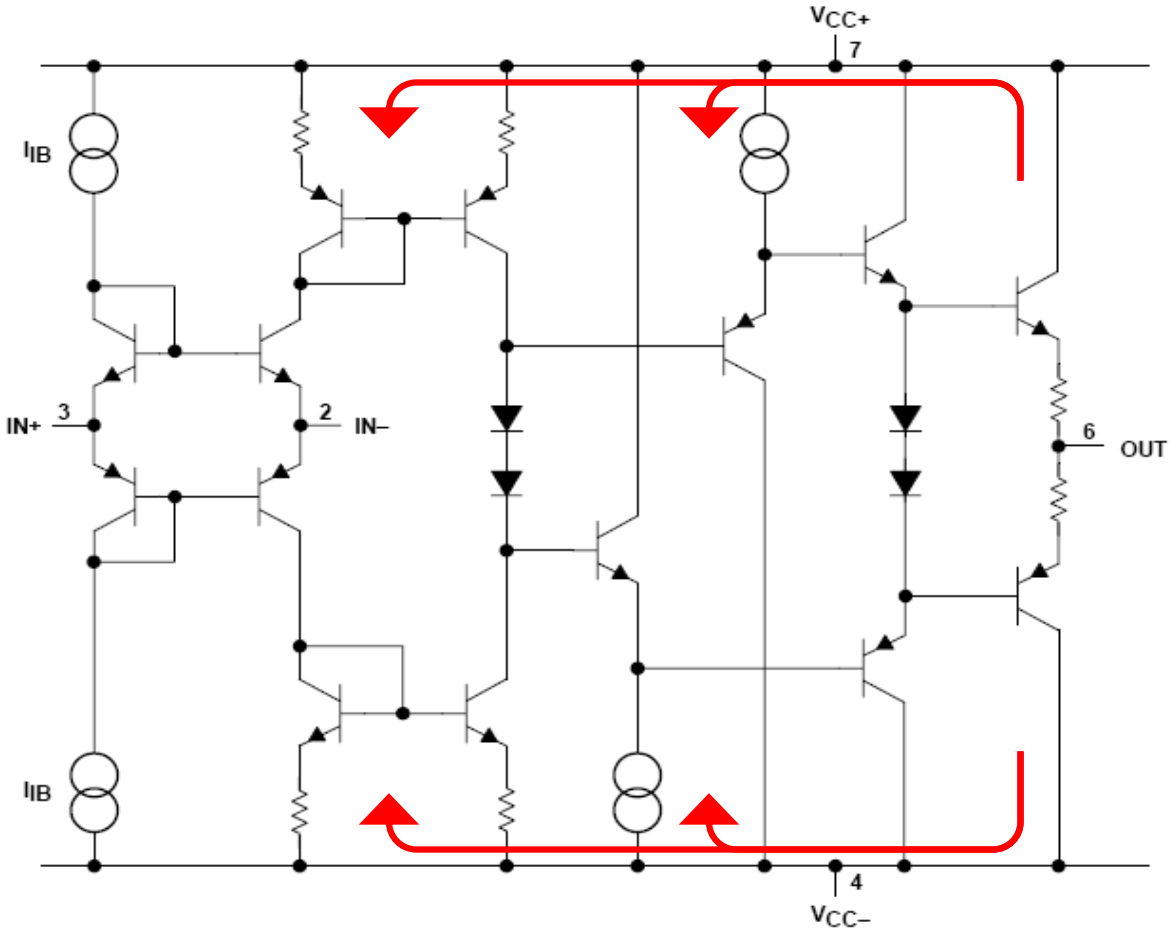
Routing Differential Traces



- Keep differential traces close together to keep noise injection as a Common-Mode signal which is rejected differentially
- Route differential traces around obstacles together, or move obstacle
- Keep trace lengths the exact same length to keep delays equal

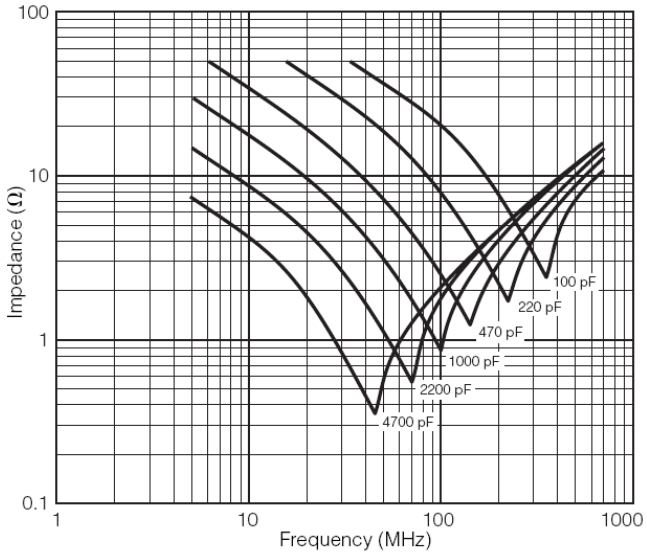
Power Supply Bypass Capacitors

- Simplified THS3001 schematic
  - *All stages interconnect through the power supplies*

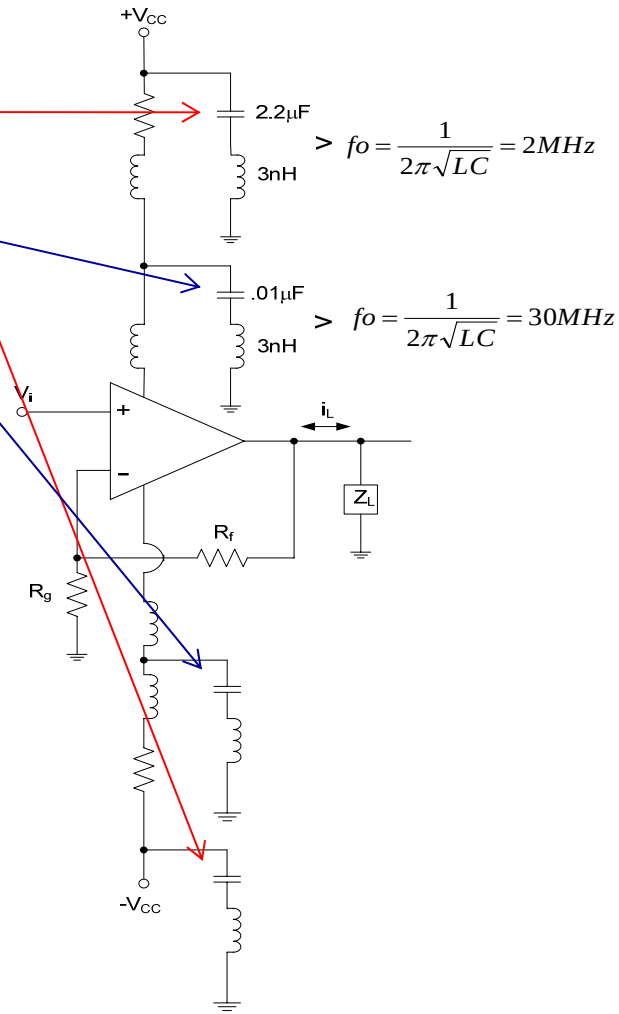


Power supply parasitic elements

- *Our general recommendations for high speed op amp bypass capacitors are:*
  1. *Place a 2.2µF to 10µF capacitor within 2" from device. It can be shared among other op amps*
  2. *Use separate 0.01µF to 0.1µF as close as possible to each supply pin*

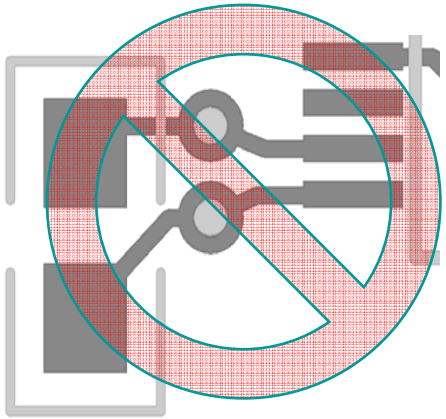


Typical capacitor impedance versus frequency curves

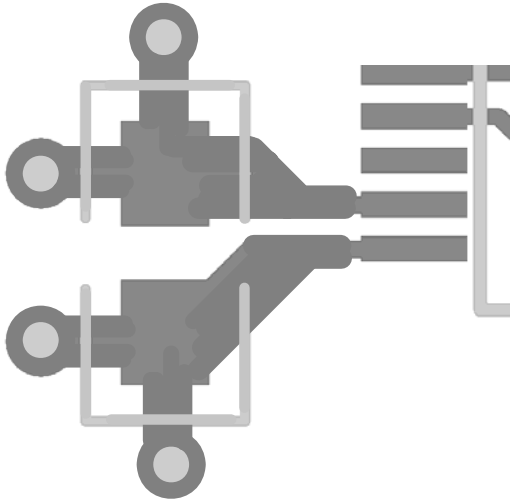


Bypass Capacitor Routing

- DO NOT have vias between bypass caps and active device – Visualize the high frequency current flow !!!
- Ensure Bypass caps are on same layer as active component for best results.
- Route vias into the bypass caps and then into the active component.
- The more vias the better.
- The wider the traces the better.
- The closer the better (<0.5cm, <0.2”)
- Length to Width should not exceed 3:1



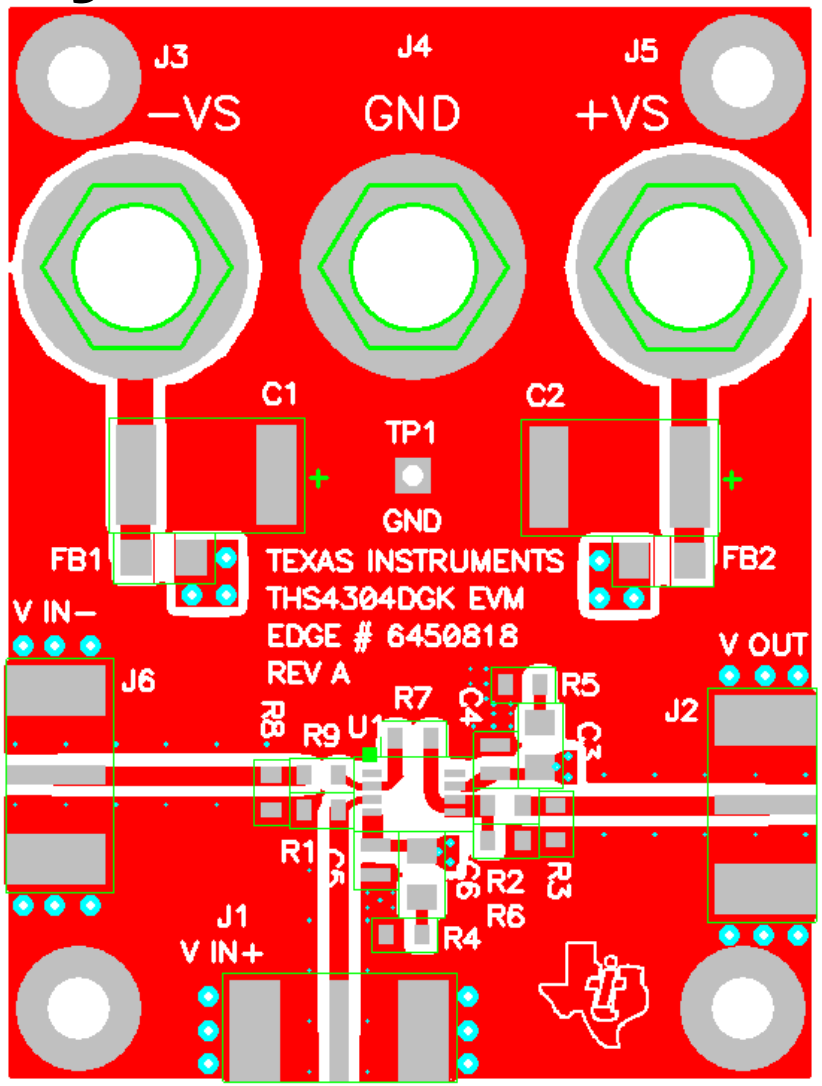
Poor Bypassing



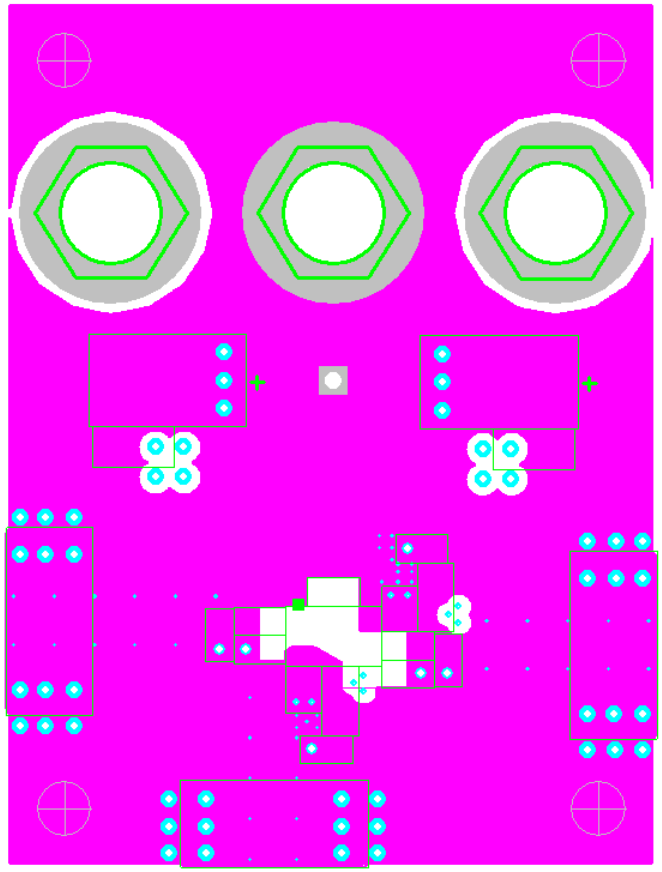
Good Bypassing

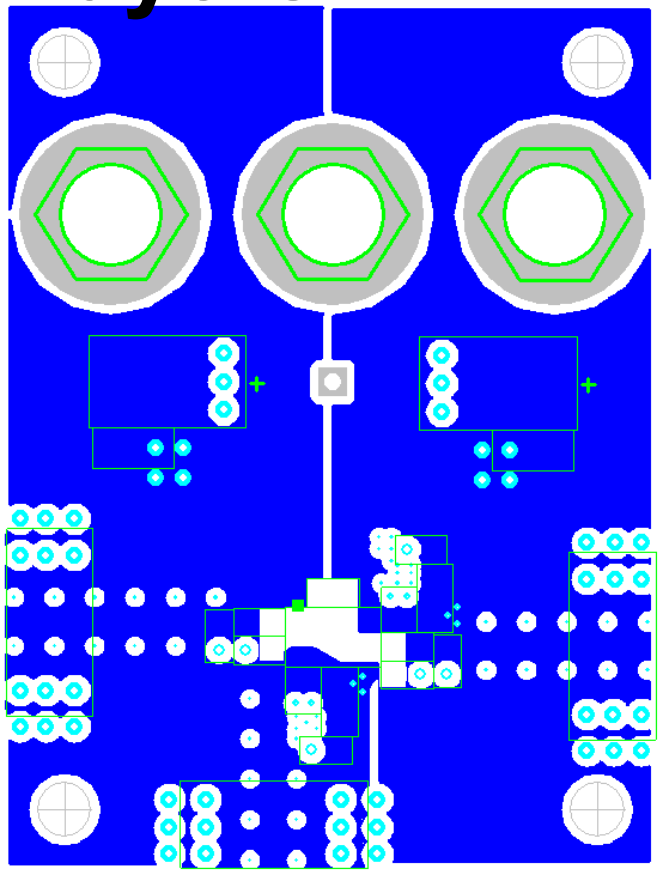
Example of High Speed Layout: Top Layer

1. Signal In/Out traces are microstrip line with Z0 = 50Ω.
2. Terminating Resistors next to Amp.
3. Output Series Resistor next to Amp.
4. 100pF NPO Bypass Caps next to Amp.
5. Larger Bypass Caps Farther Away with Ferrite Chips for HF isolation.
6. MULTIPLE Vias Everywhere to Allow for easy Current Flow – no spokes
7. Short, Fat Traces to reduce inductance
8. Side Mount SMA connectors for Smooth Signal Flow



Example of High Speed Layout: Other Layers





Layer 2: Signal GND Plane

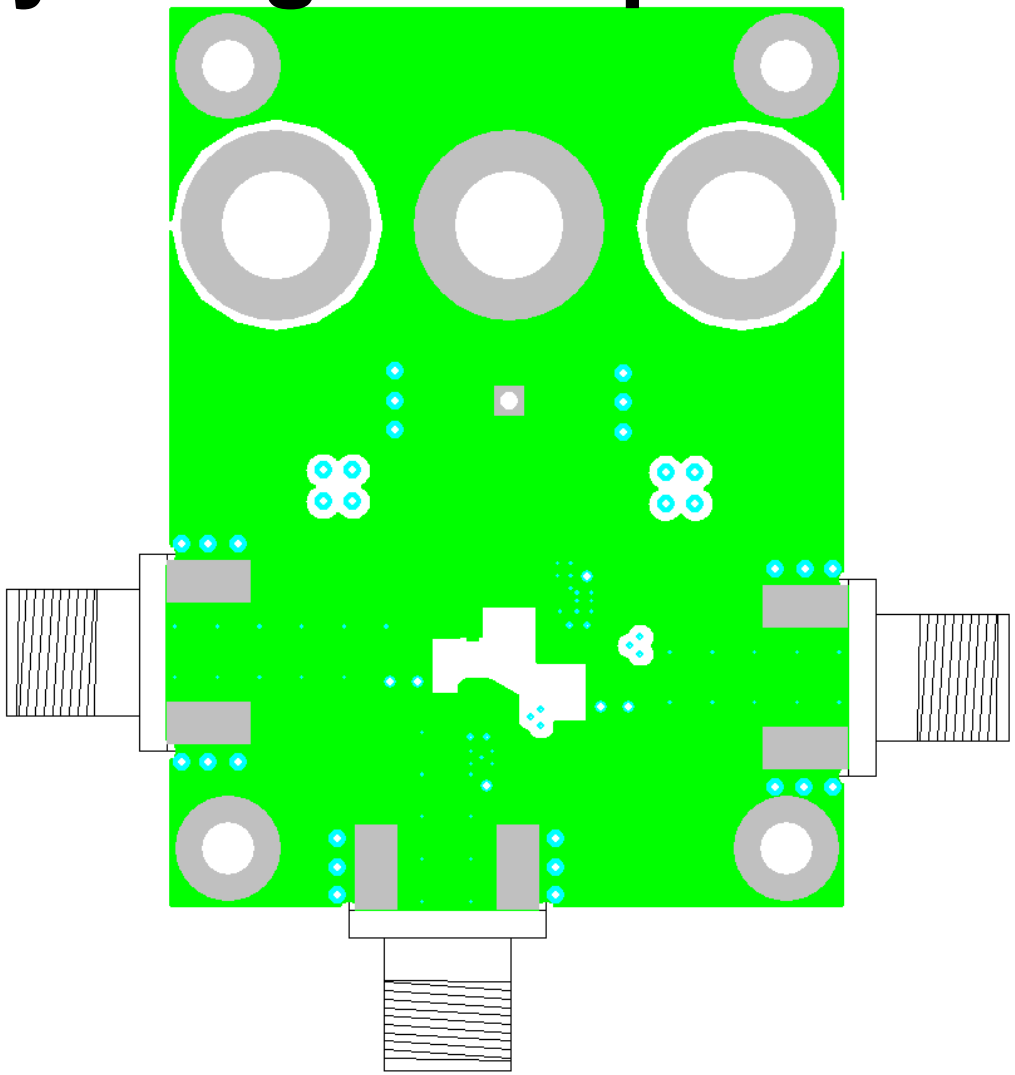
GND Plane Next To Signal Plane for Continuity in Return Current

Layer 3: Power Plane

Notice Cut-Out in Sensitive areas near Amplifier on ALL planes.

Example of High Speed Layout: Bottom Layer – ground plane

1. Solid GND plane to minimize inductance.
2. Layer-2 GND plane and Bottom Layer form excellent bypass capacitor with Power Plane.
3. All Signals are on Top Layer to minimize the need for signals to flow through vias.
4. Multiple Vias Everywhere – No spokes
5. Cut-Out around Amplifier to reduce Stray Capacitance



Agenda

1) General Considerations
   a) Models: Resistors, Capacitors, Inductors, and Circuit Board
2) High Speed Op Amp Layout
   a) Input and output considerations
   b) Signal routing
   c) Bypass capacitors
   d) Layout examples
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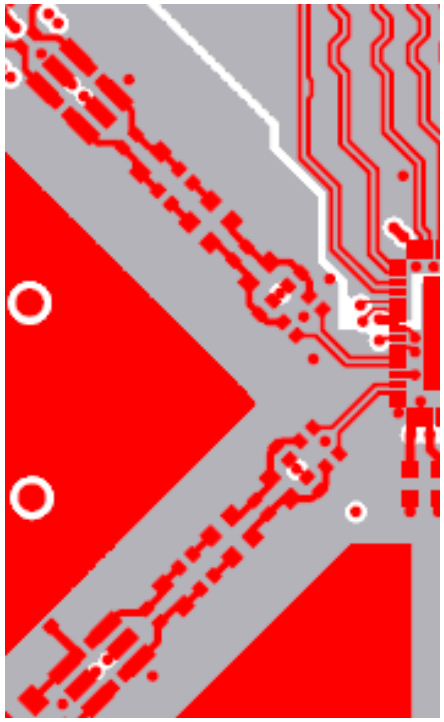
   b) Power Supply Filtering
   c) Power Supply Bypassing & Grounding
   d) Layout Tricks to Reduce EMI

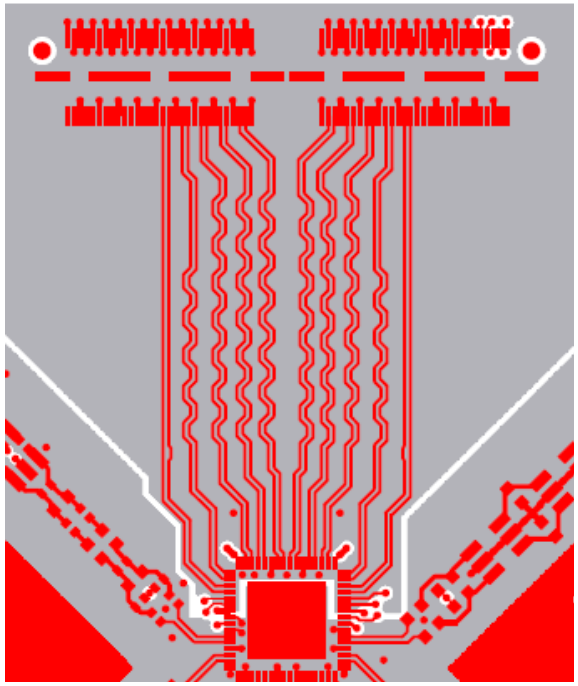
ADC inputs



Ex. TSW1070

- The analog inputs represent the most sensitive node on the high speed ADC.
- For a 2Vpp ADC input, and a 86dB SFDR target, the input error must be under 0.1mV to not degrade the converters performance.
  - Typical coupling sources:
    - ADC outputs (CMOS ADC outputs)
    - Unterminated clock lines
- Keep maximum separation between adjacent channels to minimize crosstalk.
- Modern ADCs have differential inputs, which should be routed tightly coupled and symmetrically routed.
- To minimize stray capacitance, analog anti-aliasing filter could have the ground plane below it notched out.
- Terminate analog inputs and clock inputs with terminations placed at the device input pins.

ADC Outputs



Ex. TSW1070

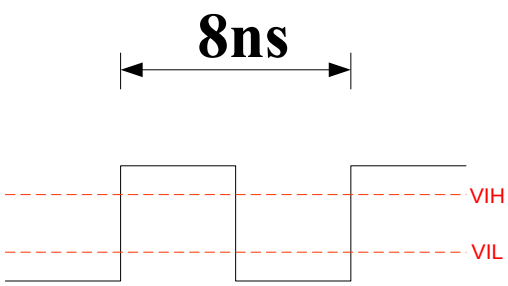
- **Output lengths should be matched.**

$$v = \frac{c}{\sqrt{\varepsilon_r}}$$

FR4=0.18ps/mil

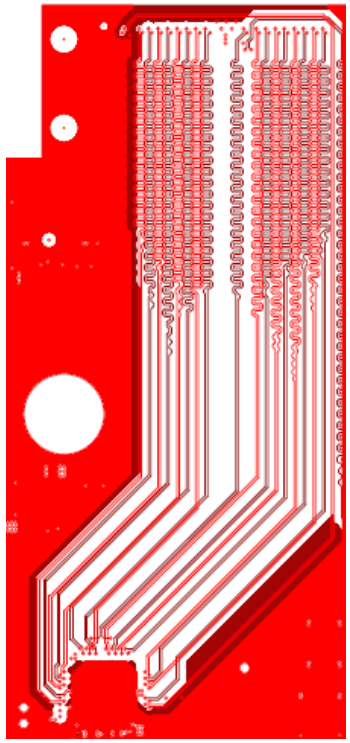
  - **FR4, 50mil matching ~ 9ps skew**
- **LVDS Outputs (preferred)**
  - **Constant current output**
    - **Minimizes coupling back to analog input.**
    - **Minimizes EMI**
  - **100 ohm termination resistor should be physically located at the receiver inputs.**

ADC Outputs cont'd - CMOS



- **CMOS Outputs**
  - At higher frequencies, parasitic board capacitance prevents full signal swing.
  - Procedure
    - Extract board resistance and capacitances (parasitic from stackup and receiver input capacitance)
    - Calculate RC time constant (67%) $\tau = R * C$
    - Compare with receiver VIH, VIL
    - Conduct a timing analysis.
  - Several TI HS ADC have programmable output drive strengths.
    - For best SNR, use the least drive strength required to satisfy timing
  - To minimize parasitic capacitance, route CMOS outputs as micro strip traces.

DAC Inputs



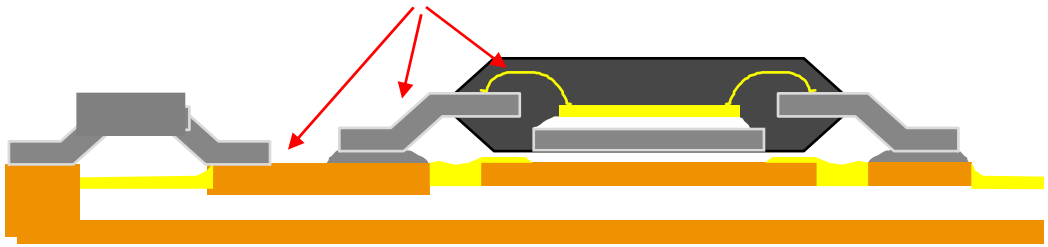
- LVDS inputs (DAC5682)
  - Should be routed as differential pairs.
  - Should have a characteristic impedance of 100 ohms.
  - CLKIN and Data inputs should be matched.

Decoupling

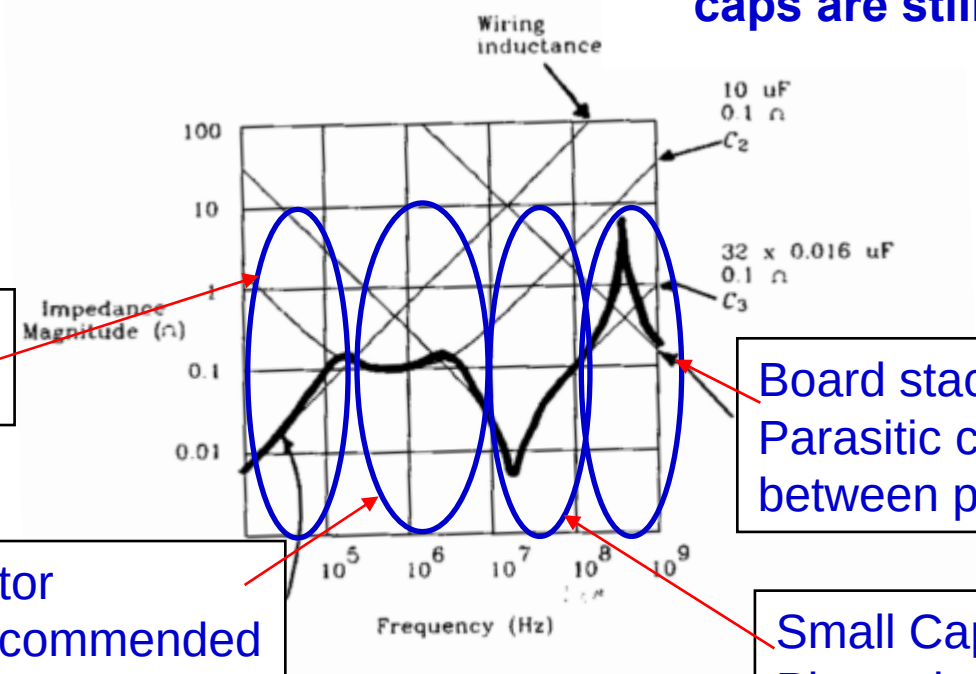
- When a load is suddenly applied,
  - The circuit tries to suddenly increase its current
  - Inductance in the power supply line acts to oppose that increase
  - The voltage of the power line sags
- Decoupling or bypass caps supply short bursts of current when the IC needs it
  - Rule of Thumb suggests one decoupling cap per power pin.
  - Many ADC's now have decoupling built into the device

Decoupling

Series Impedances



- **Multiple series impedances (bondwire, pin, trace) will act to reduce the effectiveness of the decoupling caps**
- **A lot of high speed amps and data converters have on chip capacitors to help, but external caps are still recommended**



Power Supply
Ferrite Bead

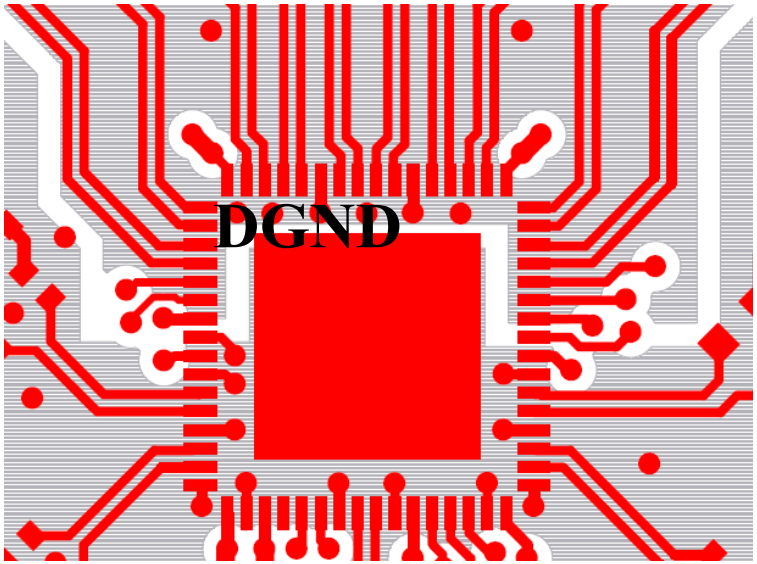
Board stack up
Parasitic capacitance
between planes

Bulk Capacitor
Low ESR recommended

Small Capacitor Array
Place close to power pins

Source: Johnson
High Speed Digital Design

Split Ground Planes

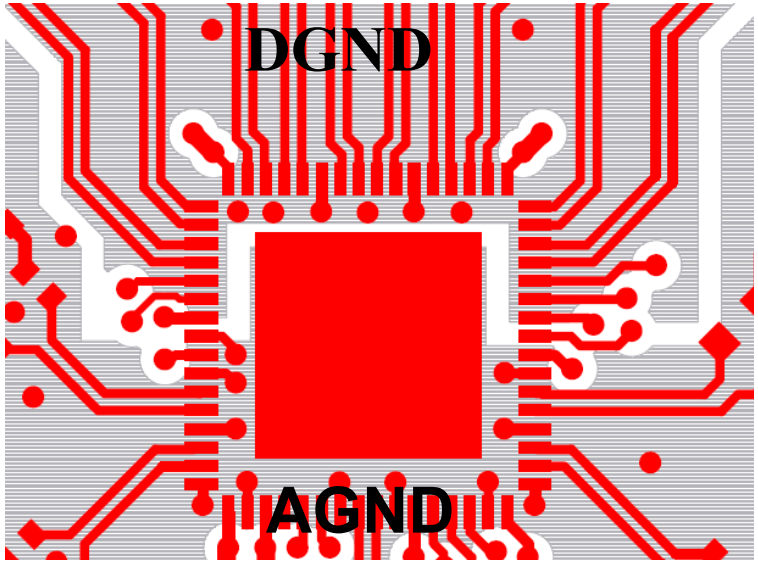


AGND

- **Reasons to split the ground plane:**
  1. Precise control over current flows back to the source.
  2. Isolate sensitive analog circuitry from digital switching.
  3. ADC CMOS interfaces.
- **How to perform the split:**
  - Identify each pin as either a digital pin or an analog pin.
  - Perform the split such that each pin has it's respective GND plane underneath the pin.

Probably OK for lower speed design with frequencies below 1MHz

Split Ground Planes



- **Reasons to not split the ground plane:**
  1. **Strong chance for error in making the split.**
  2. **Could cause a large inductive loop which gives rise to noise.**
- **FACTS:**
  - **With proper decoupling and grounding, many single GND planes perform as good as split ground planes.**
  - **LVDS outputs/inputs minimize the need to split the plane.**

Generally best to not split ground plane in very high speed design and you should plan to reconnect if you do

Total Data Converter SNR Performance

SNR contributions:

- **Quantization noise:**
  - **6 * N{# of bits} + 1.76 dB**
- **Clock jitter**
  - **Jitter or Phase Noise Performance**
- **Aperture jitter**
  - **Value extracted from the datasheet**
- **Thermal Noise**
  - **Value estimated from SNR performance from the datasheet at lowest IF**

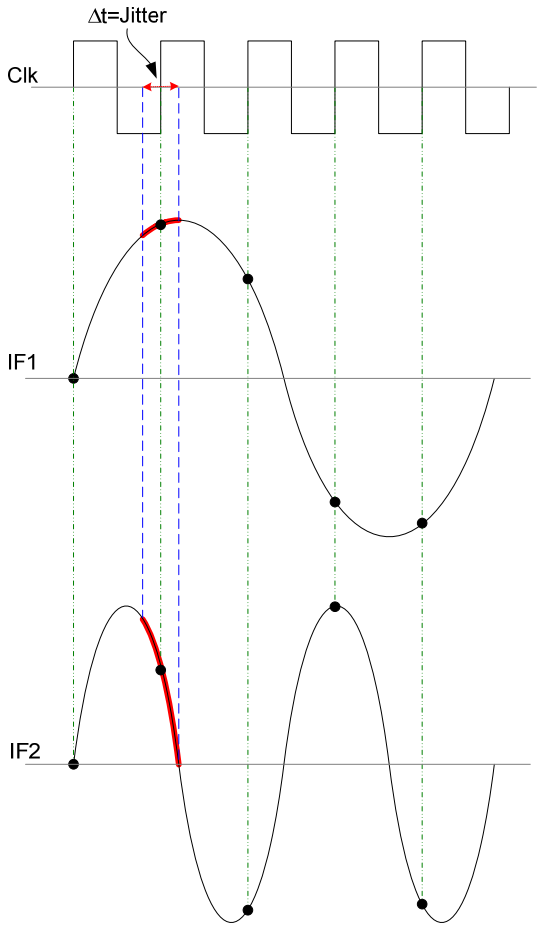
Total SNR is RMS sum individual contributions

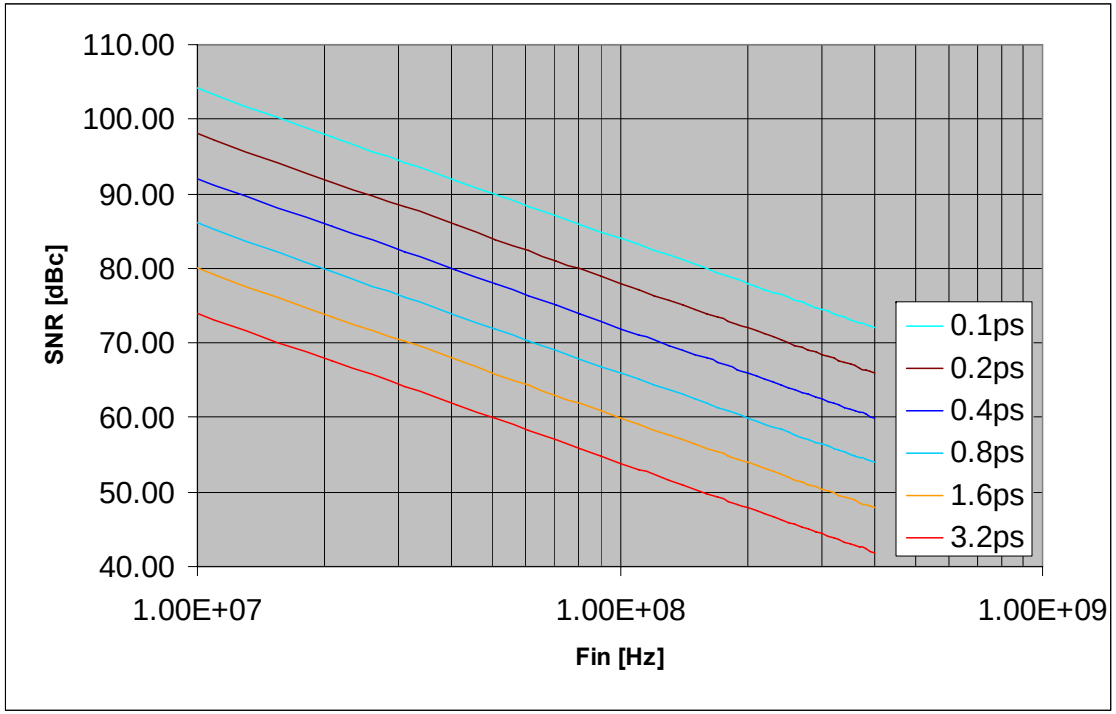
$$SNR_T = \sqrt{\sum_i \left[SNR_i\right]^2}$$

Clock jitter is only term the circuit designer can manage

Jitter SNR vs Analog Input Frequency

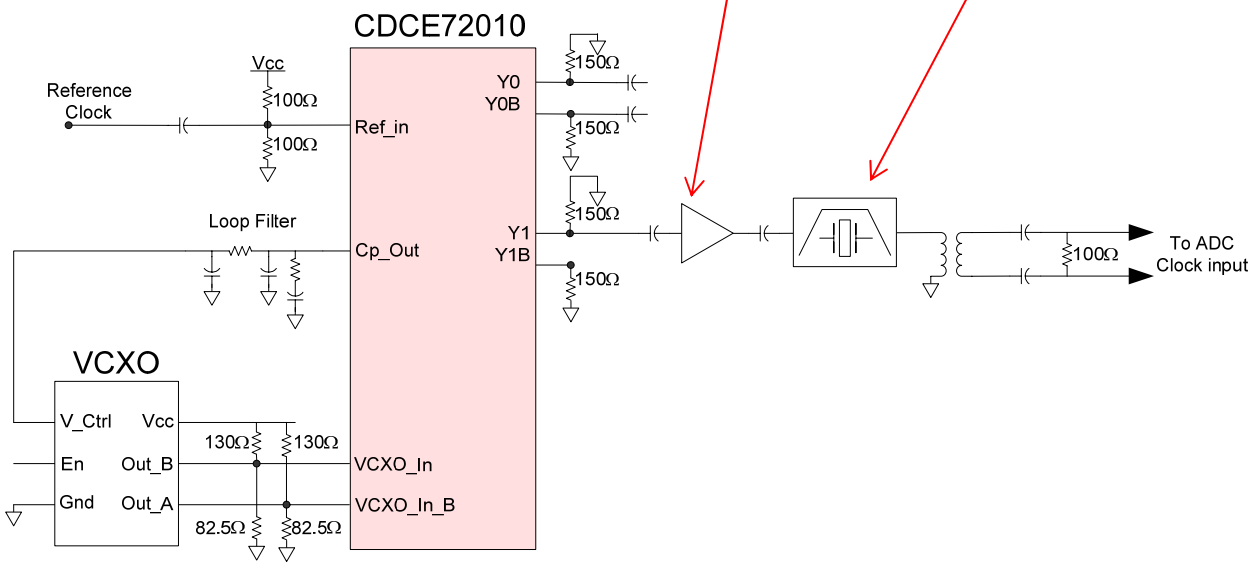
- **Jitter SNR is dependent on input frequency**
- **Higher input frequencies lead to tighter jitter requirements**





Band Limit Clock to Improve Phase Noise and Jitter

- **Clock jitter is due to noise integrated over clock input BW**
  - **Clock input BW can be up to 1 GHz for high speed converters**
- **Add narrow band Crystal filter on clock for best jitter**
  - **Small SMT Crystal Filter devices available with narrow BW**
  - **May require amplifier to compensate for insertion loss**



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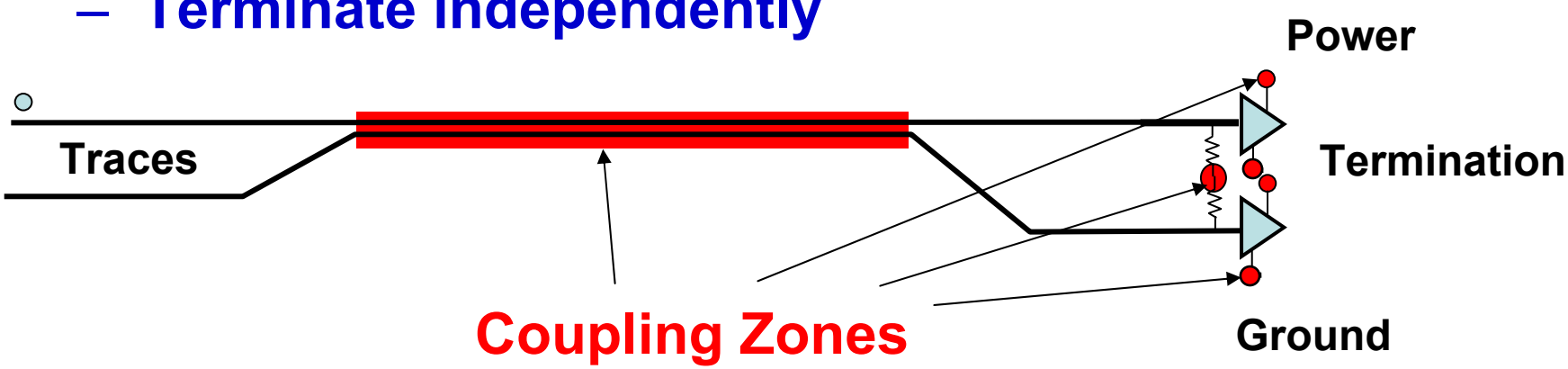
   c) Line Termination
   d) Reducing EMI

Coupling, Interference, or Cross Talk

- Coupling , Interference, or Cross Talk is when one signal affects another
- General rules to reduce coupling:
  - Increase isolation between traces
  - Isolate the power supplies (bypass/filter)
  - Use low impedance ground reduce ground bounce (planes)
  - Terminate independently



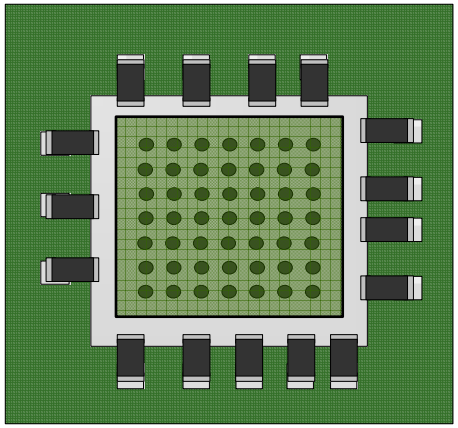
Minimizing Input Coupling

- Keep maximum separation between inputs
- Terminate independently
- Differential Reference inputs should be tightly and symmetrically routed
- Terminate close to the device input pins
- Route Clocks on internal layers to minimize EMI

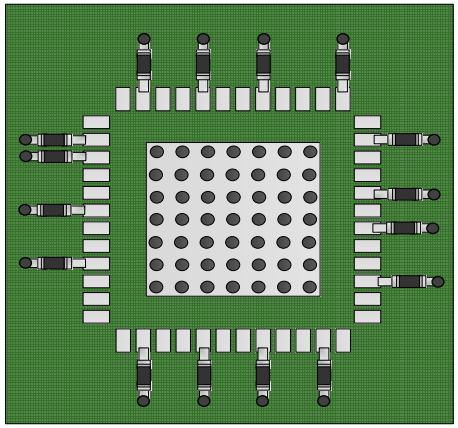
Minimizing Output Coupling

- Bypass output buffer power pins on top layers
- Match trace impedance between channels
- Match trace lengths to minimize skew between channels
- Differential outputs should be tightly and symmetrically routed
- Single ended LVCMOS may need source termination for better integrity and reduce EMI
- Route clocks on internal layers to minimize EMI

Clock Power Supply Decoupling



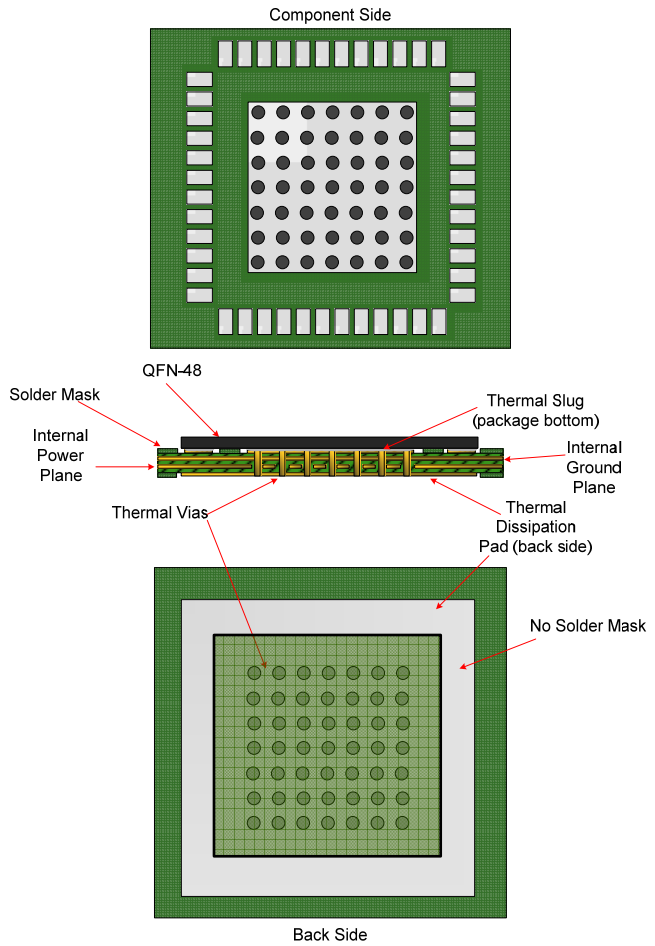
Back Side



Component Side

- **Place all bypass capacitors as close as possible to VCC Pins**
  - **Bypass capacitors shunt the noise generated by device to ground and reduces noise coupled via VCC**
  - **Bypass capacitors provide low impedance power source**

Clock Supply Grounding

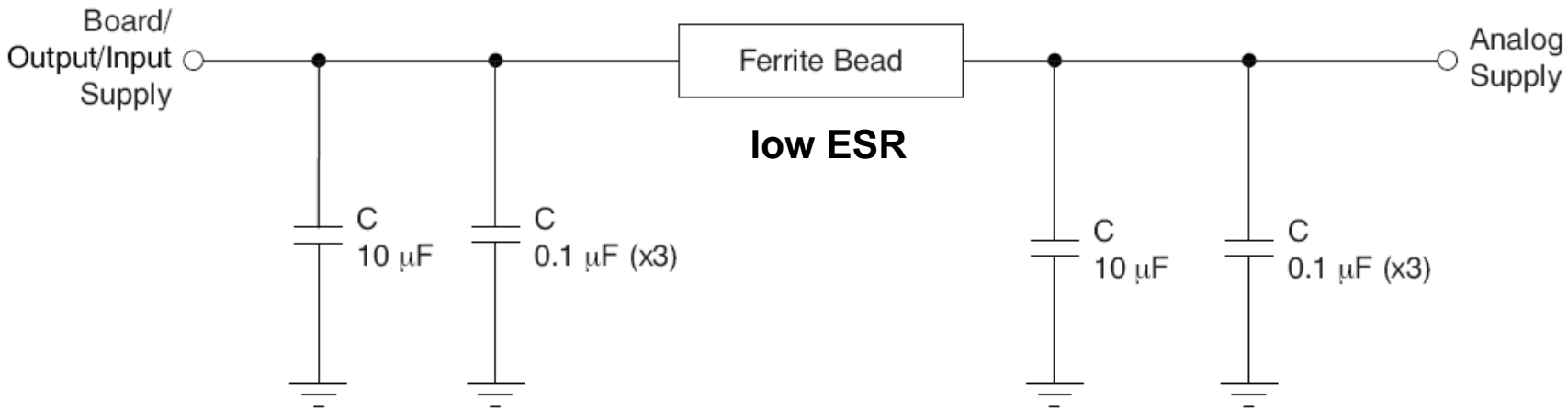


- Ground Bounce is common in a clocking Devices since all the outputs are sharing the Same ground and they are switching together

- Make sure that the Grounds On the Clocking device is grounded with minimal inductance to reduce Ground bounce

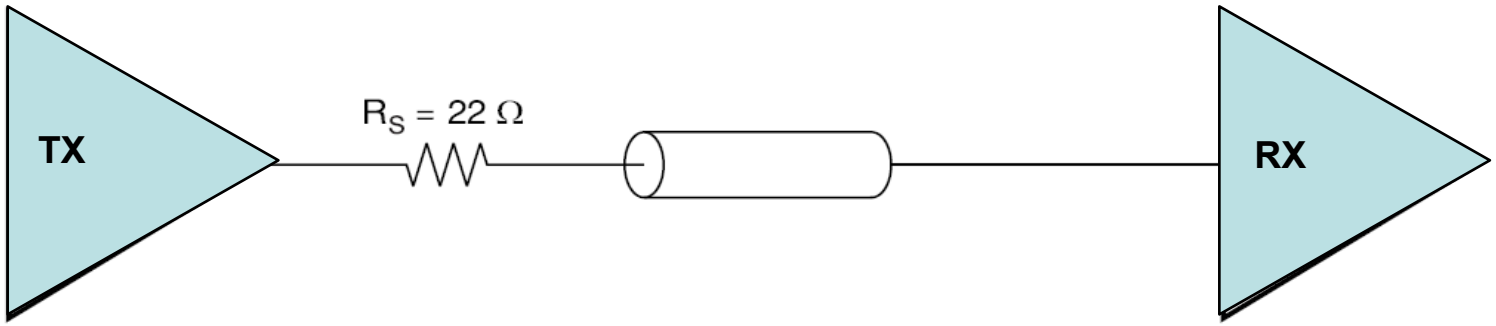
Power Supply Filtering for Critical Applications

- LC Low pass filtering used to provide better power supply isolation between sensitive blocks
  - PLL-based frequency synthesizers are very sensitive to noise on the power supply, especially analog-based PLLs
  - Must reduce noise from power supply when jitter/phase noise is critical in applications
- Rule of thumb: LPF ≤ 1/10 Bandwidth
  - Example: PLL with 400 kHz bandwidth, place LC corner ≤ 40 kHz



Termination: Single Ended LVCMOS Clock Outputs

- Single ended LVCMOS may need source termination to reduce EMC
- 22 Ω series resistor should be located at the TX outputs



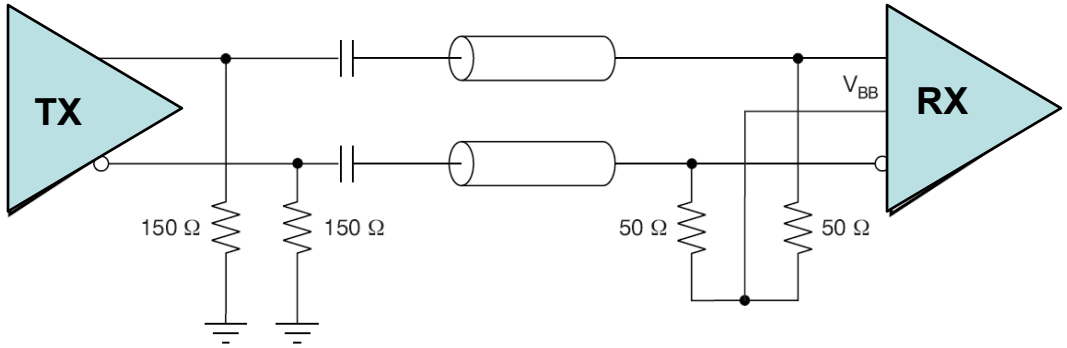
LVCMOS

Differential Clock Outputs Are Better

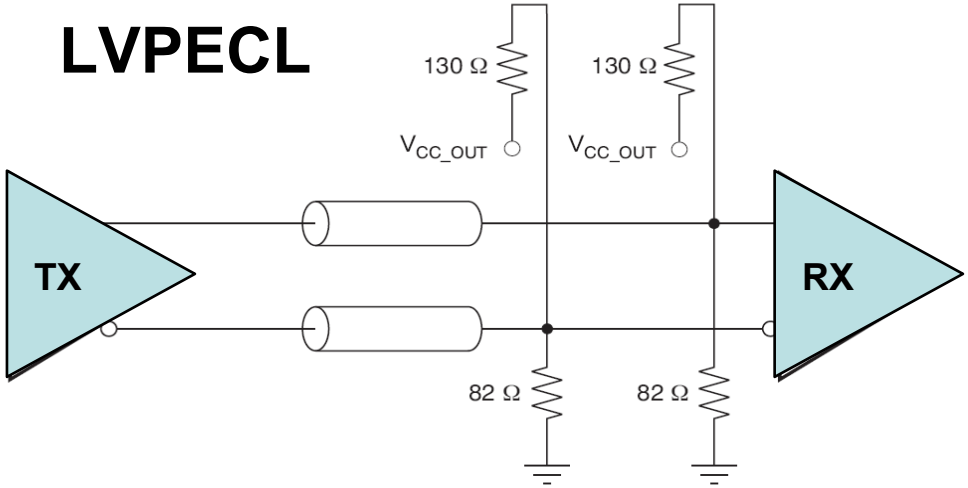
- Higher isolation from common mode noise
- Better protection against EMI
- Minimizes coupling
- Allows higher frequency operation

Termination: Differential LVPECL Clock Outputs

- LVPECL needs to have a termination to V_{CC} – 2V
  - **AC coupling**: termination resistors should be used at TX output pins and RX input pins
  - **DC coupling**: termination resistors should be RX input pins



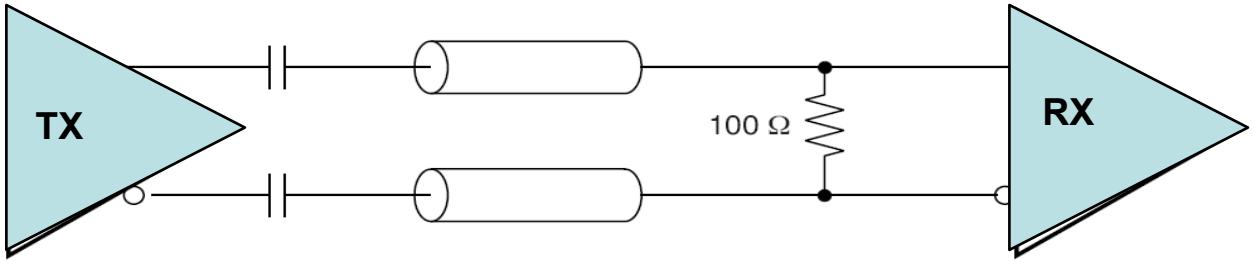
LVPECL



Termination:
Differential LVDS Clock Outputs

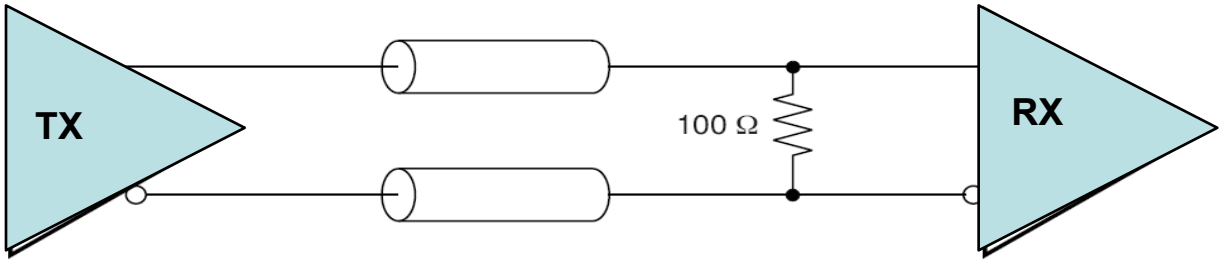
- **LVDS is generally specified as DC coupled**
  - **although most people these days use AC coupling with it**
- **For both AC and DC coupling, 100 Ω termination resistor should be located at the receiver inputs**

AC coupling



LVDS

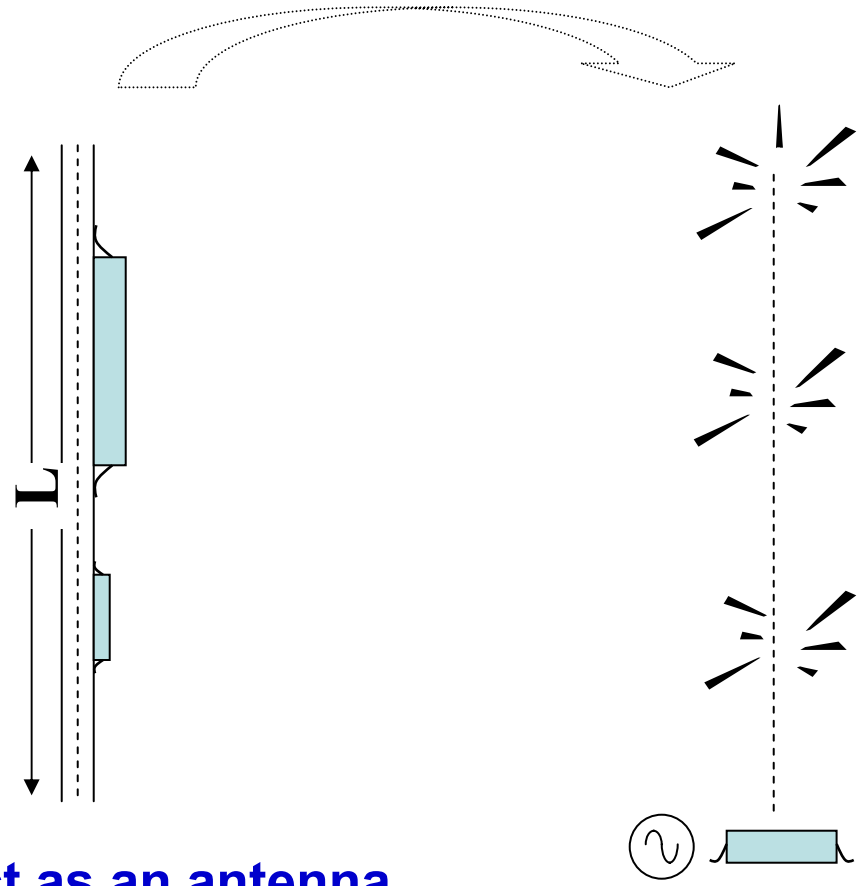
DC coupling



AC Coupling vs DC Coupling

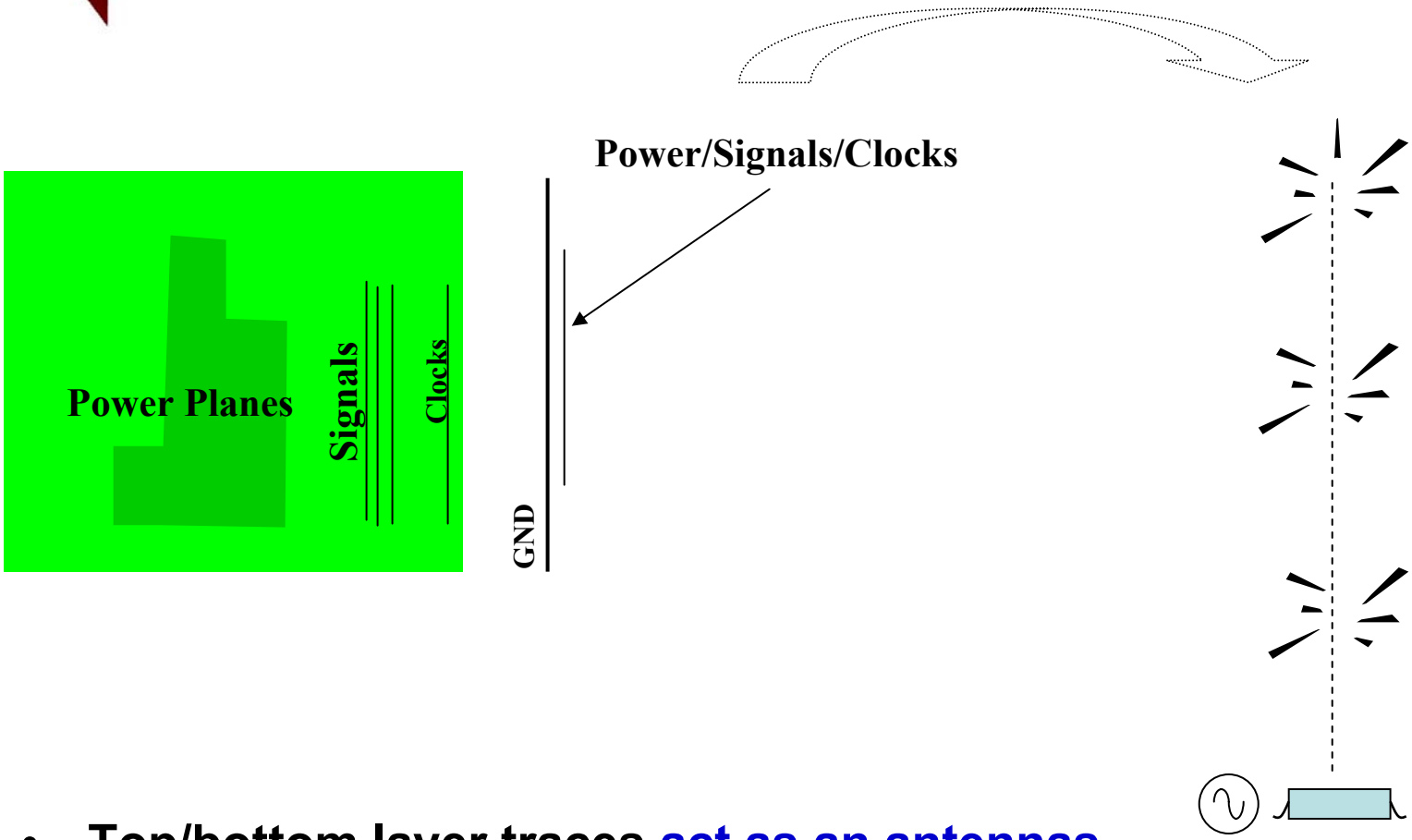
- AC coupling can be uses when signal is DC balanced (equal duration for zeros and ones)
  - Allows for different common mode biasing voltage in RX than the TX
- DC coupling is used when date is random, or very slow signals that have large DC components

PCB Edge Acts as Antenna



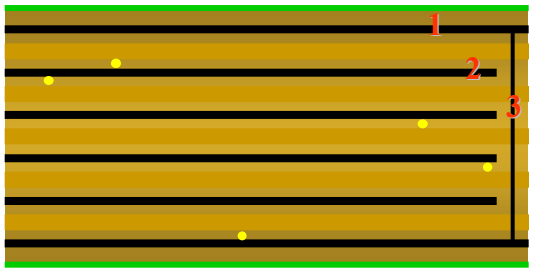
- PDB edge traces **act as an antenna**
- Radiation increases as frequency approaches multiples of $\lambda/4$
  - Remember $\lambda/4$ **is quarter wave antenna**

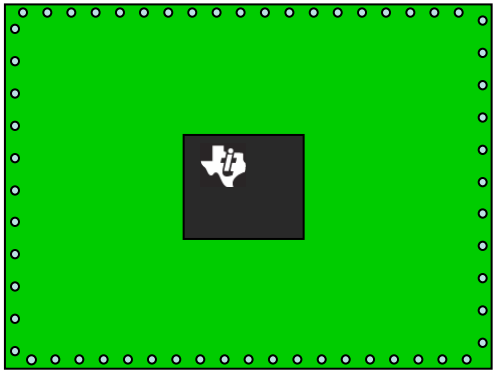
Top and Bottom Traces Are Antennas



- Top/bottom layer traces act as an antennas
- Radiation increases as frequency approaches multiples of $\lambda/4$
  - Remember $\lambda/4$ is quarter wave antenna

Reduce PCB Trace Radiation





Creating a faraday cage on the PCB to reduce PCB trace radiation:

1. Make top and bottom layers GND
2. Inner layers VCC planes and signal traces should be retracted from the board edge
3. GND Layers should be via stitched to create the PCB faraday cage
   a) Spacing ≤ $\lambda/10$ of the highest harmonic

Clocks are usually biggest source of EMI in system

The End

- Thank You
- Are There Any Questions?