TI Innovation Day France 2010

Dernières évolutions et tendances applicatives des convertisseurs rapides

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Field Application Engineers

Texas Instruments

Agenda :

- Portfolio overview & trends by application
- Tools
- Wideband digital predistortion Demonstration based on R&S equipments

TI Data Converter Portfolio

Analog-to-Digital			Digital-to-Analog	Audio	Embedded ADC
Delta-Sigma (Oversampling)	Successive Approximation (SAR)	Pipeline (Highspeed)	String R2R Current steering	ADC DAC CODEC	Embedded Processing
ADS10xx … ADS12xx **12 to 31 bit up to 128 kSPS** **ADS16xx**	**ADS72xx … ADS85xx** **8 to 18 bit up to 4 MSPS**	**ADS4xxx … ADS6xxx** **10 bit to 16 bit up to 1 GSPS**	**DAC56xx … DAC98xx** **8 bit to 18 bit 0.1-20 µs settl. time up 1 GSPS**	**ADC** **PCM18xx** **PCM42xx** **TLV320xx** **DAC** **PCM16xx** **PCM17xx** **TLV320DACxx** **CODEC** **TLV320AICxx**	**C5000™** **10 bit up to 2 MSPS** **Stellaris®** **ARM® Cortex™-M3** **10 bit up to 1 MSPS** **C2000™** **Delfino™** **Piccolo™** **12 bit up to 4.6 MSPS** **MSP430™** **12 and 16 bit up to 200 kSPS**
Low frequency signals at high resolution Temperature Pressure, Level Seismic ATE Scientific Instruments	Industrial process control Motor control 3 phase Power Control Multi Axis positioning Power Quality	Communication Imaging Defense Medical Imaging Test and Measurement	Industrial Application Test and Measurement Digitally controlled calibration Communication		
Integrated Features PGA, current sources, references, MUX, modulator only Isolation	**Integrated Features** Simultan. sampling, bipolar inputs, references, MUX	**Integrated Features** Digital processing for filtering, decimation 1/f noise reduction interleaving ready	**Integrated Features** Voltage output Current output Multiplying references bipolar output Multichannel		
$0.50 to $35.00	**$0.50 to $30.00**	**$2.50 to $800.00**	**$1.00 to $40.00**	**$1.00to $30.00**	

Dev. Tools **ADC Pro**  **DAC Tool (DXP)**  **Pipeline ADC Capture Card** 

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Data Converter Markets & Applications

Industrial

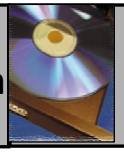
Applications
- Sensors
- Motor Control
- Test Equipment
- Programmable Logic Controllers

Market Drivers
- Low Noise
- High Accuracy/ Resolution
- Low Offset
- Low Drift
- Power
- Packaging

Communication

Applications
- Optical Networking
- Basestations
- Wireless Terminals
- Cable Modem
- WiMax

Market Drivers
- Speed
- Resolution
- Bandwidth
- Gain
- Power
- Integration



Multimedia

Applications
- Portable Media Players
- Digital Video Recorders
- Media Gateways
- Digital Cameras
- PDAs

Market Drivers
- Power
- Size
- Integration
- Cost

Medical

Applications
- ECG Electrocardiogram
- CT Scanner
- Infusion Pump
- Pulse Oximetry
- Ultrasound System

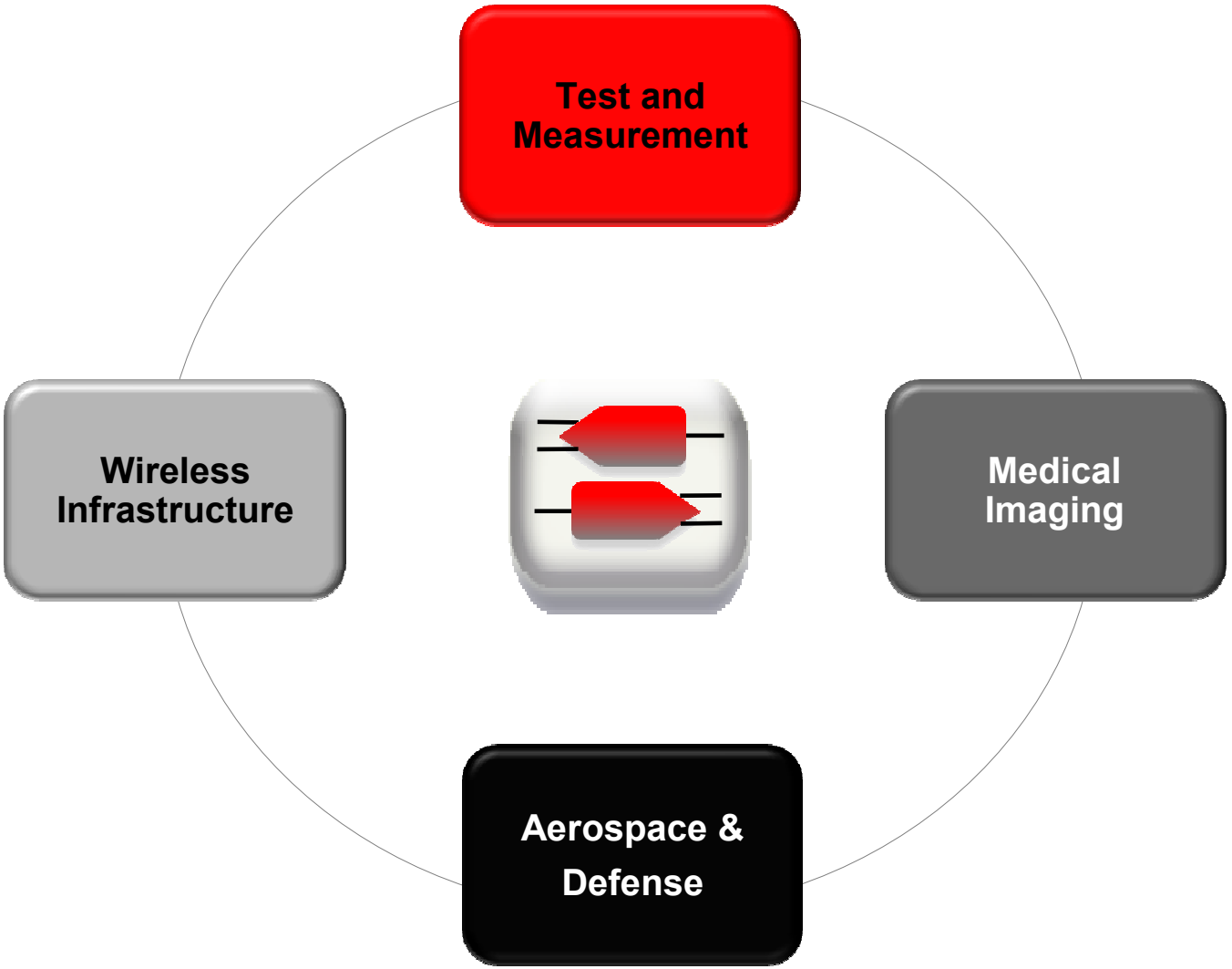
Market Drivers
- Resolution
- Sampling Rate
- Power
- Size
- Integration
- Cost

Space & Defense

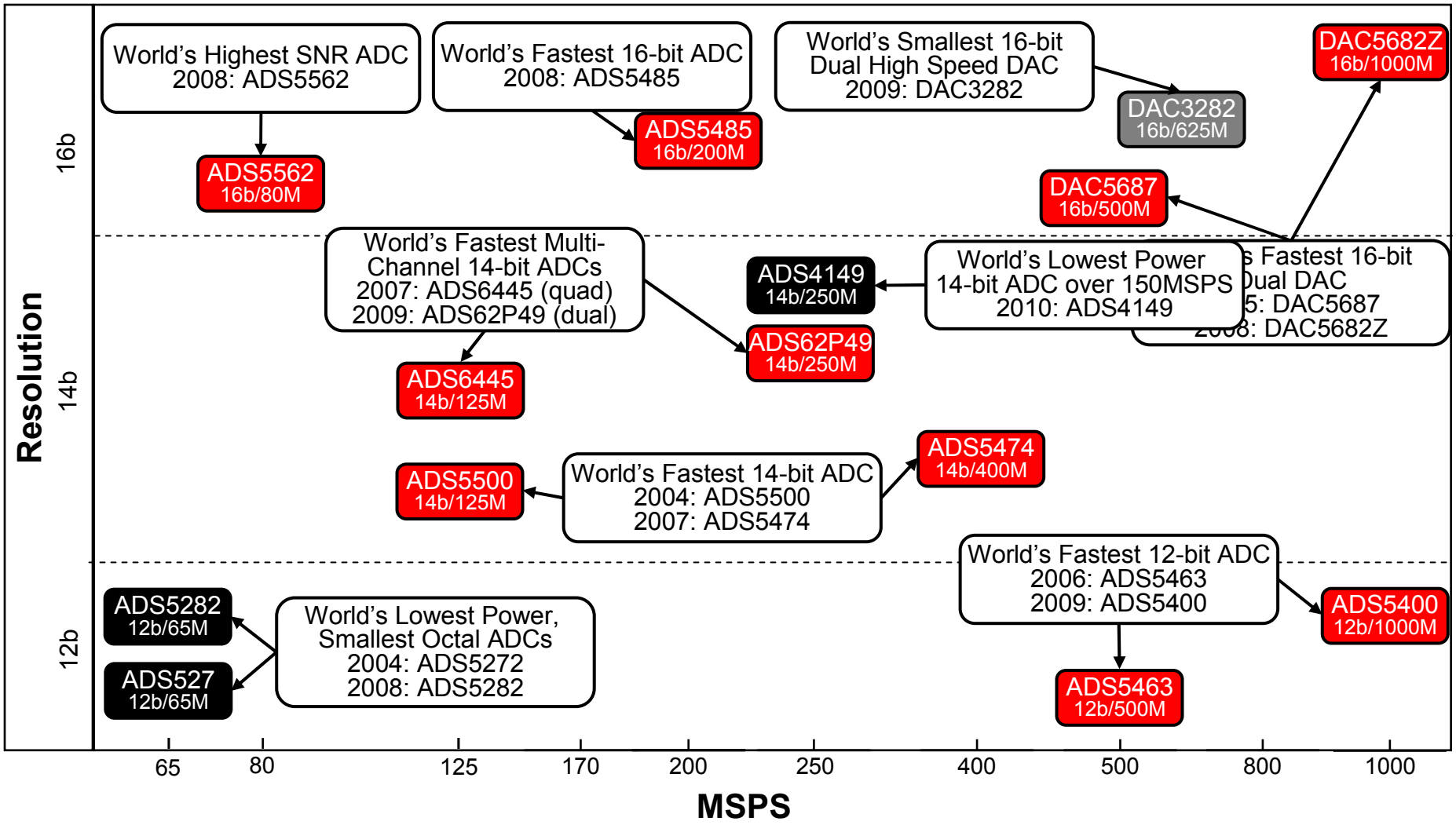
Applications
- Radar
- Software Defined Radio
- Signals Intelligence
- Satellite Communications
- Data Links

Market Drivers
- Speed
- Resolution
- Bandwidth
- IF Performance
- Power
- Integration

Primary Markets for High Speed Converters



History of High Speed, High Density and Low Power Leadership



Leadership in Design Drives Product Innovation

ADS5400
Fastest 12-bit ADC
1 GSPS

- Defense
- Data Acquisition
- Wide-band Wireless

ADS4149
14-bit, 250MSPS
Only 260 mW
Power Consumption

- Wireless Comms
- Portable Test
- Portable SDR

DAC5682Z
Dual 16-bit, 1GSPS
-pin QFN

- Wireless Comms
- Arbitrary Waveform Generation (AWG)

ADS5562
16-bit, 80MSPS ADC
84 dB SNR

- Medical Imaging
- Data Acquisition
- Portable Test

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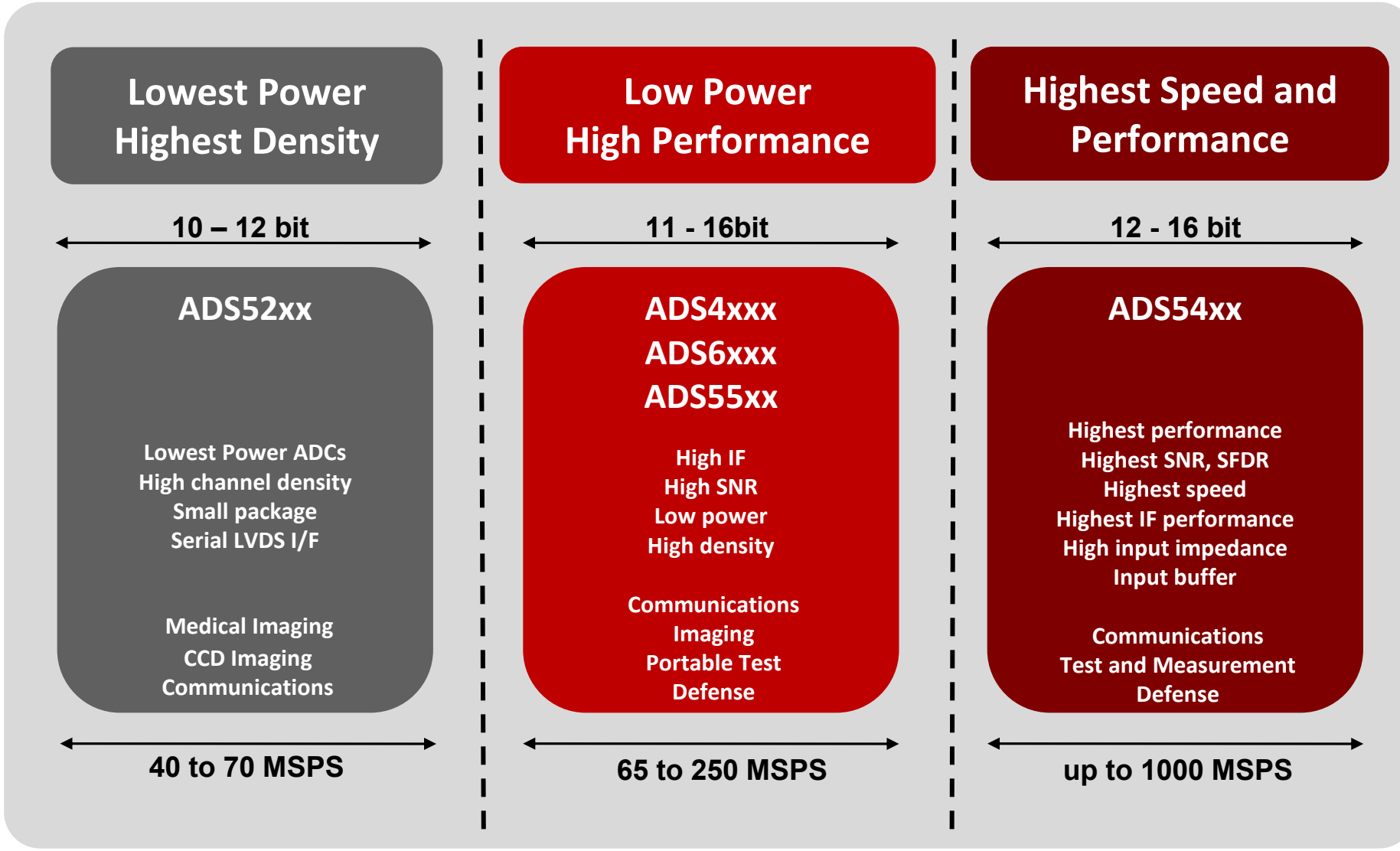
ADC

High Speed Pipeline ADC Portfolio



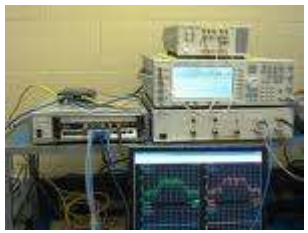
TI High Speed Converters for

Aerospace and Defense Systems

&

High Speed Test and Measurement

➔ **Speed, Performance, Power and Density**



High Speed, Wideband ADCs for :

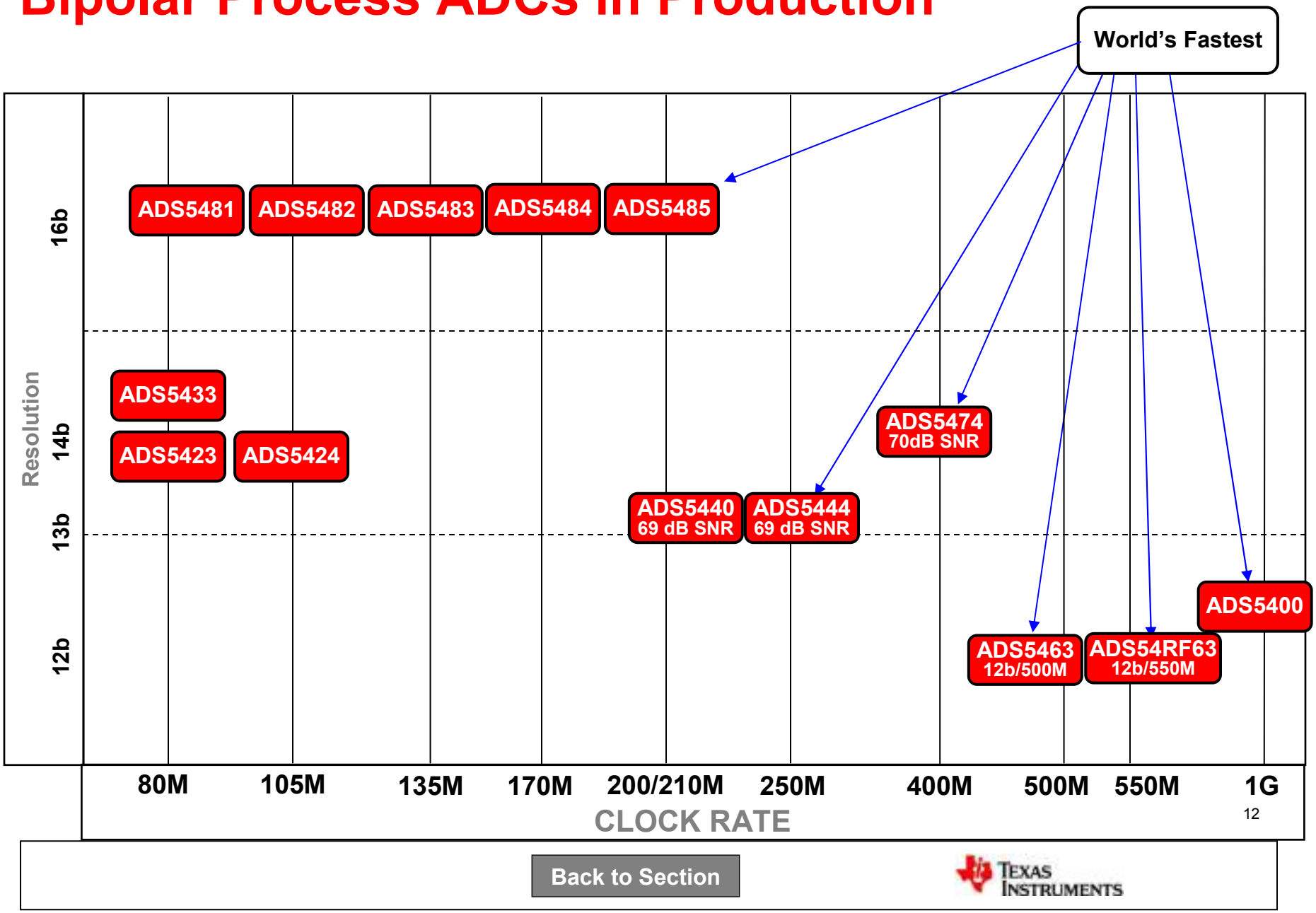
- Radar, Signals Intelligence, Electronic Countermeasures and Jamming

- Digitizers, Wireless Test Equipment and Spectrum and Network Analyzers

  - Highest speed 12-, 14- and 16-bit ADCs
  - Wide analog input bandwidths – up to 2.1GHz
  - Highest SNR, SFDR and ENOB performance available

- **ADS5400** – 12-bit, 1GSPS ADC
- ADS54RF63 – 12-bit, 500/550MSPS ADC for high IF/RF
- ADS5474 – 14-bit, 400MSPS ADC
- ADS5493 – 16-bit, 130MSPS ADC with exceptional SFDR
- **ADS5485** – 16-bit, 200MSPS ADC

Bipolar Process ADCs in Production



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ADS5400

Fully Buffered 12-bit, 1 GSPS ADC with 2.1GHz Analog Bandwidth

Features

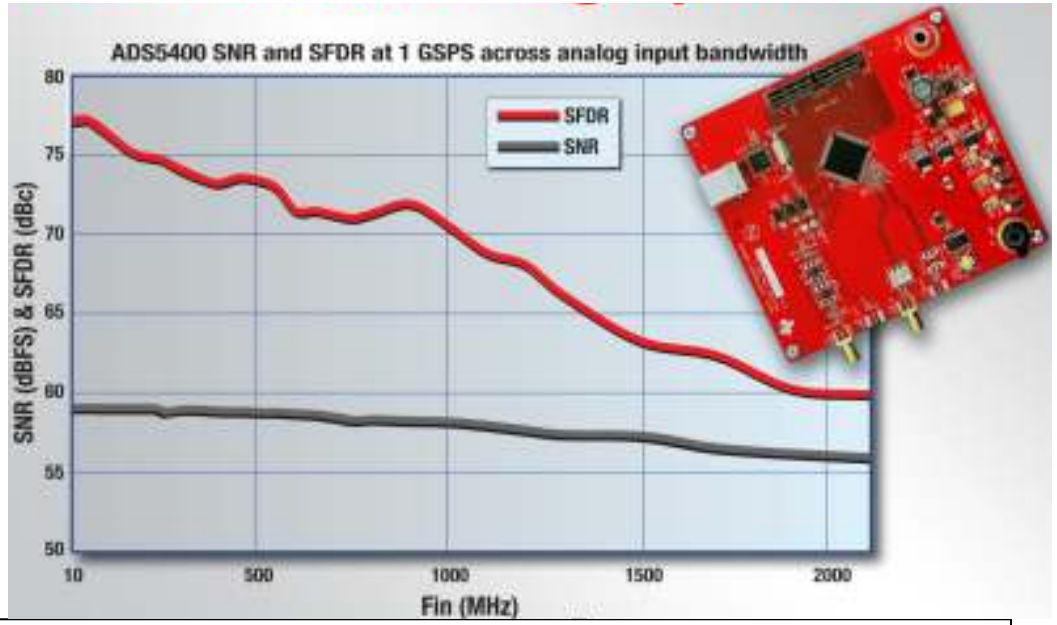
- 12-bit resolution with 1 GSPS sample rate
- High dynamic performance from DC to 4th Nyquist
  - 59 dB SNR, 75 dBc SFDR at 250MHz
  - 58 dB SNR, 70 dBc SFDR at 1000MHz
- On-chip inter-leaving trim adjustments
  - For gain: range 1.5-2.0Vpp, resolution 120uV
  - For offset: range +/-20mV, resolution 120uV
  - For clock phase: range +/-50ps, resolution 200fs
- 100 pin TQFP package (16mm x 16mm)
  - User selectable straight or de-muxed DDR LVDS outputs
- TI BiCom3tm Technology
- 2.2 Watt Power Dissipation

Benefits

- *Highest speed 12-bit device available provides un-matched bandwidth with high performance*
- Highest SNR, SFDR and SINAD available for greater than 200MHz bandwidth systems
- Enables multi-gigasample digitizers to maintain 12-bit resolution and performance
- Flexibility of reduced I/O speed or pin-count
- Works well in high temperature and high radiation environment

Applications

- Radar and Guidance Systems
- Defense Electronics Digitizers
- Test, Measurement and Instrumentation
- General Purpose High Speed Digitizers
- Wireless Communication:
  - Satellite Modems
  - Wideband I/Q receivers
  - Wireless back-haul



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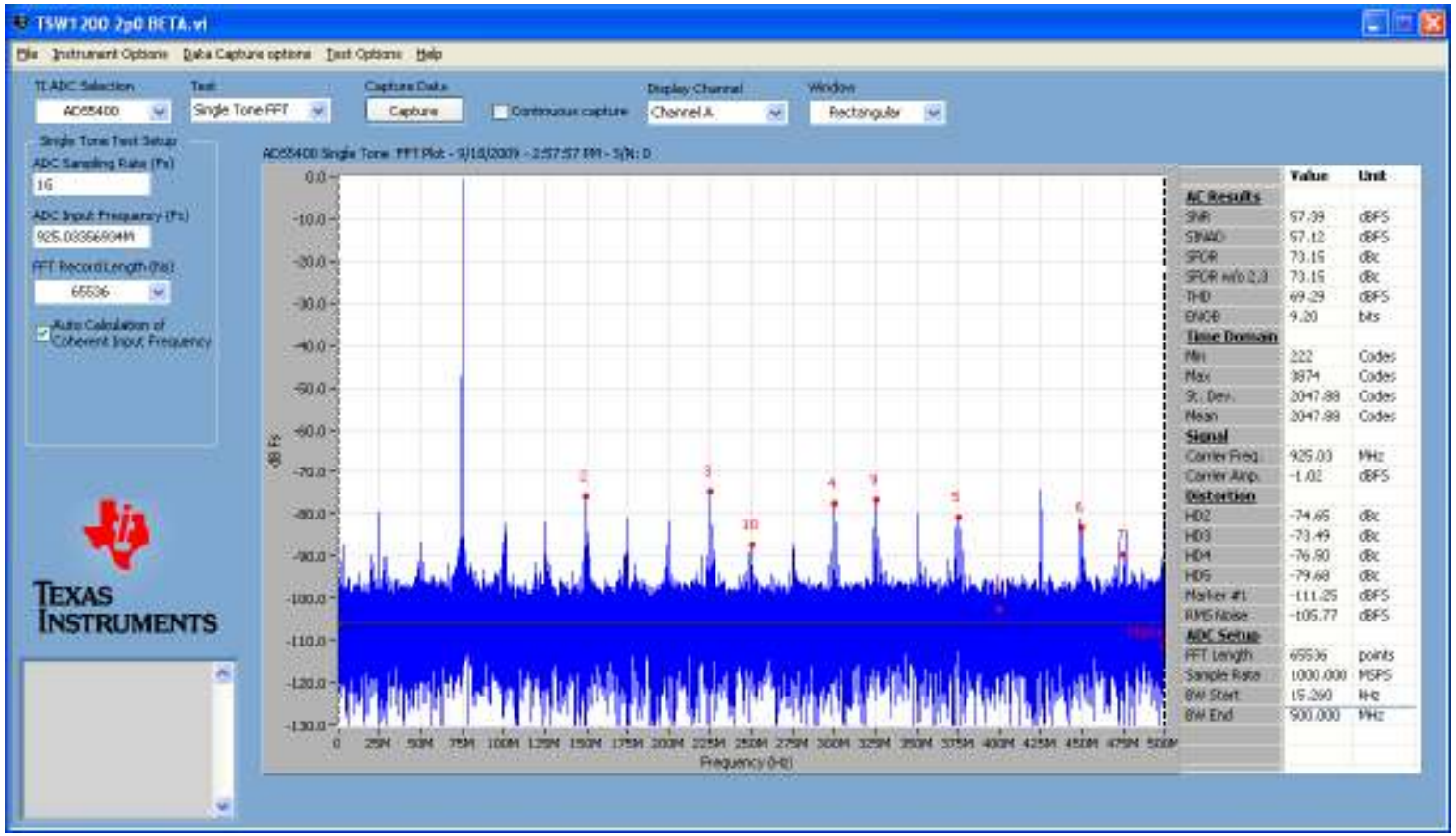
Delivering high dynamic performance across wide input frequencies



- **The ADS5400 provides 57 dB SNR with 73 dBc SFDR at a 925MHz IF**
- **Well-suited for wide bandwidth, under-sampling applications – as high as 1500MHz!**

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ADS5485

Fully Buffered 16-bit, 200 MSPS ADC

Features

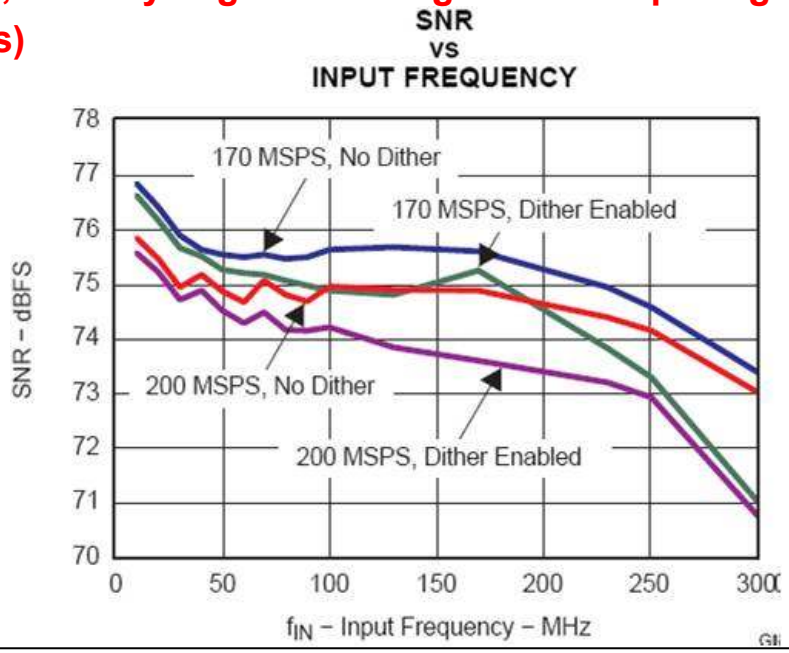
- High Performance with Fully Buffered Input
  - 75.0 dBFS SNR, 90dBc SFDR – 30MHz
  - 74.8 dBFS SNR, 85 dBc SFDR – 130MHz
- Selectable Dither for Enhanced SFDR at Lower Ain
- Wide Input Swing: 3.0Vpp
- TI BiCom3tm Technology
- Small Form: 9x9mm QFN pin Compatible to ADS5481, ADS5482, ADS5483 and ADS5484 (80 – 200 MSPS ADCs)
- 2.2 Watt Power Dissipation

Benefits

- *Best 200 MSPS SNR, SFDR and SINAD for greater receiver sensitivity*
- Higher dynamic range for -5 to -25 dBFS inputs
- Allows for the greatest SNR or higher SFDR with smaller input swing
- High reliability and latch-up immunity
- Easy migration to higher/lower speed grades

Applications

- Wireless Communication:
  - Baseband I/Q receivers
  - Software Defined Radio
  - Multi-carrier GSM
- Test, Measurement and Instrumentation
- Radar and Guidance Systems



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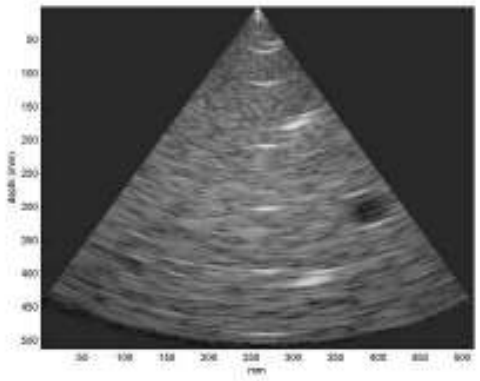


TI High Speed Converters for Medical Imaging

➔ **Low Power, High Density and High Performance**

TI for Medical Imaging:

- Low Power 8-channel ADCs for Ultrasound and MRI
  - Lowest Power Consumption
  - High Density – 8-channels in one 9mm x 9mm package
  - 10- and 12-bit resolutions
  - **ADS5282 & AFE58xx**
- High SNR ADCs for MRI Coil Receivers
  - 16-bit Resolution with up to 84 dB SNR
  - Small size – only 7mm x 7mm
- Low Power, High Speed Single and Dual ADCs for PET Detectors
  - ADS4149 – Single 14-bit, 250MSPS ADC with only 265mW of power consumption
  - **ADS4249** – Dual 14-bit, 250MSPS with only 260mW per channel power consumption

ADS5282

Ultra-Low Power 8-Channel, 12-bit 65MSPS ADC

Features

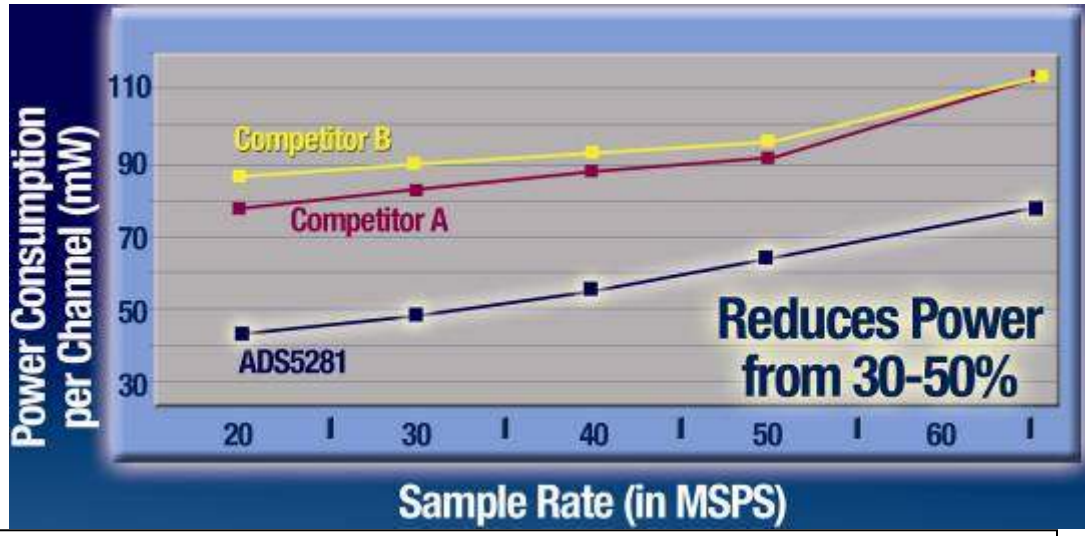
- **Lowest power: 77 mW per channel**
- **70 dBFS SNR, 85 dBc SFDR at 5MHz IF**
- **Programmable Features**
  - **1/f Noise suppression mode**
  - **0-12 dB gain in 1dB steps**
- **Up to 6 dB overload recovery in once clock cycle**
- **Serialized LVDS outputs with programmable current**
- **Pin Compatible Family: 9x9mm QFN packaging**
  - **ADS5281 also available in 80-pin TQFP pin compatible to ADS5271**

Benefits

- ***Enables high density applications to increase channel count without increasing power***
- **Performance uncompromised by low power consumption**
- **Gain and other programmable settings allow device to be optimized to your needs**
- **Immediate sensing after signal overload**
- **Reduced pin and trace counts**
- **Easy transition to higher sample rates or lower resolution**

Applications

- **Medical Imaging**
  - **Ultrasound**
  - **MRI**
  - **PET**
- **Industrial Imaging**
- **Wireless Communication**
  - **Diversity, MIMO Receivers**
  - **Software Defined Radios**
- **Multi-Channel Data Acquisition**



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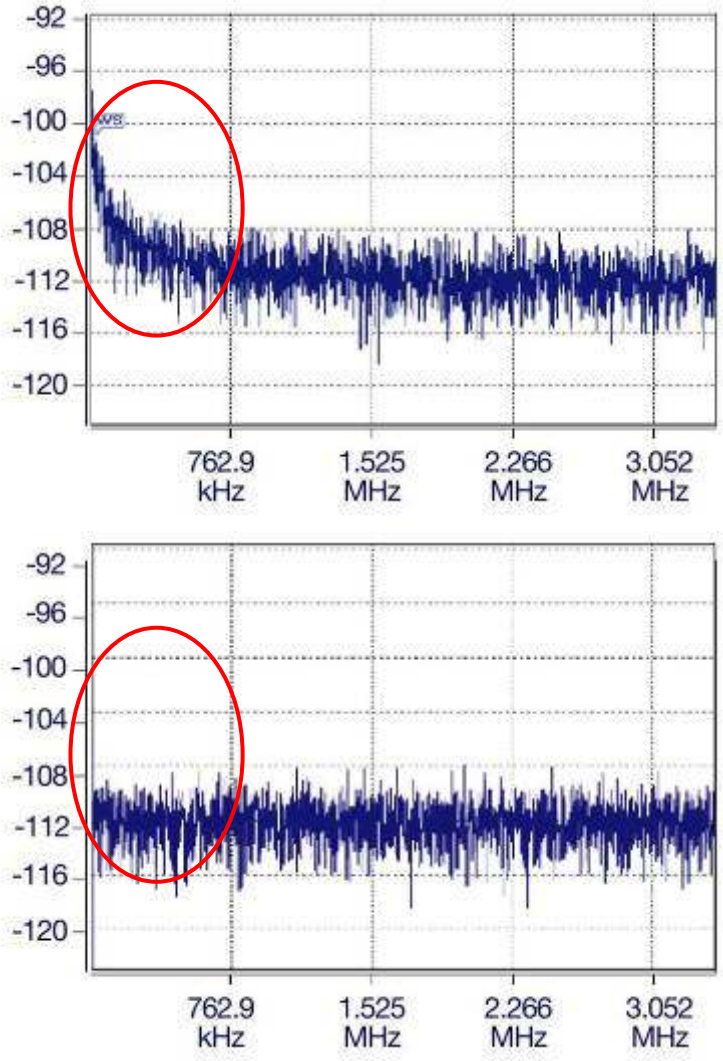
Digital Features Enhance Performance: 1/f Noise Suppression

- Suppresses 1/f (Flicker) Noise
- Enhances narrow-band SNR for very low IF and base band applications
  - Base band communications in Wireless Infrastructure
  - Portable Test and measurement
  - Ultrasound equipments with probe frequency 2.5MHz

Noise integrated from dc to	SNR with LF noise suppression mode Enabled (dBFS)	SNR with LF noise suppression mode Disabled (dBFS)
500KHz	89.2	83.6
1MHz	86.1	81.9
1.5MHz	84.4	80.9
2 MHz	83.3	80.0
2.5 MHz	82.2	79.5



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VCA8500

Ultra-Low Power Variable Gain Amplifier with Low-Noise Pre-Amp

8-Channel,

Features

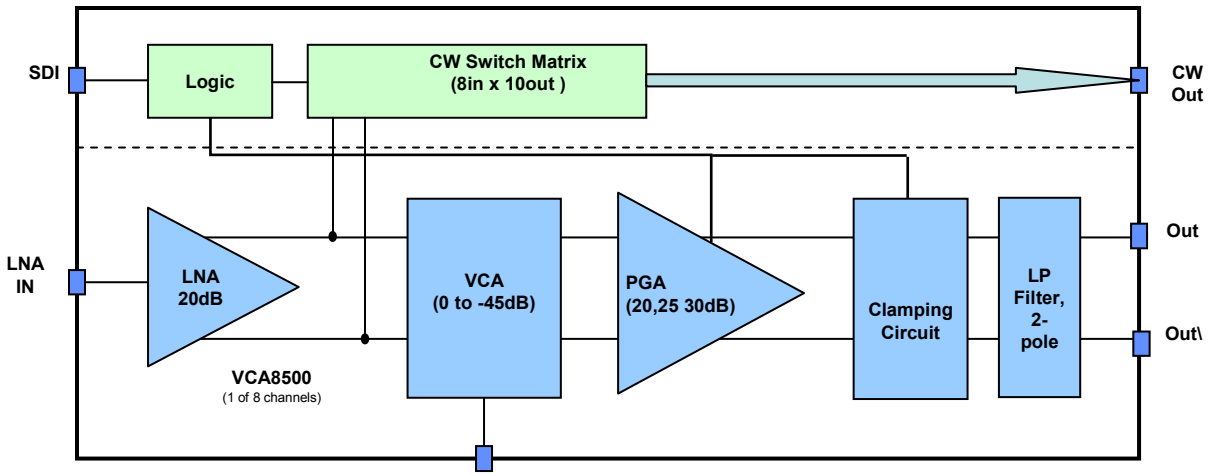
- Ultra-Low power: 63 mW per channel
- Low Noise: 0.8nV/rtHz
- Low-Noise Pre-amp (LNP)
  - 20 dB Fixed Gain
  - 250mVpp Linear Input Range
- Variable-Gain Amplifier
  - Gain control range: 45dB
  - Selectable PGA gain: 20, 25, 27, 30dB
  - Fast overload recovery
  - Output Clamping control
- Package: 64-pin 9x9 mm QFN

Benefits

- *Best in class noise performance with optimal power consumption extending performance and power savings in portable and midrange ultrasound systems*
- Low-Power: Important for portable systems; and others due to increase in channels/system
- Low-noise: LNA noise determines signal detection capability for all modes
- Size & Integration

Applications

- Ultrasound
- Sonar



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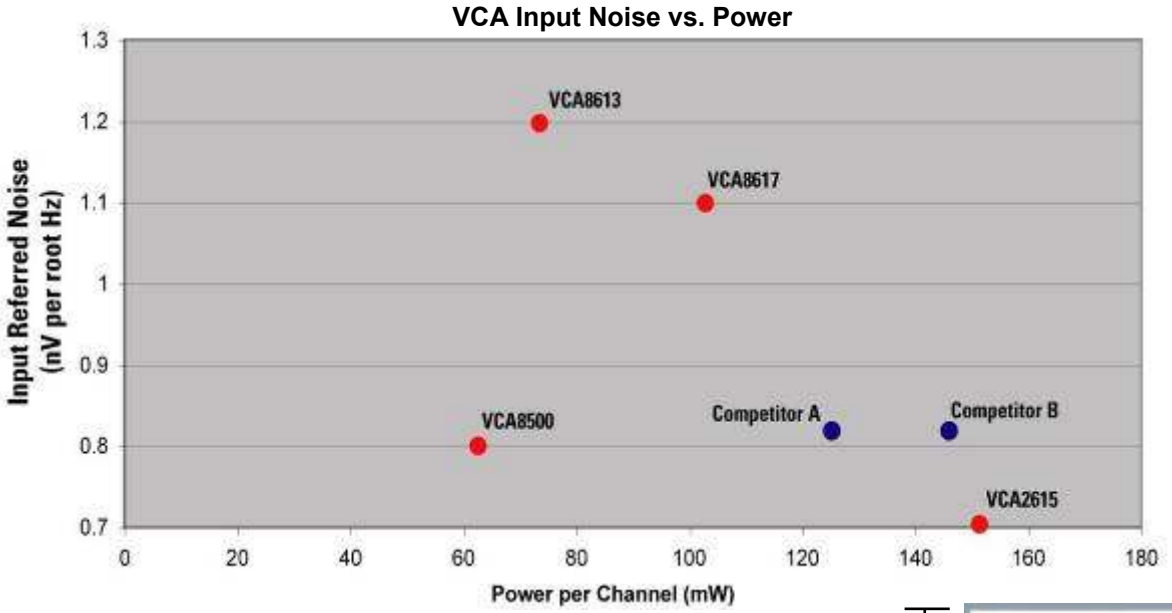
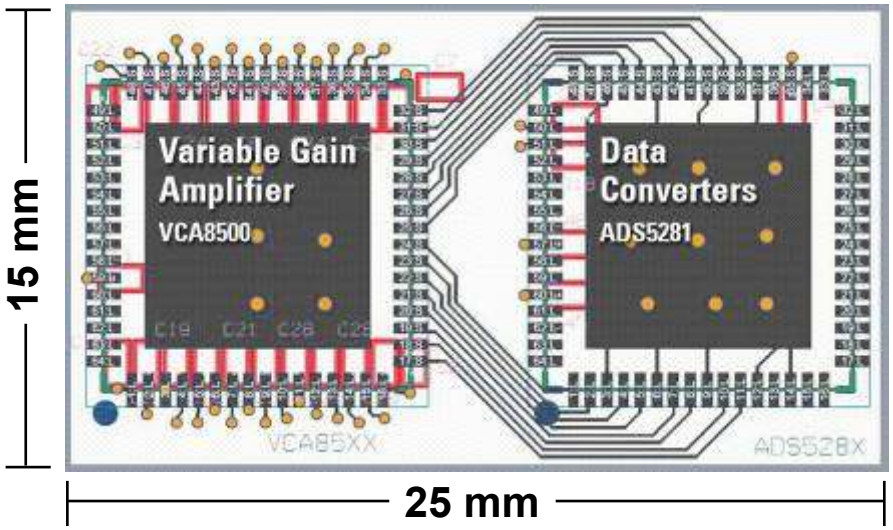
Complete Medical Signal Chain Solution with Low Noise and Power in Space-Saving Package



Complete medical signal chain with better noise performance and a combined power of less than 130 mW per channel at 50MSPS, less than any competing solution on the market today

Available in 9 x 9 mm QFN package

Direct interface for small signal chain footprint



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AFE, Pulser, & Switches for Ultrasound Systems

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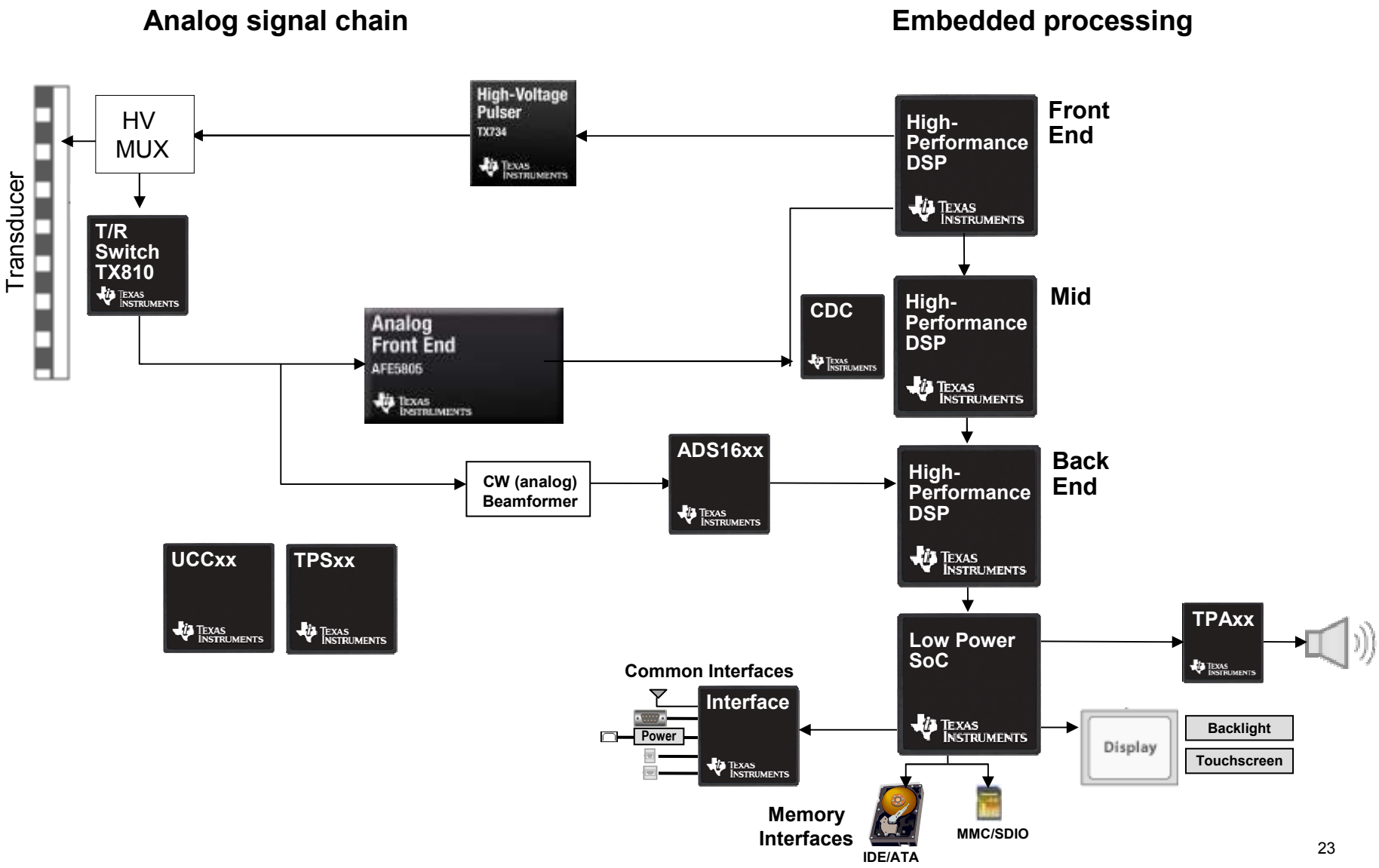
System level ultrasound



AFE5808

AFE with Passive CW Mixer for Ultrasound

Features

- Integrated LNA, VCA, PGA, LPF, 12/14-bit ADC with LVDS output up to 65 MSPS and CW doppler mixer and summing amplifier
- Low-noise optimization of 0.75nV/rtHz, 149mW/ch, 65 MSPS and an ADC with 77dBFS SNR
- Low close-in phase noise better than -155dBc/Hz at 1KHz off a 2.5 MHz carrier
- Total Max Gain: 54 db and 0.25/0.5/1 Vpp Linear Input Range
- 3rd order linear phase LPF with selectable bandwidth of 10, 15, 20, and 30 MHz and 50, 100, 200 or 400Ω active termination
- Package: 135-pin 15x9 mm BGA

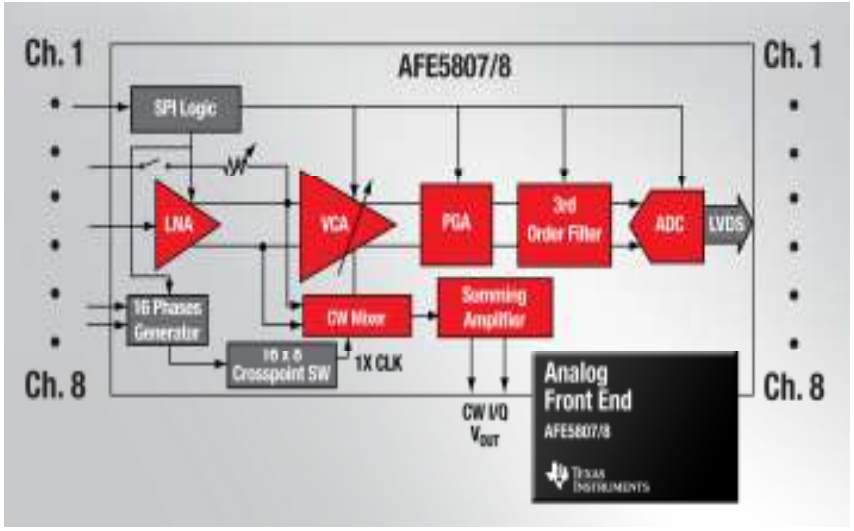
Applications

- Ultrasound
- Sonar

AFE5808EVM

Benefits

- Fully integrated AFE with CW for ultrasound
- High-performing solution for low-noise optimization and premium image quality
- Eases design with CW beamforming for Doppler Systems
- Optimized dynamic range for optimum image quality
- Supports a range of input amplitudes for different class of transducers
- 25 % smaller size for ease of design, smaller system footprint and increased channel count



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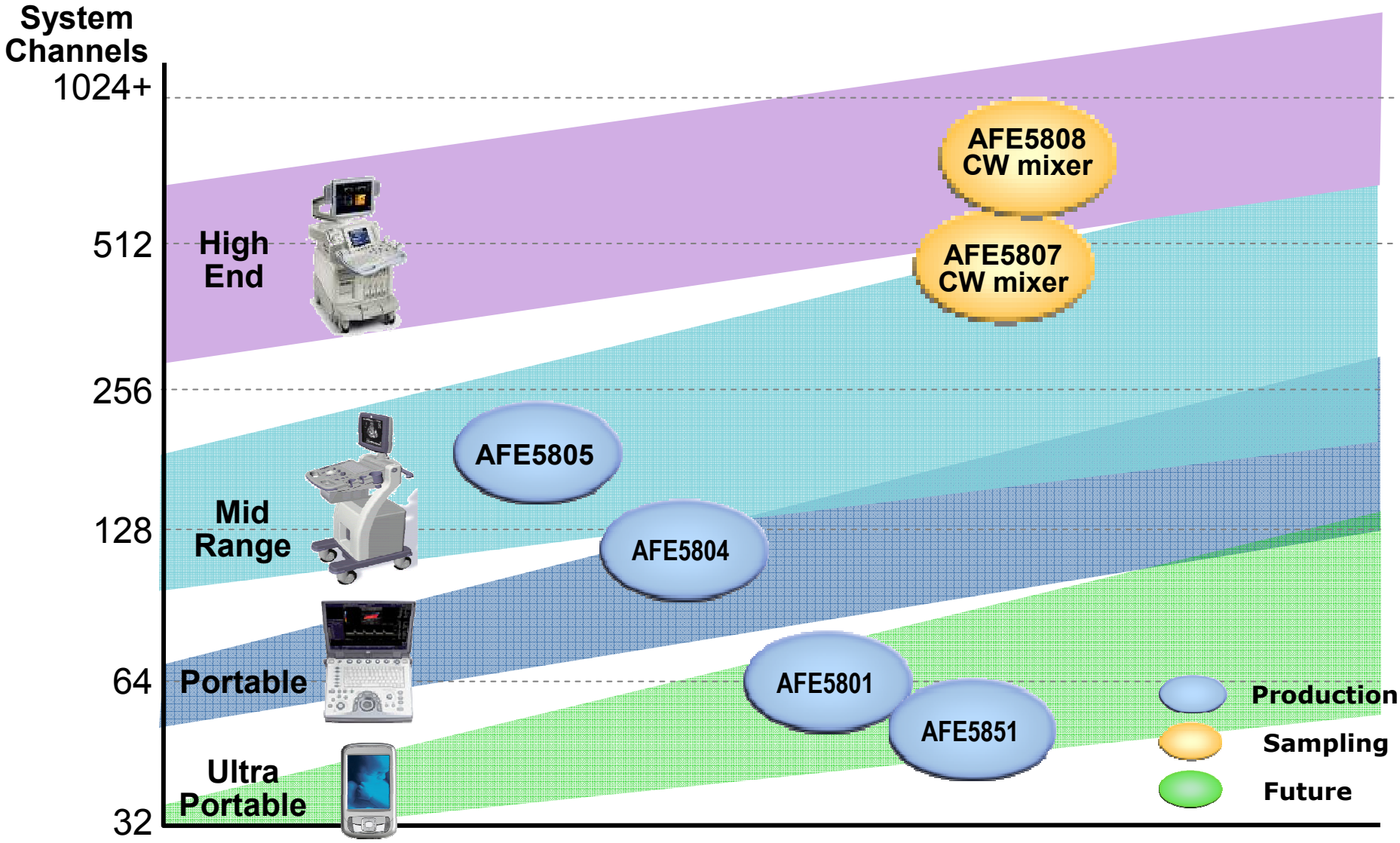
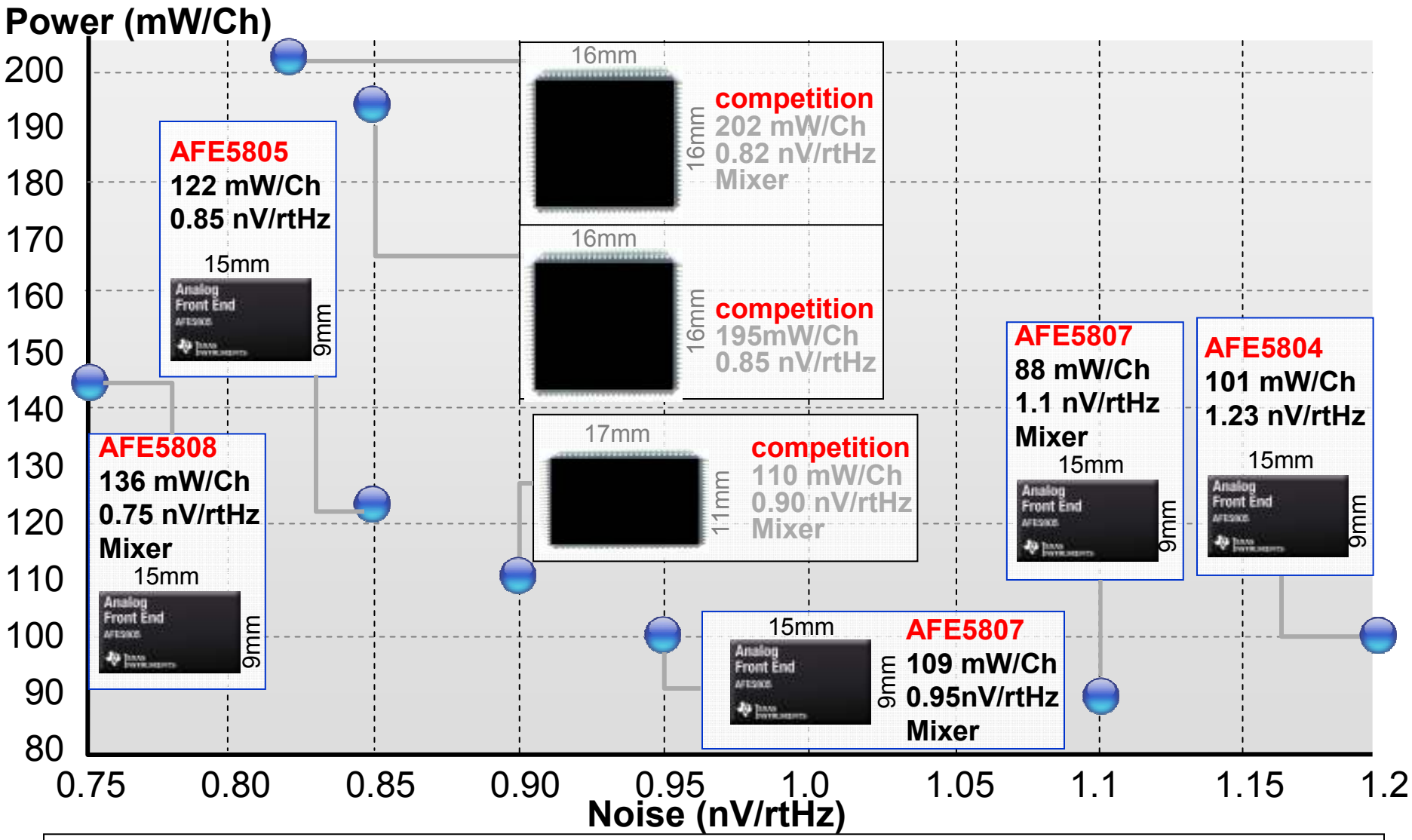
AFE family roadmap

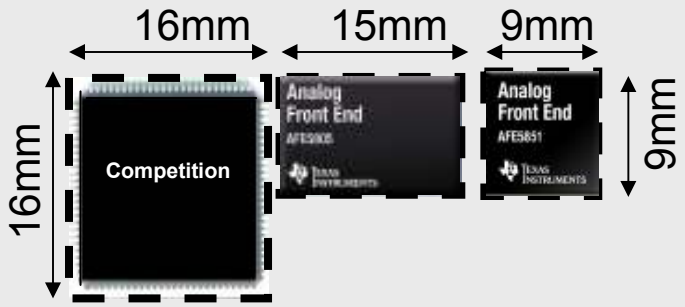


AFE with CW Mixer: Spec Comparison



Lower power & smaller size
for portable and ultra-portable systems

Board Space Savings



Increased Channel Count at Low Power

16- or 8- channels, over 50% lower power, 50% smaller size than closest competitor

AFE5804	AFE5807	AFE5801	AFE5851
8-channel	8-channel	8-channel	16-channel
101/112mW/ch *40MSPS@12bit*	87mW/Ch *40MSPS@12bit*	58mW/ch *50MSPS@14bit*	39mW/ch *32.5MSPS@14bit*
1.23/0.89 nV/rtHz	1.05 nV/rtHz	5.5 nV/rtHz	5.5 nV/rtHz
135-pin 15*9 mm	135-pin 15*9 mm	64-pin 9*9 mm	64-pin 9*9 mm

TI High Speed Converters for Wireless Infrastructure

➔ **Speed, Performance, Power and Density**

Multi-channel ADCs for multi-carrier 3G, 4G Receivers

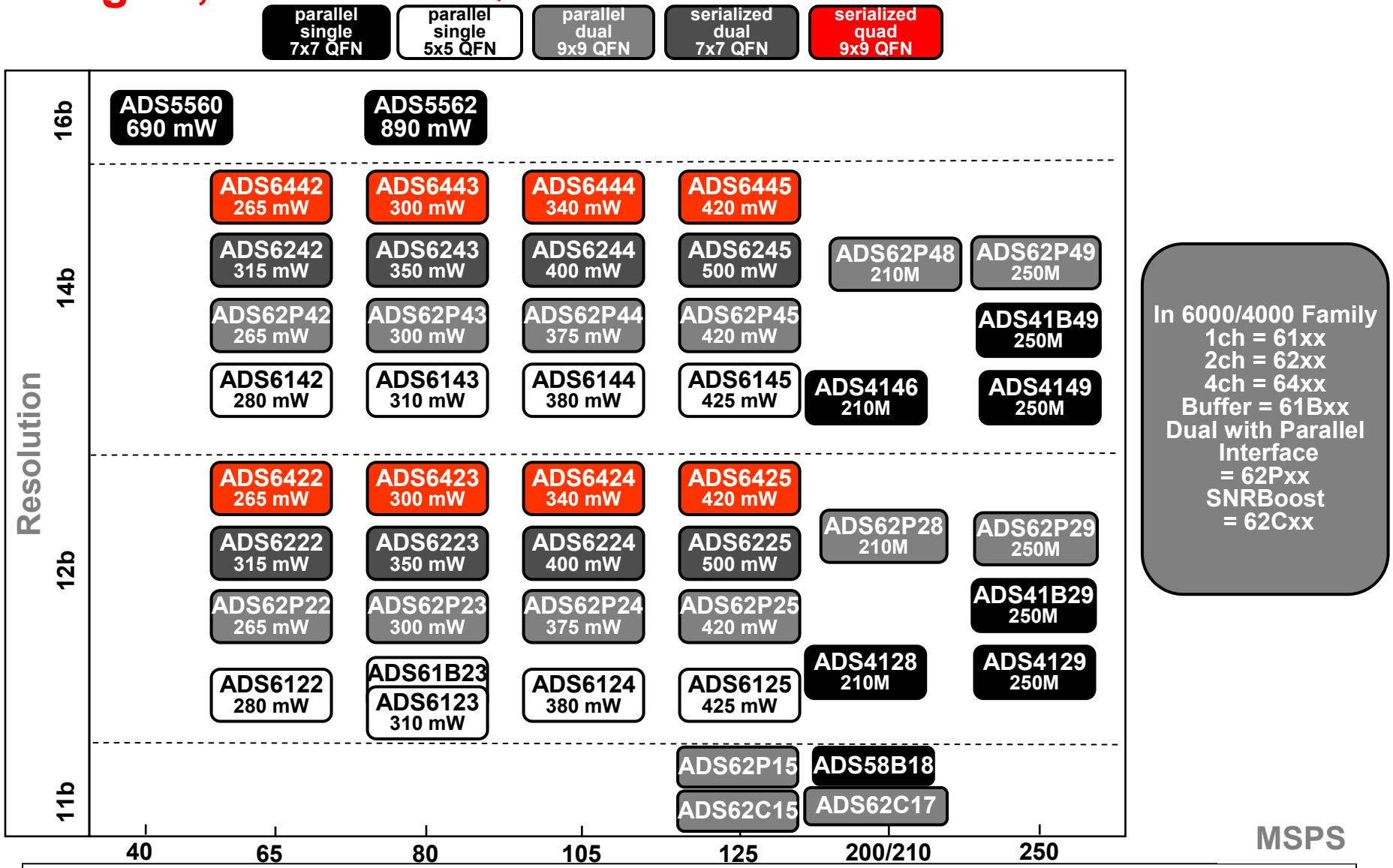
- Low power consumption
- High density – quads up to 125MSPS, duals to 250MSPS
- 12- and 14-bit resolutions; 11-bit solutions with SNR*Boost*tm

- **ADS6000** Family Overview - Single, dual and quad ADCs up to 250MSPS
  - ADS62P49 – Dual, 14-bit 250MSPS ADC
  - ADS6445 – Quad, 14-bit 125MSPS ADC with serial LVDS output
  - ADS62P45 – Dual, 14-bit 125MSPS ADC with parallel CMOS or LVDS output
  - ADS62C15 and ADS62C17 – Dual 11-bit, 125 and 200MSPS ADCs with SNR*Boost*tm

- **ADS4000** Family Overview – Low Power single and dual ADCs up to 250MSPS
  - ADS4249 – Dual 14-bit, 250MSPS with only 260mW per channel power consumption
  - ADS58C48 and ADS58C28 – Quad and dual, low power 11-bit, 200MSPS ADCs with SNR*Boost*tm

Low Power CMOS ADCs

Singles, Duals and Quads



In 6000/4000 Family
1ch = 61xx
2ch = 62xx
4ch = 64xx
Buffer = 61Bxx
Dual with Parallel Interface
= 62Pxx
SNRBoost
= 62Cxx

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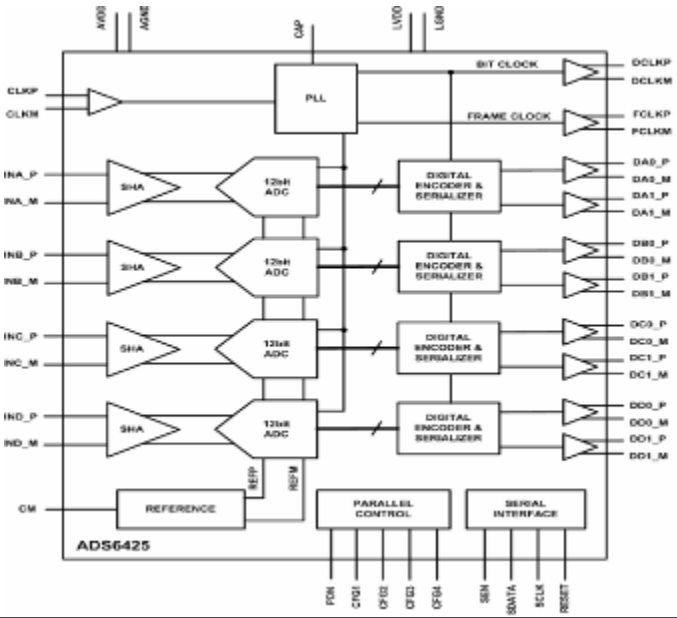
ADS6445

Low Power, High Performance Quad 14-bit 125MSPS ADC

Features

- **Pin Compatible Family: 64-pin 9x9 mm QFN package with serialized DDR LVDS Outputs**
- **73.2 dBFS SNR, 83 dBc SFDR at 50MHz IF**
- **Internal coarse and fine gain settings**
  - **71.9 dBFS SNR, 86 dBc SFDR at 50MHz IF**
  - **70 dBFS SNR, 80 dBc SFDR at 170MHz IF**
- **Low total power dissipation: 420mW/Ch**



Benefits

- ***Reduces board space up to 50% and trace count up to 60% vs. parallel outputs***
- **Best multi-channel 14-125 performance**
- **Gain and other programmable settings allow device to be optimized to your needs**
- **Low power enhances battery life and reduces thermal effects**

Applications

- **Wireless Communication:**
  - **Multi-channel Receivers**
- **Portable Test Instrumentation**
- **High-End Video Equipment**
- **Medical Imaging**
  - **Ultrasound, MRI, PET**
- **Radar and Guidance Systems**

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The Serialized LVDS Advantage

- Reduces number of traces by >60% compared to CMOS output solutions
- Eases design: less routing, smaller boards, improves manufacturability

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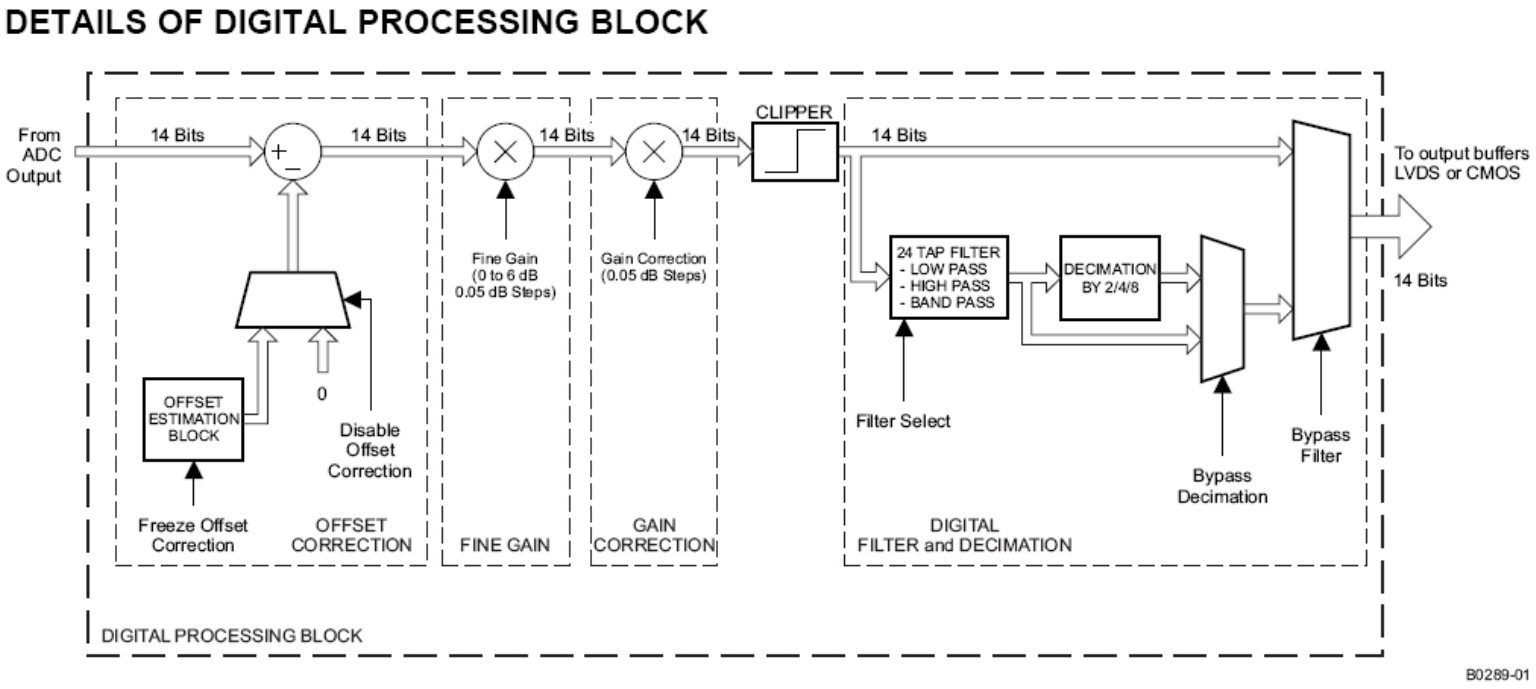
Digital Processing Features

- **Offset Correction**
- **Fine Gain Correction, in Steps of 0.05 dB**
- **Decimation by 2/4/8**
- **Built-in and Custom Programmable 24-Tap Low/High /Band Pass Filters**



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ADS4149

14-bit, 250MSPS ADC with only 255mW of power consumption

Features

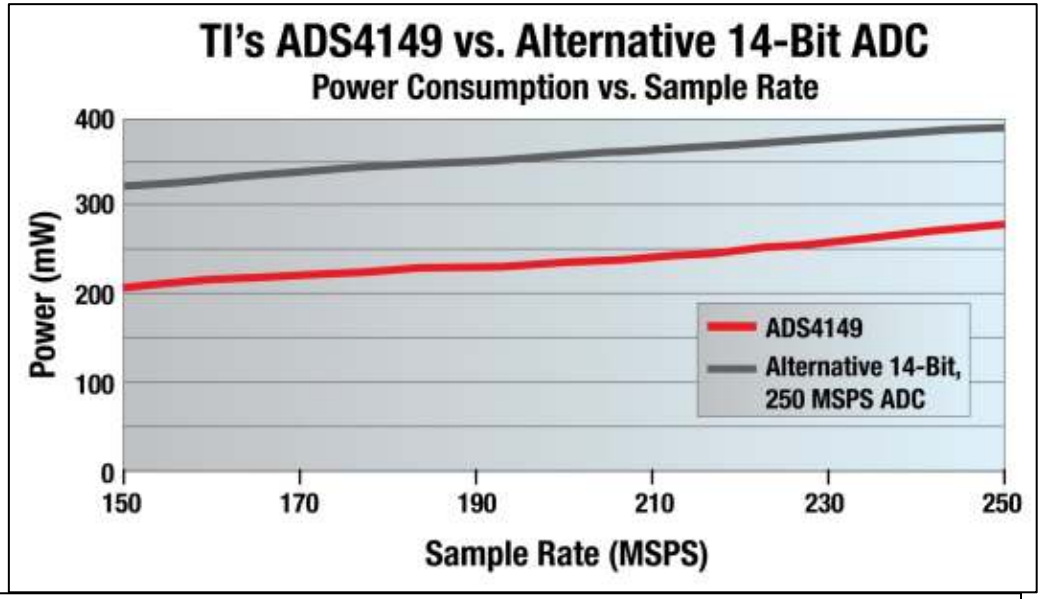
- Lowest power consumption available by 30%
  - 262mW in half-swing LVDS mode at 250MSPS
  - 200mW in half-swing LVDS mode at 160MSPS
- High performance 14-bit ADC core
  - 72.8 dBFS SNR and 86 dBc SFDR at 100MHz IF
  - 71.5 dBFS SNR and 84 dBc SFDR at 170MHz IF
- 6 dB gain in 1 dB steps for SNR/SFDR trade-off
- 7x7mm, 48-pin QFN package footprint compatible to the ADS6149 family
- Selectable DDR LVDS or CMOS outputs
- 1.8V AVdd and DVdd supplies

Benefits

- *Enables extended battery life, smaller battery sizes and higher density in portable applications*
- Highest SNR and SINAD for any 250MSPS ADC consuming less than 400mW of power
- Gain and other programmable settings allow device to be optimized to your needs
- Provides simple pathway for reduced power consumption on current ADS61xx designs
- Flexibility of reduced I/O speed or pin-count

Applications

- Software defined radios
  - Portable man-pack receivers
  - High density, multi-mode receivers
- Portable test and measurement equipment
- Wireless communication:
  - DPD feedback loops
  - Wideband digital repeaters
- General purpose portable and high density, high speed digitizers



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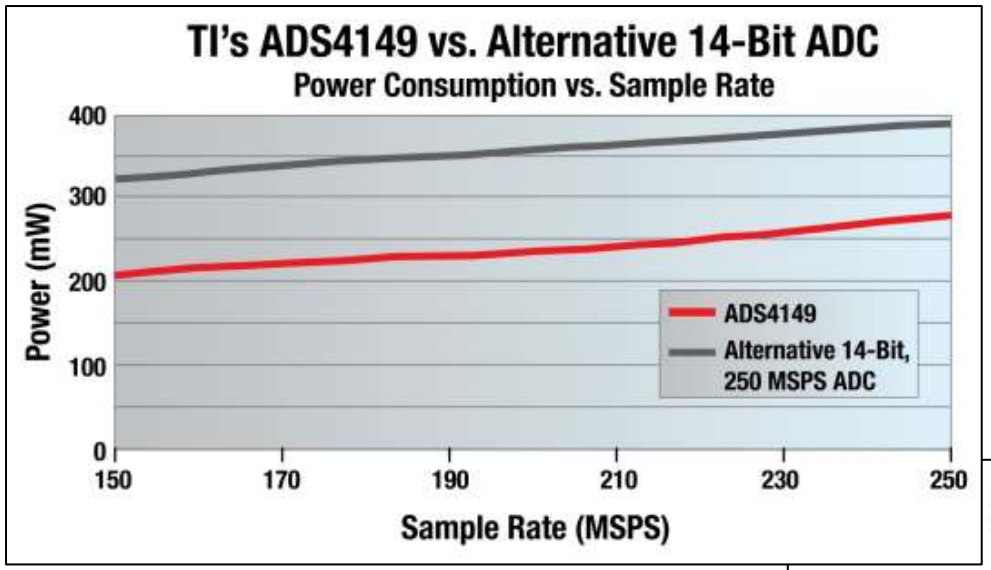
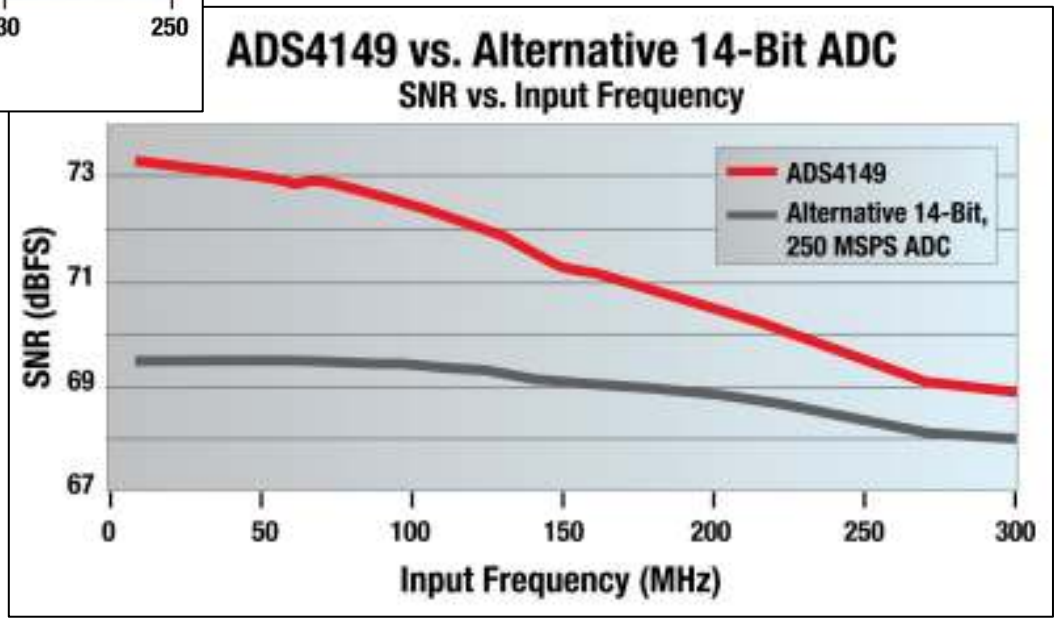
Texas Instruments

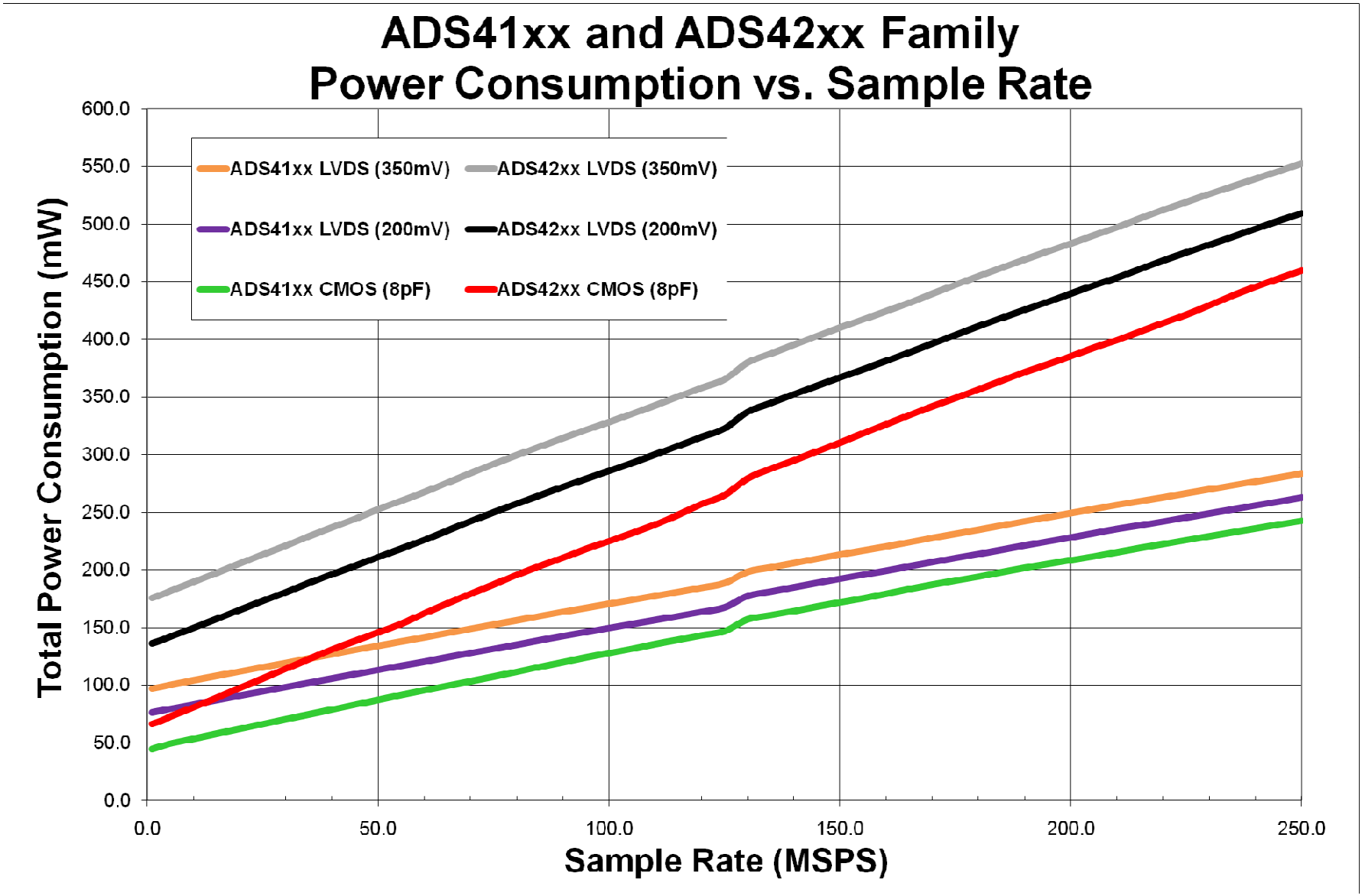
Power and performance: ADS4149 vs. competition





Texas Instruments

ADS4000 Family Power Across Sample Rate



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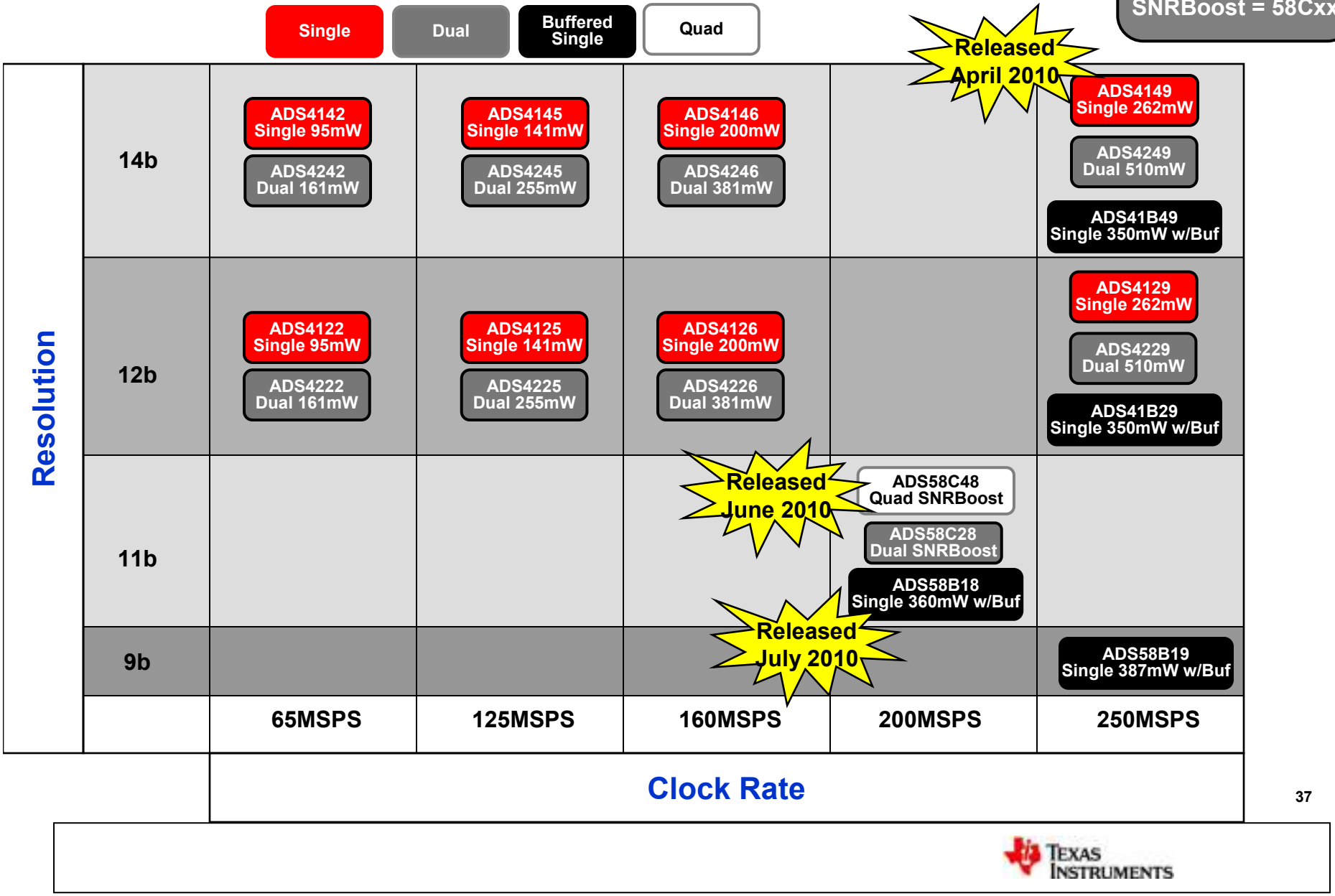
Texas Instruments

ADS4xxx/58xx Family

In 4000/58xx Family
1ch = 41xx
2ch = 42xx
Buffer = xxBxx
SNRBoost = 58Cxx



ADS4142

14-bit, 65 MSPS ADC with only 95mW of power consumption

Features

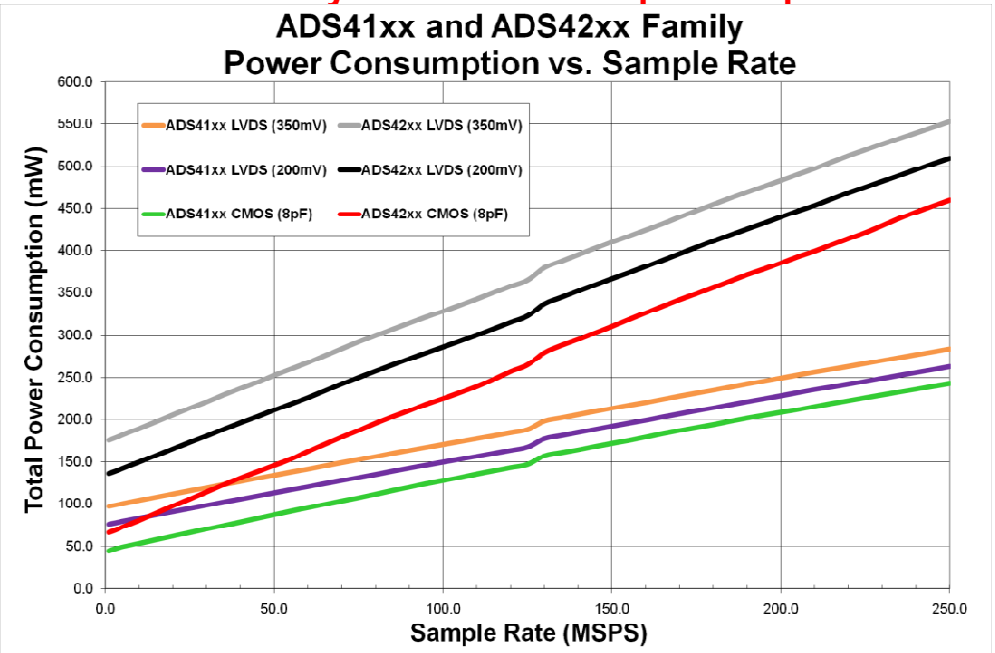
- Lowest power consumption available at 65MSPS
  - 95mW total in CMOS mode (6.2 pF load)
  - 124mW total in LVDS mode (200mV swing)
- High performance 14-bit ADC core
  - 72.0 dBFS SNR and 89 dBc SFDR at 50MHz IF
  - 69.0 dBFS SNR and 78 dBc SFDR at 170MHz IF
- 6 dB gain in 1 dB steps for SNR/SFDR trade-off
- 7x7mm, 48-pin QFN package footprint compatible to the ADS6149 family
- Selectable DDR LVDS or CMOS outputs
- 1.8V AVdd and DVdd supplies

Benefits

- *Enables extended battery life, smaller battery sizes and higher density in portable applications*
- High SNR, SFDR and SINAD offers 14-bit performance for under 100mW of power
- Gain and other programmable settings allow device to be optimized to your needs
- Provides simple pathway for reduced power consumption on current ADS61xx designs
- Flexibility of reduced I/O speed or pin-count

Applications

- Software defined radios
  - Portable man-pack receivers
  - High density, multi-mode receivers
- Portable test and measurement equipment
- Wireless communication:
  - DPD feedback loops
  - Wideband digital repeaters
- General purpose portable and high density, high speed digitizers



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Texas Instruments

ADCs for multi-carrier GSM receivers

- 16-bit resolution with up to 100 dBc SFDR
- Small package and minimal I/O

- **ADS5493** – 16-bit, 130MSPS ADC with 100dBc SFDR with 100MHz input frequency

ADS5493

16-bit, 130MSPS ADC with highest available SFDR in 2nd Nyquist

Features

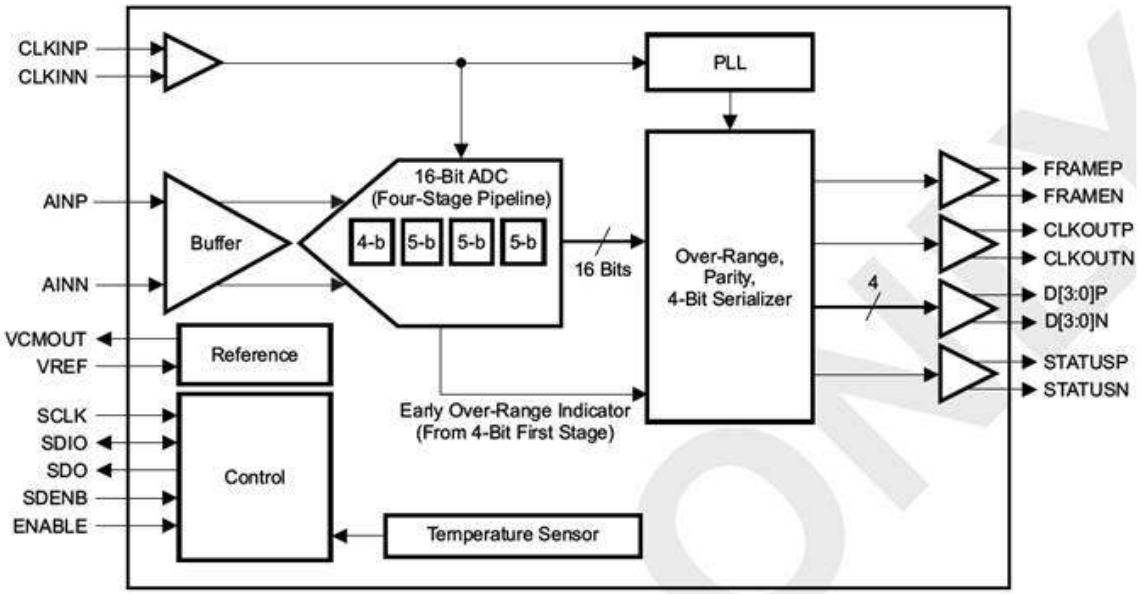
- Highest typical and guaranteed SFDR at 130MSPS
  - 105dBc typ SFDR at 30MHz IF, 93dBc guaranteed
  - 100dBc typ SFDR at 100MHz, 91dBc guaranteed
  - 95dBc typ SFDR at 170MHz
- 76 dBFS SNR across first two Nyquist zones
- Buffered, high impedance differential analog input
- 1.5-2.5 Vpp programmable input range
- 7x7mm, 48-pin QFN package with QDR LVDS interface requiring only 4 data pairs
- 1.8W power consumption

Benefits

- *Guaranteed dynamic range to meet full multi-carrier GSM cellular receiver requirements*
- Enables use in multi-carrier 3G and 4G receivers
- Eliminates kick-back and makes for flat impedance matching, easing AFE drive circuit design (THS7700)
- Allows for full-scale ADC outputs when used with reduced input differential
- Smallest 16-bit, 130MSPS ADC with halved I/O count reduces board and FPGA/ASIC costs

Applications

- Multi-mode, multi-standard wireless infrastructure, including MC-GSM
- Test and measurement instrumentation
- Software defined radios
- Radar
- Signals intelligence and jamming
- General purpose high speed digitizers



In Design, Samples Available, EVMs Available, RTP 2H 2010

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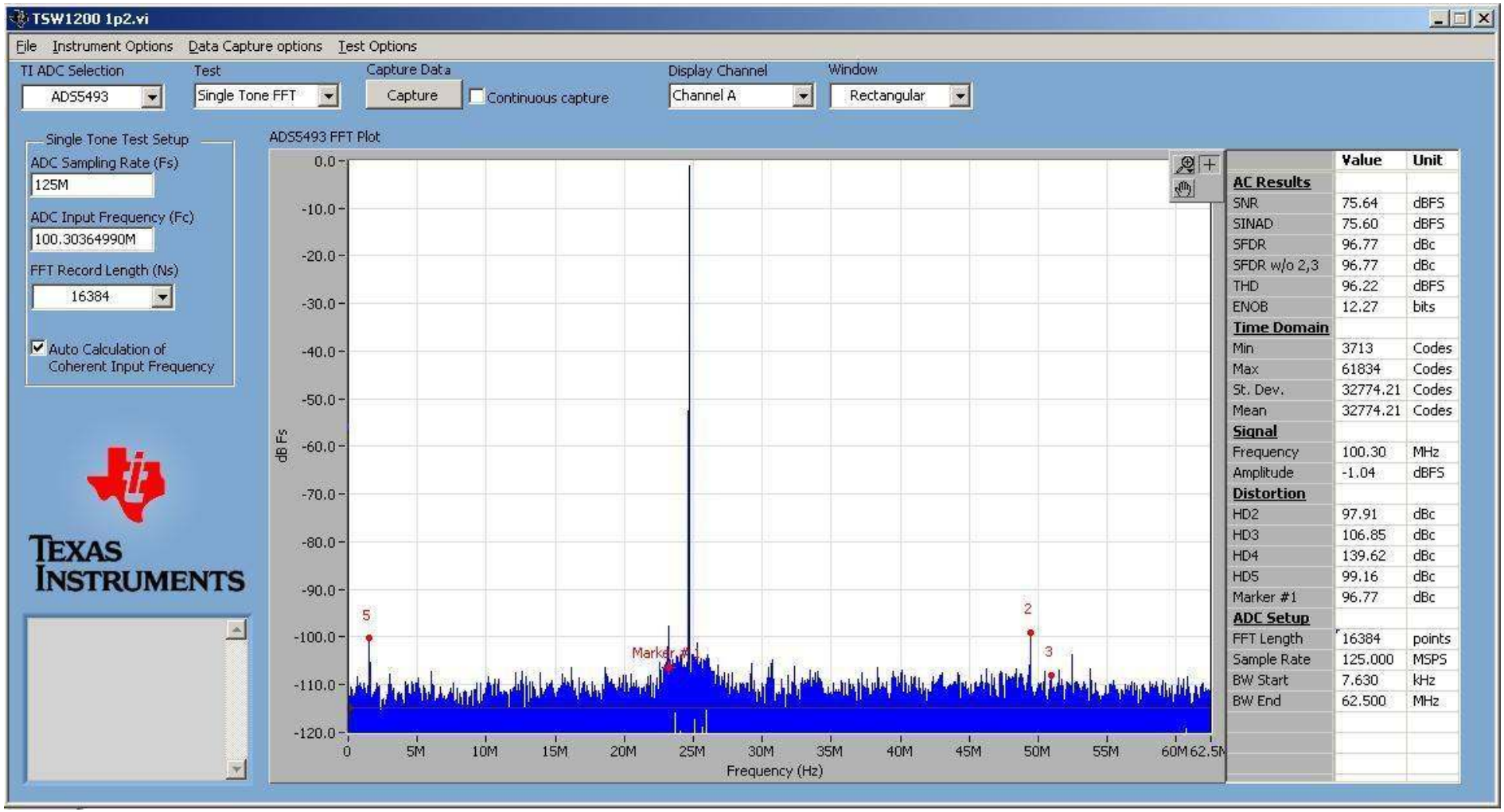
Texas Instruments

THS7700 Diff. Amp. Driving the ADS5493: 75.6 dB SNR, 96.7 dB SFDR at 100MHz IF



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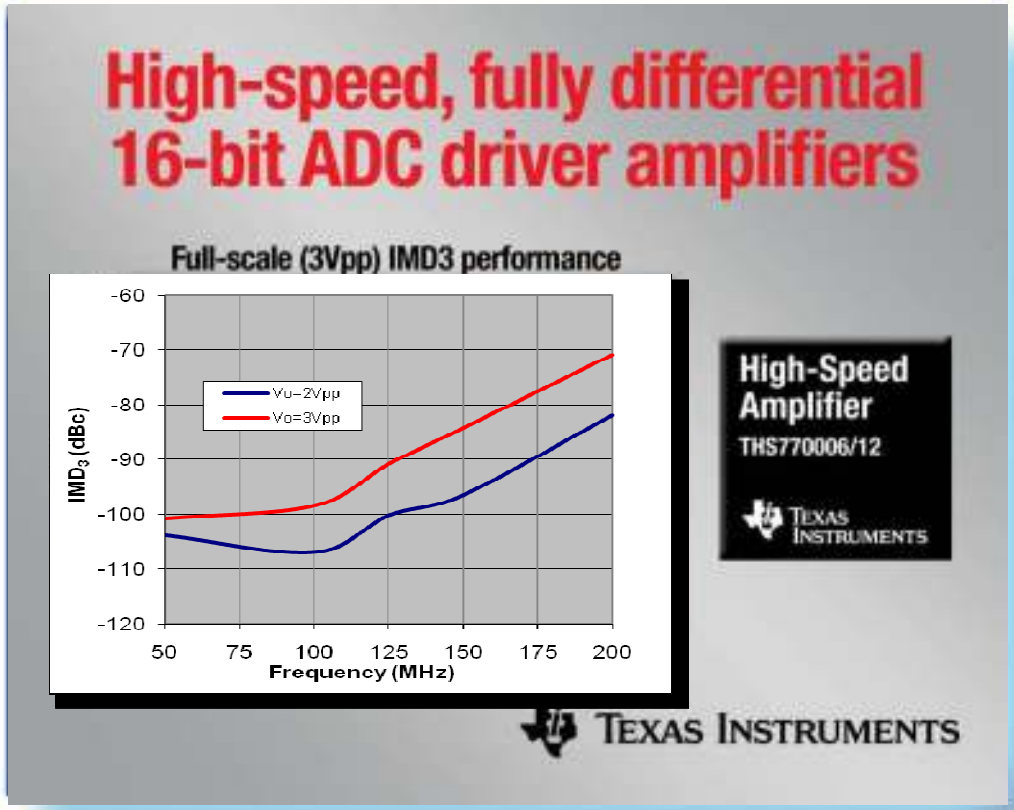
TEXAS INSTRUMENTS

THS770006/12
High-Speed, Fully Differential ADC Driver Amplifier



- **Low distortion (-107dBc IMD3), high linearity (48dBm OIP3), and 2.4GHz BW provide best in class performance enabling dynamic range required for driving 14- and 16-bit ADCs up to 200 MHz**
- **7.5ns overdrive recovery improves signal integrity by minimizing impact of jammers and blockers**
- **100mA quiescent current consumes 44% less power compared to RF amplifier implementations**

Supports:
- *Wireless Communications*
- *Radar and Guidance Systems*
- *Test, Measurement, and Instrumentation*

Texas Instruments

PGA870

Fully differential 14/16-bit ADC Driver with Digital Variable Gain Amplifier

Features

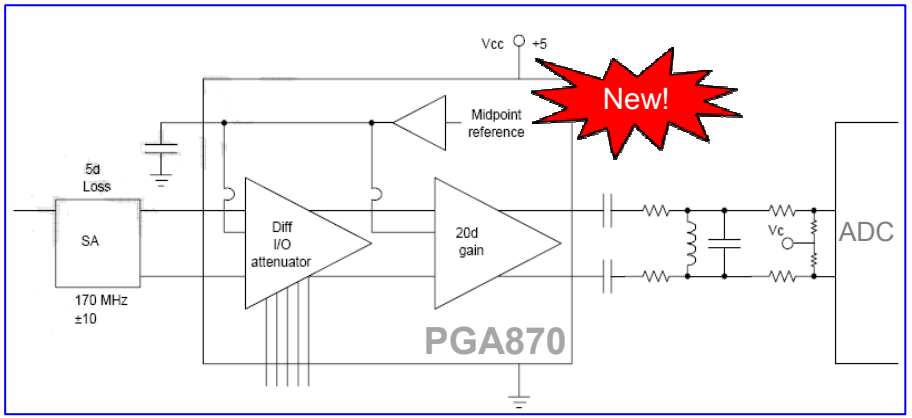
- Wideband: 650MHz -3dB Bandwidth (at all gains)
- Low Impedance, Voltage-Mode Output
- High Linearity: OIP3 = 47dBm at 100MHz
- HD2: –93dBc at 100MHz
- HD3: –88dBc at 100MHz
- IMD3: -99dBc at f1=90MHz, f2=100MHz
- Slew Rate: 2900 V/us
- Wide Adjustable Gain range: -11.5dB to +20dB
  - 6 bit gain control via parallel Interface
  - Fast gain switching time: 3ns
  - Latched & unlatched modes
  - Setup & hold time: 0.5ns - 1ns
  - 0.5dB resolution control
  - Gain may be set in active or power-down states
  - 0.2dB Absolute Gain Error Step Accuracy
- Power-down drops quiescent current to 2mA
- Supply Range +4.75 to 5.25V

Benefits

- Wideband operation is required for high speed data acquisition systems which have fast signal transitions.
- Improved gain flatness in pass band and eliminates the need for output inductors
- High linearity and low distortion are ideal for multi-mode, multi-carrier wireless applications
- Important for high speed digitizer applications to respond to fast signal transitions
- Required to accommodate varying signal levels
- 2x faster gain control switching makes this an ideal part for fast gain control loop applications i.e. 3G/4G radios.
- Power-down mode helps to reduce overall power dissipation, eg. TDD receiver architecture

Applications

- Programmable gain IF amplifier
- CDMA/WCDMA base station receivers
- Fully Differential 12/14/16-bit ADC driver
- High IF sampling receivers
- Wideband multichannel receivers
- Test and Measurement
- High Speed Digitizer Cards



Texas Instruments

ADC for Digital Pre-Distortion

- High speeds for wide feedback bandwidth – up to 500MSPS
- Buffered inputs for simplified AFE impedance matching
- 9-, 11-, 12- and 14-bit resolutions

- ADS4000 Family Overview - Single, dual and quad ADCs up to 250MSPS
  - ADS4149 – Single 14-bit, 250MSPS ADC with only 265mW of power consumption
  - ADS41B49 – Single 14-bit, 250MSPS ADC with buffered analog input and 345mW of power consumption
  - ADS58B18 – Single 11-bit, 200MSPS ADC with buffered analog input and SNR*Boost*tm
- ADS6149 – Single 14-bit, 250MSPS ADC
- **ADS61B49** – Single 14-bit, 250MSPS ADC with buffered analog input
- ADS5474 – Single 14-bit, 400MSPS ADC
- ADS5463 – Single 12-bit, 500MSPS ADC
- ADS54RF63 – Single 12-bit, 500/550MSPS ADC with high SFDR at IFs over 500MHz

ADS61B49

Low Power, High Performance 14-bit 250MSPS ADC With Buffered Input

Features

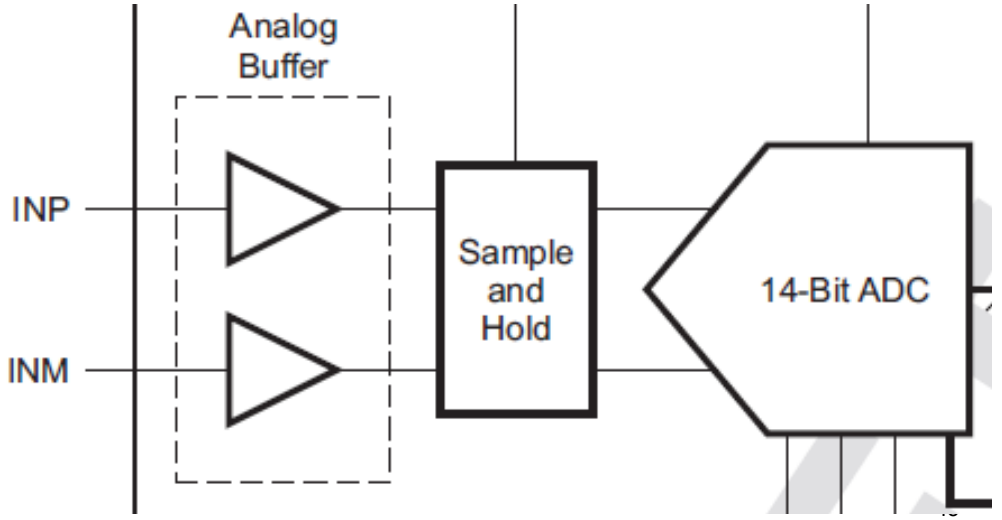
- **Fully Buffered Analog Input**
- **Pin Compatible Family: 48-pin 7x7 mm QFN package with selectable LVDS or CMOS outputs**
- **72.0 dBFS SNR, 85 dBc SFDR at 100MHz IF**
- **Internal gain settings: 1-6 dB in 1 dB steps**
  - **70.1 dBFS SNR, 87 dBc SFDR at 100MHz IF**
  - **67.5 dBFS SNR, 87 dBc SFDR at 200MHz IF**
- **Low power dissipation: 790 mW (LVDS output)**

Benefits

- ***Flatter input response for wide bandwidth input signals***
- ***Selectable outputs gives option for best performance or lowest power***
- **Best 250 MSPS performance available**
- **Gain and other programmable settings allow device to be optimized to your needs**
- **Low power enhances battery life and reduces thermal effects**

Applications

- **Wireless Communication:**
  - **Digital Pre-Distortion**
  - **MC-GSM**
- **Portable Test Instrumentation**
- **Radar and Guidance Systems**
- **High Speed Digitizers**



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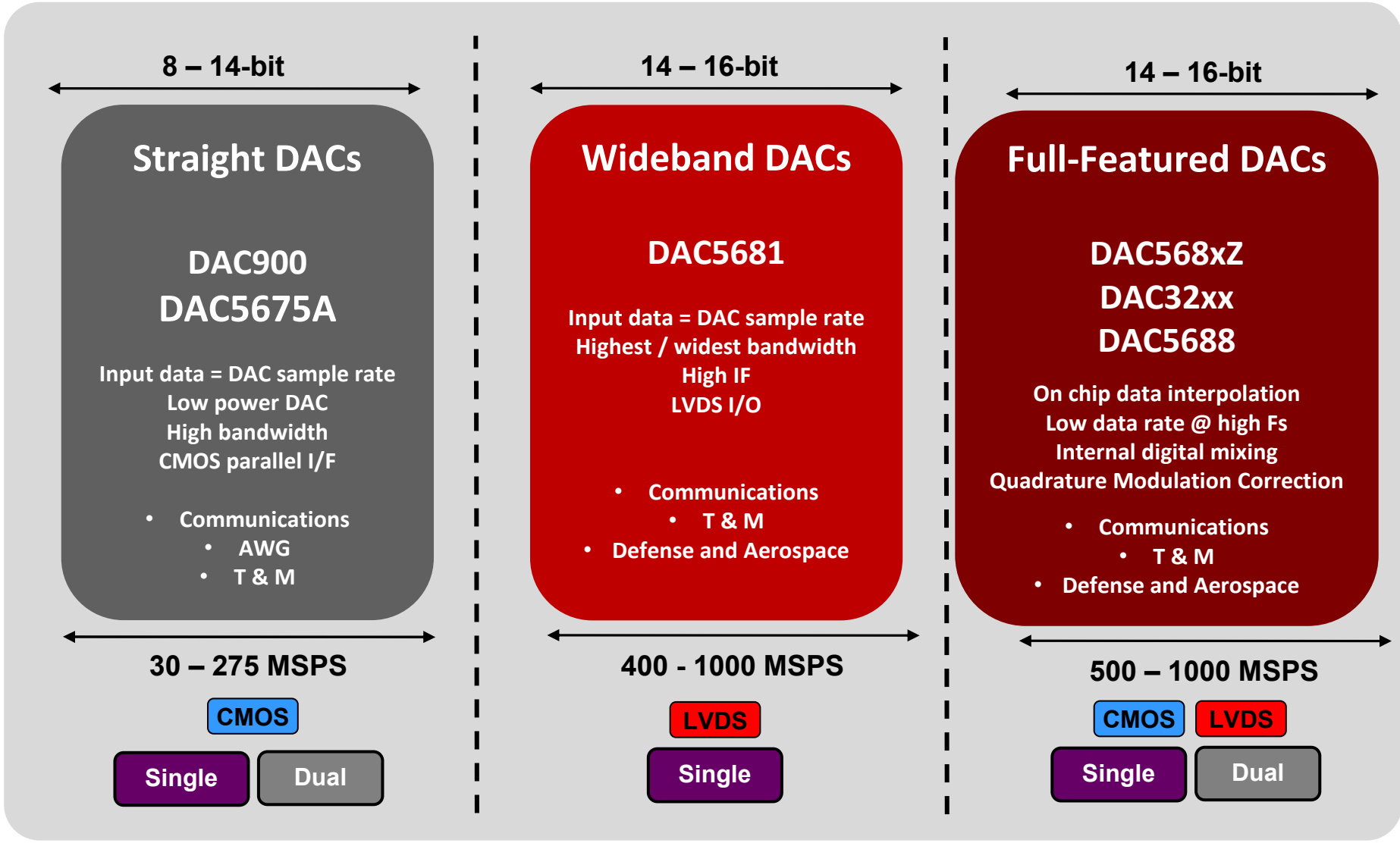
Texas Instruments

DAC

High Speed D/A converter portfolio

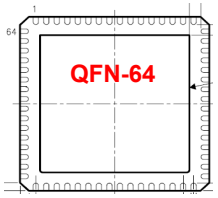


DAC5688/89

16-bit, 800MSPS, 2x, 4x, 8x Interpolation Dual DAC

Features

- Dual, 16-Bit, 250 MSPS CMOS Input Data
- Selectable 2x, 4x and 8x Interpolation Filters
- Complex Mixer with 32-bit NCO
- Integrated 2x-32x PLL Clock Multiplier (88 only)
- Digital Inverse SINC Filter
- Digital Quadrature Modulator Correction (QMC)
- 81 dBc ACLR WCDMA TM1 at 70 MHz
- Small Package: 9x9mm 64-pin QFN

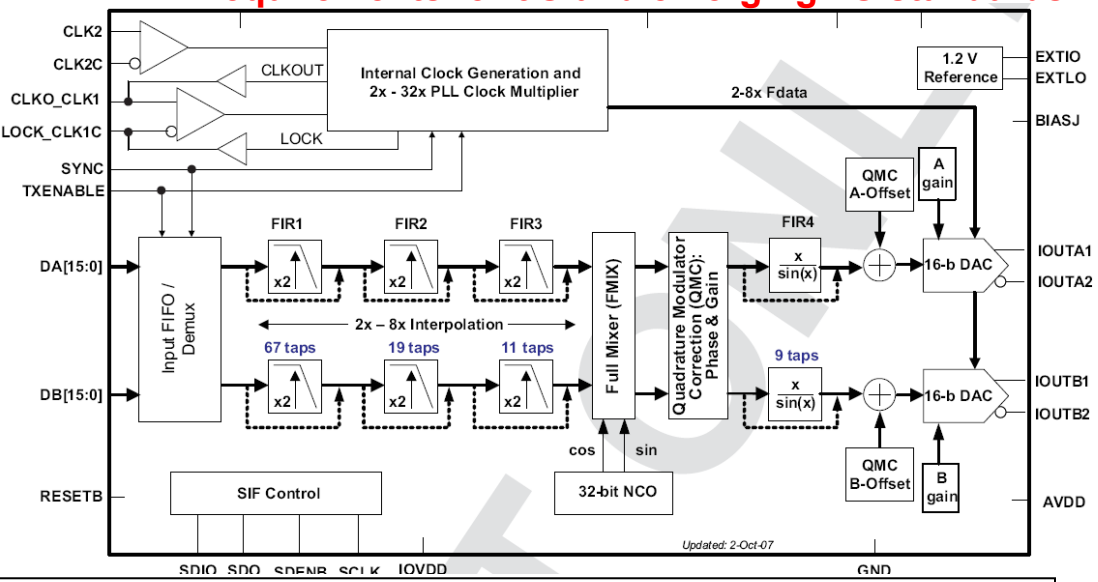


Benefits

- *2x-8x interpolation with 32-bit NCO provides simple data input and fine output frequency placement*
- Digital Inverse SINC filter compensates for natural DAC Sin (X)/X frequency roll-off
- QMC allows optimization of phase, gain and offset to maximize sideband rejection for I/Q modulation
- High performance with excellent ACLR meets requirements for 3G and emerging 4G standards

Applications

- Wireless Communications Infrastructure
- Software Defined Radio
- Power Amplifier Linearization
- 802.16d/e
- Test and Measurement Instrumentation
- Radar Systems



DAC5682Z

16-Bit, 1GSPS Dual Interpolating DAC with DDR LVDS Input

Features

- **16-bits, 1GSPS with 1GSPS DDR LVDS data bus**
- **High performance for wide-band signals**
  - **69 dBc SNR, 77 dBc SFDR at 20MHz**
  - **60 dBc SNR, 73 dBc ACLR at 180MHz (W-CDMA)**
- **Available in 9x9mm, 64-pin QFN package**
- **Pin compatible with single-channel 1GSPS interpolating DAC5681Z and straight DAC5682Z**
- **Low power dissipation: 1255 mW (full data rate, 2X interpolation)**

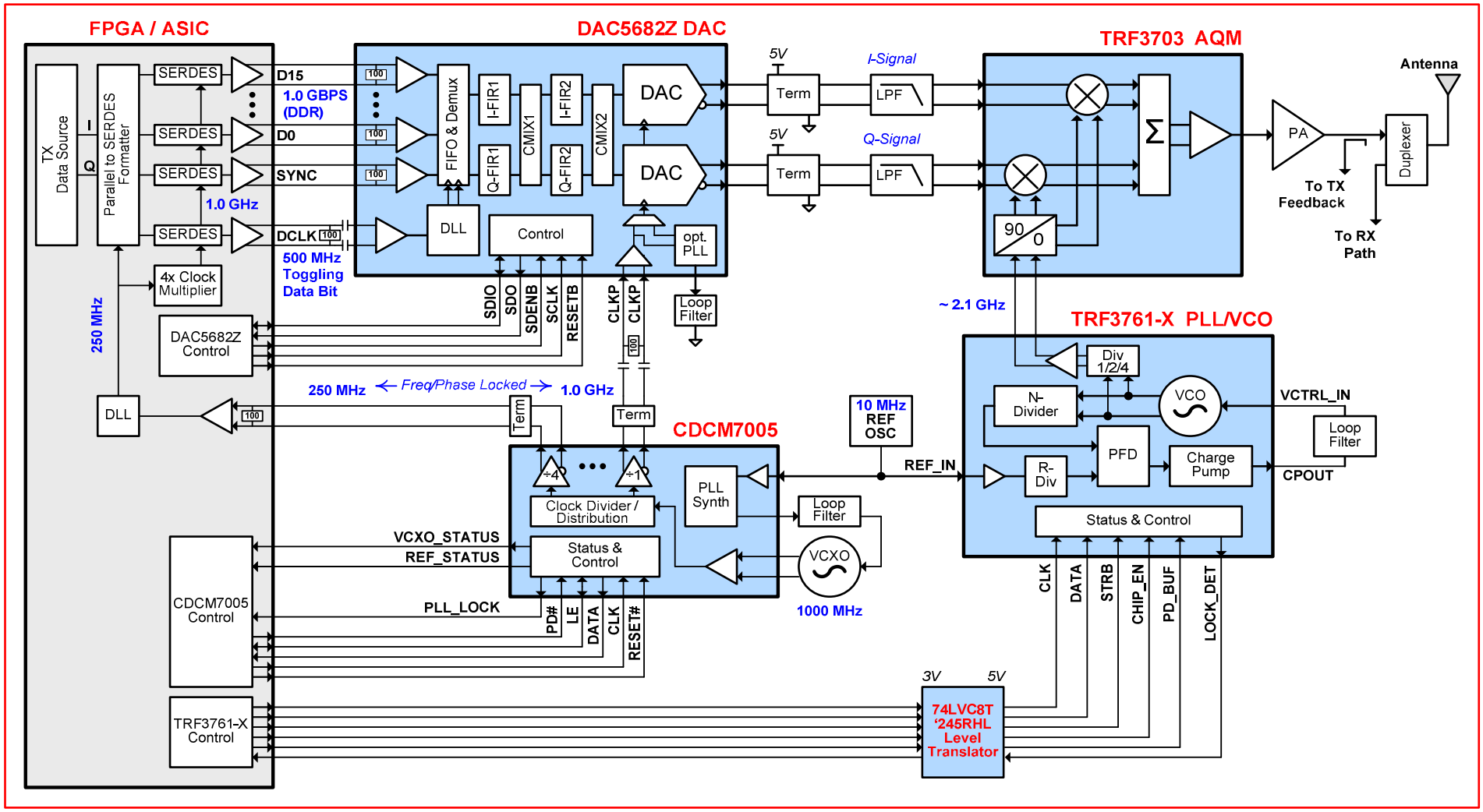
Benefits

- ***Enables up to 400Mhz of transmit bandwidth***
- **Allows for eased filter designs and wide bandwidths without compromising performance**
- **Smallest 1GSPS DAC footprint**
- **Provides flexibility in channel count and integrated digital features**
- **Minimizes thermal effects in highly confided systems while reducing power budget**

Applications

- **Wireless Communication:**
  - **Digital Pre-Distortion**
  - **MC-GSM**
  - **Direct to IF & Software Defined Radios**
- **Portable Test Instrumentation**
- **Radar and Guidance Systems**
- **High Speed Arbitrary Waveform Generators**

Example Direct Conversion Block Diagram (TSW3082/DAC5682ZEVM)



DAC3283

Dual 16-bit, 800MSPS Communications DAC

Features

- 7 mm x 7 mm, 48-pin QFN package
  - Smallest Dual 16-bit dual DAC at 800MSPS
- Single 8-byte wide interleaved DDR LVDS input bus
- High performance 16-bit DACs for I/Q transmitters
  - 95 dBc IMD, -162 dBc/Hz NSD at 10MHz IF
  - 77 dBc IMD, -155 dBc/Hz NSD at 150MHz IF
  - 80 dBc adj., 82 dBc alt. ACPR at 153MHz IF
- 2x/4x interpolation with phase, gain and offset QMC correction
- Fs/2 and Fs/4 coarse mixer
- Low power consumption – 1150mW all features on
- Scalable 2 to 20mA current output (sink)

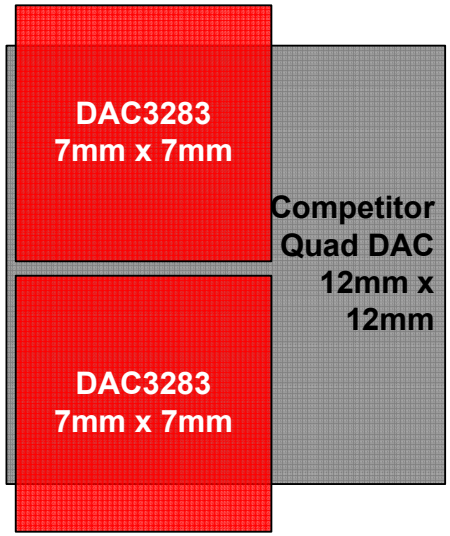
Benefits

- *Provides up to 80% board space savings for each transmitter chain*
- *Reduced I/O count saves costly FPGA pins*
- Designed to meet 3G, 4G and MC-GSM transmission requirements in high Fout designs
- Reduced I/O data rate while enhancing performance when driving I/Q modulators
- Reduced thermal effects allows for increased density in single- and multi-channel transmitters

Applications

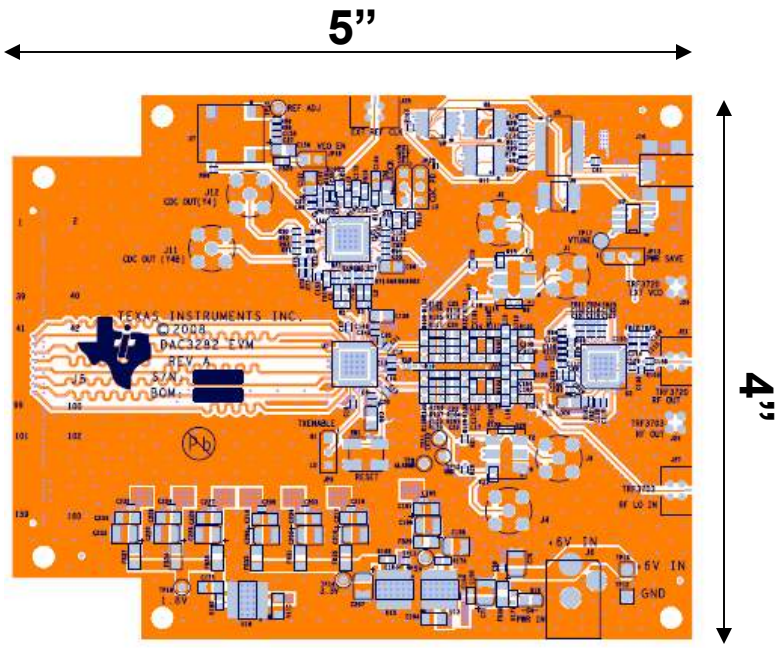
- Wireless Communications
  - 3G/4G Macro Base Stations
  - Wideband Repeaters
  - Software Defined Radios
  - Diversity Transmitters
- Software Defined Radios
- Test and Measurement – ARB
- 802.16d/e
- Power Amplifier Linearization

TI's 2x Dual DAC solution is 32% smaller!!!
Still smaller even with some extra space needed for layout



DAC3282/3283 EVM

- Features
  - DAC3282/3283
  - Quadrature Modulators:
    - TRF3720 (primary option)
      - Integrated PLL/VCO
    - TRF3703-33 (secondary option)
  - Clock Distribution:
    - CDCE62005 clock manager
      - Integrated VCO
  - Power Management



- Small design
  - DAC3283 + filter + TRF3720 + CDCE62005 = 50mm x 63mm

High Speed Data Converter Tools *at a glance…*

Data Capture / Pattern Generation

TSW1200EVM
LVDS ADC Capture Card

TSW1100EVM
CMOS ADC Capture Card

TSW3100EVM
High Speed DAC EVM
Pattern Generation

Evaluation Modules

High Speed DACs
EVMs for Every Device
In the Catalog

FPGA adapters
Direct connections
to FPGA EVM kits

Gerber Files Available
On Request

High Speed ADCs
EVMs for Every Device
In the Catalog

ADC SPI
SPI Register Programming
For ADC EVMs

Software / Design Support

IBIS Models
Available for most devices

Applications Notes

Online Community
Customers helping
Customers!

ADC Jitter and
DAC LPF Calculators

Reference Designs

TSW3070EVM
High Speed Arbitrary
Waveform Generation

Gerber Files Available
On Request

TSW4100EVM
Wideband Digital Repeater
Up to 70MHz Bandwidth!

TSW1070EVM
Amplifier-to-ADC
Reference Design

TSW1200 – LVDS ADC Capture Card

Features

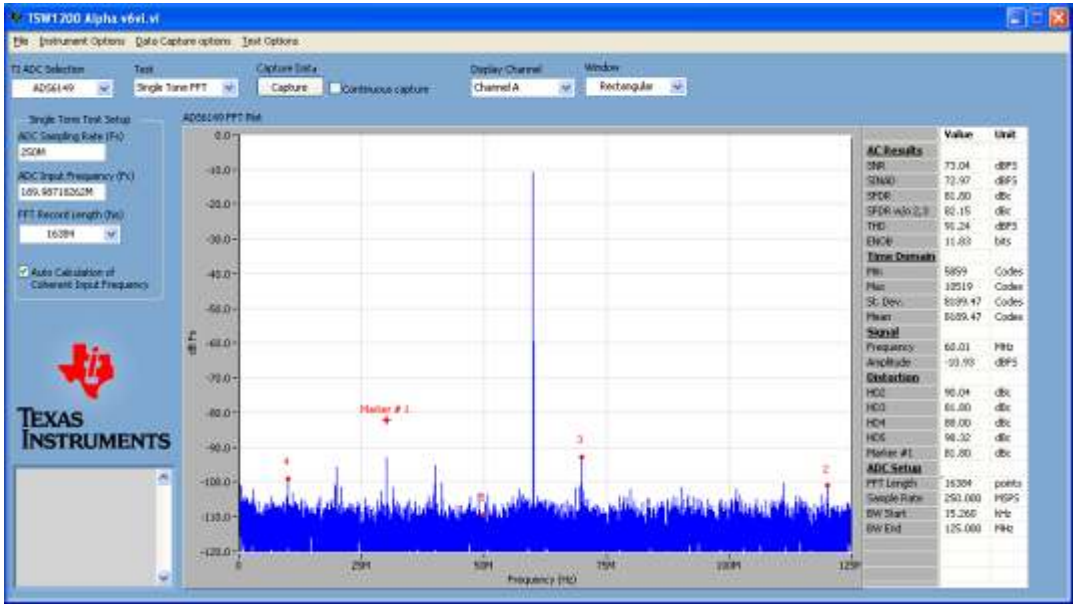
- Up to 4-channel LVDS output ADC data capture
  - Up to 16-bits and 1000MSPS
- Labview GUI for FFT and time-domain analysis
- Up to 8-channel LVDS deserialization and translation to CMOS headers (for TSW1100 capture)
- Available for $649 at TI.com

Benefits

- *Compatible with all LVDS output ADC EVMs*
- Simplified ADC performance evaluation
  - Includes coherence calculator for clock
- Compatible with multiple touchless probes and TSW1100 CMOS ADC capture tool

Applications

- Data capture for TI's entire portfolio of LVDS output ADCs (parallel, DDR, QDR, serialized)



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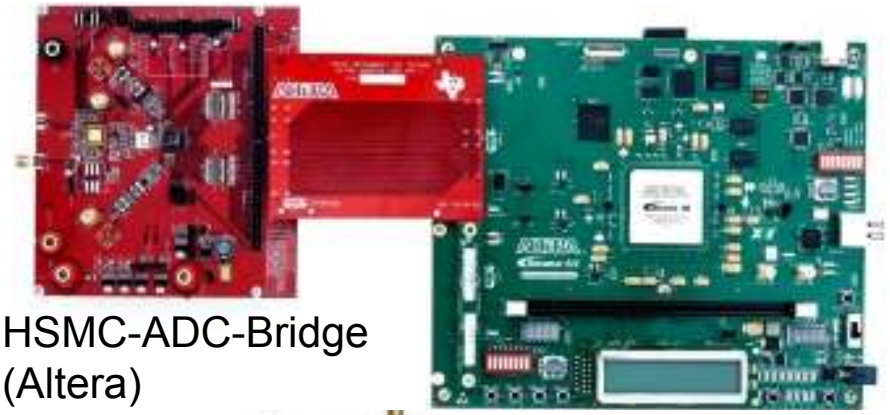
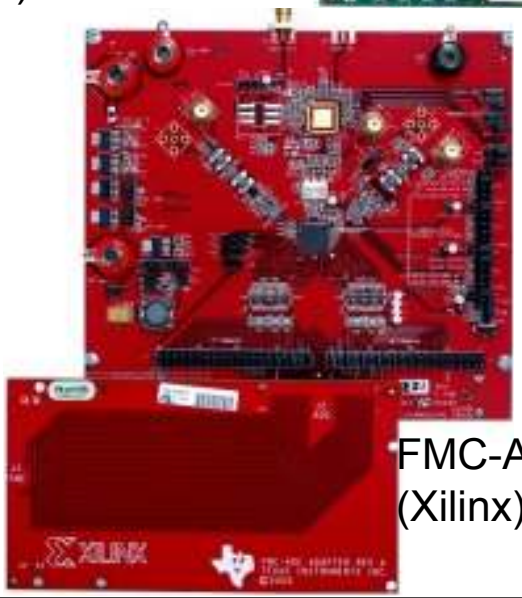
TEXAS INSTRUMENTS

FMC and HSCM Adapter Cards Enable High Speed ADC/DAC EVMs to Connect to FPGA EVMs

62 released High Speed ADC EVMs Compatible!

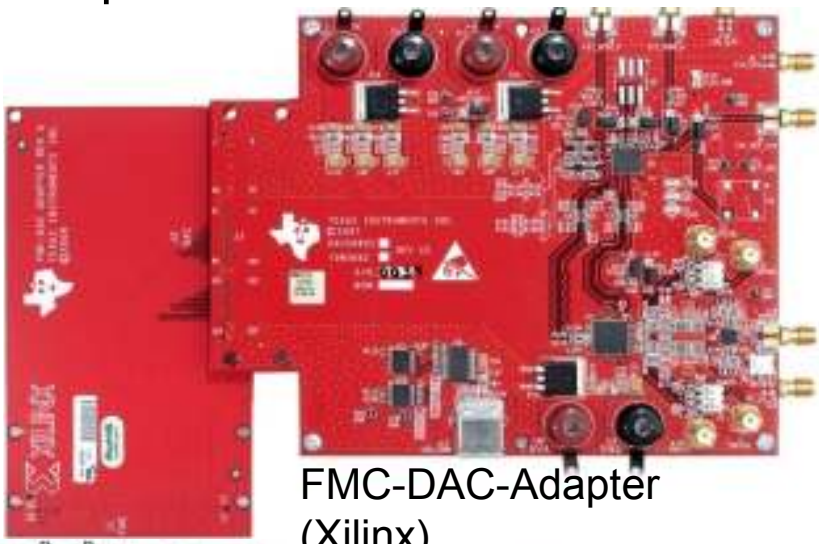


HSMC-ADC-Bridge (Altera)

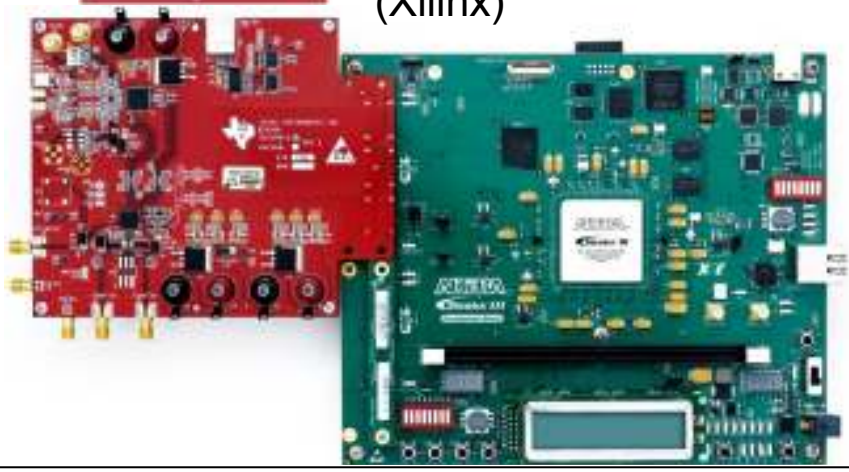


FMC-ADC-Adapter (Xilinx)

6 released High Speed DAC EVMs Compatible!



FMC-DAC-Adapter (Xilinx)



Wideband digital predistortion transmit processor demonstrator

- Live Demo

Introduction

- Recent years have seen a considerable growth in Digital Video Broadcast
- This growth generates an increasing need on high performance and low cost DVB transmitters
- Power Amplifiers consume more and more power and dramatically lowering performance in Wireless and broadcast services deployment
- Solving this problem is critical to allow providers improving quality of services
- To understand the impact of the DPD solution on PAs, TI has developed an adaptive digital pre-distortion evaluation board (EVM) on which complete solution from base-band to RF is operating
- This EVM is based on a the **GC5325**. The evaluation of this EVM has shown good results within all the wireless and broadcast standards

GC5325

Wideband Digital Predistortion Transmit IC Solution

Features

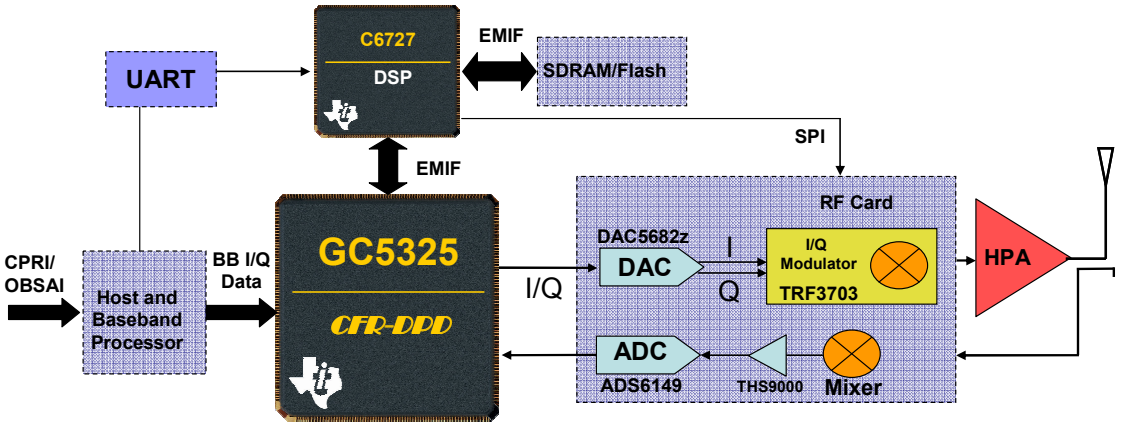
- Integrated functional transmitter blocks include:
  - Crest factor reduction (CFR)
  - Digital pre-distortion (DPD)
- Flexible DSP algorithm supports existing and emerging wireless standards
- Integrated CFR and DPD increase PA efficiencies
- Integrated DPD reduces adjacent channel leakage ratio (ACLR)
- 20MHz Bandwidth for 5th order correction
- Integrated IQ imbalance correction
- Fully automated channel equalizer
- Extremely fast DPD convergence times
- Robust convergence algorithm

Benefits

- **High Integration** - reduces design complexity, power consumption, development time, implementation size and bill-of-material (BOM) costs
- **High Performance**:
  - Integrated DPD reduces adjacent channel leakage ratio (ACLR) by 20 dB or more
  - Increases PA efficiencies to 25 percent or more for Class AB PAs and greater than 40 percent for Doherty PAs
- **Flexibility** - DPD architecture incorporates a TI DSP to run the fully adaptive linearization algorithm
- **Complete Solution** - complete signal chain solution reduces time-to-market and design risks
- **Robust** - Convergence algorithm allows dynamic carrier allocation, without disrupting cellular service

Applications

- 3GPP (W-CDMA, TD-SCDMA) Base Stations
- 3GPP2 (CDMA2000) Base Stations
- WiMAX, WiBRO, LTE (OFDMA) Base Stations
- Multicarrier Power Amplifiers (MCPAs)
- Two-Channel Transmit Diversity Applications
- Military Radio Transmitters



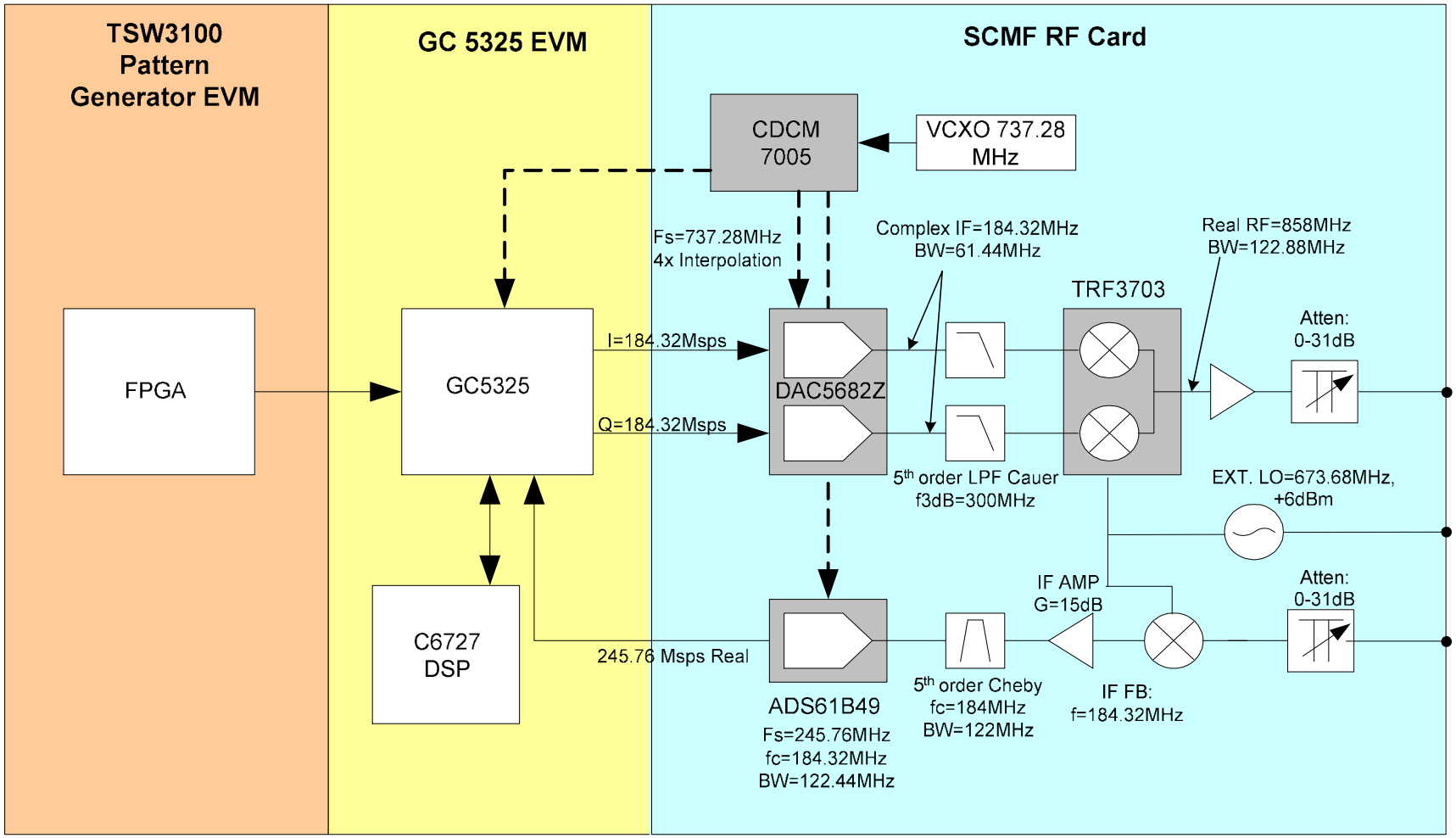
Texas Instruments

DVB-T System Requirements

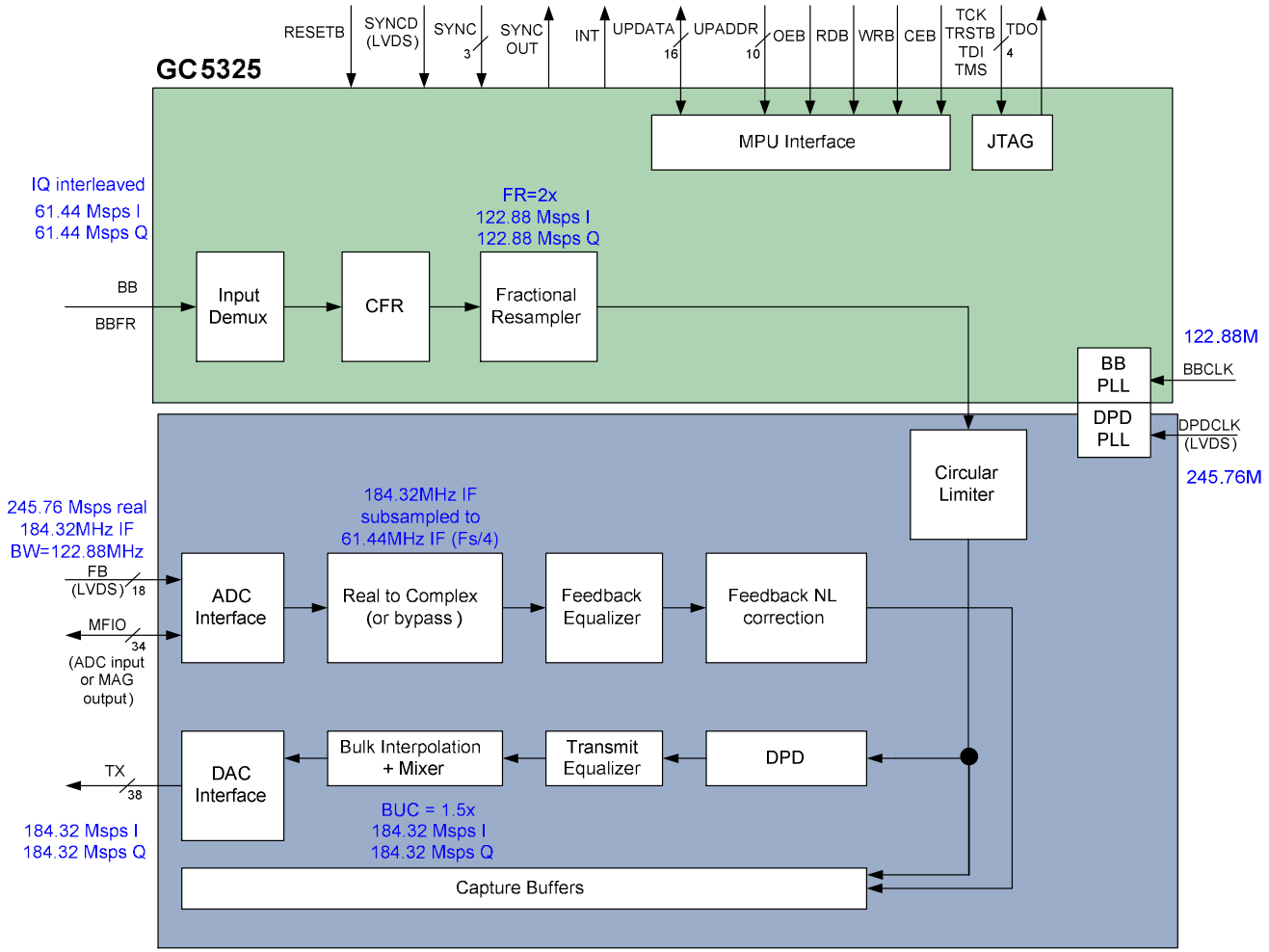
- One Transmit Path and one feedback path
- Power out: Ranges from 10Watts to 10KWatts
- RF freqs: VHF and UHF Band
- TX Requirements:
  - MER (Modulation Error Ratio) <-36dB
  - ACPR
    - Lower Power Applications (<57dBm Pout)
      - < -41dBc @4.2MHz offset in 4kHz BW
    - Higher Power Applications
      - < -36dBc @4.2MHz offset in 4kHz BW (not including cavity filter)

GC5325 EVM configuration for DVB-T

- Use existing GC configuration and frequency plan.
- Up-sample BB DVB-T signal from 9.1428Msps to 61.44Msps (default config of the GC5325SEK)
- Feedback mixer allows testing of upper channels only (CH69)



GC5325 Configuration for DVB-T

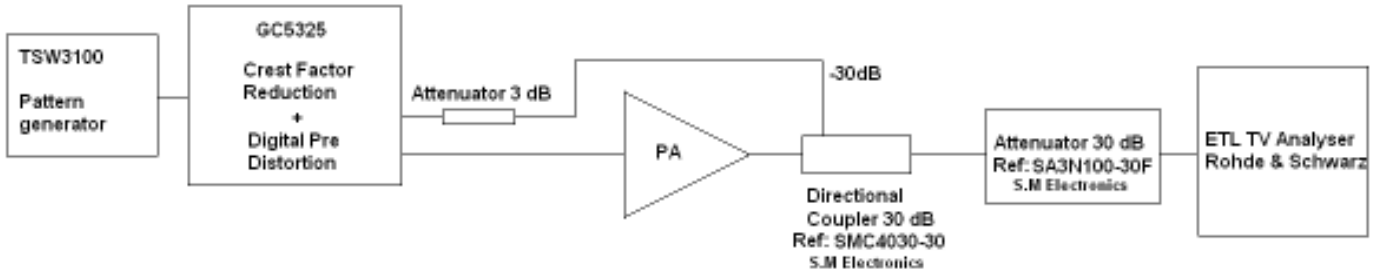


Test setup environment

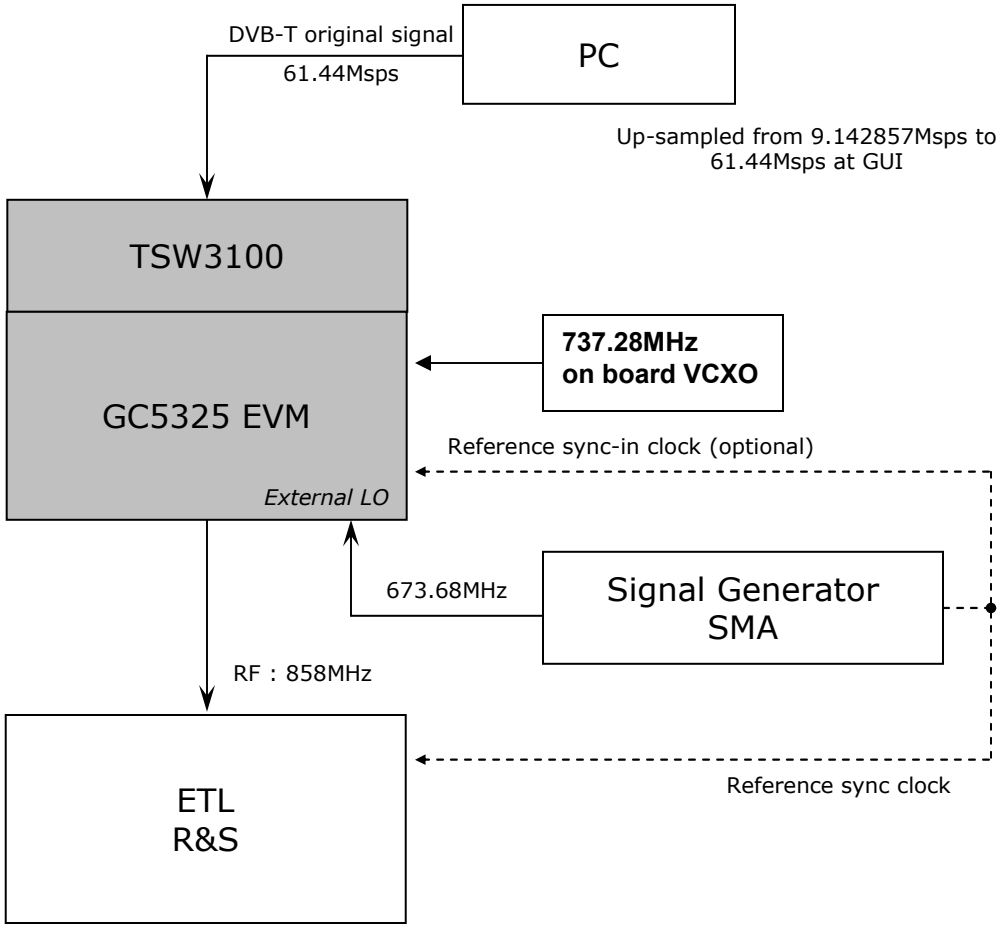
Test signal :

- 9.142857Msps with 64QAM of DVB-T
- BW=8MHz
- Mode=8k
- Code Rate=2/3
- Guard Interval=1/8

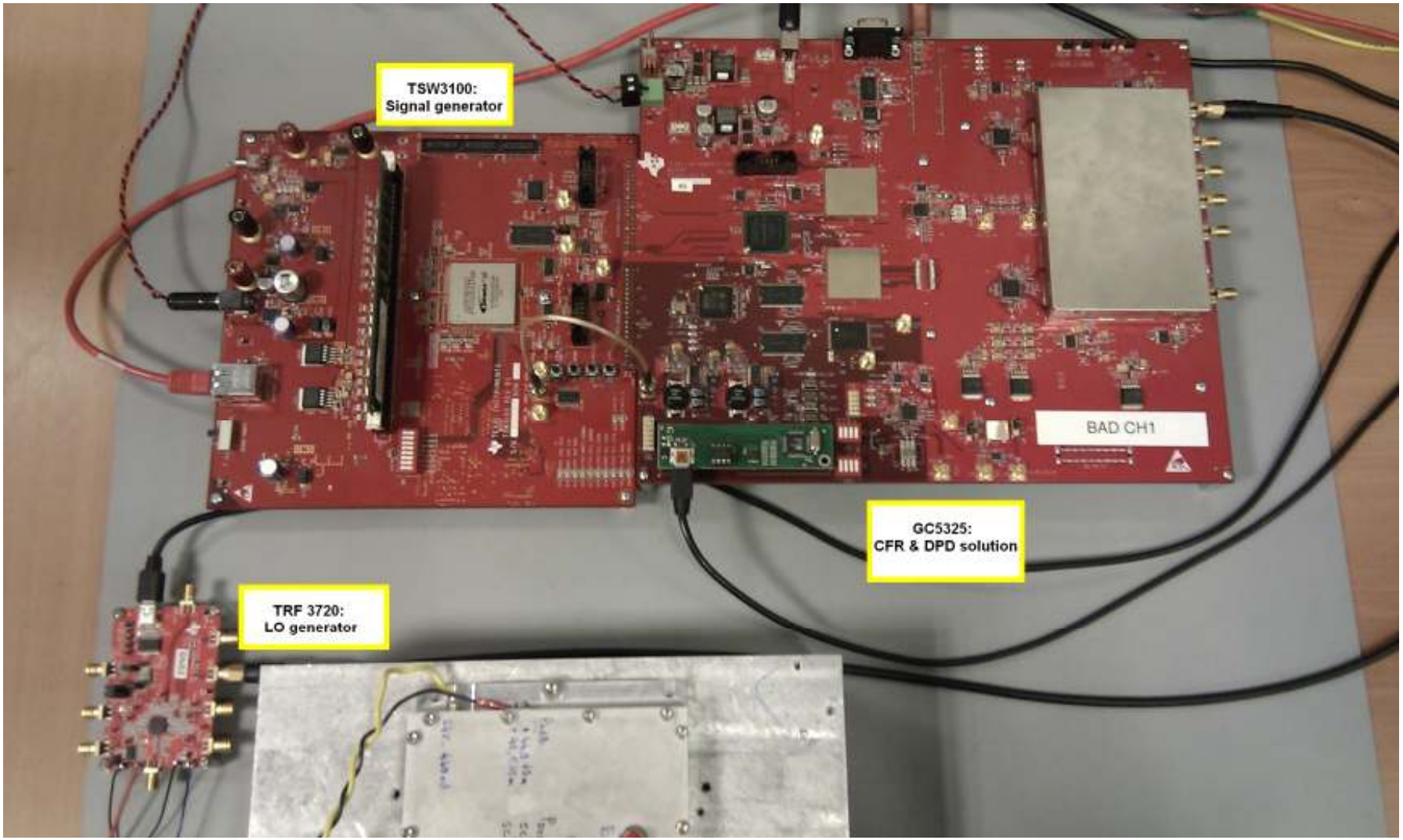
- RF : 826MHz
- IF : 184.32MHz
- Target MER : < -36dB
- External LO (SMA) : 641.68MHz/0dBm
  (Need Adjustment of level depending Signal Generator)
- Measuring Equipment & S/W : ETL & SMA Measurement Suite from R&S
- Target board : TSW3100/GC5325 EVM



Test setup environment



GC5325 System Evaluation Kit



Crest Factor Reduction (CFR)

Objective 1: Minimize Peak-to-Average Ratio (PAR) while still maintaining an MER of <-30dB (depending on applications).

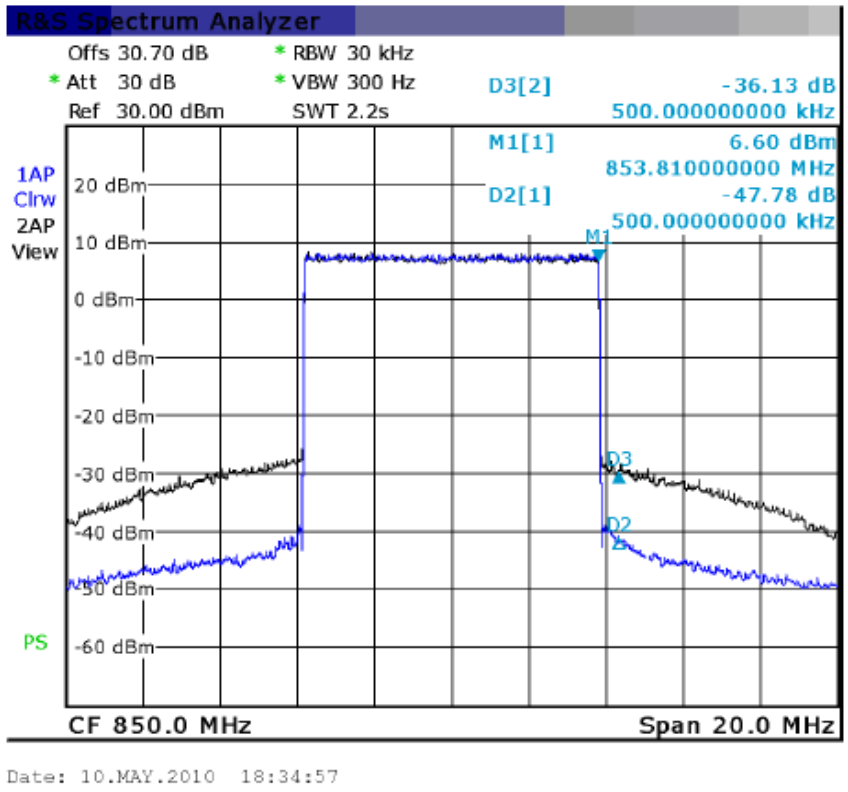
Objective 2: improve shoulders (ACPR) to maintain an -36dBc.

Results 1/6

The aim of the first measurement is **to get 36 dBc of shoulders at the output of the PA**, **without DPD**.

The input power in this case is = -10.3 *in P* dBm

Spectrum at the PA output

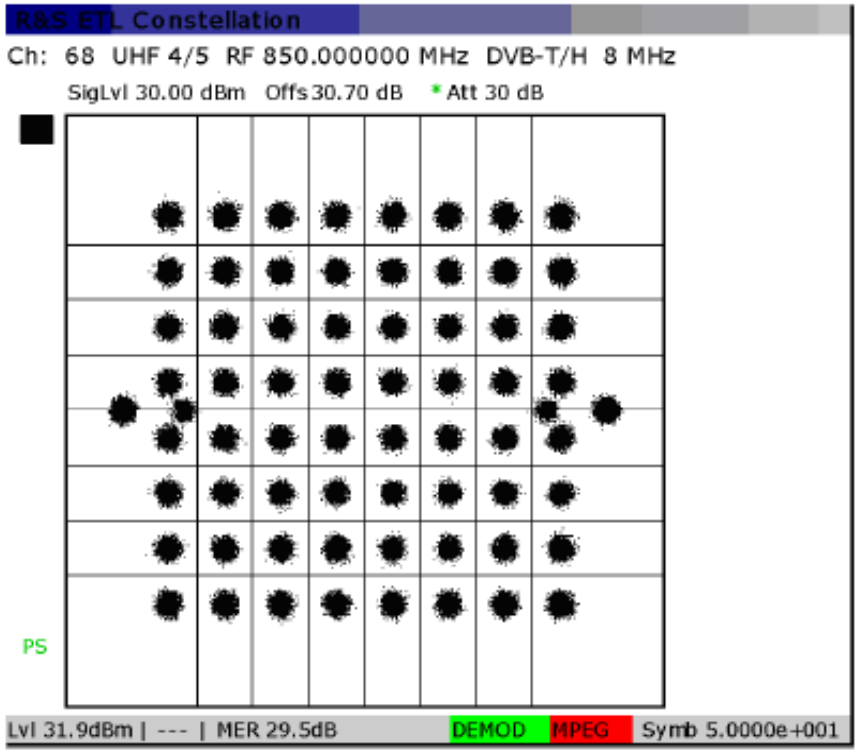
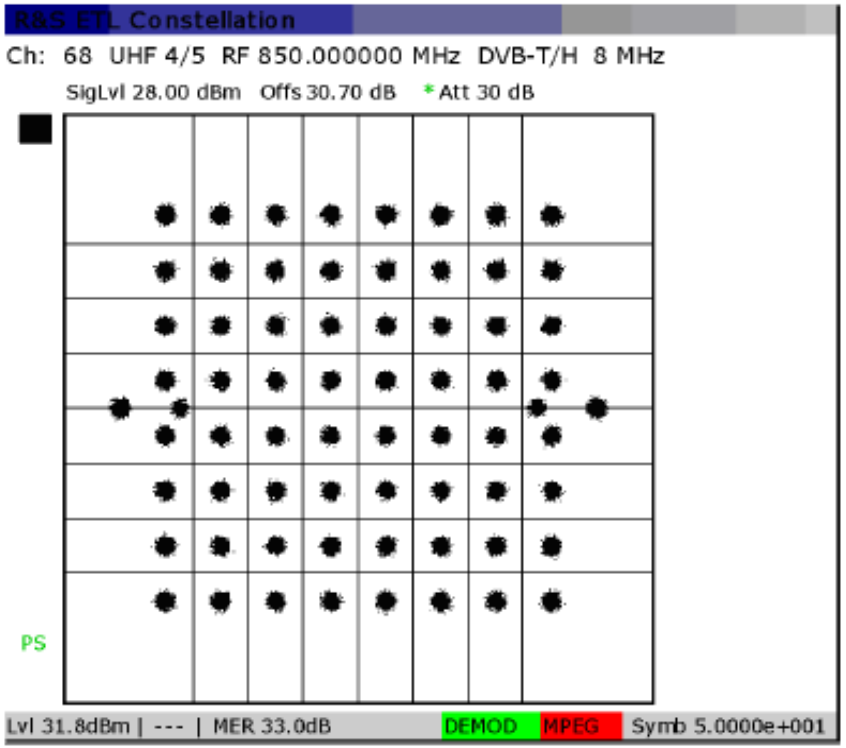


Without DPD:	With DPD:
Shoulders = 36.1dBc	Shoulders = 47.8 dBc

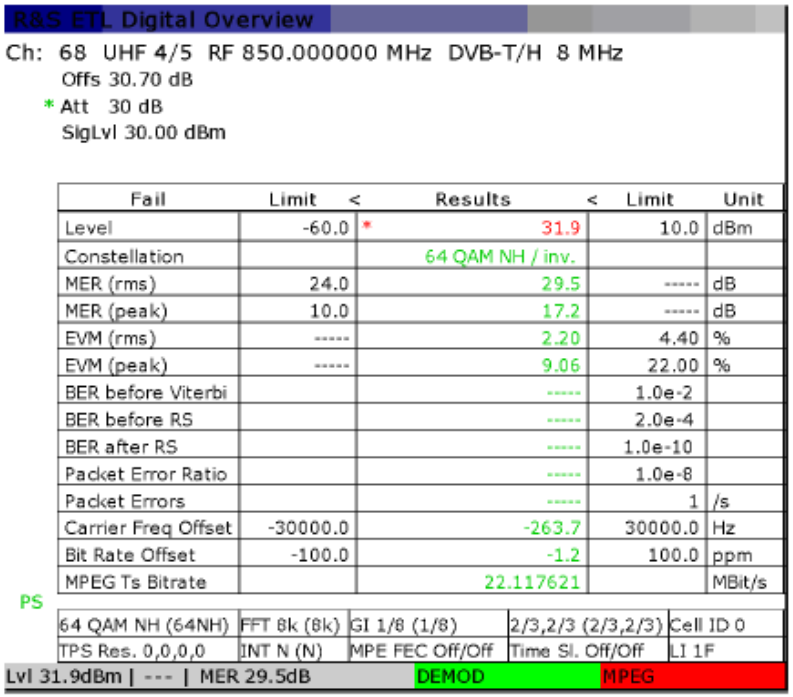
Shoulders improvement of 11.7 dB

Texas Instruments

Results 2/6

DPD OFF	DPD ON
	

Results 3/6


R&S ETL Digital Overview

Ch: 68 UHF 4/5 RF 850.000000 MHz DVB-T/H 8 MHz
Offs 30.70 dB
* Att 30 dB
SigLvl 30.00 dBm

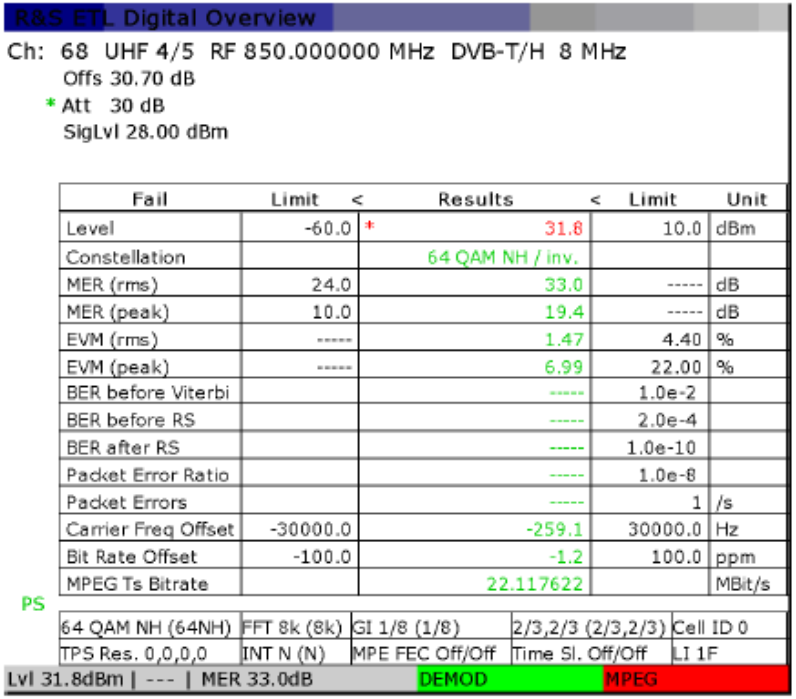
Fail	Limit	<	Results	<	Limit	Unit
Level	-60.0	*	31.9		10.0	dBm
Constellation			64 QAM NH / inv.			
MER (rms)	24.0		29.5		-----	dB
MER (peak)	10.0		17.2		-----	dB
EVM (rms)	-----		2.20		4.40	%
EVM (peak)	-----		9.06		22.00	%
BER before Viterbi			-----		1.0e-2	
BER before RS			-----		2.0e-4	
BER after RS			-----		1.0e-10	
Packet Error Ratio			-----		1.0e-8	
Packet Errors			-----		1	/s
Carrier Freq Offset	-30000.0		-263.7		30000.0	Hz
Bit Rate Offset	-100.0		-1.2		100.0	ppm
MPEG Ts Bitrate			22.117621			MBit/s

PS

64 QAM NH (64NH)	FFT 8k (8k)	GI 1/8 (1/8)	2/3,2/3 (2/3,2/3)	Cell ID 0
TPS Res. 0,0,0,0	INT N (N)	MPE FEC Off/Off	Time Sl. Off/Off	LI 1F

Lvl 31.9dBm | --- | MER 29.5dB DEMOD MPEG

Date: 10.MAY.2010 18:32:19


R&S ETL Digital Overview

Ch: 68 UHF 4/5 RF 850.000000 MHz DVB-T/H 8 MHz
Offs 30.70 dB
* Att 30 dB
SigLvl 28.00 dBm

Fail	Limit	<	Results	<	Limit	Unit
Level	-60.0	*	31.8		10.0	dBm
Constellation			64 QAM NH / inv.			
MER (rms)	24.0		33.0		-----	dB
MER (peak)	10.0		19.4		-----	dB
EVM (rms)	-----		1.47		4.40	%
EVM (peak)	-----		6.99		22.00	%
BER before Viterbi			-----		1.0e-2	
BER before RS			-----		2.0e-4	
BER after RS			-----		1.0e-10	
Packet Error Ratio			-----		1.0e-8	
Packet Errors			-----		1	/s
Carrier Freq Offset	-30000.0		-259.1		30000.0	Hz
Bit Rate Offset	-100.0		-1.2		100.0	ppm
MPEG Ts Bitrate			22.117622			MBit/s

PS

64 QAM NH (64NH)	FFT 8k (8k)	GI 1/8 (1/8)	2/3,2/3 (2/3,2/3)	Cell ID 0
TPS Res. 0,0,0,0	INT N (N)	MPE FEC Off/Off	Time Sl. Off/Off	LI 1F

Lvl 31.8dBm | --- | MER 33.0dB DEMOD MPEG

Date: 10.MAY.2010 19:44:49

$P_{out} = 31.8$ **dBm, with** $P_{in} = -10.3$ **dBm (**$G = 42.2$ **dB)**

With DPD, MER improves of 3.5 dB

1.5W

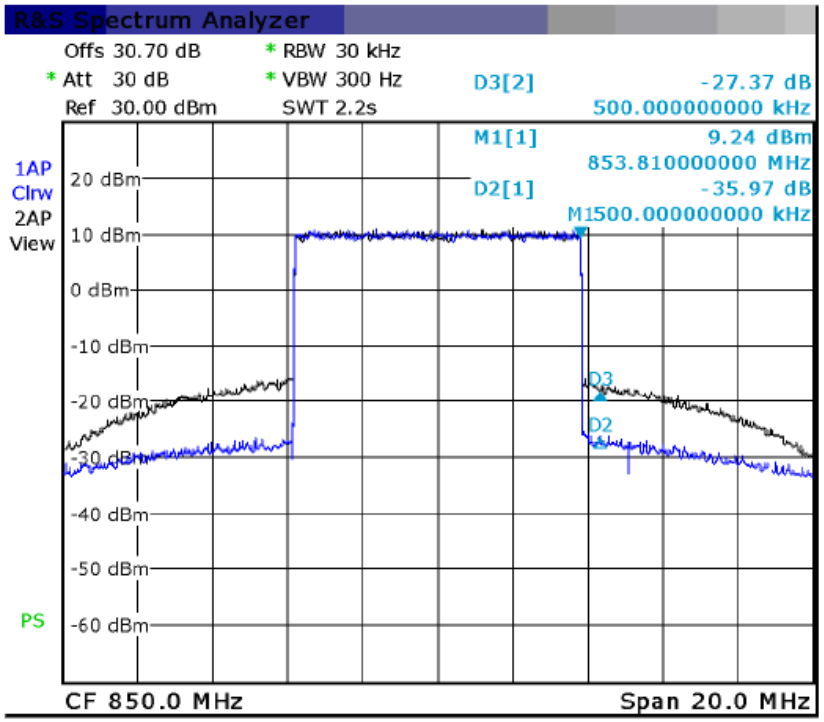
3dB MER improvement = doubling the zone coverage

Results 4/6

The aim of the first measurement is **to get 36 dBc of shoulders at the output of the PA**, **with DPD**.

The input power in this case is = -7.25 *in P* dBm

Spectrum at the PA output

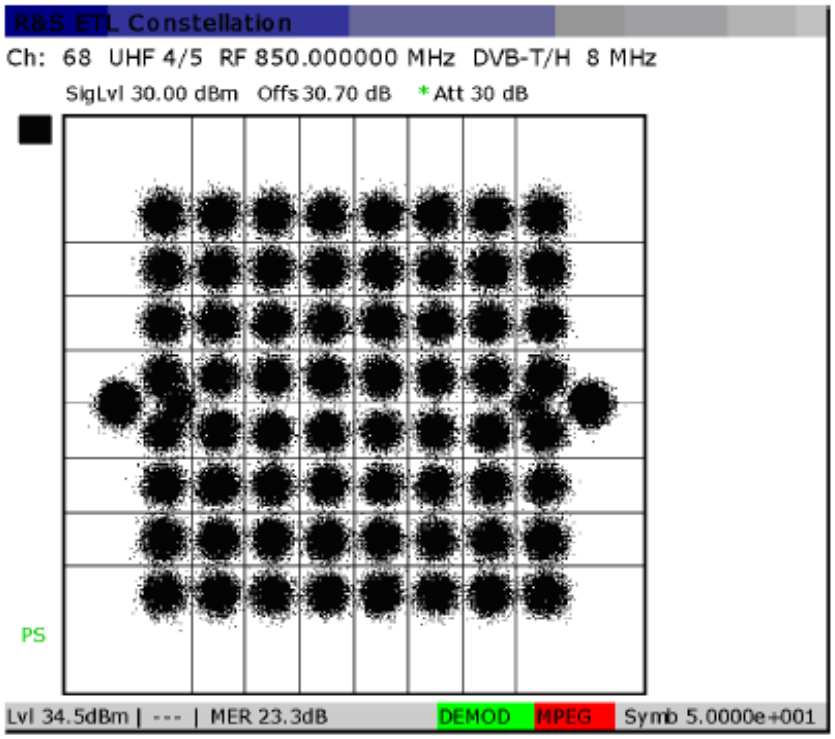
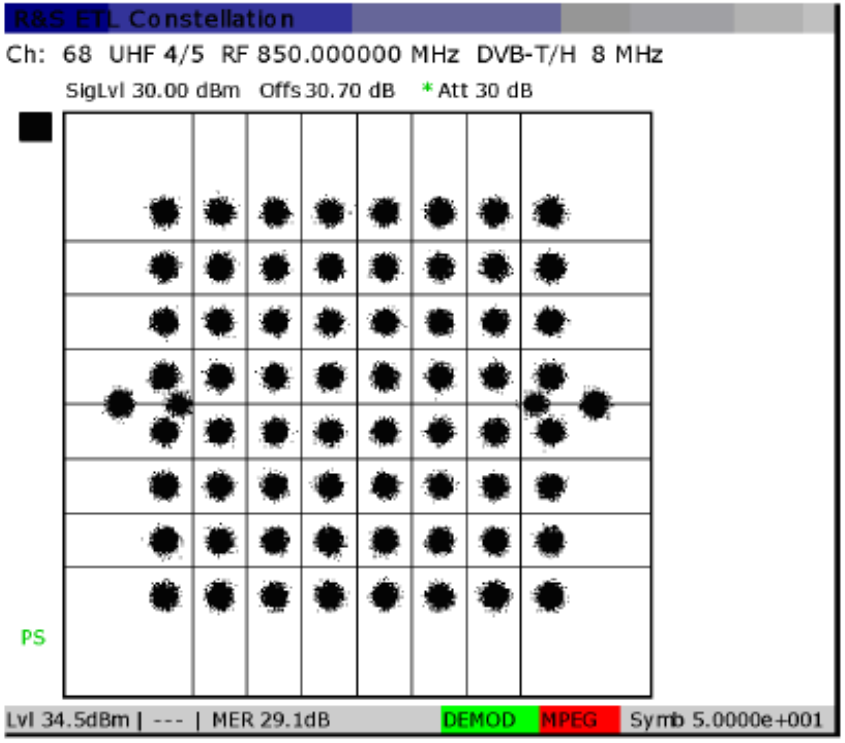


Without DPD:	With DPD:
Shoulders = 27.4 dBc	Shoulders = 36 dBc

Shoulders improvement s of 8.6 dB

Texas Instruments

Results 5/6

DPD OFF	DPD ON
	

Results 6/6

R&S ETL Digital Overview

Ch: 68 UHF 4/5 RF 850.000000 MHz DVB-T/H 8 MHz
Offs 30.70 dB
* Att 30 dB
SigLvl 30.00 dBm

Fail	Limit	<	Results	<	Limit	Unit
Level	-60.0	*	34.4		10.0	dBm
Constellation			64 QAM NH / inv.			
MER (rms)	24.0	*	23.4		-----	dB
MER (peak)	10.0		11.9		-----	dB
EVM (rms)	-----	*	4.45		4.40	%
EVM (peak)	-----		16.70		22.00	%
BER before Viterbi			-----		1.0e-2	
BER before RS			-----		2.0e-4	
BER after RS			-----		1.0e-10	
Packet Error Ratio			-----		1.0e-8	
Packet Errors			-----		1	/s
Carrier Freq Offset	-30000.0		-261.4		30000.0	Hz
Bit Rate Offset	-100.0		-1.2		100.0	ppm
MPEG Ts Bitrate			22.117621			MBit/s

PS

64 QAM NH (64NH)	FFT 8k (8k)	GI 1/8 (1/8)	2/3,2/3 (2/3,2/3)	Cell ID 0
TPS Res. 0,0,0,0	INT N (N)	MPE FEC Off/Off	Time Sl. Off/Off	LI 1F

Lvl 34.4dBm | --- | MER 23.4dB DEMOD MPEG

Date: 10.MAY.2010 18:53:22

R&S ETL Digital Overview

Ch: 68 UHF 4/5 RF 850.000000 MHz DVB-T/H 8 MHz
Offs 30.70 dB
* Att 30 dB
SigLvl 30.00 dBm

Fail	Limit	<	Results	<	Limit	Unit
Level	-60.0	*	34.5		10.0	dBm
Constellation			64 QAM NH / inv.			
MER (rms)	24.0		29.2		-----	dB
MER (peak)	10.0		16.5		-----	dB
EVM (rms)	-----		2.27		4.40	%
EVM (peak)	-----		9.78		22.00	%
BER before Viterbi			-----		1.0e-2	
BER before RS			-----		2.0e-4	
BER after RS			-----		1.0e-10	
Packet Error Ratio			-----		1.0e-8	
Packet Errors			-----		1	/s
Carrier Freq Offset	-30000.0		-262.1		30000.0	Hz
Bit Rate Offset	-100.0		-1.2		100.0	ppm
MPEG Ts Bitrate			22.117621			MBit/s

PS

64 QAM NH (64NH)	FFT 8k (8k)	GI 1/8 (1/8)	2/3,2/3 (2/3,2/3)	Cell ID 0
TPS Res. 0,0,0,0	INT N (N)	MPE FEC Off/Off	Time Sl. Off/Off	LI 1F

Lvl 34.5dBm | --- | MER 29.2dB DEMOD MPEG

Date: 10.MAY.2010 18:46:53

$P_{out} = 34.5$ **dBm, with** $P_{in} = -7.25$ **dBm (**$G = 42.2$ **dB)**

With DPD, MER improves of 5.8 dB

3W

3dB MER improvement = increasing by 4 the coverage

Conclusion

- With Texas Instruments' CFR/DPD solution, the PA can achieve a higher output power with CFR versus no CFR while maintaining the same ACLR performance.

- Measurements confirm about 46% increase in PA output power with the addition of CFR to DPD.

- There is the potential to increase PA output power even more (increase PA efficiency), while still maintaining the same ACLR performance, by increasing CFR at the expense of MER.

Thank You!