CC430: MCUs for space constrained, ultra-low-power, wireless applications

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Introduction to CC430

1. Brief introduction to CC430
2. Block Diagram of the CC430F6137 & MSP430 Peripherals
3. Derivatives of the CC430F61xx & CC430F51xx Family
4. Radio Interface & Transceiver
5. Tools Overview

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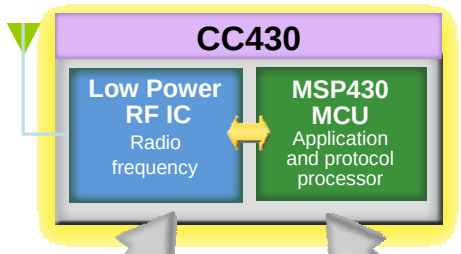
What is the CC430?



Low-power RF SoC

Low Power RF Transceiver

- High sensitivity
- Low current consumption
- Excellent blocking performance
- Flexible data rate & modulation format
- Backwards compatible

MSP430 MCU

- Market's lowest power MCU
- High analog performance
- High level of integration
- Ease of development
- Sensor interface

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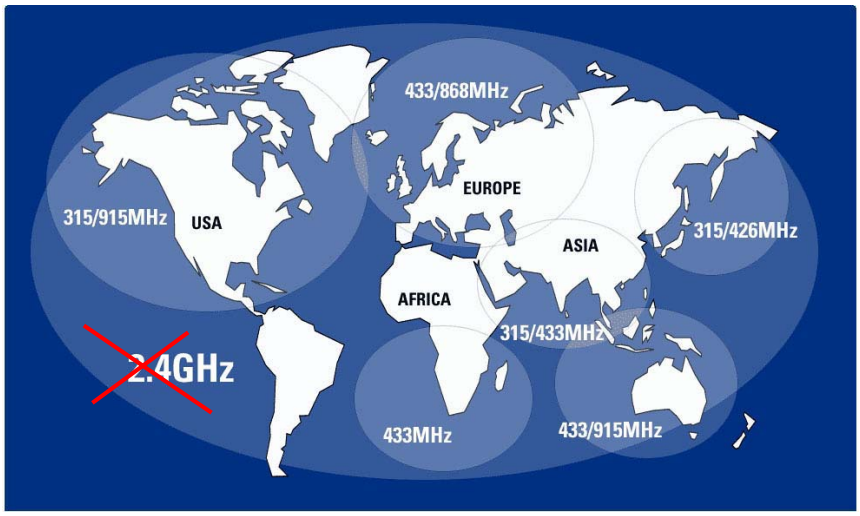
CC430 Overview

- MSP430 sub-family
  - 7 derivatives
  - MCU architecture based on the latest MSP430F5xx technology
  - Fully integrated < 1GHz radio based on the CC1101 transceiver
  - MSP430 <> CC1101 radio interface called RF1A
- What do the “CC” and “430” stand for?
  - CC for TI LPW Short Range Device
  - 430 for MSP430 microcontrollers
- What does RF1A stand for?
  - R for Radio
  - F for Frequency
  - 1 for Sub-1GHz Transceiver
  - A for the first of MSP430 based RF SoCs

Supported Frequency Bands



Supports 300–348MHz, 387–464MHz, 779–928MHz

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RF1A Radio Module

New modules only on CC430F613x: Comparator B, LCD B, AES128, Shared Reference

New 5xx modules: UCS, PMM, CRC16

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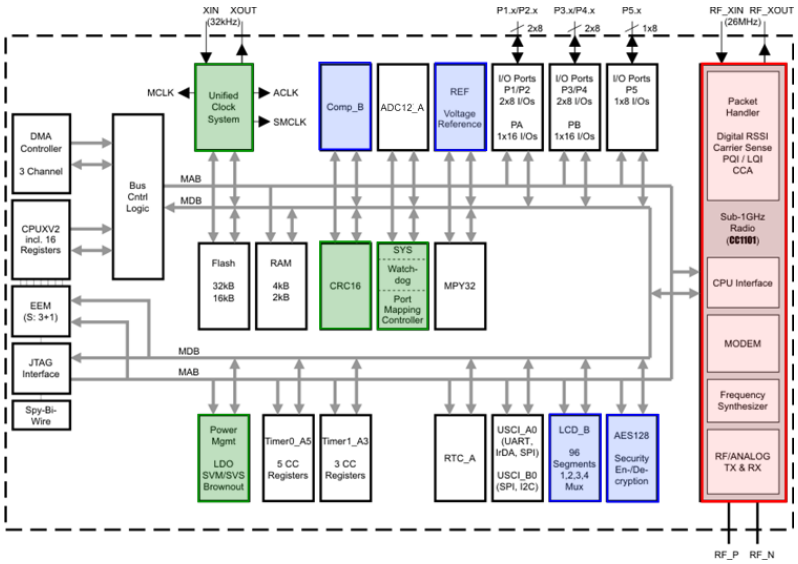
CC430F613x Block Diagram



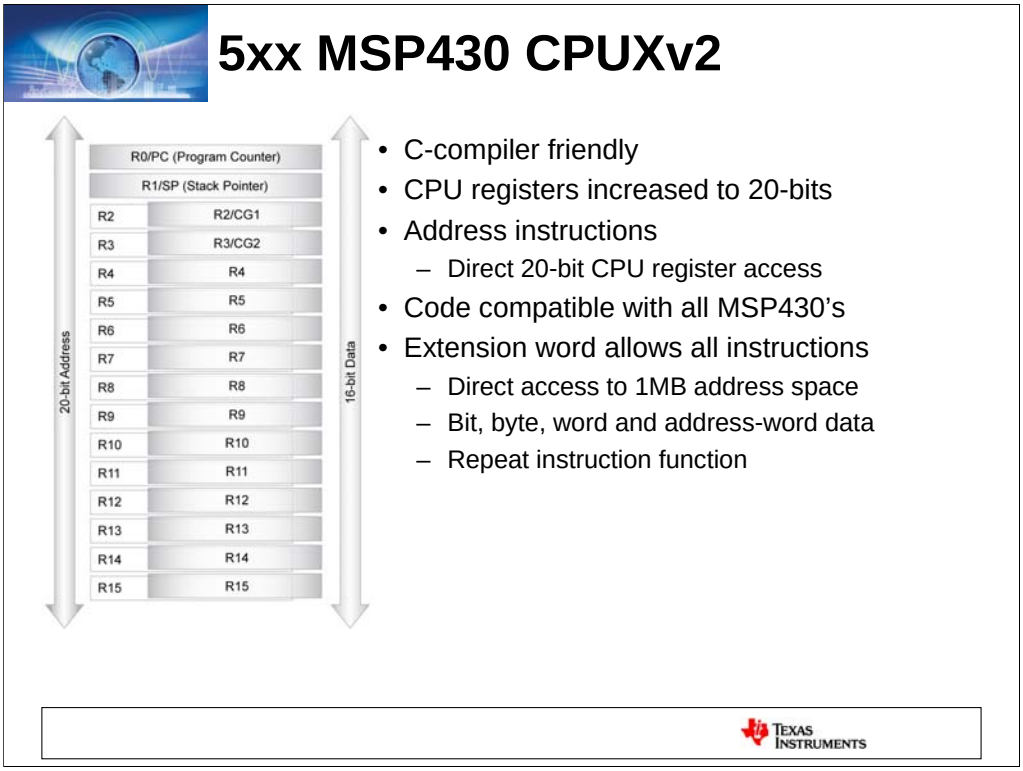
RF1A Radio Module

New modules only on CC430F613x:

Comparator B, LCD B, AES128, REF, Port Mapping Controller

New 5xx modules:

UCS, PMM, CRC16



The new MSP430X architecture is 100% compatible with the MSP430 architecture and allows 16x more memory addressing page free using less code and fewer cycles.

The MSP430X is 100% compatible with the existing MSP430 allowing existing code libraries to be reused.

Extended addressing modes are incorporated that allow the existing MSP430 instruction set to operate page-free throughout the entire 1MB memory model with improved code density faster using fewer clock cycles. Extended instructions designed for the large memory allow optimal high-level code density with full backward compatibility, making it possible to develop very sophisticated real-time applications completely in modular C libraries.

The MSP430X executes MSP430 code unaltered in the compatible 64kB memory range. To further preserve compatibly, all MSP430X interrupt vectors, RAM and peripherals registers map exactly to the MSP430. The extended memory contains expanded code and data.

Existing MSP430 byte/word (.b/.w) addressing modes are expanded allowing direct access to 20-bit addresses (.a) fields which support 1MB (20-bit) program flow and pointer capability. This 20-bit address-word capability is accomplished for program flow, stack manipulation and pointer handling with same code density as the 16-bit MSP430 by using un-used bits in OP codes field. Additionally an extension word allows full 20-bit addressing for source and destination with any MSP430 instruction and addressing mode and added repetition capability.

Cycle counts have been reduced for several addressing modes and interrupt overhead allowing faster code execution.

Additional details regarding the MSP430X architecture can be found in the MSP430F4xx and MSP430F2xx users guides.

CC430 Memory Map

- Page-free 16-bit addressing
- RAM starts at 0x1C00 and is always a contiguous block
- Main flash start moves according to RAM
- Vector table starts at 0xFF80
- User-definable interface to the Boot Strap Loader (BSL)

Interrupt vectors	00FFFF 00FF80
Program	00FF7F 005C00
RAM 16 KB	005BFF 001C00
Factory data (4 x 128B)	001BFF 001A00
User Info segment A (128 B)	0019FF 001980
User Info segment B (128 B)	00197F 001900
User Info segment C (128 B)	0018FF 001880
User Info segment D (128 B)	00187F 001800
BSL segment 3 (512 B)	0017FF 001600
BSL segment 2 (512 B)	0015FF 001400
BSL segment 1 (512 B)	0013FF 001200
BSL segment 0 (512 B)	0011FF 001000
Peripherals 4 KB	000FFF 000000

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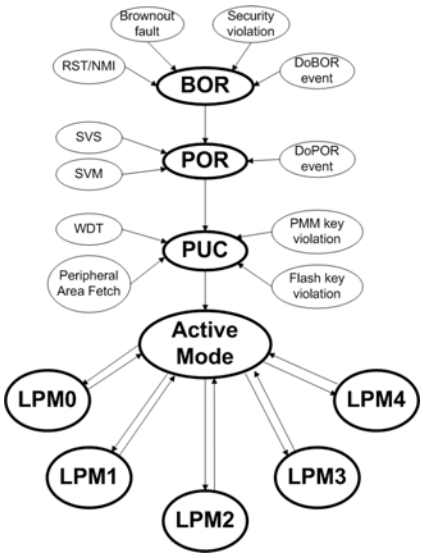
This slide shows some of the specifics

The memory map, like the 2xx and 4xx parts with > 64KB Flash, has kept its Interrupt vectors between 0xFF80 and 0xFFFF. The Factory Data was moved out of the Info segment memory to relieve the required management of any stored calibration constants, and we have made the Boot Strap Loader user-definable. Later in the presentation, we will discuss the new boot-strap loader in greater detail.

CC430 Operating Modes

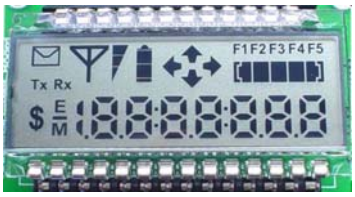


- LPM0 – LPM4 are the same as previous MSP430 generations
- BOR resets device, executes internal boot code, registers default
- SVS/M generate POR/interrupts in event of low voltage condition

This is a state diagram of the 5xx operating modes. If you know the previous MSP430 families, you should recognize the POR, PUC, ACTIVE & LOW POWER modes. The two additions are the BOR and some of the reset triggers. The BOR is not new, but rather re-classified as a deeper level of reset. It is always active, monitoring a Vcc voltage drop below 1.8V. LPM5, supported on other 5xx core devices, is not supported for the first part of the CC430.

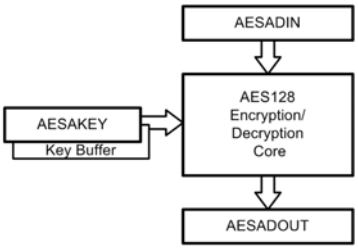
Two new triggers of a POR reset that should be highlighted include the SVS and SVM flags. These stem from the additional voltage monitoring designed into a new Power Management Module (PMM) for the 5xx, that sets a POR signal when a voltage dips below the SVS level and resets the POR signal when it climbs to a slightly higher SVM level, providing hysteresis for the voltage monitor.

LCD_B & AES128 Encryption / Decryption

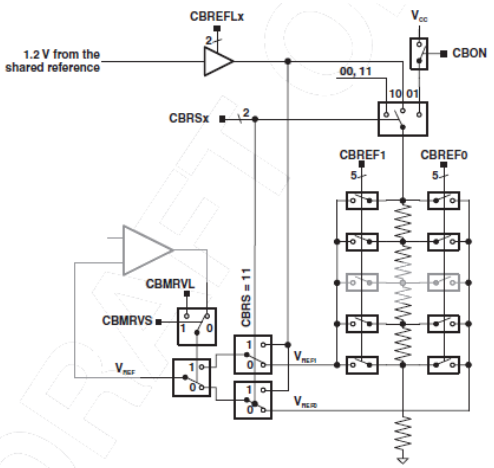


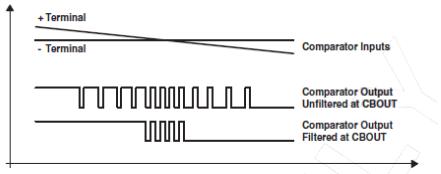
- Automatic LCD signal generation
- Blinking of individual segments
- Regulated charge pump
- Software-driver contrast control
- Integrated drivers to decouple LCD load from the bias generation

- Encryption and decryption according to AES FIPS PUB 197 with 128-bit key
- Key expansion for en- and decryption
- Off-line key generation for decryption
- AES ready interrupt flag



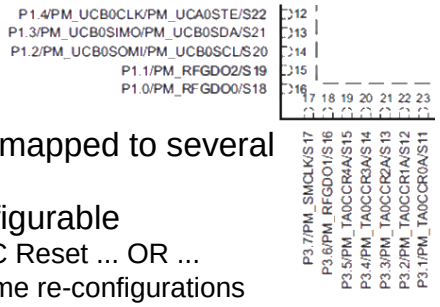
Comparator_B





- Selectable reference voltage generator, voltage hysteresis generator
- High-speed, normal, and ultra-low power modes
- Inverting and non-inverting terminal input multiplexer
- Internal output to Timer A capture
- Selectable RC filter for comparator output

Port Mapping



- Each output signal can be mapped to several output pins
- Mapping is runtime re-configurable
  - Single configuration per PUC Reset ... OR ...
  - PMARECFG bit allows runtime re-configurations
- Port mapping configuration is password protected
- Write access is locked when...
  - Invalid password is written while access is granted
  - Timeout counter reaches 32

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- Accessing the port mapping control registers has to be enabled by writing 02D52h to PMAPPWD register – similarly, a read of the PMAPPWD register results 096A5h
- There is a default mapping provided for any port pin on a given device

  - Different per device (see datasheet)

  - For every port pin a Px.y PxMAPy register is available.
- It is recommended to close a port mapping configuration sequence by writing a wrong password

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CC430 Derivatives

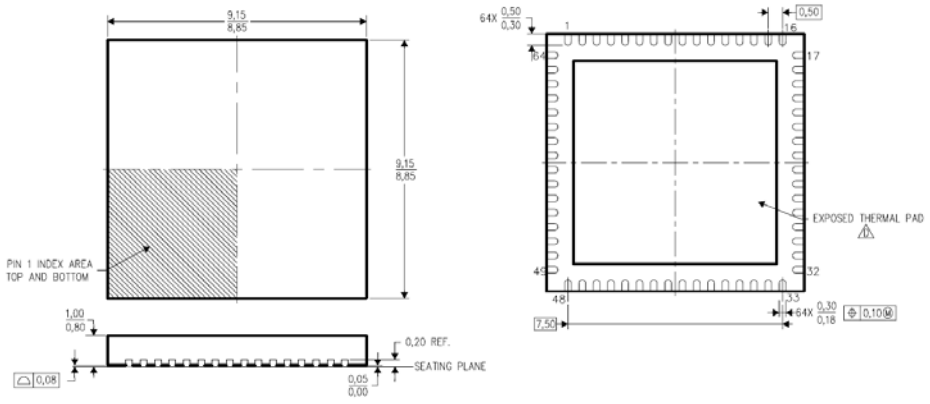
With LCD module

- **CC430F6137**
  (LCD, ADC, Comparator B, 64-Pin)
  - 32KB+512B FLASH
  - 4KB RAM
- **CC430F6135**
  (LCD, ADC, Comparator B, 64-Pin)
  - 16KB+512B FLASH
  - 2KB RAM
- **CC430F6126**
  (LCD, Comparator B, 64-Pin)
  - 32KB+512B FLASH
  - 2KB RAM
- **CC430F6125**
  (LCD, Comparator B, 64-Pin)
  - 16KB+512B FLASH
  - 2KB RAM

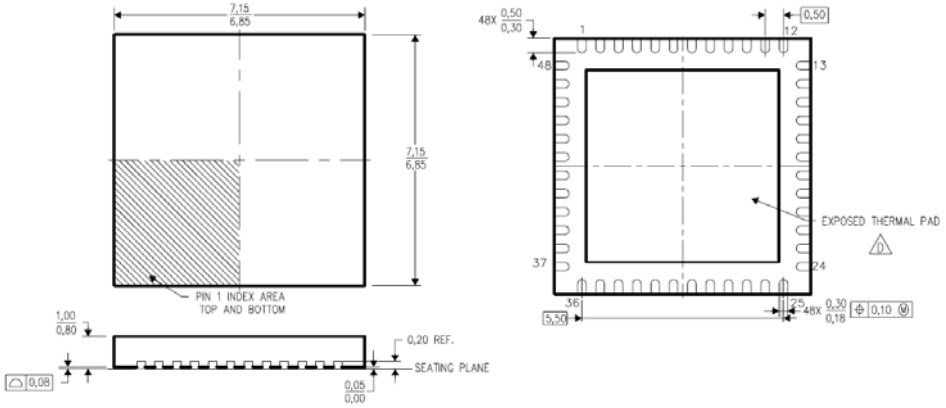
Without LCD module

- **CC430F5137**
  (ADC, Comparator B, 48-Pin)
  - 32KB+512B FLASH
  - 4KB RAM
- **CC430F5135**
  (ADC, Comparator B, 48-Pin)
  - 16KB+512B FLASH
  - 2KB RAM
- **CC430F5133**
  (ADC, Comparator B, 48-Pin)
  - 8KB+512B FLASH
  - 2KB RAM

CC430 – 64-pin RGC



CC430 – 48-pin RGZ



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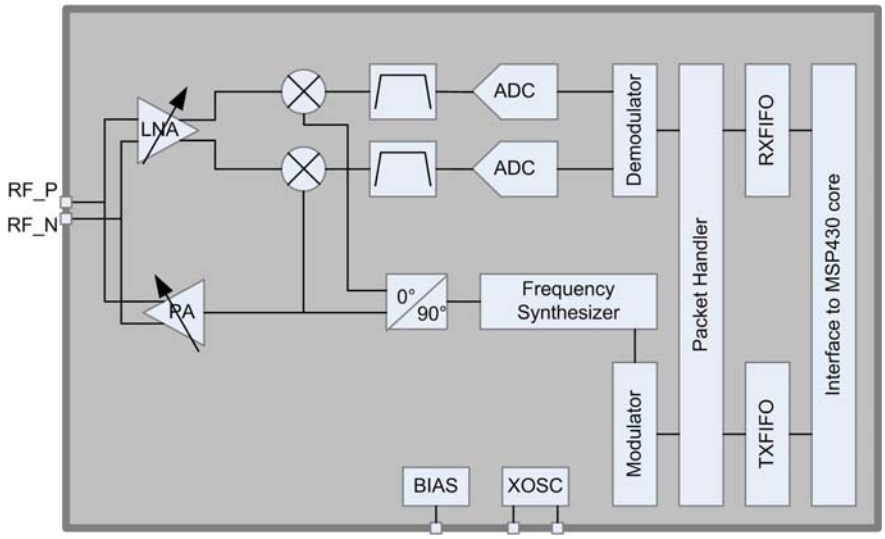
CC430 Radio


RF_P
RF_N
LNA
PA
ADC
ADC
Demodulator
0°
90°
Frequency Synthesizer
Modulator
BIAS
XOSC
Packet Handler
RXFIFO
TXFIFO
Interface to MSP430 core

CC430 Radio – TX Path

- **Power Amplifier (PA)**
  - **+10dBm output power to 50Ohm**
  - **Built in attenuation steps down to -30dBm**
  - **Due to built-in LDO, output power is stable across operating range (1.8V – 3.6V)**
  - **Output is balanced >> requires a balun at a single ended antenna**
- **PA Table**
  - **Used for PA power ramp up and ramp down**
  - **Cleaner RF environment in networks with a lot of TDMA transmissions**
  - **PA power can be limited to the necessary minimum**
    - **Useful in achieving the best power consumption budgets**

PA Table can be used to meet stringent certification requirements on power ramping from standby. No huge power load changes from 0 to max. causing VCO sweeps over the adjacent channels.

CC430 Radio – TX Path

- **Synthesizer**
  - Generates the required output frequencies
  - Reference crystal frequency range 26MHz – 27MHz
  - Very high frequency resolution (397Hz – 412Hz)
    - Can be used to correct tolerance of the reference crystal as well as drift due to temperature
- **Modulator**
  - Supports frequency modulation schemes:
    - 2-FSK, 2-GFSK and MSK
  - Supports amplitude modulation schemes:
    - ASK, OOK
  - Programmable data rates: 1.2kBaud – 500kBaud
  - Supports automatic Manchester encoding, when enabled

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1ppm at 868MHz are 868Hz >> resolution better than 0.5ppm!

Very high frequency resolution, can be used to correct frequency tolerance of the reference crystal.

This enables also compensation of the frequency drift due to temperature.

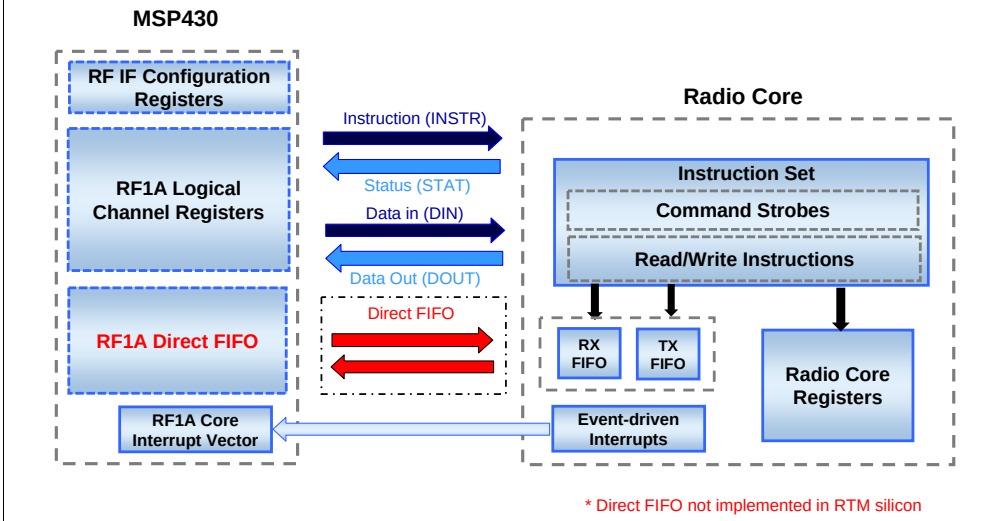
CC430 Radio – RX path

868 MHz, 1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		–111		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 18.0 mA to 15.7 mA at sensitivity limit. The sensitivity is typically reduced to -109 dBm
Saturation		–14		dBm	`FIFOTHR.CLOSE_IN_RX=0`. See more in DN010 [11]
Adjacent channel rejection		37		dB	Desired channel 3 dB above the sensitivity limit. 100 kHz channel spacing
Alternate channel rejection		37		dB	Desired channel 3 dB above the sensitivity limit. 100 kHz channel spacing
					See Figure 2for plot of selectivity versus frequency offset
Image channel rejection, 868MHz		31		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit

868 MHz, 38.4 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		–103		dBm	
Saturation		–16		dBm	`FIFOTHR.CLOSE_IN_RX=0`. See more in DN010 [11]
Adjacent channel rejection		20		dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing
Alternate channel rejection		30		dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing
					See Figure 3 for plot of selectivity versus frequency offset
Image channel rejection, 868MHz		23		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit

CC1101 data, characterization of CC430 not yet complete.

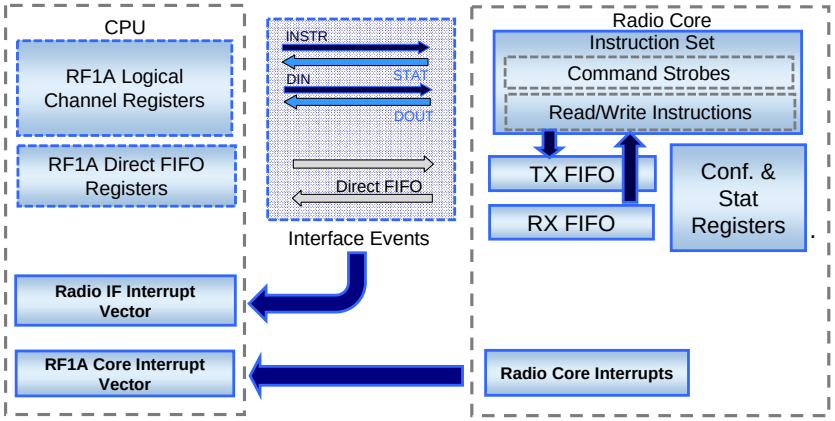
RF1A Interface



Radio Interface = three communication paths

1. Logical Communication Channels with 4 Registers for Instructions (INSTR), Radio Status (STAT), Data In (DIN), & Data Out (DOUT)
2. Direct FIFO TX/RX Buffer Access
3. Radio Core Events Mapped to CPU's RF1A Interrupt Vector

RF1A Interrupts



RF1AIFIV: RF1A Radio **Interface** Interrupts

RF1AIV: RF1A Radio **Core** Interrupts

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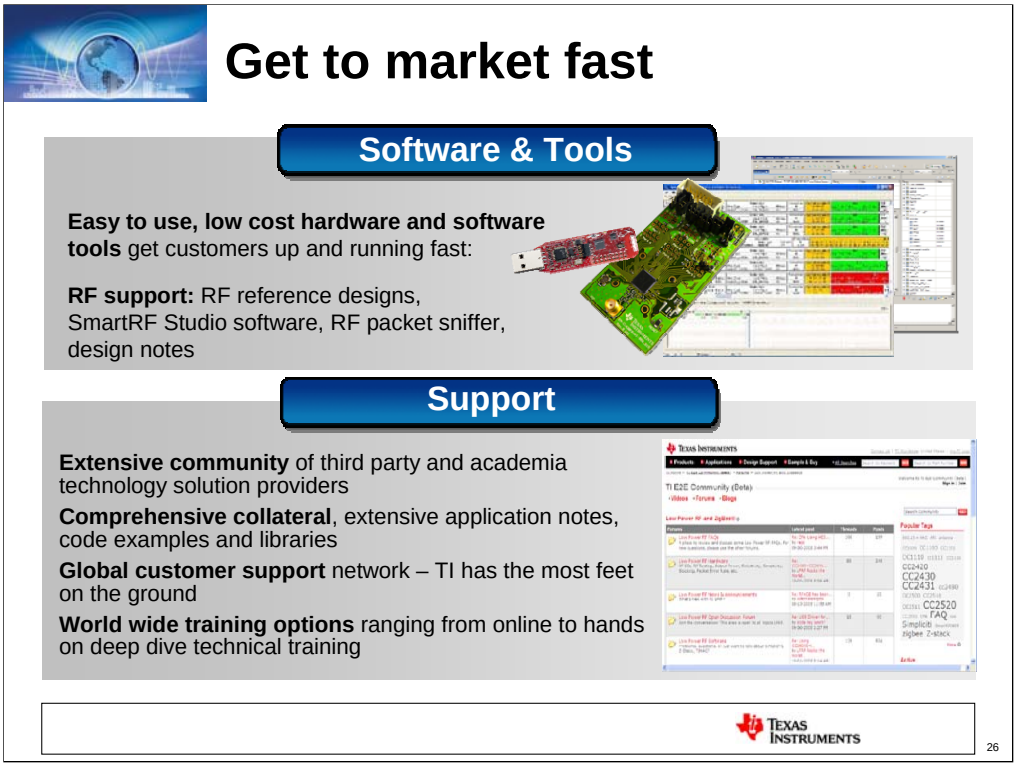


RF: TI takes the mystery out of RF design with broad support, reference designs, etc.

RF: Black boxing the RF, making development easier, don't have to have a wireless expert on staff

Easy to use, low cost hardware and software tools get customer up and running fast.

Both 430 and RF: Extensive community of third Party and academia technology solution providers (online RF and MCU community sites give engineers immediate access to a pool of experts) (Capture a web page for this?)

TI: Comprehensive collateral, extensive application notes, code examples and libraries.

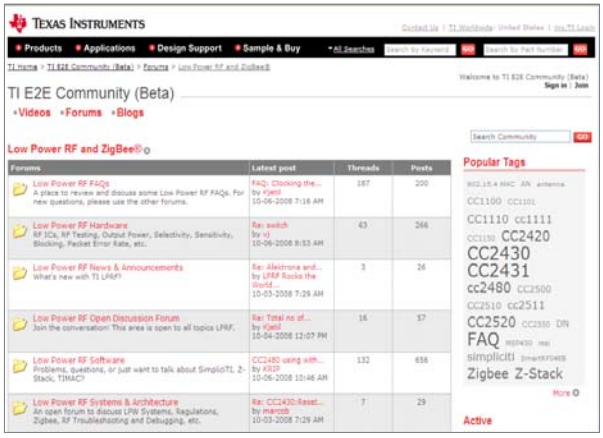
TI: Global customer support network – TI has the most "feet on the ground."

TI: World wide training options ranging from online to hands on deep dive technical training

TI is taking the mystery out of RF design with RF reference designs, SmartRF Studio software, RF packet sniffer and design notes. Designers can get up and running easily with a CC430 development kit and free tools, such as the Code Composer Essentials (CCE) or IAR Integrated Development Environment (IDE). Third-party support, training and university programs, code examples and libraries also facilitate ease of use and shorten time to market.

Additionally, TI's Low-Power RF and microcontroller E2E online communities offer the opportunity to interact directly with engineers and other experts to ask questions, share knowledge, explore ideas and help solve problems. Go to community.ti.com , sign-up, subscribe to a forum and start exploring the TI E2E online community today.

Vibrant E2E community



- **Share knowledge, explore ideas, solve problems**
- **Direct access to TI engineer expertise**

Visit http://community.ti.com to engage in an interactive, forum discussion

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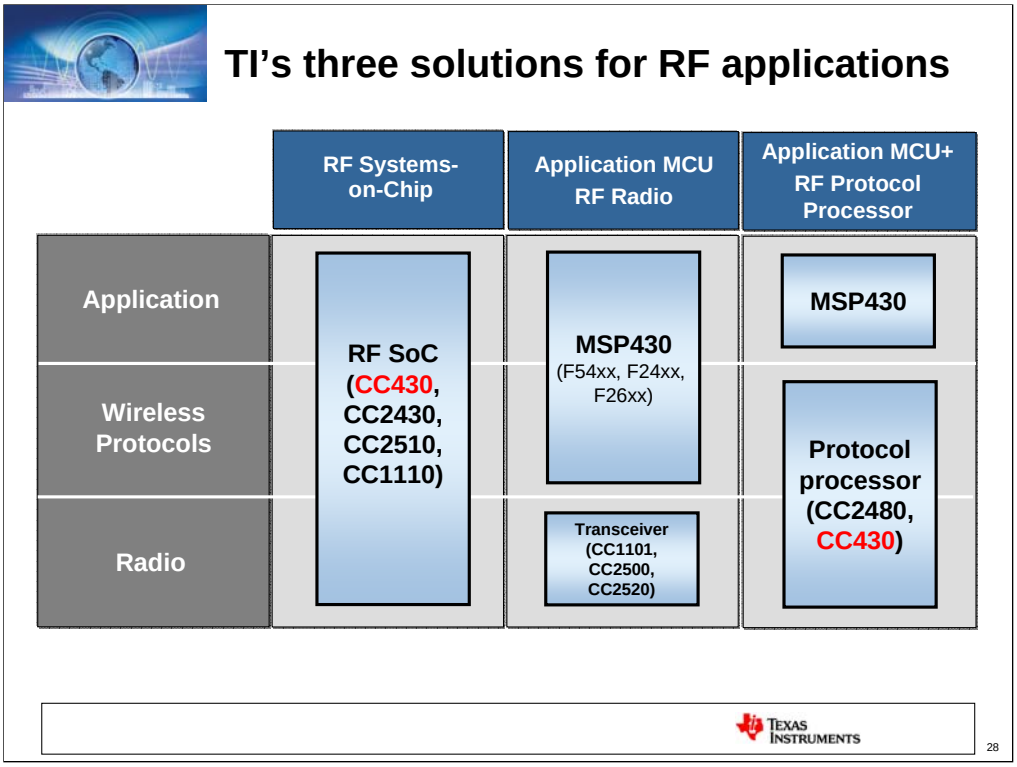
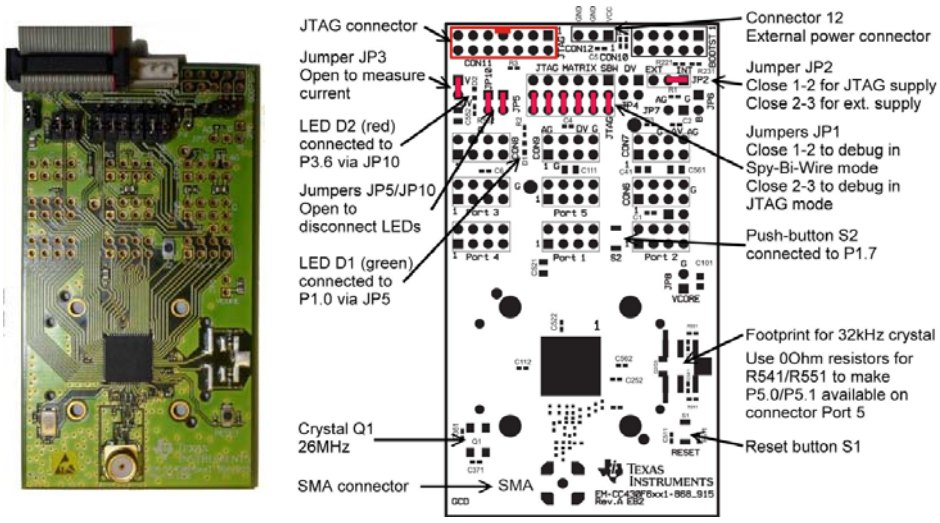
Additionally, TI's Low-Power RF and microcontroller E2E online communities offer the opportunity to interact directly with engineers and other experts to ask questions, share knowledge, explore ideas and help solve problems. Go to community.ti.com , sign-up, subscribe to a forum and start exploring the TI E2E online community today.

We can use the general address for now



De facto standard for ultra low power and ease of use now has an RF extension.

EM-CC430F6xx1-868_915



The main digital logic of the MSP430 device requires a voltage that is lower than the range allowed by

DVCC. For this reason, the PMM incorporates an integrated low dropout (LDO) voltage regulator that

generates a secondary core voltage rail, VCORE.

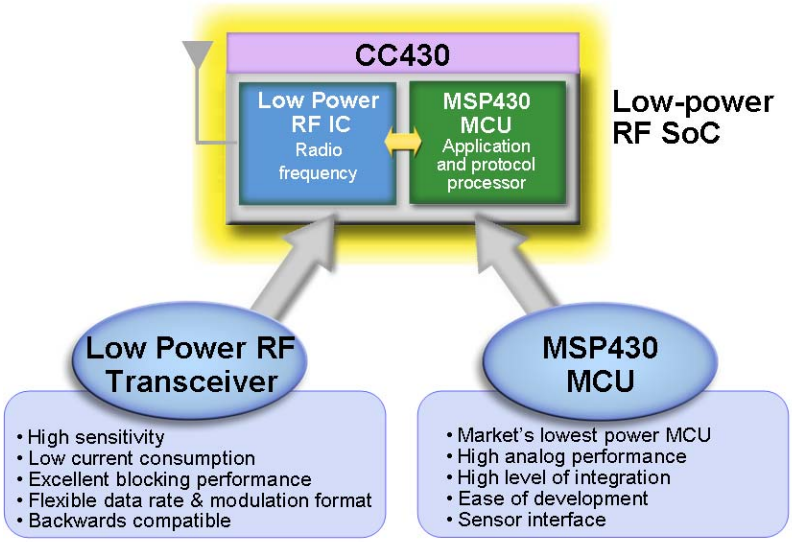
CC430 Sample Kit Contents

- 2 x EM-CC430F6xx1-868/915 evaluation modules
- 2 x 868 / 915MHz antennas
- 2 x battery holders including four AAA batteries and connector power cables
- 18 x PCB 2x4 pin headers
- 1 x 32kHz Crystal
- 1 x CC430F6137 sample kit documentation

Sample Kit Documentation

- CC430 Hardware
  - User Guide, Datasheet, EVM Design Files, Errata
- CC430 Software
  - CC430F6137 C Code Examples
  - Example RF software in CCE & IAR, 868 & 915 MHz
- Development Tools
  - CCE v3 & CC430 CCE Patch
  - IAR Kickstart & CC430 IAR Kickstart Patch
  - Installation and respective FET User Guides
- Getting Started.pdf

The End


CC430
Low Power RF IC
Radio frequency
MSP430 MCU
Application and protocol processor
Low-power RF SoC
Low Power RF Transceiver
• High sensitivity
• Low current consumption
• Excellent blocking performance
• Flexible data rate & modulation format
• Backwards compatible
MSP430 MCU
• Market's lowest power MCU
• High analog performance
• High level of integration
• Ease of development
• Sensor interface