# Clocking To Maximize HS Signal Chain Performance

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# Outline

- What is Jitter?
- Jitter and SNR
- Phase Noise Measurements
- Phase-Locked Loops
- Loop Filter Design
- Clocking HS Data Converters
- Signal Integrity Issues
- Summay

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# What is Jitter?

Jitter is any edge deviation from ideal. Jitter is composed of both deterministic and random (Gaussian) content.

**Causes of deterministic jitter:**

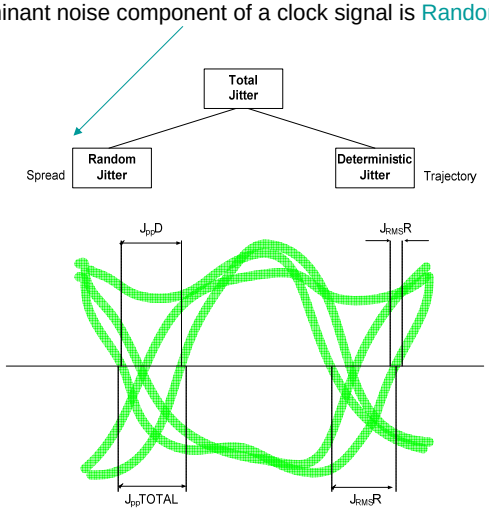
- Duty cycle distortion of a signal
- Simultaneous switching outputs
- Signal cross talk and EMI
- Substrate current, noise on power planes, GND reference shift
- Data pattern dependant signal distortion

**Causes of random jitter:**

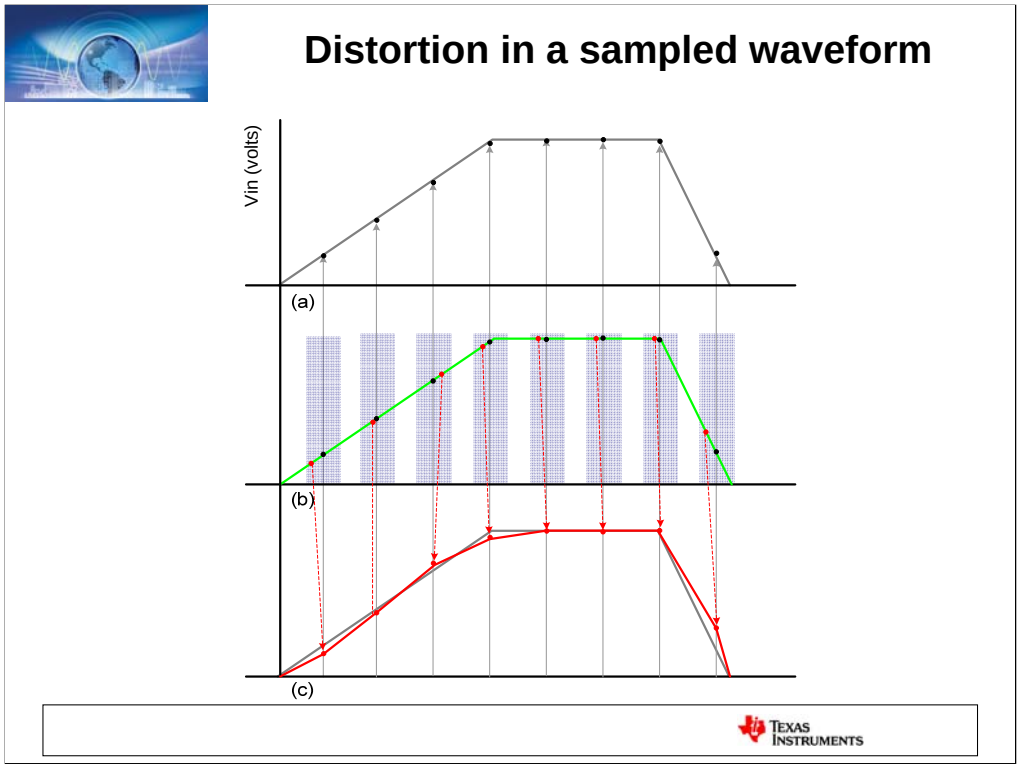
- Thermal noise of semiconductors ( VCO,Charge Pump)
- **1/f noise** causing low frequency jitter components

# Elements of Total Jitter

The dominant noise component of a clock signal is Random Jitter.




Random Jitter (RMS jitter) is derived from the phase noise plot of the clock signal.




Consider the three plots above.

The center plot represents a trapezoidal pulse (perhaps as captured on an oscilloscope). It is a continuous waveform (i.e. for each position in time on the horizontal axis there is a corresponding voltage on the horizontal axis).

The Black dots represent ideal sample points and these points are transposed to the plot on the top. The original waveform can be determined by connecting the points.

Superimposed over the center plot are regions which represent a possible location of a sampling point if there is jitter on the sample clock. While the top plot contains points which appear in the exact center of these regions, the actual sample point can appear randomly anywhere in the region. Some possible sample points are show as red dots on the center plot. These values are transposed to the plot on the bottom. Notice the value recorded is not the correct voltage level because it is sampled at the incorrect location. It is transposed to the point in time in which the sample was ideally to be taken (in the center of the sampling region). This results in the signal being distorted as shown by the red trace on the bottom plot.

## Signal to Noise Ratio

Assuming a sinusoidal input for $V_{in}$ we have,

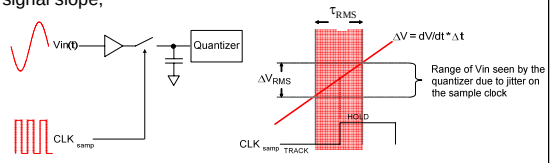
$v(t) = V_o \sin 2\pi ft$

Differentiating with respect to time yields the signal slope,

$$\frac{dv}{dt} = 2\pi f V_o \cos 2\pi ft$$

Taking the RMS value,

$$\frac{dv}{dt}_{rms} = \frac{2\pi f V_o}{\sqrt{2}} = \frac{\Delta V_{RMS}}{\tau_{RMS}}$$




Therefore, the RMS error voltage due to jitter is

$$\Delta V_{RMS} = \frac{2\pi f V_0 \tau_{RMS}}{\sqrt{2}}$$

Signal to noise ratio (SNR) is defined by,

$$SNR = 20\log_{10}\left[\frac{signal}{noise}\right] = 20\log_{10}\left[\frac{V_o/\sqrt{2}}{\Delta V_{rms}}\right]$$

Therefore, the SNR component due to jitter is:

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{\max}\tau_{RMS}}\right]$$

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The slide above shows the derivation of theoretical data converter SNR (Signal to Noise Ratio) due to jitter. It provides the following insight:

1. The frequency of the sample clock is not a factor.
2. The sample frequency of the data converter is not a direct factor, the input bandwidth of the data converter is (fmax).
3. The jitter value (tj) in Equation (6) represents total jitter which is the root sum squared of the sample clock jitter and the converter aperture jitter.

For many communications systems the bandwidth of the channel is fixed; however, the channel capacity needs to grow. Why?

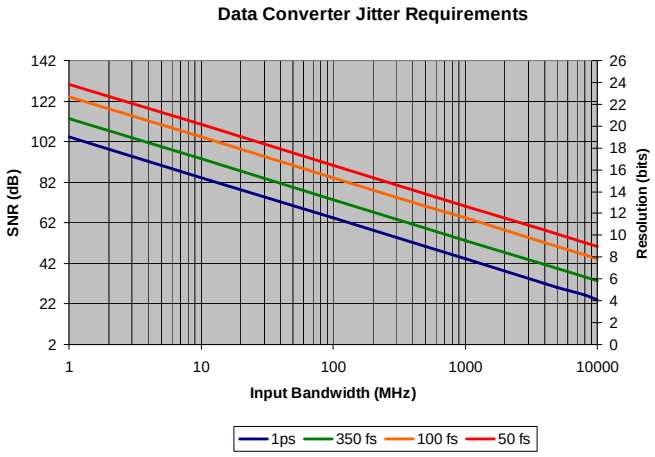
1. Multimedia content requires more capacity
2. High definition content requires more capacity
3. Growing populations and an expanding subscriber base requires more capacity.

In fixed bandwidth applications, SNR is the only lever engineers have to control channel capacity? What types of applications have fixed bandwidths?

# Data Converter Clocking

$$SNR_{ADC} = 6.02N + 1.76$$

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{\max}\tau_{RMS}}\right]$$

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- This figure plots SNR vs. input frequency for fixed values of jitter.
- We can note a couple of things about this graph
  - Lower jitter = better SNR
  - For a constant jitter, SNR decreases as the frequency of the sampled signal increases

# Caveat emptor

Sampling jitter | Quantization Error | Input Noise

$$SNR = -20\log\left(\sqrt{\left(2\pi f_{in} t_{rms}\right)^2 + \frac{2}{3}\left(\frac{1+DNL}{2^N}\right)^2 + \left(\frac{2\sqrt{2}V_{noiserms}}{2^N}\right)^2}\right)$$

$$SNR_{ADC} = 6.02N + 1.76$$

(Full Scale Sine Wave with no clock jitter, DNL, or input referred noise)

## Example of SNR Importance

$$C = B \cdot \log_2(1 + SNR)$$

Where C is the Channel Capacity
and B is the Channel Bandwidth

Shannon's Channel Capacity Theorem provides
Theoretical limit of Spectral Efficiency for a given SNR

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Shannon's Equation

# Summary

- Systems care about Signal to Noise Ratio for many reasons (e.g. Shannon's Equation).
- Signal to Noise Ratio is a parameter that can be optimized by:
  - Architectural Choices
  - Signal Chain Design
  - Component Choices
  - Careful Clock Design
- Clock Jitter and Skew are factors that directly influence ADC and hence overall signal chain performance.

# Why Consider Phase Noise?

- **Phase Noise and Jitter are directly related and we will need to understand this relationship, because:**
  - **Clock jitter directly impacts data converter performance, therefore in order to understand data converter clocking, we must first understand clock jitter and how to control it.**
  - **From an Instrumentation standpoint, usually easier to measure in freq domain**

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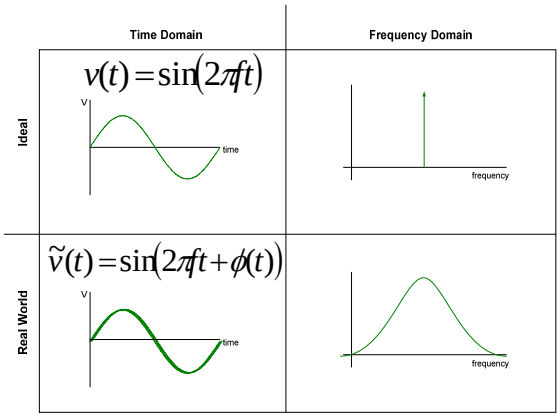
# Phase Noise

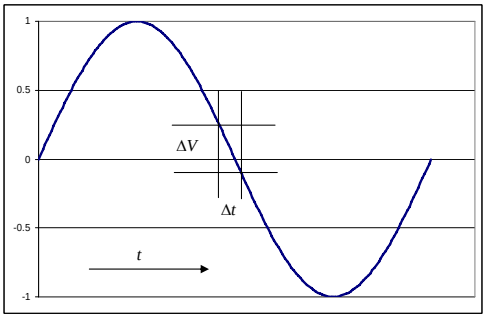


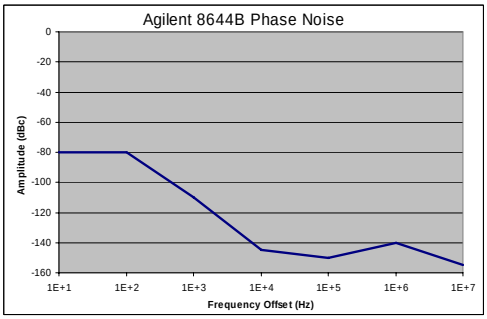

**Phase Noise Definition**:

Rapid, short-term, random fluctuations in the phase of a waveform, caused by time domain instabilities.

# Jitter ⟷ Phase Noise

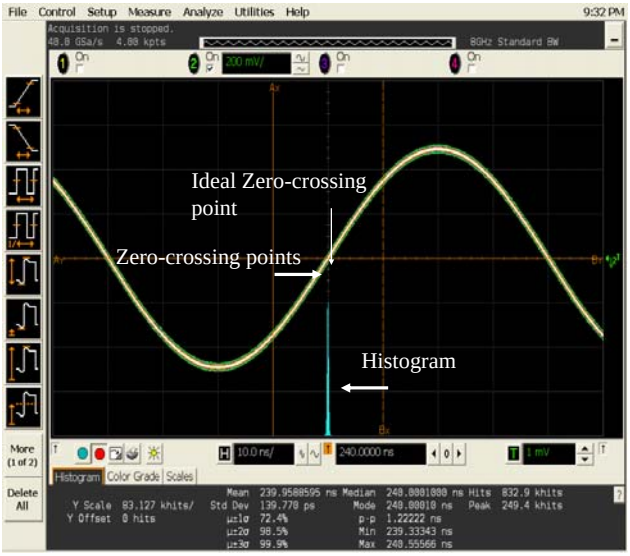
$$t_{j,RMS}\Big|_{f_1 - f_2} = \frac{1}{2\pi F_C}\sqrt{2\int_{f_1}^{f_2} 10^{\frac{PH(f)}{10}}\,df}$$



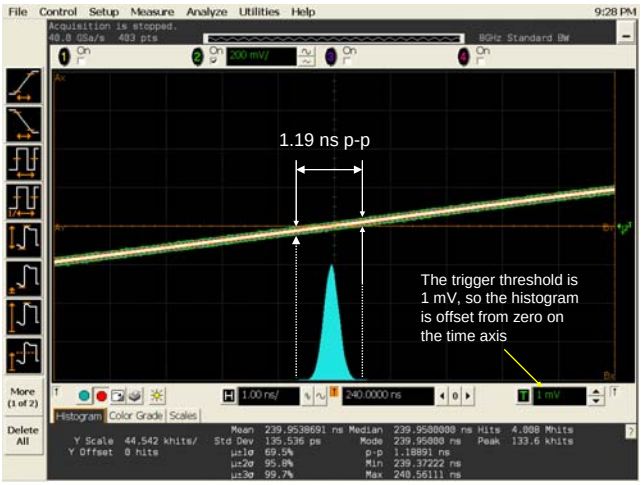

- **Jitter is the term used in the time domain with units of rms time (such as 1ps rms)**
- **Phase Noise is the term used in the frequency domain. It has units of dBc/Hz and is measured over a bandwidth**

# Phase Noise in the time domain



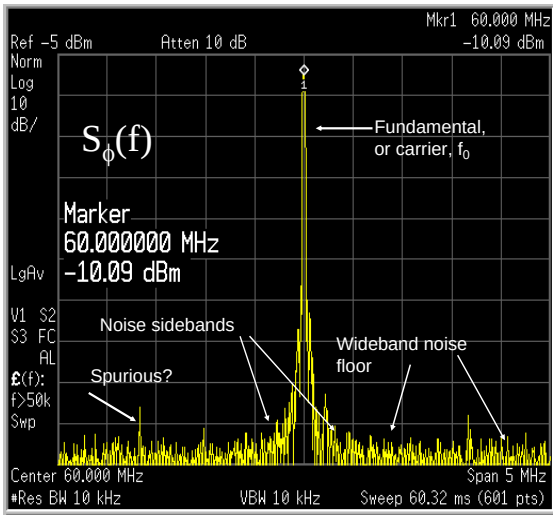

A digital scope is useful for viewing jitter in the time domain but is not adequate for measuring jitter due to limited time resolution

# Phase noise in the time domain



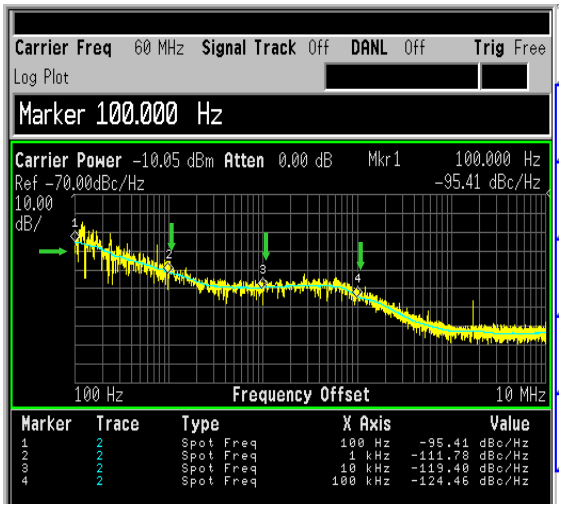

Expanding the time scale shows the Gaussian-like distribution of the jitter around the zero-crossing point

# Phase Noise in the Frequency Domain



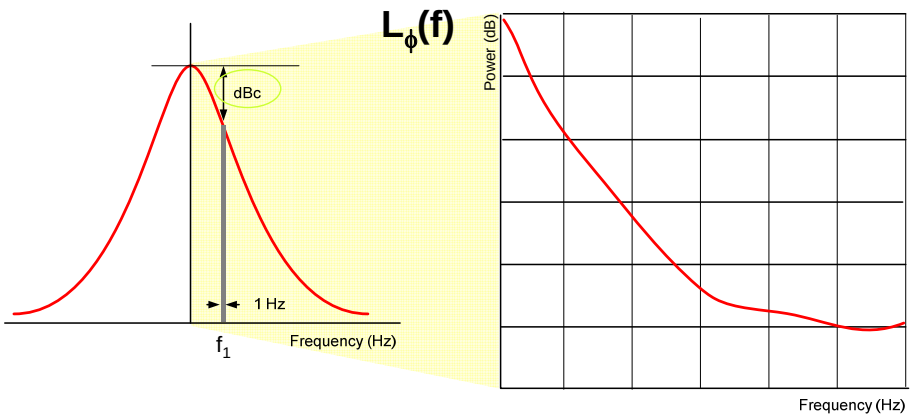

In the frequency domain, the noisy clock is not an ideal impulse. It appears as a spike with noise side bands that cause the base to spread.

# Phase Noise: Frequency Domain




Specialized spectrum analyzers allows us to view and measure the phase noise PSD.

## Phase Noise Power Spectral Density (PSD)




Phase noise power is measured in a 1 Hz bandwidth at offsets from the carrier that cover a specified range of frequencies

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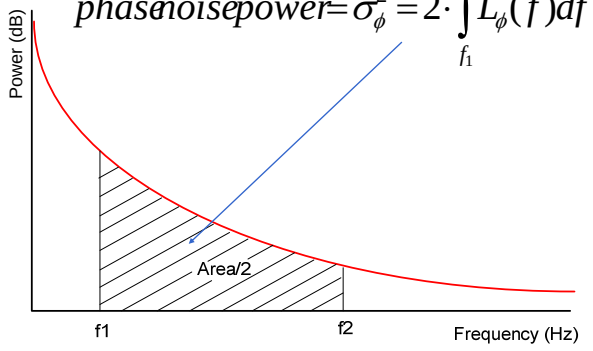
- Conventionally, the power spectral density (PSD) of the phase noise spectrum is specified in units of dBc/Hz.
- At a particular offset frequency ($f_1$), the spectrum analyzer measures the power in a 1 Hz bandwidth. Call this power $P_{f1}$ Watts.
- To convert this to dBc, we take 10 times the log of the ratio of the carrier power (in Watts) to the phase noise power (in Watts):
  - $P_{dBc} = 10*\log(P_{carrier}/P_{f1})$
- By normalizing the phase noise power in this way, we can compare different oscillators without being concerned about the absolute power level of the oscillator.

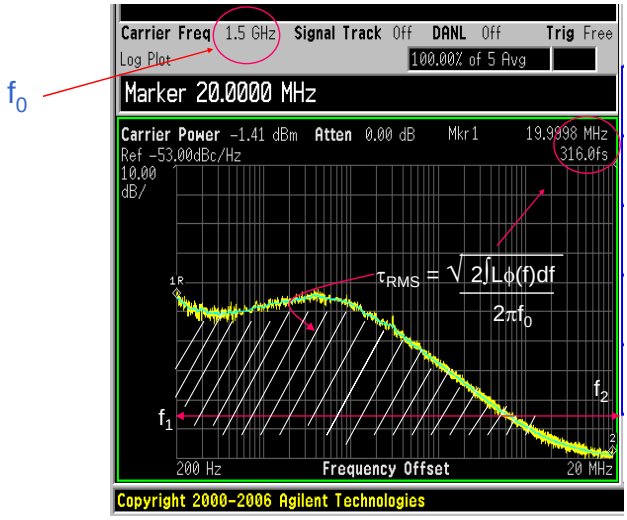
# Integrated Phase Noise Power

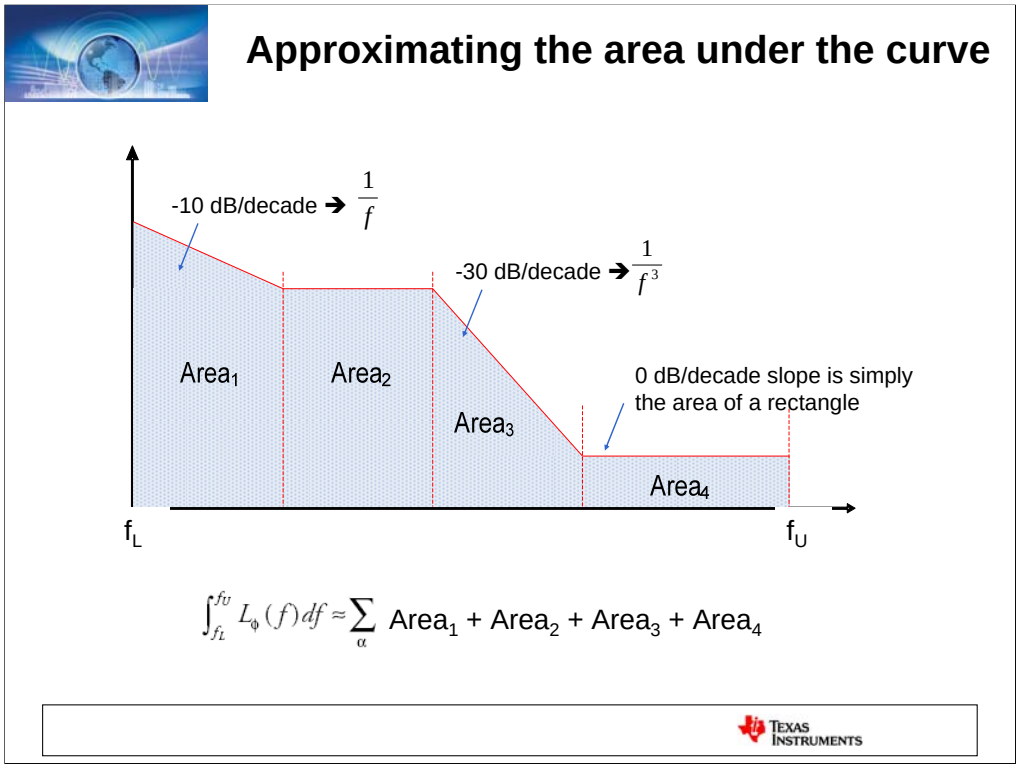
$$power = \int_{-\infty}^{+\infty} S_{PSD}(f)df$$

$$phase\,noise\,power = \sigma_\phi^2 = 2 \cdot \int_{f_1}^{f_2} L_\phi(f)df$$



# Converting Phase Noise to RMS Jitter






•This slide illustrates the area approximation method.

•Each slope of the log domain phase noise plot is converted to a straight-line approximation

•These straight line approximations will have the mathematical form: $-\alpha$ log(f). For a slope of -10 dB/decade, $\alpha = 1$. Likewise, $\alpha = 2$ for a -20 dB/decade slope.

•In the linear domain, this is equivalent to a curve having the form $1/f^{\alpha}$ or $f^{-\alpha}$

•The noise sources found in PLLs and VCOs are often characterized in this way, using 1/f, $1/f^2$, $1/f^3$, etc. A well-known paper by Leeson describes this approach to modeling noise.

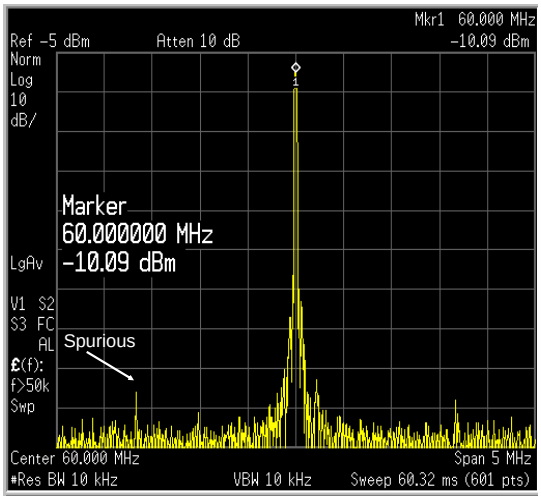
•Therefore, each sub-region under the curve is characterized by an equation of the form: $a_n*(1/f^{\alpha})$

•$a_n$ is an appropriate gain term.

•The integral solutions for $1/f^{\alpha}$ are well known, so it is straightforward to integrate the area for each region, and then find the total area by summing the regions.

•This becomes the approximation for the total single sideband phase noise.

# Spurious Response



## Spurious Response Causes

- **Intrinsic**
  - **Fractional PLLs**
  - **Dividers**
  - **Crosstalk within device (e.g. multi-PLL)**
  - **Reference Spurs**
- **Extrinsic**
  - **Reference Spurs (spurious content on reference oscillator)**
  - **Crosstalk with other devices**
  - **Crosstalk with other systems**
  - **Conducted and Radiated Susceptibility (EMI)**
    - **For example, wireless broadcast**

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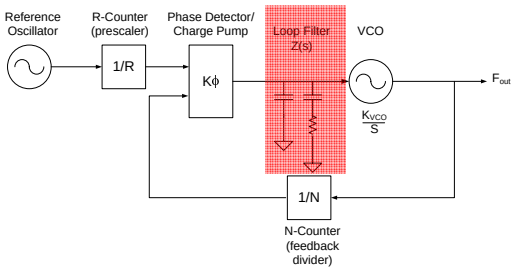
# Phase Noise Summary

- Phase noise is the instantaneous, random deviation in the ideal phase of a clock signal.
- Phase noise is observed in the frequency domain using a spectrum analyzer to plot the power spectral density of the phase noise.
- Total power of the phase noise in a specific frequency band is found by summing the area under the phase noise density curve for that band.
- RMS jitter is derived from RMS phase noise by normalizing the phase noise to the carrier frequency.
  - RMS jitter represents the area under the PSD curve
  - Integration limits must be included when specifying RMS jitter

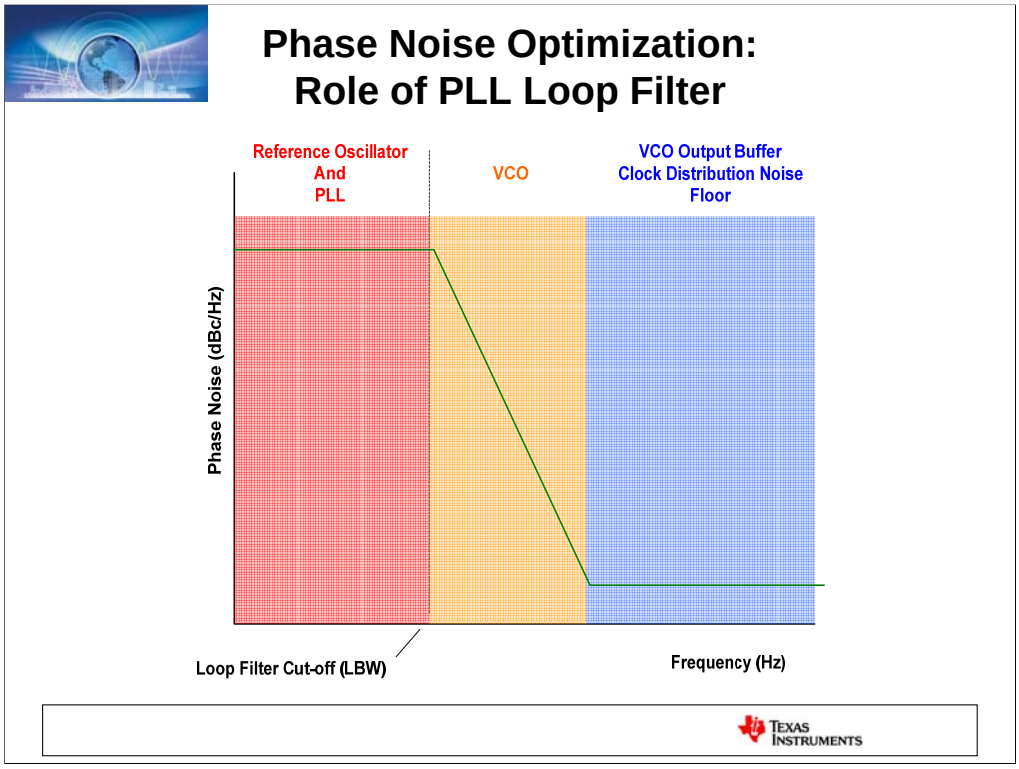
## Phase Noise Optimization - Introduction

- We have learned that Phase Noise is related to Jitter.
- We have learned that Clock Jitter degrades the Signal to Noise Ratio (SNR) performance of a data converter.
- Now we will study how to optimize (minimize) clock phase noise and hence clock jitter.

# Phase Noise Optimization: Role of PLL Loop Filter




- **Sometimes integrated into PLL or synthesizer.**
- **Is used to optimize trade-offs between critical parameters such as *phase noise* and *lock time*.**
- **Usually implemented with passive components due to the need to optimize noise.**
- **Is generally one of the most complex steps of system design incorporating a PLL.**



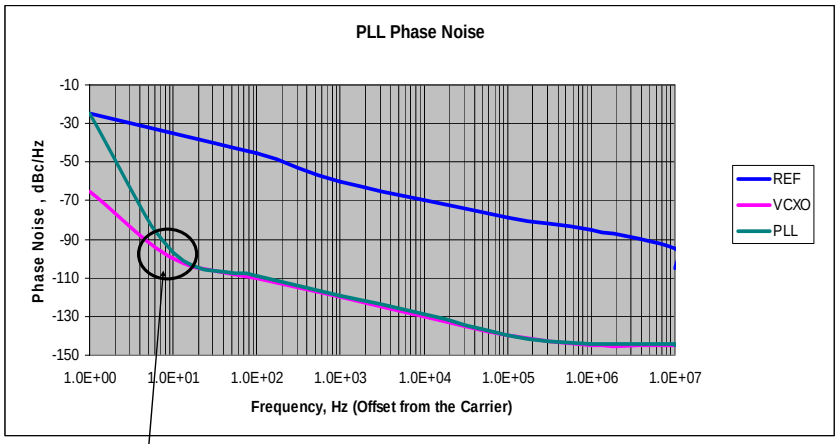

•The diagram above shows three primary regions in the frequency domain, in terms of offset from the carrier frequency of the clock.

•In each region, certain functions or components in the PLL will be the major noise sources

Close into the carrier, the noise of the reference oscillator dominates. Moving slightly away from the carrier, the noise of the PLL takes over. The point at which the VCO becomes a factor is determined by the bandwidth of the loop filter.

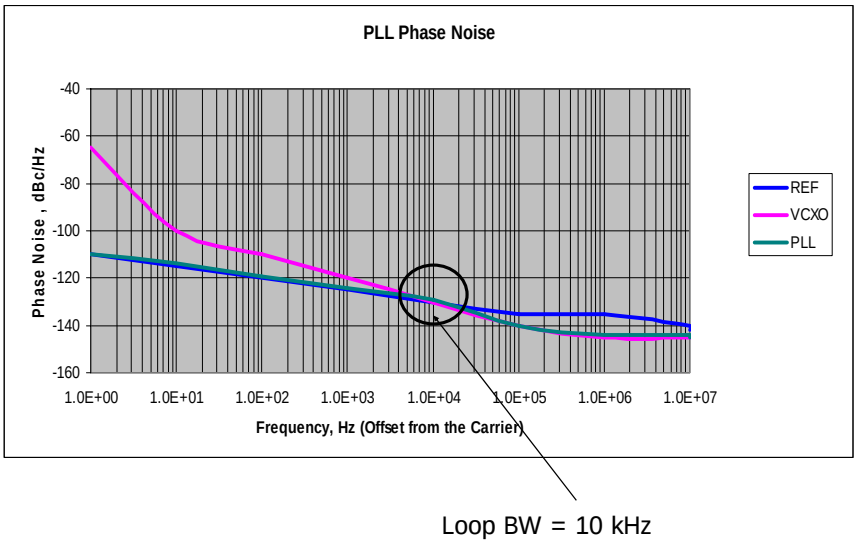
For the most part, the primary lever that a designer has to control the shape of the phase noise profile is the loop filter of the phase locked loop.

# Recommended PLL Loop BW: Noisy Ref Clock



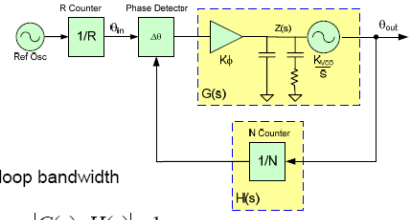

PLL Loop Bandwidth = 10 Hz

# Recommended PLL Loop BW: Clean Ref Clock




Loop BW = 10 kHz

# PLL Loop Bandwidth Dependencies




- Equality is at loop bandwidth

$$|G(s)\cdot H(s)| = 1$$

$$= \left| K_{VCO}\cdot K_\phi \cdot \frac{Z(s)}{s}\cdot\frac{1}{N}\right| = \frac{K_{VCO}\cdot K_\phi}{N}\left|\frac{Z(s)}{s}\right| = 1$$

$$\therefore$$

$$\left|\frac{Z(s)}{s}\right| = \frac{N}{K_{VCO}\cdot K_\phi}, \quad \Rightarrow \omega_C \propto K_{VCO}, K_\phi, \frac{1}{N}$$

- Loop bandwidth is determined by Z(s) AND $K_{VCO}$, $K_\phi$, and N.
- Changing N or $K_\phi$ changes the loop bandwidth!!

# Selecting Loop BW

| Condition | Loop Bandwidth | Why? |
|---|---|---|
| **Noisy reference input.**<br>**Good VCO.** | **A narrow loop bandwidth would be used to minimize the contribution of the reference input.** | **A narrow bandwidth allows the VCO performance to dominate. This why a high quality VCO is normally used.** |
| **Good reference.**<br>**Noisy VCO** | **A wide loop bandwidth would be used to allow the reference to dominate inside the loop bandwidth** | **This will minimize the overall noise profile and total noise power because the VCO noise is suppressed inside the loop.** |

# CDCM7005

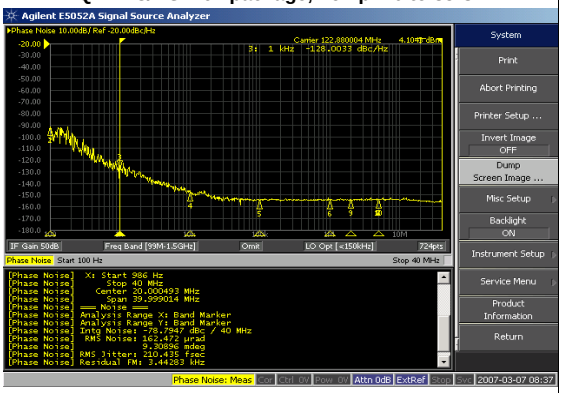
## 2:5 External VCXO Ultra Low Jitter Frequency Synthesizer

### Features

- Input frequencies up to 200MHz SE
- Output frequencies up to 1.5GHz
- Output provides up to 5 LVPECL/10 LVCMOS
- Low Output Skew (~ 20ps, typ)
- Ultra low additive jitter (~50fs, RMS)
- Provides holdover functionality
- Loop Bandwidth Calculator Software

### Benefits

- Wide input/output frequency range supports high and low end of frequency standards
- Selectable input/output standards reduces translation logic
- External loop filter provides maximum flexibility
- SPI interface provides in-system programming
- QFN-48/BGA-64 package, Temp -40 to 85 C




### Applications

- Wireless BTS (Macro, Micro Cells)
- SONET
- Data Communications
- Test Equipment
- Jitter Cleaners

1Ku / $10.75

CDCM7005QFN-EVM

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# CDCE72010

## 2:10 External VCXO Ultra Low Jitter Frequency Synthesizer

### Features

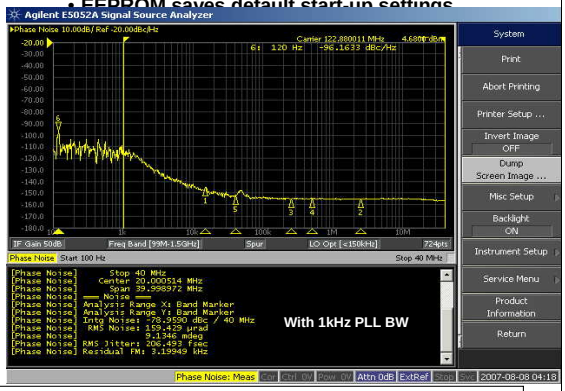
- Input frequencies up to 180MHz SE/500MHz Differential LVDS/LVPECL/LVCMOS
- Output frequencies up to 1.25GHz
- Output up to 10 LVPECL/10 LVDS/20 LVCMOS
- Optional High Swing LVPECL output
- Wide-range integer divide selectable by output
- Individual Phase Adjust
- Ultra low additive jitter (~50fs, RMS)
- Low Output Skew (~ 20ps, typ)
- Provides holdover functionality
- On-chip EEPROM

### Benefits

- Wide input/output frequency range supports high and low end of frequency standards
- Selectable input/output standards reduces translation logic
- External loop filter provides maximum flexibility
- EEPROM saves default start-up settings

### Applications

- Wireless BTS (Macro, Micro Cells)
- SONET
- Data Communications
- Test Equipment
- Jitter Cleaners




Jun/08 In Production

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# CDCE62005

## 3:5 Integrated VCO Low Jitter Frequency Synthesizer

### Features

- Input frequencies from 80kHz to 500MHz
- Crystal Inputs from 2MHz to 42MHz
- Output frequencies from 4.25MHz to 1.175GHz
- Output up to 5 LVPECL/5 LVDS/10 LVCMOS
- Individual phase adjust
- Optional high swing LVPECL mode
- Wide-range integer divide selectable by output
- Low output skew (~ 20ps, typ)
- Integrated/External PLL Loop Filter
- Low jitter (< 1ps RMS)
- On-chip EEPROM

### Benefits

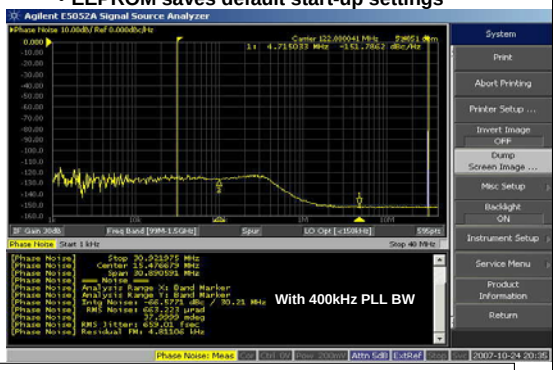
- Fully Integrated twin VCOs support wide output frequency range
- Wide input/output frequency range supports high and low end of frequency standards
- Selectable input/output standards reduces translation logic
- Integrated/external loop filter provides flexibility
- EEPROM saves default start-up settings

### Applications

- Wireless BTS
  (Pico cell, WiMax, Macro Base band)
- Data Communications
- Medical
- Test Equipment
- Jitter Cleaners

Sampling now

Sep/08 In Production

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# PLL Summary

- PLL parameters such as R, N, $K_\phi$, $K_{VCO}$ and the loop filter bandwidth will influence the overall noise performance at the output.
- Each function in a PLL/VCO clock circuit contributes to the overall noise at the output of the VCO
- The loop transfer function for each noise source determines the frequency region of the phase noise in which the respective noise source will dominate in final output.

# Clocking High Speed Data Converters

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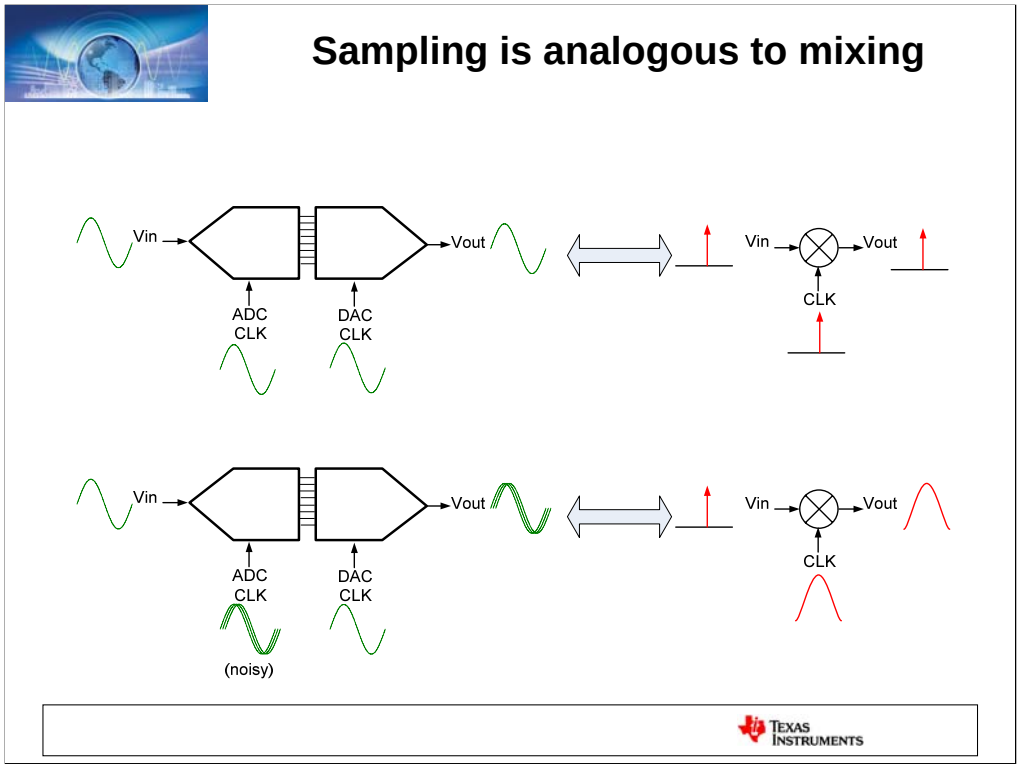
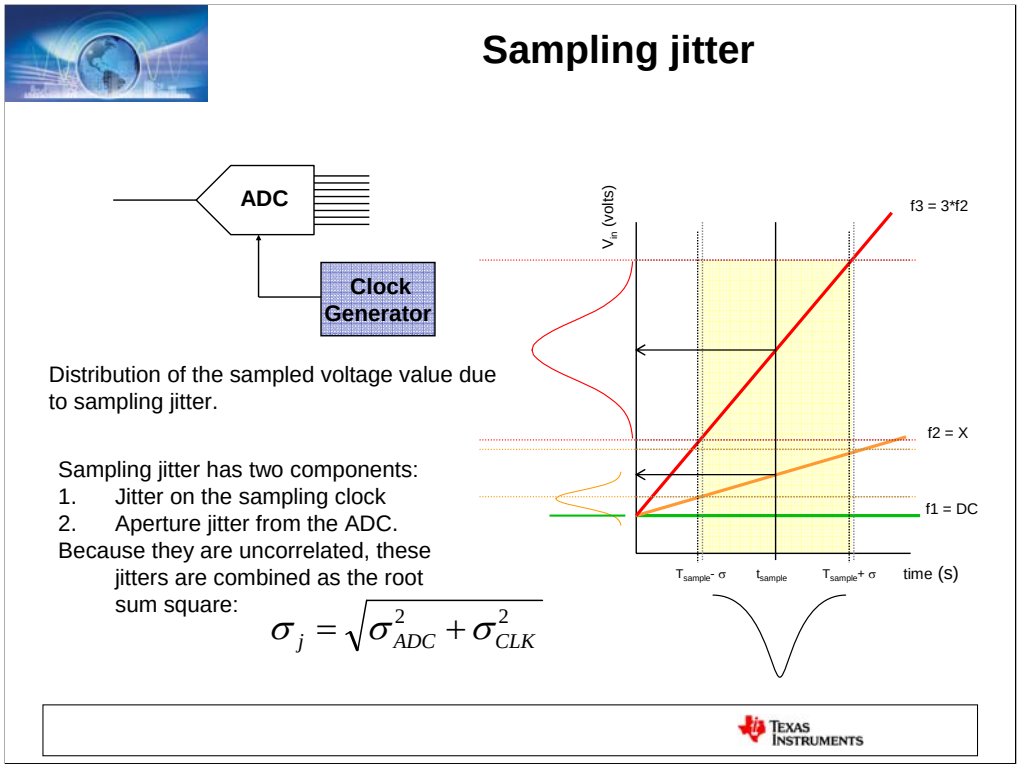



Data converter clocking in the time domain is analogous to mixing in the frequency domain.

Let's take a closer look at what happens at the exact time that an input waveform is sampled.




The plot shown above will be used to understand how the voltage error (noise) due to clock jitter is related to the frequency of the input signal

The green, orange, and red lines represent portions of input signals with varying input frequencies.

The green waveform is DC (0Hz), the orange waveform in at frequency f, and the red is at frequency 3f.

The black vertical line represents an ideal sampling point and the yellow shaded region represents a normal distribution of where the sampling point actually occurs due to noise on the sampling clock. Notice how the higher the input frequency (and hence the input slope), the wider the distribution of voltages will be read by the converter.

# ADS5525

## 12-bit, 170MSPS ADC with CMOS & DDR LVDS Outputs

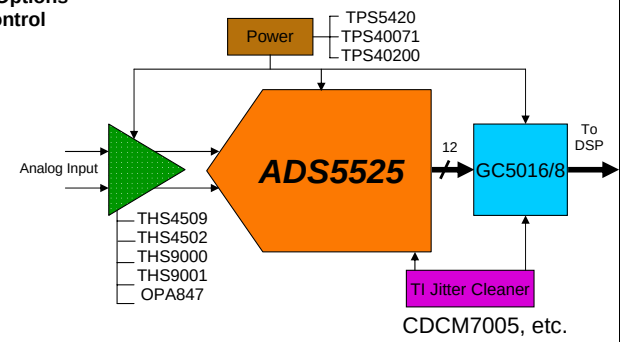
### Features

- Maximum Sample Rate: 170 MSPS
- 12-Bit Resolution; No Missing Codes
- Power Dissipation: Core 1 W, Total 1.13 W
- 11 ENOB Guaranteed at 70-MHz IF
- Programmable power scaling
- 70.5-dBFS SNR at 70-MHz IF
- 84-dBc SFDR at 70-MHz IF
- Internal Sample and Hold
- Parallel CMOS and DDR LVDS Output Options
- Selectable Output Timing and Level Control
- Internal or External Reference
- 3.3-V Analog and Digital Supply
- 48-Pin QFN Package (7 mm x 7 mm)

### Applications

### Benefits

- Highest SNR and SFDR available 12-bit 170 MSPS sample rate
- Space saving QFN package – smallest package available
- Increased performance benefits a variety of test and measurement, communications and imaging applications.




EVM

**ADS5525EVM**
**Samples and EVMs available**

Texas Instruments

# ADS5525 Clocking

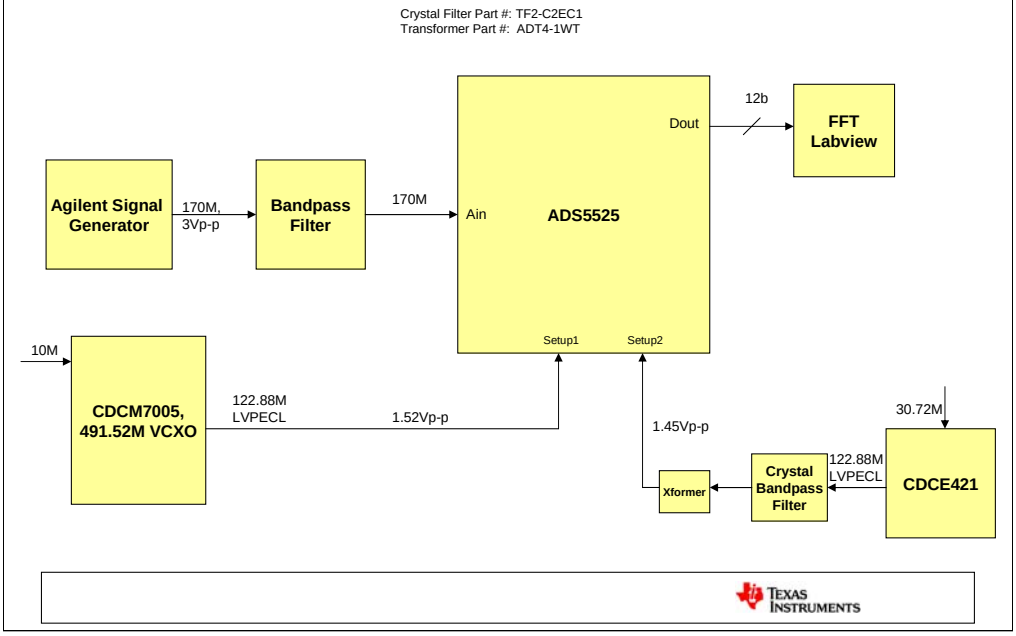
Calculate Required Clock Jitter to achieve desired SNR

| | | | |
|---|---|---|---|
| **Input Frequency** | **170.00** | **MHz** | **desired input frequency to ADC analog inputs** |
| **Aperture Jitter** | **150.00** | **fs rms** | **aperture jitter comes from ADC datasheet** |
| Ext Clock Jitter | 267.25 | fs rms | **rms jitter of clock source at ADC clock inputs** |
| **Total Jitter** | **306.47** | **fs rms** | **rms jitter of clock and ADC jitter combined** |
| **SNR** | **69.70** | **dBc** | **Signal-to-Noise Ratio of ADC** |

Datasheet performance

http://www.ti.com/litv/zip/slac133

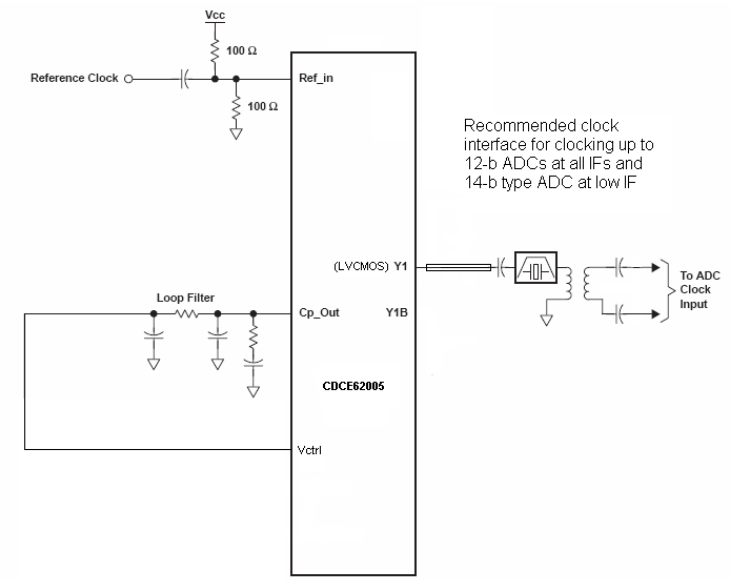
# Test Setup


Crystal Filter Part #: TF2-C2EC1
Transformer Part #: ADT4-1WT
Agilent Signal Generator
170M, 3Vp-p
Bandpass Filter
170M
Ain
ADS5525
Dout
12b
FFT Labview
Setup1
Setup2
10M
CDCM7005, 491.52M VCXO
122.88M LVPECL
1.52Vp-p
1.45Vp-p
Xformer
Crystal Bandpass Filter
122.88M LVPECL
30.72M
CDCE421
Texas Instruments

# ADS5525 Performance

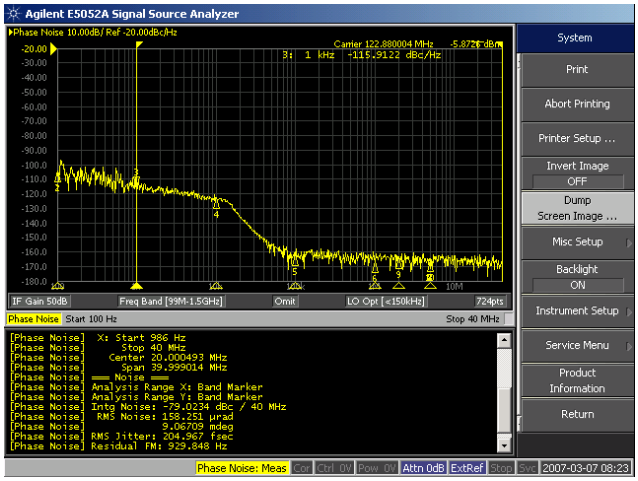
| Device | IF (MHz) | Clock (MHz) | SNR (dB) | SFDR (dB) | D/S SNR (dB) | D/S SFDR (dB) |
|---|---|---|---|---|---|---|
| **CDCE421 + BPF (CDCE62005 + BPF)** | **170** | **122.88** | **69.63** | **78.59** | **69.7** | **79** |
| **CDCM7005/LVPECL** | **170** | **122.88** | **69.66** | **78.42** | **69.7** | **79** |

# Clock Interface to ADC

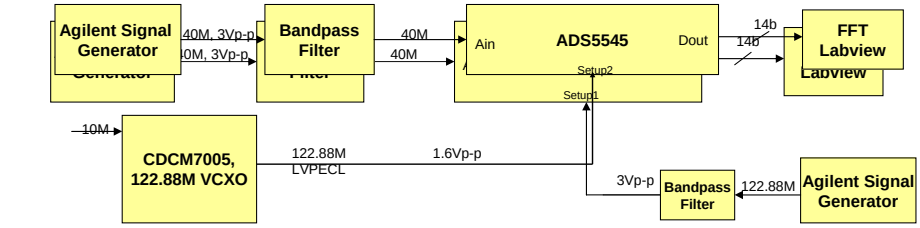


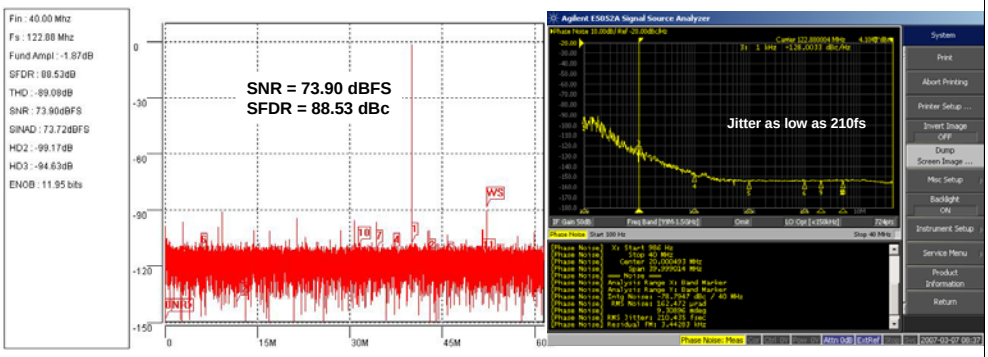
# Clock Interface to ADC

CDCE72010/CDCM7005/LVDS2505 BPF)

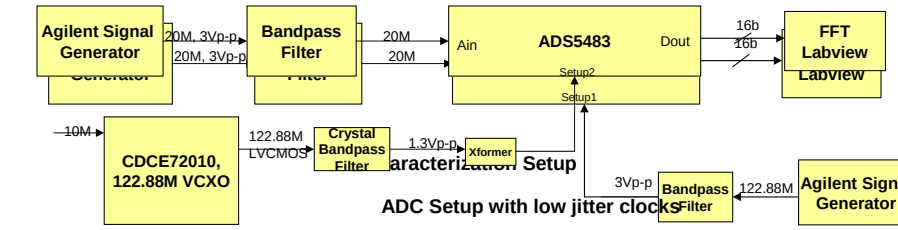


# Example: Partial Signal Chain Solution

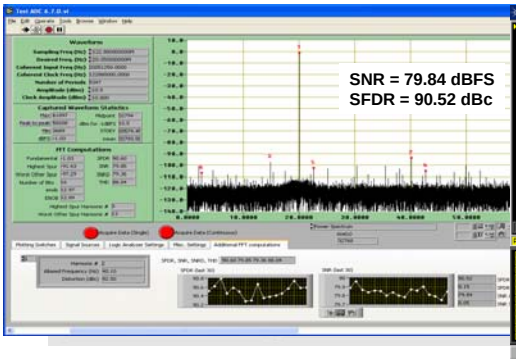


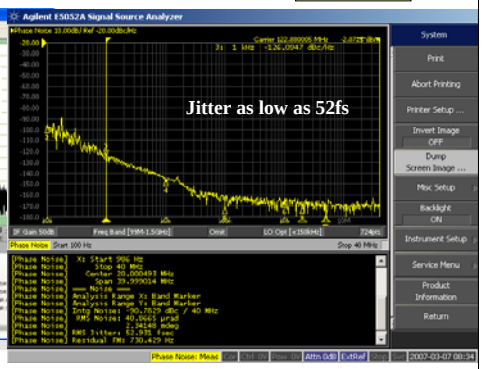



# Example: Partial Signal Chain Solution




ADC Setup with low jitter clocks

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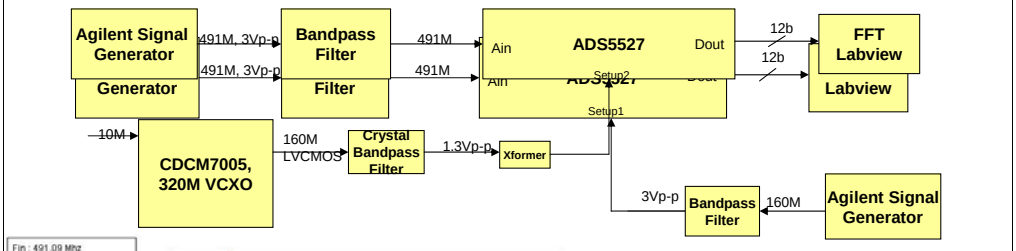
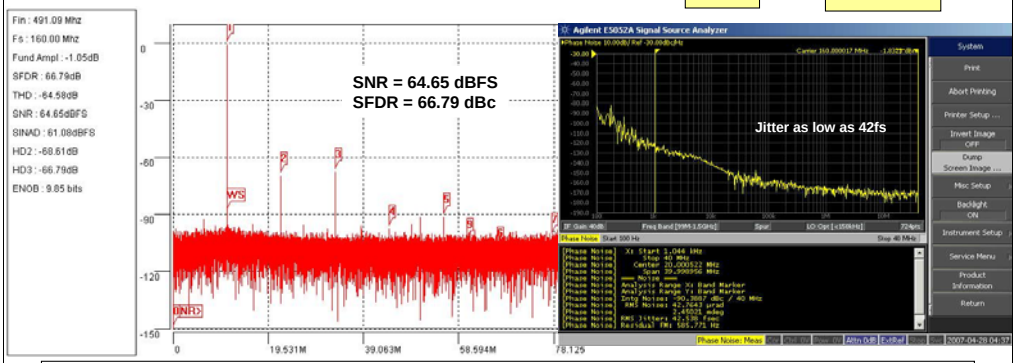
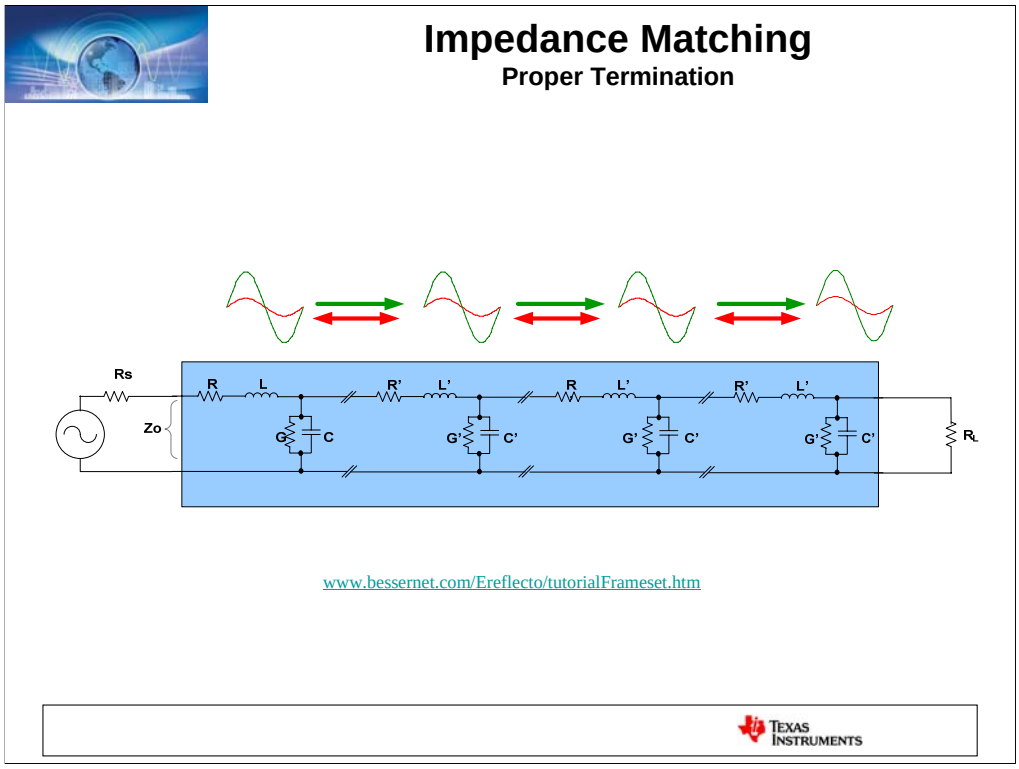
# Example: Partial Signal Chain Solution



# Signal Integrity Issues




It is important to understand the faster a signal must switch from one state to another defines whether the signal path is a transmission line or not. For example, a 100 Kbps Non-Return to Zero (NRZ) coded signal has a 10 micro-second bit period. Allowing 20% of that bit period for transitioning from one state the next (the transition time) means the transition time could be as long as 2 micro-seconds without interfering with the reliability of the data. Considering that electromagnetic waves travel through copper wires at about 180 pico seconds per inch, this transition wave could travel over 900 feet before completing the transition from one state to another. This is a very slow transition time that would tolerate a very long transmission line before having to use the analog transmission line techniques to engineer the reliability of the data transfer. On the other hand, if the signal is 1 Gbps NRZ, then the bit period is only 1 ns and transmission times are on the order of 200 ps. This wave travels a little over 2.5cm before completing the transition. This means transmission line terminations are a critical design feature for all 1 Gbps interconnects.

The lesson is that the faster the signal then the shorter the interconnect before it needs to be treated like a transmission line. Note that Mbps and MHz are not equal when referring to data transmission. For example, a 100 MHz clock signal has a high and low state for each period. A 100 Mbps data rate using NRZ (non return to zero) coding where the data is changing every state would actually be switching at a frequency of 50 MHz because each bit is only half of the period.

Les Besser provides an applet on-line which can be used to observe the impact of improper termination with respect to the incident and reflecting wave which travels along the media (transmission line).

## Impedance Matching
### Proper Termination

- **Layout**
  - **Stubs**
  - **Vias**
- **Transition**
  - **Connectors**
  - **Cables**
  - **Discontinuities**
- **Termination**
  - **Receiver Characteristics**
  - **Where to terminate**

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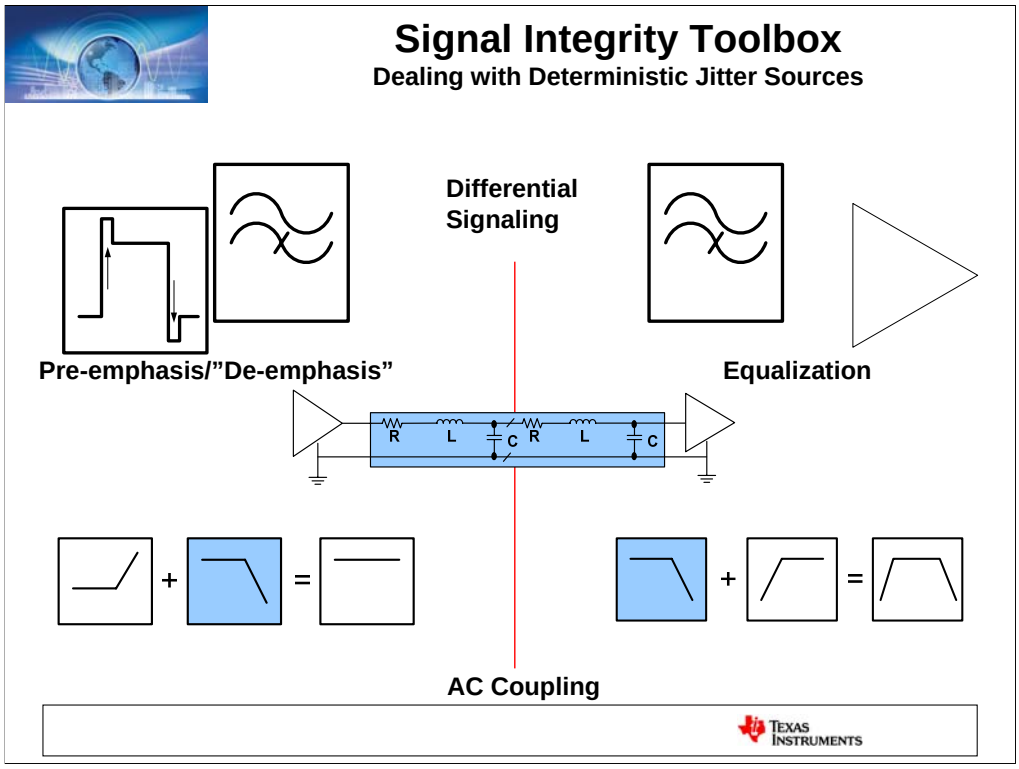


The benefits of differential signaling and AC coupling have been discussed. There are additional tools in the signal integrity engineer's arsenal to deal with signal transmission challenges.

The goal is to flatten out the overall frequency response of the channel which is, as we have already discussed, low pass. Even if the channel is properly terminated, longer channel lengths and/or higher signal frequencies introduce attenuation and hence a degradation of signal to noise ratio.

Transmitter Side Solutions (pre-emphasis, de-emphasis)

Transmitters with signal conditioning provide output compensation for transmission loss. The goal is to flatten the overall response of the channel. Pre-emphasis boosts the signal level of the high frequency components of the input signal to counter the low pass response of the channel. De-emphasis reduces the low frequency component of the signal having the same net impact as pre-emphasis. Important features to think about when considering a transmitter with signal conditioning is if the transmitter offers programmable or fixed levels of output voltage and/or output rise times. Programmable solutions offer the greatest degree of flexibility.

Receiver Side Solutions (Equalization)

In much the same way that an audio equalizer allows the listener to tailor the frequency content of audio equipment, the equalizer allows for input compensation to adjust for the loss of higher frequency components. They do so by generating boost for the higher frequency components thus opening up the eye.

# Summary

- Jitter is a critical factory in determining system performance
- Phase noise measurements provide a powerful tool for jitter characterization
- PLL loop filter can be designed to clean jitter
- A combination of PLL+BPF may be required depending on system reqts
- Signal Integrity also very important

## Questions?

THANK YOU!

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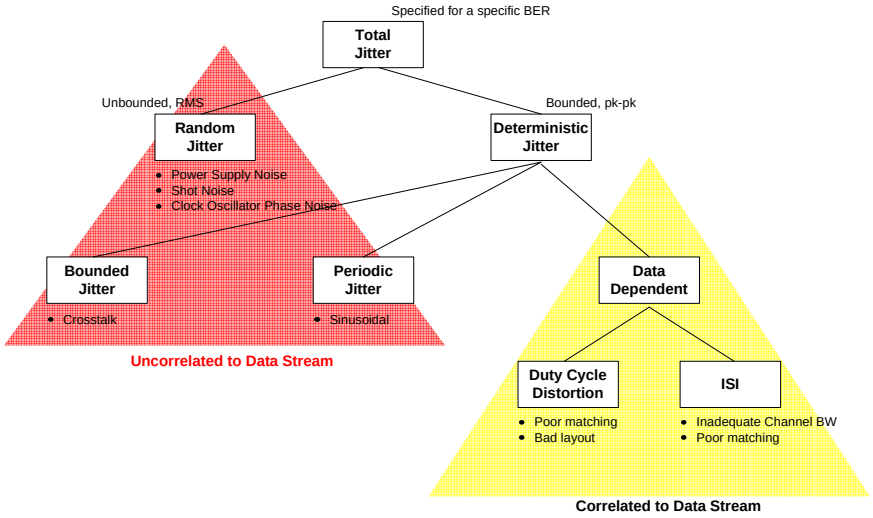
## Some Additional Slides

# Jitter Tree


Specified for a specific BER
Total Jitter
Unbounded, RMS
Bounded, pk-pk
Random Jitter
Deterministic Jitter
Power Supply Noise
Shot Noise
Clock Oscillator Phase Noise
Bounded Jitter
Crosstalk
Periodic Jitter
Sinusoidal
Uncorrelated to Data Stream
Data Dependent
Duty Cycle Distortion
Poor matching
Bad layout
ISI
Inadequate Channel BW
Poor matching
Correlated to Data Stream

# PLL Summary

Desired: Signal with wide tuning range, good accuracy and stability, and acceptable phase noise.

| | Oscillator 1: Crystal Reference | Oscillator 2: VCO | PLL Output |
|---|---|---|---|
| Tuning Range (pulling) | **Narrow** | Wide | Wide |
| Accuracy | Very Good | **Poor** | Very Good |
| Phase Noise | Superb: close in<br>**Poor: far out** | **Poor: close in**<br>Very Good: far out | Good: close in<br>Very Good: far out |
| Stability and Drift | Potentially Good | **Poor** | Good |

A PLL can substitute **desirable performance characteristics** for **undesirable characteristics**.

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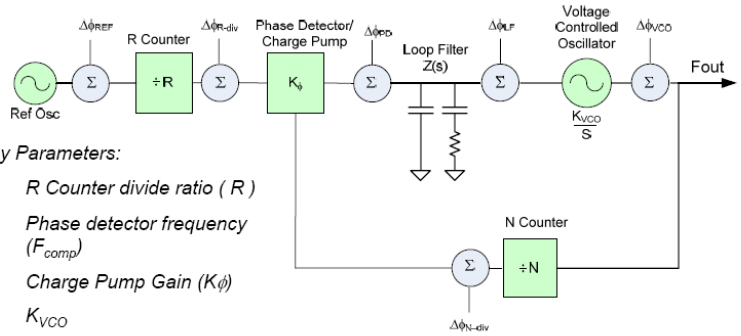
# Phase Noise Optimization




*Key Parameters:*

1. *R Counter divide ratio ( R )*
2. *Phase detector frequency ($F_{comp}$)*
3. *Charge Pump Gain ($K\phi$)*
4. *$K_{VCO}$*
5. *N Counter divide ratio ( N )*
6. *Loop Filter Z(s)*

**Understand the influence of the noise sources ➔ tradeoffs**

*Other Considerations:*

1. *Lock Time*

# Phase Noise Optimization - Levers

| PLL Functional Block | To minimize Noise contribution… | Why? |
|---|---|---|
| **Phase Detector/Charge Pump** | **Maximize charge pump gain ($K_\phi$) (up to a certain point)** | **The phase detector noise contribution is proportional to $1/(K_\phi)^2$** |
| **R-counter and N-counter divide ratios** | **Maximize phase detector compare frequency → this minimizes N** | **The noise contribution of the R and N dividers is proportional to $N^2$.** |
| **Reference oscillator** | **Use highest frequency practical and use R > 1 if possible. If deciding between maximizing R and minimizing N, minimize N.** | **The noise contribution from the reference oscillator is proportional to $(N/R)^2$** |

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•This table provides some guidance on design choices in PLL/VCO design that can be manipulated to improve phase noise performance.

•Keep in mind that no amount of clever design or optimization can overcome the use of poor quality components

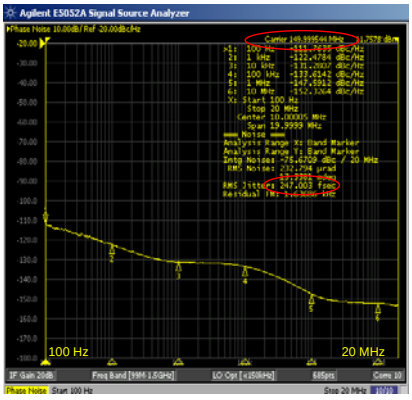
•Using the best reference clock and VCO that meet cost targets is always a given.

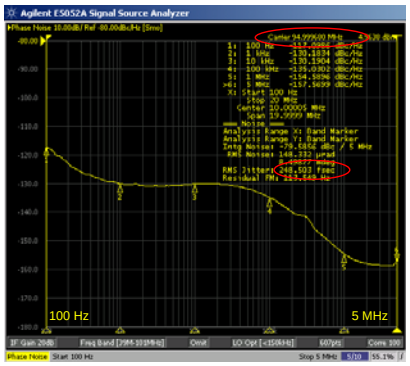
•If close-in phase noise is important for a particular application, then choose components that give the desired close-in performance and acceptable performance at higher offsets.

## Comparing Clock Performance

Can we compare these oscillators?

$$\tau_{RMS} = \frac{\sqrt{2 \cdot \int_{f_L}^{f_U} L_\phi(f) df}}{2\pi f_0}$$

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- When comparing RMS jitter or total phase noise between clocks, the ***limits of integration*** must be identical
  - Comparing two clocks that have different phase noise bandwidths is invalid
- When comparing RMS jitter between clocks, ***the carrier frequencies*** must be identical
  - Remember, jitter is proportional to the inverse of the clock frequency.
  - If two clocks have the same phase noise power but operate at different frequencies, the clock at the higher frequency will have lower jitter.
- Total (integrated) phase noise power says nothing about the distribution of the noise.
  - PSDs having different shapes may yield the same total phase noise power
- A good clock can be made to look bad if a wider region of integration is chosen relative to a lower quality oscillator

## Comparing Clock Performance

- **It is possible to re-normalize phase noise data for clocks of different frequencies in order to compare them.**

$$S_{new}(f)_{dB} = S_{old}(f)_{dB} + 20 \cdot \log_{10}\left(\frac{f_{new}}{f_{old}}\right)$$

## FFT Refresher

- Fs = Sampling Rate = 80MS/s
- Fin = Input Frequency = 70MHz
- N = Number of Points
- Fbin = FFT Bin Width

$$Fbin = Fs / N$$

| | |
|---|---|
| N = 32K and Fs = 80MS/s | Fbin = 2441Hz |
| N = 256K and Fs = 80MS/s | Fbin = 305 Hz |
| N = 512K and Fs = 80MS/s | Fbin = 153 Hz |

# FFT Refresher

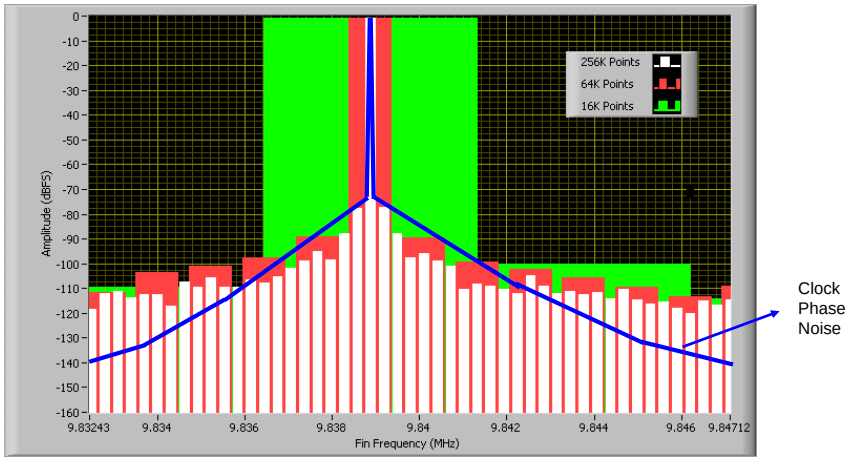
- **Fs = Sampling Rate = 80MS/s**
- **N = Number of Points**
- **SNR = ADC noise**
- **Noise_Floor = Average Noise from SNR**

$$Noise\_Floor = 10 \bullet LOG\left[\frac{10^{-SNR/10}}{N/2}\right]$$

**N = 32K and SNR = 75dBFS Noise_Floor = -117dBFS**
**N = 256K and SNR = 75dBFS Noise_Floor = -126dBFS**
**N = 512K and SNR = 75dBFS Noise_Floor = -129dBFS**

## The Problem – FFT Performance

**Real ADS5433 at 80MS/s and 70MHz (Using 8644Bs)**




TEXAS INSTRUMENTS

The graph shows an ADC's FFT plots with different number of points. As seen in the plots, the green plot is with smallest number of points, as indicated by the largest bandwidth of the analog spectrum analysis of the ADC outputs, and the white plot is with largest number of points, as indicated by the smallest bandwidth. The FFT plots are overlaid with the ADC sampling clock phase noise mixed with the analog input of the ADC.

If we consider any of the three FFT plots, due to the finite bandwidth of the analog spectrum, any clock phase noise mixing within the bandwidth is masked and thus the SNR is dictated by clock phase noise mixing beyond the bandwidth/2 in the single side band

## Clock Jitter Considerations in the lab

- **Minimum number of points (N) for DC performance is 4 x $2^M$, where M is the ADC bit resolution (to ensure no missing codes for INL, DNL of ADC)**
- **Number of points (N) for optimal AC performance (SNR) is about $2^{M-1}$ to $2^M$, where M is the ADC bit resolution**
- **Any variation in clock jitter within Fbin (Fs +/- Fbin/2) is not important**
- **For Nyquist system, wideband phase noise up to Fs/2 is important**
- **Clock phase noise in wide band aliases back into close-in phase noise**

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{\max}\tau_{RMS}}\right]$$

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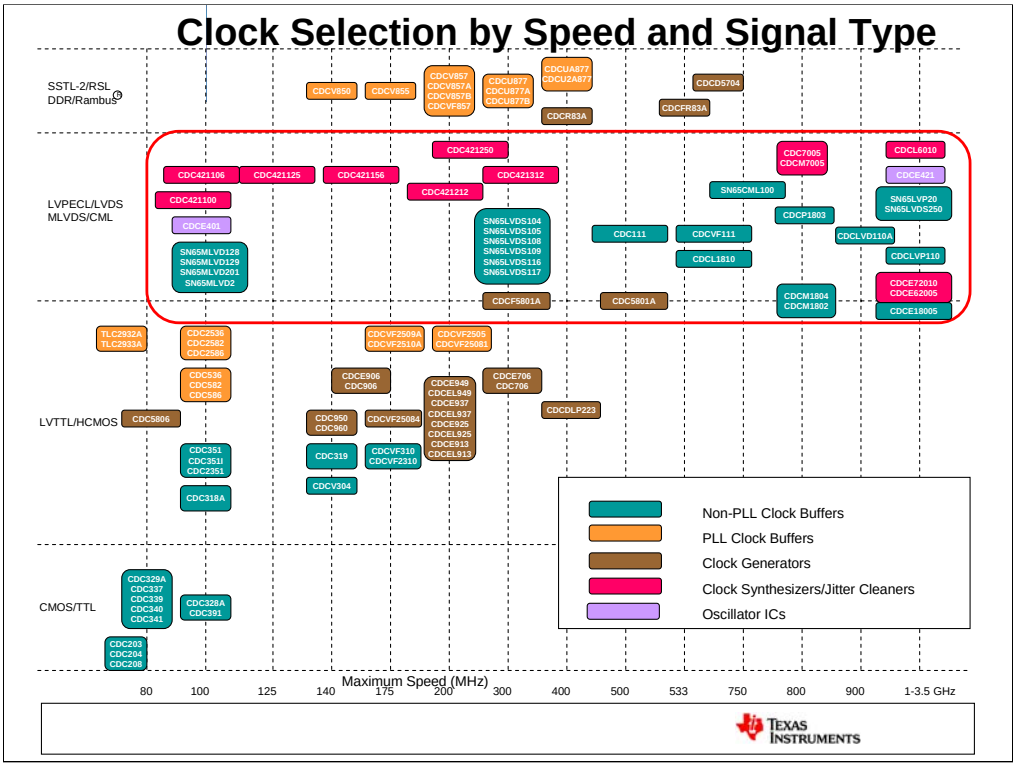
## Clock Jitter Considerations in the application

- **Close-in and far-out phase noise important for all applications**
  - **Clock phase noise in wide band aliases back into close-in phase noise**
- **Start & stop bandwidth for clock jitter dictated by any conforming industry standard or customer/application requirement**
- **For example, in wireless BTS systems**
  - **Clock integration bandwidth would depend on channel spacing and channel bandwidth**

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{\max}\tau_{RMS}}\right]$$


Clock Selection by Speed and Signal Type
SSTL-2/RSL
DDR/Rambus
LVPECL/LVDS
MLVDS/CML
LVTTL/HCMOS
CMOS/TTL
CDCV850
CDCV855
CDCV857
CDCV857A
CDCV857B
CDCVF857
CDCU877
CDCU877A
CDCU877B
CDCUA877
CDCU2A877
CDCR83A
CDCD5704
CDCFR83A
CDC421250
CDC421106
CDC421125
CDC421156
CDC421312
CDC421212
CDC421100
CDCE401
SN65MLVD128
SN65MLVD129
SN65MLVD201
SN65MLVD2
SN65LVDS104
SN65LVDS105
SN65LVDS108
SN65LVDS109
SN65LVDS116
SN65LVDS117
CDCF5801A
CDC111
CDCVF111
CDCL1810
CDC5801A
CDC7005
CDCM7005
SN65CML100
CDCP1803
CDCL6010
CDCE421
SN65LVP20
SN65LVDS250
CDCLVD110A
CDCLVP110
CDCE72010
CDCE62005
CDCE18005
CDCM1804
CDCM1802
TLC2932A
TLC2933A
CDC2536
CDC2582
CDC2586
CDCVF2509A
CDCVF2510A
CDCVF2505
CDCVF25081
CDC536
CDC582
CDC586
CDCE906
CDC906
CDCE706
CDC706
CDCE949
CDCEL949
CDCE937
CDCEL937
CDCE925
CDCEL925
CDCE913
CDCEL913
CDCDLP223
CDCS806
CDC950
CDC960
CDCVF25084
CDC351
CDC351I
CDC2351
CDC319
CDCVF310
CDCVF2310
CDC318A
CDCV304
CDC329A
CDC337
CDC339
CDC340
CDC341
CDC328A
CDC391
CDC203
CDC204
CDC208
Non-PLL Clock Buffers
PLL Clock Buffers
Clock Generators
Clock Synthesizers/Jitter Cleaners
Oscillator ICs
Maximum Speed (MHz)
80
100
125
140
175
200
300
400
500
533
750
800
900
1-3.5 GHz
Texas Instruments

# Clock Selection by Output and Signal Type