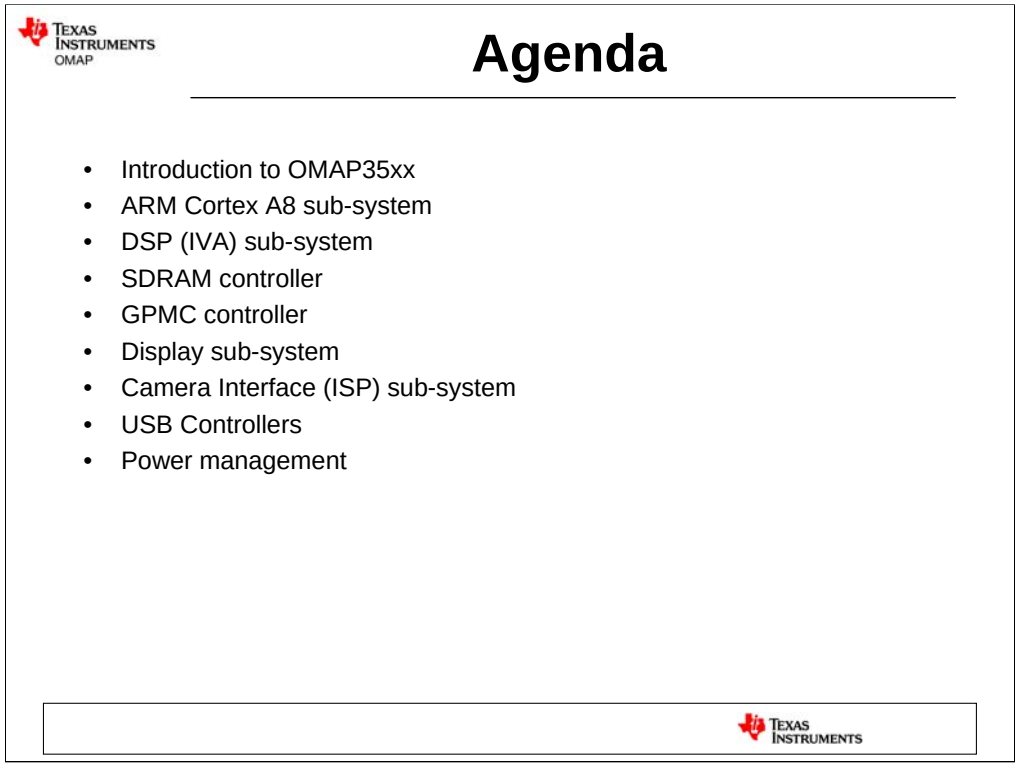
Texas Instruments
OMAP

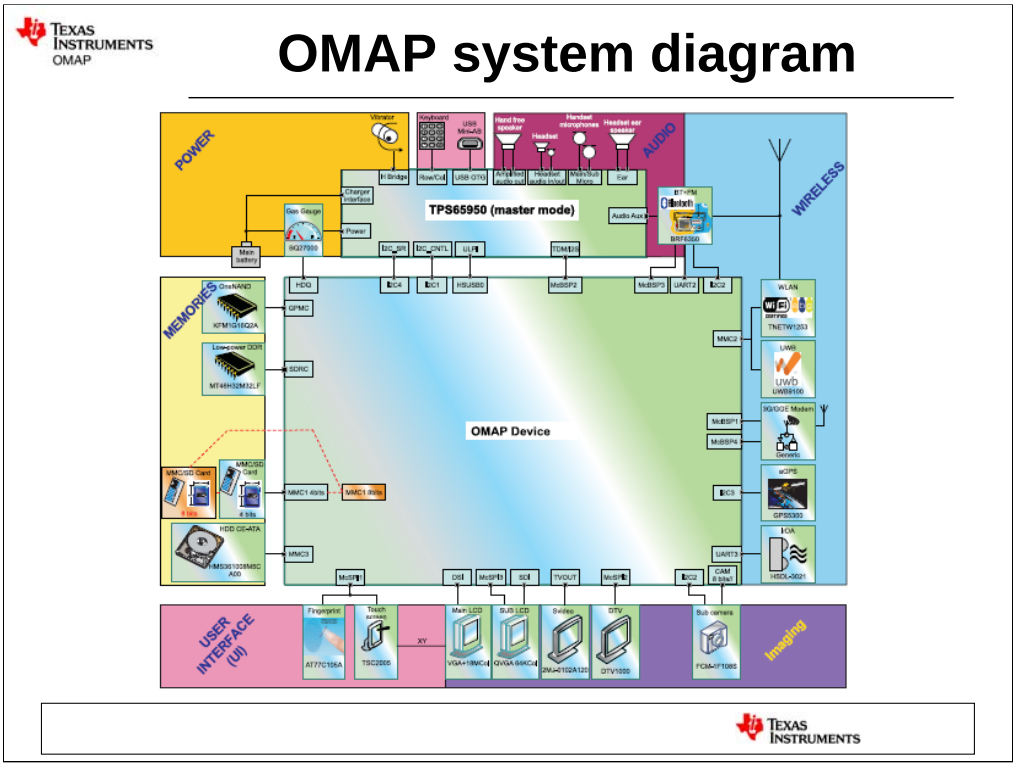
OMAP35xx Overview
2009 Tech Day

Texas Instruments



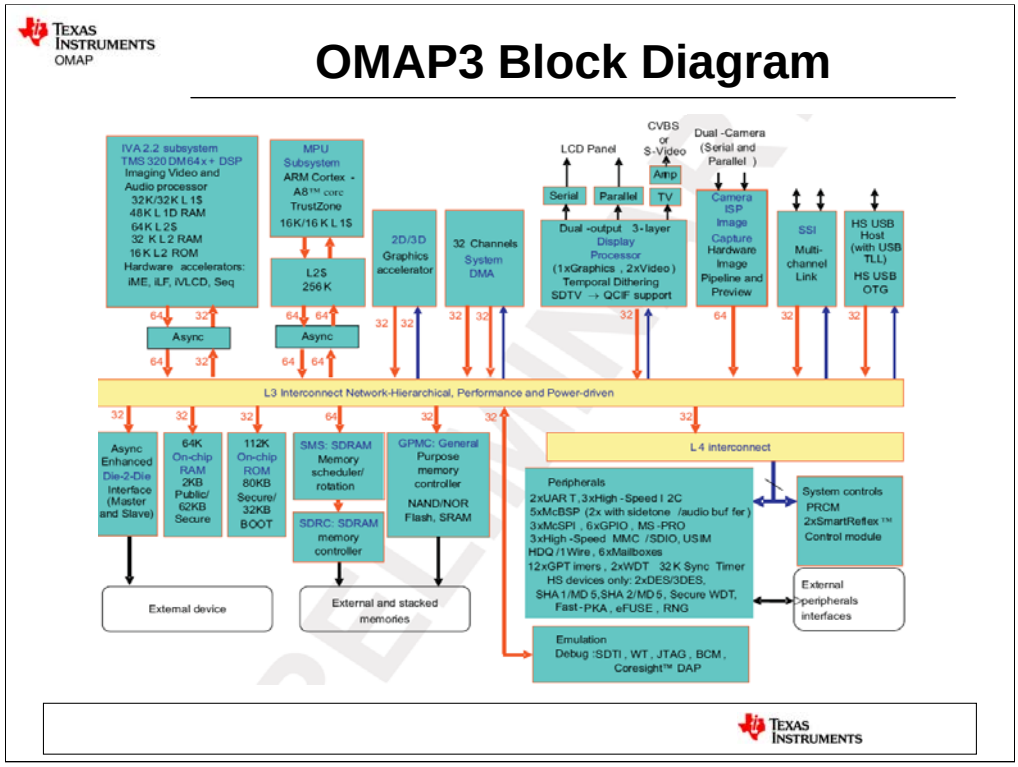
This presentation attempts to give the audience a deeper insight into the hardware capabilities of the OMAP35xx System on a Chip (SoC). The presentation limits itself to the block diagram level of each of the sub-systems discussed and targets a total presentation time of approximately 1 hour including 15 minutes Q and A.

For programming register level depth, timing specific implementation details, etc. the audience is encouraged to read the Technical Reference Manual (TRM) or take on of the customer specific 2-3 day training classes provided on a per customer basis.



The OMAP SoC provides an almost complete System on a Chip. Only few external components are needed to create a complete working system. Besides the basic components, such as level shifters (OMAP 35xx has 1.8V I/O), PHY-s (all USB PHY are external), there will be a need for external devices based on the features required for the full system. This figure shows a system comprised of Blue Tooth and WiFi and external Modem wireless connectivity, Touch screen and LCD User interfaces, fingerprint recognition Biometrics, external Hard drive, SD and MMC cards, etc.

Because of the high level of peripheral integration, the OMAP35xx device family only requires very minimal external HW to control a large amount of different storage, Interface and Display media.



Note that for High Security (HS) devices the engagement is very customer specific and requires a different engagement model. However the crypto HW engines are accessible even on the General Purpose (GP) devices in the OMAP35xx family.

Texas Instruments
OMAP

ARM Sub-system

Texas Instruments

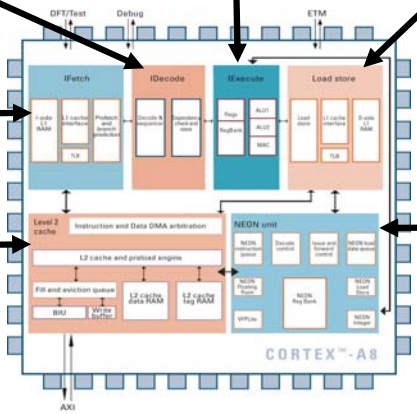
CORTEX A-8 block diagram

In-Order Superscalar Pipeline
- 2.0 DMIPS/MHz

Support for ARMv7
- Added new support for Thumb-2,Jazelle-RCT and NEON

Advanced Dynamic Branch Prediction
- 95% accurate across industry benchmarks

Integrated L2 Cache (0K, 64K – 2M)
- Optimizes access to larger data sets and minimizes bus traffic
- AXI bus to system memory and peripherals
- L2 Preloading Engine for larger data sets

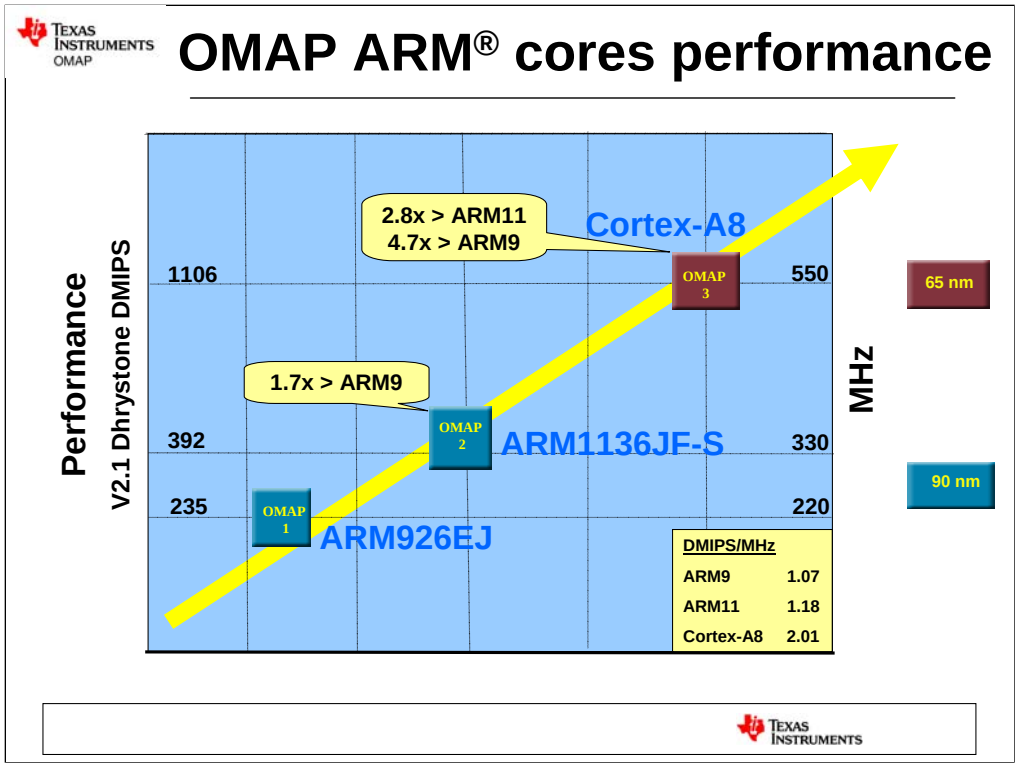


High speed Level 1 Caches (16K)
- Dual 32 entry TLB
- Minimized access time maximizes throughput to main memory
- Controlled array access minimize power consumption

Dedicated NEON unit for media and signal processing
- 2 to 4x performance improvement
- Integer and Floating Point support

NEON™ Hardware Capabilities

- Two Integer 64-bit ALUs operating in parallel
  - Can perform 128-bit length equivalent ALU operation in 1 cycle
- 64-bit datapath with data types up to 128 bits
  - Up to 8-byte SIMD integer
  - 2-way SIMD single-precision FP
- Supports 128-bit data streaming from both L1D$ and L2$
  - Byte permute function allows for on-the-fly data shuffling
- Two Integer Multipliers of 32x16
  - Each can perform one 32x16, two 16x16 or four 8x8 operations in a single pass
  - Support 32x32 operation in two passes



•Dhrystone is a short synthetic benchmark (simple programs that are carefully designed to statistically mimic some common set of programs) program intended to be representative for system (integer) programming.

•The Dhrystone benchmark contains no floating point operations.

•Dhrystones per second is the metric used to measure the number of times the program can run in a second. Dhrystone tries to represent the result more meaningfully than MIPS (million instructions per second), because MIPS cannot be used across different instruction sets (e.g. RISC vs. CISC) for the same computation requirement from users. Thus, the main score is just

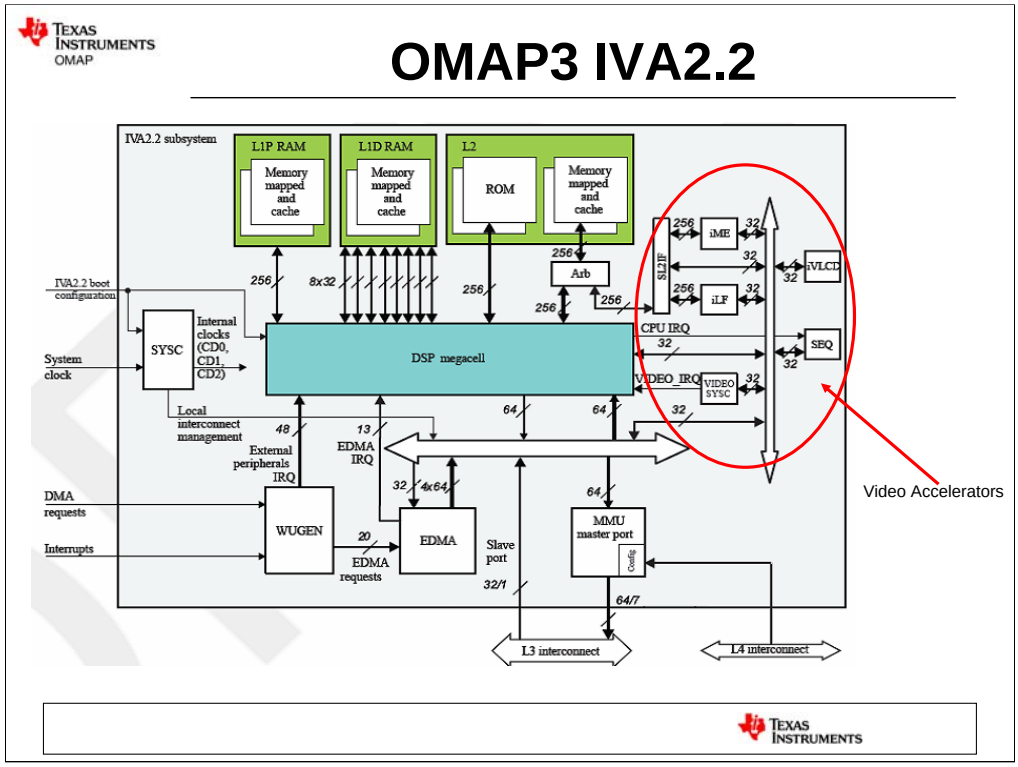
•Dhrystone loops per second. Another common representation of the Dhrystone benchmark is the **DMIPS** - Dhrystone MIPS - obtained when the Dhrystone score is divided by 1,757 (the number of Dhrystones per second obtained on the VAX 11/780, nominally a 1 MIPS machine).

Texas Instruments
OMAP

DSP Sub-system

(IVA = Imaging, Video, Audio)

Texas Instruments



ME = Motion Estimation

VLCD = Variable Length Code/Decode

LF = loop filter HW

SEQ = sequencer

Video Sysc = ??

OMAP3 Video Performance Comparison*

Scenario	Cortex A8 & Neon w/ HLOS 550MHz	OMAP3530 w/ IVA2.2 400MHz
MPEG4 SP encode + audio	HVGA, 30fps	D1-720p, 30fps[2] [4]
H264 BL encode + audio	CIF, 25fps	D1, 30fps[3]
MPEG4 SP decode + audio	D1, 30fps	D1-720p, 30fps[2] [4]
H264 BL decode + audio	HVGA, 30fps	D1, 30fps[3]
VC1 MP decode + audio	VGA, 30fps	D1, 30fps
RealVideo9 decode + audio	-	D1, 30fps[1]
MPEG2 MP decode + audio	-	D1, 30fps
JPEG encode (with ISP)	6Mpix/s (sw)	55Mpix/s (hw)
Video Stabilisation	Yes (TI)	Yes (TI)

* Assumes 25% margin

[1] based on 3rd party implementations
[2] Can support up to MPEG4 Advanced Simple Profile
[3] Can support up to H.264 Main Profile / High Profile
[4] Can support up to MPEG4 HDTV (720p)
[5] Assumes 50MHz for audio (awaiting better audio estimates on Neon)

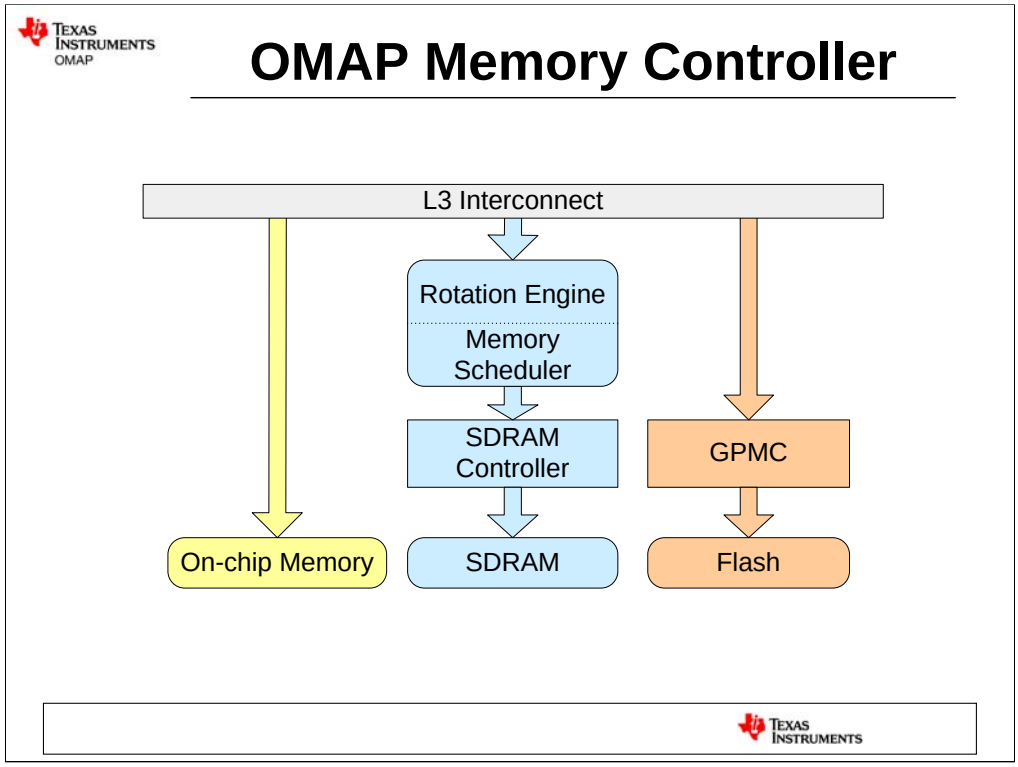
Texas Instruments
OMAP

Memory Controllers

Texas Instruments

Two Memory Controllers

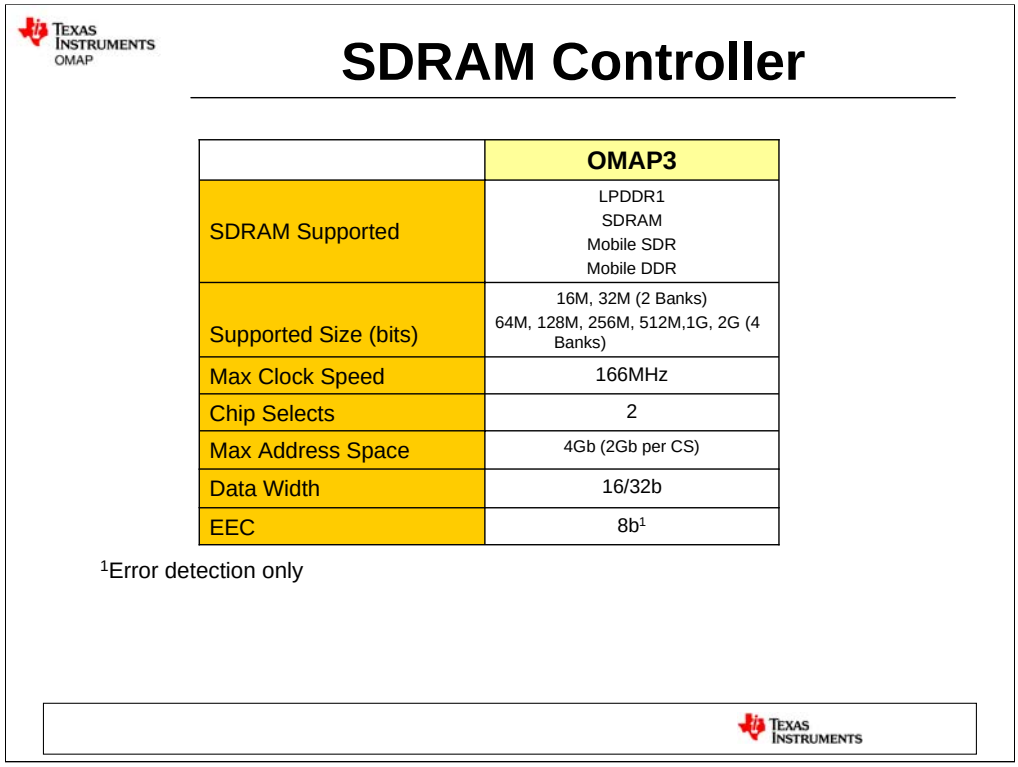
- OMAP contains two dedicated memory controller subsystems:
  - General purpose memory controller (GPMC)
    - Controls all accesses to Flash-type memory
    - Supports maximum 8 devices (up to 1Gbyte in total) with address / data multiplexing
    - Provides HW support for ECC calculation (for NAND)
  - SDRAM controller subsystem consists of these parts (SDRC)
    - Virtual rotated frame buffer
      - Rotation engine supporting rotations of 0°, 90°, 180° or 270°
    - SDRAM memory-access scheduler
      - Optimizes latency and bandwidth usage between initiators
    - SDRAM controller
      - Provides the physical interface to various SDRAM types
      - Two chip selects supporting maximum 256-Mbyte each



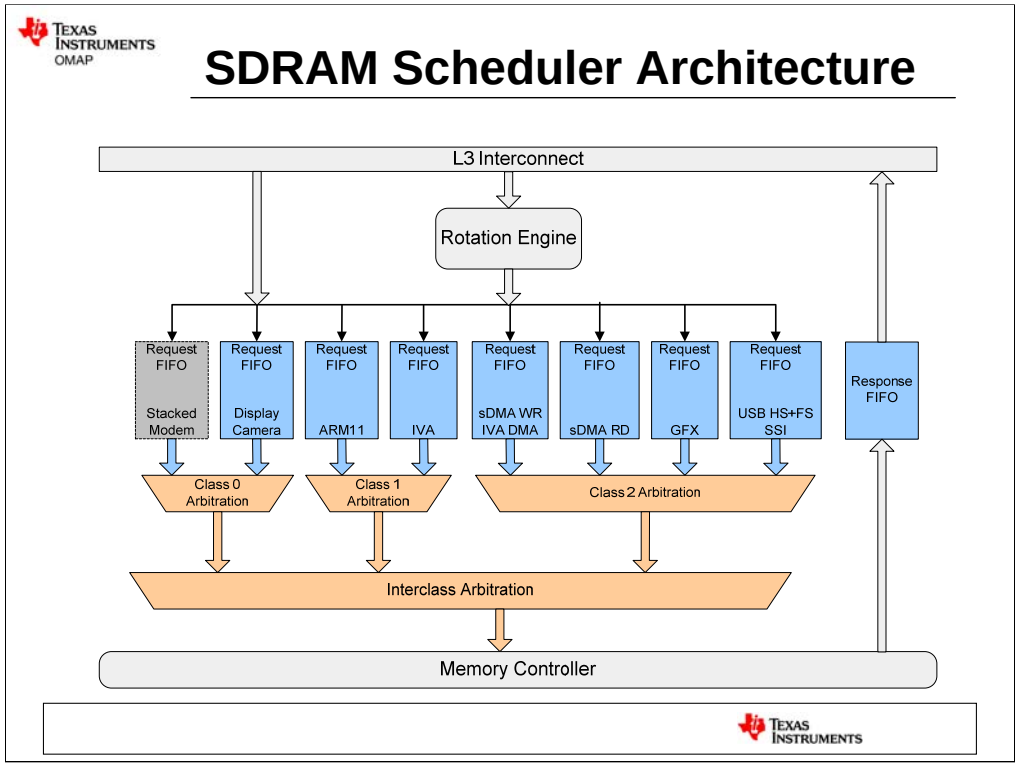
Rotation engine allows in-line rotation of memory images through VRFB, implementing a complex algorithm to minimize page faults. In silicon version(s) up to 3.1, the feature is not working correctly, hence page faults will apply. Recommended not to use in these Si versions.

DMA: supports skip and stride, transparent copy and block fill methods. This allows scaling, rotation and other features.

VRFB = Virtual Rotation Frame Buffer.

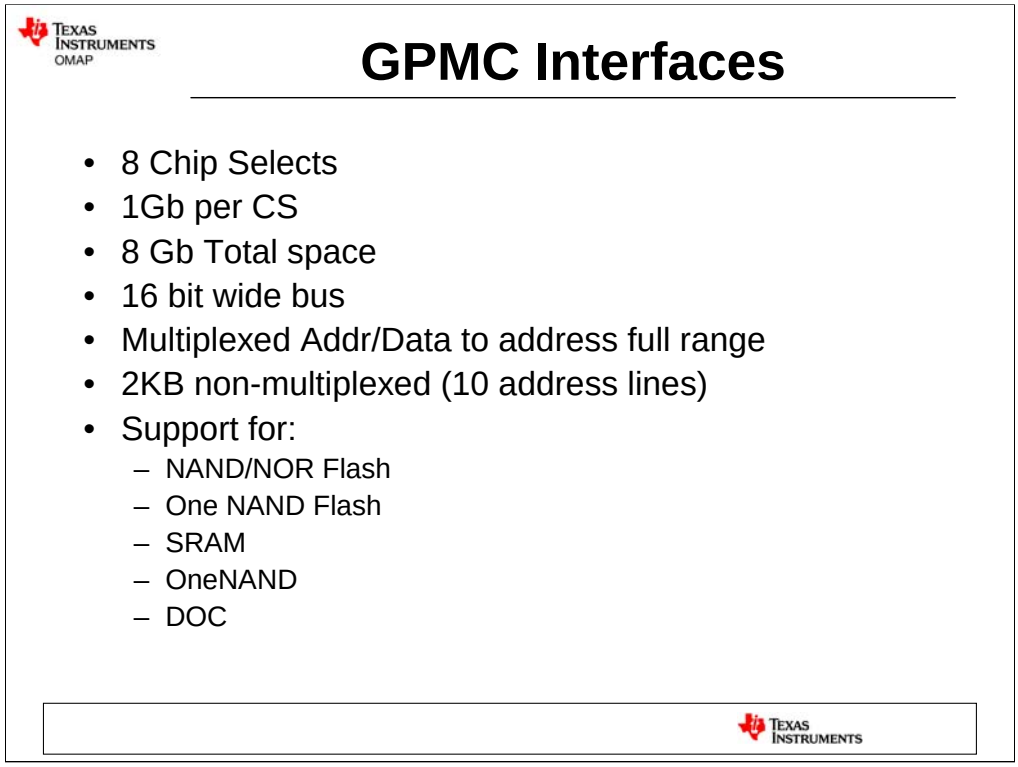


Limitation to Low Power memory types is coming from the limited I/O drive capability of the device as it is targeted to the low power consumption markets. The roadmap versions (like OMAP37xx are targeted to support LP DDR as well as regular DDR.



Note that the arbitration is programmable in each class, but the priorities between classes is not programmable.

Stacked modem on OMAP34xx only – feature will be phased out in the future generations.

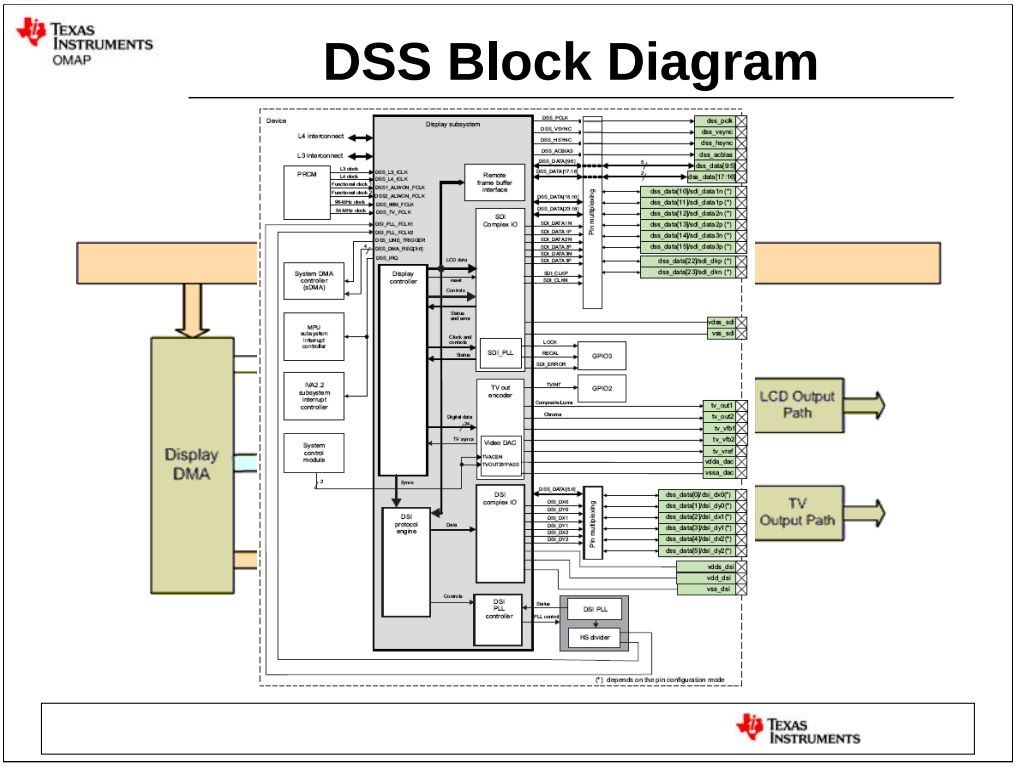


Note that to use the full range of the addressable space on the GPMC bus, one must use it in multiplexed mode. In non-multiplexed mode only 10 address lines are available, limiting the addressable space to 2KB per CS.

Texas Instruments
OMAP

Display Sub-system (DSS)

Texas Instruments



Display modes

· Programmable pixel display modes (1, 2, 4, 8, 12, 16, and 24 bits-per-pixel [BPP] modes)

· Programmable display size supported:

· XGA - 1024x768 VESA Timings at 60 fps (pixel clock = 63.5 MHz)

· WXGA - 1280x800 VESA timings at 59.91 fps (pixel clock = 71MHz)

· SXGA+ - 1400x1050 Direct drive of LCD with minimal blanking at 50 fps (pixel clock = 75MHz)

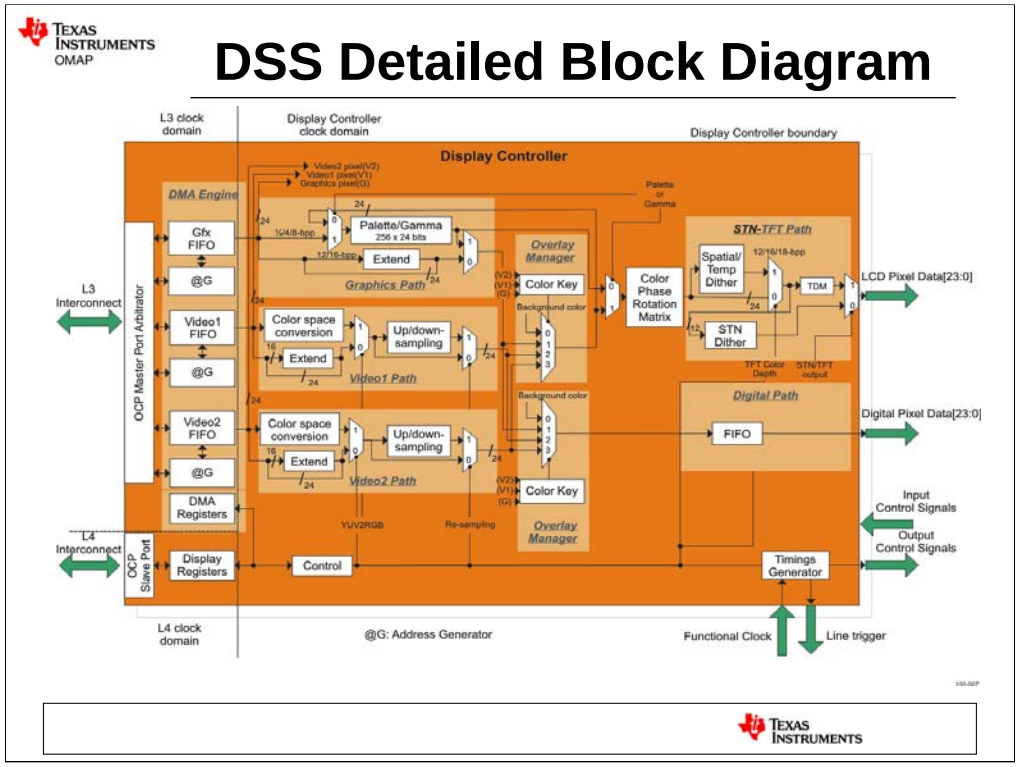
· HD 720p - 1280x720 CEA 861-D TIMINGS at 60 fps (pixel clock = 74.25 MHz)

· 256 x 24-bit entries palette in red, green, and blue (RGB)

· Programmable pixel rate up to 75 MHz

Note: The panel size is programmable and can be any width that is a multiple of 8 pixels (line length) in the range [1:2048] pixels (in the case of the RFBI mode, the minimum transfer

size is a byte). The maximum resolution is 2048 (lines) x 2048 (pixels).



Overlay managers cannot take input from the same source.

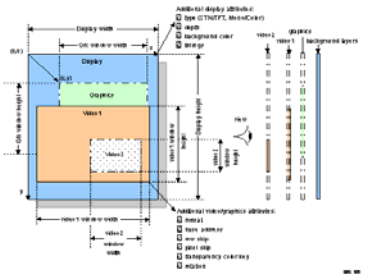
NTSC/PAL encoder outputs with the following standards:

- · NTSC-J, M
- · PAL-B, D, G, H, I
- · PAL-M
- · CGMS-A as described in the CEA-608-x Standard.

– Support Macrovision 7.11 (optional function enabled/disabled by eFuse) and CGMS-A as described in the CEA-608-x Standard.

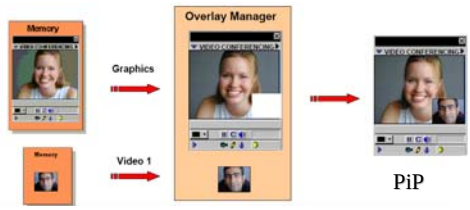
Display Overlay Manager

- Combines different input components into one output image
  - Each input component can be any size up to full display screen size
  - Each input component can start at any location
  - Up to three input components exist:
    - Graphics
    - Video 1
    - Video 2
  - Additionally a solid background color can be selected
- Two overlay managers exist:
  - Overlay manager 1 for LCD output
  - Overlay manager 2 for TV output
  - Cannot share same input source
- Orders the different input components
  - Video2 >> Video1 >> Graphics >> Background

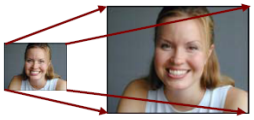


Cannot share the same input source: this means that the image that is put on the LCD can not be replicated exactly the same on the TV output if they are made up from overlays.

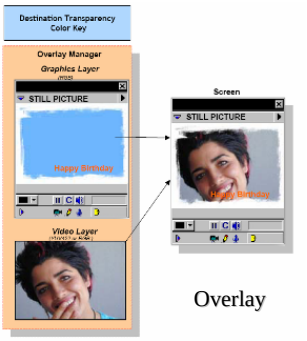
Display subsystem examples



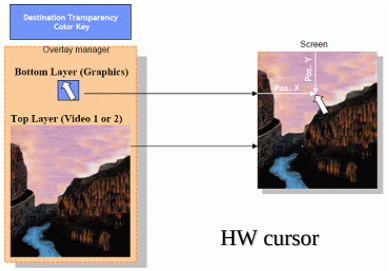
PiP



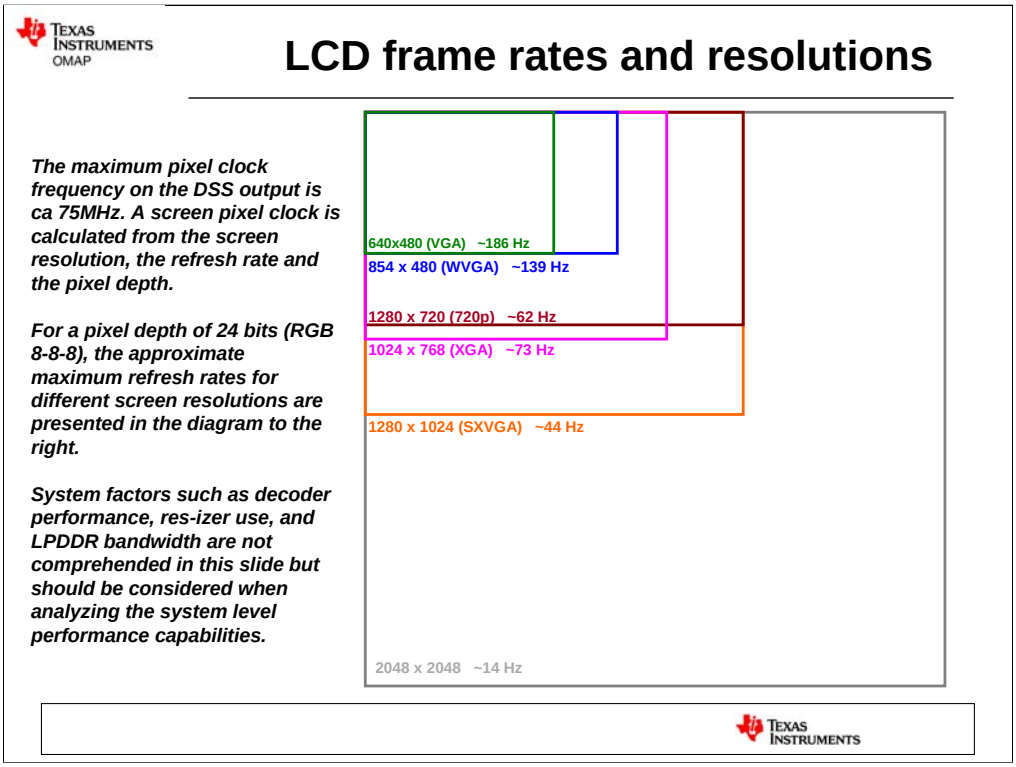
Scaling



Overlay



HW cursor



•OMAP35x LCD controller can support up to 2048 x 2048. However, the challenge is normally keeping enough data flowing to support this resolution.

•Maximum pixel resolution of OMAP35x LCD controller is 2048 x 2048 with clock limited to 74.25 MHz

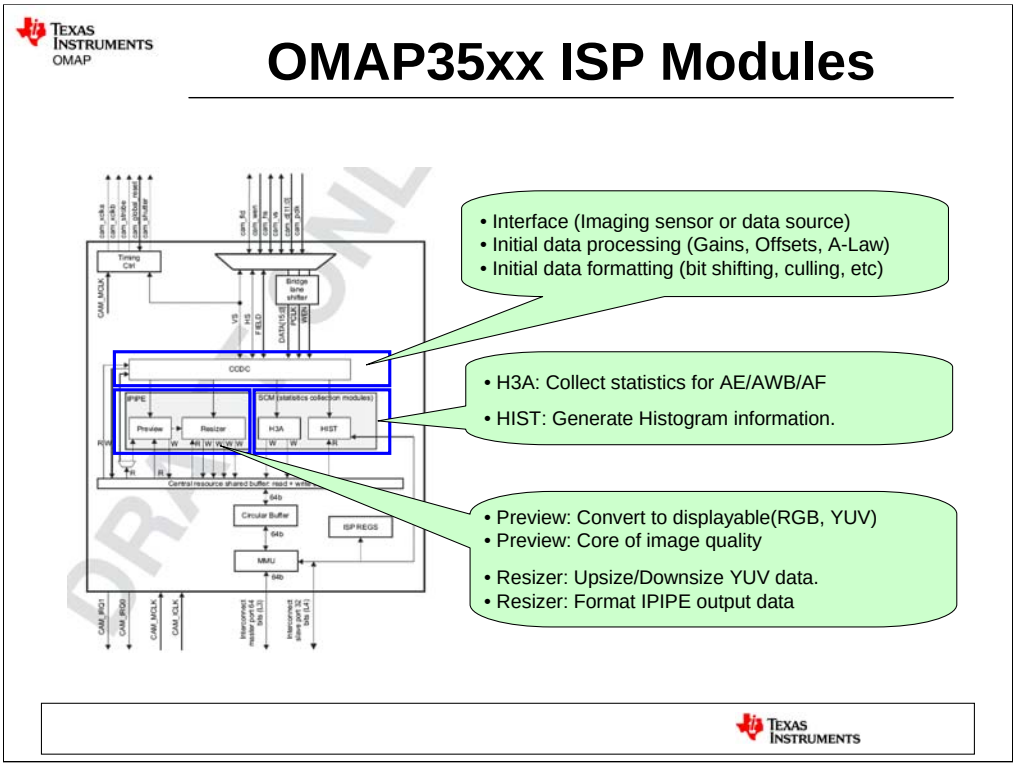
•General rule of thumb for the maximum frame rate (74250000 / (X * Y * 1.3)).

- •For direct drive LCD's the 1.3 can be replaced with a value closer to 1 (this factor is related to blanking times on LCD's)
- •This is an approximation only. Care should be taken to do a more thorough analysis before a final decision is made.

Texas Instruments
OMAP

Camera Interface (ISP)

Texas Instruments



Supports MIPI DS1 and DS2 formats.

AE = Auto Exposure

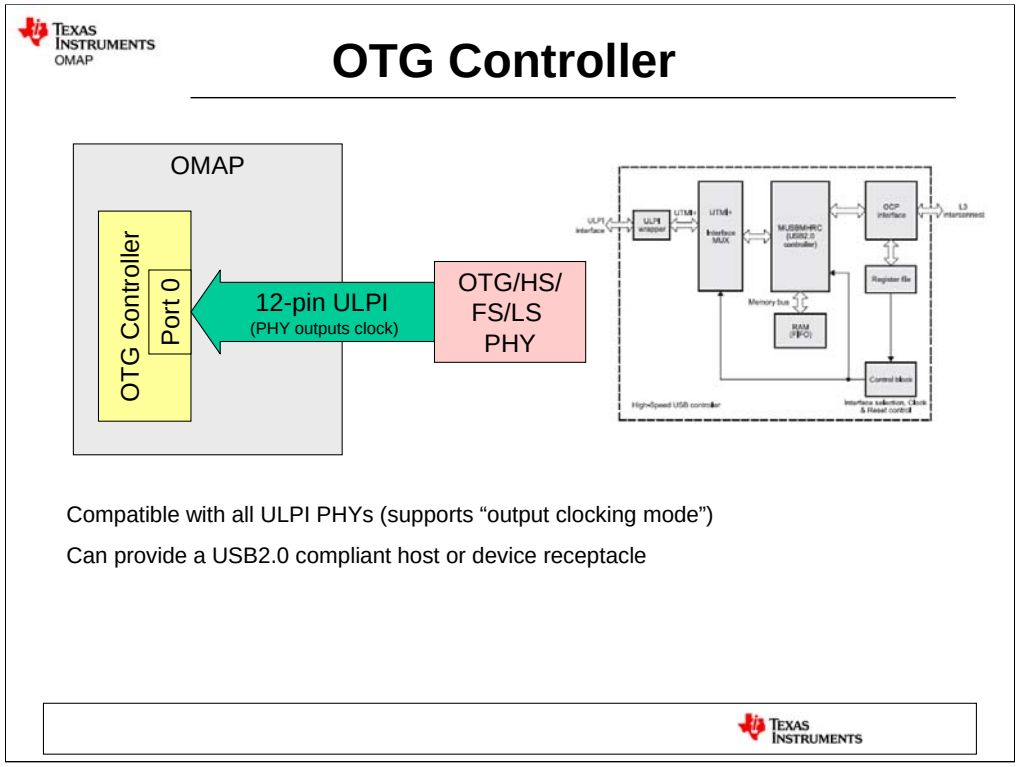
AWB = Auto White Balance

AF = Auto Focus

Texas Instruments
OMAP

USB controllers

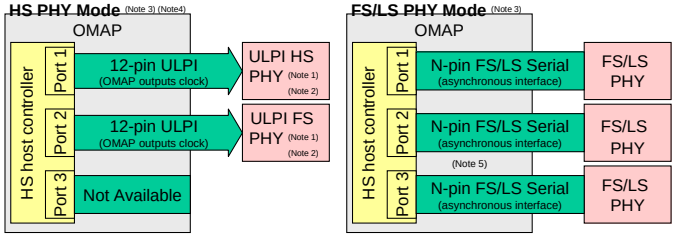
Texas Instruments



Similar to the DaVinci USB OTG Controller without the integrated PHY

OTG controller is MUSBMHRC core IP from Mentor Graphics.

Host Controller



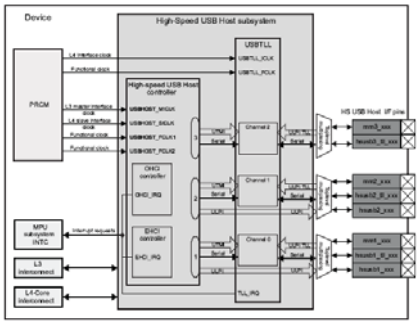
Note 1: Host controller drives the clock, so PHY must support "input clocking mode"

Note 2: OMAP does not support directly connecting FS/LS devices to this PHY, therefore, this PHY cannot provide a USB 2.0 compliant type-A receptacle without the use of a USB HUB

Note 3: HS and FS/LS modes are mutually exclusive in pre 2.1 Si.

Note 5: Port 3 is not available on the 0.65mm BGA package.

Port 2 maximum speed approx 55MHz (errata Si v 3.1)



Note 1: This PHY must support "input clocking mode"

Note 2: OMAP does not support directly connecting FS/LS devices to this PHY. Therefore, this PHY cannot provide a USB 2.0 compliant Type-A receptacle without the use of a HS USB hub.

Note 3: HS and FS/LS Modes are mutually exclusive (ES2.1 and prior)

Note 4: HS PHY Mode and TLL Mode are mutually exclusive (ES2.1 and prior)

Note 5: Port 3 is not available on the 0.65mm package

Texas Instruments
OMAP

Power Management

Texas Instruments

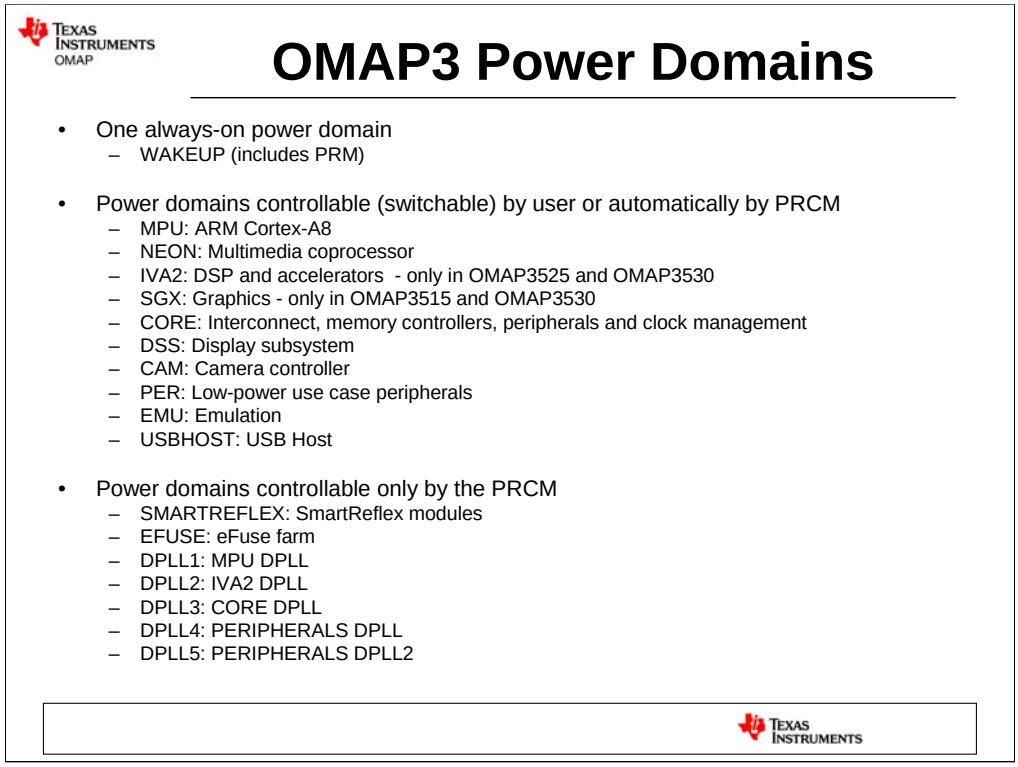
Power Management

OMAP is a System on a Chip with many sub-systems

- Not all sub-systems have to be active all the time
- Different Silicon processes have different power requirements
- Different applications have different frequency/MIPS requirements

How to control all these different handles?

- Dynamic Voltage scaling
- Dynamic Frequency scaling
- Smart Reflex technology
- Selective sub-system de-activation
- Memory retention and silicon logic retention



Variety of domains allows large number of combinations of voltage, power and frequency scaling. However, certain tested combinations should be used to provide the best performance at known combinations of clocks, voltage and power. These are mentioned in the TRM under OPP (operating points).

Voltage Domain chars

Voltage domain	Regulator type	Voltage range	Characteristics
VDD1: Processor sub-system(s) voltage	Ext. SMPS	0V/0.9V-1.35v (Note1)	-SmartReflex control -5 OPPs -Retention voltage, 0V for off-mode
VDD4: Processor(s) memory (ARM and IVA2.2 L1& L2 caches)	Int. LDO	0V/1.0V/1.2V/1.35V	-Internal LDO uses the IO1.8V supply -Scalable -LDO voltage tracks VDD1 when 1.2V<VDD1<1.35V -1.0V when all processor memory are in retention
VDD2: Device core	Ext. SMPS	0V/0.9V-1.15V (Note1)	-SmartReflex control -3 OPPs -Retention voltage, 0V for off-mode
VDD5: Device Core memory	Int. LDO	0V/1.0V/1.2V	-Internal LDO uses the IO1.8v supply -Scalable -1.0V when all core memory are in retention
VDD3: Wakeup	Int. LDO	1.0V/1.2V	-Internal LDO uses the IO1.8v supply -LDO voltage selectable
IO1.8V	Ext. LDO or SMPS	1.8V	-Fixed
IO3.3V	Ext. LDO or SMPS	3.3V	- Fixed
VPLL	Ext. LDO	1.8V	- Fixed
VDDAC	Ext. LDO	1.8V	- Fixed

Note1: Voltage could be optimized lower by SmartReflex (AVS)

DVFS

Dynamic Voltage and Frequency Scaling (DVFS)

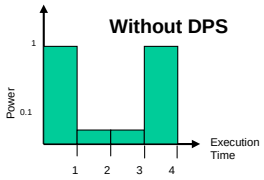
- Higher voltage needed to meet higher performance (frequency)
- No need to run at the highest frequency (and highest voltage and power) all the time
- Depending on performance required by the application scenario, can lower clocks and lower voltage, thereby lowering power consumption
- Define and characterize Operating Performance Points (OPPs) for the device.
  - OPP is a voltage and frequency pair, specifying the minimum voltage at which all devices can meet that frequency requirement (i.e. if a device is picked at random and supplied with the OPP voltage, it will be capable of running at the OPP frequency no matter where it falls on the process curve)
- DVFS applicable to VDD1 and VDD2 in OMAP3

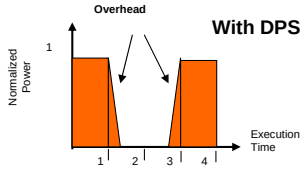
	OPP	ARM MHz	Vdd1
OMAP 35xx	5	600	1.35
	4	550	1.27
	3	500	1.2
	2	250	1
	1	125	0.9

OPP	L3 MHz	Vdd2
3	166	1.15
2	100	1
1	41.5	0.9

Dynamic Power Switching

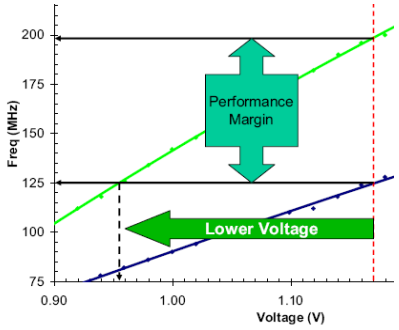
- A section of the device operates in a high performance state to complete its tasks as fast as possible, after which it automatically switches to a low-power state
  - Example: a processor could go into a lower power mode while waiting for a DMA to transfer data
  - Context save/restore may be necessary if switching to a low power state where the memory is lost → additional overhead
  - Acceptable wakeup latencies on the order of microseconds





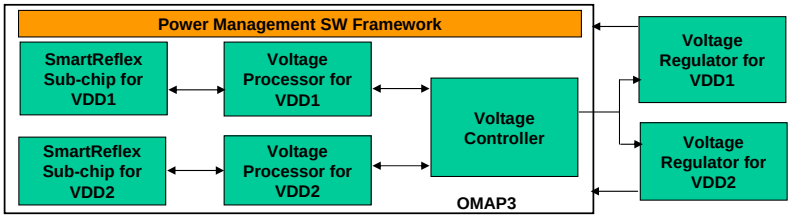
Smart Reflex

- Silicon manufacturing process yields a distribution of performance capability
- For a given frequency requirement:
  - Devices on hot/strong/fast end of distribution can meet this at a lower voltage
  - Devices on cold/weak/slow end of distribution need higher voltage
- Simple system will set the higher voltage for operating all devices
- Smarter system will adapt operating voltage per device:
  - **SmartReflex**, TI's Adaptive Voltage Scaling (AVS) implementation



Green line: Hot device
Blue line: Cold device

SmartReflex Class-3



- Continuously compare actual to target performance
- Notify system of excessive performance error

- Compute voltage compensation needed for performance error seen
- Initiate I2C commands

- Manages the use of I2C4
- Issues I2C commands to external voltage regulators

- Voltage regulators with output level programmable via a single I2C register write

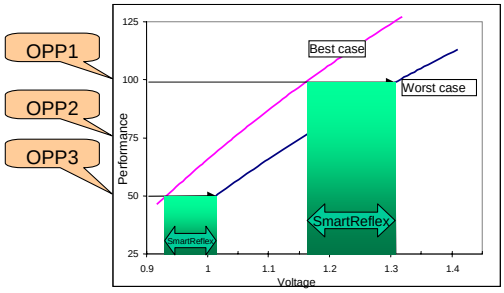
Hardware
Software

VDD1: vdd_mpu
VDD2: vdd_core

DVFS vs AVS

DVFS:

- Select OPP from available OPPs based on MIPS requirement in scenario
- Lower frequency requirement -> lower voltage
- All die treated the same for a particular application scenario



	OPP	ARM MHz	Vdd1
OMAP 3503	5	600	1.35-1.12
	4	550	1.27-1.07
	3	500	1.2-1.00
	2	250	1.0-0.9
	1	125	0.9-0.8

OPP	L3 MHz	Vdd2
3	166	1.15-0.95
2	100	1.0-0.85
1	41.5	0.9-0.8

AVS (SmartReflex)

- After selection of OPP, scale voltage based on device-specific properties (process capability, temperature)
- Faster (also stronger/warmer) process -> lower voltage
- Each die treated differently

OMAP35x power options