Solving Common Design Issues in High-Speed Data Converters

Texas Instruments

Overview of Topics

- **Advanced Topics - ADC**
  - **Sampling Theory**
  - **Analog Input**
  - **Clock/SNR Relationship**
  - **Digital Outputs**
  - **Evaluation**
  - **Dithering**
  - **Inter-leaving**
  - **Averaging**

Sampling Theorem

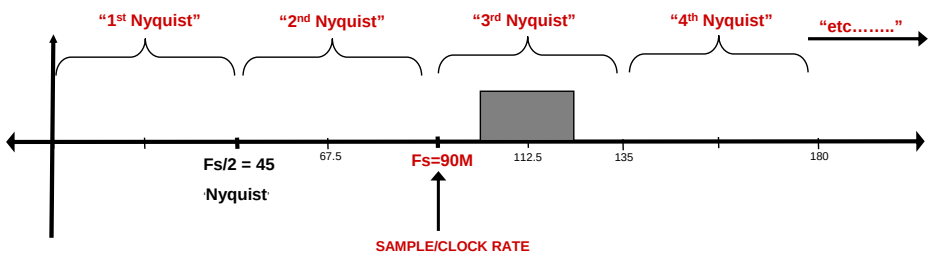
- Sampling
- Nyquist
- Aliasing

What did Nyquist Say about Sampling?

- **The** Nyquist Frequency**, named after Harry Nyquist or the Nyquist–Shannon sampling theorem, is half the sampling frequency of a discrete signal processing system.**

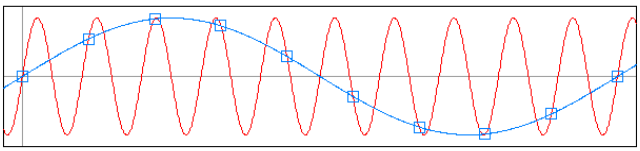
- **The** Nyquist Rate **is the minimum sampling rate required to avoid aliasing when sampling a continuous signal. In other words, the Nyquist rate is the minimum sampling rate required to allow *unambiguous* reconstruction of a band-limited continuous signal from its samples. If the input signal is real and band-limited, the Nyquist rate is simply twice the highest frequency contained within the signal.**

Nyquist Zones



What is Aliasing?

- **Aliasing - two different sinusoids give the same digital samples**
  - **If F_s is the Sampling Frequency (clock rate)**
  - **a high frequency $F_{red} = 10/9 * F_s$**
  - **and a low frequency at $F_{blue} = 1/9 * F_s = F_{red} - F_s$**
  - **Both look like $1/9 * F_s$ to the ADC**
  - **Thus one might say,**
    - **"the frequency at F_{red} is aliased down, or *under-sampled*, to be at frequency F_{blue} at the ADC digital outputs in the spectral domain"**
    - **Or better yet, "the ADC can't tell the difference"**



example: Wikipedia.org

Under-sampling (Aliasing)

- We just down-converted a signal from a high frequency to a lower frequency – that sounds useful
  - This is called Under-sampling
- This usually requires an analog frequency mixer
- What is not always clear in the definition of the Nyquist Rate is that it refers to the bandwidth of the signal, not the frequency
  - In the example given, the bandwidth of each signal is practically zero – these are discrete tones at 1/9 and 10/9 of Fs
  - But signals with no bandwidth contain little information and are therefore not usually very useful for communication systems
  - So let's look at aliasing with some bandwidth involved….

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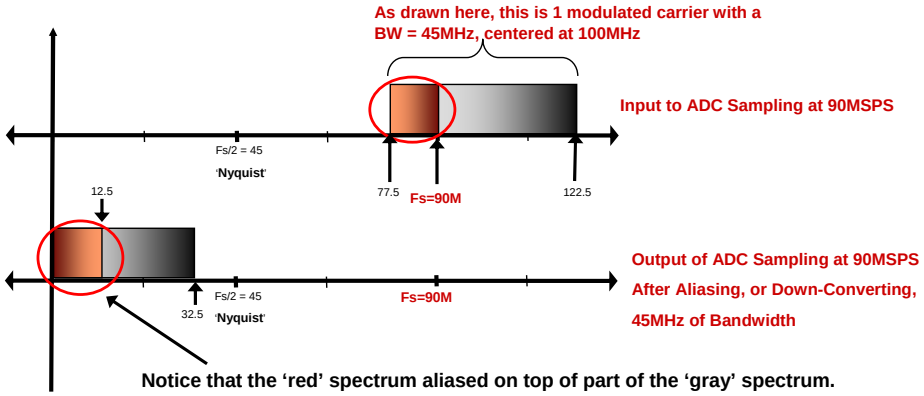
Bad Aliasing (graphically speaking)

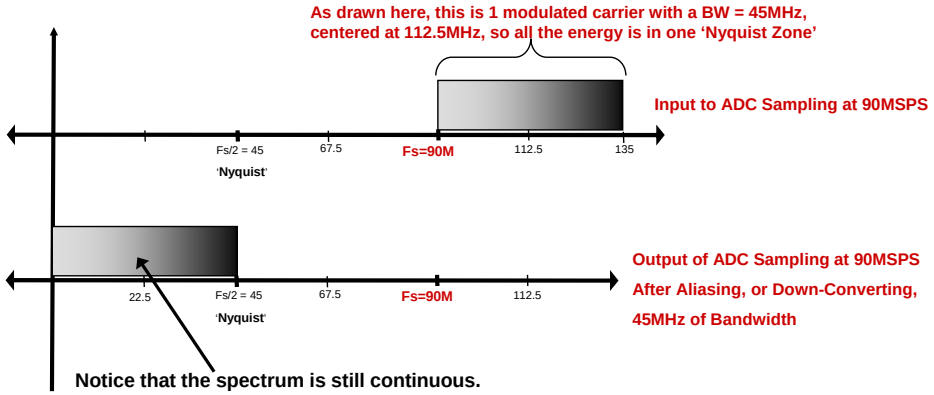


Notice that the 'red' spectrum aliased on top of part of the 'gray' spectrum.

Notice also that the red horizontally inverted, while the gray did not

This would NOT be okay – a digital down-converter (DDC) would not be able to recover the information.

Good Aliasing

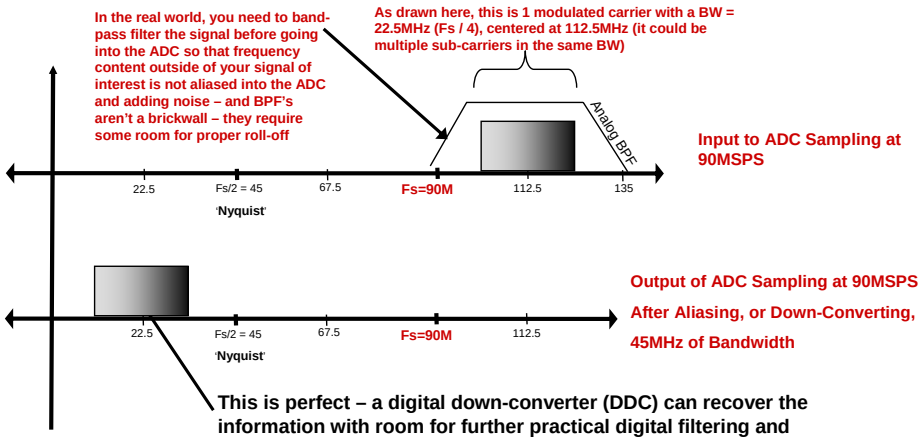


Notice that the spectrum is still continuous.

Notice that the color is not horizontally inverted – this is because we used an 'odd' nyquist zone (the 3rd). If we had used an 'even' zone, the color would reverse – it is spectrally inverted. This is not a bad thing, but might need to be known in order to process the band.

Many radio designs take full advantage of 'good aliasing' to eliminate an entire analog frequency down-conversion stage – saving board space, power, and money

Practical Aliasing Example

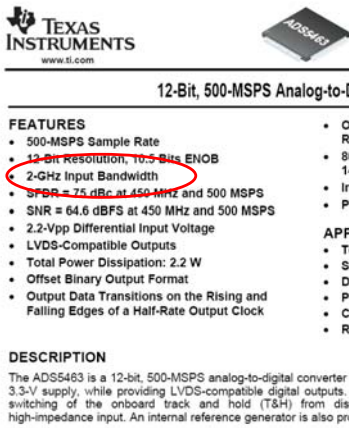


This is perfect – a digital down-converter (DDC) can recover the information with room for further practical digital filtering and digital frequency mixing – usually to baseband.

Many radio designs take full advantage of 'good aliasing' to eliminate an entire analog frequency down-conversion stage – saving board space, power, and money

Can all ADCs Under-sample?

- **Pipeline ADCs are usually designed to have Input Bandwidth that exceeds the intended operating range or 'Performance Bandwidth'**
- **The ADS5463, with a 2GHz Input Bandwidth, could sample input frequencies up to 2GHz (carrier, not BW) at 500MSPS – but the performance is frequency dependent**
- **There are ADCs that cannot under-sample, which are sometimes called Nyquist Converters, and are usually high precision and have much slower sample rates**



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12-Bit, 500-MSPS Analog-to-

FEATURES

- 500-MSPS Sample Rate
- 12-Bit Resolution, 10.5 Bits ENOB
- 2-GHz Input Bandwidth
- SFDR = 75 dBc at 450 MHz and 500 MSPS
- SNR = 64.6 dBFS at 450 MHz and 500 MSPS
- 2.2-Vpp Differential Input Voltage
- LVDS-Compatible Outputs
- Total Power Dissipation: 2.2 W
- Offset Binary Output Format
- Output Data Transitions on the Rising and Falling Edges of a Half-Rate Output Clock

DESCRIPTION

The ADS5463 is a 12-bit, 500-MSPS analog-to-digital converter 3.3-V supply, while providing LVDS-compatible digital outputs. switching of the onboard track and hold (T&H) from dis high-impedance input. An internal reference generator is also pr

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ADC Analog Inputs

Analog Inputs – High Speed ADC

- **Differential Inputs**
- **Input Common Mode**
- **Transformers**
- **Amplifiers**

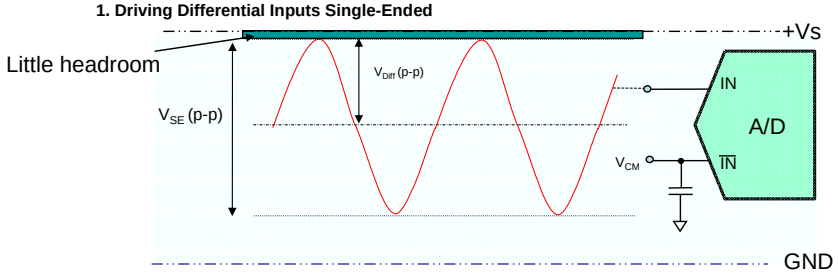
Differential inputs

- **Differential inputs**
  - **Two inputs signals, 180 degrees out of phase**
  - **½ signal swing compared to Single Ended**
  - **Common mode noise rejection**
  - **Typically gives best distortion performance, including high-IF**

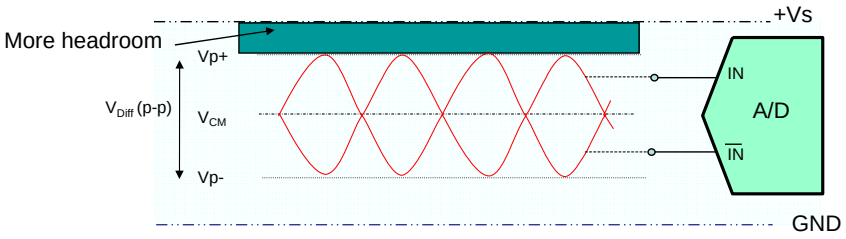
Reduced signal swing requirement typically reduces the drivers distortion, thereby increasing system performance

Single-ended vs. Differential Signals

1. Driving Differential Inputs Single-Ended



2. Driving Differential Inputs Differentially

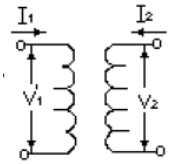


ADC Common Mode (VCM)

- ADCs have an internally generated common mode, however it can be set externally
- Internally generated common mode of the ADC can be used as an output to source the common mode of a driving amplifier
  - Sometimes the VREF can be used as the VCM – but be careful – they are not always the same voltage
- VCM can be forced from an external common mode (ex. amplifier)
  - Follow the datasheet recommendation for range. External VCM range can vary between ADCs. Ex. ADS5547 VCM =1.5V +/-100mV
  - Using external VCM can reduce the dynamic range and headroom.

Transformers

- **Transformers**
  - **Isolated Input\Output – does not pass DC!**
  - **Common Mode can be applied to the center tap to bias ADC inputs**
  - **Can provide voltage step-up or step down**
  - **Can provide Single-ended to differential conversion**
  - **Provides best AC performance, particularly at high-IF**
  - **They are passive devices, no noise or power added**
  - **Zp/Zs = (Np/Ns)^2 = (Vp/Vs) ^{2}**

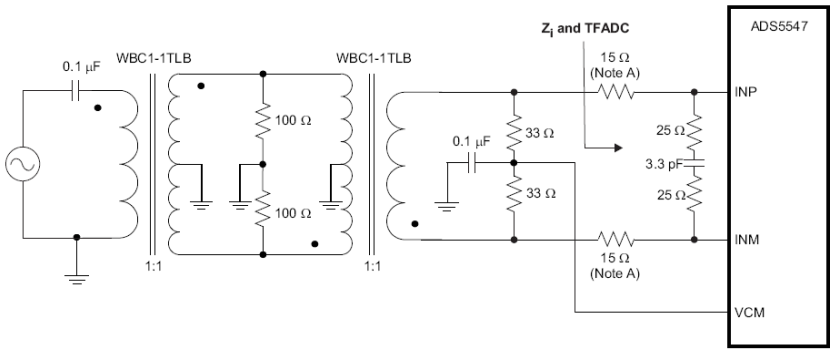


$$P_1 = P_2$$

$$V_2 = n \cdot V_1$$

$$Z_2 = n^2 \cdot Z_1$$

Transformer Example



A. Use lower series resistance (≈ 5 Ω to 10 Ω) at high input frequencies (> 100 MHz)

Figure 38. Example Drive Circuit With RF Transformers

Notice this ADC provides a pin called VCM.
Not all do (even from TI).

Amplifiers

- **Reasons to use an Op Amp**
  - **Op amps can provide the gain needed for driving the ADC at its full dynamic range**
  - **Used in DC or time domain applications**
  - **Baseband applications!!**
  - **The CM input of the opamp can be used to level shift the signal to the right level for the ADC**
  - **Opamps like the THS4509 can either be used as differential in to differential out, or as single-ended in to differential out amplifiers**
- **Considerations when using an opamp**
  - **For best overall performance, the input bandwidth should be limited, such that unwanted noise is also band-limited**
  - **Excellent performance can be achieved up to at least 100MHz or so of analog input**

Amplifier Example

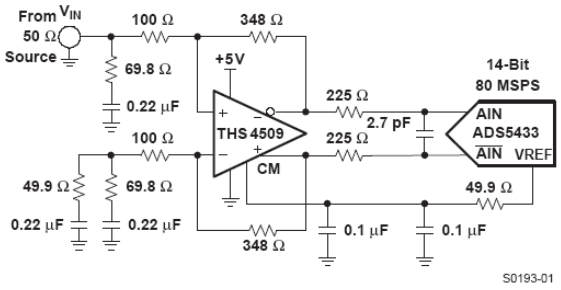


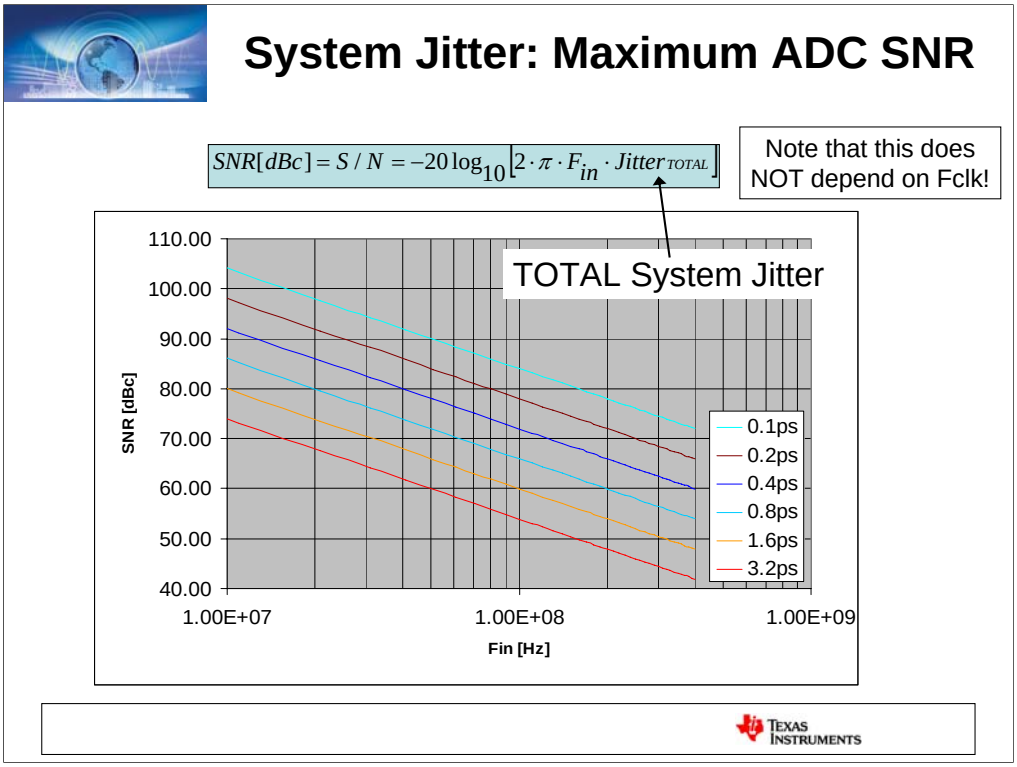
Figure 36. Using the THS4509 With the ADS5433

Notice the VREF is used here as the common mode.
This is allowed here because VREF = VCM

Clock/SNR Relationship

Clock/SNR – Why is this important?

- We have met many customers that do not get the expected SNR from the ADC
- The #1 reason by far is the clock source does not meet the jitter requirement to achieve the desired ADC
- We have seen customers clocking the ADC with 30ps jitter clocks from FPGAs when values far below 3ps were required
- In most applications, when using >12bit converters, it is not a good idea to clock the high speed/performance ADC from an FPGA
- In many cases, the clock circuitry must be treated with similar care to the RF circuitry



This amount of jitter will then limit the theoretical maximum (without taking into account other sources of noise) SNR that one can achieve. For instance, if our total jitter is 0.8ps, at an input frequency of 200MHz, the maximum SNR achievable would be 60dB.

Observe that this will not depend on how many bits the ADC has, or what is my sampling frequency.

Estimation of Clock Jitter Requirement

- **Solve for the *approximate* RMS jitter required of the system in order to get at least 70dB SNR at 100MHz F_{in}**
  - **Total System Jitter Required:**

$$SNR[dBc] = -20\log_{10}\left[2\cdot\pi\cdot F_{in}\cdot Jitter_{TOTAL}\right]$$

$$Jitter_{TOTAL} = (10\text{^}(-SNR[dBc]/20))/2\cdot\pi\cdot F_{in}$$

$$(10\text{^}(-70/20))/2\cdot\pi\cdot 100e6 = 503fs$$

- **…now solve for an estimate of the required Clock Jitter with 150fs of internal ADC aperture jitter**
  - **External Clock Jitter Required (*Estimate*) :**

$$Jitter_{CLOCK} = [(Jitter_{TOTAL})\text{^}2 - (Jitter_{ADC})\text{^}2]\text{^}0.5$$

$$Jitter_{CLOCK} = [(503e\text{-}15)\text{^}2 - (150e\text{-}15)\text{^}2]\text{^}0.5 = 480\ fs$$

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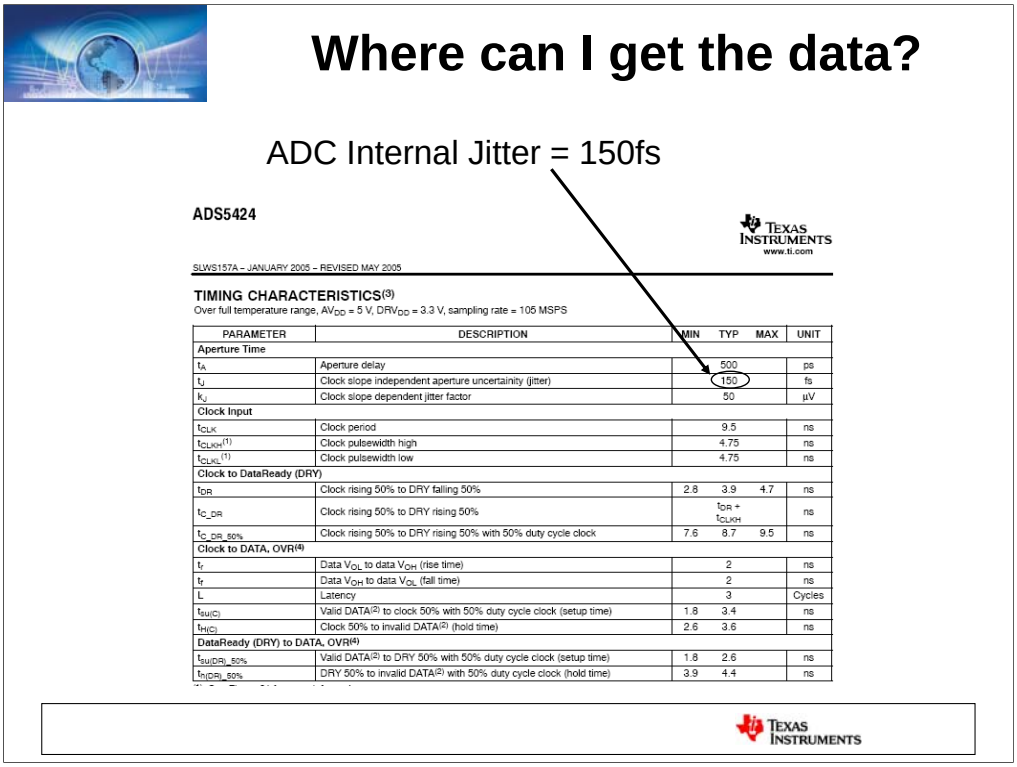
This calculation is useful for a 1st order estimate of the required clock jitter, given a desired SNR, known analog input frequency, and ADC aperture jitter.

Estimation of Clock Jitter Requirement

- The previous calculations are to be used to get a quick estimate of the clock jitter required to achieve the desired SNR
- It assumes that the slope and amplitude of the clock are sufficient
- The ADC could also have dependencies on clock slope and amplitude
- The clock slope dependency relies on information not commonly published (though it is for the example given)
- Clock amplitude dependency can often be found in the form of plots in the datasheet that show performance vs clock amplitude at certain input frequencies

Where can I get the data?

ADC Internal Jitter = 150fs



ADS5424

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SLWS157A – JANUARY 2005 – REVISED MAY 2005

TIMING CHARACTERISTICS(3)

Over full temperature range, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, sampling rate = 105 MSPS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Aperture Time					
t_A	Aperture delay		500		ps
t_J	Clock slope independent aperture uncertainity (jitter)		150		fs
k_J	Clock slope dependent jitter factor		50		μV
Clock Input					
t_{CLK}	Clock period		9.5		ns
t_{CLKH}(1)	Clock pulsewidth high		4.75		ns
t_{CLKL}(1)	Clock pulsewidth low		4.75		ns
Clock to DataReady (DRY)					
t_{DR}	Clock rising 50% to DRY falling 50%	2.8	3.9	4.7	ns
t_{C_DR}	Clock rising 50% to DRY rising 50%		t_{DR} + t_{CLKH}		ns
$t_{C\_DR\_50\%}$	Clock rising 50% to DRY rising 50% with 50% duty cycle clock	7.6	8.7	9.5	ns
Clock to DATA, OVR(4)					
t_r	Data V_{OL} to data V_{OH} (rise time)		2		ns
t_f	Data V_{OH} to data V_{OL} (fall time)		2		ns
L	Latency		3		Cycles
$t_{su(C)}$	Valid DATA(2) to clock 50% with 50% duty cycle clock (setup time)	1.8	3.4		ns
$t_{h(C)}$	Clock 50% to invalid DATA(2) (hold time)	2.6	3.6		ns
DataReady (DRY) to DATA, OVR(4)					
$t_{su(DR)\_50\%}$	Valid DATA(2) to DRY 50% with 50% duty cycle clock (setup time)	1.8	2.6		ns
$t_{h(DR)\_50\%}$	DRY 50% to invalid DATA(2) with 50% duty cycle clock (hold time)	3.9	4.4		ns

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So, considering all the above, Texas Instruments has started to include on its datasheet (see ADS5423/4) two values that the circuit designer can use to compute his estimated final jitter, depending not only on his/her clock jitter, but also on the shape of his/her clock:

1. A term that is constant, independent of clock amplitude. This would basically be the N3 of our model.

2. A term that divided by the clock slope will account for this new addition to the model.

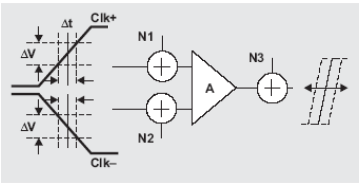
Previous datasheets show a single jitter term that would correspond to a unique clock shape. Circuit designer should be careful with specmanship from some manufacturers who could specify the ADC clock jitter under ideal conditions (with input clock slope very fast).

Internal ADC jitter

$(ADC\_Jitter_{total})^2 = (jitter_{N3})^2 + (jitter_{N1,N2})^2$

$= (jitter_{N3})^2 + (K(N1,N2)/clock\_slope)^2$

Where *clock_slope* for a sinusoidal signal is:



$$V = Amplitude * \sin(\omega t)$$

$$clock\_slope = \frac{dV}{dt} = Amplitude * \omega * \cos(\omega t)$$

$$\max clock\_slope = Amplitude * \omega$$

$$\max clock\_slope = Amplitude * 2\pi f$$

ADC Jitter depends on the clock slope and indirectly the Clock Amplitude

So, let's model the internal ADC jitter as, jitter due to the addition of noise by the ADC clock amplifier on a finite clock slope (N1 and N2), and by the internal ADC clock distribution jitter (N3 - which is not affected by the clock amplitude).

The slope of a sine wave is determined by taking a derivative of the sinewave.

The maximum slope happens at the 0 crossing, so the cosine term = 1 and you are left with an amplitude dependent jitter term.

Calculation for ADC internal jitter (more exact)

- **What is the total internal jitter of the ADS5424 ADC when fed a 3.0Vpp 105M sinewave clock due to aperture jitter and the clock amplitude/slope?**

t_j	Clock slope independent aperture uncertainity (jitter)	150	fs
k_j	Clock slope dependent jitter factor	50	µV

$$(ADC\_Jitter_{total})^2 = (jitter_{N3})^2 + (K(N1,N2)/(Vp*2*pi*f)^2$$

$$158fs = sqrt((150f)^2 + (50u/(1.5*2*pi*105M))^2)$$

- **…and now a 0.5Vp sinewave clock = 338 fs**
- **That is a big jump in jitter (from 158 fs to 338 fs) due to clock amplitude reducing from 3Vpp to 0.5Vpp**
- **This dependency on clock level (and therefore slope) usually shows up in the curves of SNR/SFDR vs Clock Level**

ADC internal jitter Spec

t_J	Clock slope independent aperture uncertainity (jitter)	150	fs
k_J	Clock slope dependent jitter factor	50	µV

- **Notice, even at 3Vpp, the calculated total jitter with a sinewave clock is 158fs, but spec says 150fs**
  - **The 150fs assumes no dependency on clock amplitude/slope**
  - **Therefore, it is usually a good idea to design the external clock jitter with the assumption that the ADC total internal jitter is worse than the spec**
  - **In practice, customers do not and will not go through the calculations using the clock slope dependent jitter factor simply because very few ADC datasheets provide this value and because the customers are not educated on how to use it**
  - **Therefore, estimates are usually made using the aperture jitter value, the simple calculation provided earlier and the plots of SNR/SFDR vs Clock Level (Amplitude)**

Where can I get the Clock Amplitude data?

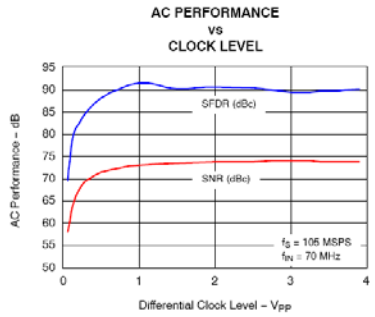


Figure 22

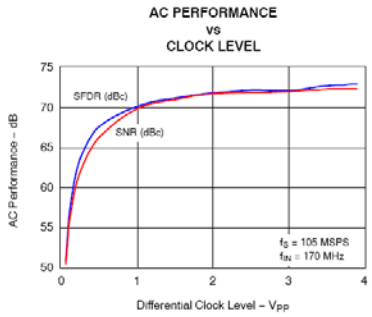
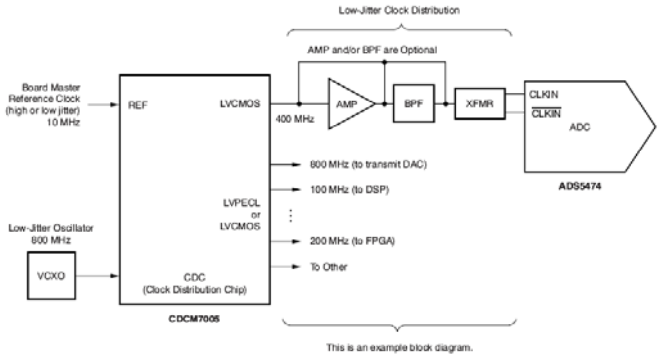


Figure 23

These are from ADS5424

So, considering all the above, Texas Instruments has started to include on its datasheet (see ADS5424) plots that the circuit designer can use to estimate the required clock amplitude.

How Do I Build the Low Jitter Clock Circuit?



Consult the CDCM7005 data sheet for proper schematic and specifications regarding allowable input and output frequency and amplitude ranges.

Figure 47. Optimum Jitter Clock Circuit

The jitter of this total clock solution at the clock input pins on the ADC will be determined primarily by

1) The jitter of the VCO/VCXO chosen
2) The additive jitter in the CDC chip
3) The characteristics of the BPF

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The jitter of this total clock solution at the clock input pins on the ADC will be determined primarily by

1) The jitter of the VCO/VCXO chosen
2) The additive jitter in the CDC chip
3) The characteristics of the BPF

The BPF (bandpass filter) is sometimes required to reject the clock noise that is not near the clock frequency to improve the overall jitter.

The amp is optional if the insertion loss of the BPF (assuming it is required as well) causes the clock amplitude to be too low at the ADC clock pins.

ADC Digital Outputs

- CMOS
- LVDS
- TIMING

CMOS Outputs

- **Parallel CMOS (3.3V logic) outputs**
  - **Pro: Simple to interface to, lower power at slow Fclk**
  - **Con: Requires lots of IO**
  - **Con: Large, fast output edges can create “spurs” on board if you are not careful.**
  - **Example: ADS5500**

LVDS Outputs

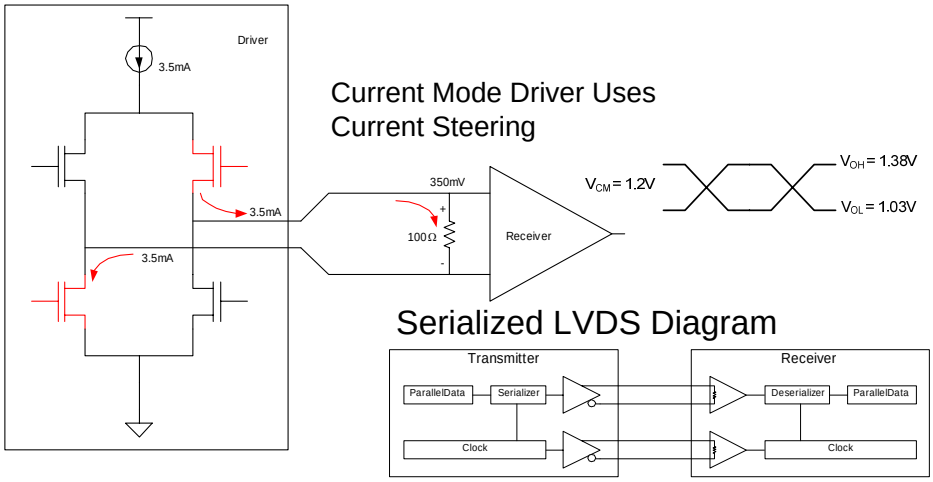
- **LVDS (ANSI/TIA/EIA-644)**
  - **Differential Output Swing 700mVpp (350mVpp on each side)**
    - **Vcm = 1.2V**
    - **Common mode noise immunity**
  - **Current mode output, Iout = 3.5mA**
    - **100 ohm termination needed at receiver**
    - **Class A output has low dI/dt noise**
    - **Supply independent**
  - **Lower EMI on board designs.**
  - **Ex. ADS5547-option, ADS5463, ADS6445, ADS6145-option**

Parallel LVDS

- **LVDS**
  - **DDR can reduce clocking frequency by a factor of 2**
    - **When 1 bit is sent per digital output**
    - **Example ADS5463**
    - **Sometimes called ‘half rate DDR’**
  - **DDR clocks data bits on both rising and falling edges**
  - **Or……**
  - **DDR cuts the output pin count by 2, allows for smaller packages**
    - **When 2 bits are sent per digital output**
    - **Example ADS5547**
    - **Sometimes called ‘full rate DDR’**
  - **DDR is supported by FPGAs (Altera, Xilinx)**

LVDS

Simplified LVDS Diagram



Current Mode Driver Uses
Current Steering

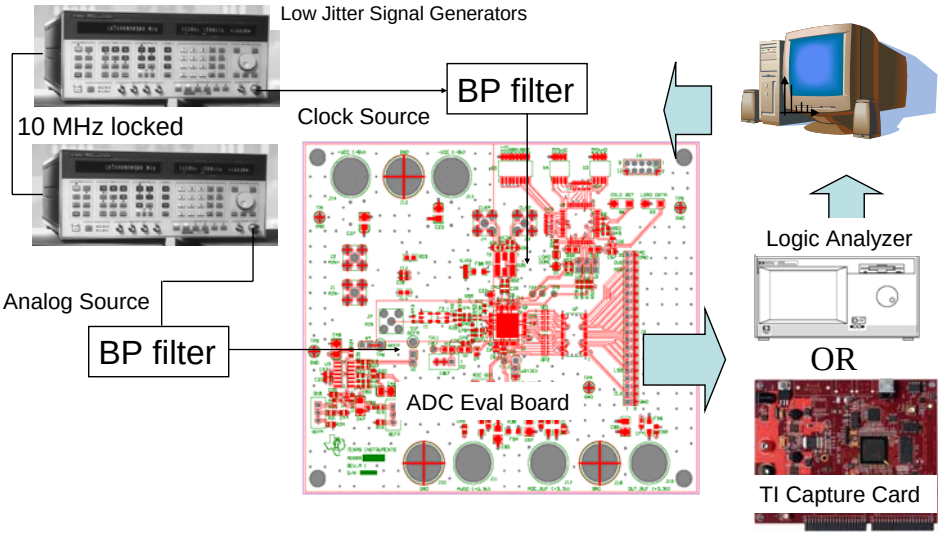
Serialized LVDS Diagram

Output Timing

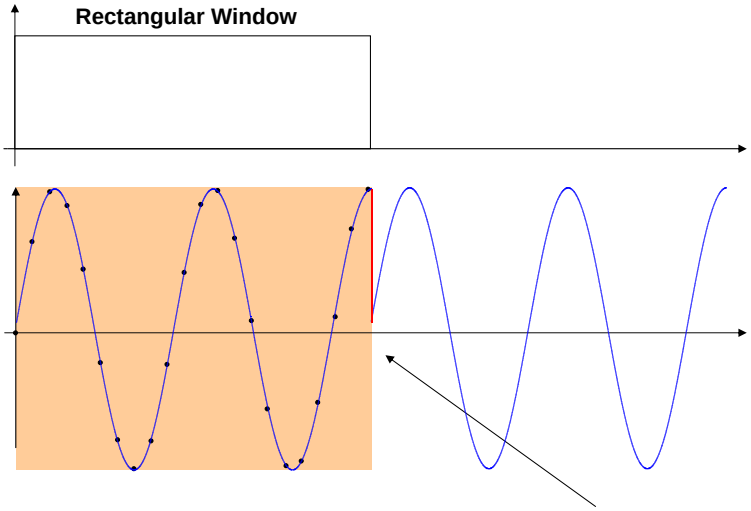
- To achieve proper board operation between an ADC's outputs and the digital device receiving the data (like an FPGA), a timing analysis will be required
- The output timing parameters of the ADC must be carefully studied along with the setup/hold times of the receiving circuit
- Board design is important – all digital lines should be carefully matched in length and impedance
- Many times the clockout of the ADC is used to capture the data into the digital device
  - The clockout may have to be time delayed in order to achieve proper timing
- This is a detailed topic that we will avoid in this material – but beware of it!
  - It causes many headaches for customers and our apps support team

LAB Evalution

Testing the ADC (Low Jitter Setup)

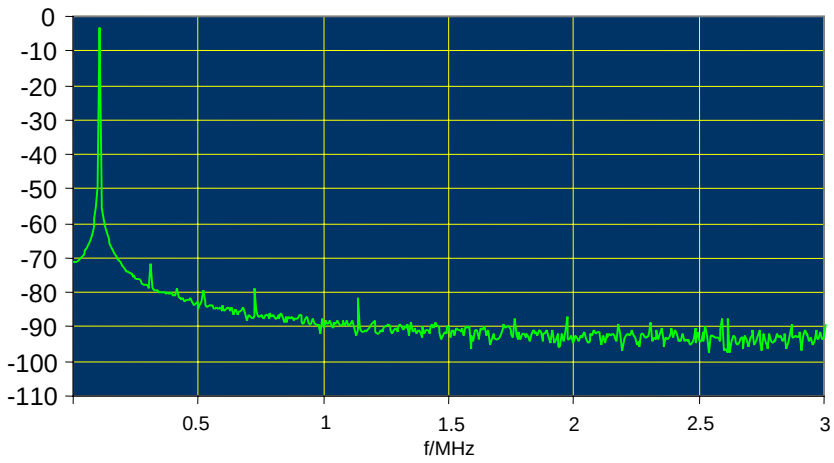


FFT Window



Non-integer number of periods within a FFT window causes discontinuity

Leakage across FFT bins



Coherent Testing

To avoid leakage and pattern generation, ADC test set-up typically uses coherent testing

Requirements for coherence:

$$\frac{f_{signal}}{f_{sample}} = \frac{BIN}{N}$$

BIN = FFT bin

N = Total number of FFT bins

Coherent Testing - Example

Wish:
Fs = 61.44 MSPS
Fin = 50.0000 MHz
N = 8k FFT (8192 samples)

There would be a break in the captured sinusoid because Fin = 50.0000MHz does not land in this FFT bin perfectly

Applying the formula:
BIN = odd_round [N x Fin/Fs] = = odd_round [6666.67] = 6667

Applying BIN back into the formula:
Fs = 61.44MSPS
Fin = BIN x Fs/N = 6667 x (61.44e6 / 8192) = 50.0025 MHz

Now, 50.0025 MHz will land perfectly in a bin, 6667, and we have coherency.

Coherent Testing - Example

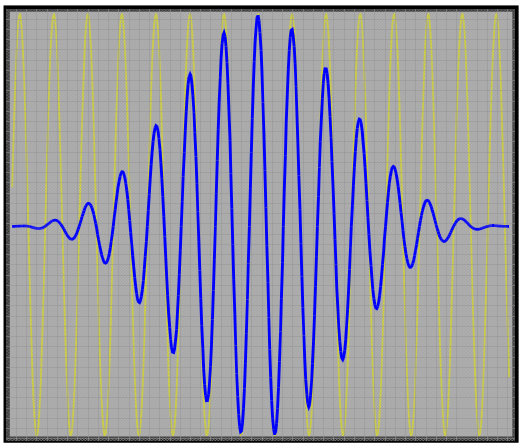
Checking our formula:

$$\frac{f_{signal}}{f_{sample}} = \frac{BIN}{N}$$

$$\frac{50.0025}{61.44} = \frac{6667}{8192} = 0.813842773438$$

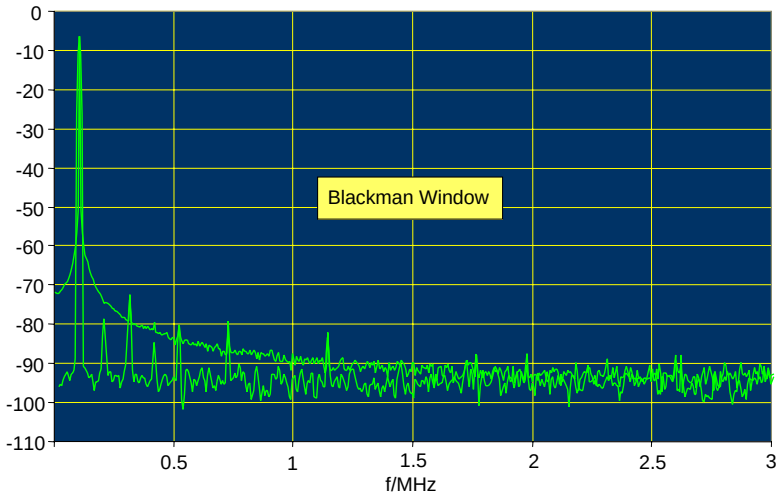
Without coherency, windowing must be applied.

Windowing Sampled Data



Blackman Window: $y(n) = 0.42 - 0.58 \times \cos(\frac{2\pi n}{N}) + 0.08 \times \cos(\frac{2\pi n}{N})$

Windowed Frequency Domain



Necessary if the ADC input frequency is not coherent

Dither

Dither in an ADC

- An ADC will have deterministic and systematic errors that repeat each time those codes are exercised
- Dither (low level noise) can randomize those errors such that they are minimized
- The harmonics are still present, but at lower levels
- Dither can have the adverse affect of increasing the overall noise floor – acceptable for some applications
- Some Dither techniques add the noise in areas of the circuit that need to be randomized and then attempt to subtract the noise later so that the degradation in SNR is minimized or not even noticeable by the user
- It is a technique used to improve the ADC's distortion beyond its inherent linearity

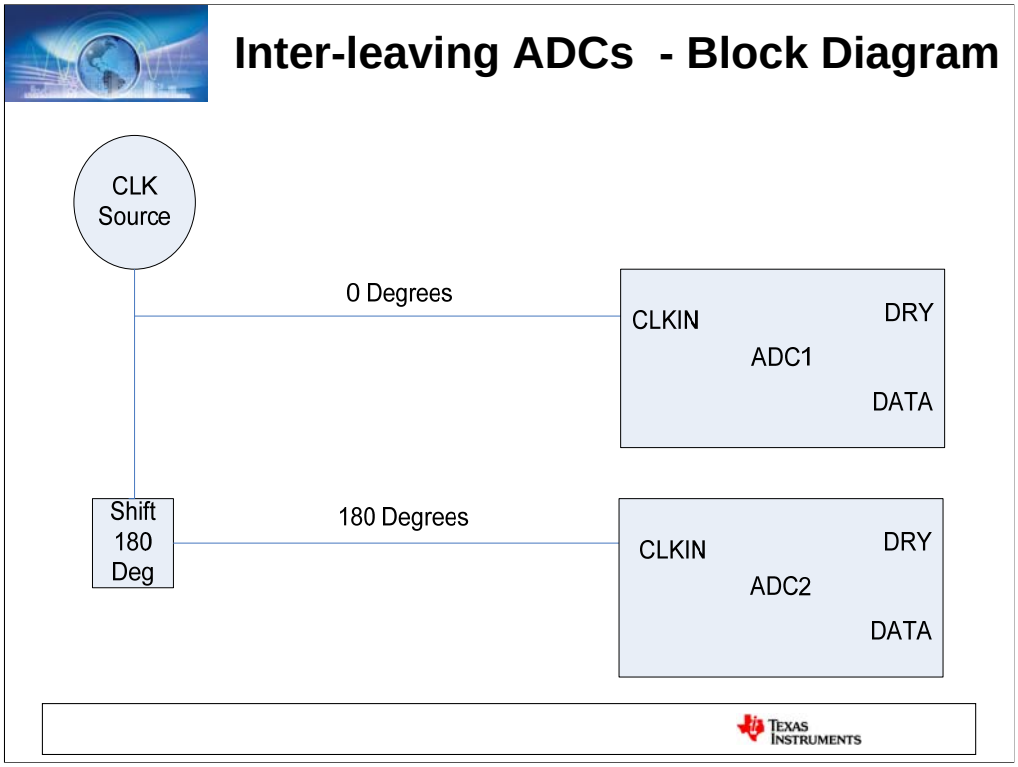
Dither in TI High Speed ADCs

- **TI High Speed ADCs have not traditionally used dither to improve harmonic performance in a way that is apparent to the customer or selectable as an option by the user**
- **We have recently begun to explore using it**
- **Dither can also be applied to the input signal external to the ADC by the customer**
- **In some cases, 'real world' signals contain enough noise to behave as dither**

Inter-Leaving ADCs

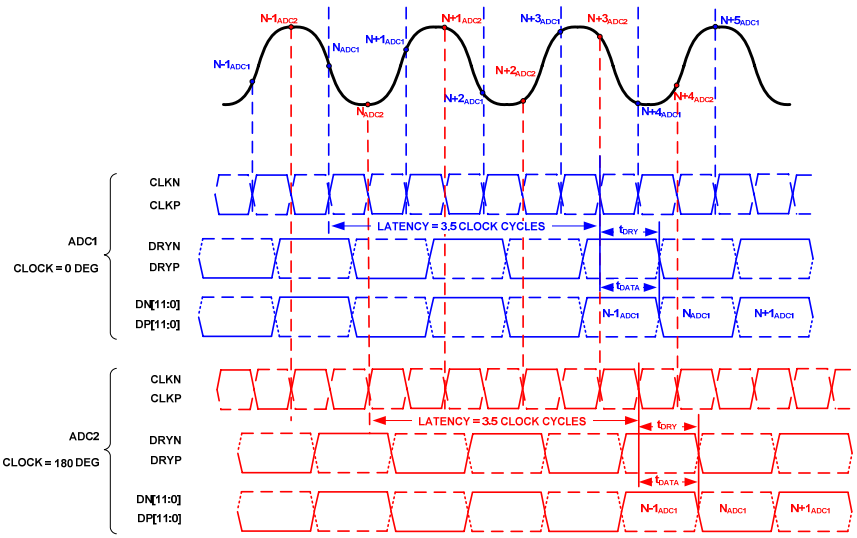
Inter-leaving ADCs

- **What is Inter-leaving?**
  - **Also known as “ping-ponging”**
- **The same analog input signal is converted by multiple ADCs, with each ADC operating off a different phase of clock**
- **The result is a higher effective sample rate, with the number of ADCs as the multiplier in clock rate**



If four ADCs are inter-leaved, each receives 90 degree phase shifted clocks (0, 90, 180, 270 degrees)

Inter-leaving ADCs - Timing Diagram



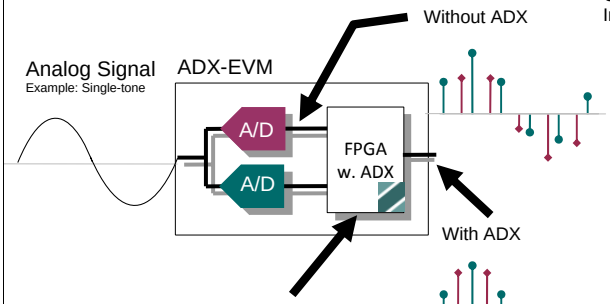
Inter-leaving ADCs: Drawbacks

- A phase (clock) or gain mismatch between any of the ADCs will cause a spur at Fs/2 – Fin
- An offset between the ADCs will cause a spur at Fs/2 if two are inter-leaved and Fs/4 if four are inter-leaved
  - Not a big deal for 2 but in the middle of the band for 4 converters
- The differences in gain, phase, and offset will have to be calibrated to a sufficient level to reduce the spurs to an acceptable dBc.
- This causes system complexity and a re-calibration is likely required with temperature changes
- Some ADCs provide the means to adjust some of these internally, but most do not
- When not provided, the customer has to create methods external to the ADC to adjust for gain, phase, and offset
- (Fs here is the final effective sample rate of the system)

Interleaving of Data Converters

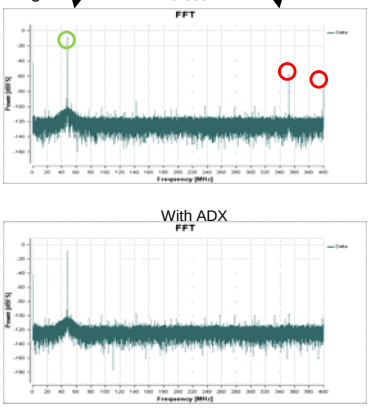
Evaluation Module ADX-EVM [14bits@800MSPS]

On EVM:
2xADS5474 on-board give [14 bits @ 800 MSPS]



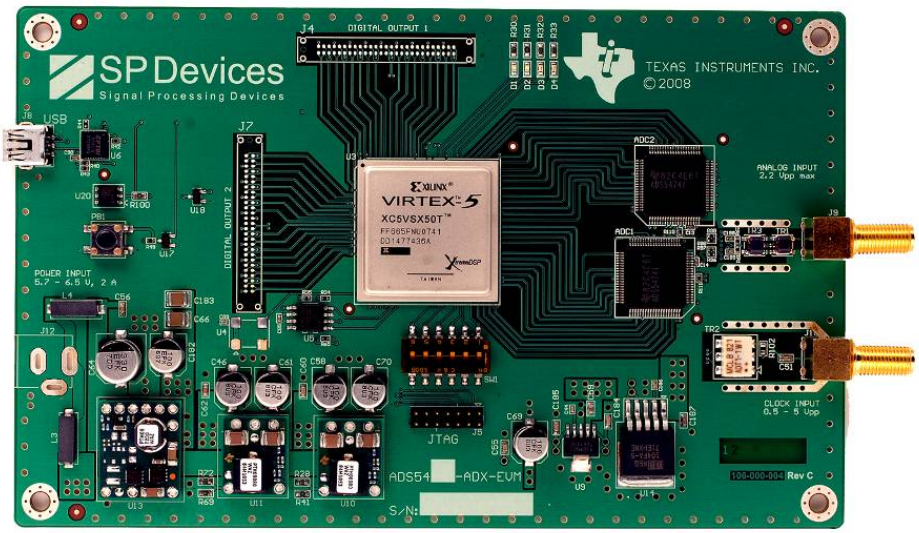
Red rings:
Distortion due to
mismatched ADC's

Green ring:
Input signal



ADX from SP Devices
Patented Estimation and
Correction Algorithms for Interleaving
(FPGA IP-core)

SP Devices' technology


SP Devices
Signal Processing Devices
TEXAS INSTRUMENTS INC.
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J4 DIGITAL OUTPUT 1
J8 USB
J7 DIGITAL OUTPUT 2
XILINX
VIRTEX-5
XC5VSX50T
ADC2
ADC1
ANALOG INPUT
2.2 Vpp max
POWER INPUT
5.7 - 6.5 V, 2 A
CLOCK INPUT
0.5 - 5 Vpp
JTAG
ADS54__-ADX-EVM
S/N:
108-000-004 Rev C

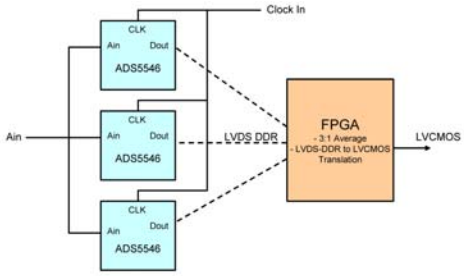
Averaging ADCs

Averaging ADCs

- Similar to inter-leaving, the same signal is converted by multiple ADCs
- They can operate from the same phase of clock and the effective clock rate is not changed
- The benefit is that the digital outputs from each ADC can be digitally averaged together, increasing the SNR by ~10*log10(N)
  - Where N = number of ADCs
  - Assuming they all have identical SNR
- Distortion is not improved using averaging, only uncorrelated noise

Averaging ADCs

- **TI AFA Tommy Neu in FL and Engineering Manager Grant Christiansen wrote an article on the topic for Planet Analog, published June 24, and on the web July 4, 2007**
- **Test Case: Three ADS5546's are averaged**
  – what is the measured improvement in SNR?
- **The Setup: 190MSPS clock**



Averaging ADCs

- **Measured SNR vs Analog Input Frequency**

Fin [MHz]	SNR_{Jitter} at 170fs [dBFS]	Total calc. SNR [dBFS]	Measurement 1 ADC [dBFS]	SNR_{Jitter} at 110fs [dBFS]	Total calc. SNR [dBFS]	Measurement 3 ADC [dBFS]
10	99.4	74	73.9	103.2	78.8	78.5
100	79.4	73.2	73.0	83.2	77.7	77.6
150	75.9	72.3	71.7	79.7	76.6	75.9
210	73.0	71.2	70.0	76.8	75.2	74.5

If the *N* ADCs have the same SNR_{dB}, then the combined SNR is:

$$SNR_{dB,combined} = -10\log\left(\frac{10^{-SNRdB/10}}{N}\right) = -10\log\left(10^{-SNRdB/10}\right) + 10\log N = SNR_{dB} + 10\log N.$$

So, the theoretical increase in SNR for *N* parallel ADC channels with equal SNRs is 10 log *N* decibels, or 3 dB for two channels and 4.8 dB for three channels.

http://www.planetanalog.com/showArticle.jhtml?articleID=200900432

More Questions?

- **Need help selecting a high speed ADC or DAC for your system?**
- **More questions about using a high speed ADC or DAC?**
- **Email:**

  hs_converter_apps@list.ti.com