High Speed Op Amp Design Considerations

Dan Seslar
Texas Instruments
Analog Field Applications

Texas Instruments

Agenda

1) Understanding VFB and CFB Op Amps
   a) VFB and CFB Definitions
   b) Simplified Schematics and Modeling
   c) Differences and Similarities
   d) Application Examples
2) High Speed Design and Layout
   a) Components
   b) Input and output considerations
   c) Impedance matching
   d) Signal routing
   e) Bypass capacitors
   f) Thermal Design
   g) Layout examples
   h) Trouble shooting
   i) Vias

Introduction

- VOLTAGE FEEDBACK AMPLIFIER
  abbreviated VFA or VFB
- CURRENT FEEDBACK AMPLIFIER
  abbreviated CFA or CFB
- VFB and CFB are the two most prevalent architectures used to design high-speed op amps today

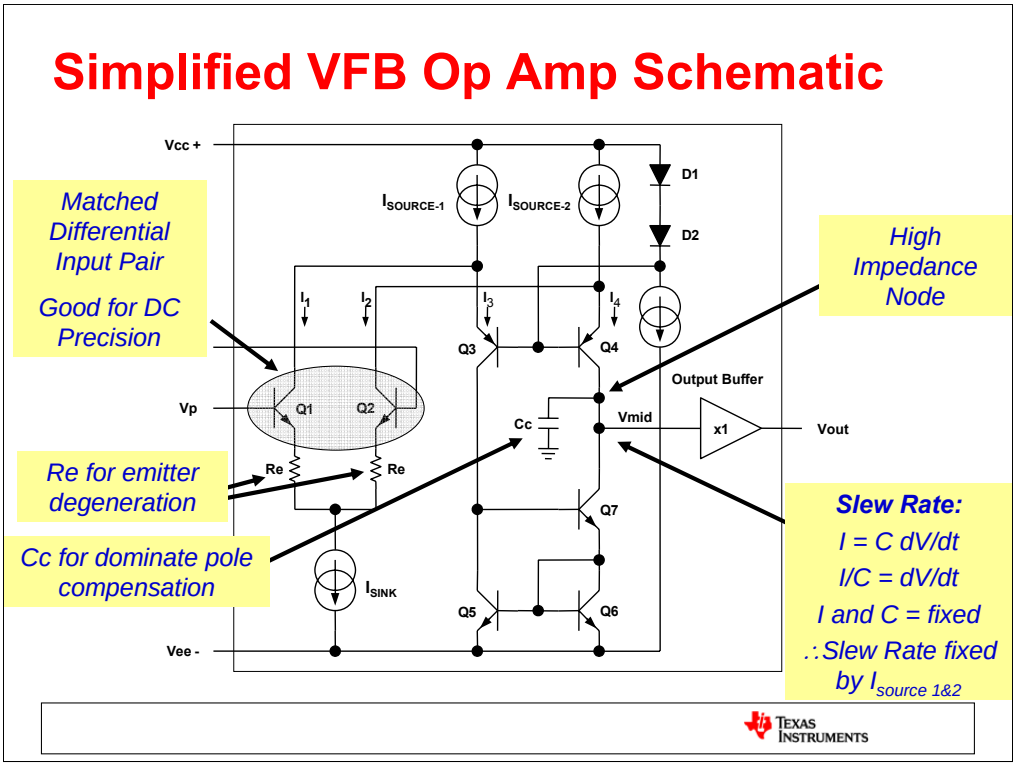
Definitions

- **VOLTAGE FEEDBACK AMPLIFIER – VFB**

1. *The error signal is modeled as a voltage*
2. *Both inputs are high impedance*
3. *Feedback is modeled as a voltage*

- **CURRENT FEEDBACK AMPLIFIER – CFB**

1. *The error signal is modeled as a current*
2. *The positive input is high impedance, and the negative input is low impedance*
3. *Feedback is modeled as a current*



Differential Pair

Q1 and Q2 comprise a classic differential pair (sometimes referred to as a long tail pair). Three equal current sources, I, are used to balance and bias the circuit.

When Vn = Vp, I1 = I2 and the collector currents of Q1, Q2, Q3, and Q4 are equal.

When Vp < Vn, Q2 turns on harder and I2 increases. Since I1 + I2 = I-Sink, I1 decreases. Due to I-Source1 and I-Source2 currents being constant, a decrease in I2 results in an increase in I4. At the same time, since I1 decreased, I3 increased.

When Vp > Vn, Q1 turns on harder and I1 increases. Since I1 + I2 = I-Sink, I2 decreases. Due to I-Source1 and I-Source2 currents being constant, a decrease in I1 results in an increase in I3. At the same time, since I2 decreased, I4 increased.

Thus the differential voltage at the input Vn and Vp causes differential currents to be generated in Q3 and Q4 “folding” them into the high impedance node.

The differential input stage is modeled by a transconductance amplifier, gm.

Since both inputs drive the base of differential pair transistors, the input is fairly high impedance and well matched. This results in generally very good DC precision (Vio is very low along with low drift) and good low frequency distortion.

1High Impedance Node

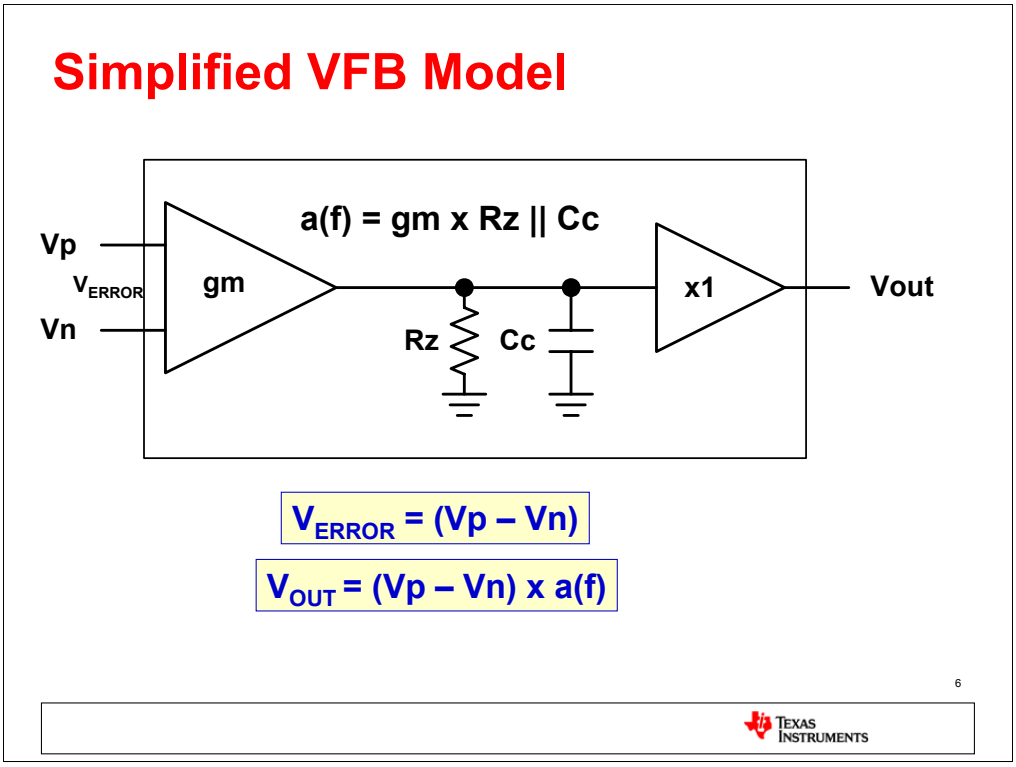
The push-pull currents of I3 and I4 develops a voltage at the high impedance node, Vmid, formed by Q4 and the Wilson current mirror Q5 – Q7. The high impedance stage is modeled by a parallel impedance, Rz||Cc. Rz models the equivalent dc impedance comprised of the output impedance of the current mirror and Q4. Cc is purposely added by design for compensation.

The maximum slew rate of the amplifier is set by the available current, I-Source2 and the mirrored current of I-Source1 (through the Wilson Mirror) of which I-Source1 and I-Source2 are made equal to each other, and the value of Cc.

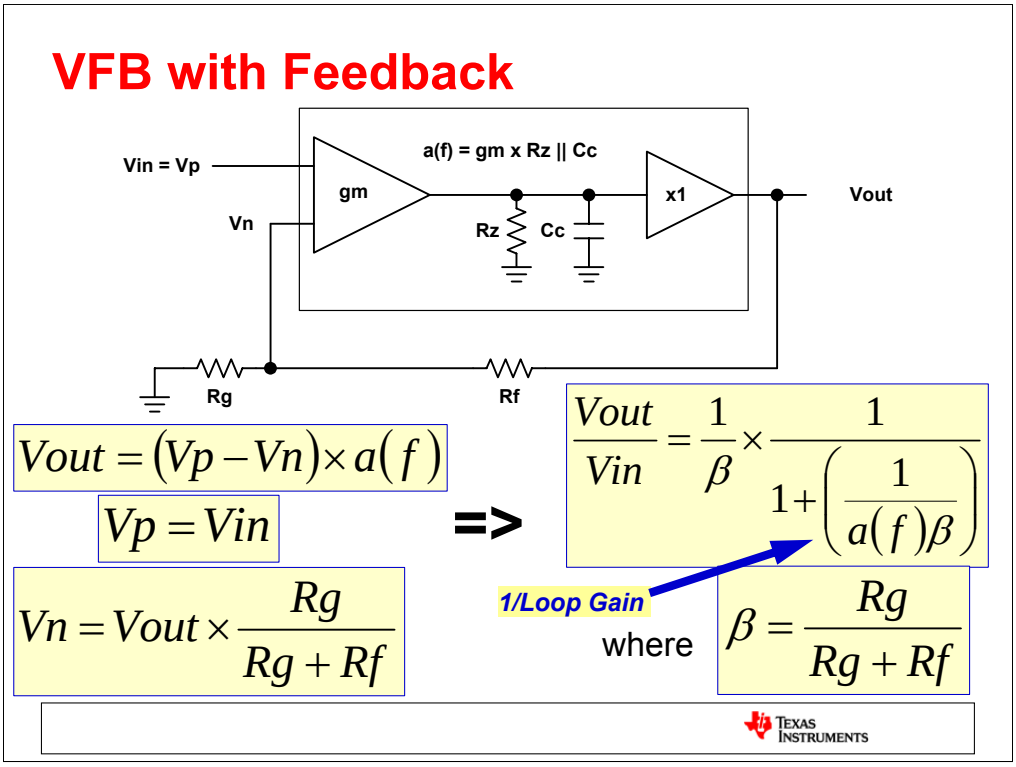
The open loop gain of the amplifier, a(f) = gm x Rz||Cc.

1X1 Output Buffer

Various architectures are used for the output buffer, but it is typically a 2 or 3 stage class AB amplifier. The purpose of the output buffer is simply to give the op amp output drive capability.



A useful block diagram can be constructed for a voltage feedback amplifier as shown above, where the open loop gain, a(f), is equal to gm x Rt||Cc. In this model Vout = Ve x a(f), where the “error” voltage Ve = Vp – Vn.

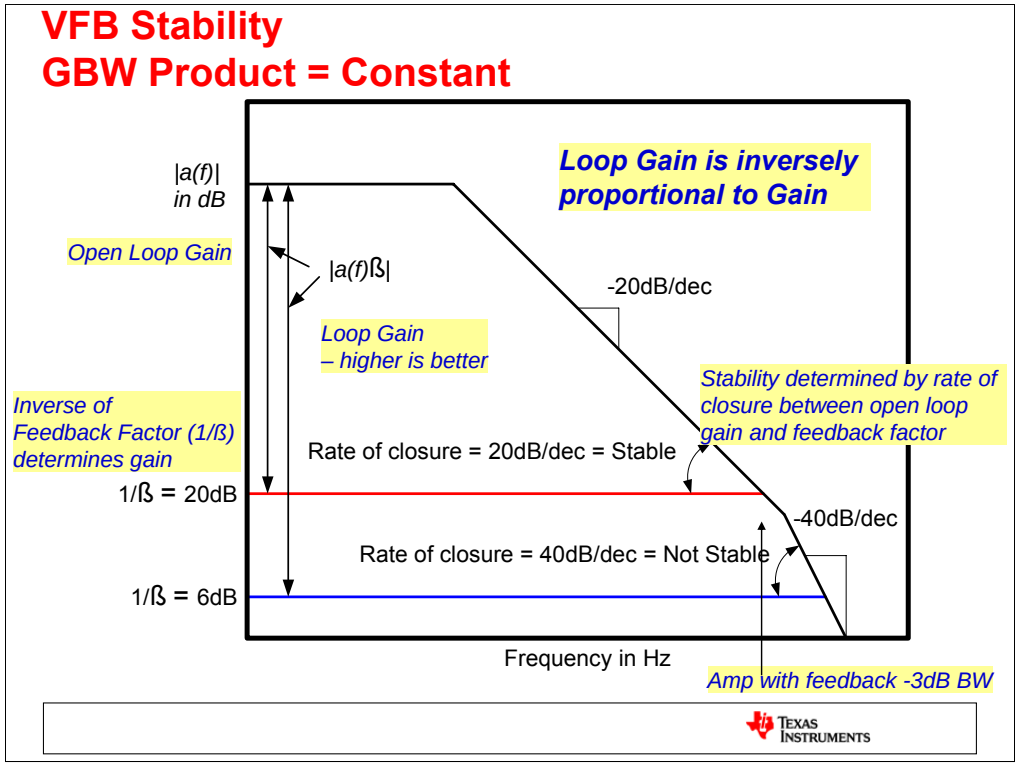


Negative feedback provides a means to set the amplifier gain with stable passive components, and the non-inverting gain can be calculated as shown above. As long as a(f)β >> 1, the non inverting gain is 1 + Rf/Rg.

In similar fashion, it can be shown the inverting gain is equal to (1 – 1/ β) x 1 / (1 + 1 / a(f) β), which can be idealized to (1 – 1/ β) = -Rf/Rg if a(f)β >> 1.

Rg / (Rg + Rf) = β is called the feedback factor as it determines the amount of the output voltage that is fed back to the negative input to null the error voltage, Vp – Vn.

a(f)β is called the “loop gain” as it is the gain around the loop from the negative input to output and back again. It is one of the most critical factors in op amp performance and has special meaning in the context of stability as shown in the following slide.



The diagram shows an op amp that is stable in a gain of 20dB (10V/V), but is not stable in a gain of 6dB (2V/V). This is usually referred to as a minimum gain stable op amp or a “de-compensated” op amp (in reference to a unity gain op amp, which is “compensated” for all non-reactive feedback conditions).

Plotting the inverse of the feedback factor, 1/β, on the plot of a(f) is a good way to visually show the interaction of gain and stability. 1/β is the non-inverting gain of the op amp also referred to as the “noise gain”.

Remember from that analog class you took in college:

1. When the slope of the magnitude in dB is -20dB/dec, the phase is -90°
2. When the slope of the magnitude in dB is -40dB/dec, the phase is -180°
3. On a log scale (which a dB scale is), subtracting is the same as dividing the linear numbers
4. The signal is phase shifted -180° going from inverting input to the output

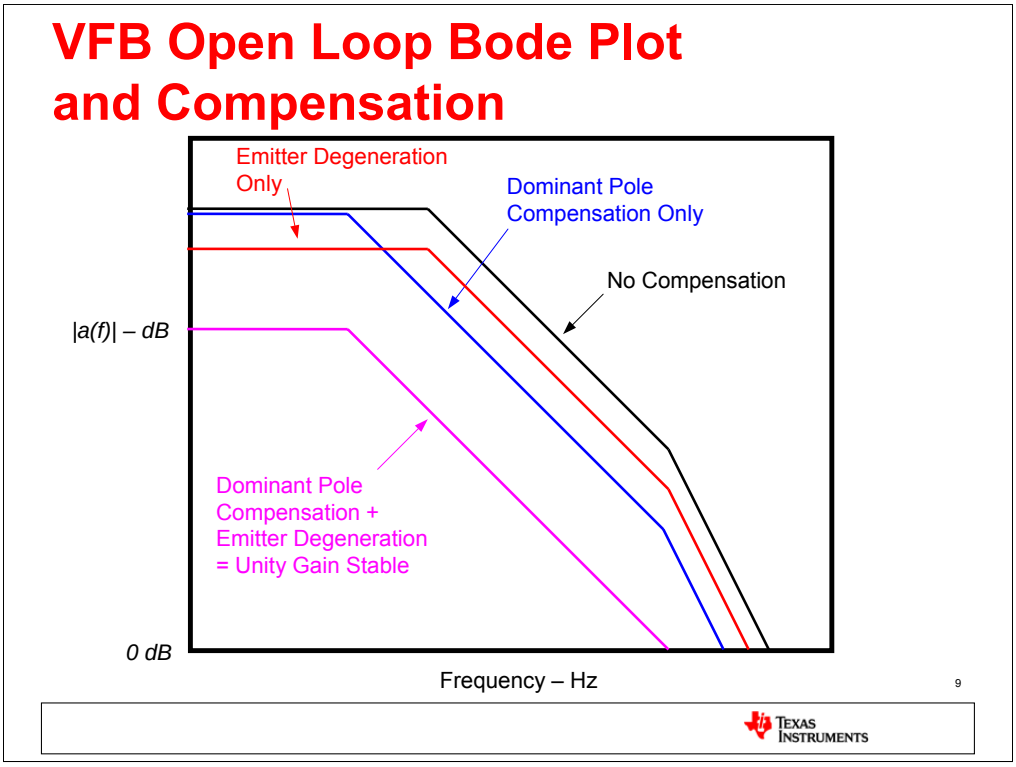
So on this graph, the difference between the 1/β and a(f) is $|a(f)| - |1/\beta| = |a(f)\beta|$. When the difference is 0dB (the point where the two lines intersect) the magnitude of the loop gain, $a(f)\beta = 1$.

The rate of closure between 1/β and a(f) indicates the phase of the loop gain. At 20dB, the phase is -90° and at 40dB it is -180°.

Add the -180° phase shift of the op amp when the closure rate is 40dB, the criteria for oscillation is met i.e. $|a(f)\beta| = 1$ and $< a(f)\beta = \pm 360°$. Under this condition the amplifier will spontaneously oscillate. So the amplifier is stable at a noise gain of 10V/V, but not at 2V/V.

Another point to be drawn from the graph is the constant gain bandwidth product (GBW), which is a standard feature of a VFB op amp. The point where 1/β and a(f) intersect sets the -3dB bandwidth of the amplifier. The -20dB/dec slope is actually a slope of -1. So over most of the useable bandwidth of the op amp the bandwidth is inversely proportional to the gain of the amplifier. Thus it has a constant GBW i.e. if the bandwidth is 100MHz at a gain of 10, it will be 10MHz at a gain of 100 – the GBW is 1000MHz.

For high gain applications, use de-compensated op amps. De-compensated op amps sacrifice stability at lower gain for higher GBW, higher slew rate, and lower noise. They are easily spotted in data books and selection guides by their minimum gain requirements.

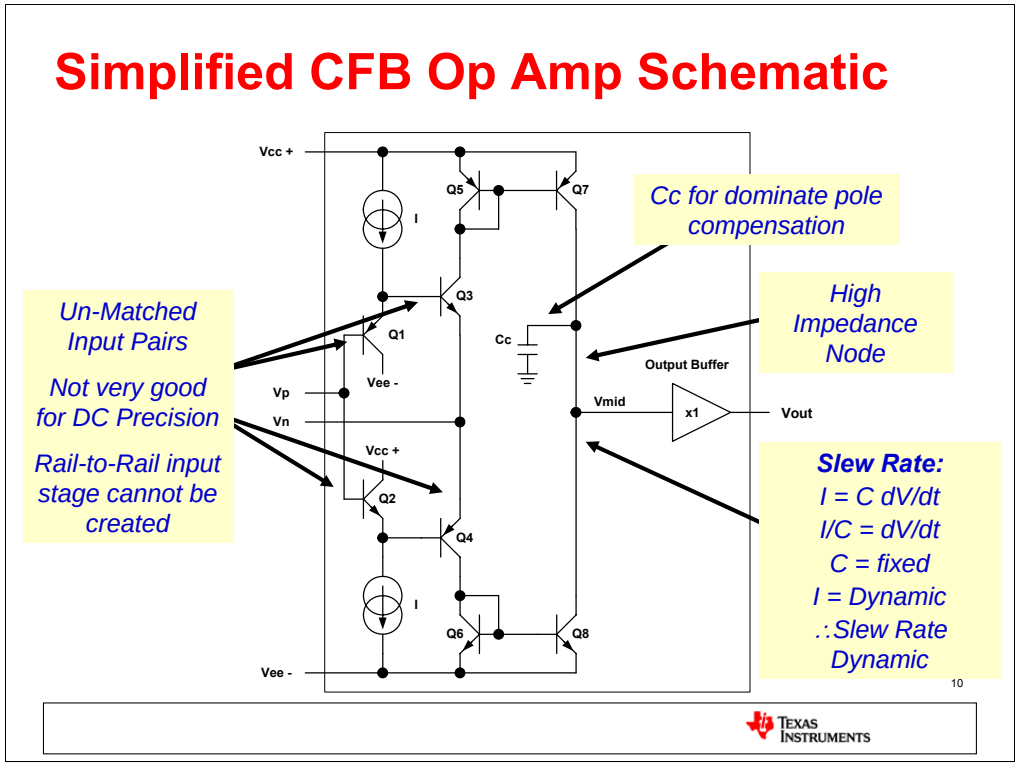


1 Compensation Components

Changing the value of the emitter degeneration resistors, Re, will vary the gm of the input stage. Larger values reduce the gm of the input stage, the open loop gain of the amplifier, and the bandwidth. The thermal noise of the Re resistors also has a direct impact on the input noise of the op amp, where larger values mean more noise.

Adding Cc is called dominant pole compensation. Larger values reduce the pole frequency and the bandwidth of the amplifier. Slew rate (SR) is set by the current I and the capacitor Cc, where SR = I / Cc. So increasing Cc reduces the slew rate

A balance between emitter degeneration and dominant pole compensation is used to compensate the amplifier for the desired performance. The trade offs are noise and slew rate. Unity gain or minimum gain amplifiers can be designed.



1Class AB Input

Q1 through Q4 comprise a class AB amplifier with input Vp and output Vn. The current sources supply current to the stage to bias it into class AB operation.

When Vn = Vp, no current flows from Vp to Vn, the stage sees only the bias current of the current sources, and Q7's current matches Q8's current.

When Vp > Vn, Q3 turns on harder and Q4 starts to turn off causing an offset current in the current mirrors, Q5/Q7 and Q6/Q8.

When Vp < Vn, Q4 turns on harder and Q3 starts to turn off offsetting the mirrors in the opposite direction.

The voltage gain from Vp to Vn is unity. The positive input, Vp, is high impedance, and the negative input, Vn, is low impedance where the input signal (Vp – Vn) produces a current. This is modeled by a unity gain buffer with offset or "error" current out of the inverting input.

Since the positive input, Vp, drives the base of a transistor(s) it is high impedance, whereas the negative input, Vn, drives the emitter of a transistor(s) and is low impedance. Thus the inputs are not well matched and do NOT have good DC precision (higher Vio and drift) and only reasonable low frequency distortion performance.

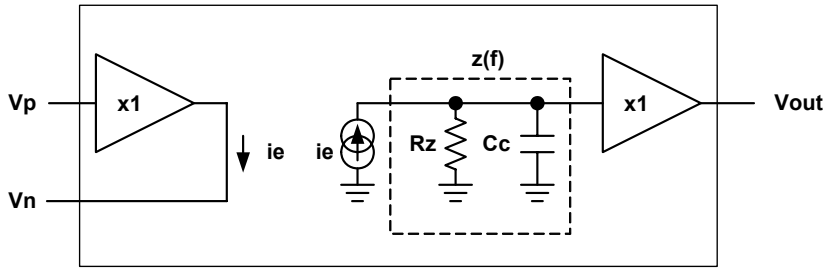
1High Impedance Node

The currents from the mirrors, Q5/Q7 and Q6/Q8, flow into the high impedance node, and develops the output voltage at Vmid.

The high impedance stage is modeled by a parallel impedance, Rz||Cc fed by the offset current from the input stage. Rz models the equivalent dc impedance comprised of the output impedance of the current mirrors. Cc is purposely added by design for compensation. Rz||Cc = Zc or the transimpedance gain.

The maximum slew rate of the amplifier is set by the current, I, the beta of the transistors, the transistor size ratios used in the mirrors, and the value of Cc. So the maximum slew rate can be much higher for a CFB op amp than a VFB op amp for the same quiescent bias current.

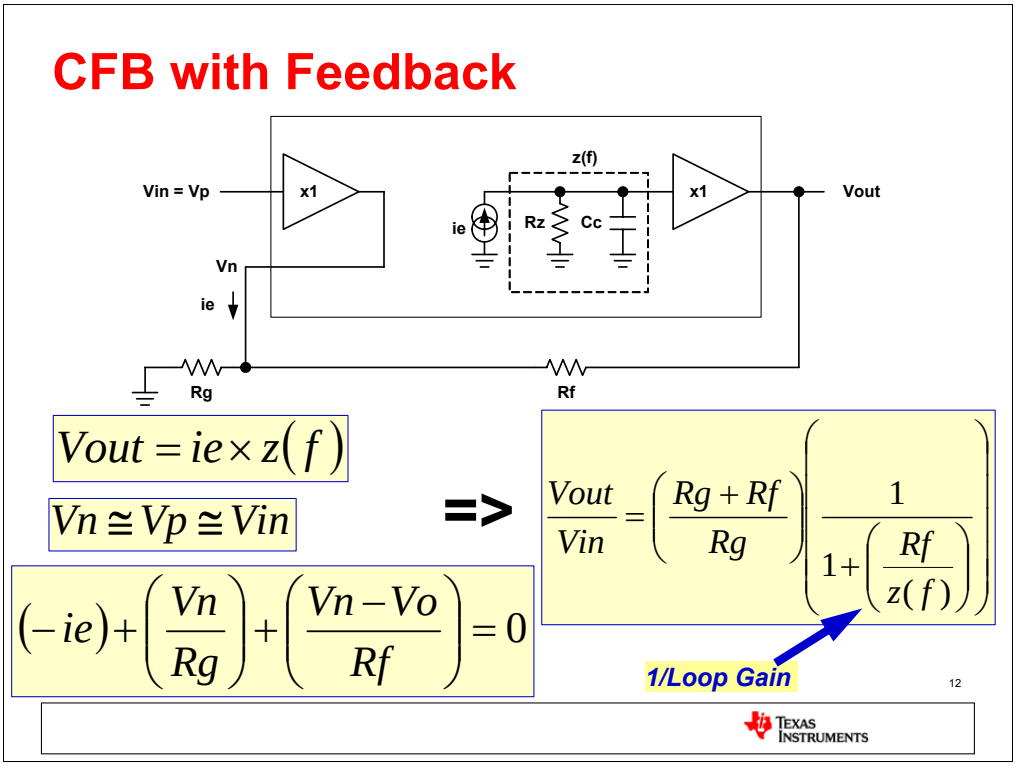
Simplified CFB Model



$$V_{OUT} = i_e \times z(f)$$

Texas Instruments

A useful block diagram can be constructed for a current feedback amplifier as shown above, where the transimpedance gain, z(f), is equal to Rz||Cc. In this model Vout = ie x z(f), where the “error” is ie.

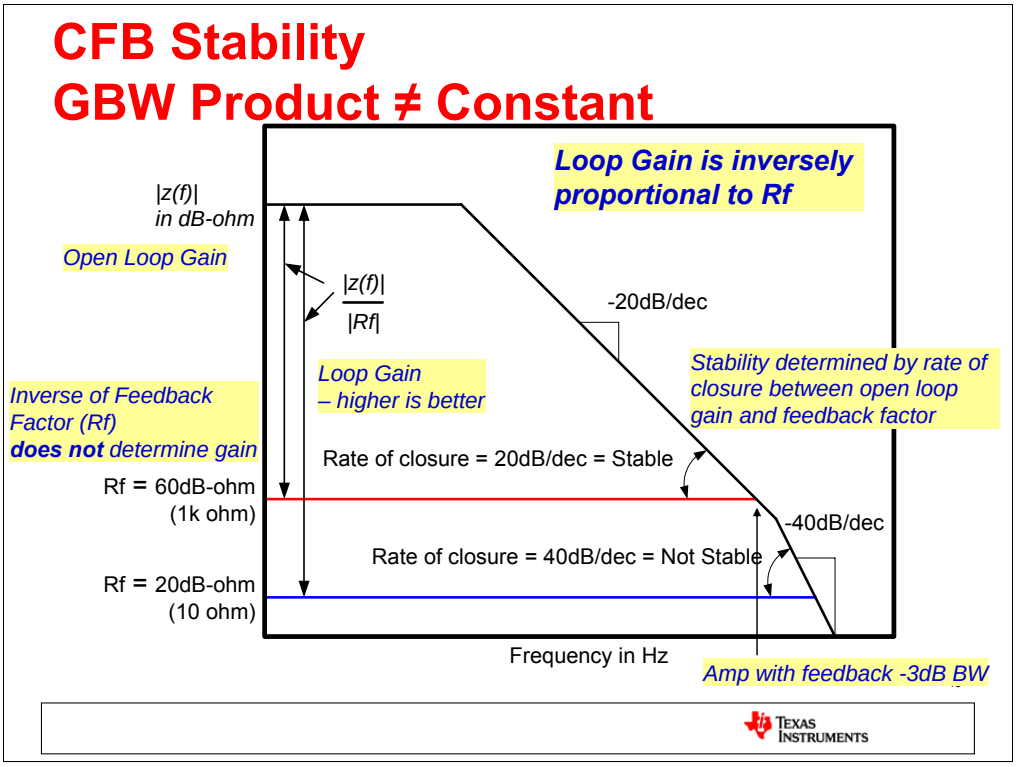


As with a VFB op amp, negative feedback provides a means to set the amplifier gain with stable passive components, and the non-inverting gain can be calculated as shown above. As long as Rf/z(f) << 1, the non inverting gain is set by the resistor ratio 1 + Rf/Rg.

In similar fashion, it can be shown the inverting gain is equal to = -Rf/Rg if Rf/z(f) << 1.

In a CFB op amp 1/Rf is the feedback factor as it transfer function that determines the amount of the output voltage that is fed back as a current to the negative input to null the error current, ie.

Look back at the formula we derived for gain in a VFB op amp and you will see that Rf/z(f) is equivalent to the term a(f)β. In a CFB, z(f)/Rf is the “loop gain” of the op amp as it is the gain around the loop from the negative input to output and back again. As with VFB op amps, it is one of the most critical factors in op amp performance and has special meaning in the context of stability as shown in the following slide.



The diagram shows an op amp that is stable with a feedback resistor, Rf = 1kΩ (60dB-ohm), but is not stable with Rf = 10Ω (20dB-ohm).

Plotting Rf or the inverse of the feedback factor on the plot of z(f) is a good way to visually show the interaction of feedback impedance and stability.

As before:

1. When the slope of the magnitude in dB is -20dB/dec, the phase is -90°
2. When the slope of the magnitude in dB is -40dB/dec, the phase is -180°
3. On a log scale (which a dB scale is), subtracting is the same as dividing the linear numbers
4. The signal is phase shifted -180° going from inverting input to the output

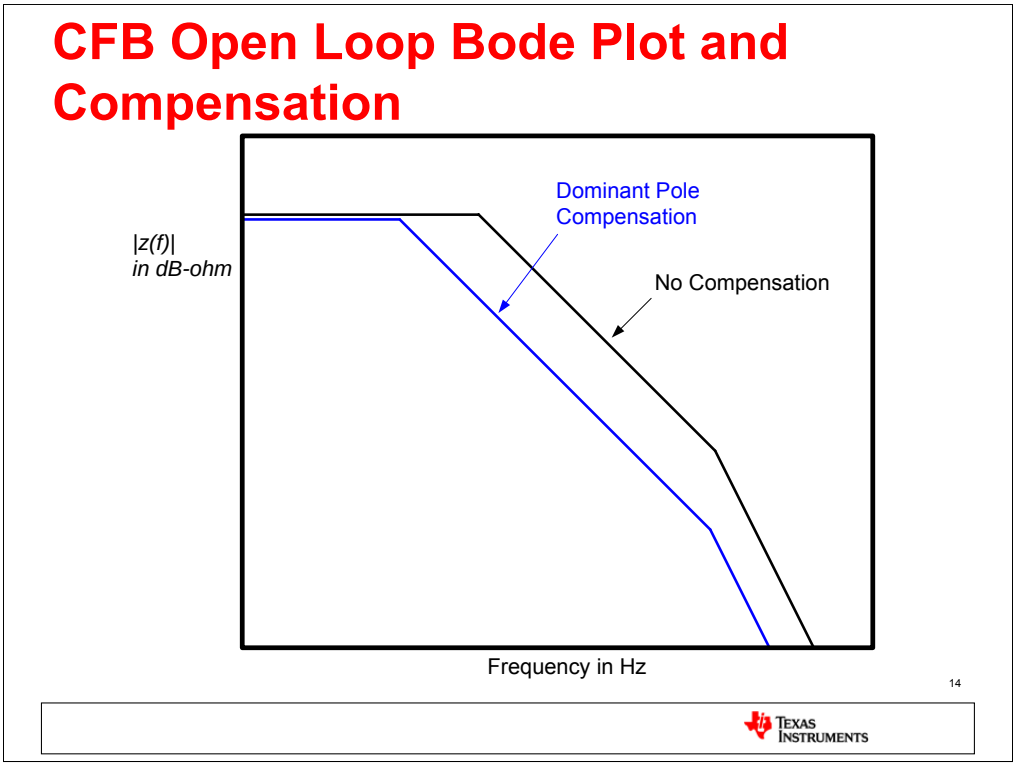
So on this graph, the difference between the Rf and z(f) is |z(f)| - |Rf| = |z(f)/Rf|. When the difference is 0dB (the point where the two lines intersect) the magnitude of the loop gain, z(f)/Rf = 1.

The rate of closure between Rf and z(f) indicates the phase of the loop gain. At 20dB, the phase is -90° and at 40dB it is -180°.

Add the -180° phase shift of the op amp when the closure rate is 40dB, the criteria for oscillation is met i.e. |z(f)/Rf| = 1 and < z(f)/Rf = ±360°. Under this condition the amplifier will spontaneously oscillate. So the amplifier is stable with Rf = 1kΩ, but not with Rf = 10Ω.

Another point to be drawn from the graph is the bandwidth is set by the value of feedback resistor and is independent of gain. The point where Rf and z(f) intersect sets the -3dB bandwidth of the amplifier. You can lower the value of Rg, keeping Rf the same, and get higher gain with the same bandwidth or you can raise the values of both Rg and Rf, keeping the ratio the same, and lower the bandwidth of the amplifier. In essence the gain of a CFB of amp is separated from the open loop transimpedance and stability criteria, and so the bandwidth is separated from the gain.

If you want to think about it too much, you could come up with the fact that a CFB has a constant feedback resistor bandwidth product in the same way a VFB has a constant GBW



1 Compensation Components

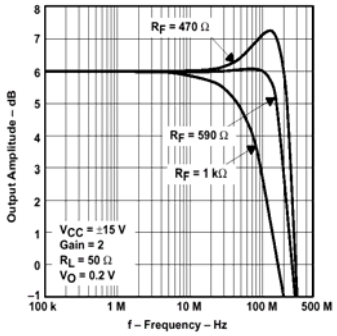
In a CFB op amp there is no emitter degeneration and compensation is controlled with the Cc capacitor only.

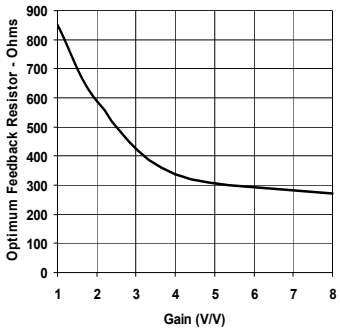
Adding Cc will add a dominant pole that reduces the frequency response and helps compensate the op amp. Larger values reduce the pole frequency and the bandwidth of the amplifier.

Increasing Cc will reduce the slew rate, but also will require a lower value of feedback resistor for stable operation (this is covered on the next slide). A lower value of feedback resistor is desired to reduce the noise developed due to the current noise at the inverting input and the impedance seen at the node.

A balance between feedback resistor value and dominant pole compensation is used to compensate the amplifier for the desired performance. The trade offs are noise and slew rate.

Selecting Feedback Resistor Value for CFB



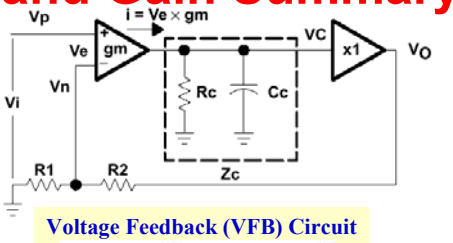


- Current Feedback (CFB) Amplifiers stability is dependant on feedback resistor (RF)
- As RF decreases, Bandwidth increases, but Phase-Margin (stability) decreases
- Increasing the Bandwidth can reduce distortion (increases excess open-loop gain)
- Reducing RF (and RG) reduces overall output noise
- Optimum RF value is different for every amplifier
- Feedback Resistor value can be reduced as gain increases to maximize performance

Reducing the feedback resistor can substantially improve overall performance!

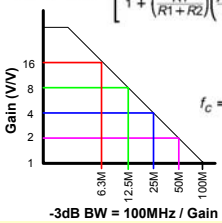
CFB op amps allow you to optimize the loop gain, by selection of the feedback resistor value, based on the closed loop gain of the amplifier. At higher gains, lower feedback resistors can be used without sacrificing stability.

VFB vs CFB Amplifiers – Bandwidth and Gain Summary



Voltage Feedback (VFB) Circuit

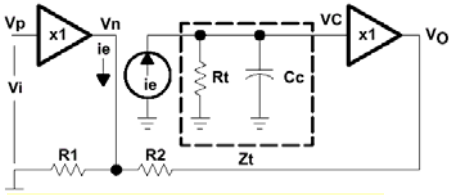
$$\frac{Vo}{Vi} \cong \left(\frac{R1+R2}{R1}\right)\left[\frac{1}{1+\left(\frac{R1}{R1+R2}\right)\left(\frac{j2\pi fCc}{gm}\right)}\right]$$



$$f_c = \left(\frac{gm}{2\pi Cc}\right)\left(\frac{R1}{R1+R2}\right)$$

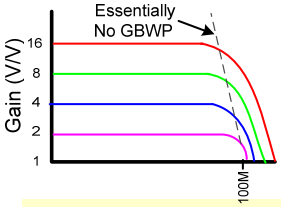
-3dB BW = 100MHz / Gain

Bandwidth is Dictated by gm (fixed by design) and Gain – Hence Gain Bandwidth Product



Current Feedback (CFB) Circuit

$$\frac{Vo}{Vi} \cong \left(\frac{R1+R2}{R1}\right)\left[\frac{1}{1+(j2\pi fR2Cc)}\right]$$



$$f_c = \frac{1}{2\pi R2Cc}$$

Bandwidth is Dictated by R2 (Feedback Resistor)

Texas Instruments

VFB and CFB Amplifiers Have the Same Ideal Gain

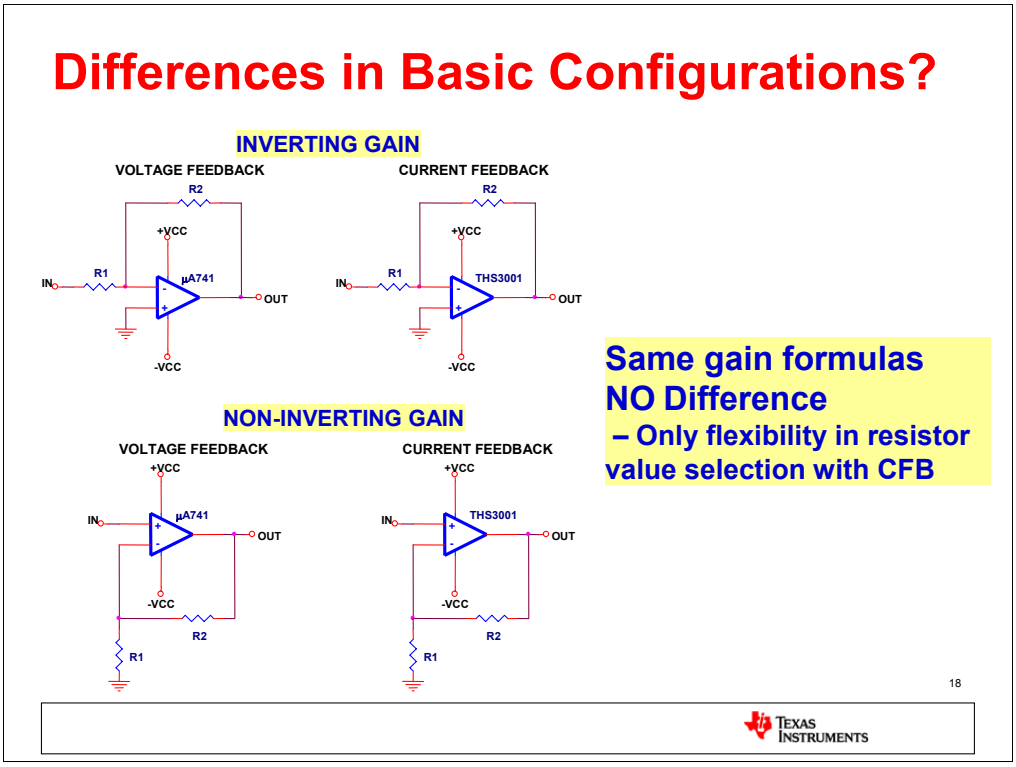
Ideal Gain VFB Amplifier = Ideal Gain CFB Amplifier

Non-Inverting Amplifier

$$Gain = 1 + \frac{R_F}{R_G}$$

Inverting Amplifier

$$Gain = \frac{-R_F}{R_G}$$



In almost every case, you can use a current feedback op amp the same way you would use a voltage feedback amplifier. The only concern is feedback resistor value and stability in CFB amps.

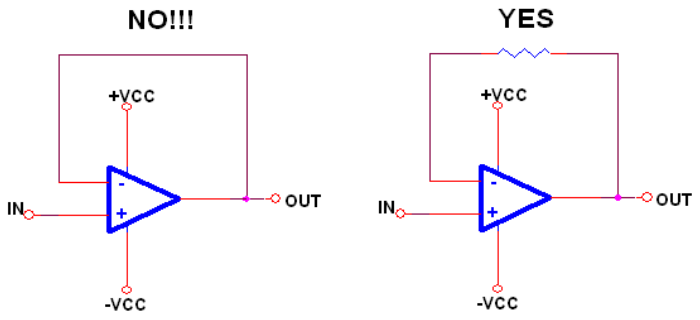
The gain of an inverting stage is –Rf/Rg, and a non-inverting stage is 1+Rf/Rg, but not for just any Rf. It has to be the right one for the amplifier. The correct value for Rf is specified on the data sheet for the part. Voltage Feedback amplifiers allow a lot of flexibility for the choice of the feedback resistor. But, the current feedback amplifiers will have a limited selection as shown in the previous slides. In general, the data sheets will recommend the proper feedback resistor values. Use of these listed values are a great starting point and can be tweaked in accordance with stability / bandwidth trade-offs.

Also keep in mind that the non-inverting input impedance of both VFB and CFB amplifiers is extremely high (>1MOhm) resulting in NO difference in the use of either circuit.

The inverting node input impedance is very low (typically between 10 and 50 ohms) for a CFB amplifier while a VFB amplifier maintains a very high input impedance. BUT, in the closed loop-configuration, there is no difference between these amplifiers when looking at the input impedance from a system standpoint.

Common CFB Application Mistake

A CFB in unity gain must use a resistor for stability

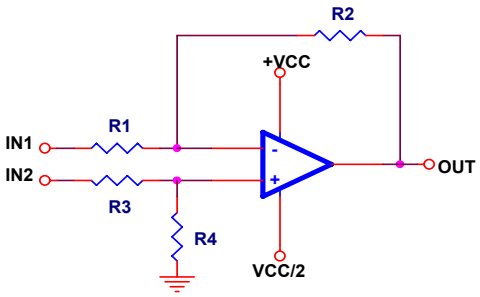


Texas Instruments

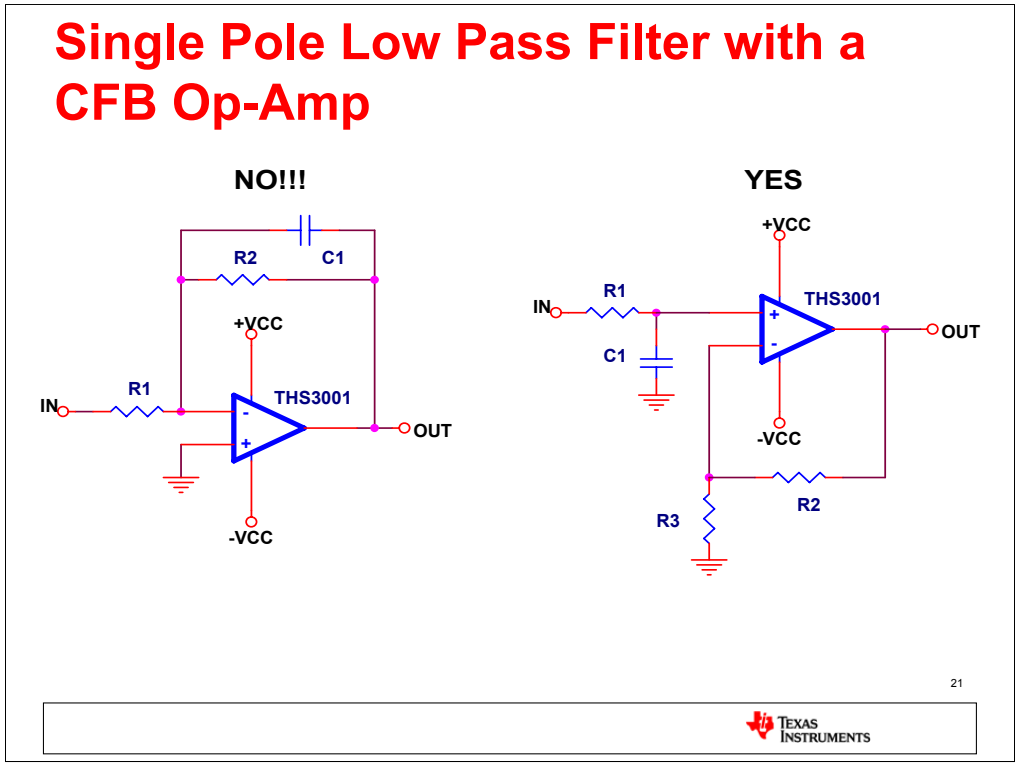
Do *not* use a current-feedback op amp as a traditionally configured unity gain buffer (output connected directly to inverting input)! Correct and incorrect unity gain buffers are shown on the slide. A feedback resistor – value recommended on the data sheet – should always be used as a starting point.

Differences in Basic Configurations?

Difference Amplifier Configuration



Same gain formula NO Difference
– Only flexibility in resistor value selection with CFB



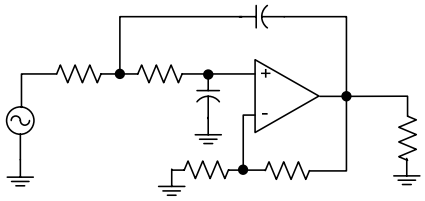
For a majority of cases, you should never use a capacitor in the feedback path. The impedance of this capacitor goes to essentially zero resulting in NO compensation of the amplifier and the result will be an oscillator.

For the advanced designer, there are special tricks that can be done to get around this limitation which allows capacitors to be used in the feedback path to create filters. Basically it is a matter of placing a resistor, inductor, or ferrite chip between the – input node of the amplifier and the “summing” node of the original design. Of course there are trade-offs when this is done such as noise and offsets. But, for some applications this may be acceptable.

See TI Analog Applications Journal 3Q 2003 and 3Q 2004 for more information on this technique.

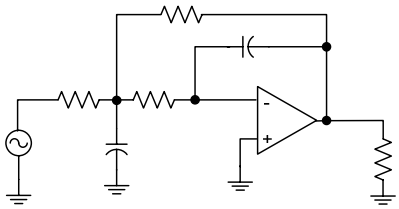
Active Low Pass Filters

Sallen-Key Low-Pass Filter



NO Problem with both VFB and CFB amplifiers

Multiple Feedback (MFB) Low-Pass Filter



Only for use with Unity-Gain Stable VFB amplifiers – slight mods allow use with CFB

22

Texas Instruments

Sallen-Key filters can be used with both CFB and VFB amplifiers with no problems as the negative feedback path has resistors in the path. The feedback resistor value can be chosen independently of the filter component values.

The Mulitple Feedback (MFB) filter has a capacitor between the amplifier output and the inverting summing node. This does NOT allow the use of CFB amplifiers or de-compensated VFB amplifiers. Only unity gain stable VFB amplifiers can be used with this filter. Although a CFB amplifier can be used if the same simple modification to the MFB circuit done in the previous slide is applied to this circuit.

High pass circuits also follow these exact same rules – the Sallen-Key circuit can be used for both amplifiers while the MFB circuit can only be used with unity-gain stable VFB amplifiers and CFB amplifiers with slight modifications.

DC Precision Differences

Differences Dictated Architecturally by Different Input Stages

Voltage Feedback

- Very Low V_{io}
- Low Voltage Drift
- Matched I_b terms (cancellation)
- Low I_{offset} drift

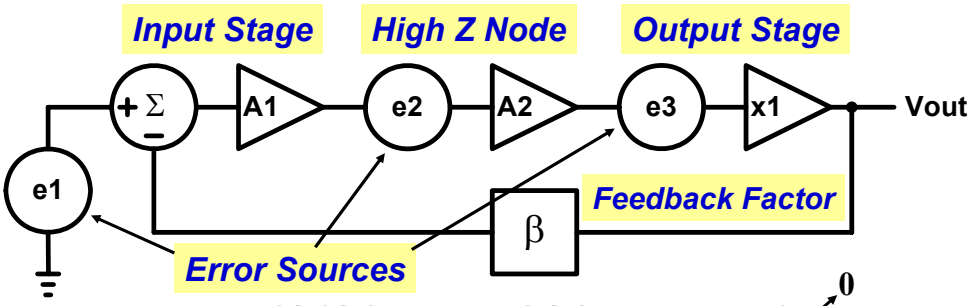
Current Feedback

- Low V_{io} voltage
- Bi-directional voltage drift
- Un-correlated I_b
- No meaningful I_{offset} spec

Texas Instruments

As the beginning of this presentation showed, the input stages of each type of amplifier will dictate the DC precision – aka accuracy – of each amplifier. The VFB amplifier's matched input differential pair consisting of same size transistors and same bias points will allow for better DC accuracy. The CFB amplifier has unmatched transistors operating at different bias points – typically due to NPN and PNP's having different characteristics – resulting in poor DC accuracy.

Distortion and Feedback



$$\text{Vout} = \frac{e1A1A2}{1 + A1A2\beta} + \frac{e2A2}{1 + A1A2\beta} + \frac{e3}{1 + A1A2\beta} \to 0$$

Output stage distortion is reduced by 1+A1A2β

loop gain

Texas Instruments

Total Distortion

Intrinsic Linearity

Total Distortion = +

Reduction in distortion due to loop gain in negative feedback configuration

---

- Loop gain has no effect on noise or distortion in the input stage

VFB and CFB Amplifiers perform better with higher loop gain at the frequency of operation

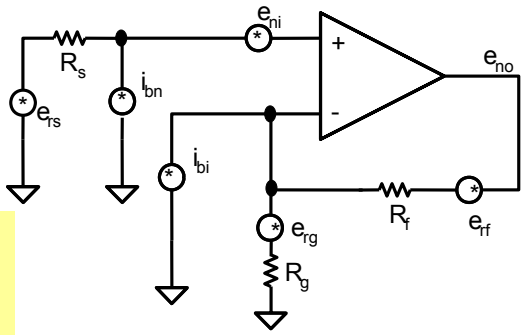
Noise Analysis Differences

$$e_{no}^2 = (e_{rs}NG)^2 + (i_{bn}R_sNG)^2 + (e_{ni}NG)^2 + (i_{bi}R_f)^2 + (e_{rf}^2) + (e_{rg}^2(\frac{R_F}{R_G})^2)$$

$$e_{no}^2 = \left[e_{ni}^2 + (i_{bn}R_s)^2 + 4kTR_s\right]NG^2 + (i_{bi}R_f)^2 + (4kTR_fNG)$$

$$NG = 1 + \frac{R_f}{R_g}$$

4kT=16.4E-21 J @ T = 298° K



VFB Amplifier
Noise dominated by e_{ni}
Typically 1 to 15 nV/√Hz
i_{bn}= i_{bi} Typically 1 to 2pA/√Hz

CFB Amplifier
Noise in low gain dominated by I_{bn}
Typically 12 to 18 pA/√Hz, ibn ≠ ibi
e_{ni} Typically 1 to 3 nV/√Hz

See Application Note AB-103 "Noise Analysis for High Speed Op Amps"

26

Texas Instruments

This is the general analysis circuit for op amp output noise including all noise sources. It is important to remember that the specs in a data sheet do not include the total noise due to the external components. Therefore vendors can mislead one to believe their part is lower noise when in fact they are required to use large resistors possibly giving higher overall noise even if the input voltage noise for the op amp itself is quite low.

Noise can be a very confusing issue. Some points to keep in mind.

The only noise that can be measured is at the output of the amplifier.

Input referred noise is simply the output noise divided by the gain back to the input that you care about - could be the non-inverting input, inverting input, or the input of a prior stage.

Output noise power is made up of the sum of numerous noise contributors. Often, one or two of these are clearly dominant and swamp out all others. This leads to simplified noise equations that drop out terms - leading to much confusion. General equations should include a fairly complete model even if some terms are often (but not necessarily always) negligible.

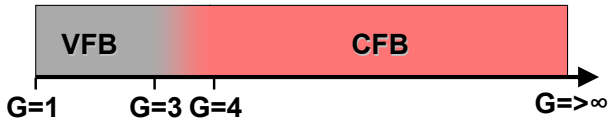
VFB amplifiers are dominated by Voltage noise (Eni)

CFB amplifiers are dominated by current noises, especially the inverting current (ibi) noise when utilized in low gains (<5V/V)

CFB amplifiers can have lower noise than a VFB amplifier when used in high gains – although decompensated VFB amplifiers may result in even better noise performance than a CFB amplifier.

VFB vs. CFB – What to Use and When

- Gain <=3 – VFB is typically better
  - VFB has lower noise in low gains due to low inverting current noise
  - VFB has Gain Bandwidth Product limits to high frequency operation
  - VFB typically has better distortion at lower gains



- Gain =>4 – CFB is typically better
  - CFB has lower noise due to lower Rg resistor value in high gain
  - CFB does not have Gain Bandwidth Product limitation
  - CFB typically has better distortion at higher gains

Caveat: De-compensated VFB amps may be an alternative to CFB at higher gains

27

Texas Instruments

Although there are several attributes that separate a VFB amplifier from a CFB amplifier, there are typically only a few specifications that can be looked at when deciding on what topology is best for a given application. The first specification to look at is gain requirements of the amplifier. There are typically other specifications that go along with gain requirements. All of the key requirements dictate the best amplifier for the socket – not just one. Remember that there are always exceptions to these rules of thumb, but this does give a good starting point.

For gains equal to or less than 3, a VFB amplifier generally makes for a very good choice. One of the biggest reasons for this is the output noise of the amplifier. As other slides have shown, a VFB amplifier output noise is dominated by the voltage noise of the amplifier. Thus, the dominant VFB output noise is equal to voltage noise times the gain. Thus, as long as the gain is low, the overall noise will also be low.

A CFB amplifier output noise is generally dictated by the inverting current noise times the feedback resistance. Although this noise is not multiplied by the amplifier gain at the output, this contribution with low gain is generally the dominate noise component in the amplifier.

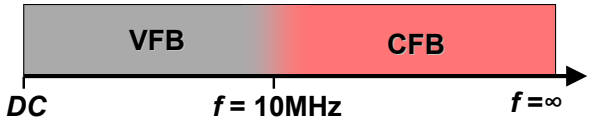
One other aspect of VFB amplifier working at low gains is their loop gain is very large. This will help keep distortion very low.

For amplifier gains greater than or equal to 4, the CFB amplifier is generally a better amplifier. The main reason for this is the feedback resistor is typically reduced as gain increases. This does two things. The first thing it does is to reduce the main noise contributor as the inverting current noise multiplied by the feedback resistor term is decreased. The other thing reducing the feedback resistor accomplishes is it decompensates the CFB amplifier. This results in a the lack of a gain bandwidth product the VFB amplifier has. Thus, high bandwidths are maintained at high gains with a CFB amplifier. Additionally, this decompensation helps maintain the distortion performance even at higher gains.

An alternative to using a CFB amplifier with high gains is to choose a decompensated VFB amplifier. The only limitation is these decompensated VFB amplifiers must maintain a minimum closed loop gain as dictated by their specifications. Failure to do so can easily result in oscillations. But, if the gain requirement is say 15V/V, and a VFB amplifier is desired, then choosing a decompensated VFB amplifier with a minimum gain of 10V/V or 12V/V – such as the THS4021 or OPA847 - would perform very well in the application.

VFB vs. CFB – What to Use and When

- **Frequency of Interest <= 10-MHz**
  - **VFB has better distortion at lower frequency**
  - **VFB can be used for all filters and as integrators**
  - **VFB has Better DC accuracy – Better Vio, Iib, matching, and drifts**



- **Frequency of Interest >10-MHz**
  - **CFB typically has much higher Slew Rates**
    - **Better 3rd-Order Harmonics at higher frequency**
    - **Higher output Voltage Swing is achievable at higher frequencies**
  - **CFB allows higher bandwidth at higher gains**

28

Texas Instruments

The next specification to look at is the frequency of interest. This is not necessarily the bandwidth of the amplifier, but rather the frequency range of the signals that are of most importance. If the frequency of interest is 10-MHz or less, a VFB amplifier is typically a very good choice. Again there are exceptions to this rule of thumb, but it is a good starting point. VFB amplifiers work very well with these frequencies due mainly to the architecture of the amplifier. Additionally any type of filter can be constructed with a VFB amplifier including integrators. Couple this with good input offset voltage, matched input bias currents, and low drift, the VFB amplifier makes for an excellent choice for low frequency operation.

As the frequency of interest increases to over 10-MHz, the CFB amplifier generally makes an excellent choice. The ability to work at high gains and high frequencies is an obvious reason for this. But the other key attribute for the CFB amplifier is the exceptionally large slewrates. Third order harmonics are dominated by slewrate limitations. Thus, the higher the slewrate, the better the third order harmonics tend to be.

Coupled with slewrate is the output swing. Using the formula Vout(peak) = SlewRate / (2 Pi f) one can easily see that at high frequencies, to achieve reasonably large output swings requires significantly large slewrates. Thus, even if a VFB amplifier has a very large bandwidth, if it does not have a large slewrate, the output swing will be severely limited.

VFB vs. CFB – General Application Recommendations

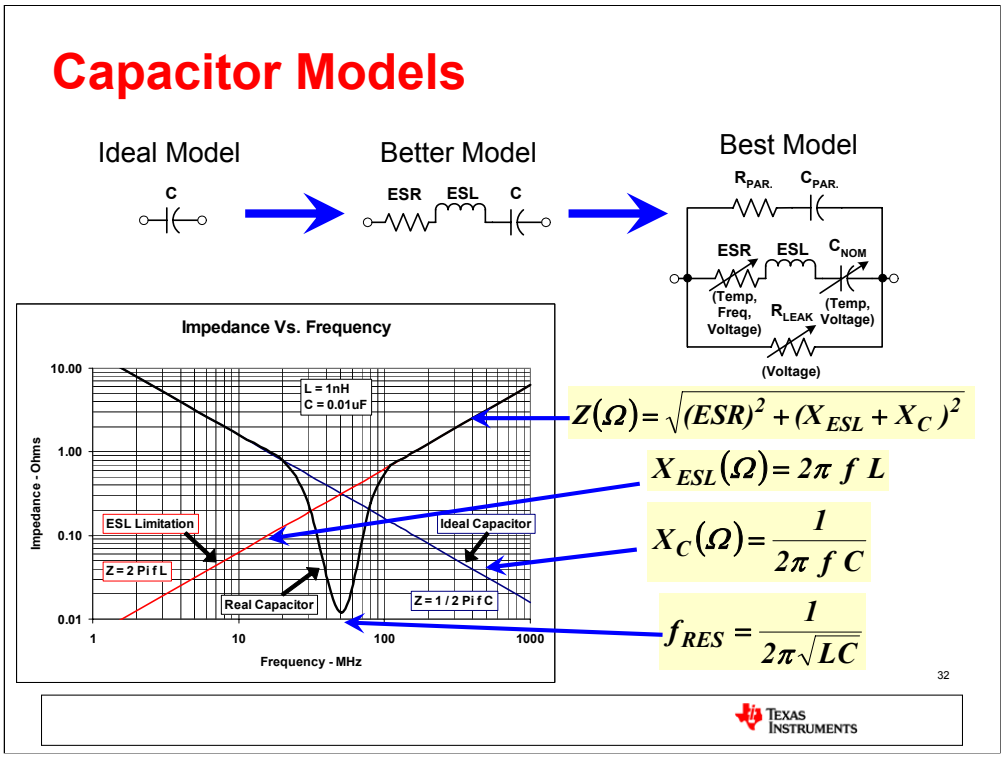
	Low Gain	Low Gain/Low Noise	Low Gain/Low THD	High Gain	High Gain/Low Noise	High Gain/Low THD	DC Precision	Low Frequency	High Frequency	ADC driver	Integrator	Active Filter	Line Driver (e.g. DSL)	Buffer	Pulse Amplifier
VFB	x	x	x				x	x		x	x	x		x	
CFB				x	x	x			x	x		x	x		x

High Speed Layout Considerations

Applies to both VFB and CFB Op Amps

High Speed Layout Key Points

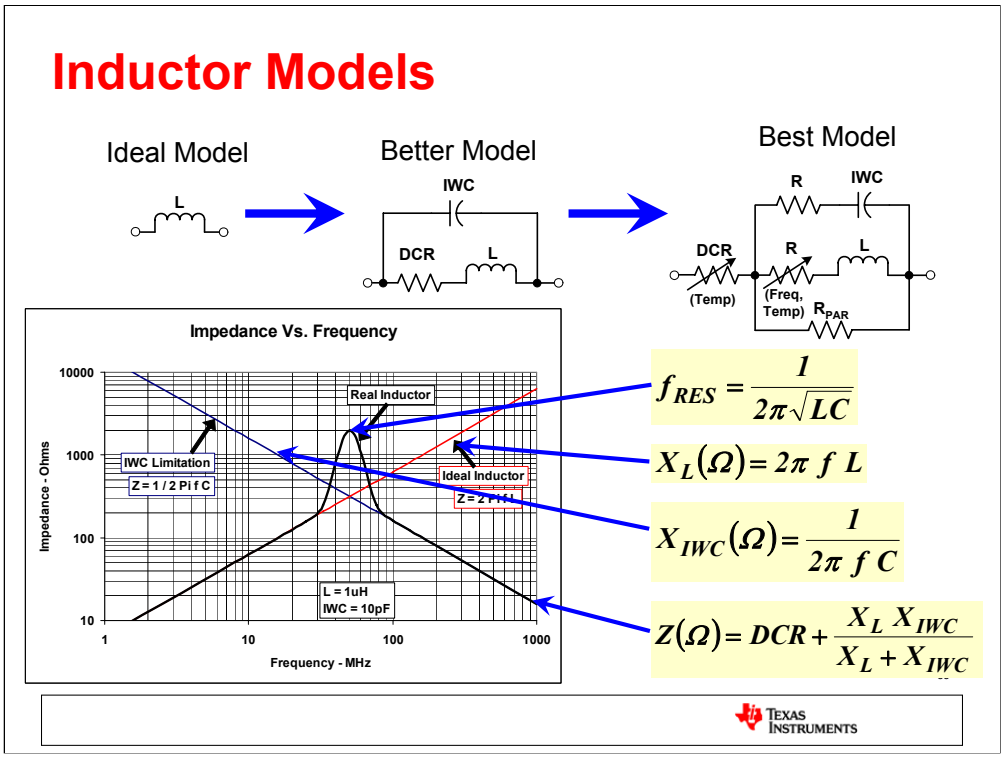
1. Use the right components
2. Layout properly



Capacitors are utilized extensively within most systems. They are used for power-supply bypassing, AC-coupling, integrators, filtering, etc. But, capacitors are not perfect components. They have elements within them that limit their usefulness. The most pronounced elements are the true capacitance, the equivalent series resistance (ESR), and the equivalent series inductance (ESL). It is the ESL which causes the capacitor to stop behaving like a true capacitor at high frequencies as the impedance starts to increase rather than keep decreasing.

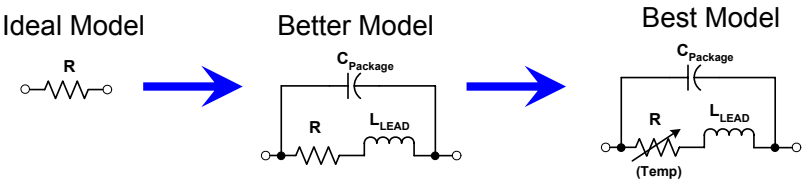
This ESL gets compounded when leaded capacitors are utilized rather than surface mount technology (SMT) capacitors. As the lead inductance increases, the high frequency impedance limitation also increases. This increase is directly proportional to the amount of lead inductance increase. For example, if the lead inductance of the example above increased from 1nH to 4nH by using a leaded ceramic capacitor, the impedance due to ESL increases by a factor of 4. The resonant frequency is also reduced by the square root of the increase, or by a factor of 2 for this example from 50MHz to 25MHz. It should be pretty clear that avoiding the use of any leaded device should be adhered to for high frequency designs.

It should also be noted that when multiple capacitors are placed in parallel, resonances can occur which cause a relatively high impedance to occur. If these resonances occur at the signal frequency or clock frequency, the effect of the capacitor is essentially nullified due to the high impedance at this resonant frequency. Sometimes adding a resistor in series should be done with one of the capacitors to dampen the resonance effect. Additionally, it has been found that sometimes simply removing one of the parallel capacitors actually can improve the system as the resonance is eliminated.



Just as capacitors have other elements within them, inductors also have other elements. This includes the DC resistance (DCR) and the interwinding capacitance (IWC). Just as the capacitor stops behaving like a capacitor at high frequencies, an inductor stops behaving like an inductor at high frequencies. At the transition point the impedance will have a resonance causing a substantial rise in the impedance of the inductor. This resonance can cause issues in some situations and should not be ignored.

Resistor Models



- Using SMT resistors minimizes lead inductance to the point that PCB traces are the limiting factor
- SMT packages also minimize the capacitance between the leads such that this parasitic is usually insignificant
- Note that resistor packs CAN have significant lead inductance and resistor-to-resistor capacitance, so choose wisely based on the application
- Resistors will have temperature coefficients, 200PPM is common, but higher precision is available
- AVOID Wire-wound resistors and leaded resistors for high speed applications due to their large inductance

34

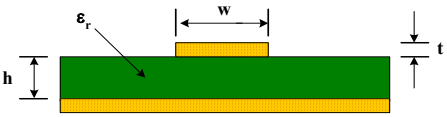
Texas Instruments

Resistors also have elements which make them have a frequency dependence characteristic. The capacitance is usually caused by the resistor package and the PCB mounting pads. The inductance is caused by the resistor leads and the PCB trace length.

In general, these extra elements can be ignored if the resistance value is relatively low – below 1k-ohm for example. But, they cannot be ignored if leaded resistors or wire wound resistors are utilized.

PCB Components

Component: Copper Traces
Purpose: Interconnect two or more points
Problem: Inductance and Capacitance



x = length of trace (cm)
w = width of trace (cm)
h = thickness of board (cm)
t = thickness of trace (cm)
e_r = PCB dielectric constant (FR-4 ≈ 4.5)

$$L(nH) \approx 2x \ ln\left(\frac{5.98\,h}{0.8\,w + t}\right)$$

$$C(pF) \approx \frac{0.264x\ (\varepsilon_r + 1.41)}{ln\left(\frac{5.98\,h}{0.8\,w + t}\right)}$$

$$T_p(ps/cm) = 31.6\sqrt{L(nH)C(pF)}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}}$$

0.8mm (0.031") trace on 0.8mm (0.031") thick PCB (FR-4) has:

≈ 4nH and 0.8pF per cm

≈ 10nH and 2.0pF per inch

35

Texas Instruments

The PCB consists of layers of metal and insulator and can consist of several layers. Examining some common elements of a PCB will help the reader understand what many people believe is "Black Magic".

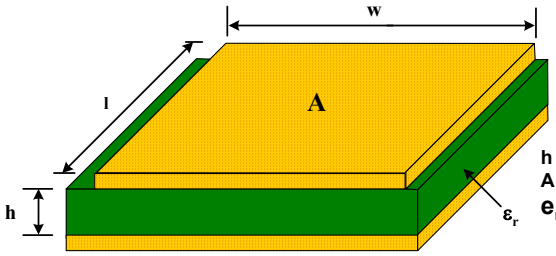
Copper traces are utilized to connect one element node to another node. The shape of these traces determine one very important aspect of a PCB – the characteristic inductance, capacitance, and ultimately the characteristic impedance. Resistance is generally ignored as most designs do not carry more than several mA of current and the results can often be negligible.

Characteristic impedance (Z_0) was covered previously, so this will not be discussed here. But what is important is the inductance and capacitance as determined by the trace dimensions and the PCB dielectric (ε_r). FR-4, probably the most common PCB material used by manufacturers today and has a permeability range normally from 4.0 to 5.0, but 4.5 is often used as a typical permeability. Check with the PCB manufacturer to determine what material they utilize and the associated permeability.

NOTE: Reference the book entitled "High-Speed Digital Design – A Handbook for Black Magic" written by Howard Johnson and Martin Graham, 1993, Prentice-Hall, ISBN 0-13-395724-1.

PCB Components

Component: Copper Planes
Purpose: Used For Ground Planes and Power Planes
Problem: Stray Capacitance on Signal Traces
Benefit: Adds Bypass Capacitance with low Inductance



$$C(pF) \approx \frac{0.0886\ \varepsilon_r\ A}{h}$$

h = separation between planes (cm)
A = area of common planes = l*w (cm²)
ε_r = PCB dielectric constant (FR-4 ≈ 4.5)

0.8mm (0.031") thick PCB (FR-4) has:
≈ 0.5pF per cm²
≈ 32.7pF per inch²

36

Texas Instruments

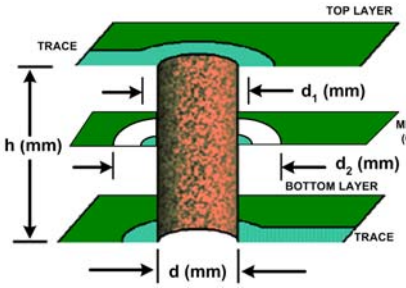
Copper planes are typically found when power planes and ground planes are utilized. Planes make an excellent high frequency capacitor and can often be utilized for high frequency bypassing in complement with traditional capacitors.

The use of a solid ground plane is generally preferred over a grid plane. A solid plane minimizes inductance to the absolute minimum which is a desirable trait for high speed signals – which includes both Analog and Digital signals. But, as will be discussed later, this plane can cause capacitance problems to sensitive nodes of the circuit. Be aware of all attributes of the circuit and do not blindly use planes everywhere.

A side benefit of a solid plane is it becomes a very good thermal conductor and can act as a heat sink to keep thermal levels of all devices minimized. But on the flip side, temperature sensitive components may not want to have the ground plane nearby due to this heat spreading.

PCB Components

Component: Vias
Purpose: Interconnect traces on different layers
Problem: Inductance and Capacitance



$$L(nH) \approx \frac{h}{5}\left[1 + ln\left(\frac{4h}{d}\right)\right]$$

$$C(pF) \approx \frac{0.0555\ \varepsilon_r\ h\ d_1}{d_2 - d_1}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \qquad T_p(ps/cm) = 31.6\sqrt{L(nH)C(pF)}$$

0.4mm (0.0157") via with 1.6mm (0.063") thick PCB has ≈ 1.2nH
1.6mm (0.063") Clearance hole around 0.8mm (0.031") pad on FR-4 has ≈ 0.4pF

e_r = PCB dielectric constant (FR-4 ≈ 4.5)

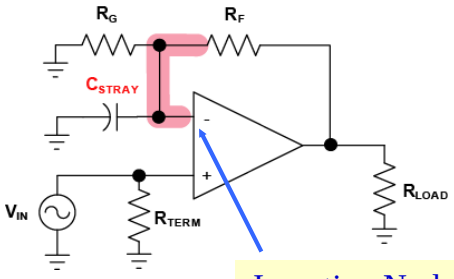
37

Texas Instruments

Vias are utilized to simplify trace routing around other components or when there is a high density of interconnections to be made (i.e. BGA packages). Just as a PCB trace had inductance and capacitance, so to does a via. Generally these elements are ignored as the length of the vias are typically very small relative to the rest of the trace. But, this Can cause issues if the signals are very high frequency (>100MHz) or have energy / harmonics at high frequencies.

The easiest way to minimize problems of a via is to simply not use them with signal traces. At the very least it should be minimized. If vias must be used, there are other issues to worry about that will be discussed later.

(-) Input Capacitance



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(1 + 2\pi C_{STRAY} R_G\right)$$

$$f_{ZERO} = \frac{R_F + R_G}{2\pi C_{STRAY} R_F R_G}$$

- Inverting node (-) of an op amp is sensitive to stray capacitance (C_{STRAY})
- R_F,R_G and C_{STRAY} create a zero to in the feedback which can lead to instability
- As Little as 1pF of C_{STRAY} can cause stability problems
- Node includes the entire trace up to the placement of R_F, R_G, and any other component on the inverting node

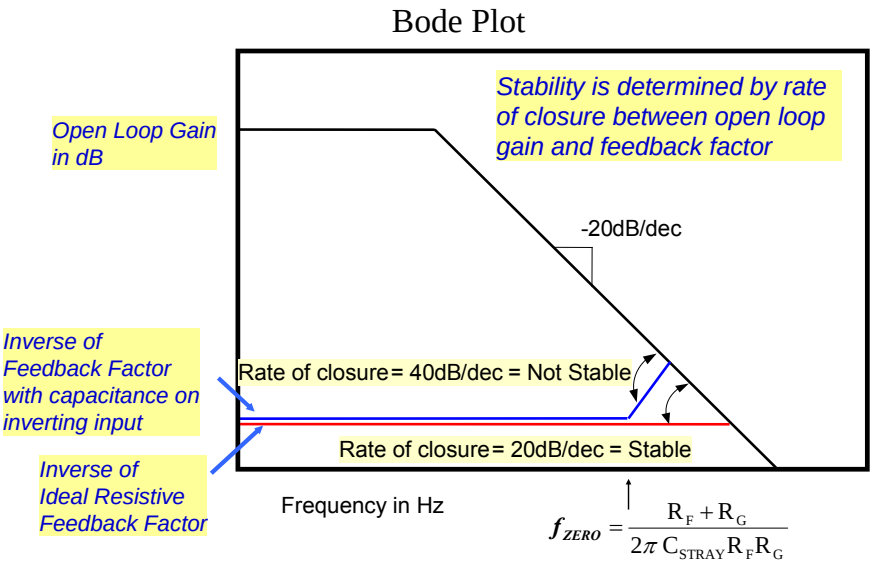
38

Texas Instruments

As discussed, having stray capacitance at the wrong place can cause serious concerns. Having stray capacitance at the inverting node of an amplifier is one of those places. The stray capacitance causes a zero in the transfer function. If the zero intersects the amplifier's open-loop response at a 40-dB/decade rate of closure, this will cause the amplifier to be unstable and it will oscillate. Having as little as 1-pF can cause problems with the system.

Remember that the inverting input node includes everything connected to it up to the point there is some resistance or impedance of reasonable value (ie. >50-ohms).

(-) Input Capacitance is Bad

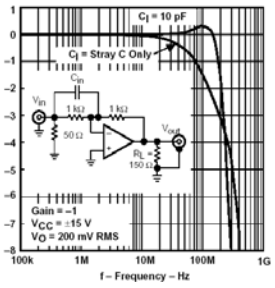


The diagram shows an op amp that is stable with pure resistive feedback, but is not stable with capacitance added at the negative input with zero causing rate of closer greater than 20dB/dec.

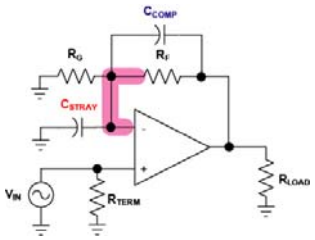
Minimizing Stray C at (-) Input

Solutions:

1. **Eliminate Ground Planes and Power Planes under and near the inverting input (-)**
2. **Shorten trace by moving components closer to the inverting input (-)**
3. **Reduce R_F and R_G values**
4. **Increase Gain of System**
5. **Use Inverting Configuration Place Compensation Capacitor Across R_F**



Inverting Mode



Compensation

$$C_{COMP} = \frac{R_G}{R_F} C_{STRAY}$$

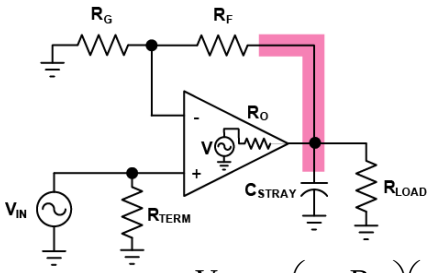
Texas Instruments

There are several ways to minimize the effects of stray capacitance at the inverting input node of an amplifier. These are illustrated above.

The fundamental task at hand to make the amplifier stable once again is to reduce the intersection point of the noise gain and the open-loop response to as close to a 20-dB/decade rate of closure as possible. Even if this is close, this should be sufficient to create a stable system.

For more information on some of these techniques, refer to the TI Application Report entitled “Effect of Parasitic Capacitance in Op Amp Circuits”, SLOA013.

Output Capacitance



$$f_{POLE} \approx \frac{1}{2\pi C_{STRAY} R_O}$$

Assuming:

$R_O << R_F, R_{LOAD}$

$$\frac{V_{OUT}}{V_{IN}} = \left(1+\frac{R_F}{R_G}\right)\left(1+\frac{R_O}{R_F+R_G}+\frac{R_O}{R_{LOAD}}+2\pi C_{STRAY} R_O\right)$$

- **Op amps are sensitive to capacitance on output (C_{STRAY})**
- **Real op amps have output Impedance (R_O)**
- **R_O and C_{STRAY} create a pole to in the open loop gain which can lead to instability**

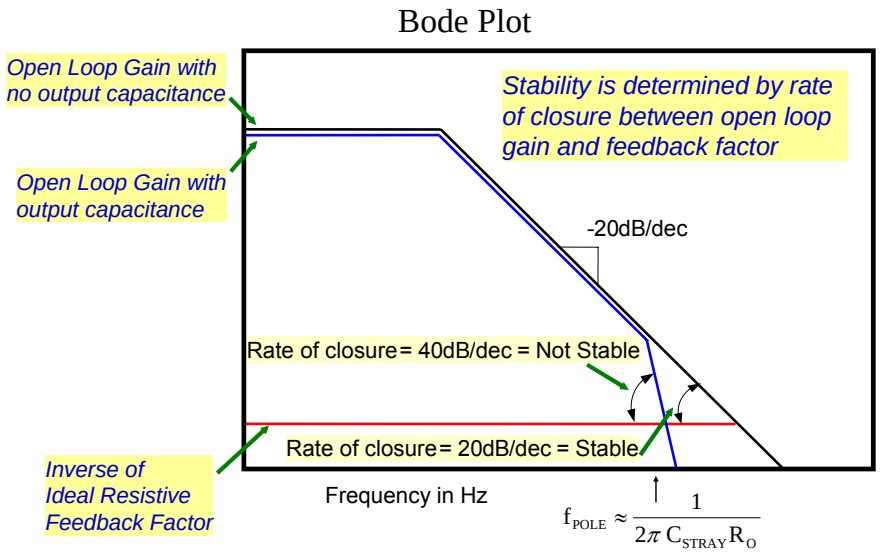
41

Texas Instruments

Stray capacitance at the output of high speed amplifier can also cause the amplifier to become unstable. This is caused by the pole formed by the amplifier's internal resistance and the capacitive loading. This RC network causes excess phase shift in the loop gain of the amplifier.

Just like the stray capacitance at the inverting input node, stability is dictated by the noise gain of the amplifier intersecting the open-loop gain and should be as close as possible to the 20-dB/decade rate of closure as possible.

Output Capacitance is Bad

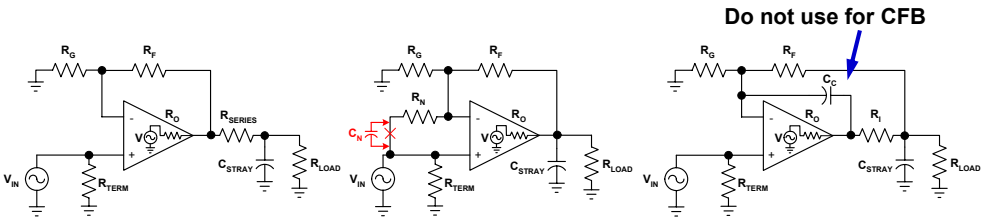


The diagram shows an op amp that is stable with pure resistive feedback and no output capacitance, but is not stable with capacitance added at the output causing rate of closer greater than 20dB/dec.

Minimizing Effects of C at Output

Solutions:

1. **Eliminate Ground Planes and Power Planes under output node**
2. **Use series output resistor**
3. **Shorten traces by moving components closer to output pin – especially Series Matching R**
4. **Increase Noise Gain of System (i.e. decrease feedback factor)**
5. **Use Feedback Compensation**



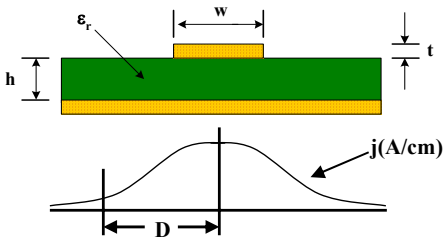
Adding Series R for Isolation **Increasing Noise Gain Only** **Feedback Compensation**

Texas Instruments

Solving the stability of the amplifier with a capacitive load can be relatively simple. Most common ways are to isolate the capacitive load by some real resistance. Another way to make the amplifier stable is to increase the gain of the amplifier, or increasing the noise gain of the amplifier, which both attempt to reduce the rate of closure to the 20-dB/decade goal for stability.

Current Density

$$j(A/cm) = \frac{I_o}{\pi \, h} \times \frac{1}{1 + \left(\frac{D}{h}\right)^2}$$



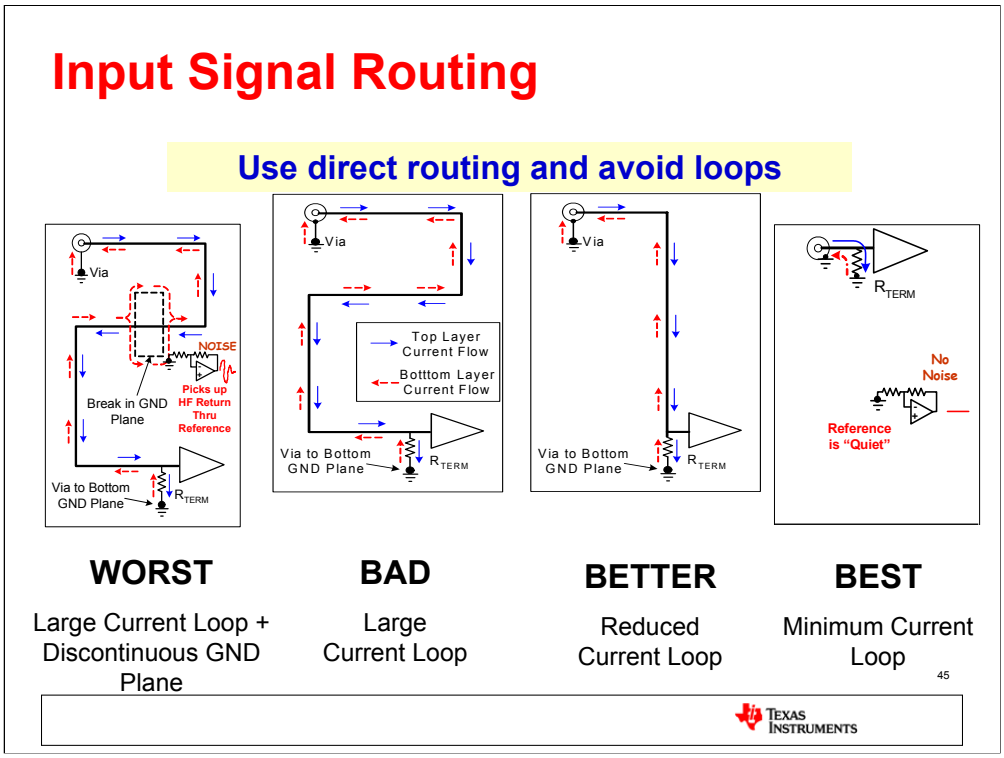
I_o = total signal current (A)
h = PCB thickness (cm)
D = distance from center of trace (cm)

- Illustrates Return Current Flow is directly below the signal trace. The creates the path of least impedance.
- Must have Solid return path (i.e. Solid Ground Plane) under the signal trace to maintain homogeneous nature of current density.

Texas Instruments

Current density is the concentration of current flowing through a conductor. This is especially important when looking at return currents.

One thing that many people forget about is for a current to flow out to a point, there MUST be a return path or else current will Not flow. Since there is a current flow, then the return current flow will find a way back to its' source one way or another. Return current density is highest directly under (or over) the signal trace it was sourced from. Even if a solid ground plane is used, the concentration of current flow will still be adjacent to the signal source trace.



As just discussed, the lowest impedance path of a high speed signal is directly under a PCB trace. This minimizes the current loop area substantially. The “worst” case scenario shows a long winding trace creates a large current loop area which is made even worse by the break in the ground plane. The obvious issue with this is the ground plane is often used as a reference point for other parts of the system. If the current flow density is high near one of these reference points, this can (and often does) cause noise to occur in the circuit and often propagates throughout the entire signal flow.

As the bad layout shows, also shows a long winding trace that does not follow the “shortest distance between two points is a straight line” method. The better layout minimizes the distance while reducing the current loop area. But, the best way to do the layout is to place the receiver part as close as possible to the input. This easily is the smallest loop area and delays in the signal path are drastically reduced. A key benefit of this method is the reference ground point for other circuits are kept “quiet” and should have no contribution from the undesirable current flow.

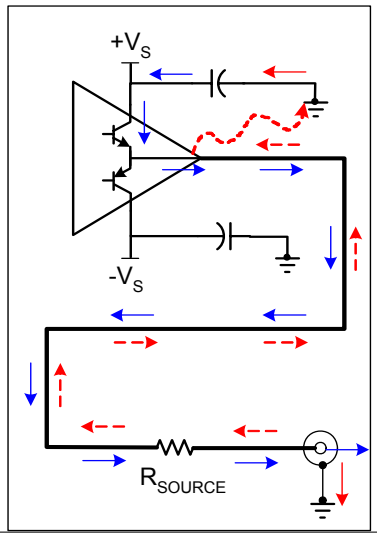
This also minimizes the need for adhering to strict strip-line techniques as the signal path acts as a lumped circuit and not a distributed circuit. A lumped circuit typically has rising edges much less than the delay time of the transmission line, thus minimizing issues. The construction of transmission lines naturally keeps the source and return currents close to each other. This helps minimize current loop area and drastically reduces noise along the path on the PCB and also EMI.

Output Signal Routing

Use direct routing and avoid loops

Problems:

1. **Long winding path causing large current loop area.**
2. **HF bypass caps are placed too far away from amplifier and GND. Inductance eliminates benefit of bypass caps.**
3. **GND of bypass caps are too far away from amplifier output.**
4. **Series Resistor (RSOURCE) is too far away from the amplifier. Causes C-loading on amplifier and lack of a transmission line.**
5. **Single GND point on connector**



46

Texas Instruments

Looking at the Output current path shows the exact same phenomenon as the input current flow – the return current path will follow the signal trace path wherever it may go. One issue that is often overlooked is where does this return current flow once it reaches the output of the driver? As we all know, current must close the loop or else there is no current flow.

In the example above, the return current flows through the bypass capacitors and back into the power supply lines. Now we see that the bypass capacitors are part of the loop and will have impact on the performance of the system. Obviously it makes sense to place the capacitors as close as possible to the driver power supply pins and the actual output trace.

Another issue with the above system is the source resistance is very far away from the driver. As will be discussed later, this is a bad thing for the driver and may cause stability problems. Additionally, the transmission line typically starts at the load side of the resistor. This system may have a undefined characteristic impedance that may cause reflection concerns.

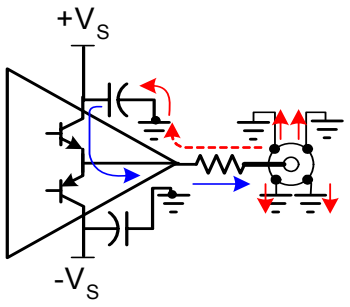
The last concern is the single ground connection point of the connector. This may cause a significant impedance mismatch in the return current flow.

Output Signal Routing

Use direct routing and avoid loops

Solutions:

1. **Amplifier is next to Connector minimizing loop area.**
2. **HF bypass caps are now placed next to amplifier power supply pins and has short GND connection.**
3. **GND of bypass caps near amplifier output – but not too close to cause C-loading issues.**
4. **Source Resistance is next to amplifier output.**
5. **Multiple GND points on connector.**

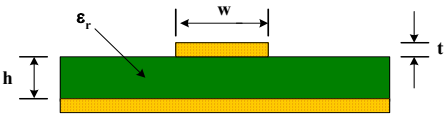


Texas Instruments

As seen before, the simple solution is to simply minimize the current flow area as much as possible. Easily solved by moving the connector and the driver next to each other. The bypass caps are now very close to the driver power supply pins and have very short trace lengths that are near the driver output pin. The series resistor that matches the transmission line characteristic impedance is placed very close to the driver. Additionally the connector has multiple ground connection points to minimize impedance issues.

Input and Output Trace Impedance

Match impedance of input transmission line
Match impedance of output transmission line



x = length of trace (cm)
w = width of trace (cm)
h = height of trace (cm)
t = thickness of trace (cm)
e_r = PCB Permeability (FR-4 ≈ 4.5)

$$L(nH) \approx 2x \ ln\left(\frac{5.98\,h}{0.8\,w + t}\right)$$

$$C(pF) \approx \frac{0.264x\ (\varepsilon_r + 1.41)}{ln\left(\frac{5.98\,h}{0.8\,w + t}\right)}$$

$$T_p(ps/cm) = 31.6\sqrt{L(nH)C(pF)}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}}$$

0.8mm (0.031") trace on 0.8mm (0.031") thick PCB (FR-4) has:

≈ 4nH and 0.8pF per cm

≈ 10nH and 2.0pF per inch

48

Texas Instruments

The PCB consists of layers of metal and insulator and can consist of several layers. Examining some common elements of a PCB will help the reader understand what many people believe is "Black Magic".

Copper traces are utilized to connect one element node to another node. The shape of these traces determine one very important aspect of a PCB – the characteristic inductance, capacitance, and ultimately the characteristic impedance. Resistance is generally ignored as most designs do not carry more than several mA of current and the results can often be negligible.

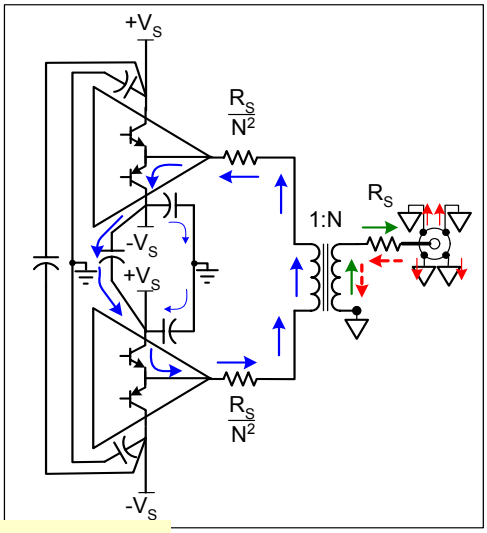
Characteristic impedance (Z_0) was covered previously, so this will not be discussed here. But what is important is the inductance and capacitance as determined by the trace dimensions and the PCB dielectric (ε_r). FR-4, probably the most common PCB material used by manufacturers today and has a permeability range normally from 4.0 to 5.0, but 4.5 is often used as a typical permeability. Check with the PCB manufacturer to determine what material they utilize and the associated permeability.

NOTE: Reference the book entitled "High-Speed Digital Design – A Handbook for Black Magic" written by Howard Johnson and Martin Graham, 1993, Prentice-Hall, ISBN 0-13-395724-1.

Differential Output Signal Routing From 2 Amplifiers

Guidelines

1. **Minimize Loop Area on Driver Side.**
2. **Utilize a single Capacitor between opposite amplifier supplies as this should be the main current flow. Adding this Capacitor can reduce 2nd-Order Distortion by 6 to 10dB!**
3. **Use bypass caps to GND at a mid-point to handle stray-C return path currents but do not disrupt differential current flow.**



Use direct routing and avoid loops

49

Texas Instruments

Using two individual amplifiers in a differential drive configuration, such as a ADSL line driver, also must follow the same concepts discussed previously. The use of a transformer helps isolate the driver-side current flow and the line side current flow. Since the drivers' outputs are differential, there must be a differential current flow from one driver to the other. The bypass capacitors allow this to occur and should follow the concepts previously discussed. The only difference here is we want to force the current to flow through a bypass capacitor connected from the positive supply of one driver to the negative supply of the other driver.

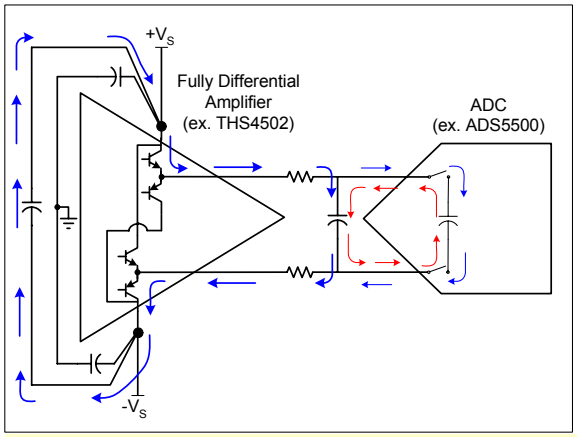
The use of bypass capacitors to the ground plane will still be required, as will be discussed later. To make sure the current does NOT flow into the ground, place these capacitors symmetrically to each other and connect the ground at the midpoint of the capacitors. The differential current flow should have no reason to go into the ground plane. Combined with the single capacitor across the supplies, this configuration can reduce even-order harmonics by 6 to 12dB.

Although not shown above, there will be interwinding capacitance across the transformer windings. There must be a way for high frequency current flowing through this capacitance to return back to the source, or else there can be issues.

Differential Output Signal Routing From FDA

Guidelines

1. **Minimize Loop Area on Driver Side.**
2. **Utilize a single Capacitor between opposite amplifier supplies as this should be the main current flow.**
3. **Use bypass caps to GND at a mid-point to handle stray-C return path currents but do not disrupt differential current flow.**
4. **Filter Cap should allow for small Loop Areas – including "kick-back" current flow.**



Use direct routing and avoid loops

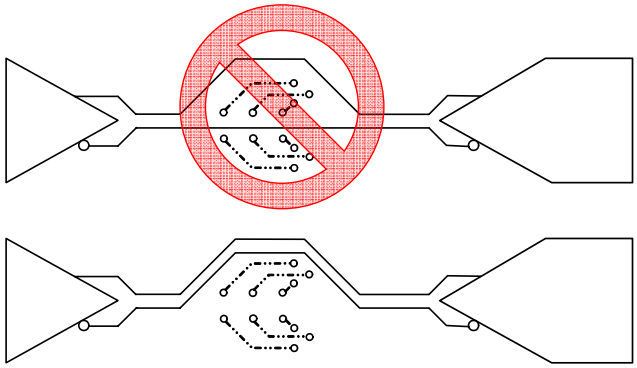
50

Texas Instruments

A fully differential amplifier follows essentially the same concepts as the single-ended differential driver. The only difference is the two outputs are in the same package. But, the bypass capacitors should follow the same principles as mentioned before – one capacitor form the positive supply to the negative supple, and the two bypass capacitors to ground should optimally be placed symmetrically to each other and connected to ground at the midpoint.

One of the most common uses for a fully differential amplifier is to drive an ADC. When doing this, pay attention to the current flows around the amplifier and the ADC (caused by the ADC's internal capacitor). Keep the paths as symmetrical as possible.

Routing Differential Traces



- Keep differential traces close together to keep noise injection as a Common-Mode signal which is rejected differentially
- Route differential traces around obstacles together, or move obstacle
- Keep trace lengths the exact same length to keep delays equal

51

Texas Instruments

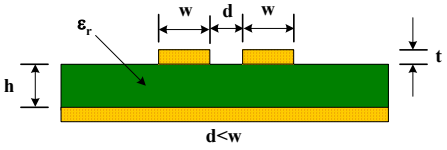
When routing differential traces, they should always be routed together (side-by-side). This keeps any noise injection into the signal a true common-mode noise which gets rejected by the receiver. If noise only gets into one channel and not the other, the amount of rejection is minimal at best.

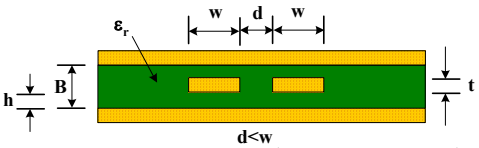
Additionally, the lengths of both traces should be kept the same length. Otherwise the signals can arrive at the receiver at different times and cause performance issues. This is especially true for very fast switching digital signals and very high analog signals (>1-GHz).

Impedance of Differential Traces

MICROSTRIP
- Most Commonly Used
- Less Propagation Delay
- May Radiate more RF
- Only requires 2 Layers

STRIPLINE
- More Propagation Delay
- Better Noise Immunity/Radiation
- Requires at least 3 Layers
- May be harder to control Z_0





$$Z_{diff}(\Omega) \approx 2 * Z_0\left(1 - 0.48e^{-\frac{0.96d}{h}}\right)$$

$$Z_{diff}(\Omega) \approx 2 * Z_0\left(1 - 0.347e^{-\frac{2.9d}{B}}\right)$$

$$Z_0(\Omega) \approx \frac{60}{\sqrt{0.475\,\varepsilon_r + 0.67}} \ln\left(\frac{4\,h}{0.67(0.8w + t)}\right)$$

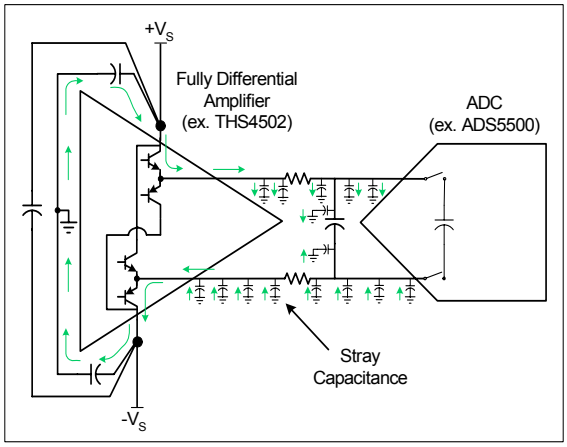
$$Z_0(\Omega) \approx \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4\,h}{0.67\pi(0.8w + 1)}\right)$$

Texas Instruments

Just like single traces, differential traces also can have a characteristic impedance dictated by the inductance and capacitance. Keeping the differential traces close together is highly desirable as it minimizes noise injection problems and minimizes the radiated electromagnetic field.

Why Use Bypass Capacitors?

1. **Allows Common-Mode Return Currents a path back to the source to complete the loop**
2. **Preserves Differential Current Flow – use mid-point grounding**
3. **Some of these currents will flow back into the opposite phased signal path through the stray capacitance**



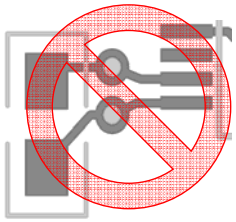
Remember: Minimize ALL Current Loops – Differential AND Common-Mode

Texas Instruments

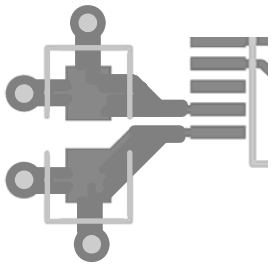
Adding capacitors to ground, even in a fully differential system, needs to be done to account for the current flowing through the stray capacitance of the system. This stray capacitance can even occur inside the silicon of the driver and/or the ADC. As you know by now, the current will find a way back to its' source in-order to complete the loop. The bypass capacitors to ground allow this current flow to occur and will minimize the loop area.

Bypass Capacitor Routing

- DO NOT have vias between bypass caps and active device – Visualize the high frequency current flow !!!
- Ensure Bypass caps are on same layer as active component for best results.
- Route vias into the bypass caps and then into the active component.
- The more vias the better.
- The wider the traces the better.
- The closer the better (<0.5cm, <0.2")
- Length to Width should not exceed 3:1



Poor Bypassing



Good Bypassing

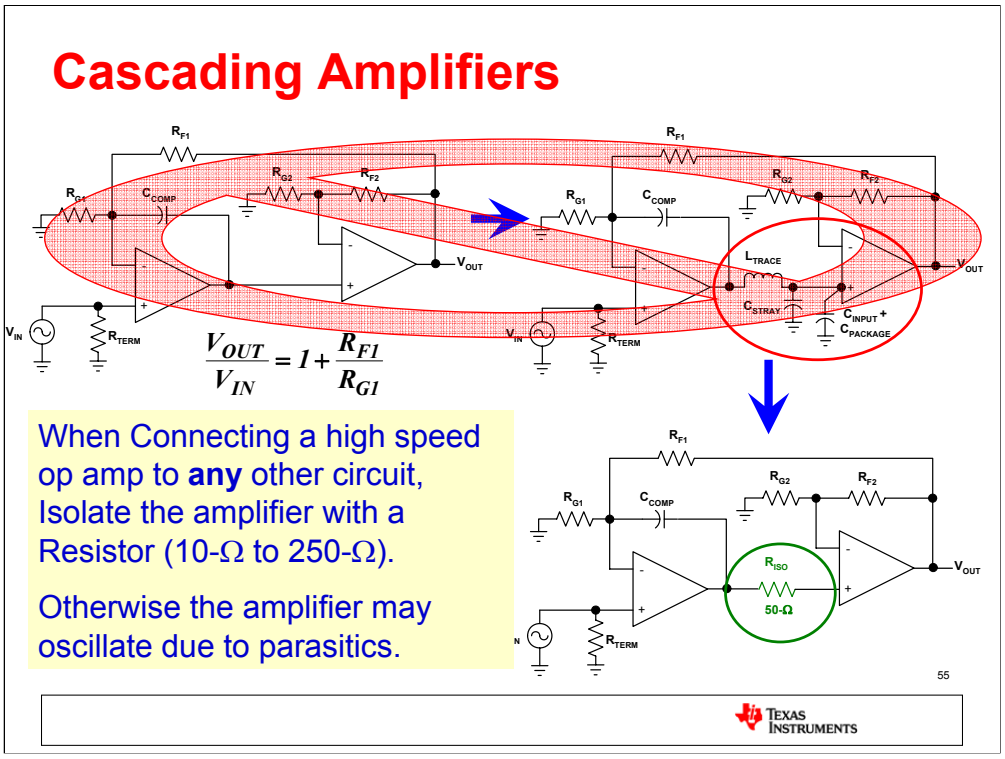
54

Texas Instruments

Now that the characteristics of a capacitor are known and the proper one has been selected, the next thing to do is place it on the PCB. For bypass capacitors this can be a concern if done without taking time to think about the high frequency implications of routing. The rule of thumb of placing capacitors as close as possible to the IC power input pins should be adhered to. Otherwise there can be too much inductance and a resonance effect can take place along with the straight forward impedance increase due to the inductance.

Typically the power and ground are on inner layers of the PCB and must be brought up to the IC level by vias. As we have learned, the more vias utilized, the lower the impedance. So using multiple vias is highly recommended for BOTH power supply voltage connection and Ground connection.

Additionally, the vias should run into the capacitor and then into the IC. This forces the current flow into the capacitor. Placing vias directly on the capacitor mounting pads can be an effective way to minimize routing area and still achieve the current flow routing.



Sometimes high-speed amplifiers need a series input resistor, because package parasitics become more and more apparent at higher signal frequencies. Package parasitics are mainly due to the leadframe pins, bondwire and the IC die itself. The pins and bondwire can be modeled as high frequency inductors, with small capacitors between each. The die adds parasitic capacitance from the bondpad on the die to the die substrate.

All together, these parasitics can form resonant circuits, with high Q values and resonant frequencies in the hundreds of MHz. Most problems that are created by these parasitics occur at the high impedance input of the IC. Even if the overall bandwidth of the IC is much less than the resonant frequency, the transistors in the input stage can still be affected.

An indication of problems associated with the parasitics is higher than expected gain peaking of the amplifier. A series input resistor will help prevent excessive gain peaking problems or even oscillation by dampening the parasitic LC circuit. Typical values for this resistor are between 10Ω to 250Ω. The value can vary widely because of different PC-board parasitics that will add to this problem.

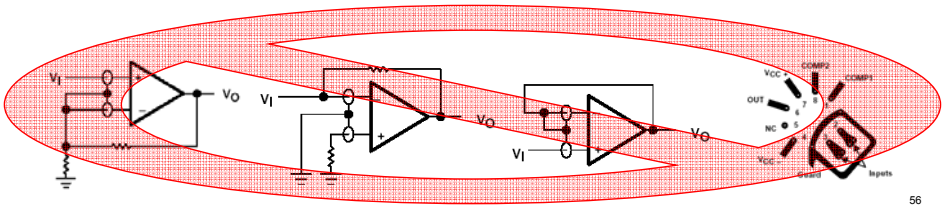
One rule, however, exists: the smaller the package the less its parasitics and the smaller the associated effects. Therefore, designers should choose SOIC (or smaller) packages over DIP packages whenever possible.

Avoid Low Speed Techniques

Low Speed Techniques are typically used for circuits with Amplifiers and/or Data Converters with speeds ≤1MHz

Common Things to Avoid:

1. **Ground Planes**
   - **Common to Pour Copper Planes Everywhere**
   - **Instead, use with caution – Causes STRAY CAPACITANCE**
2. **Guard Rings**
   - **Typically used to minimize Leakage currents**
   - **But cause stray capacitance similar to Ground Planes – use with caution**



56

TEXAS INSTRUMENTS

"Low Speed" techniques are considered things done that work acceptably at frequencies below 1MHz. But would cause issues at frequencies above 10MHz.

Some of the most common mistakes are due to the capacitance issue. Having ground planes everywhere can be a good thing as it reduces inductance and creates a bypass capacitor. But, if placed in the wrong spot, it can be disastrous to the system.

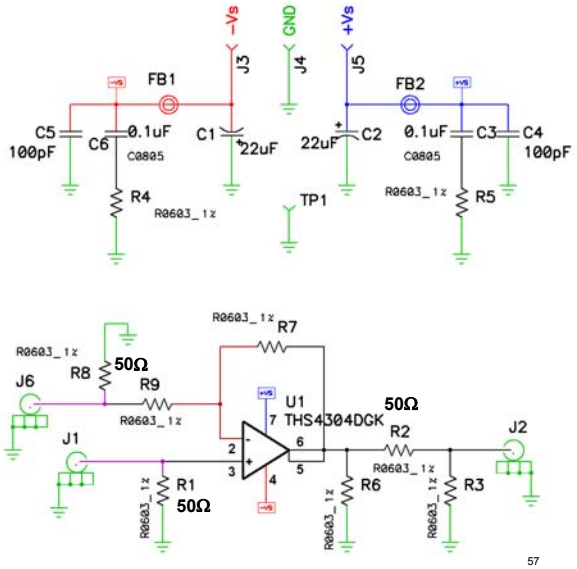
The use of guard rings for low leakage systems should generally e avoided as this also causes capacitance to occur in sensitive areas of an amplifier – most notably the inverting input node (aka summing node).

Another rule is to use low value resistors. Using anything above several k-ohms is generally not recommended. This is because even a small stray capacitance of 1-pF with a 10-kohm resistor can cause a pole (or worse yet a zero) to occur at 16MHz, which is typically well within a high speed amplifier's frequency of operation causing stability issues.

Lastly, minimize trace lengths to avoid trace inductance which can also cause instability concerns if in the wrong spot.

Example of High Speed PCB - Schematic

1. Multiple Caps for Low Freq. and High Freq. Bypassing
2. Look for ALL Current Paths and their Loops
3. Pay attention to Sensitive Inverting Input Node
4. Match Impedances
5. Ferrite Chips Used to Isolate Power Supply Currents
6. SMA Connectors
7. Small (0603) Components to minimize Inductance

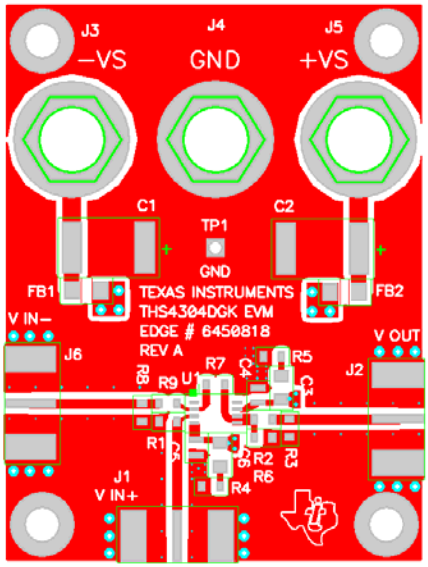


Texas Instruments

Let's see an example of a high speed PCB looks like. This is a schematic for the THS4303, a very high speed voltage feedback op-amp that has a bandwidth greater than 1.5-GHz. With such high bandwidth, the design must pay attention to all high speed constraints or else the amplifier will be unstable.

Example of High Speed Layout: Top Layer

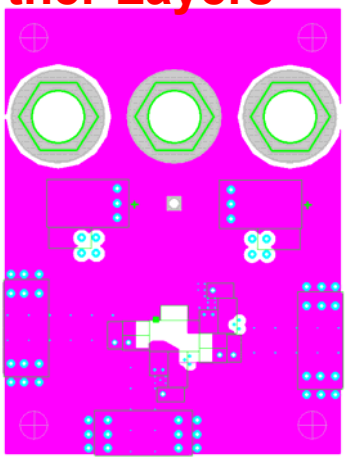
1. Signal In/Out traces are microstrip line with Z0 = 50Ω.
2. Terminating Resistors next to Amp.
3. Output Series Resistor next to Amp.
4. 100pF NPO Bypass Caps next to Amp.
5. Larger Bypass Caps Farther Away with Ferrite Chips for HF isolation.
6. MULTIPLE Vias Everywhere to Allow for easy Current Flow – no spokes
7. Short, Fat Traces to reduce inductance
8. Side Mount SMA connectors for Smooth Signal Flow
9. Rounded Signal Traces, no 90° bends



Texas Instruments

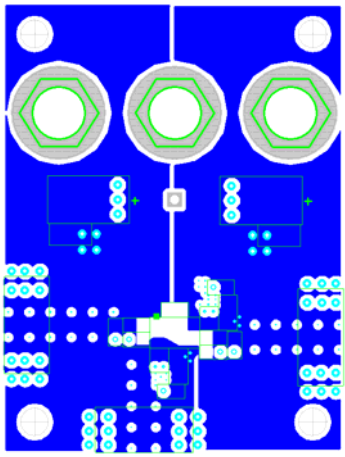
The top layer of the PCB is shown. Because this si a relatively simple system, all of the components are mounted on the top layer. This eliminates the signal trace via concerns to ensure the best situation possible.

Example of High Speed Layout: Other Layers



Layer 2: Signal GND Plane

GND Plane Next To Signal Plane for Continuity in Return Current



Layer 3: Power Plane

Notice Cut-Out in Sensitive areas near Amplifier on ALL planes.

59

Texas Instruments

Notice the Ground layer is directly below the signal layer. This is to allow for the return current signal flows to be as close a possible to the signal traces. The PCB material thickness also dictates the characteristic impedance input and output traces.

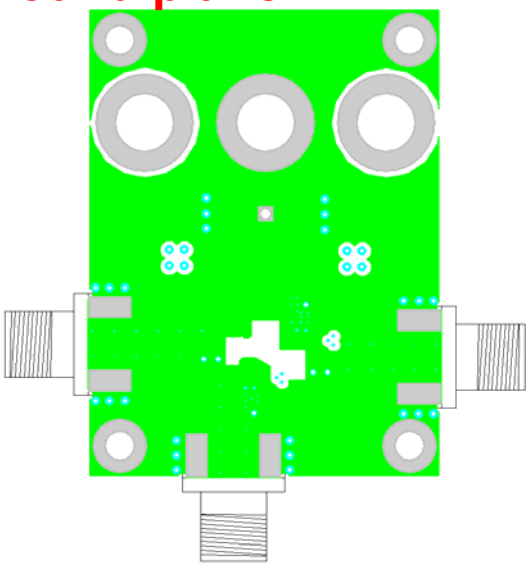
The power layer is below the ground layer, which helps form a good bypass capacitor by using the simple parallel plate capacitor method.

Notice the removal of ground plane and power plane around the sensitive areas of the amplifier. This includes the inverting input node, the feedback capacitor trace path, and the output node up to the series characteristic impedance matching resistor.

Also notice that multiple vias are placed on the component pads (SMA connectors and bypass capacitors for example).

Example of High Speed Layout: Bottom Layer – ground plane

1. Solid GND plane to minimize inductance.
2. Layer-2 GND plane and Bottom Layer form excellent bypass capacitor with Power Plane.
3. All Signals are on Top Layer to minimize the need for signals to flow through vias.
4. Multiple Vias Everywhere – No spokes
5. Cut-Out around Amplifier to reduce Stray Capacitance

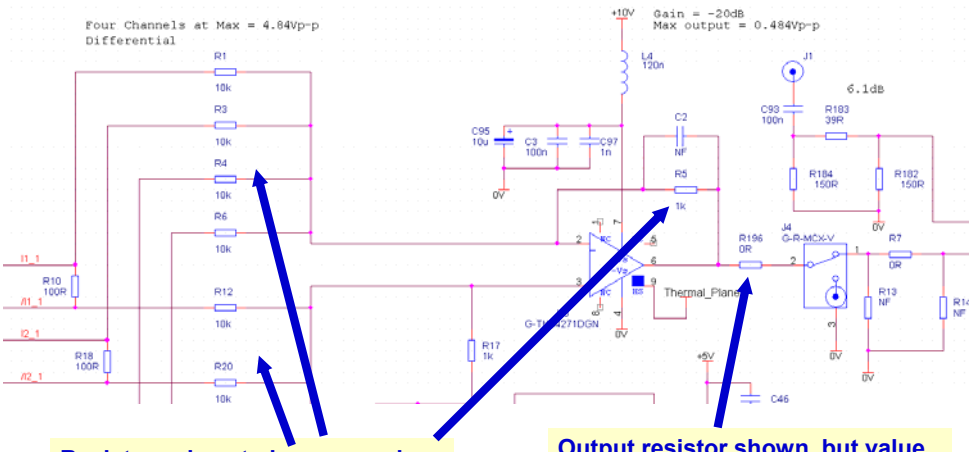


Texas Instruments

Notice the number of vias utilized between the top layer ground, second-layer ground, and the bottom layer ground. This ensures minimal current loop areas allowing the return currents to flow where they want to flow – directly under the signal trace.

Lastly, there are NO spoke connections to any ground point. Spokes are typically used for thermal relief, which they provide along with increased impedance due to restricted current flow. This solid connection ensures minimal inductance and although not really required for this design, good thermal conductivity.

Bad Component Values

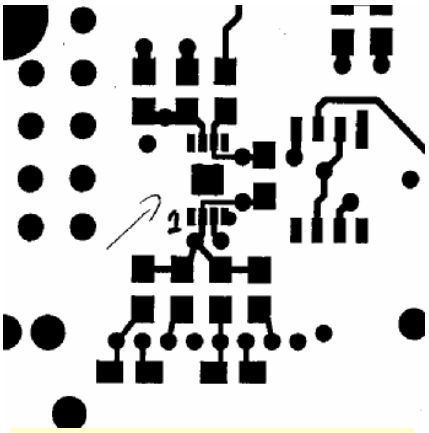


Resistor values to large => reduce by factor of 10x

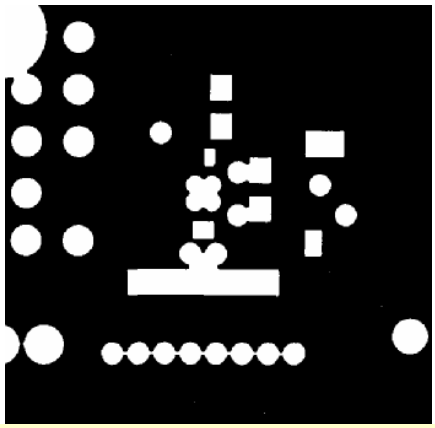
Output resistor shown, but value is 0 ohm = should use 10 ohm (or more)

Texas Instruments

Bad Layout



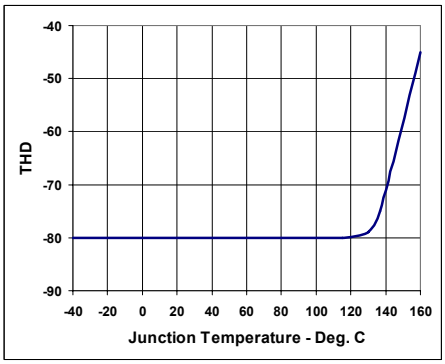
Top Layer: Signal



Layer 2: Signal GND Plane. Notice plane not removed to reduce CSTRAY, and no connection from PwrPad vias

Thermal Issues – Silicon

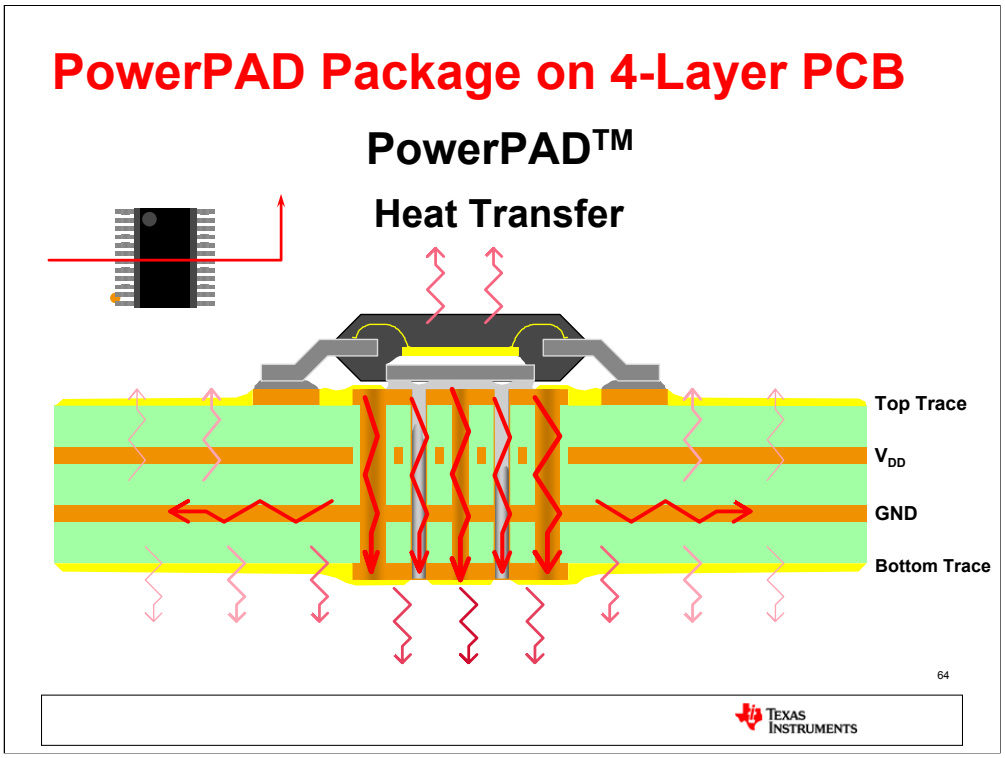
- Lower Junction Temperature Improves Long-Term Reliability
- Amplifier performance degrades with high junction temperature



Texas Instruments

Thermal issues often arise in many systems. As far as the integrated circuit is concerned, the silicon temperature has a working area that is defined by the process of the silicon. Elevated junction temperatures can reduce long term reliability resulting in a part that ultimately fails.

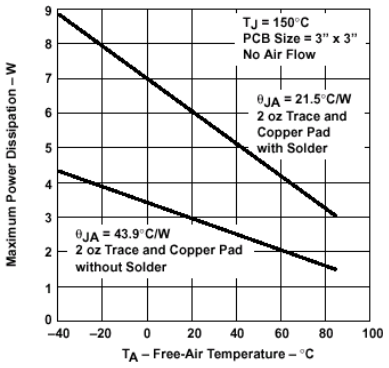
Additionally, the performance of the part typically start to degrade at temperature extremes – both hot and cold. So it makes sense to pay attention to the thermal characteristics of the part, the power dissipation of the part, which package to use, and ultimately the PCB layout.



Utilizing the copper planes on the PCB for thermal conduction is an excellent way to remove the heat from an IC. The use of a PowerPAD can allow over 3X better heat dissipation that a traditional package without the thermal pad while still using the same footprint.

Thermal Management

- **Must do thermal management at the device, the board, and the box levels**
  - **Device: proper package heat sinking**
    - **Thermal vias to Cu planes**
    - **Unobstructed airflow**
    - **Soldering the device thermal pad to the PCB**
  - **Board level**
    - **Heat flow out of the board**
    - **Air flow, PCB card guides, PCB with metal heat sinks**
  - **Other Devices**
    - **Other Active parts generate Heat**
    - **Can cause localized hot-spots on PCB – effectively reducing thermal flow and increasing Silicon Temp.**



Texas Instruments

See Application note SPRA953 – IC Package Thermal Metrics for more information. The only thing that must be done is to lay out the PCB correctly for this pad and soldering the part to the pad. Failure to solder the pad to the PCB will result in an increase in thermal resistance and cause the junction temperature to rise which may hinder it's performance or reduce the long term reliability.

See Application note SLMA002 –"PowerPAD Thermally Enhanced Package" for more information.

Thermal Calculations

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CA}$$

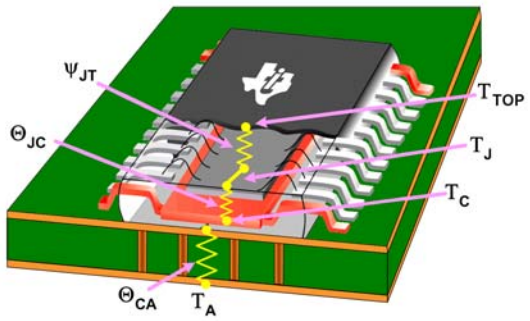
$$Power = \frac{T_{JUNCTION} - T_{AMBIENT}}{\Theta_{JA}}$$

Θ_{JC} = Thermal Resistance Junction to Case (°C/W)

Θ_{CA} = Thermal Resistance Case to Ambient (°C/W)

Θ_{JA} = Thermal Resistance Junction to Ambient (°C/W)

$$T_{JUNCTION} = T_{TOP} + (\Psi_{JT} \cdot Power)$$



Ψ_{JT} is useful to calculate Junction Temperature

Ψ_{JT} is NOT a true Thermal Resistance – Only used as a Tool

Remember θ_{CA} is dependant upon package, PCB design, and external environment. Thus, θ_{JA} can fluctuate considerably from design to design!!!

Texas Instruments

Trying to figure out what the silicon junction temperature really is can be quite a daunting task. But using simple formulas can make things go quickly. The hardest part about doing thermal calculations is trying to figure out the PCB thermal impedance. Every PCB design is different which results in the Θ_{CA} value to be different. Add to the fact that other active devices, and some passive devices too, create heating of the PCB, the design can be difficult.

Once a PCB is built and populated, one way to measure the silicon junction temperature is by using the Ψ_{JT} formula. For PowerPAD packages, the dominant heat flow is through the PowerPAD itself. Very little heat flows through the package. But it is difficult to measure the case temperature as it is soldered onto the PCB.

Ψ_{JT} allows you to simply measure the top of the package, and quickly calculate the junction temperature. This is not a thermal resistance in the classical sense as there is essentially no heat flow through this point. But rather it is a measurement tool to simplify the measurement of the junction temperature.

See Application note SPRA953 – IC Package Thermal Metrics for more information.

Measuring PCB Parasitic Capacitance

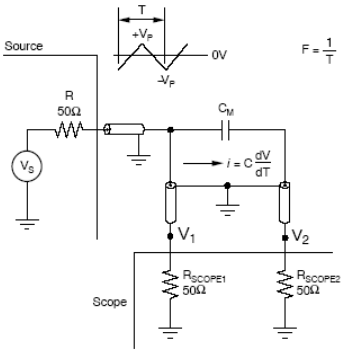
After building a PC boards one often is not sure the traces have the correct inductance or capacitance. It's even more difficult to measure those values without network analyzer or TDR.

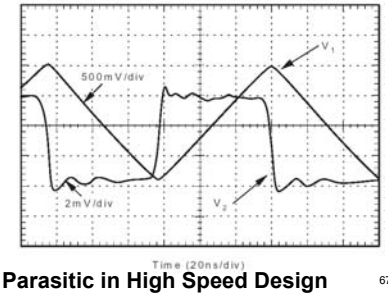
A very easy way to measure trace's capacitance is to use a ramp generator and oscilloscope, with the hook-up shown here.

$$i = C\frac{dV}{dt} \rightarrow \frac{dV}{dt} = \frac{2 \cdot V_{1PP}}{\frac{T}{2}} = V_{1PP} \cdot F \cdot 4$$

$$V_{2PP} = (50\Omega)C\frac{dV}{dt} = (50\Omega)C \cdot V_{1PP} \cdot F \cdot 4$$

$$C_M = \frac{V_{2PP}}{V_{1PP}} \cdot \frac{1}{4(50\Omega)F}$$





See application note SB0A094 Measuring Board Parasitic in High Speed Design

Texas Instruments

In some cases, it is desirable to know how much parasitic (stray) capacitance is actually on a trace. This may help determine stability problems or to verify a characteristic impedance.

A relatively simple way to measure this is with the above test set-up. This set-up uses an HP8116A function generator (V_{gen}) to drive a tiangle wave through coaxial cable where one end is solder to the boards trace, ground plane, etc and two identical points are measured using an oscilloscope terminated in 50Ω.

This method can measure capacitance to an accuracy of 30f to 50f and includes fringing effects associated with high frequency fields.

See the TI Application Report entitled "Measuring Board Parasitics in High-Speed Analog Design", SBOA094

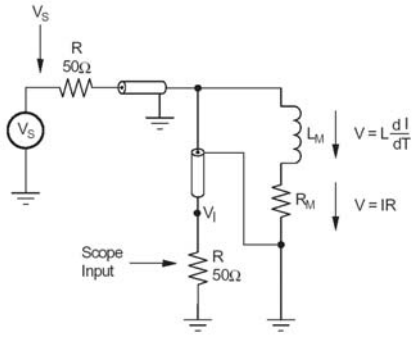
Measuring PCB Parasitic Inductance

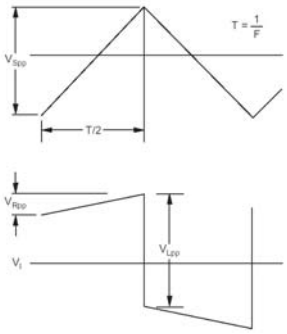
A very easy way to measure trace's Inductance is to use a ramp generator and oscilloscope, with the hook-up shown here.

$$\frac{V_{S_{PP}}}{R} = I_{TEST}$$

$$V_{L_{PP}} = \frac{L_m \cdot 2 \cdot V_{S_{PP}}}{\frac{R \cdot T}{2}} = \frac{L_m \cdot 4 \cdot F \cdot V_{S_{PP}}}{R}$$

$$L_m = \frac{V_{L_{PP}} \cdot R}{4 \cdot F \cdot V_{S_{PP}}} \qquad R_M = R \frac{V_{R_{PP}}}{V_{S_{PP}}}$$



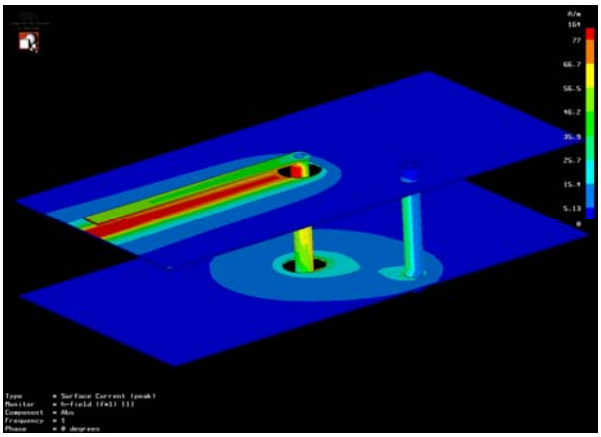


See application note SB0A094 Measuring Board Parasitic in High Speed Design

Very similar to measuring the capacitance of a PCB trace, this set-up shows how to accurately measure a PCB trace's inductance.

Taking a Look at Vias

- Must have Return Path Vias next to Signal Path Vias.
- Notice Large Current Density Area flow in return path.
- Will have a change in impedance with this configuration.



2-Layer PCB showing Current Density of PCB trace and Single Return Path Via.

69

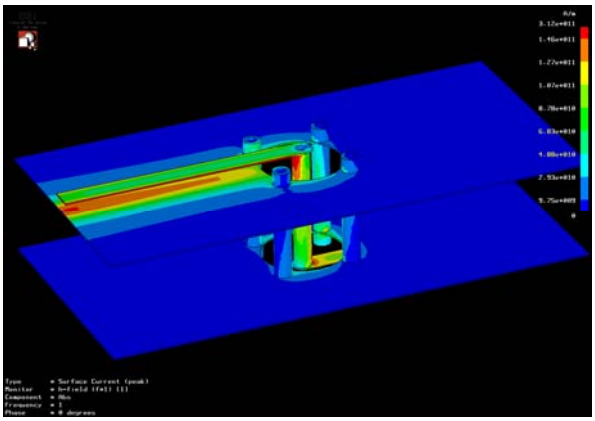
Texas Instruments

Now let's take a look at vias once again. We know that the return current density follows the trace path directly under the signal trace. But what happens when the signal trace goes through a via? How will the return current flow form the bottom ground layer to the top ground layer? The current WILL find a way to do this, one way or another and you may not like the path it chooses.

To minimize this return current flow path problem, every time a via is utilized, a ground via should also be utilized next to the signal via. This allows the return current to flow near the signal current flow. But, the signal via flows through essentially a cylinder that wants to have the return current flow 360° around it. If a single ground via is used for the return current, the characteristic impedance of the trace will be altered slightly and may be an issue.

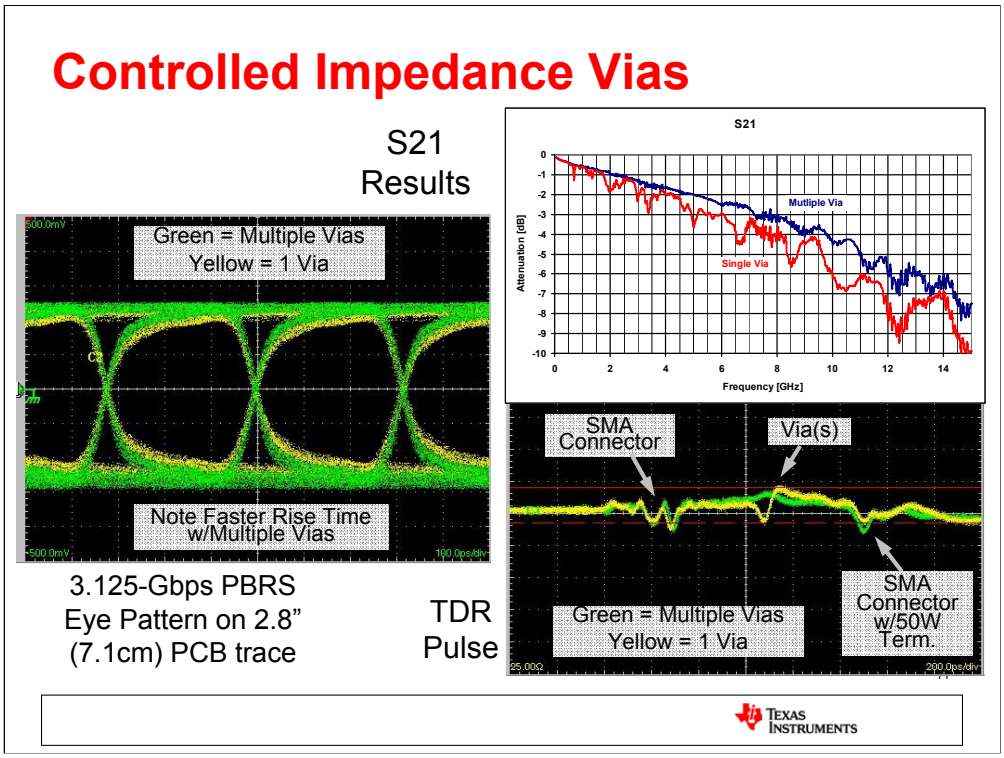
Controlled Impedance Vias

- Better Solution is to add Multiple Return Path Vias.
- Notice minimal Current Density Area Flow at vias.
- Improved impedance – reduces reflections.



2-Layer PCB showing Current Density of PCB trace and Multiple Return Path Vias.

The obvious solution to help maintain the characteristic impedance of the via is to use multiple ground vias around the signal via. Using 4-ground vias next to the signal via shows very good results and should be utilized if possible.



These graphs show the difference between a single ground via and the 4-ground via configuration. These tests are real results form a test PCB constructed to illustrate the differences between the two scenarios.

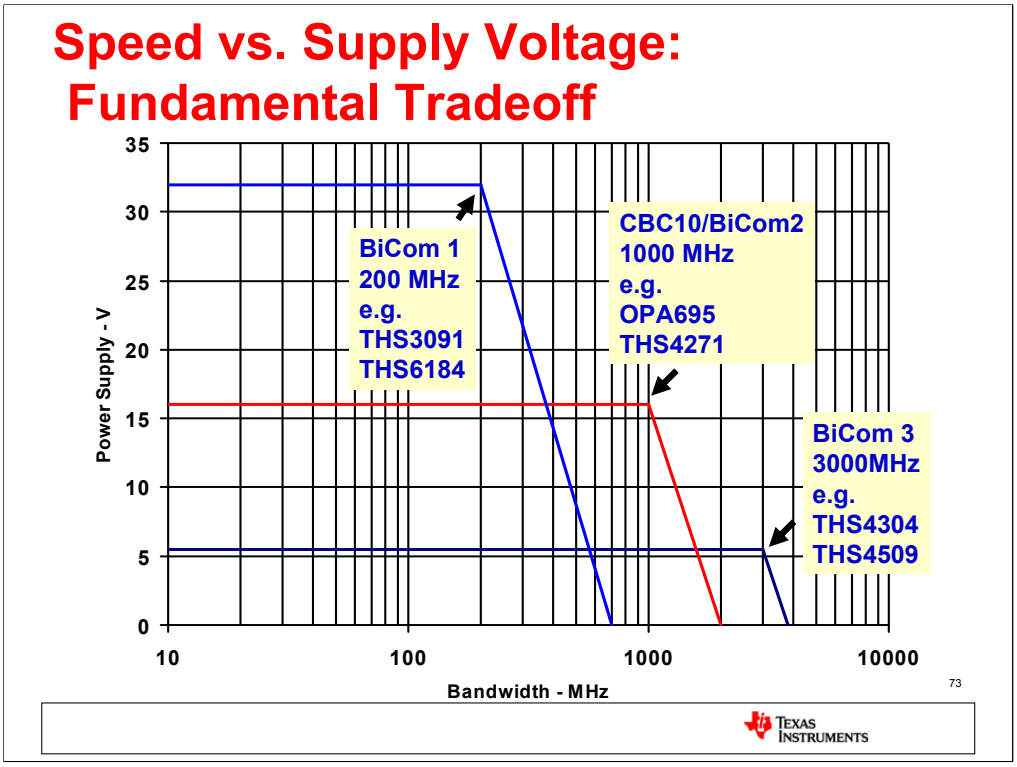
As these results show, using the 4-via configuration widens the PBRS (pseudorandom-bit-stream) eye pattern indicating a better high frequency system. It also improves the S21 (input reflection) considerably, and a TDR (time-domain-reflectometry) pulse shows improved impedance matching through the via.

For more information see the October 2, 2003 article in EDN magazine entitled “Designing Controlled-Impedance Vias” written by Thomas Neu, Texas Instruments.

High Speed Amplifier Product Overview

Wide Range of Amplifier Products

- Operational Amplifiers: VFB, CFB, FDA, Fixed Gain
- Variable & Programmable Gain Amplifiers
- Video Buffers with Integrated Signal Conditioning
- Video MUX
- Wired Communications Line Drivers



For the non-overlapping areas at the periphery of frequency are easy – but, for instance at a 100MHz requirement on a single +5V supply, parts from 5 different processes might work (including the 5V CMOS OPA3xx series) – lots of overlap. Normally, for a given level of performance the faster processes will achieve the desired results with lower supply current in the overlap region.

High Speed Amplifier “Hot Parts” List

	Note 1.	The supply voltage is the total across the device - these are in approx. ascending order of performance in each block						
	Note 2.	All of these devices are >50MHz Bandwidth and are unity (or low) gain stable (except where noted NUGS - Non-Unity Gain Stable)						
	Note 3.	In most cases the single channel version is shown - often there is also multi-channel and/or versions with disable not shown here, but will be shown in the single data sheets						
	Note 4.	In some cases, there is only a dual or quad of a part and that is what is listed. If not specifically stated otherwise, each part # here is a single.						
NEW PARTS IN RED			**OPERATING SUPPLY VOLTAGE <5.5V**			**OPERATING SUPPLY VOLTAGE RANGE FROM 4V --> 12V (approx.)**		**OPERATING SUPPLY SUPPLY RANGE FROM 10V --> 32V (approx)**
		THS4304	Unity Gain Stable ,1GHz		OPA830	RR Output, Low power, low cost	THS4051	Moderate Speed, Low cost
					OPA820	Low Noise, Low power, Low cost	THS4081	Low power,
					OPA2613	Dual, low noise, High Io, DSL Driver	THS4031	Low Noise,
					OPA690	High Slew Rate, low power	THS4011	Highest Speed +/-15V VFB
VOLTAGE FEEDBACK					OPA698	Fast Recovery Output Limiting		
OP AMPS (VFB)					OPA656	JFET Input, excellent DC precision		
					THS4271	Very low harmonic distortion		
					OPA890	Low Power, Unity Gain Stable w/Disable		
					OPA2889	Dual, Very Low Power, UGS w/Disable		
					OPA847	Lowest Noise, Highest Bandwidth -NUGS		
					OPA4872	4:1 High-Speed Video Multiplexer		
					OPA684	Very Low power, low BW vs. Gain variation	THS3110	Low power, moderate speed, high Io
					OPA691	Low Power, high output current	THS3120	Medium speed
CURRENT FEEDBACK					OPA694	Low power >500Mhz	THS6132	Dual, Class G, DSL Driver
OP AMPS (CFB)					OPA2674	Dual, with power control, DSL Driver, High Io	THS6182	Dual, Class AB, DSL Driver
					OPA695	Very wideband, high Intercept	THS6184	Quad, Class AB DSL Driver
							THS3091	Highest Speed +/-15V CFB
FULLY DIFFERENTIAL		THS4509	G>+2, Very wideband, very low distortion		THS4502	Wideband, Centered Input Range	THS4130	Audio speed, very low noise & distortion
AMPLIFIERS (FDA)		THS4508	G>+2, Very wideband, very low distortion					
			Input Voltage Range Includes Negative Supply					
		THS4511	Unity Gain Stable, Very wideband, very low distortion					
			Input Voltage Range Includes Negative Supply					
		THS4513	Unity Gain Stable, Very wideband, very low distortion					
		THS4520	Unity Gain Stable, Wideband, RRO, low distortion					
FIXED GAIN		THS4302	2.5GHz, Gain of 5V/V		OPA832	RR output Gain of 2 Video Line Driver		
		THS7303	Triple 2X1 Video Mux/driver with selectable filter		OPA693	>1.2GHz Gain of 2 Video Line Driver		
		THS7313	Triple 2X1 Video Mux/driver with selectable filter		BUF602	>1.4GHz Unity Gain Buffer with MidRef.		
		THS7314	Triple SDTV Amp w/5th order filter and 6-dB gain		OPA875	2:1 High-Speed Video Multiplexer, G=+2		
		THS7316	Triple, HDTV Amp w/ 5th order filter and 6-dB gain					
		THS7318	Triple, Low Power EDTV/SDTV line driver w/LP filters					
		THS7353	Triple 2X1 Video Mux/driver with selectable filter					
		THS7315	Triple, SDTV Amp w/ 5th Order Filter and 5.2V/V Gain					
		THS7347	Triple RGBHV Video Buffer w/I^2C Control					
		THS7327	Triple RGBHV Video Buffer w/I^2C Control					
ADJUSTABLE GAIN		THS7530	Differential I/O, 300MHz BW, 35dB Gain adjust		VCA810	+/-40dB Range, 30MHz BW		

Texas Instruments

OPA659

Industry's fastest JFET input amplifier

Features

- **Large Signal Bandwidth**
  - @ 2Vpp: 575 MHz (G=1)
  - @ 6Vpp: 200MHz (G=1), 25MHz (G=10)
- **SR=2550V/µs** (4V step)**, 8ns settling time and 8ns overdrive recovery** (1% 4 V step)
- **Excellent SFDR: 60dBc @ 100MHz**
- **Power Supply Voltage: ± 3.5V to ± 6.5V**

Benefits

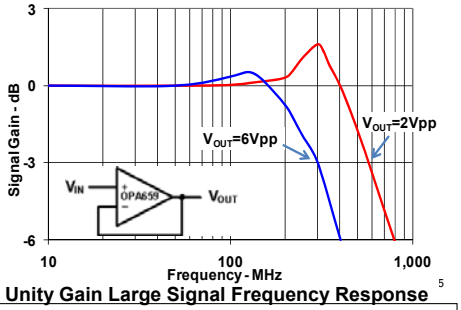
- **3x wider large signal (>2Vpp) bandwidth vs. competition**
- **3x faster pulse response maintains fast signal integrity**
- **25dB improvement over comp, providing higher linearity and lower distortion**
- **Delivers 20% higher output voltage swing**

Applications

- **High impedance data acquisition input amp**
- **High impedance oscilloscope input amp**
- **Wideband photodiode transimpedance amp**
- **Wafer scanning equipment**

EVM

OPA659EVM (Contact Factory)



Unity Gain Large Signal Frequency Response

Texas Instruments

THS4520

Low Distortion, Fully Differential, RR Out, High Speed Amplifier

Features

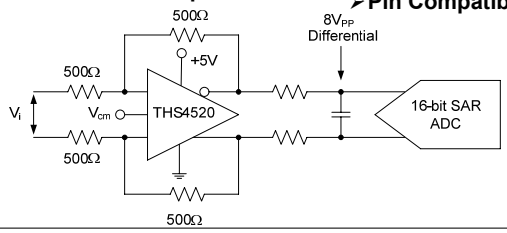
- 3.3V and 5V Single Supply Operation
- Small Signal Bandwidth: 450MHz (G=2V/V)
- Slew Rate: 570V/µs (2V step, G=2V/V)
- Settling Time: 7ns to 0.1% (2V step, G=2V/V, R_L=200Ω)
- HD_2: -115dBc at 100kHz (8Vpp, G=2V/V, R_L=1kΩ)
- HD_3: -123dBc at 100kHz (8Vpp, G=2V/V, R_L=1kΩ)
- Input Voltage Noise: 2nV/√Hz (f>100kHz)
- Output Current : 105mA
- Output Common-Mode Control
- Power-Down Quiescent Current: 15µA
- QFN-16 package

Applications

- 3.3V and 5V High Resolution ADC driver
- Wireless communication
- Medical instrumentation
- Test and Measurement
- Differential DAC output amplifier

Benefits

- Single to differential conversion
- Very low 2nd harmonic distortion
- Pin Compatible FDA family



EVM

EVM Available

$2.25/1kpcs

Texas Instruments

OPA695 Ultra-Wideband, Current Feedback Operational Amplifier with Disable

- Performance features
  - AC Signal Handling Properties
    - 1400MHz Bandwidth at Gain = +2V/V (2900V/usec slew rate)
    - 450MHz Bandwidth at Gain = +/-8V/V (4300V/usec slew rate)
    - 3rd Order Intercept > 32dBm to 100Mhz
    - 1.8nV Input Noise Voltage
    - Broadcast Video dG/dP = .04%/.007°
  - DC Specifications & Properties
    - Low input offset voltage (<±3mV worst case at 25C)
    - High output voltage/current (+/-4V with +/-90mA)
    - Precise supply current(12.9mA) - Optional Shutdown to 100uA
    - ±5V and single +5V specifications
    - Single +5V to +12V supply range supported

OPA695

Ultra-Wideband, Current Feedback Operational Amplifier with Disable

- **1400MHz Bandwidth (Gain of +2)**
- **2500V/usec Slew Rate (Gain of +2)**
- **78dBc SFDR at 10Mhz (500Ω Load)**
- **0.9nsec Rise/Fall Time for 2V step**
- **1.8nV/√Hz Input Noise**

Key Differentiators:

- **High Intercept to High Gains**
- **Single +5->+12V Supply operation supported**
- **SOT23-6 Packaging**

- **APPLICATIONS/MARKETS**
  - •Broadband Video Line Drivers
  - •LO Buffer/Mixer Driver to 1GHz
  - •Wideband ADC Buffer
  - •IF Stage Amplifier
  - •High Frequency Active Filters

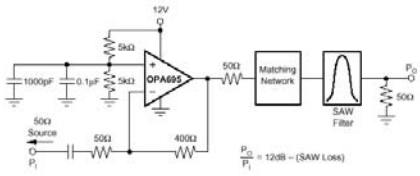
- **RELATED PRODUCTS**
  - **•OPA693 -700MHz Video line Driver**
  - **•OPA691 - 240Mhz, 5mA, Current Feedback Op Amp.**
  - **•THS3202 - dual, 1GHz, current Feedback Op Amp**

Suggested Resale (1000+)	Package Options	Temperature Ranges
OPA695ID - $1.34 OPA695IDBVR - $1.35 OPA695IDGKR - $1.35	SO-8 SOT23-6 MSOP-8	-40 to +85C

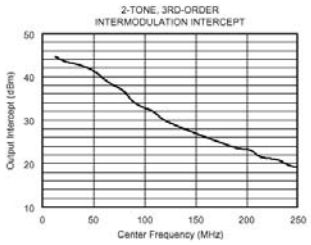
Texas Instruments

OPA695 Applications

12dB Gain, IF Amplifier with Exceptional Intercept Using Low Power



Low Distortion, 12dB Gain SAW Driver



- **Available Tools/Resources**
  - **•EVM Boards - by package style (unloaded, free)**
  - **•SO-8 (DEM-OPA68xU)**
  - **•SOT23-6 (DEM-OPA6xxN)**
- **Macromodels**
  - **• On e-LAb**