2009 Toronto Tech Day

Component and Layout Considerations for DC/DC Converters

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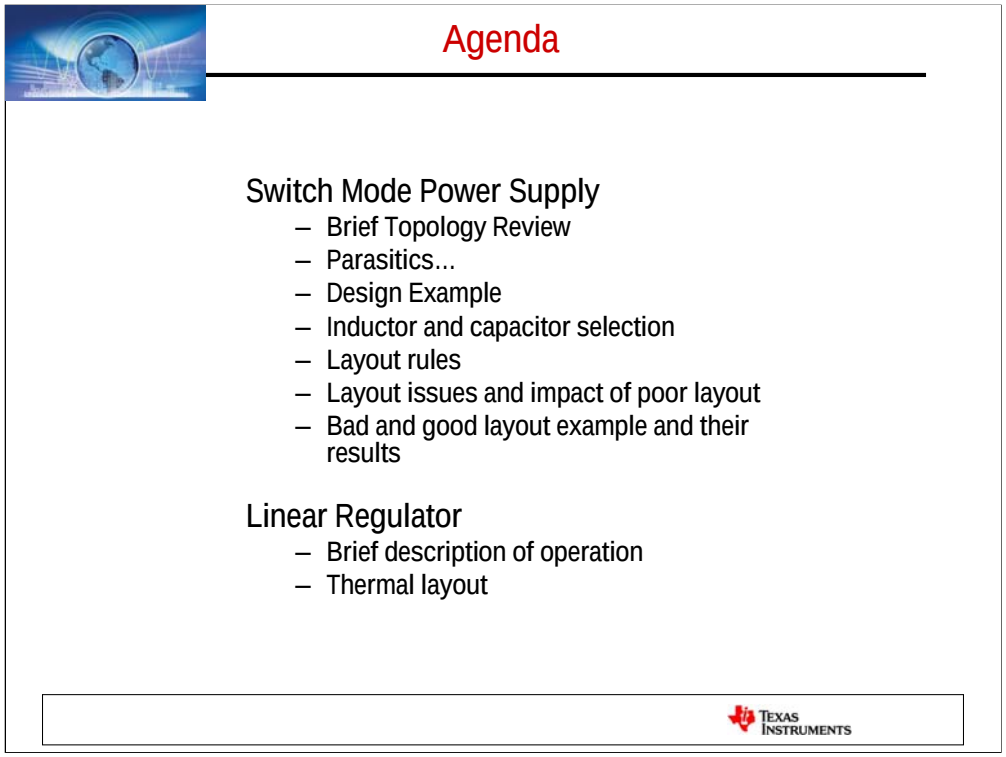
Texas Instruments



The presentation looks at two example DC/DC converter solutions to converter a 3.3VDC input to 1.8VDC output at 1.5Amps of load current. The first example solution is based on a switching power supply and the second is based on a linear regulator. The presentation covers how to select external components for each solution and provides layout guidelines to implement a successful solution.

Switching Regulator Solution

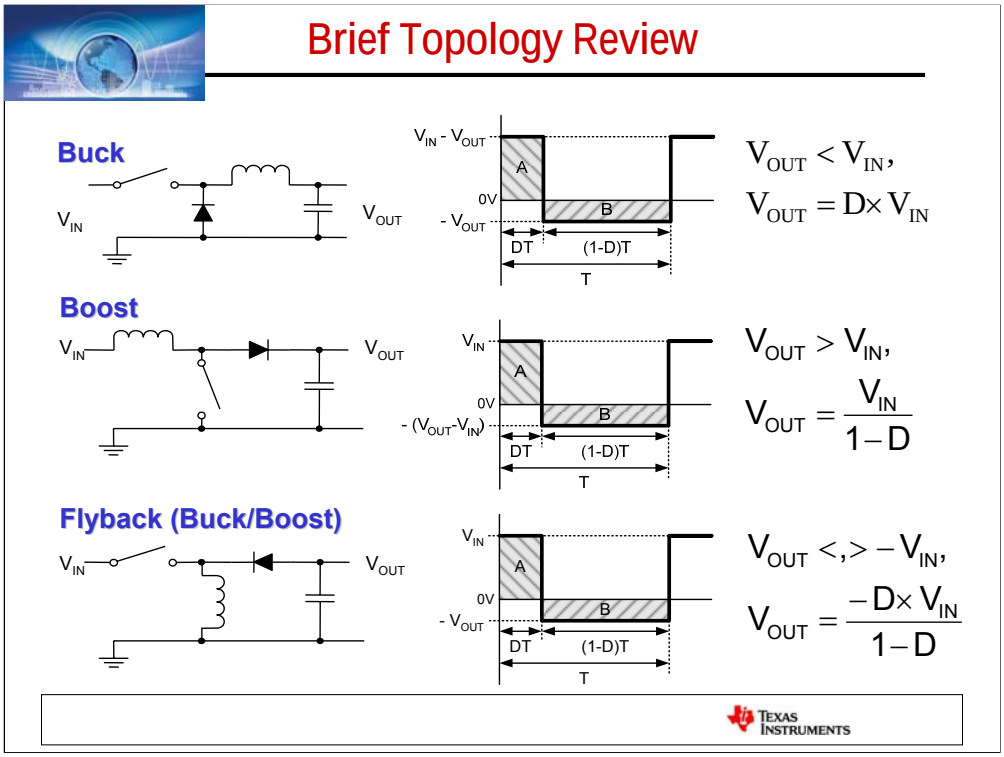
Pros and Cons of SMPS

Advantages

+ High efficiency
+ Can be scaled to provide any amount of power (mW to kW)
+ Small solution size (compared to the linear regulator)

Disadvantages

- Output switching noise
- External part selection impacts stability and performance
- Usually more expensive solution than linear regulator



Just to be brief and finish in one day…

The Most Important Components

The ones that you forgot about:

Parasitics…

The design stage takes 90% of the project time
Debugging takes the other 90% of the time

Parasitics

DC Parasitics (Resistance)

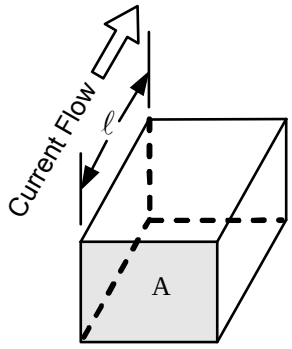
AC Parasitics

Components Parasitics

Magnetic Coupling

Ground Bouncing

Resistance Calculation Example



$$R = \frac{\rho l}{A}$$

$\rho = resistivity$

Material	μΩ-cm	μΩ-in
Copper	**1.70**	**0.67**
Copper (Plated)	**6.0**	**2.36**
Gold	**2.2**	**0.87**
Lead	**22.0**	**8.66**
Silver	**1.5**	**0.59**
Silver (Plated)	**1.8**	**0.71**
Tin -Lead	**15**	**5.91**
Tin (Plated)	**11**	**4.3**
Palladium	**11**	**4.3**

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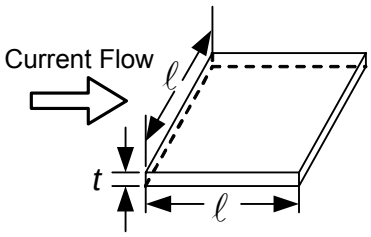
Opening the Cu mask for tin plating will not help.

Count Squares to Estimate Trace Resistance

Copper resistivity is 0.67 μΩ-in in. at 25°C and doubles for 254°C rise



$$R = \frac{\rho(\ell)}{t(\ell)}$$

$$R = \frac{\rho}{t}$$

Copper Weight (Oz.)	Thickness (mm/mils)	mΩ per Square mm (25°C)	mΩ per Square (100°C)
1/2	**0.02/0.7**	**0.86**	**1.3**
1	**0.04/1.4**	**0.43**	**0.65**
2	**0.07/2.8**	**0.23**	**0.26**

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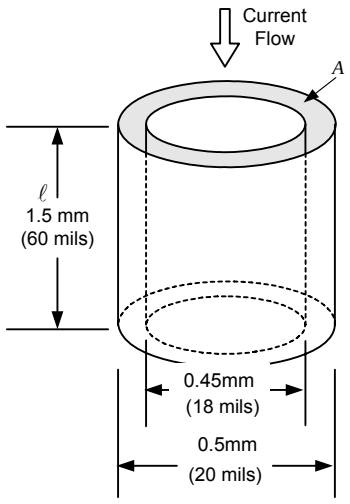
These slides are meant for gaining a ‘good practice feeling’ for the PCB parasitics assessment.

Vias Have Resistance Too

Typical rule of thumb is 1 A to 3 A per via



$$R = \frac{\rho l}{A}$$

$$R = \frac{\rho l}{\pi(r_o^{\,2} - r_i^{\,2})}$$

$$R = \frac{2.36 \times 10^{-6} \times 0.06}{\pi(0.01^2 - 0.009^2)} = 2.4\ m\Omega$$

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18 mils vias will ‘suck’ the solder under the IC’s thermal pads, check with the CM, usually 9mils are OK

Parasitics

DC Parasitics (Resistance)

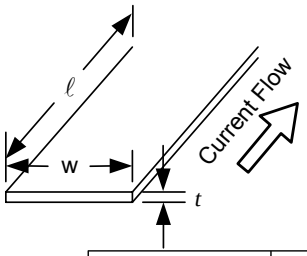
AC Parasitics

Components Parasitics

Magnetic Coupling

Ground Bouncing

Self Inductance of PWB Traces



$$L = 2\ell\left(\ell n\left(\frac{\ell}{t+w}\right)+\frac{1}{2}\right)\ nH\ (cm)$$

$$L = 5\ell\left(\ell n\left(\frac{\ell}{t+w}\right)+\frac{1}{2}\right)\ nH\ (in)$$

w (mm/in)	T(mm/in)	Inductance (nH/cm or nH/in)
0.25/0.01	**0.07/0.0028**	**10/24**
2.5/0.1	**0.07/0.0028**	**6/14**
12.5/0.5	**0.07/0.0028**	**2/6**

Due to the natural logarithmic relationship, large changes in conductor width have limited impact on inductance

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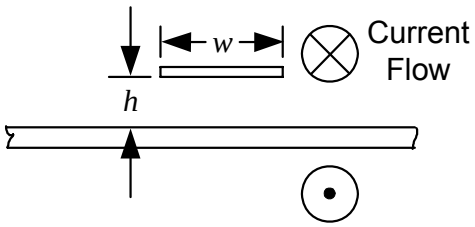
Compare the circled value with the one in the next slide

PWB Traces Over Ground Planes



$$L = \frac{2hl}{w} \text{ nH/cm}$$

$$L = \frac{5hl}{w} \text{ nH/in}$$

Metric			English		
h (cm)	w (cm)	Inductance (nH/cm)	h (in)	w (in)	Inductance (nH/in)
0.25	**2.5**	**0.2**	**0.01**	**0.1**	**0.5**
1.5	**2.5**	**1.2**	**0.06**	**0.1**	**3.0**

Substantial inductance reduction

Inductance inversely proportional to width

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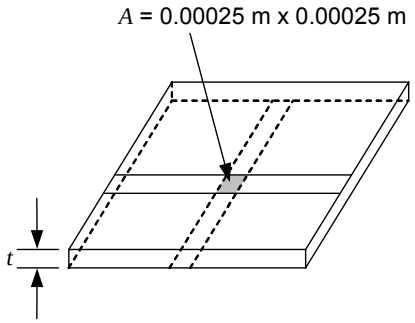
This shows as a good practice having the high current traces overlapped in adjacent layers

Stray PCB Capacitance

Consider two 10 mil traces crossing with 10 mil PWB thickness



$$C = \frac{\varepsilon_R \times \varepsilon_O \times A}{t}$$

$$C = 5\left(\frac{10^{-9}}{36\pi}\right)\left(\frac{0.00025^2}{0.00025}\right)$$

$$C = 0.01\ pF$$

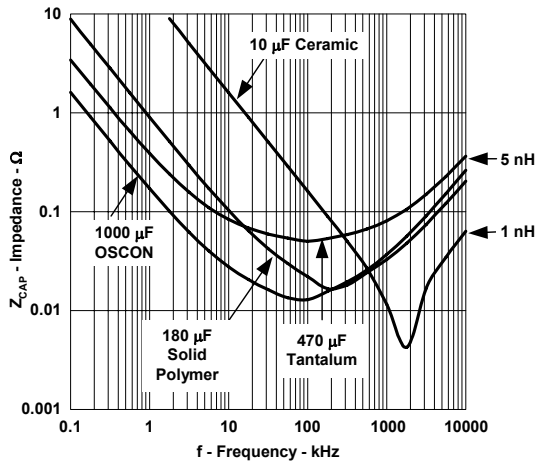
Not much capacitance but consider the area of all those components connected to the summing node

Parasitics

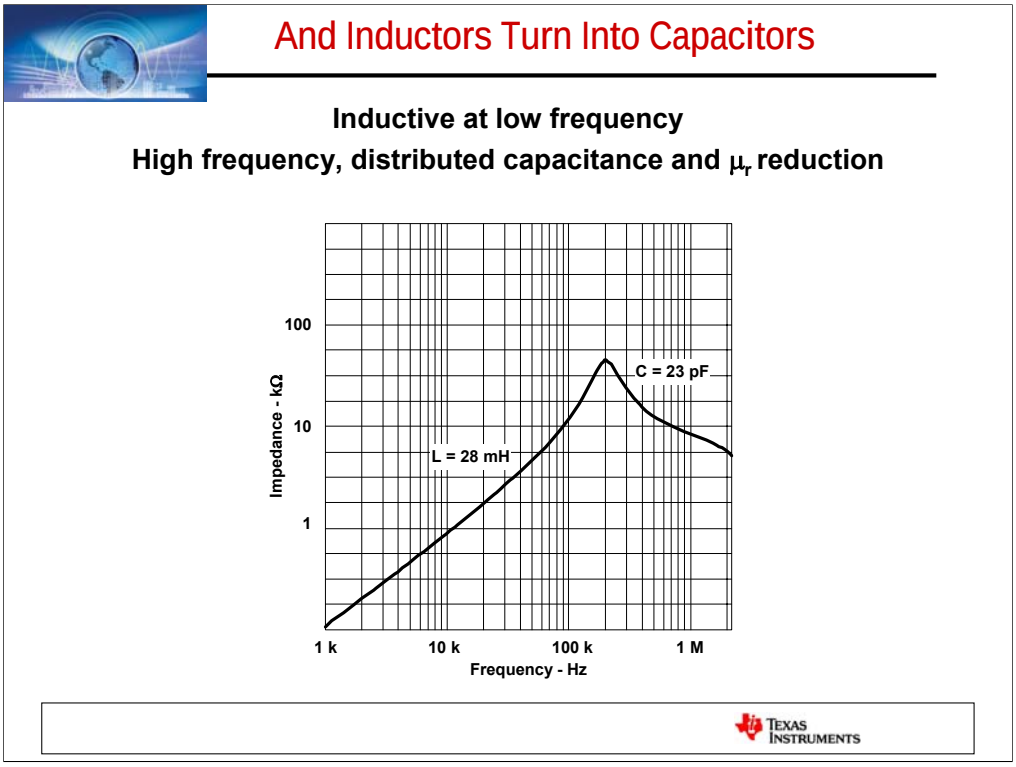
DC Parasitics (Resistance)
AC Parasitics
Components Parasitics
Magnetic Coupling
Ground Bouncing
Thermal Considerations
Design Examples

Capacitors Are Inductive...

Above Their Self-Resonant Frequency

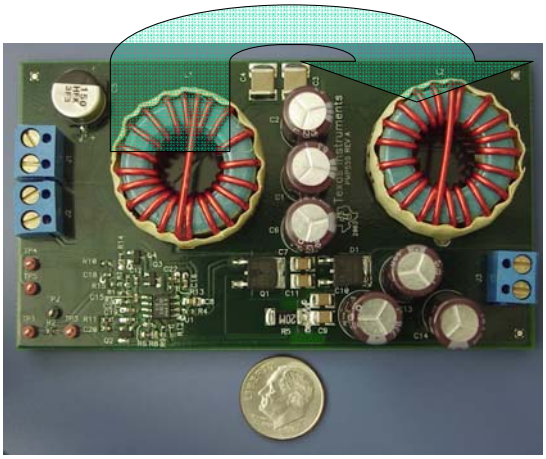


Measured ESL correlates well with the rule of thumb: inductance of 15 nH/inch

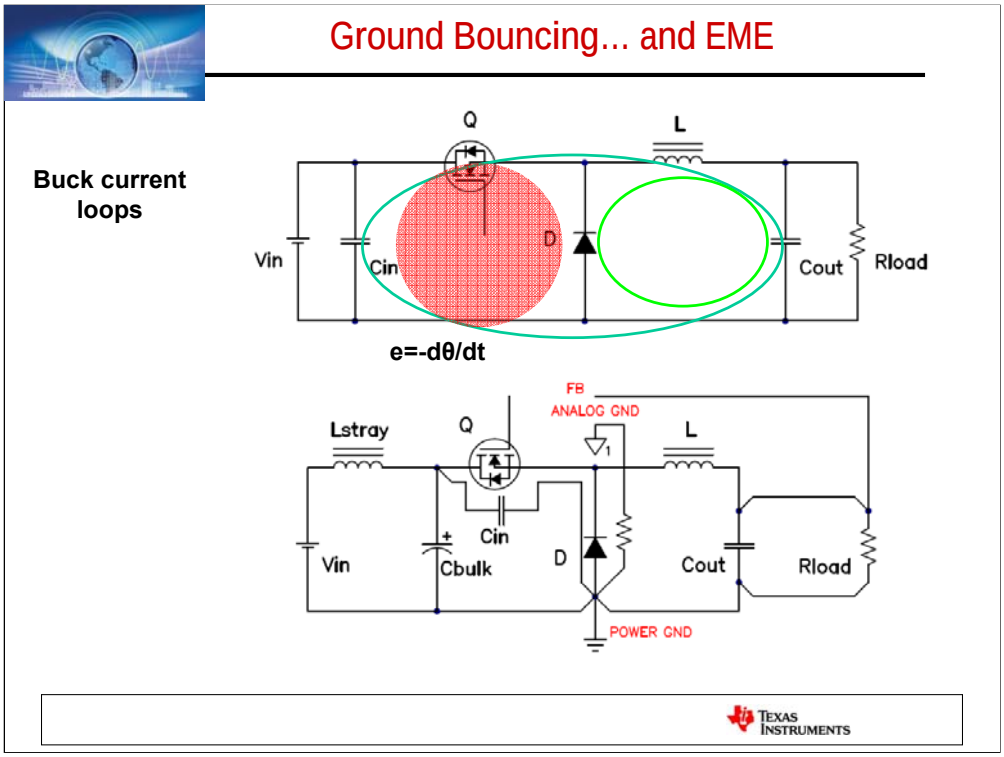


Check with the inductor manufacturer the fsr - self resonant frequency – as well as the frequency losses, a measure of the core performance and winding structure. Same for the inductor's polarity if marked.

Magnetic Coupling



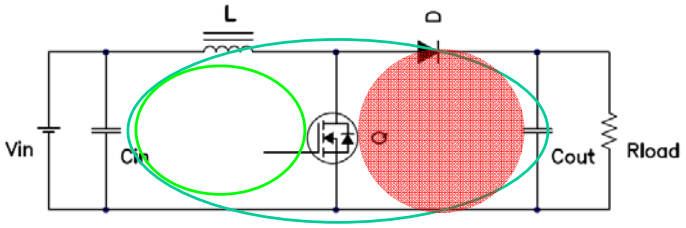
Consider alternate orientation of second inductor to minimize coupling



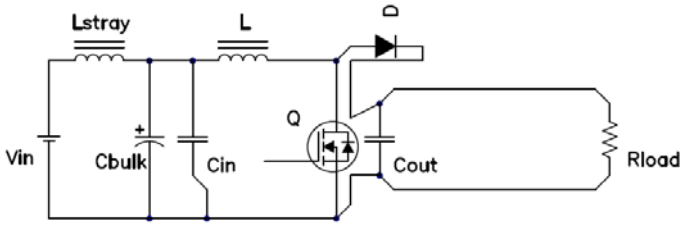
For layout designers: give two netlist names to the two grounds… short them with an software reported error at the design's end

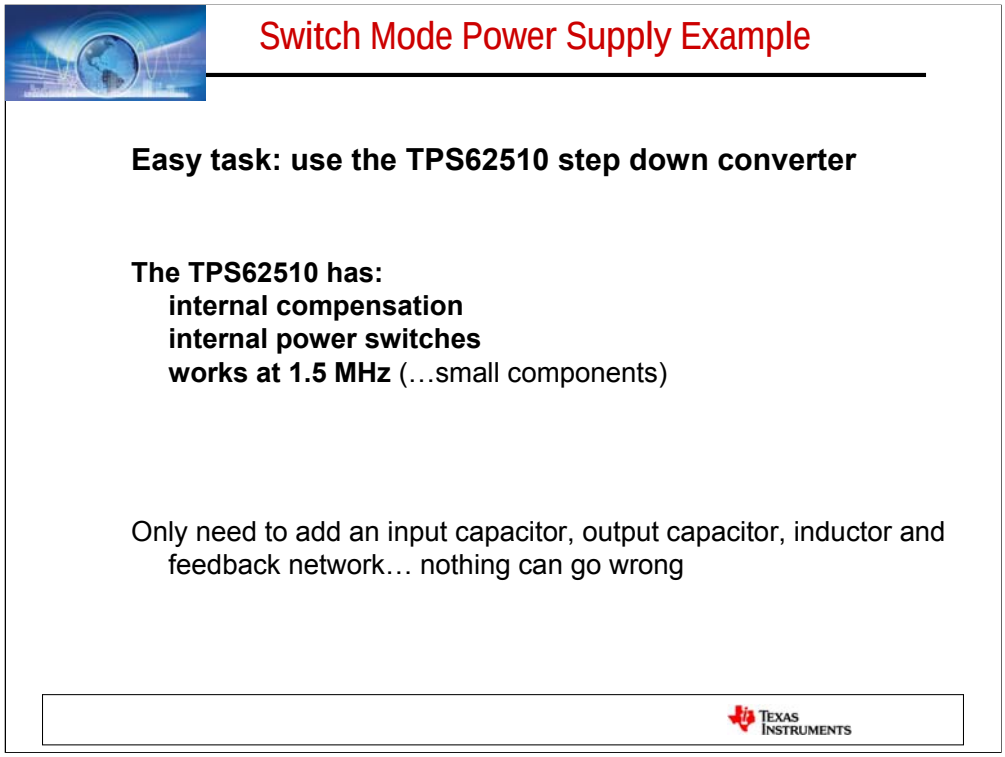
Ground Bouncing... and EME

Boost current loops



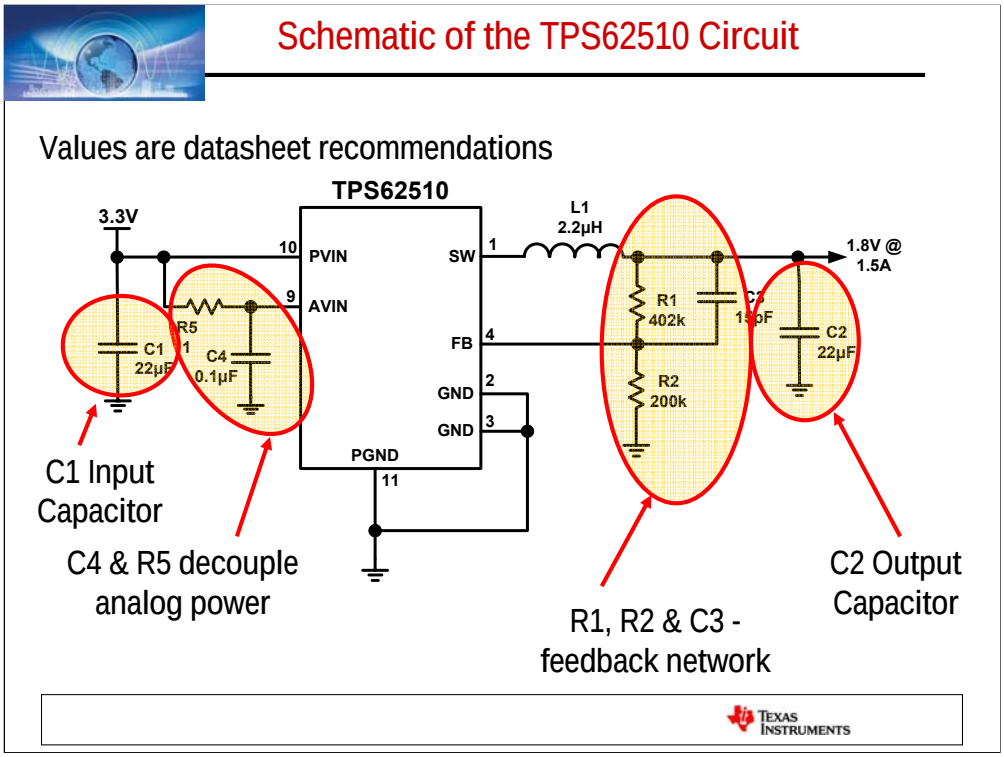
e=-dθ/dt



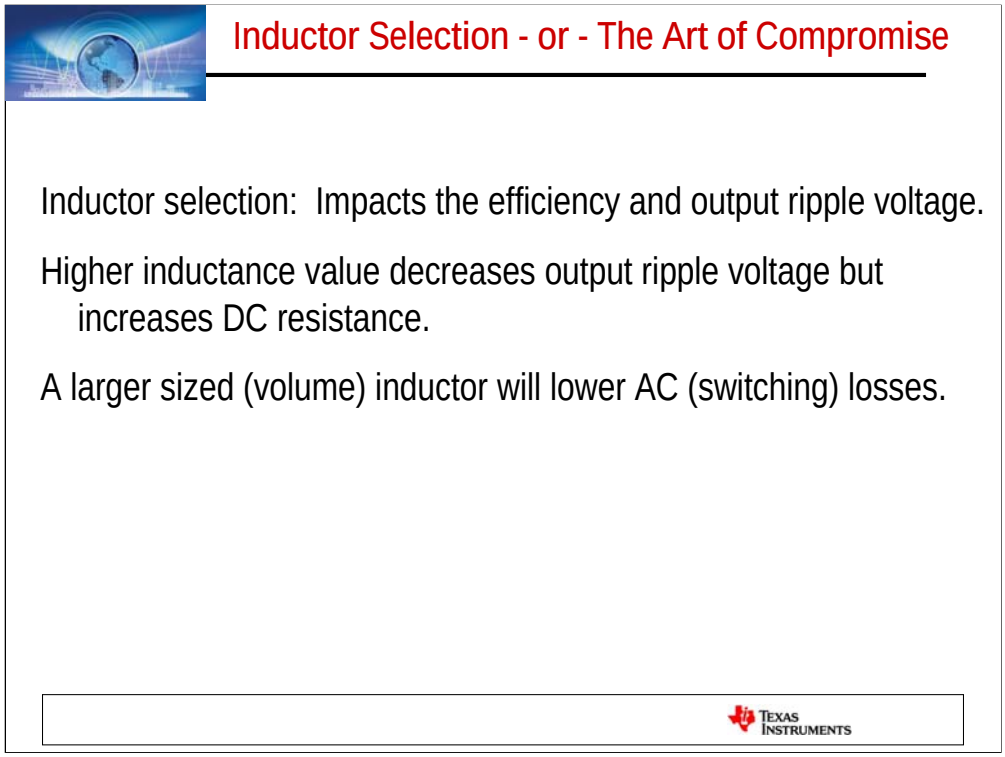


Assume you have already selected a suitable converter. For the following examples we will look at the TPS62510 step down converter which is acceptable for the input voltage, output voltage and load current. The TPS62510 is internally compensated and has internal power switches. The designer needs to add an input capacitor, output capacitor, inductor and feedback network in order to complete the converter. The TPS62510 is a 1.5Mhz switch mode power supply. This high of a switch frequency requires some special attention to layout which we will look at.

Schematic of the TPS62510 Circuit



This is the schematic for the TPS62510 DC/DC converter. It shows the required external components. The first step to designing with a portable power part is to select the external components. For this example, we will start with the inductor selection.



There are several parameters that are effected by the inductor. The inductor impacts the efficiency, output voltage ripple, size and cost of the solution. For example, selecting a high inductance value will decrease the output voltage ripple making the converter quieter but will increase the size and cost of the solution and may lower the efficiency due to higher DC resistance of the coil. A physically larger inductor may improve efficiency by reducing AC losses but this too will increase the solution size and cost. The designer must make trade-offs between size, cost, efficiency and output noise when selecting an inductor.

Inductor Selection

Inductor ripple current and output capacitor ESR) determine the output ripple voltage.

A higher inductance value lowers ripple currents so the converter will have lower output ripple voltage.

The higher the inductor ripple current, the higher the AC losses in the inductor.

Lower ripple allows for higher output current

$$\Delta I_L = V_{out}\left(\frac{1 - \frac{V_{out}}{V_{in}}}{L \cdot F}\right)$$

Texas Instruments

The output voltage ripple is created by the inductor ripple currents acting through the equivalent series resistance (ESR) of the output capacitor. The lower portion of the slide shows the equation for the inductor ripple current in a step-down converter. For most converter designs, the output voltage, switching frequency and rang of input voltages are fixed by system requirements. The only variable that effects the inductor ripple current available to the designer is the value of the inductor. From the equation, we can see that the inductor ripple current is inversely proportional to the inductance value. Increasing the inductance lowers the ripple current and thus would lower the output voltage ripple as well.

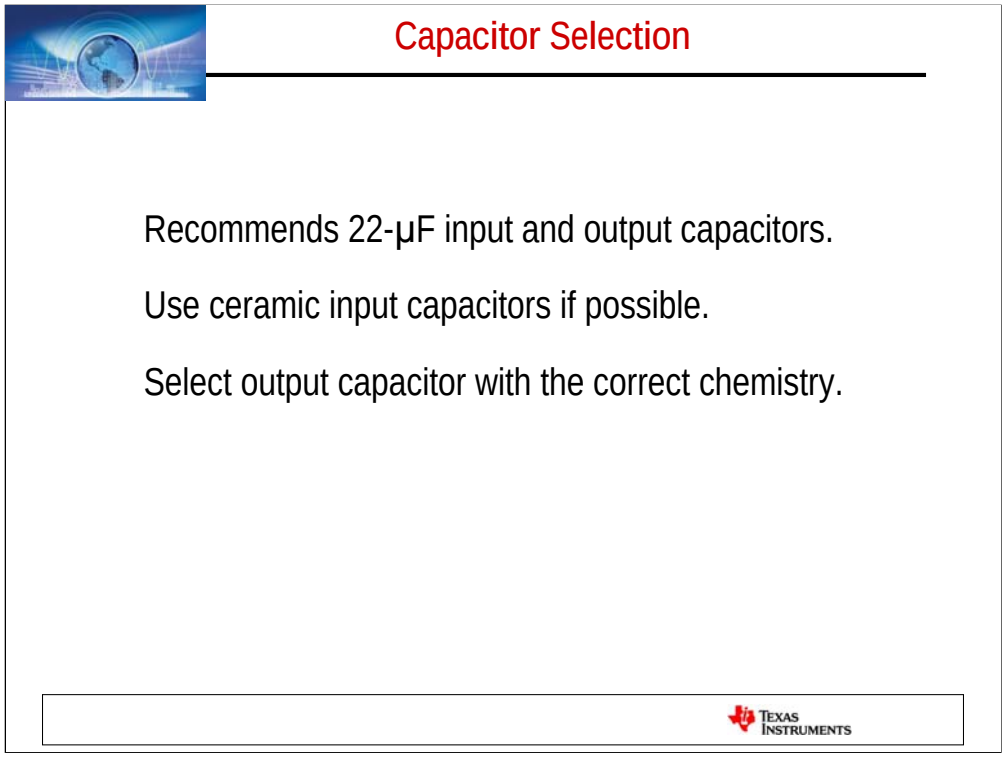
Inductor Selection

Inductor Part Number		SIZE VOLUME (mm3)	LOSSES Rdc (Ohms)	AC Loss (mW)	DC loss (mW)	Total Loss (mW)	Converter Efficiency at full load
ME3220	2.2µH	16.0	0.104	21.32	234	255.32	77.9%
LPS4012	2.2µH	19.2	0.1	14.75	225	239.75	78.2%
LPS4012	3.3µH	19.2	0.1	12.62	225	237.62	78.3%
DO1608C	2.2µH	85.8	0.07	6.63	157.5	164.13	80.0%
DO1608C	3.3µH	85.8	0.08	3.88	180	183.88	79.5%
DO1813H	2.2µH	271.1	0.035	3.95	78.75	82.7	82.0%
DO1813H	3.3µH	271.1	0.04	2.42	90	92.42	81.7%

A higher inductance in the same package reduces AC losses. However, this example has high DC current so DC losses dominate

AC and DC losses decrease as Volume increase

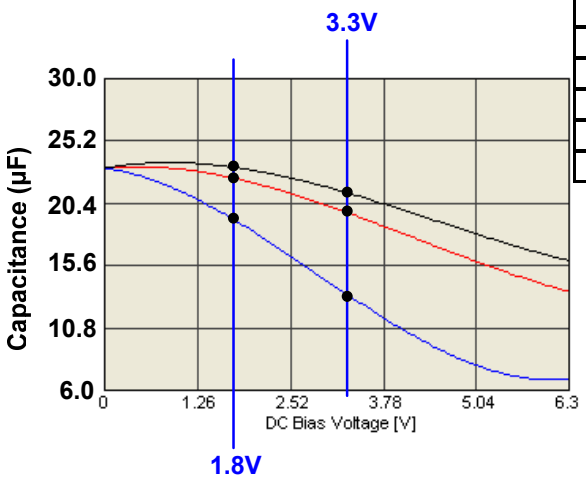
Need to compromise between the inductor size and efficiency



Some converters require specific amounts of ESR in the output capacitor in order to be stable. Substituting capacitors could cause problems. Ceramic capacitors are okay to use in the TPS62510 design.

Capacitance versus DC Bias

DC Bias	Case Size	Effective Capacitance (uF)
1.8	805	18.8
1.8	1206	22.2
1.8	1210	23.1
3.3	805	13.3
3.3	1206	19.6
3.3	1210	21.1



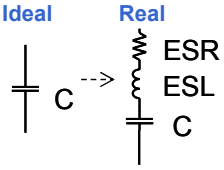
22 µF, 6.3V, X5R, 1210

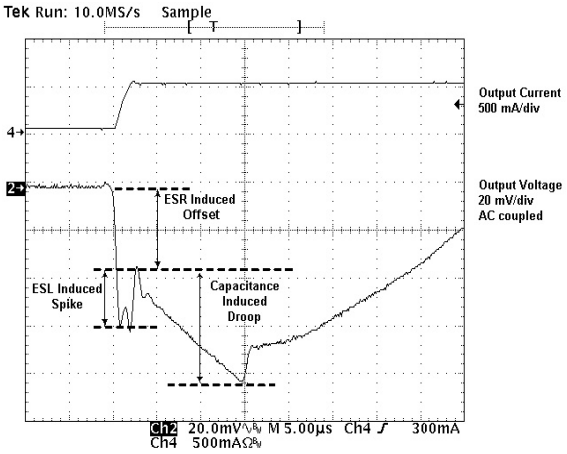
22 µF, 6.3V, X5R, 1206

22 µF, 6.3V, X5R, 0805

Capacitor Transient Response

Output capacitor parasitics





Part Placement and Layout

Problems from Poor Layout:

Low efficiency
Poor regulation
Power limiting
Excessive ripple
Radiated and conducted EMI
Destroy components in worst case

What Causes Layout Issues?

Changing currents through stray inductance produce unwanted voltages

$$V_{stray} = L_{stray}\frac{dI}{dt}$$

Changing voltages across stray capacitances produce unwanted currents.

$$I_{stray} = C_{stray}\frac{dV}{dt}$$

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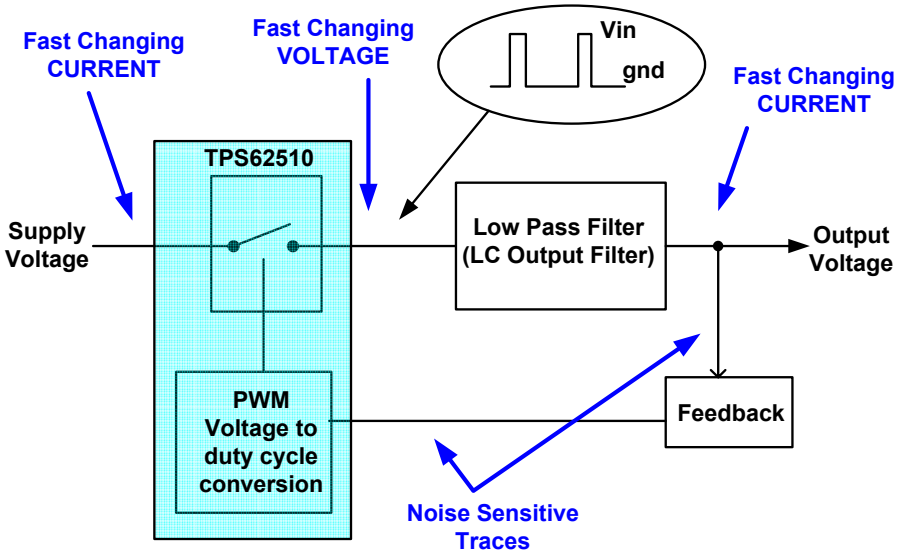
Power supplies require switching to convert power. This typically involves switching large currents. The current slew rate (di/dt) increases with increased switching frequency. High di/dt signals interact with stray inductance to produce unwanted or unexpected voltages.

High di/dt signals passing through a trace that forms a loop on the PCB will radiate EMI.

High switching frequencies also produce higher voltage slew rates (dv/dt) which interact with stray capacitance and produce unwanted current flows.

Review of SMPS - BUCK



Ground Bouncing

General High Frequency Board Layout Rules

Keep input capacitor close to the IC with low inductance traces.

Use single point grounding.

Isolate analog signal paths from power paths.

Keep trace from switching node pin to inductor short:

- Reduce EMI emissions and noise that may couple into other portions of the converter.

Output voltage feedback sampling must be taken right at output capacitor and shielded.

Always think about the parasitics!

Routing Rules (cont.)

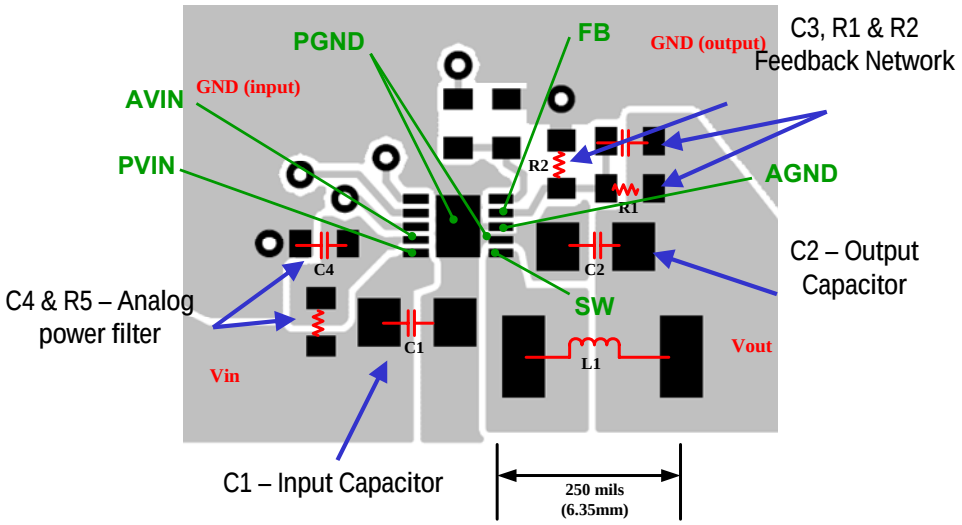
For high dv/dt signals keep copper to a minimum to prevent making unintentional parallel plate capacitors with other traces or to a ground plane. Best to route signal and return on same layer.

For high di/dt signals: keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to help prevent EMI.

Always avoid vias when possible. They have high inductance and resistance. If vias are necessary always use more than one in parallel to decrease parasitics.

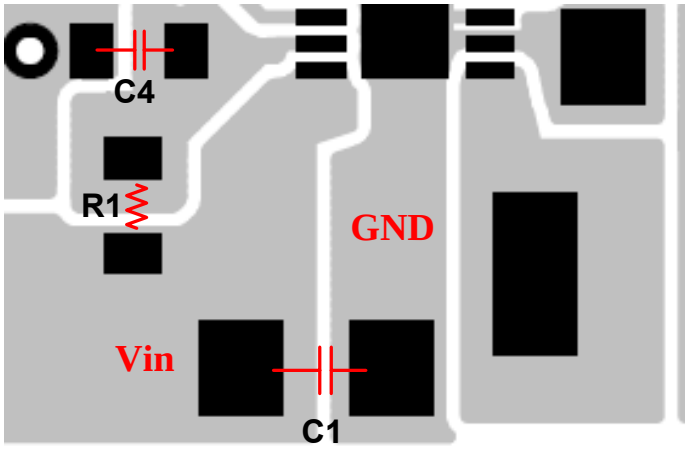
Do not use an auto-router or pour ground planes. Always manually route and pour grounds to keep single point grounding scheme and avoid current loops.

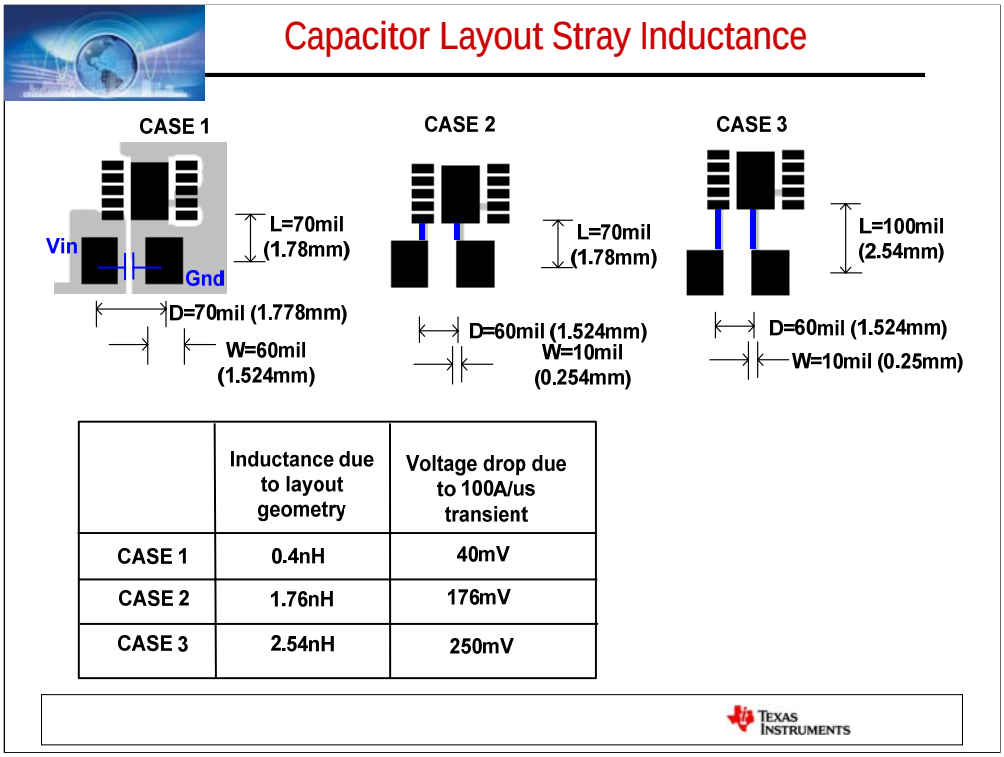
Good Layout – Base Line



Poor Input Capacitor Layout

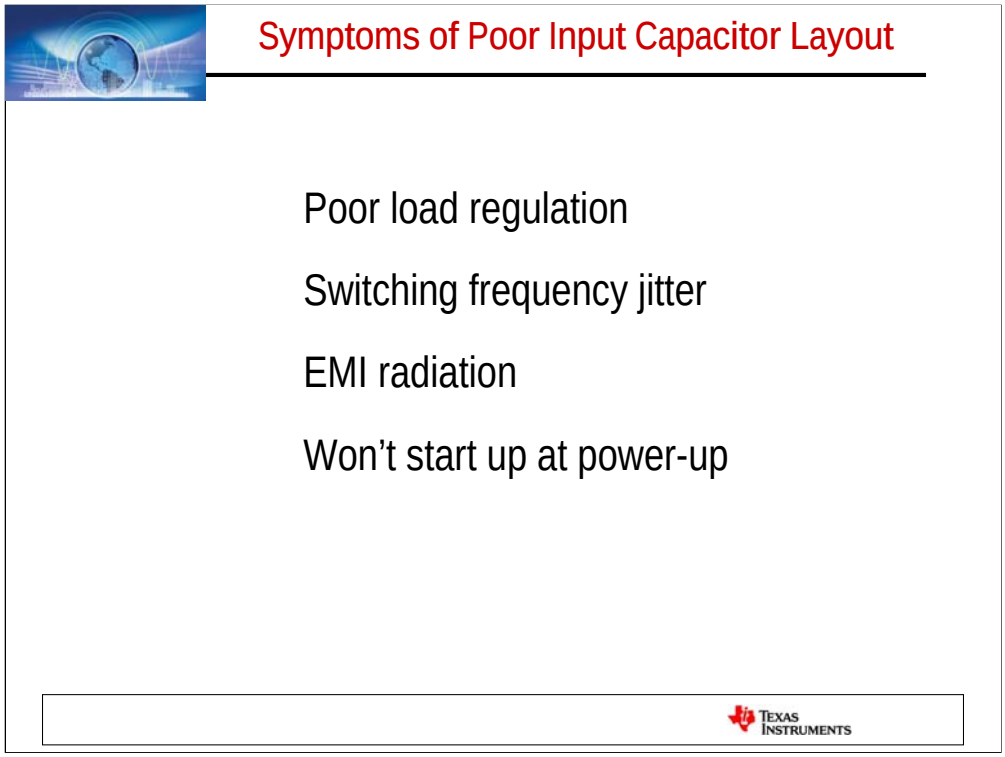
Input capacitor moved 110 mils farther from IC.





	Inductance due to layout geometry	Voltage drop due to 100A/us transient
CASE 1	0.4nH	40mV
CASE 2	1.76nH	176mV
CASE 3	2.54nH	250mV

This does not include the ESR or ESL of the capacitor or the bond wires. These could add another 1 - 2nH



Poor load regulation - can't get current into the gates of the Mosfets for fast turn-on

Switching frequency jitter - from noise injected into the internal bias supply

EMI radiation – ripple currents acting through loop antennas

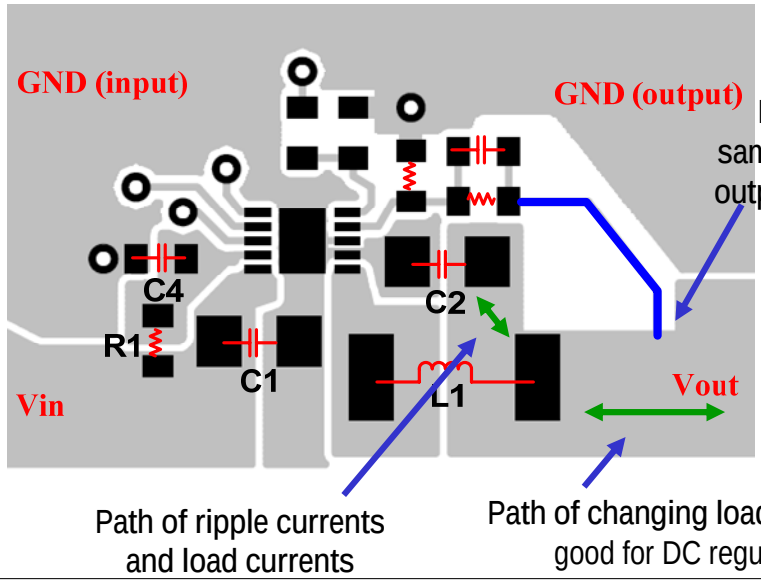
Won't start up at power-up - from noise injected into the internal bias supply

Layout Comparison

Measured Input Voltage Ripple

	Clock Jitter (ns)	Input Ripple (mV)	Load Regulation (%/A)
Base Line	13.5	140	0.07
Poor Input Capacitor	18	300	0.11

Poor Feedback Sampling

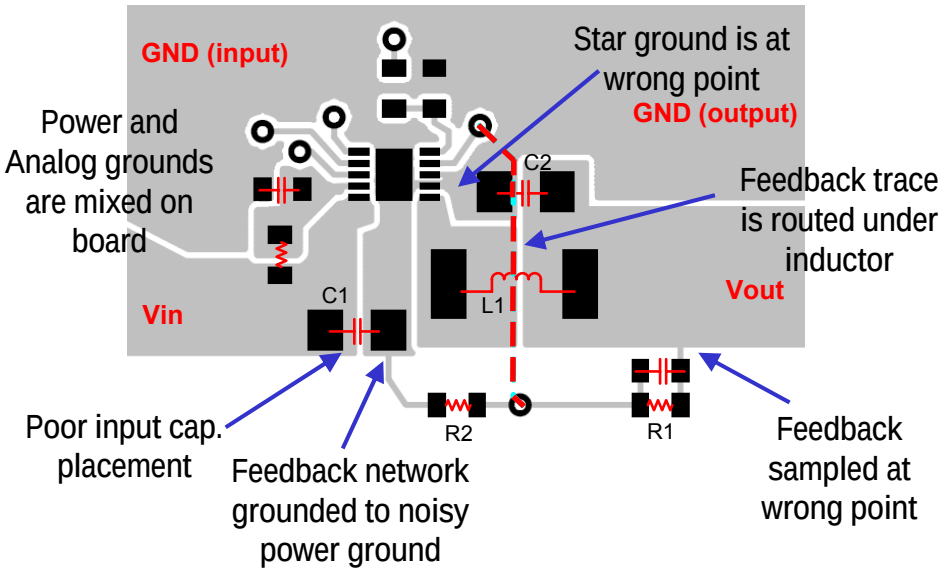


Symptoms of Poor Feedback Layout

Poor load regulation and load transient behavior.

	Load Regulation (%/A)	Output Droop due to Load Step (mV) No load to full load
Baseline	**0.07**	**120**
Poor Feedback	**0.19**	**220**

A Very Bad Layout



Bad Layout Problems

IC would not start up properly with load.

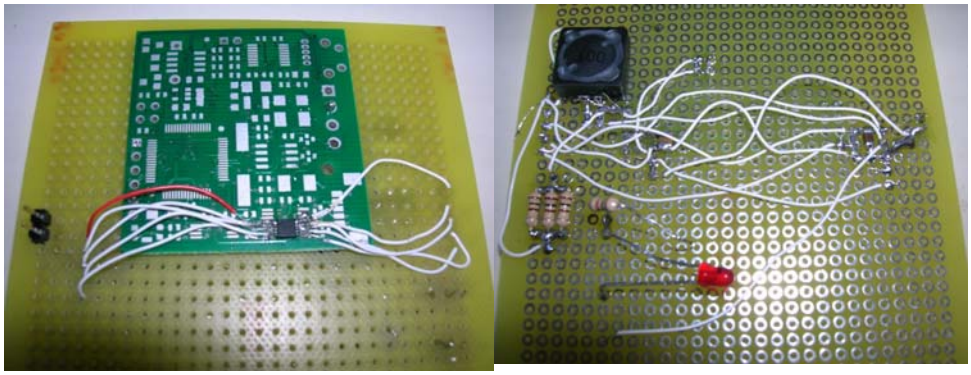
Would not regulate with load.

Two errors made the biggest impact for this layout.

- Routing the feedback trace path under the inductor.
- Poor grounding.

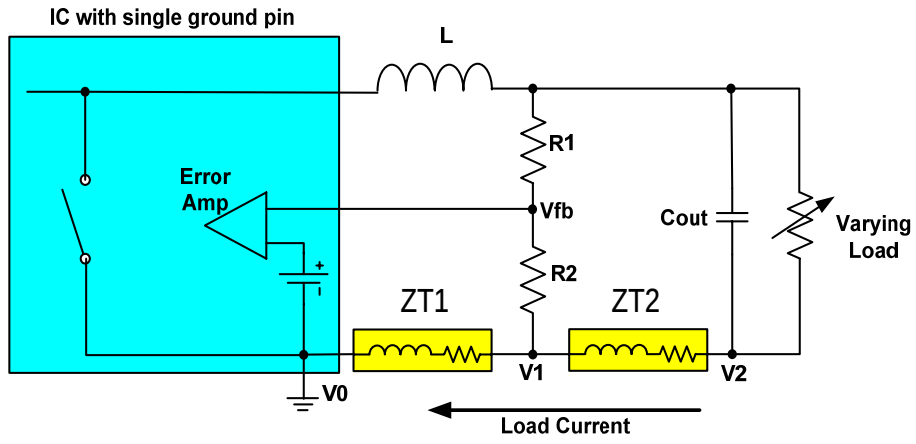
“Come on, nobody would do that ……”

Worst Case Layout



What's ~~wron~~g right with this layout?

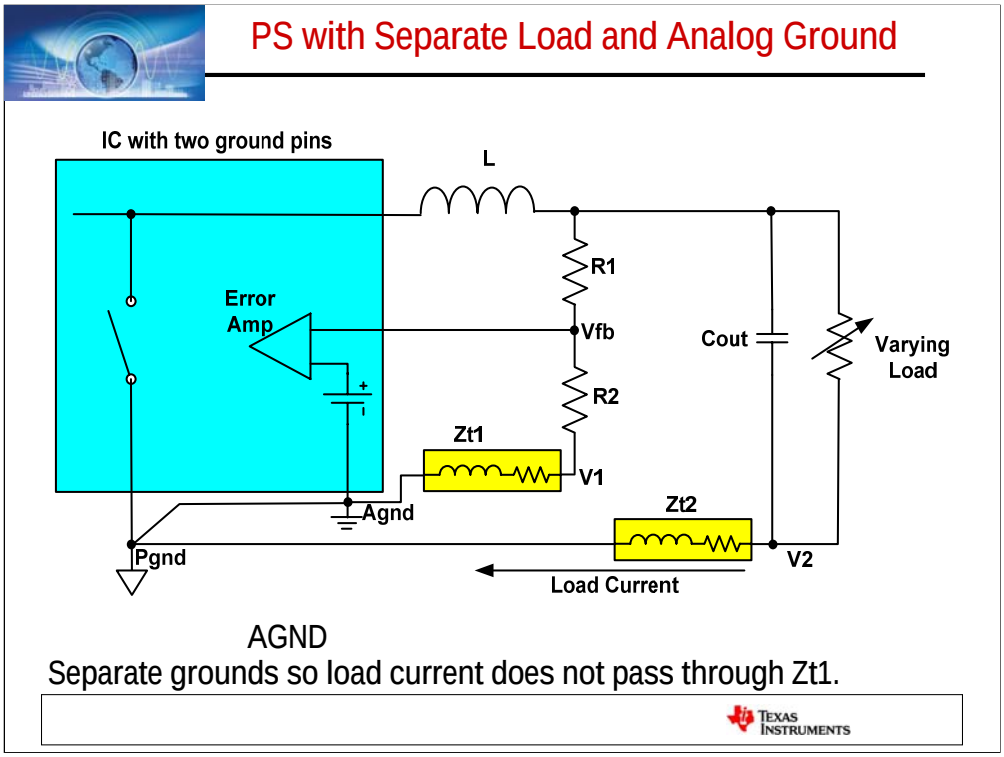
PS with Shared Load and Analog Ground



Changing load current act through ZT1 to produce output voltage error.

To maintain accurate regulation, voltage V1 needs to be at the same potential as V0. Changing load currents act through Zt1 which causes the voltage a V1 to change. This couples through R2 to induce errors in the feedback voltage Vfb and thus errors in the output.

This will typically lead to switching jitter and poor regulation.



IC with separate ground pins isolate the high load currents from the analog path. Agnd must be equal to PGND potential in order to maintain regulation. Agnd and PGND are tied together at the IC to keep potentials the same while keeping the paths isolated as much as possible.

Comparison of All Layout Examples

	Clock Jitter (ns)	Input Ripple (mV)	Load Regulation (%/A)	Output Droop due to Load Step (mV) No load to full load
Baseline	13.5	140	0.07	120
Poor Input Capacitor	18	300	0.11	125
Poor Feedback	14	140	0.19	220
All Bad	Does Not Operate			

Linear Regulator Solution

Advantage and Disadvantage of LDO

Advantages

+ Easier to use with few external components.
+ High Power Supply Ripple Rejection (PSRR).
+ Inexpensive (typically).
+ Quiet output - no switching noise.

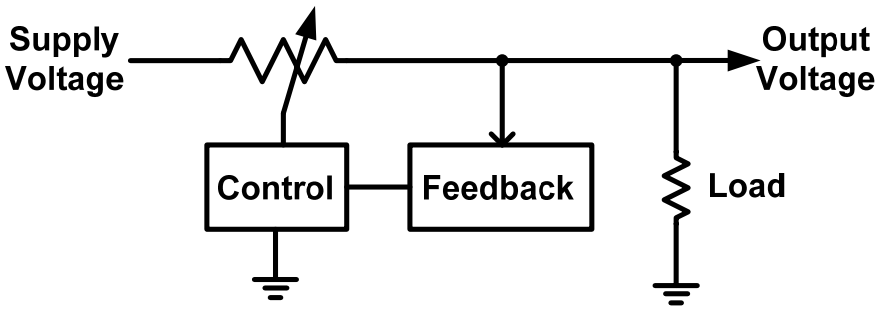
Disadvantages

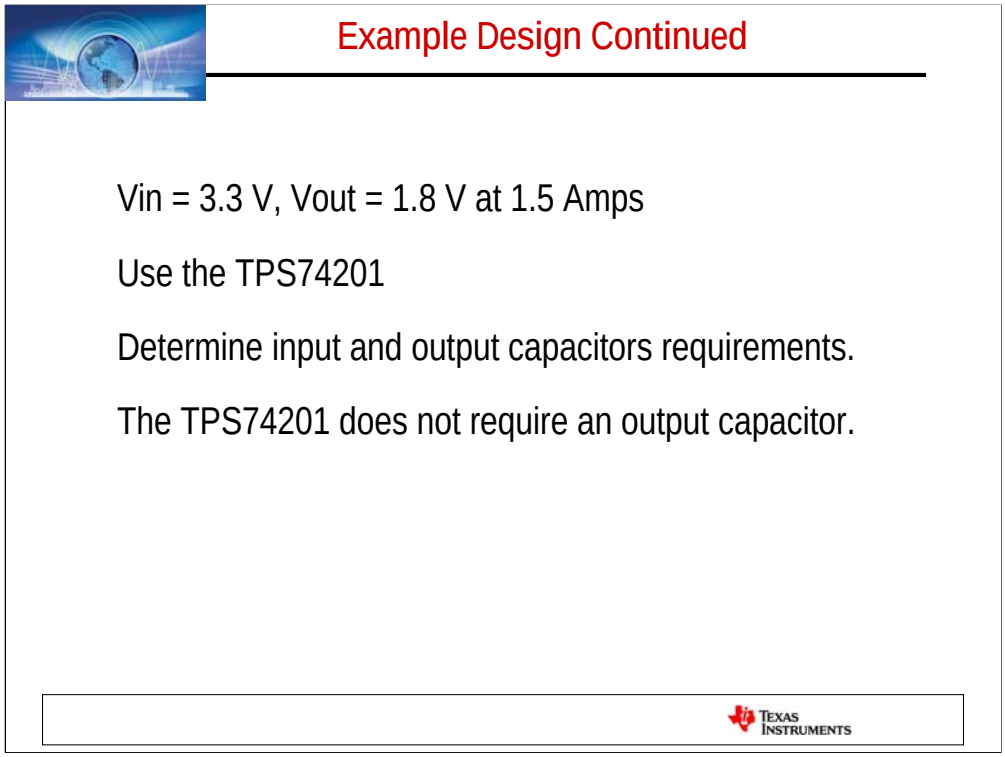
Poor efficiency for large input to output voltage ratios.

Large solution size due to heat sinking needs.

Review of Linear Operation

The Low Drop Out regulator (LDO) acts as a variable resistor in series with the load.





We first looked at converting 3.3V to 1.8V @ 1.5Amps using a switching power supply. Now we will do the same thing with a linear regulator.

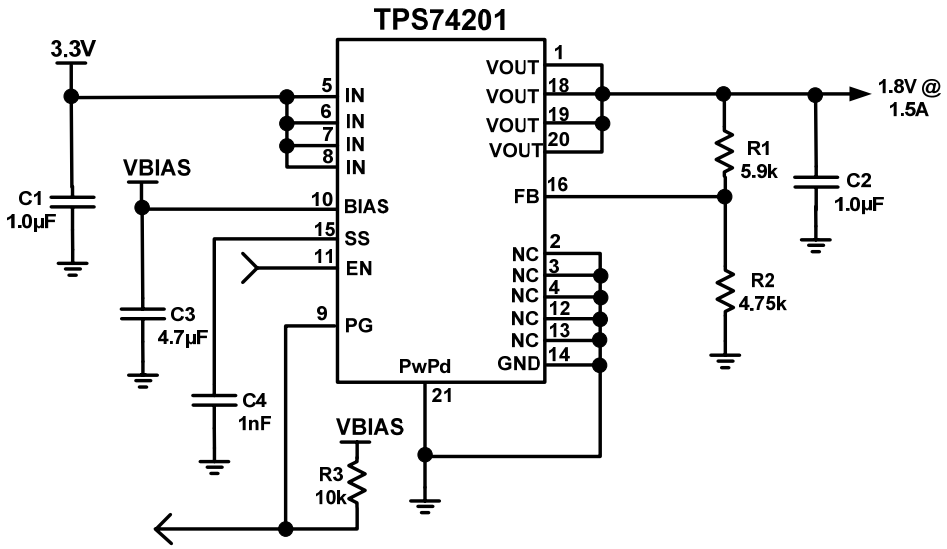
For this example, we will use the TPS74201 which is capable of providing 1.5Amp of output current.

Next, determine if input and output capacitors are required.

The datasheet states an input capacitor is required. Just like switching power supplies, a ceramic capacitor is the best choice due to its low ESR and ESL.

The TPS74201 does not require an output capacitor but is usually recommended to improve the converters response to transient loads. However, if an output capacitor is used, the TPS74201 is stable with any chemistry of output capacitor

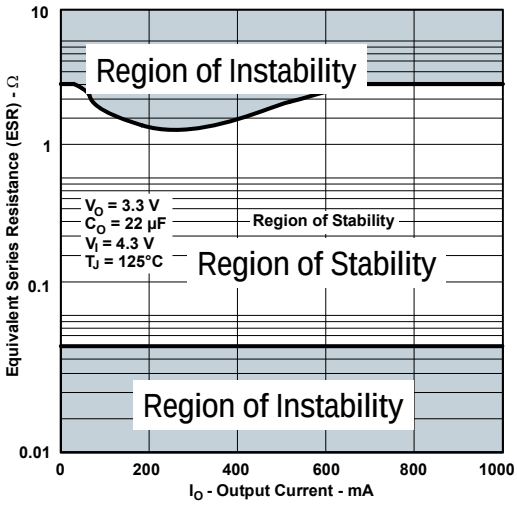
Linear Schematic



Output Capacitors

V_O = 3.3 V
C_O =22 µF
V_I = 4.3 V
T_J = 125°C

BE CAREFUL: Check Datasheet for output capacitor ESR requirements.



Example from the TPS76801 d/s

BE CAREFUL: Most linear regulators have ESR requirements for the output capacitor in order to maintain stability. This will be stated in the datasheet. There is usually a graph of the range of ESR allowed.

Linear Power Dissipation

- All of the load current passes through the linear regulator.
- The power dissipated by the linear regulator is:

$$P_{DISP}=(V_{IN}-V_{OUT})I_{LOAD}$$

For V_{IN} = 3.3, V_{OUT} = 1.8 and I_{OUT} = 1.5 A, P_{DISP} = 2.25 W.
Select a package that can support the power dissipation.

Package	θ_{JA}	θ_{JC}	TA < 25°C Power Rating	Derating Factor Above 25°C
QFN	36.5° C/W	4.05° C/W	2.74 W	27.4 mW/°C
DDPAK	36.5° C/W	2.32° C/W	5.32 W	27.4 mW/°C

Package Selection

Package	θ_{JA}	θ_{JC}	$T_A < 25^oC$ Power Rating	Derating Factor Above 25°C
QFN	36.5°C/W	4.05°C/W	2.74 W	27.4 mW/°C
DDPAK	36.5°C/W	2.32°C/W	5.32 W	27.4 mW/°C

Calculate the maximum power dissipation allowed for T > 25°C.

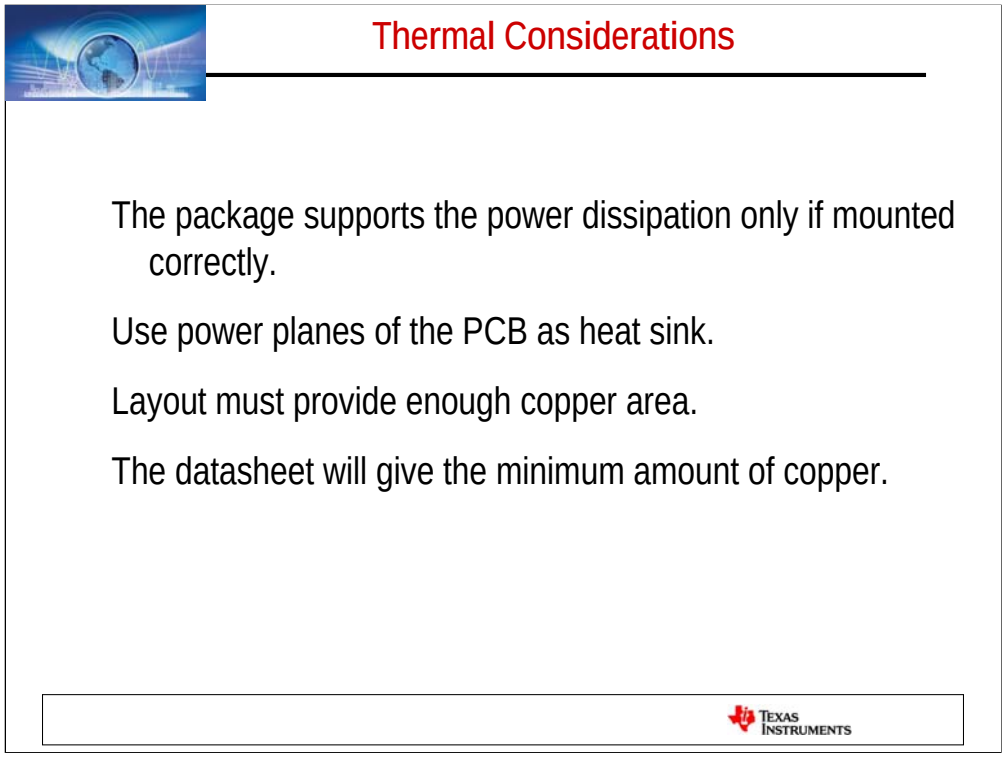
$$P_{maxT_A} = P_{max25C} - (T_A - 25) \bullet (derate)$$

- How much power can each package support if T_A > 35°C?

$P_{QFN} = 2.74 - (35 - 25) \bullet 0.0274 = 2.466$ W

$P_{DDPAK} = 5.32 - (35 - 25) \bullet 0.0274 = 4.788$ W

- Either can support the 2.25 W dissipation with T_A = 35°C. Use the QFN for the smallest size.



The package supports the power dissipation but only if soldered to an appropriate heat sink.

Usually, the power planes of the PCB are used as a heat sink. The heat from the regulator is conducted to the planes which then conduct or radiate the heat away to the ambient environment.

The layout must provide enough copper to adequately move the heat (thermal energy) away from the regulator.

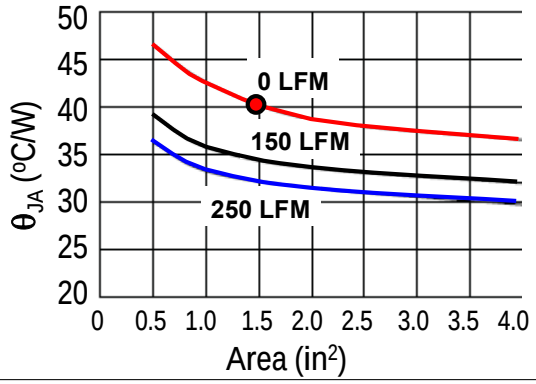
The datasheet will give guidelines on the minimum amount of copper.

Required Copper Area

Use the T_{JMAX}, T_A and P_{DISP} to calculate an effective Θ_{JA}.

$$\theta_{JA} = \frac{T_{max} - T_A}{P_{DISP}} = \frac{125°C - 35°C}{2.25W} = 40°C/W$$

- Need 1.5 in^2 copper to achieve 40°C/W with no air flow.



Linear Layout

All layout rules for the SMPS apply to the linear regulator.

Linear load currents do not pass through the ground pin of the IC.

Poor layout can still produce output noise during load transients.

Need layout that follows the rules and still has good thermal performance.

Texas Instruments

All of the layout rules for the switching power supply still apply to the linear regulator.

Only major difference is that the load currents do not pass through the ground pin of the linear regulator.

The linear regulator does not have switch noise but can still produce noise during transients if the layout is poor.

The challenge is to provide a layout that follows the rules and still has good thermal performance.

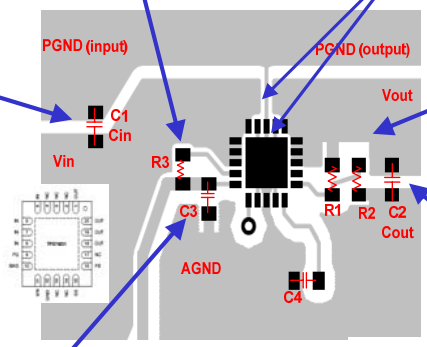
Poor Linear Regulator Layout

Thin Connections to ground make poor thermal performance

Input Capacitor has high impedance path

PG Pull up

Input Cap



Feedback Network

Output Cap

V_{bias} Cap

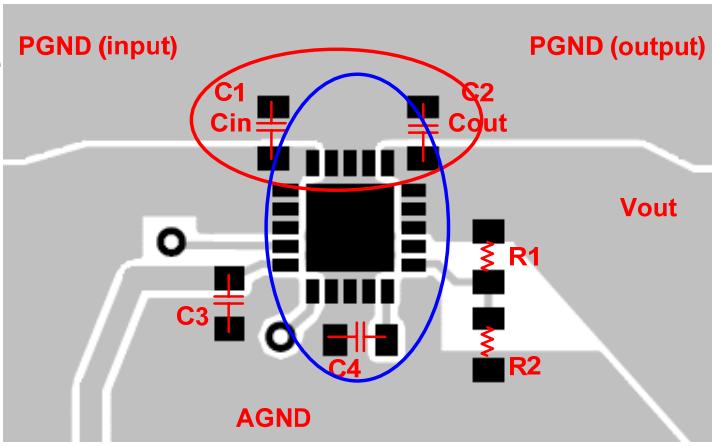
Output Capacitor has high impedance path and is tied to wrong ground point

Good Linear Layout

Thermal pad of IC connects to ground plane with large area traces for good thermal performance

Good placement of input and output capacitors. Large traces large with low impedance

Separate Analog and power grounds and connected at one point



Conclusions

A successful power supply design involves appropriate component selection to achieve optimum results.

Even with all components selected correctly, the performance of the converter can be compromised by poor layout.

There are several basic layout rules that should be followed. These rules apply to both switching power supplies and linear regulators.

The layout of the linear regulator must take thermal performance into account.

Appendix A: Common PCB Parameters

Copper Weight	Copper Thickness	
1/2 oz	0.7 mil	17 um
1 oz	1.4 mil	35 um
2 oz	2.4 mil	70 um

Standard Board Thickness		
1/32"	31.2 mil	0.8 mm
1/16"	62.5 mil	1.6 mm
1/10"	100 mil	2.4 mm
1/8"	125 mil	3.2 mm

Material	Єr
Standard FR4	4.1
Tetra Functional FR4	4.1
Standard FR2	4.5
Nelco N4000-6	4
Getek	3.9
BT Epoxy Glass	4.1
Cyanate Ester	3.8
Polymide Glass	4.1
Teflon	2.2

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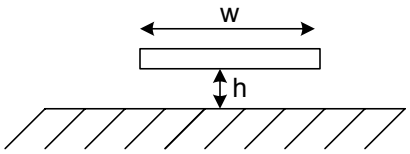
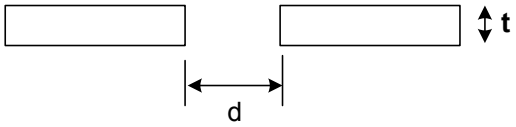
Appendix B: Capacitance of Common PCB Structures

Trace over trace or ground plane



$$\frac{C}{l} \approx \frac{8.854\varepsilon_r w}{h} \quad \text{(pF/m)}$$

Co-planar traces

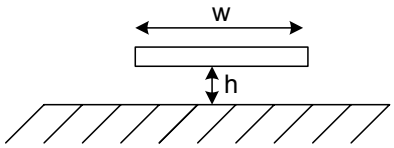


$$\frac{C}{l} \approx \frac{8.854t}{d} \quad \text{(pF/m)}$$

Dimensions can be any units but must be the same. For example, if w is in mils then h must also be in mils.

Appendix C: Inductance of Common PCB Structures

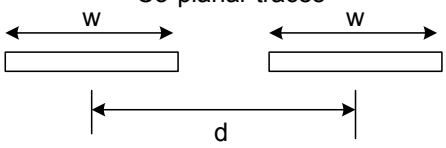
Trace over ground plane



$$\frac{L}{l} \approx \frac{\mu_0 h}{w}$$

In H/m, h and w can be any units as long as they are the same.

Co-planar traces



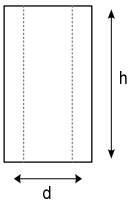
$$\frac{L}{l} \approx \frac{\mu_0}{\pi} \cosh^{-1}\left(\frac{d}{w}\right)$$

In H/m, d and w can be any units as long as they are the same.

$$\mu_0 = 4\pi \cdot 10^{-7}$$

Appendix C: Inductance of Common PCB Structures

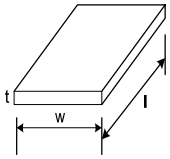
Via



$$L = 5.08h\left[\ln\left(\frac{4h}{d}\right)+1\right]$$

Answer in nH, h and d are in inches

Single Trace



$$L = 5l\left[\ln\left(\frac{l}{t+w}\right)+0.5\right]$$

Answer in nH, t, l and w are in inches