



Op Amp Stone Soup

A “Cookbook” Collection of Single Supply Op Amp Circuits



Tim Green
Linear Applications Manager
Tucson Division
green_tim@ti.com



Op Amp Stone Soup:

This presentation will offer a "Stone Soup" collection of useful op amp circuits to solve linear application problems on a daily basis. Each op amp circuit (pre-built in the included TINA SPICE schematic) is presented as a definition-by-example with a brief overview of its functionality, applicable transfer function and/or waveforms and key equations for re-scaling the function to your exact application. A sampling of the ingredients include the following circuits: Voltage-to-Current Conversion, Drive Circuits (Bridge-Tied-Load, Parallel Op Amps, High Current Cascade Reference Buffer), Translation Circuits (Single-Ended to Differential, Differential to Single-Ended, Differential In to Differential Out), Conditioning Circuits (Full-Wave Rectifier, Supply Splitter, Integrator Amp in Feedback, Isolation Amplifier, $G=1/G=-1$ amp), and Comparator Circuits (AC Coupled, Comparator with Hysteresis).

These are built specifically for single-supply applications which require special considerations often not needed when dual supply op amps are available. Any engineer interfacing with customers will find these op amp building blocks invaluable and ready to run on TINA SPICE right out of the pot.



The Story of Stone Soup

Some travelers come to a village, carrying nothing more than an empty pot. Upon their arrival, the villagers are unwilling to share any of their food stores with the hungry travelers. The travelers fill the pot with water, drop a large stone in it, and place it over a fire in the village square. One of the villagers becomes curious and asks what they are doing. The travelers answer that they are making "stone soup", which tastes wonderful, although it still needs a little bit of garnish to improve the flavor, which they are missing. The villager doesn't mind parting with just a little bit to help them out, so it gets added to the soup. Another villager walks by, inquiring about the pot, and the travelers again mention their stone soup which hasn't reached its full potential yet. The villager hands them a little bit of seasoning to help them out. More and more villagers walk by, each adding another ingredient. Finally, a delicious and nourishing pot of soup is enjoyed by all.

"Stone Soup" is a Grimm Brothers fable. Source: Wikipedia

http://en.wikipedia.org/wiki/Stone_soup



Much like the fable of "Stone Soup" this presentation started as an "empty pot" with many curious villagers (Linear Applications Engineers) eager to throw in a special ingredient of their own. Hope you enjoy the resulting pot full of op amp circuits.



Discrete Transistor Review

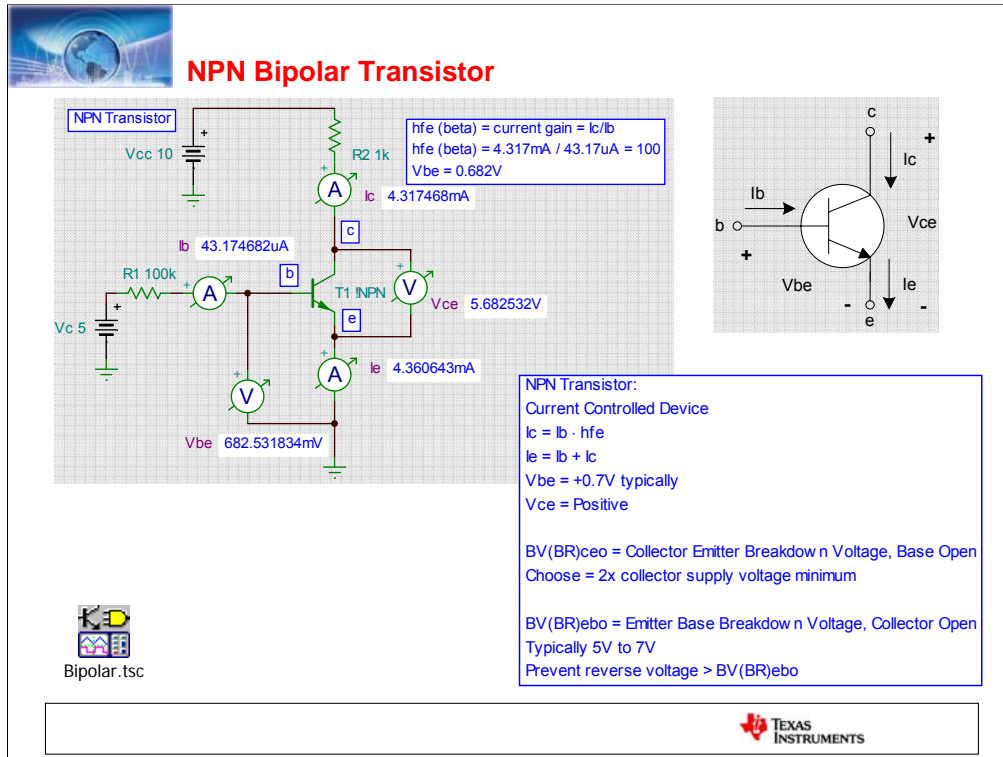
Bipolar Transistors: NPN & PNP

Depletion Mode JFETs: N-Channel & P-Channel

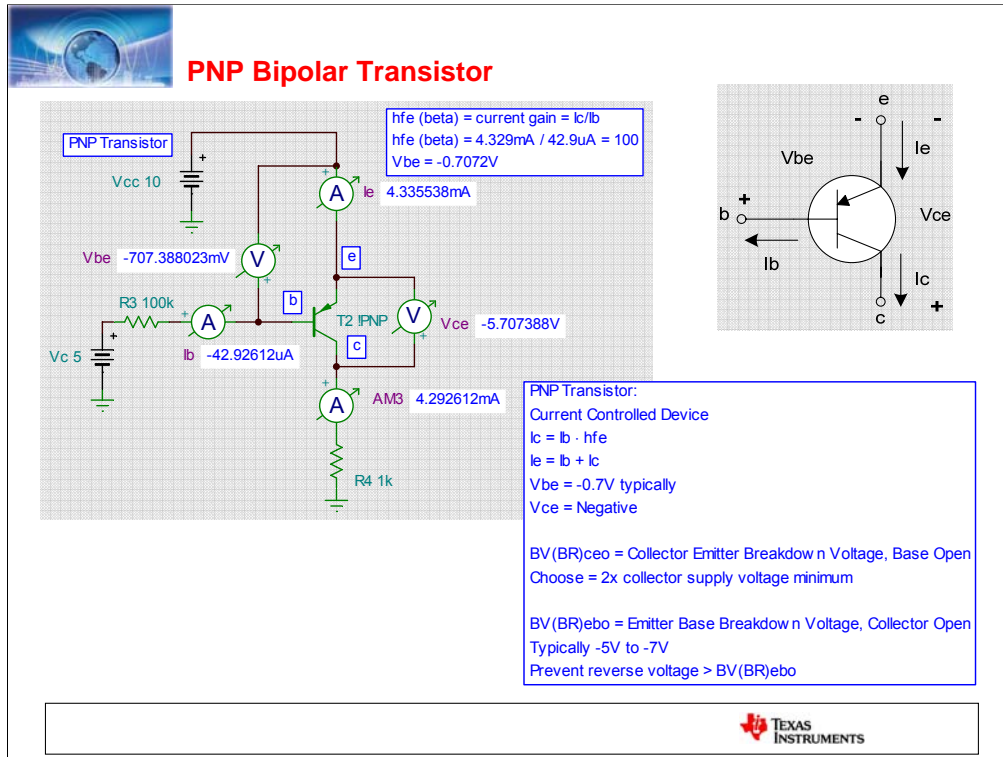
Enhancement Mode MOSFETs: N-Channel & P-Channel



Before we look at our single supply circuits we will do a brief overview of common discrete transistors that are often required to help in single supply op amp applications.



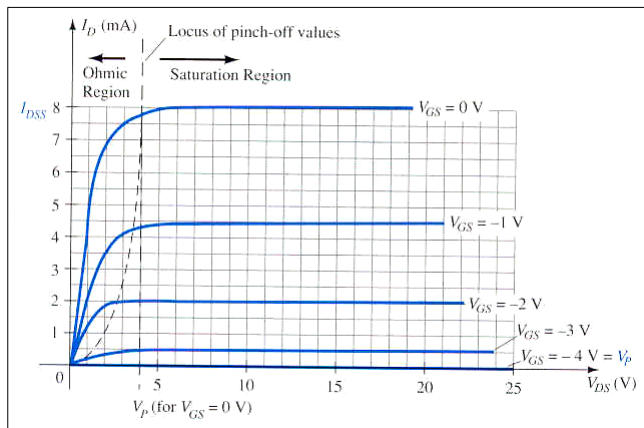
The NPN Bipolar Transistor is a current controlled device. It requires a base-emitter forward voltage drop to begin to conduct current through the base-emitter junction which will then be gained up to the collector. Emitter current is a summation of collector current plus base current. For proper operation the NPN transistor must have a positive base emitter voltage and a positive collector-emitter voltage as current flows from collector through emitter.



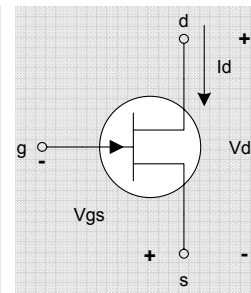
The PNP Bipolar Transistor is a current controlled device. It requires a base-emitter forward voltage drop to begin to conduct current through the base-emitter junction which will then be gained up to the collector. Emitter current is a summation of collector current plus base current. For proper operation the PNP transistor must have a negative base emitter voltage and a negative collector-emitter voltage as current flows from emitter through collector.



N-Channel Depletion Mode JFET



Ohmic Region = Triode Region
Saturation Region = Pinch-off Region



N_jfet.tsc



N-Channel Depletion Mode JFETs are fully turned on with $V_{GS} = 0$ V and it takes a negative V_{GS} to turn the device off. They are voltage controlled devices with no gate current flow when they are properly biased. For normal operation the gate-source junction and gate-drain junction must both be reversed biased. In the triode region the JFET can be used as a voltage-controlled resistor.



N-Channel Depletion Mode JFET: $V_{gs} = 0V$

N-Channel Depletion Mode JFET
Voltage Controlled Device

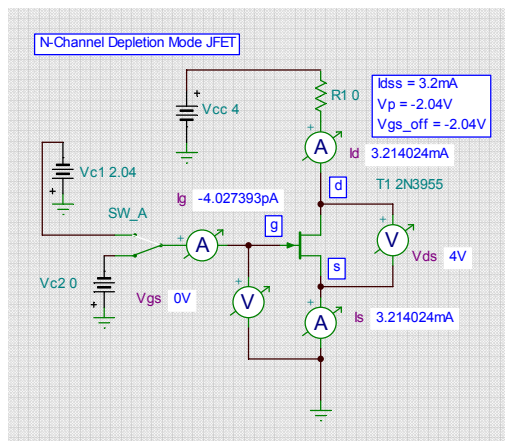
V_{gs_off} = Negative Voltage
 V_{gs_on} = 0V
 I_{dss} = Drain Saturation Current

V_{gd} must be negative to keep reverse biased

I_d is proportional to V_{gs} and V_{ds}
 $I_d = I_s$ (Current flow from I_d to I_s)
 $I_g = 0A$

V_p = Negative for N-Channel JFET
 V_p = Pinch-off Voltage which determines either:
Triode Region (ohmic): $V_p < V_{gs} < 0V$, $V_{ds} < V_{gs} - V_p$
Saturation (pinch-off) Region: $V_p < V_{gs} < 0V$, $V_{ds} > V_{gs} - V_p$

V_{gd} = Gate to Drain Breakdown Voltage
 $V_{gs(r)}$ Reverse Gate to Source Breakdown Voltage
Usually $V_{gd} = V_{gs(r)}$
Choose = 2x max voltage minimum of:
Maximum of Drain Voltage or Gate Voltage





N-Channel Depletion Mode JFET: $V_{gs} = -2.04V$

N-Channel Depletion Mode JFET
Voltage Controlled Device

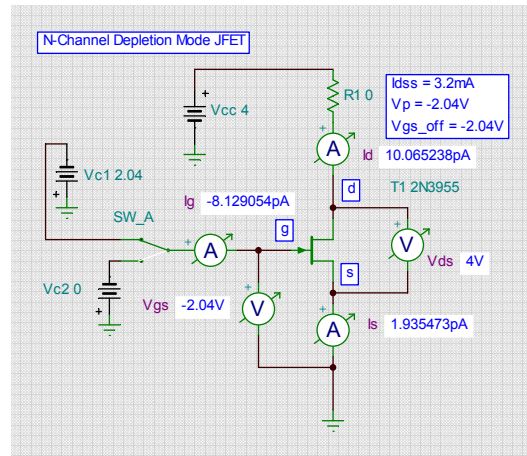
V_{gs_off} = Negative Voltage
 V_{gs_on} = 0V
 I_{dss} = Drain Saturation Current

V_{gd} must be negative to keep reverse biased

I_d is proportional to V_{gs} and V_{ds}
 $I_d = I_s$ (Current flow from I_d to I_s)
 $I_g = 0A$

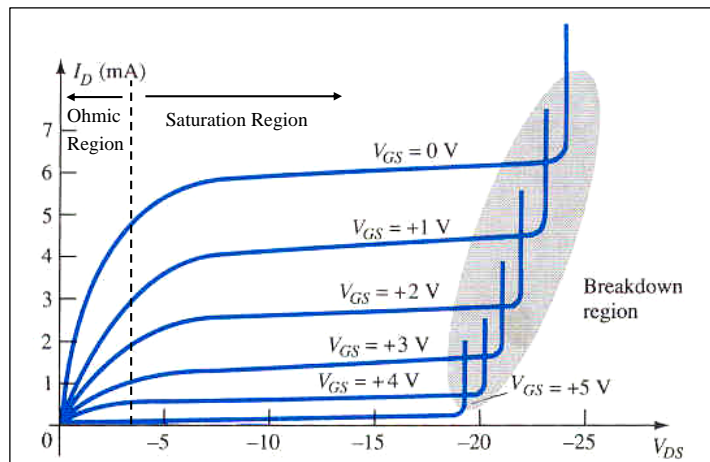
V_p = Negative for N-Channel JFET
 V_p = Pinch-off Voltage which determines either:
Triode Region (ohmic): $V_p < V_{gs} < 0V$, $V_{ds} < V_{gs} - V_p$
Saturation (pinch-off) Region: $V_p < V_{gs} < 0V$, $V_{ds} > V_{gs} - V_p$

V_{gd} = Gate to Drain Breakdown Voltage
 $V_{gs(r)}$ Reverse Gate to Source Breakdown Voltage
Usually $V_{gd} = V_{gs(r)}$
Choose = 2x max voltage minimum of:
Maximum of Drain Voltage or Gate Voltage

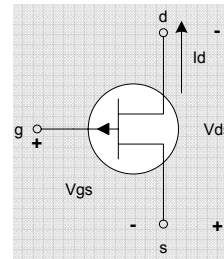




P-Channel Depletion Mode JFET



Ohmic Region = Triode Region
Saturation Region = Pinch-off Region



P_jfet.tsc



P-Channel Depletion Mode JFETs are fully turned on with $V_{GS} = 0V$ and it takes a positive V_{GS} to turn the device off. They are voltage controlled devices with no gate current flow when they are properly biased. For normal operation the gate-source junction and gate-drain junction must both be reversed biased. In the triode region the JFET can be used as a voltage-controlled resistor.



P-Channel Depletion Mode JFET: $V_{gs} = 0V$

P-Channel Depletion Mode JFET
Voltage Controlled Device

V_{gs_off} = Positive Voltage

$V_{gs_on} = 0V$

I_{dss} = Drain Saturation Current

I_d is proportional to V_{gs} and V_{ds}

$I_d = I_s$ (Current flow from I_s to I_d)

$I_g = 0A$

V_p = Positive for P-Channel JFET

V_p = Pinch-off Voltage which determines either:

Triode Region (ohmic): $0V < V_{gs} < V_p$, $V_{ds} > V_{gs} - V_p$

Saturation (pinch-off) Region: $0V < V_{gs} < V_p$, $V_{ds} < V_{gs} - V_p$

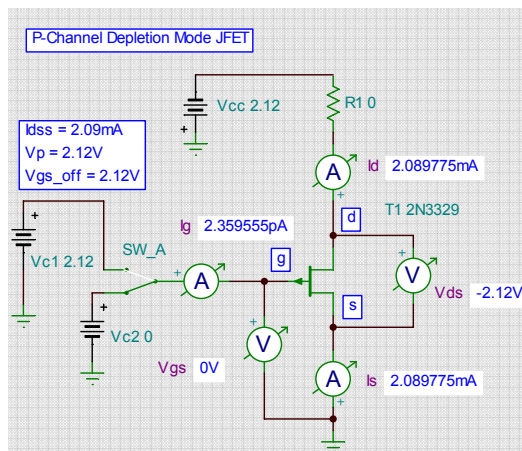
V_{gd} = Gate to Drain Breakdown Voltage

$V_{gs(r)}$ Reverse Gate to Source Breakdown Voltage

Usually $V_{gd} = V_{gs(r)}$

Choose = 2x max voltage minimum of:

Maximum of Drain Voltage or Gate Voltage





P-Channel Depletion Mode JFET: $V_{gs} = 2.12V$

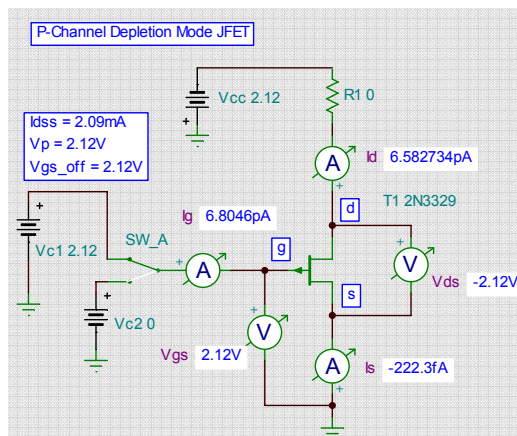
P-Channel Depletion Mode JFET
Voltage Controlled Device

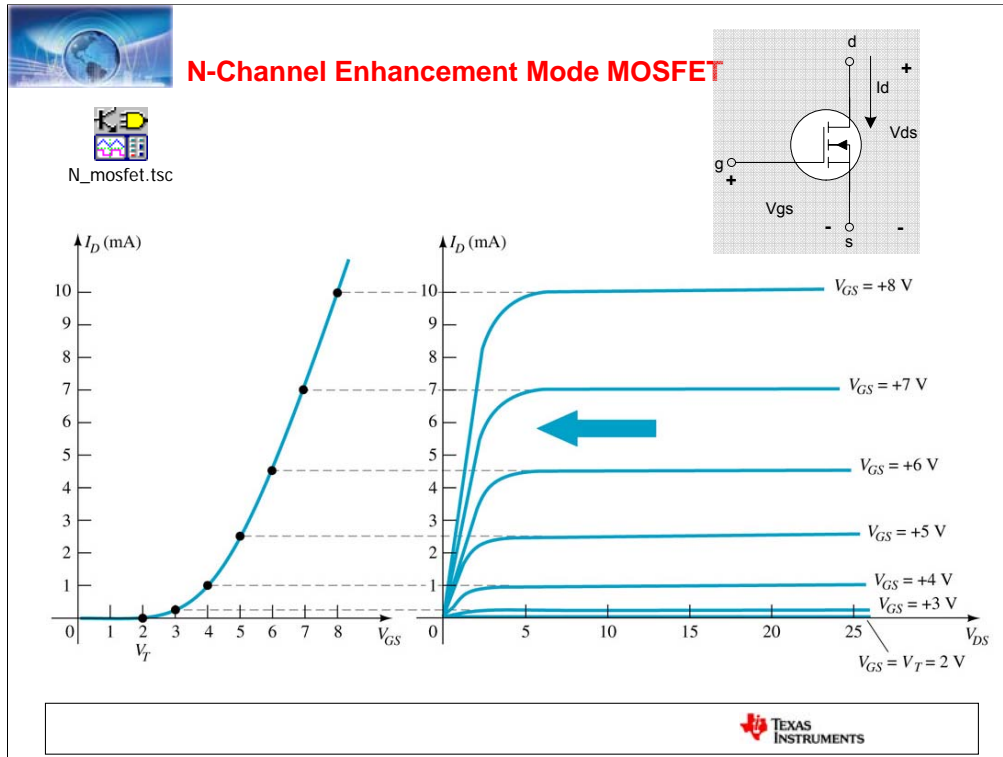
V_{gs_off} = Positive Voltage
 $V_{gs_on} = 0V$
 I_{dss} = Drain Saturation Current

I_d is proportional to V_{gs} and V_{ds}
 $I_d = I_s$ (Current flow from I_s to I_d)
 $I_g = 0A$

V_p = Positive for P-Channel JFET
 V_p = Pinch-off Voltage which determines either:
Triode Region (ohmic): $0V < V_{gs} < V_p$, $V_{ds} > V_{gs} - V_p$
Saturation (pinch-off) Region: $0V < V_{gs} < V_p$, $V_{ds} < V_{gs} - V_p$

V_{gd} = Gate to Drain Breakdown Voltage
 $V_{gs(r)}$ Reverse Gate to Source Breakdown Voltage
Usually $V_{gd} = V_{gs(r)}$
Choose = 2x max voltage minimum of:
Maximum of Drain Voltage or Gate Voltage





N-Channel Enhancement Mode MOSFETs are voltage controlled devices with a positive V_{GS} turning them on and $V_{GS} = 0$ turning them off. The gate-source junction must NOT be subjected to over-voltage or permanent damage can occur. In the triode region the MOSFET can be used as a voltage-controlled resistor similar to the Depletion Mode JFET with the advantage that current does not flow if gate-source or drain-gate junctions are reverse biased.



N-Channel Enhancement Mode MOSFET: $V_{gs} = 0V$

N-Channel Enhancement Mode MOSFET
Voltage Controlled Device

$V_{gs_off} = 0V$

V_{gs_on} = Positive Voltage

$V_{gs(th)}$ = start of MOSFET turn-on

I_{dss} = Drain Saturation Current

I_{dss} = max current flow for fixed V_{gs} with varying V_{ds}

I_d is proportional to V_{gs} and V_{ds}

$I_d = I_s$ (Current flow from I_s to I_d)

$I_g = 0A$

$V_{ds(max)}$ = Maximum drain to source voltage

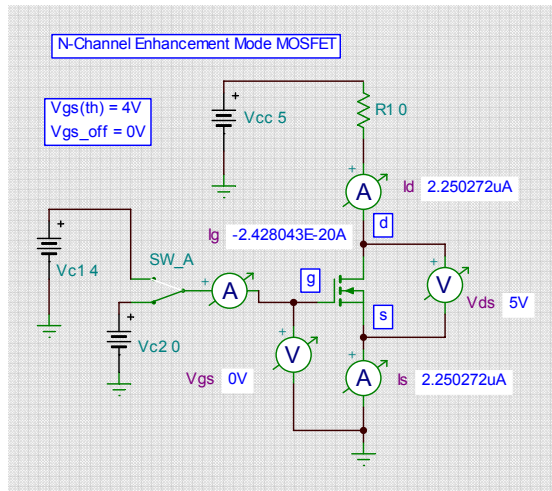
Choose $V_{ds(max)} = 2 \times$ supply voltage

$V_{gs(max)}$ = maximum gate to source voltage

Do not exceed $V_{gs(max)}$ or device is destroyed

$I_d(max)$ = maximum drain current

Choose $I_d(max) = 2 \times$ maximum load current





N-Channel Enhancement Mode MOSFET: $V_{gs} = 4V$

N-Channel Enhancement Mode MOSFET
Voltage Controlled Device

$V_{gs_off} = 0V$

V_{gs_on} = Positive Voltage

$V_{gs(th)}$ = start of MOSFET turn-on

I_{dss} = Drain Saturation Current

I_{dss} = max current flow for fixed V_{gs} with varying V_{ds}

I_d is proportional to V_{gs} and V_{ds}

$I_d = I_s$ (Current flow from I_s to I_d)

$I_g = 0A$

$V_{ds(max)}$ = Maximum drain to source voltage

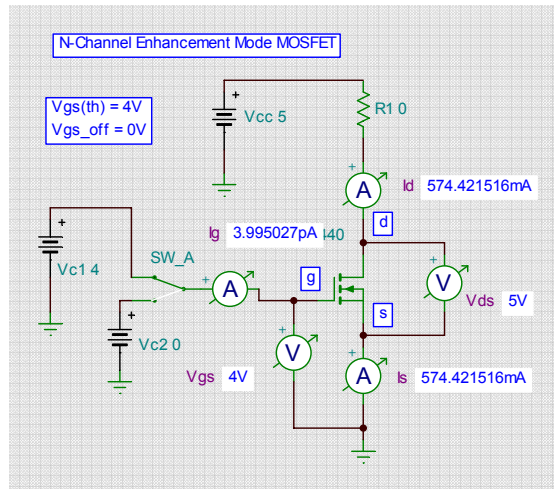
Choose $V_{ds(max)} = 2 \times$ supply voltage

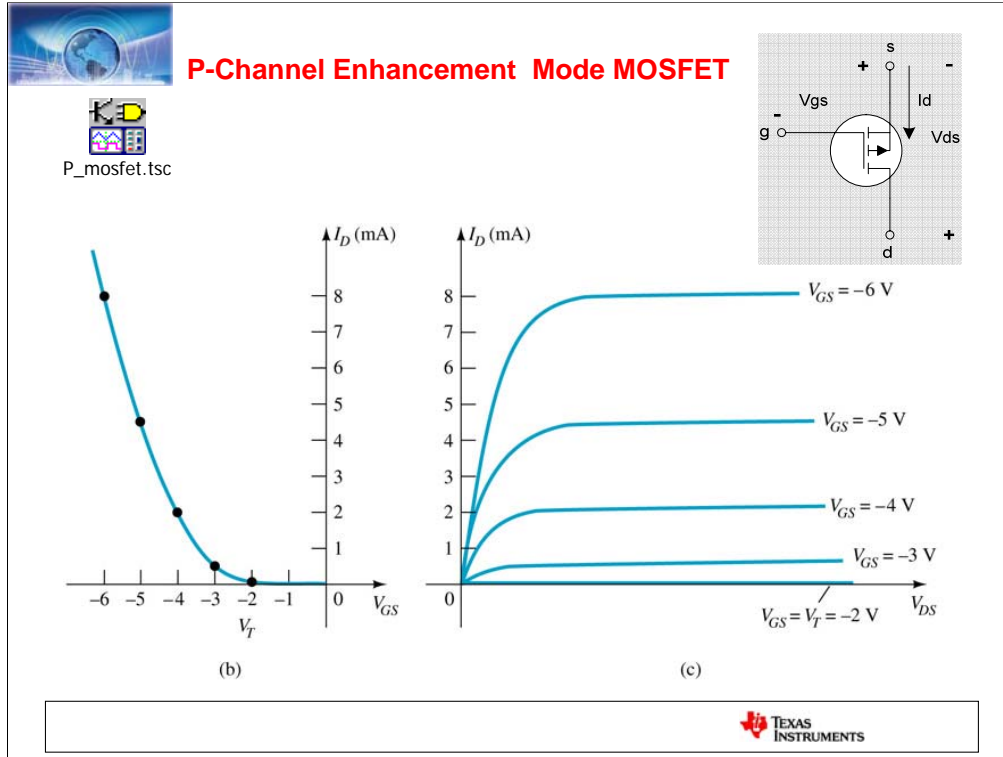
$V_{gs(max)}$ = maximum gate to source voltage

Do not exceed $V_{gs(max)}$ or device is destroyed

$I_d(max)$ = maximum drain current

Choose $I_d(max) = 2 \times$ maximum load current





P-Channel Enhancement Mode MOSFETs are voltage controlled devices with a negative V_{GS} turning them on and $V_{GS} = 0$ turning them off. The gate-source junction must NOT be subjected to over-voltage or permanent damage can occur. In the triode region the MOSFET can be used as a voltage-controlled resistor similar to the Depletion Mode JFET with the advantage that current does not flow if gate-source or drain-gate junctions are reverse biased.



P-Channel Enhancement Mode MOSFET: $V_{gs} = 0V$

P-Channel Enhancement Mode MOSFET
Voltage Controlled Device

$V_{gs_off} = 0V$

V_{gs_on} = Negative Voltage

$V_{gs(th)}$ = start of MOSFET turn-on

I_{dss} = Drain Saturation Current

I_{dss} = max current flow for fixed V_{gs} with varying V_{ds}

I_d is proportional to V_{gs} and V_{ds}

$I_d = I_s$ (Current flow from I_s to I_d)

$I_g = 0A$

$V_{ds(max)}$ = Maximum drain to source voltage

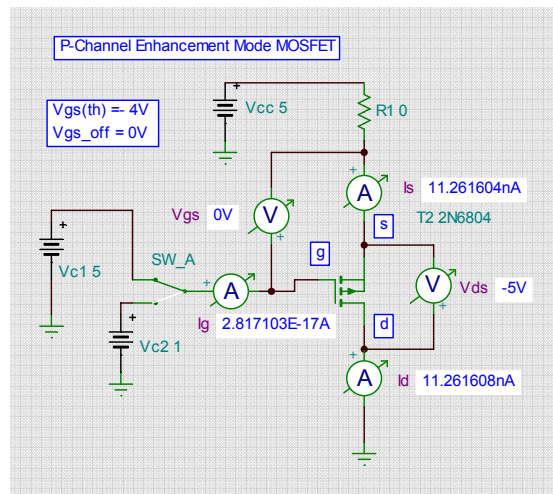
Choose $V_{ds(max)} \approx 2 \times$ supply voltage

$V_{gs(max)}$ = maximum gate to source voltage

Do not exceed $V_{gs(max)}$ or device is destroyed

$I_d(max)$ = maximum drain current

Choose $I_d(max) \approx 2 \times$ maximum load current





P-Channel Enhancement Mode MOSFET: $V_{gs} = -4V$

P-Channel Enhancement Mode MOSFET

Voltage Controlled Device

$V_{gs_off} = 0V$

V_{gs_on} = Negative Voltage

$V_{gs(th)}$ = start of MOSFET turn-on

I_{dss} = Drain Saturation Current

I_{dss} = max current flow for fixed V_{gs} with varying V_{ds}

I_d is proportional to V_{gs} and V_{ds}

$I_d = I_s$ (Current flow from I_s to I_d)

$I_g = 0A$

$V_{ds(max)}$ = Maximum drain to source voltage

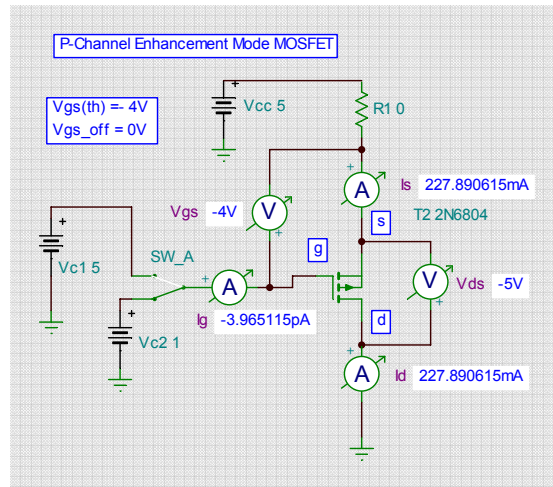
Choose $V_{ds(max)} \approx 2 \times$ supply voltage

$V_{gs(max)}$ = maximum gate to source voltage

Do not exceed $V_{gs(max)}$ or device is destroyed

$I_d(max)$ = maximum drain current

Choose $I_d(max) \approx 2 \times$ maximum load current





Voltage-to-Current Circuits
Drive Circuits
Translation Circuits
Conditioning Circuits
Comparator Circuits



Voltage-to-Current Circuits

V-I High Side Referenced

V-I Low Side Referenced

V-I Improved Howland Current Pump



V-I High Side Referenced Given:

Design Goal:

$V_{cc} = +5V$

$V_{in} = 0V \text{ to } 1V \rightarrow I_{out} = 0 \text{ to } 100mA$

$R_{load} = 40 \text{ ohms}$, Grounded Load

1% FSR accuracy in transfer function (I_{out}/V_{in})

Design Considerations:

Need to Sense current in High Side

Need to level shift V_{in} to control High Side Current

Need a Power Device & RRIO op amp for sense and control

Design Preliminary Analysis:

Use N-Channel MOSFET for Level Shifting

Use P-Channel MOSFET for High Side Current Control

$V_{headroom} = V_{cc} - [I_{out(max)} * R_{load}]$

$1V = 5V - [100mA * 40 \text{ ohms}]$

$V_{headroom}$ is all that is left for MOSFET V_{ds} drop + High Side Current Sense Resistor Drop

PPSL (Preferred Parts Selection List) Parts:

Overkill but we can work with them!

MOSFETs:

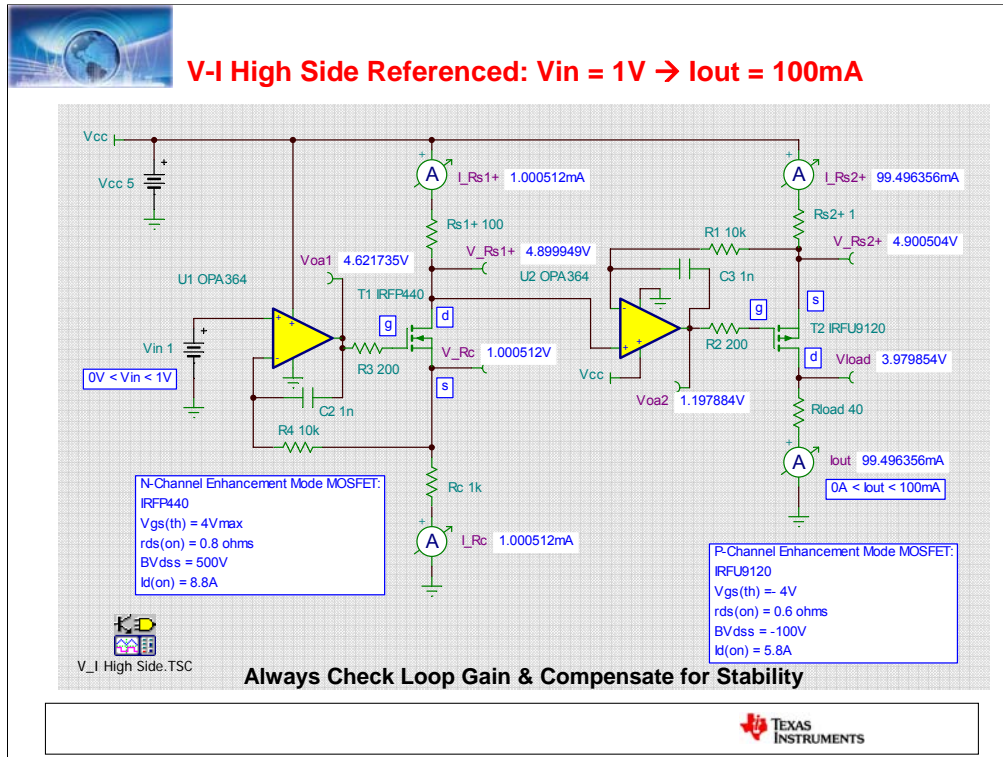
N-Channel Enhancement Mode MOSFET:
IRFP440

$V_{gs(th)} = 4V_{max}$
 $r_{ds(on)} = 0.8 \text{ ohms}$
 $BV_{dss} = 500V$
 $I_{d(on)} = 8.8A$

P-Channel Enhancement Mode MOSFET:
IRFU9120

$V_{gs(th)} = -4V$
 $r_{ds(on)} = 0.6 \text{ ohms}$
 $BV_{dss} = -100V$
 $I_{d(on)} = 5.8A$

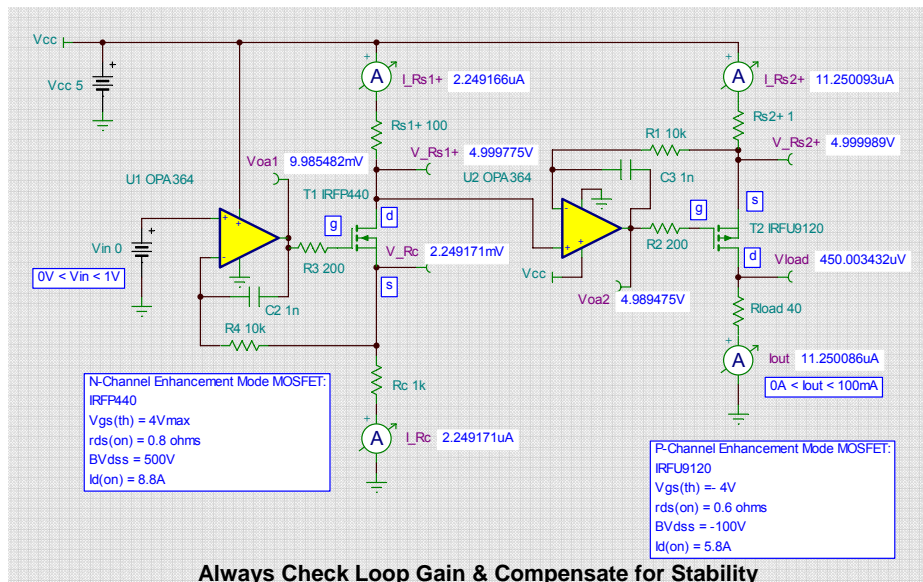




The V-I High Side Referenced circuit is intended to receive a ground referenced command voltage and control current in the high side of the output to drive a grounded load. To level shift the ground referenced V_{in} up to the positive supply, V_{cc} , an N-Channel Enhancement Mode MOSFET is used along with U1, a single supply RRIO op amp, OPA364. V_{in} is impressed across R_c due to the open loop gain of the op amp and feedback across R_c . This will cause a current I_{Rc} to flow. Since there is no error gate current the drain current of T1, I_{Rs} will be the same as I_{Rc} . I_{Rs} times R_{s1+} will create a voltage drop referenced to V_{cc} . The output power stage consists of U2, OPA364, and a P-Channel Enhancement Mode MOSFET. The input voltage to U2 is referenced to V_{cc} as is the feedback across R_{s2+} and the op amp loop gain will move the output of U2 to control the gate of T2 until the op amp inputs equal each other. The overall scaling for full-scale is 1V in across R_c creates $I_{Rc} = 1mA$. $I_{Rc} = I_{Rs+} = 1mA$ times R_{s1+} of 100 ohms yields a 100mV drop from V_{cc} at U2, +input. 100mV at U2, -input means I_{out} must be equal to $100mV/R_{s2+}$ or $100mV/1 = 100mA$. Key design considerations are adequate voltage control on single supply for the V_{gs} of the MOSFETs used. Lower cost, lower MOSFETs can be found that will do equally as well as those used here for demonstration of this often-used design concept. For the level shifting of V_{in} to be referenced to V_{cc} a JFET can be used but care must be taken to ensure the gate-source and gate-drain junctions do not become forward biased or undesired voltages may occur in the translation circuitry.



V-I High Side Referenced: $V_{in} = 0V \rightarrow I_{out} = 0A$





V-I High Side Referenced: Design Details

Design Details:

1) Rs2+ Selection

Choose Rs2+ to drop 100mV at Iout=100mA

$$Rs2+ = 100mV / 100mA = 1\Omega$$

Small headroom but enough reasonable signal

2) Level Shift:

$$V_{RC} = V_{in}$$

$$I_{RC} = V_{in} / R_c$$

$$I_{RC} = I_{Rs1+} \text{ (Use MOSFET -> small error current)}$$

$$V_{Rs1+} = V_{cc} - (I_{Rs1+} \cdot R_{s1+})$$

$$V_{Rs1+} = 100mV \text{ for } V_{in} = 1V. \text{ Choose } I_{Rs1+} = 1mA \text{ at } V_{in} = 1V$$

$$R_{s1+} = 100mV / 1mA = 100\Omega$$

$$R_c = 1V / 1mA = 1k\Omega$$

Ensure T1 can provide Vgs(on) with Vcc - VRC(max)

$$V_{gs(on)} = 5V - 1V = 4V \rightarrow \text{Okay}$$

Use U1 = RRIO Op Amp

3) Output Current Control

Use P-Channel MOSFET since:

Turn off Voa2 goes to Vcc

Turn on Voa2 can go Gnd -> 5V = Vgs

Feedback around U2 is relative to Vcc across Rs2+

Use U2 = RRIO Op Amp

Auto-zero will improve accuracy due to Vos on U2

4) Stability considerations on U1 and U2

Both U1 and U2 need to be analyzed for stability and compensated

5) %FSR Accuracy

$$\%FSR \text{ Accuracy} = \{ [I_{out(fs)}]_{ideal} - I_{out(fs)}_{actual} \} / [I_{out(fs)}]_{ideal} \cdot 100$$

$$\%FSR \text{ Accuracy} = \{ [100mA - 99.496356mA] / [100mA] \} \cdot 100 = 0.5036\%$$





V-I Low Side Referenced Given:

PPSL (Preferred Parts Selection List) Parts:

NPN Power Transistor:

Design Goal:

$V_{CC} = +12V$

$V_{in} = 0V$ to $4.096V \rightarrow I_{out} = 0$ to $500mA$

$R_{load} = 20\ \Omega$, Floating Load

0.5% FSR accuracy in transfer function (I_{out}/V_{in})

Design Considerations:

Need to Sense current in Low Side

Need to drive high current \rightarrow External Transistor

Need RRO Op Amp, Input CM to Ground

NPN Power Transistor:

TIP33

$V_{(br)ceo} = 40V$

$I_{c(continuous)} = 10A$

$h_{fe} @ I_c = 0.5A = 100$

$V_{be} @ I_c = 0.5A = 0.65V$

$P_d = 80W @ T_c = 25^\circ C$

$R_{\theta ja} = 35.7^\circ C/W$

$T_{jmax} = 150^\circ C$

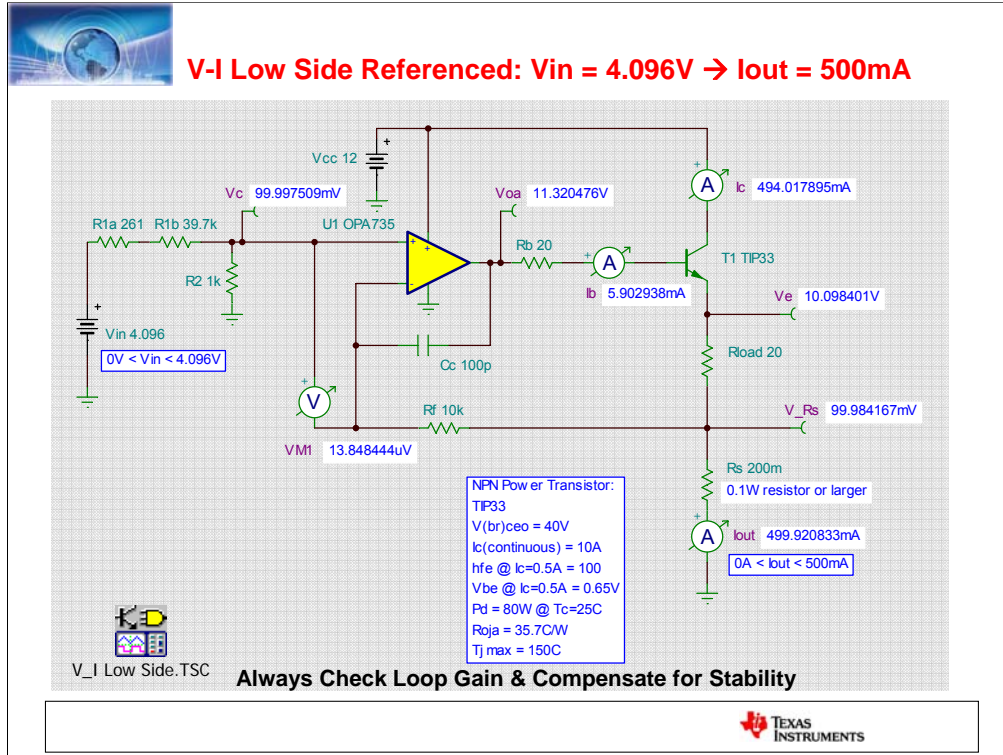
Design Preliminary Analysis:

If there is voltage headroom then:

Use Bipolar Emitter-Follower after op amp for simplest design

Low drop across sense resistor \rightarrow maximize headroom & minimize power dissipation

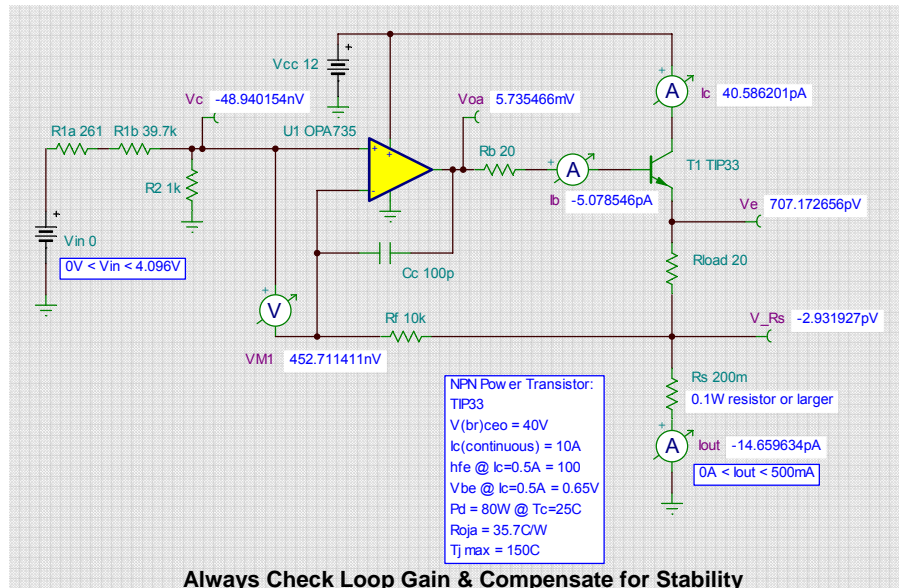




This V_I Low Side Referenced circuit simplifies boosting output current in applications where there is adequate voltage headroom to use a familiar emitter-follower current boost stage after a small signal op amp. In this arrangement accurate current control is kept through the floating load as both base current and collector current become emitter current and flow into the load and into the load current sense resistor, R_s . The top of R_s is fed back into the $-$ input of $U1$. Since this is a non-inverting circuit we must pay attention that we do not have any common mode violations on $U1$. The OPA735 has common mode input to ground and $V_{cc}-1.5V$. For this arrangement and operation we are safe. The only errors in this are resistor tolerances on the V_c divider, tolerance on R_s , and the V_{os} of $U1$.



V-I Low Side Referenced: $V_{in} = 0V \rightarrow I_{out} = 0A$



Always Check Loop Gain & Compensate for Stability





V-I Low Side Referenced: Design Details

Design Details:

1) Select R_s

$$V_{Rs} = I_{out} \text{ at } I_{out} = 0.5A$$

Help with headroom, minimize power dissipation in R_s , still good signal at full scale.

$$V_{Rs} = 100mV / 0.5A = 200m\Omega$$

2) Scale V_{in} full scale

$$V_c = 100mV \text{ for } V_{in} = 4.096V$$

Load V_{in} with 0.1mA at full scale

$$R_2 = V_c / 0.1mA = 100mV / 0.1mA = 1k\Omega$$

$$R_1 = R_{1a} + R_{1b}$$

$$0.1mA = V_{in} / (R_1 + R_2)$$

$$0.1mA = 4.096 / (R_1 + 1k) \rightarrow R_1 = 39.96k\Omega$$

Use standard values:

$$R_{1a} = 261\Omega$$

$$R_{1b} = 39.7k\Omega$$

3) Check I_{out} Current Control at Max I_{out}

$$V_{Rs} = I_{out(max)} \cdot R_s = 500mA \cdot 200m\Omega = 100mV$$

$$V_e = V_{Rs} + I_{out} \cdot R_{load} = 100mV + 500mA \cdot 20\Omega = 10.1V$$

Assume TIP33 $V_{be} = 0.65V$

$$\text{Assume TIP33 } h_{fe} = 100 \rightarrow I_b = 500mA / 100 = 5mA$$

Choose R_b to add 100mV or so to headroom, R_b helps limit transient current into TIP33 base

R_b also helps isolate transistor parasitic capacitances at high frequency from op amp output

$$V_{drop} \text{ across } R_b = 20\Omega \cdot 5mA = 0.1V$$

$$V_{oa} = V_e + V_{be} + V_{Rb} = 10.1V + 0.65V + 0.1V = 10.85V$$

OPA734 at 5mA out looks like about 0.5V swing to rail so we have 0.65V margin for supply to dip or worst case V_{be} to occur, or degradation in h_{fe} requiring more I_b through R_b .

4) %FSR Accuracy

$$\%FSR \text{ Accuracy} = \{ [I_{out(fs)} \text{ Ideal} - I_{out(fs)} \text{ actual}] / [I_{out(fs)} \text{ Ideal}] \} \cdot 100$$

$$\%FSR \text{ Accuracy} = \{ [500mA - 499.920833mA] / [500mA] \} \cdot 100 = 0.0158\%$$

This design leaves plenty of margin for resistor tolerances.

The auto-zero accuracy of OPA734 and the simplicity of the design minimizes errors here.





V-I Improved Howland Current Pump

Design Goal:

$V_{cc} = +5V$

$V_{in} = 0V$ to $500mV \rightarrow I_{out} = 0$ to $500mA$

$R_{load} = 8\ \Omega$, Grounded Load

1% FSR accuracy in transfer function (I_{out}/V_{in})

Design Considerations:

Need to Sense current in High Side

Need to drive high current \rightarrow Power Op Amp?

Need RRO Op Amp, Input CM to Ground

Design Preliminary Analysis:

If there is voltage headroom then:

Power Op Amp offers single IC solution

Low drop across sense resistor \rightarrow maximize headroom & minimize power dissipation

Given:

PPSL (Preferred Parts Selection List) Parts:

OPA569 Power Op Amp

OPA569 Power Op Amp:

2.7V to 5.5V supply

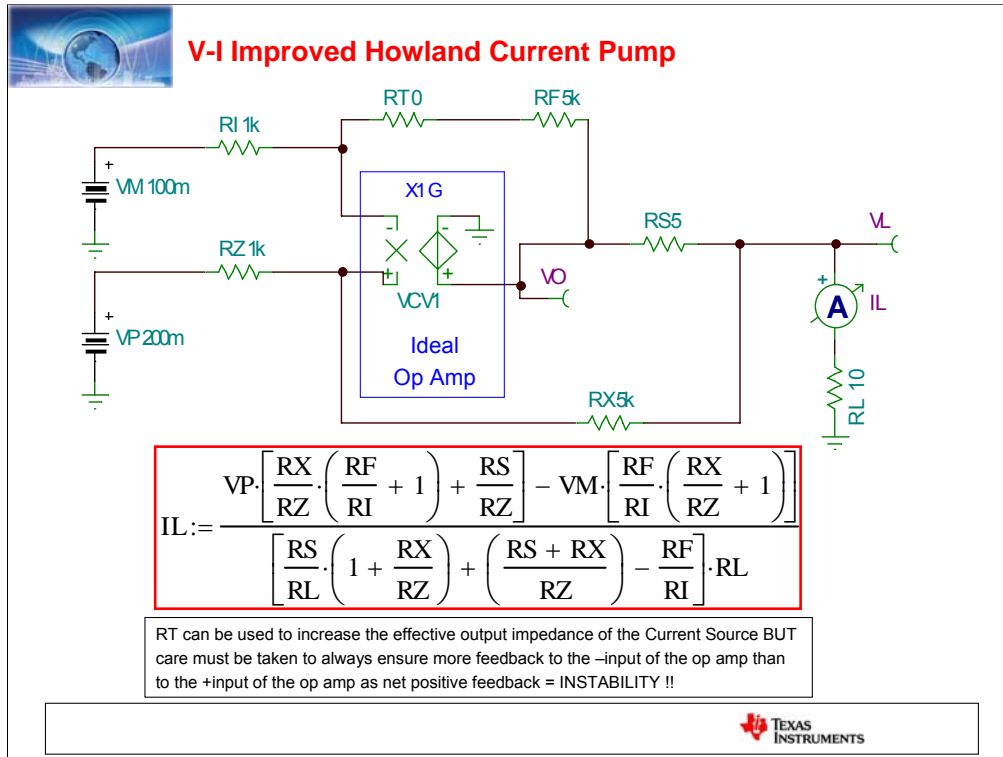
Input voltage range includes V_{cc} & Gnd

2A Output Current Capability

$\pm 300mV$ swing from rail at $\pm 2A$ out

Input Offset Voltage = $\pm 2mV$ max





The Improved Howland Current Pump uses two feedback paths to form a net differential feedback path across a high-side current sense resistor capable of driving a grounded load. In single supply applications this works well for creating bipolar current flow in a load by using the Improved Howland Current Pump in a BTL (Bridge Tied Load).



V-I Improved Howland Current Pump

Set $R_X=R_F$ and $R_Z=R_I$ and move all tolerances to worst case for accuracy analysis

RT	RF	RX	RI	RZ	RS	RL	IL	VL	VO	AM1 Sensitivity (%)	Comments
2.858407	5000	5000	1000	1000	5	10	0.100000052	1.000000100	1.500667000	0.000000000	Rt adjusted for Ideal IL
0	5000	5000	1000	1000	5	10	0.099866893	0.998666893	1.498666900	0.133158931	Rt=0, Nominal Values
2.858407	5050	5000	1000	1000	5	10	0.102371216	1.023712000	1.536255000	-2.371162767	1% Resistor Changes
2.858407	5000	5050	1000	1000	5	10	0.098700599	0.987005991	1.481159000	1.299452324	1% Resistor Changes
2.858407	5000	5000	1010	1000	5	10	0.097727653	0.977276527	1.466563000	2.272397818	1% Resistor Changes
2.858407	5000	5000	1000	1010	5	10	0.101353602	1.013536000	1.520981000	-1.353549296	1% Resistor Changes
2.858407	5000	5000	1000	1000	5.05	10	0.099009365	0.990094651	1.490756000	0.990686485	1% Resistor Changes
2.858407	5000	5000	1000	1000	5	10.1	0.099999329	1.009993000	1.510665000	0.000723	1% Resistor Changes
0	5050	4950	990	1010	4.95	10	0.108995522	1.089955000	1.630222000	-8.995465322	1% Worst Case w/RT=0
2.858407	5050	4950	990	1010	4.95	10	0.109152449	1.091524000	1.632570000	-9.152392241	1% Worst Case w/RT=Nom

1% Resistors (w/RT=0) could yield 9% Accuracy at T=25°C

0.1% Resistors (w/RT=0) could yield 0.9% Accuracy at T=25°C

Still useful for V-I control in Motors, Valves, TECs, LEDs, etc

Other system feedback re-adjusts VM or VP for final results



A detailed error analysis of the Improved Howland Current Pump shows that for worst case tolerances 1% resistors will only yield a 9% accurate I_{out}/V_{in} transfer function. Often this is okay as an outside control loop will re-adjust the V_{in} command voltage as needed. It is often the critical current control that is needed in the overall control loop. If 0.1% resistors are used the accuracy of the I_{out}/V_{in} transfer function can be increased to 1%.



V-I Improved Howland Current Pump

$$I_L := \frac{V_P \cdot \left[\frac{R_X}{R_Z} \cdot \left(\frac{R_F}{R_I} + 1 \right) + \frac{R_S}{R_Z} \right] - V_M \cdot \left[\frac{R_F}{R_I} \cdot \left(\frac{R_X}{R_Z} + 1 \right) \right]}{\left[\frac{R_S}{R_L} \cdot \left(1 + \frac{R_X}{R_Z} \right) + \left(\frac{R_S + R_X}{R_Z} \right) - \frac{R_F}{R_I} \right] \cdot R_L}$$

$$I_L := \frac{V_P \cdot \left[\left(1 + \frac{R_F}{R_I} \right) + \frac{R_S}{R_F} \right] - \left(\frac{R_F}{R_I} + 1 \right) \cdot V_M}{R_S \cdot \left(1 + \frac{R_I}{R_F} + \frac{R_L}{R_F} \right)}$$

Set $R_X=R_F$ and $R_Z=R_I$

Assume:

$$R_F = R_X$$

$$R_I = R_Z$$

$$R_F \gg R_S$$

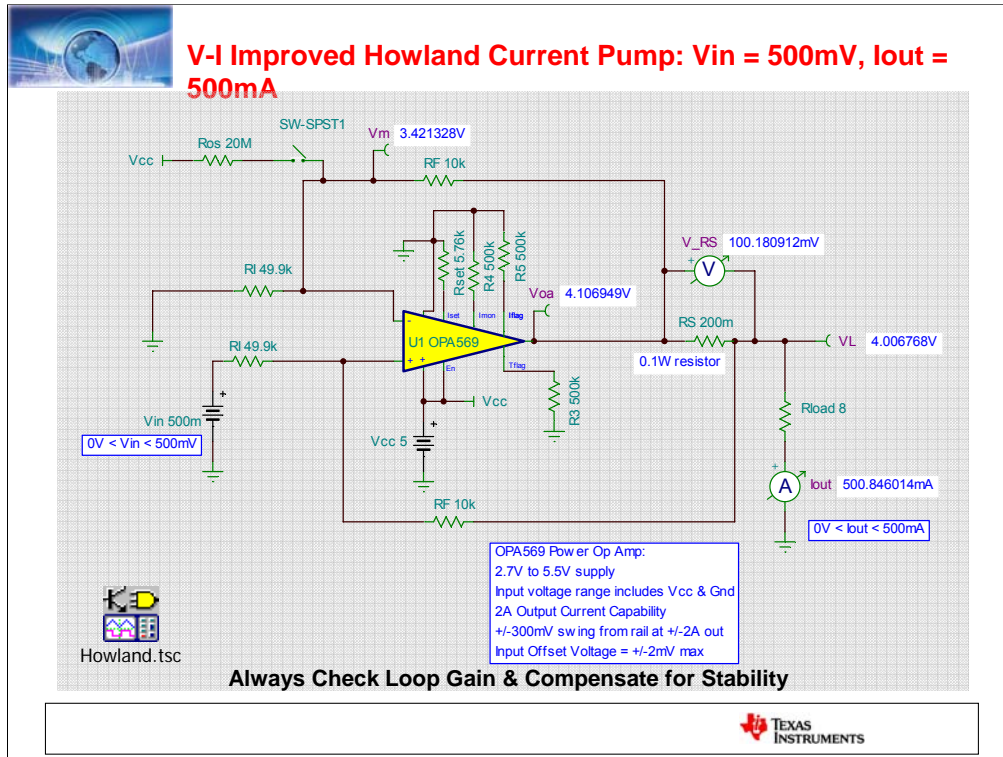
$$R_F \gg R_L$$

$$I_L := \frac{(V_P - V_M) \cdot \frac{R_F}{R_I}}{R_S}$$

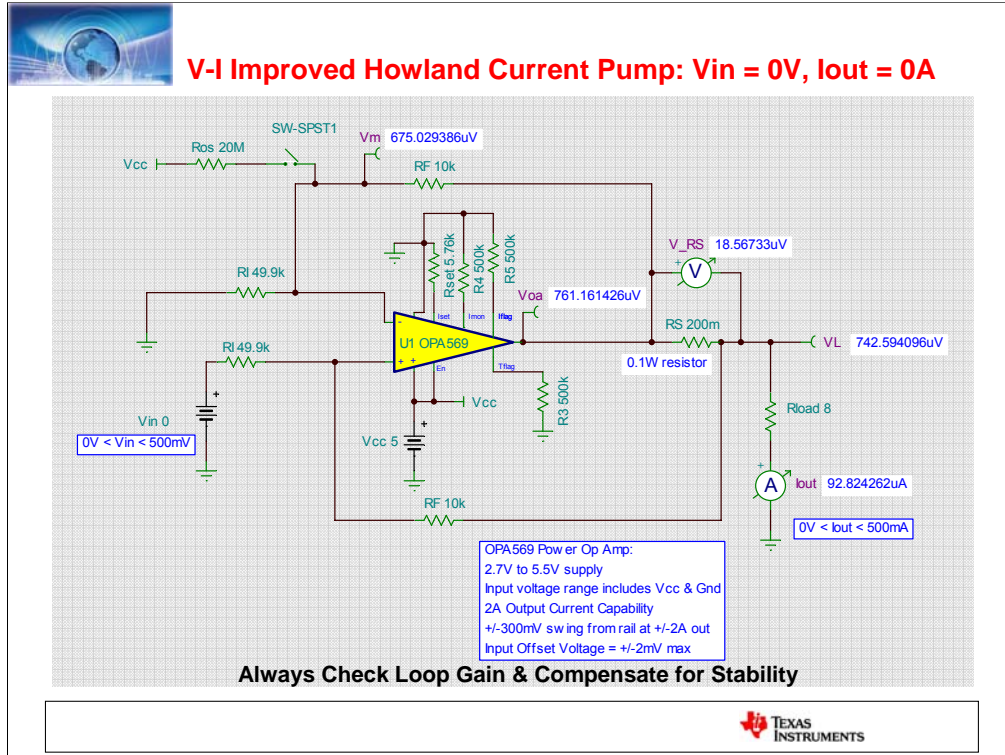
*Input Voltage is Gained up
and Differentially forced
across R_S*



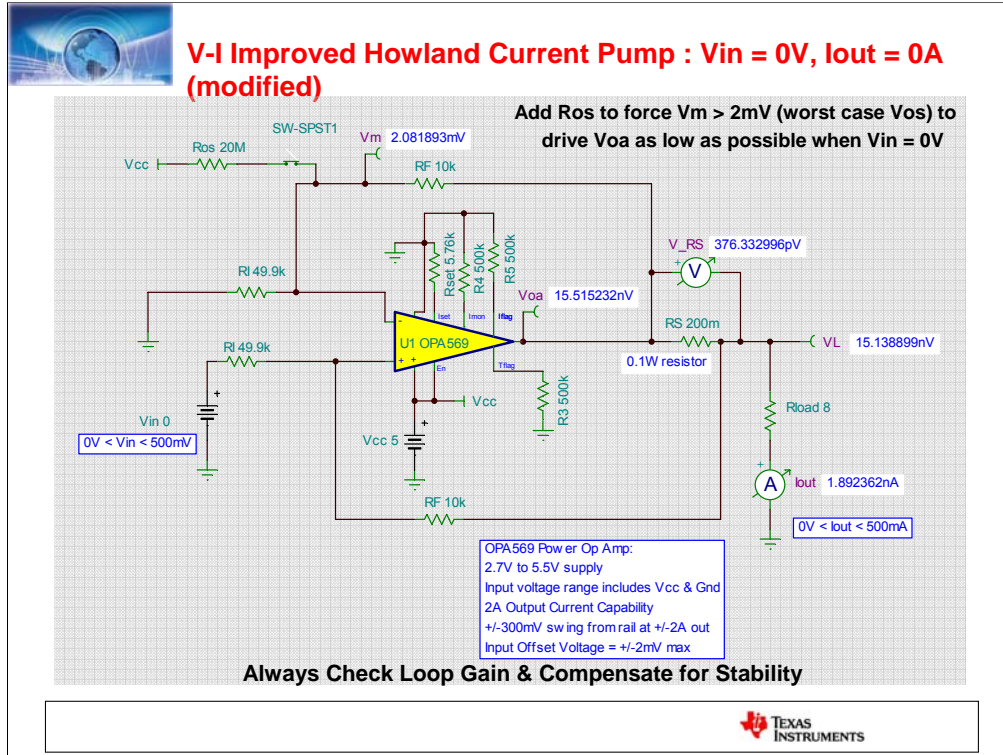
By using symmetrical values in the Improved Howland Current Pump and scaling the feedback much larger than the load or sense resistor (which is usually the case in applications using this circuit) the transfer function becomes more manageable and easier to use. The final transfer function clearly shows that this input voltage is gained up and impressed across the current sense resistor.



A high current implementation of the Improved Howland Current Pump is shown here using the OPA569 Power Op Amp. Attention must be paid to ensure adequate voltage headroom on the single supply. RR input on the OPA569 allows accurate current control down to zero volts out. V_{in} is gained by $10\text{k}/49.9\text{k}$ or about 0.2 and impressed across R_s of 200mohm . For 500mV in this means 100mV across 200mohm or $I_{out}=500\text{mA}$.



For zero V_{in} we a 92uA current still through the load due to the input offset voltage of the OPA569.



If we add R_{os} and sum in a 2mV offset into the input of the oPA569 we can ensure we drive the output of the OPA569 off in the case where $V_{in}=0V$. This offset should be greater than the worst case V_{os} of the oPA569. This large value resistor value for R_{os} will not appreciably degrade the scaling accuracy of the I_{out}/V_{in} transfer function.

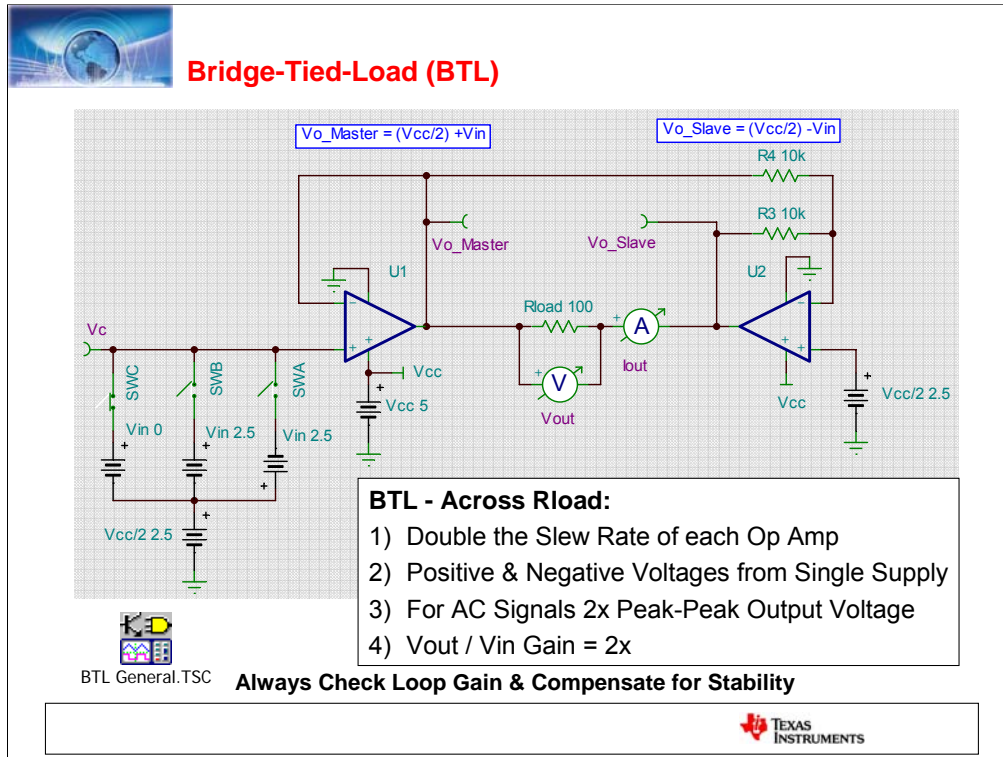


Drive Circuits

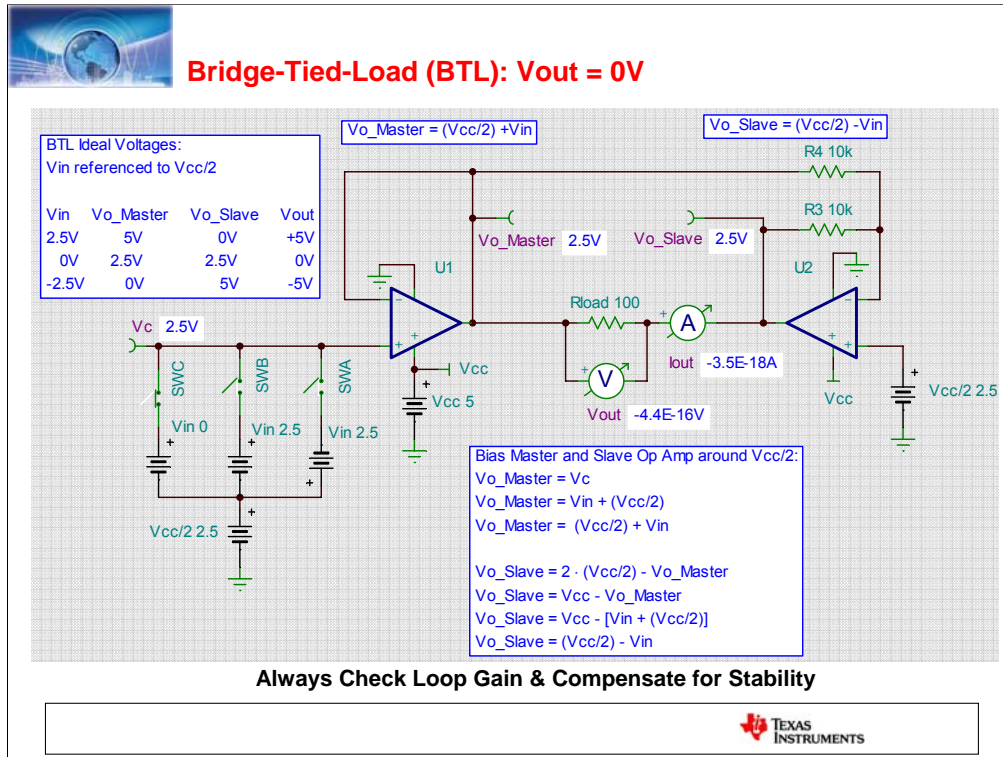
Bridge-Tied-Load (BTL)

Parallel Op Amps

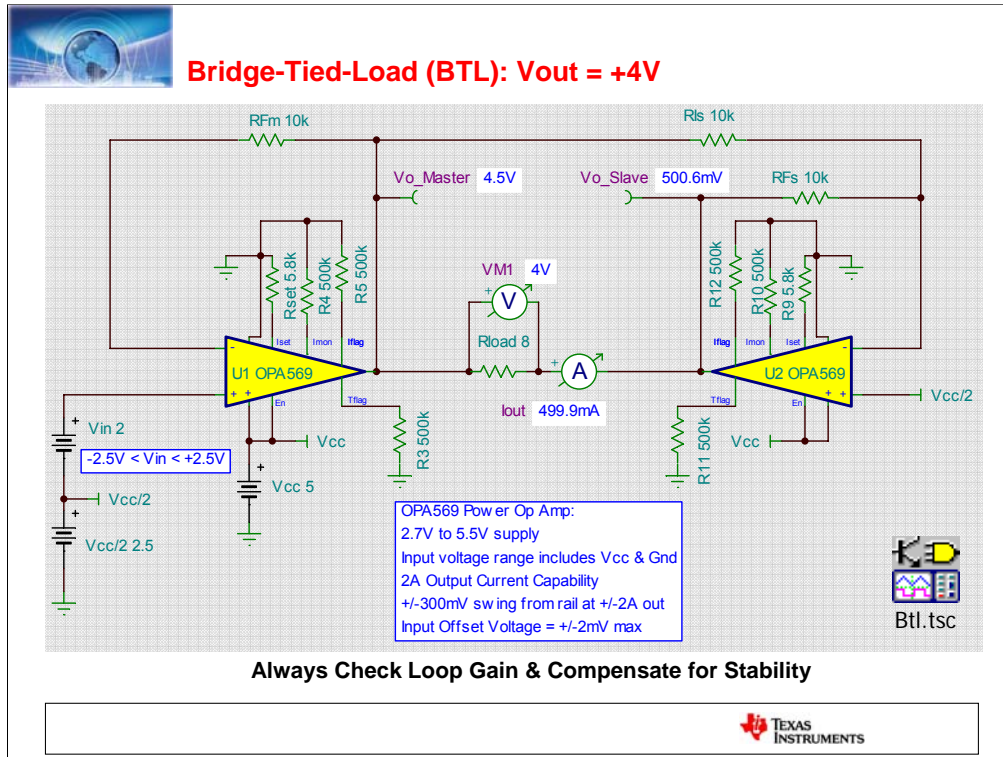
High Current Cascade Reference Buffer



The Bridge-Tied-Load (BTL) arrangement offers many advantages for single supply applications as long as the load can float (neither end of the load can be ground referenced). With the BTL positive and negative voltages can be created across the load using only a single supply. This occurs because U1 output can be at V_{cc} while U2 output is at ground creating a “positive” voltage across the load. If U1 output is now taken to ground and U2 output to V_{cc} we create a “negative” voltage across the load. This effect allows one to create double the peak-to-peak voltage for an AC excitation application. Likewise the slew rate across the load is doubled. For example if U1 is slewing up at $1V/\mu s$ then U2 output is slewing down at $1V/\mu s$ with an effective $2V/\mu s$ experienced at the load. The V_{out}/V_{in} transfer function is doubled for this configuration since a $+1V$ change (relative to mid-supply) out of U1 results in a $-1V$ change (relative to mid-supply) out of U2 yielding a net $2V$ change across the load.



The BTL single supply application here is set for Master amplifier $G=1$, although other gains can be used. If the input V_{in} is reference to mid-supply as shown then $V_{in}=0V$ will result in $0V$ across the load. If U1 and U2 have adjustable output current limits set the Master Amplifier to current limit first for balanced power dissipation in case of a load short between the two outputs.



Two OPA569 power op amps in a BTL arrangement offer high current and close swing to the rail. Here since we are set for $G=1$ on the Master Amplifier the load sees twice the voltage of V_{in} . For $V_{in} = 2V$ the load is commanded to see $4V$.

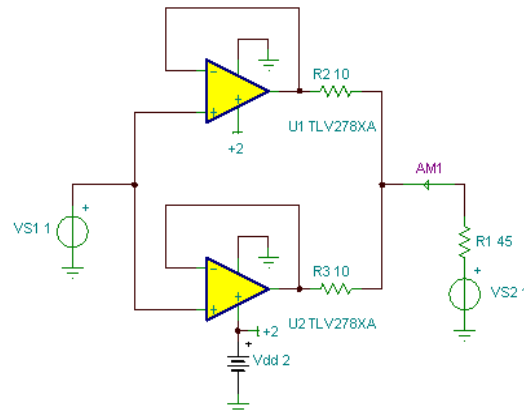


Parallel Op Amps

Why Parallel Op Amps?

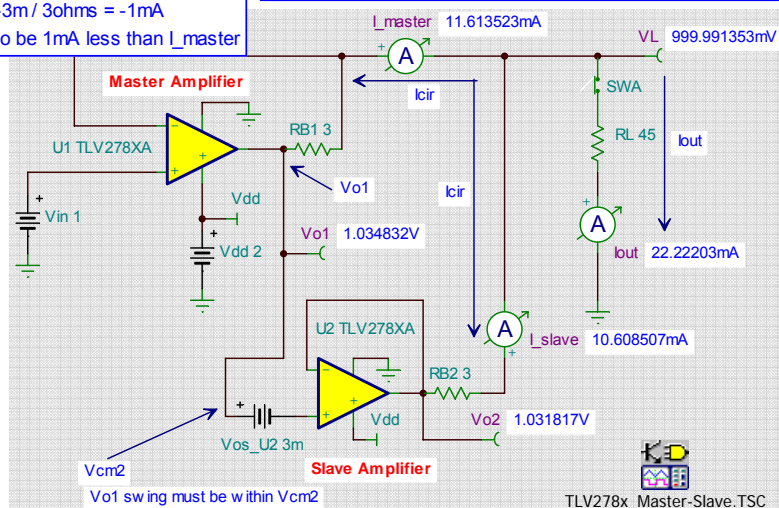
Increase Current to Load
Keep Class AB Output
Easier than External Devices

Dual Drive Arrangement for Parallel Op Amps Does not Give Accurate VL (voltage at load)



Parallel Op Amps offers an easy way to get higher current drive with closer swing to the rail using simple IC Op Amps. Ballast Resistors, Shown here as R2 and R3 are required in this implementation to reduce the effects of different Vos of each op amp which can cause high circulating current between the two op maps. This “Dual Drive” arrangement does not accurately control the voltage at the load.

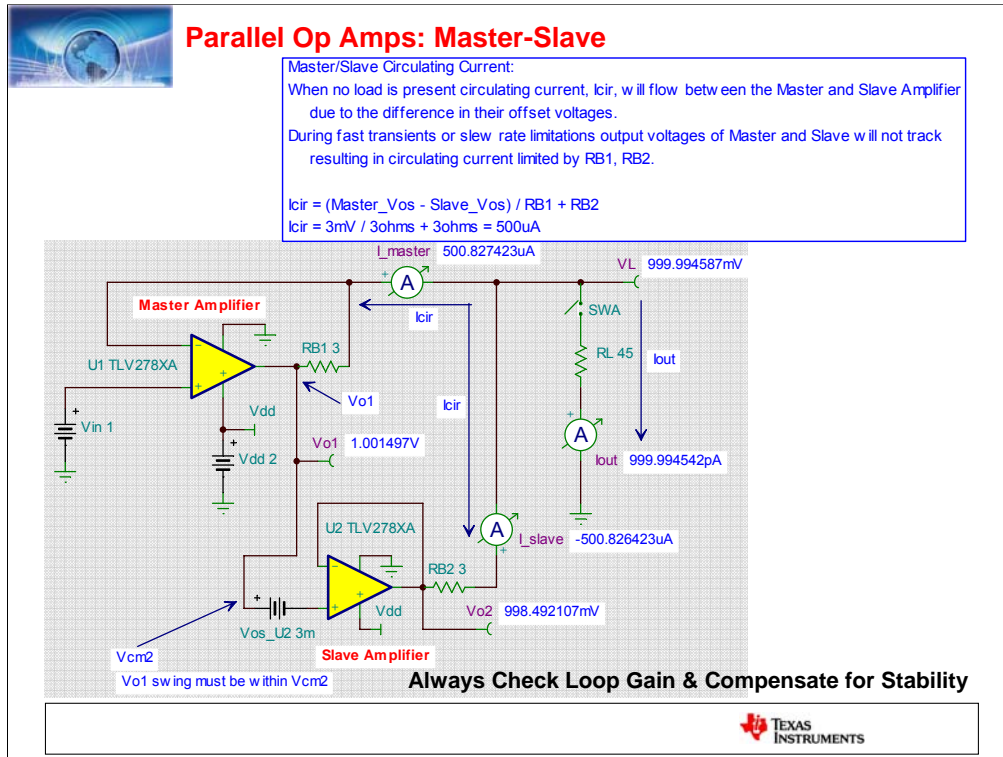
Master-Slave Arrangement for Parallel Op Amps Gives Accurate VL (voltage at load)



Always Check Loop Gain & Compensate for Stability



40



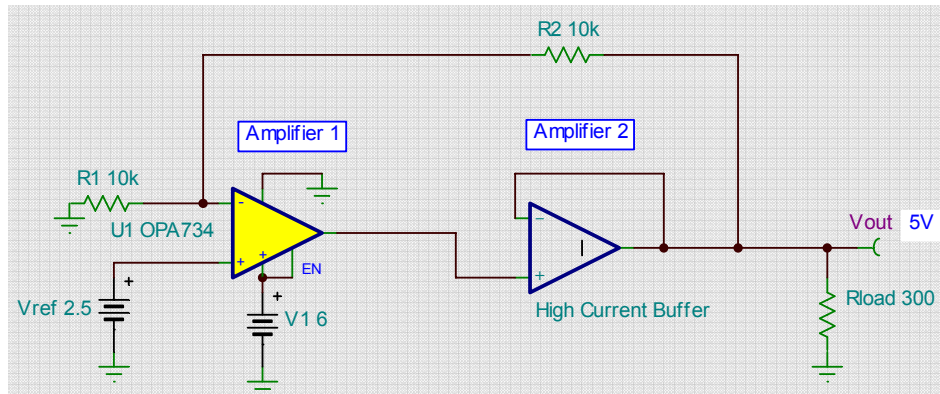
The use of Ballast resistors R_{B1} and R_{B2} limit circulating currents between the Master Amplifier and Slave Amplifier when no load is connected. For this arrangement the circulating current will be the difference in input offset voltages of the two amplifiers divided by $R_{B1} + R_{B2}$. In addition load transients or fast slewing can cause the output voltages of the Master and Slave amplifiers not to track exactly resulting in circulating currents. As a rule-of-thumb it is recommended to limit the slew rate of parallel op amp configurations to about $\frac{1}{2}$ of the op amp slew rate to prevent large circulating currents in a slew limited condition.



High Current Cascade Reference Buffer

High Current Cascade Reference Buffer:

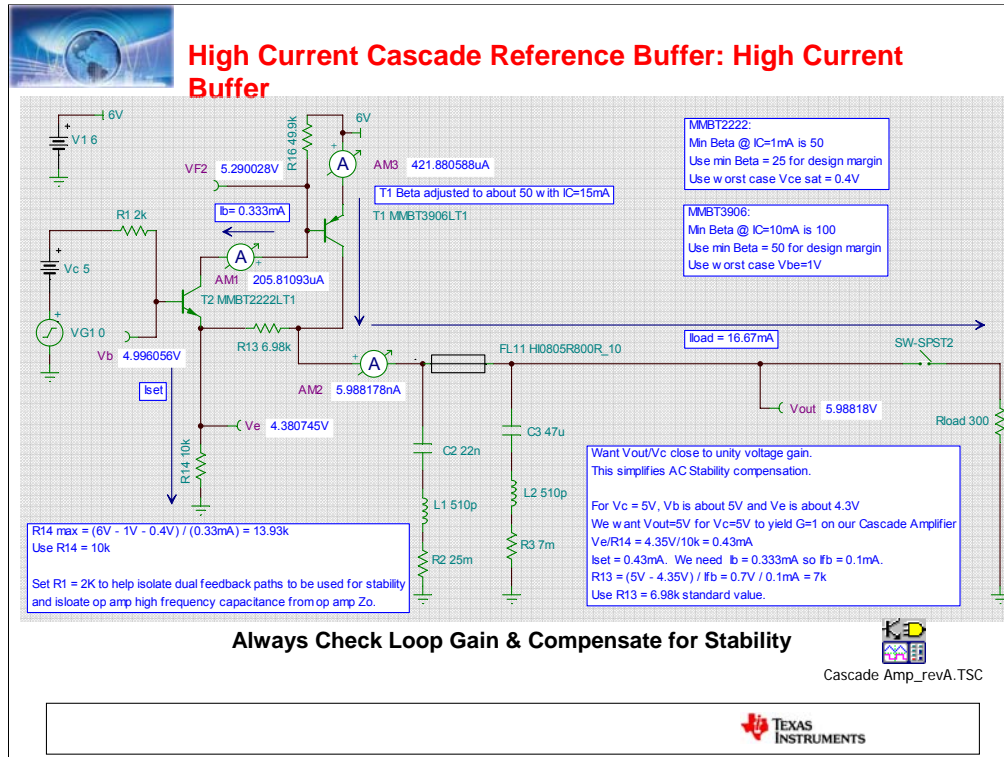
- 1) Amplifier 1 provides closed loop accuracy
- 2) Amplifier 2 provides high current & unity gain simplifies AC Stability compensation
- 3) Single supply demands close swing to rail on Amplifier 1 and Amplifier 2



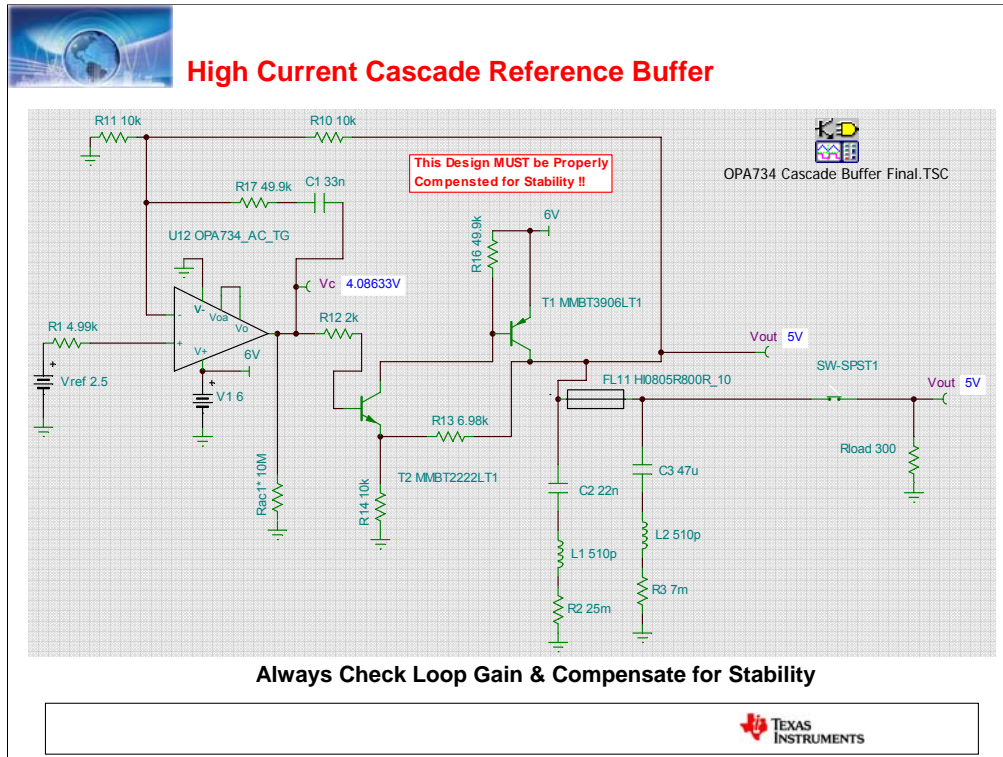
Always Check Loop Gain & Compensate for Stability



Sometimes in single supply applications it is necessary to create a buffered reference which needs to delivery high current. This can be effectively accomplished by the use of a cascade amplifier arrangement as shown above. Amplifier 1 can be an auto-zero accurate amplifier which does not required large drive currents. Amplifier 2 can be a high current unity voltage gain with high current capability. The loop is closed accurately around Amplifier 1. Single supply will require close swing to the rail on both Amplifier 1 and Amplifier 2.



The High Current Buffer is formed by a level shifting NPN transistor, T2, driving a PNP transistor, T1. T1 can swing close to the rail and with 5V to work with there is plenty of drive towards ground with T2 and overcome T1 Vbe plus provide adequate base current drive. In effect T2 can be thought of as a simple op amp with its -input at its emitter. WE use this T2, T1 amplifier instead of controlling a PNP transistor direct out of an op amp to help ease stability compensation with capacitive load. If we just drive a PNP transistor direct we end up with voltage gain in the feedback of the op amp. Voltage gain in the feedback of an op results in a negative 1/Beta, usually -20dB to -40dB depending upon the PNP transistor used. This makes compensating a cascade amplifier arrangement more difficult as direct feedback around an op amp from output to -input can never produce a 1/Beta of less than 1 or 0dB. We will design our High Current Buffer to have about a gain of 1 for our given load and voltage output.



The final High Current Cascade Reference Buffer is shown above. A detailed loop gain AC stability analysis will confirm that this circuit is stable. This exercise is left to the user or contact Linear Applications, Texas Instruments, Tucson Division for assistance.

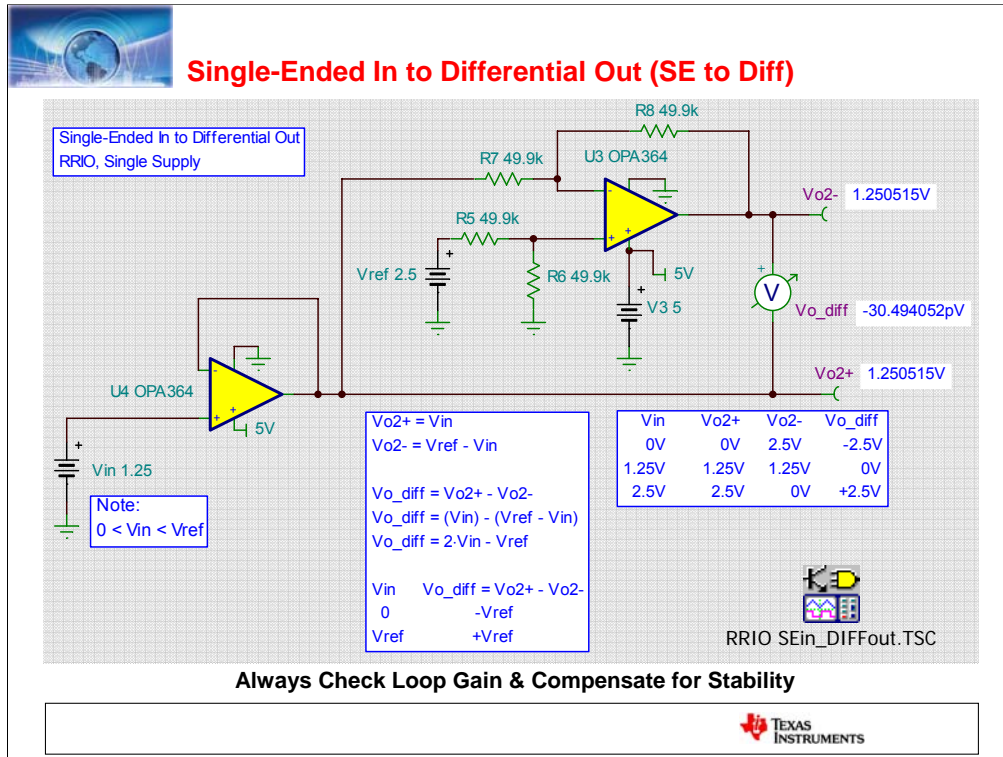


Translation Circuits

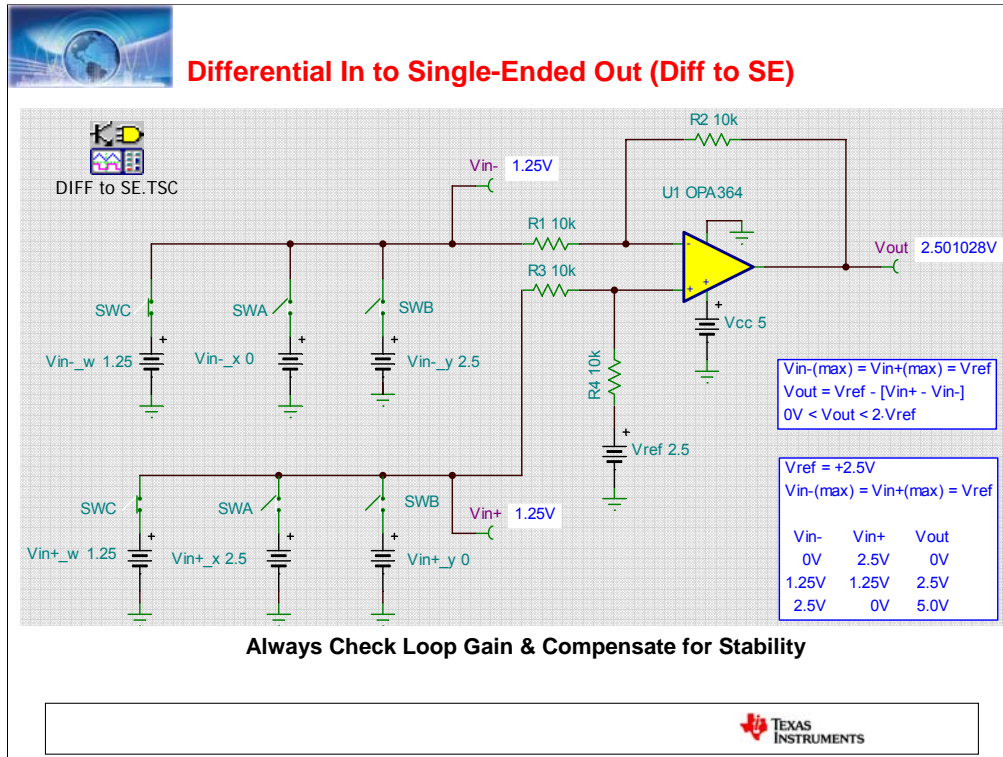
Single-Ended In to Differential Out

Differential In to Single-Ended Out

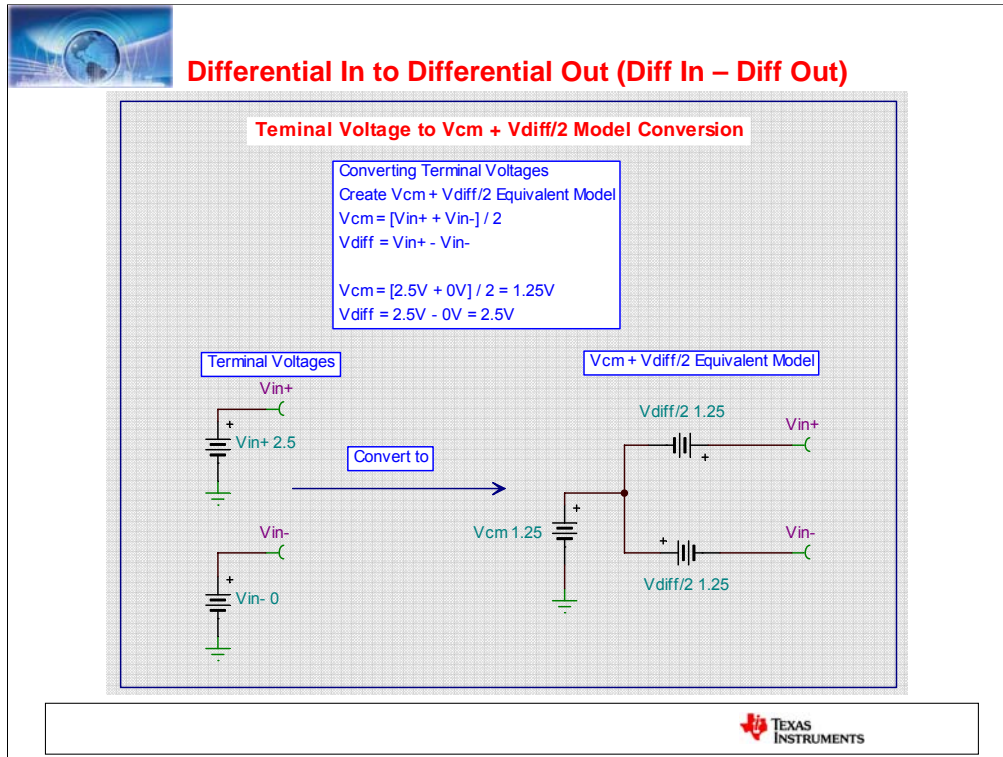
Differential In to Differential Out



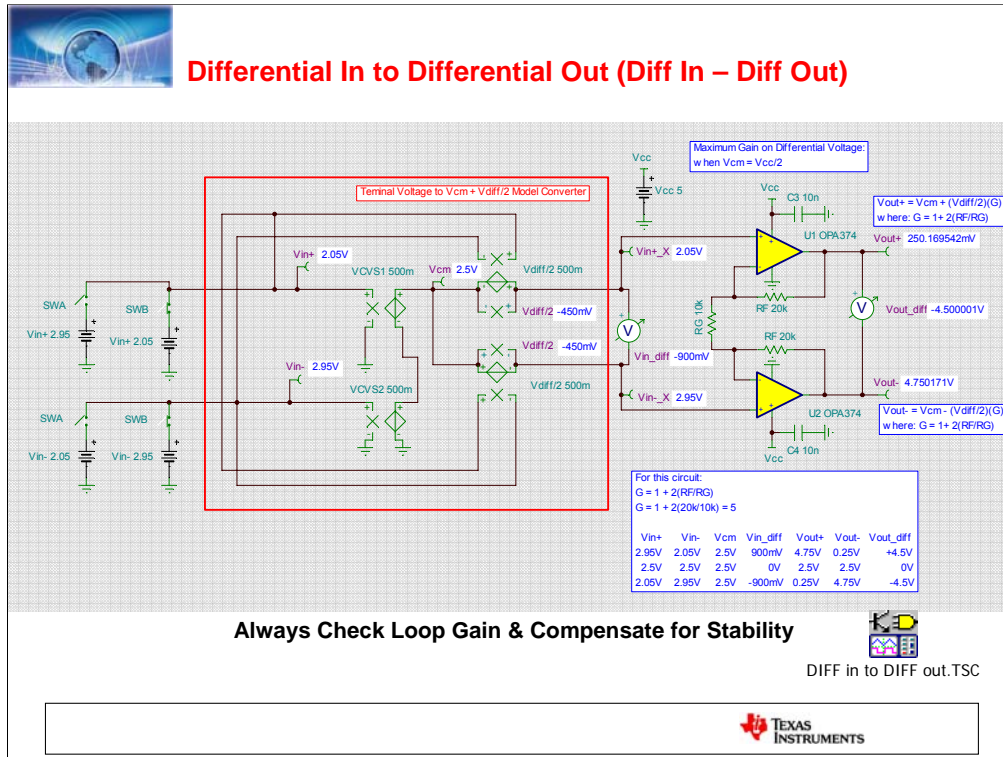
This Single-Ended In to Differential Output circuit will accept input voltage levels from 0 to V_{ref} . V_{ref} here is 2.5V. The details shown above show the proper accurate conversion for single-ended V_{in} of 0V to 2.5V yielding a differential output of -2.5V to +2.5V. If a good single supply difference amplifier with close swing to the rail and auto-zero for low offset voltage and drift it can replace U3.



Differential In to Single-Ended Out is easily achieved by a Difference Amplifier as shown here. With the +input of the Difference Amplifier offset by $V_{ref} = V_{cc}/2$. With a $\pm 2.5V$ (with reference to $V_{cc}/2$) differential input a single-ended output of 0V to 5V is provided.



Or analysis of Differential In to Differential Out amplifiers it is convenient to create a mathematical equivalent model of input voltages which will simplify analysis. This “Terminal Voltage to Vcm + Vdiff/2 Model” is shown above.



Detailed analysis using the “Terminal Voltage to $V_{cm} + V_{diff}/2$ Model” will result in the equations V_{out+} and V_{out-} shown in this slide. Note that these voltages swing symmetrically about V_{cm} which is why, for maximum differential gain, it is desirable to have $V_{cm} = V_{cc}/2$. Here we can translate $\pm 900mV$ differential input (with reference to $V_{cm} = V_{cc}/2$) to $\pm 4.5V$ differential output (with reference to $V_{cm} = V_{cc}/2$). If we did not want gain ($G=1$) we could simply remove R_G . The TINA SPICE circuit contains a pre-built “Terminal Voltage to $V_{cm} + V_{diff}/2$ Model” conversion circuit to help with V_{out+} and V_{out-} analysis.



Conditioning Circuits

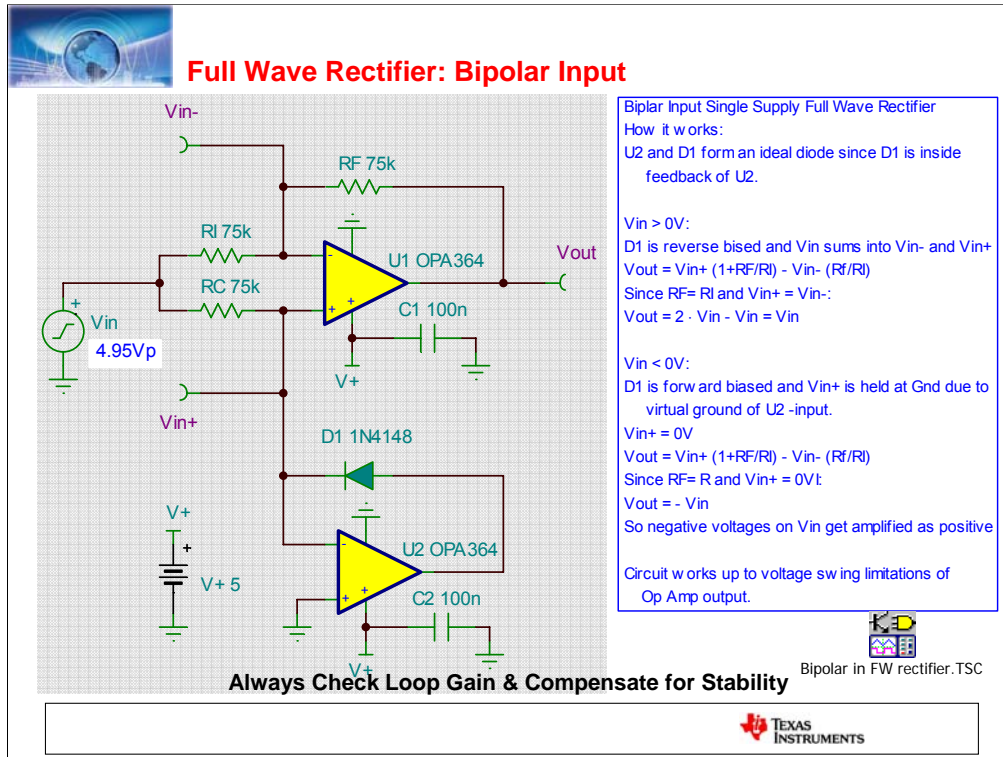
Full Wave Rectifiers

Supply Splitter

Integrator in Feedback

Isolation Amplifier

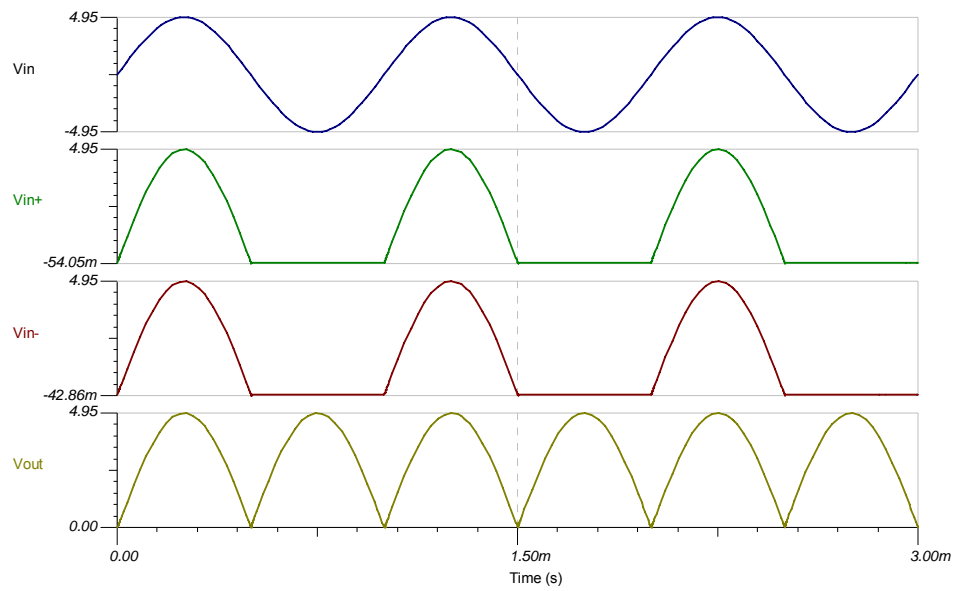
$G=+1$, $G=-1$ Amp

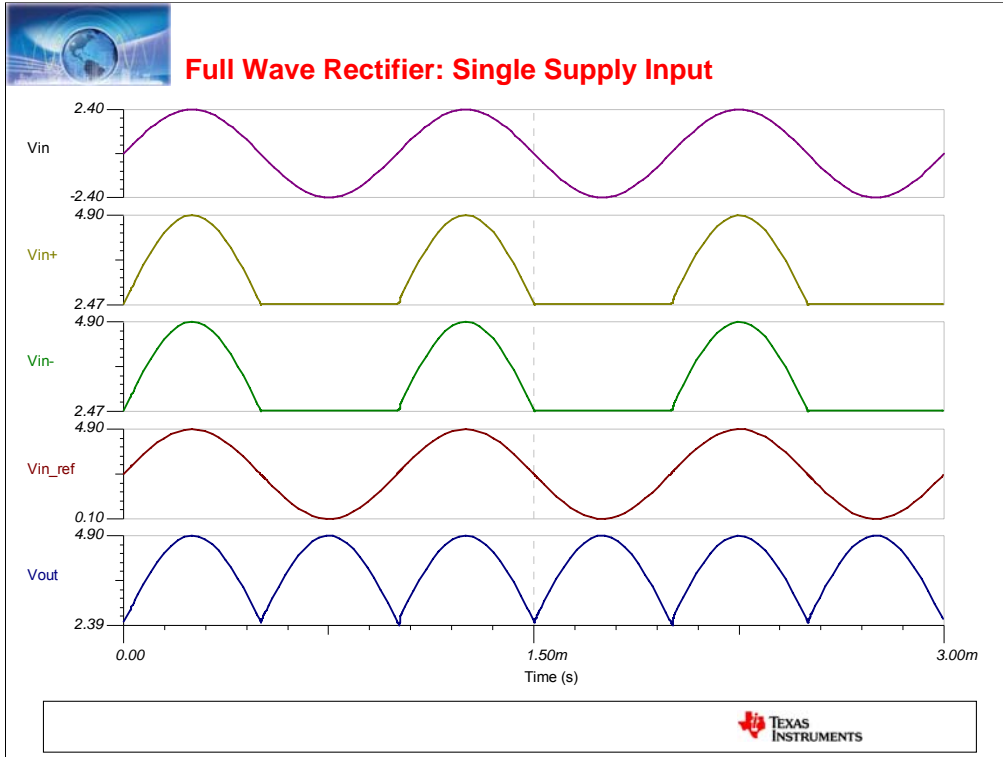


This clever Full Wave Rectifier: Bipolar Input circuit accepts negative peak sine waves (up to the supply rail of the device 5V in this example). For our supply of +5V this circuit will accept up to a 10Vpp sinewave centered on zero volts with +5Vp and -5Vp. For positive peaks (above ground) U1 acts as a summer amplifier and U2 and D1 are out of the picture. For negative peaks (below ground) D1 and U2 form a ground clamp and drive the +input of U1 to be held at 0V or ground. U1 now acts only as an inverting amplifier. The result is a full wave rectified sinewave at Vout.



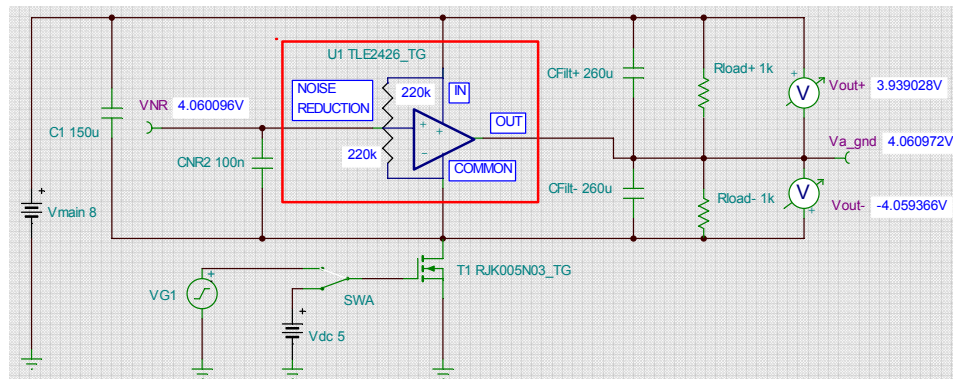
Full Wave Rectifier: Bipolar Input







Supply Splitter: Basic Operation & Wrong Noise Filter



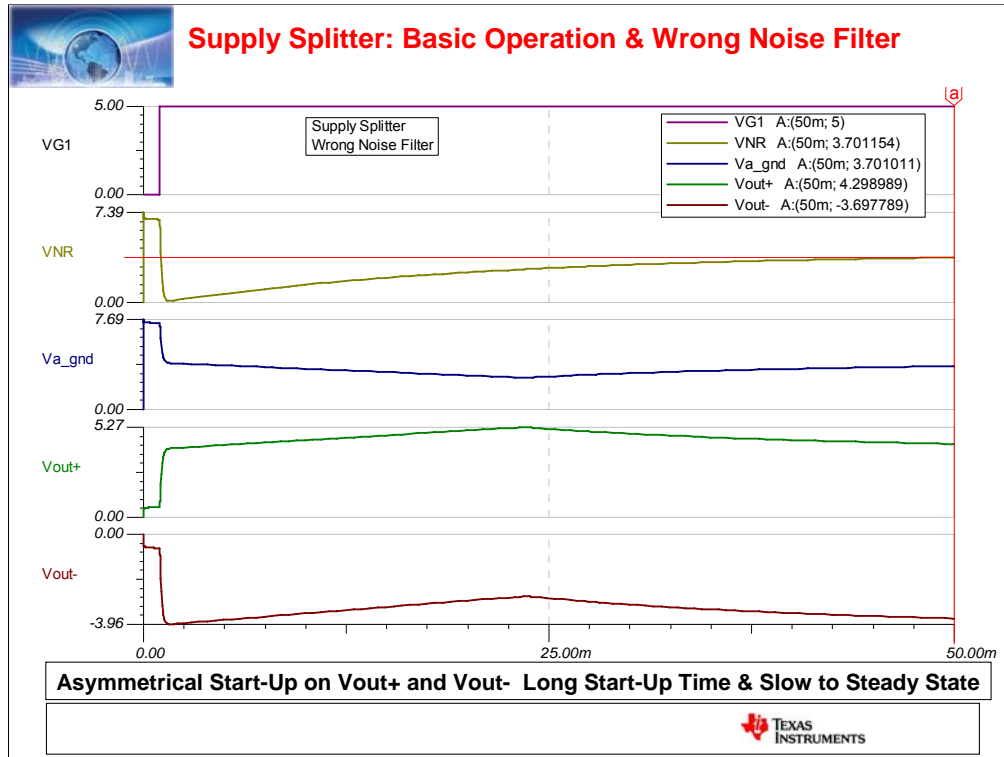
Always Check Loop Gain & Compensate for Stability



Supply Splitter Wrong.TSC



The TLE2426 is an op amp with two internally matched resistors intended to be used as a supply splitter as shown in this slide. The TLE2426 is designed to drive large capacitive loads. Any single supply op amp can be used as a supply splitter in the arrangement shown in this slide. A noise reduction pin which sets the supply midpoint is brought out to add additional capacitive filtering to lower overall noise on the output of the TLE2426, V_{a_gnd} . As shown here we will add a 100nF noise filter capacitor, CNR2 as shown. Lets now see what type of transient turn-on behavior this circuit will have.



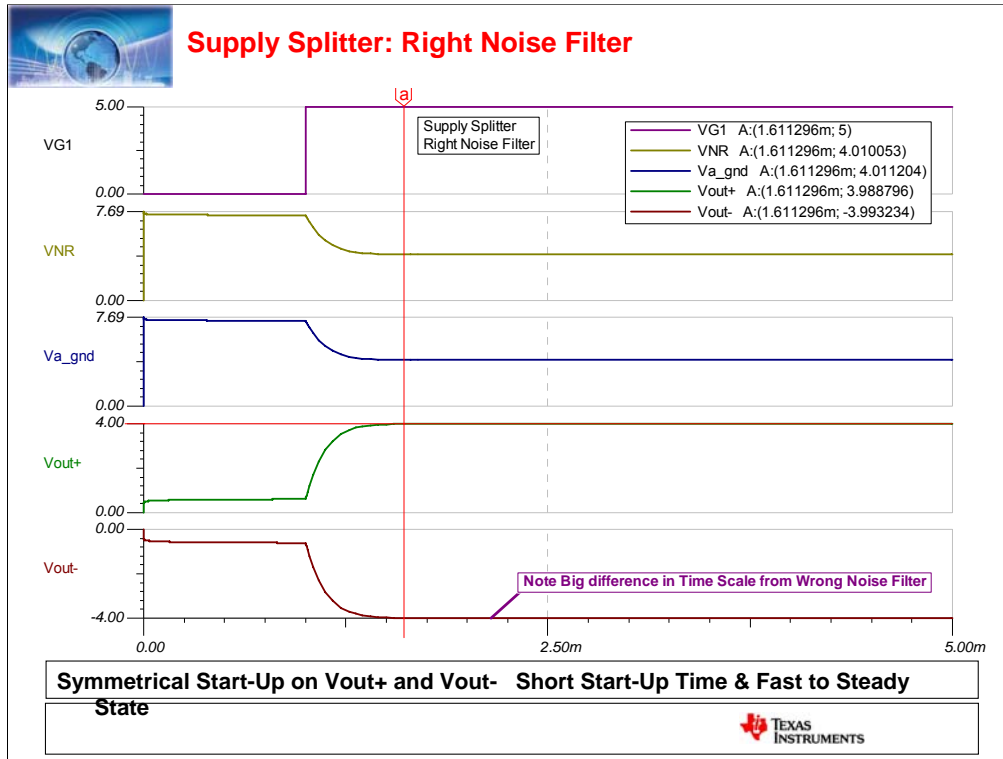
With our noise reduction capacitor, CNR2, we see an asymmetrical startup on each of our supplies V_{out+} and V_{out-} . In addition it takes a long time to reach steady state, up to 50ms.



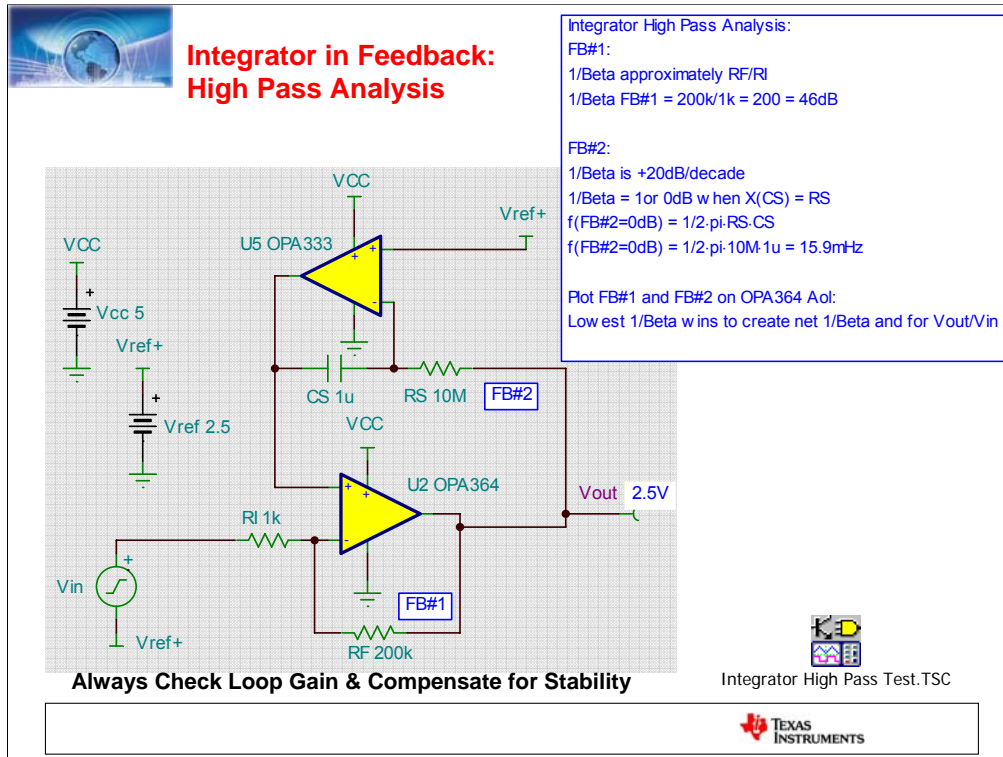
Supply Splitter Right.TSC



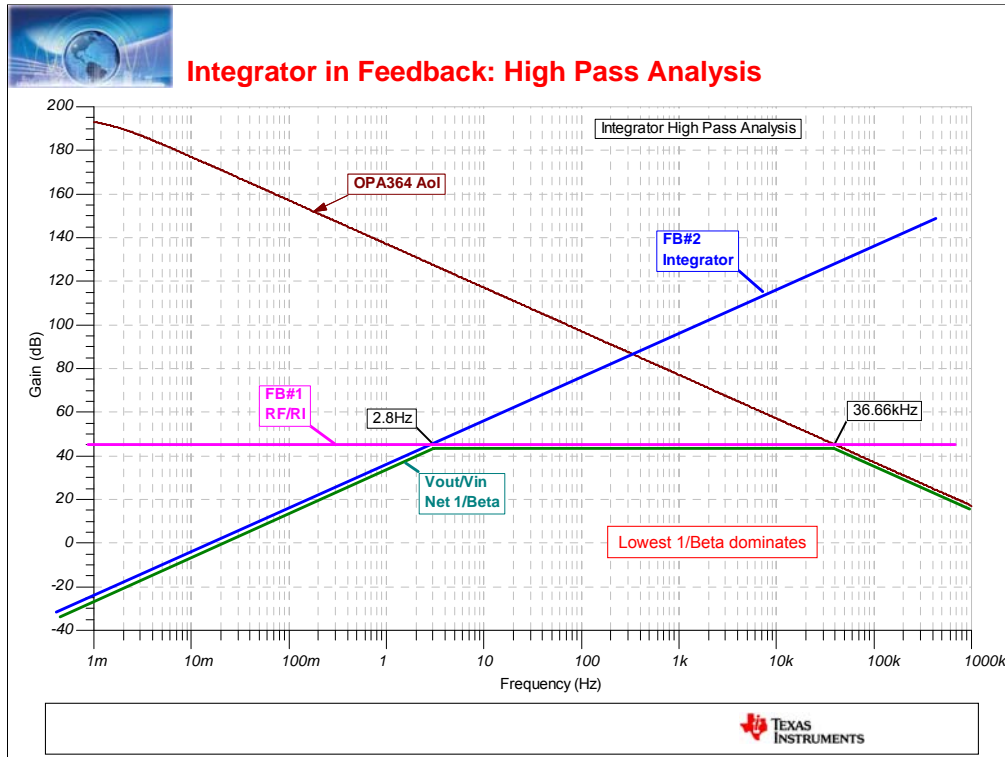
57



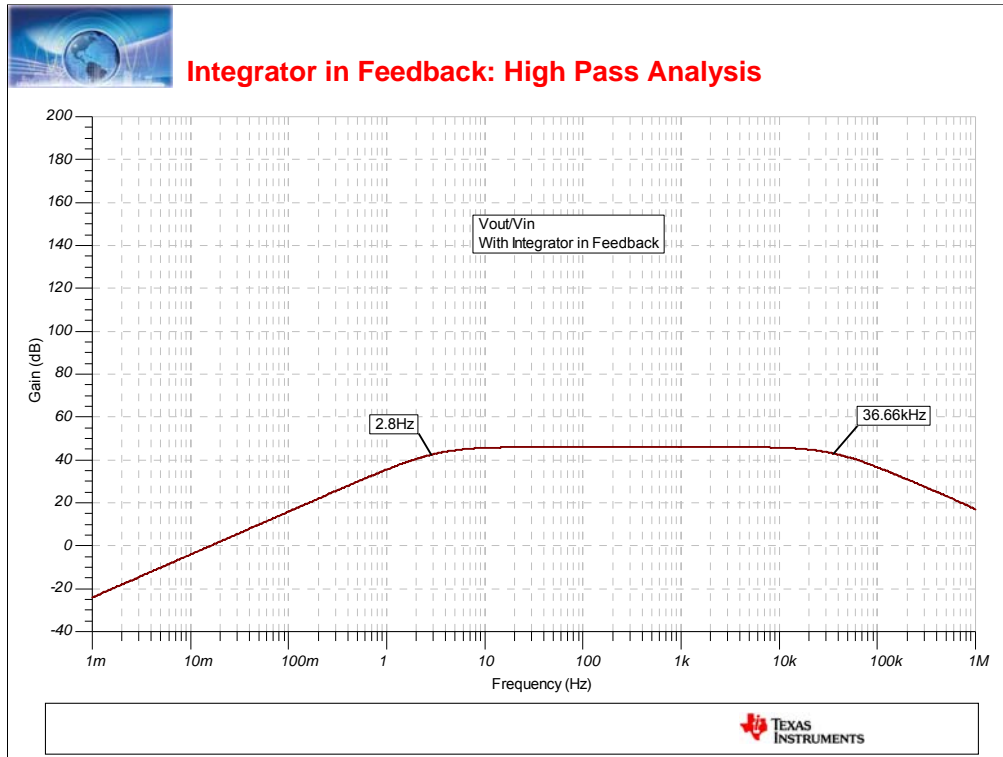
Results of the additional capacitor CNR1 to the noise reduction pin of the TLV2426, VNR, shows dramatic improvement with symmetrical outputs on Vout+ and Vout- and a short start-up time to steady state of about 1.6ms.



A useful building block for many popular single supply circuits such as Medical ECG and Photodiode Transimpedance Amplifiers is an Integrator in Feedback as shown in this slide. Let's first analyze how this creates a High Pass Filter function for the signal conditioning amplifier U2. Observe that there are two feedback paths around U2, FB#1 and FB#2. FB#1 is composed of R_F and R_I and is flat for all frequencies. FB#2 is our integrator and at low frequency will feed back large voltages from V_{out} due the gain created by CS and RS . Large fed back voltage means large Beta or inversely small $1/\text{Beta}$. As frequency increase CS goes towards a short and the gain of the integrator decreases meaning smaller voltages fed back. Smaller voltages fed back means smaller Beta or inversely larger $1/\text{Beta}$. Since there is only one reactive element, CS in the feedback we predict a $1/\text{Beta}$ plot for FB#2 to have $+20\text{dB/decade}$ slope.



Our hand analysis of FB#1 and FB#2 plotted on the Aol for the signal conditioning amplifier U2 is shown here. Stability Analysis rules tell us when using dual feedback paths around op amp circuits the largest β path will dominate. An easy analogy to remember is that if two people are talking to you in one ear which person do you hear the easiest – the one talking the loudest! So the op amp will “listen” to the feedback path with the largest β or smallest $1/\beta$. The net $1/\beta$ plot the op amp sees is the lower one at any frequency of FB#1 or FB#2.



A TINA Spice simulation confirms our hand analysis predictions.

The diagram illustrates a two-stage op-amp circuit for a photodiode model. The first stage, U1 (OPA381), is configured as a voltage follower with its non-inverting input connected to the photodiode model (labeled 'Photodiode Model') and its inverting input connected to the output. The photodiode model is represented by a current source 'Iphoto' and a capacitor 'C12 10p'. The second stage, U2 (OPA364), is configured as an integrator. Its non-inverting input is connected to a reference voltage 'Vref+'. The inverting input is connected to the output of U1 through a resistor 'R1 1k'. The feedback path from the output 'Vout' to the inverting input of U2 consists of a capacitor 'CS 1u' and a resistor 'RS 10M'. The output 'Vout' is shown as 2.499316V. The circuit is powered by 'VCC' and 'Vref+' (2.5V). A blue box highlights the photodiode model and its connection to the first op-amp.

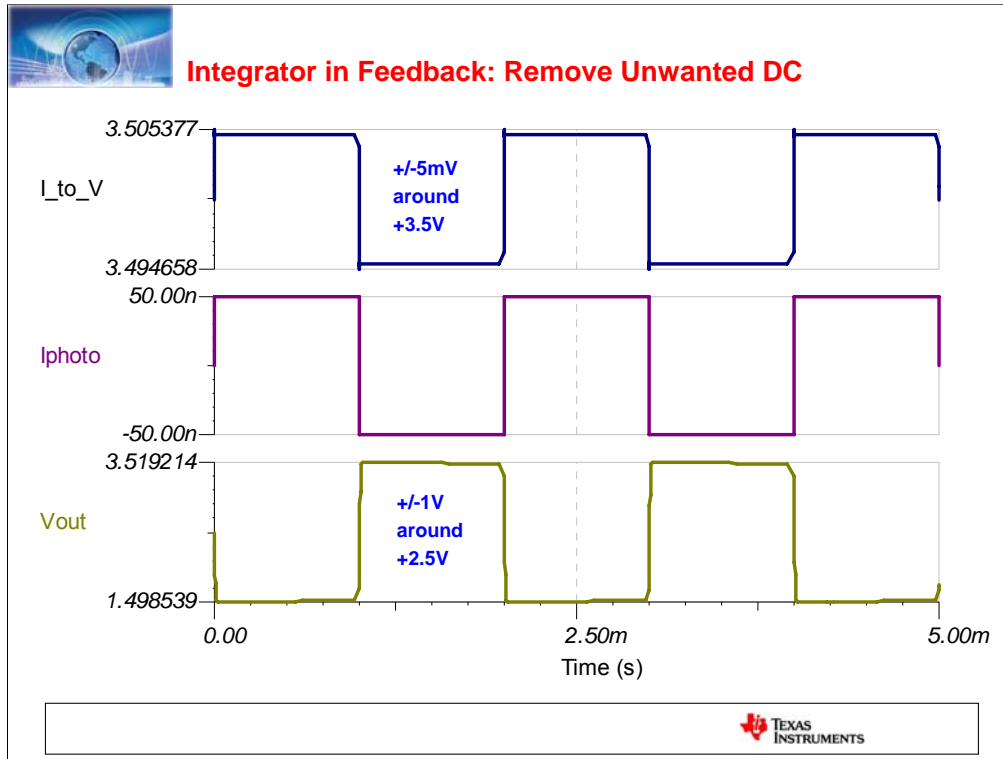
Integrator in Feedback: Remove Unwanted DC

Always Check Loop Gain & Compensate for Stability

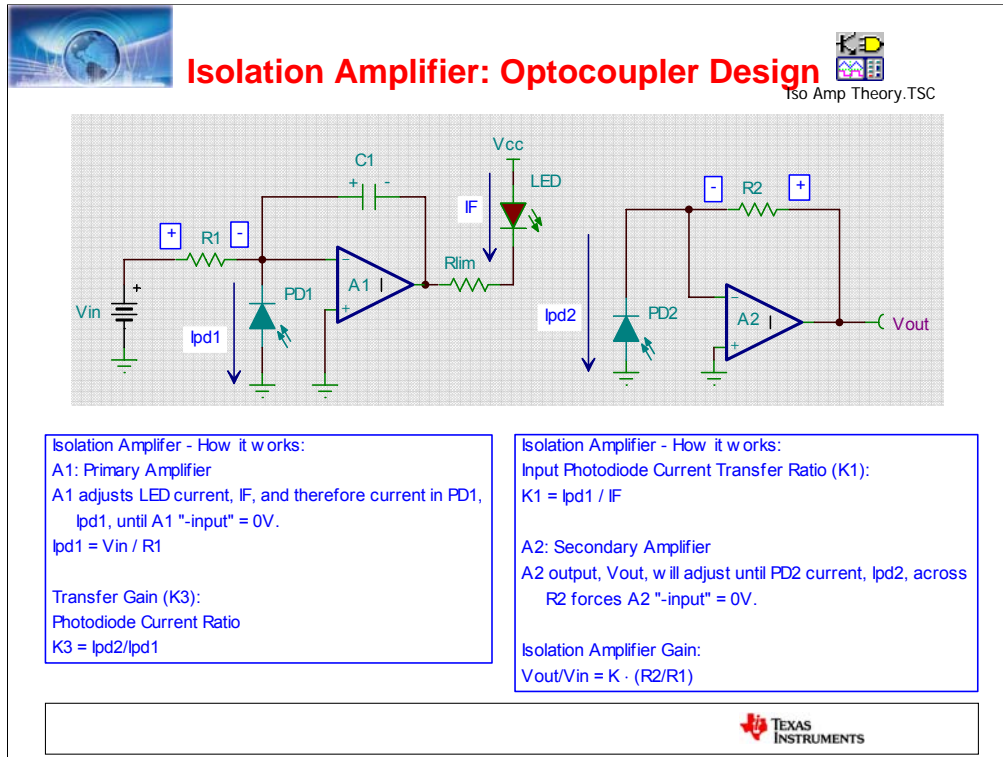
OPA381_single_HP.TSC

TEXAS
INSTRUMENTS

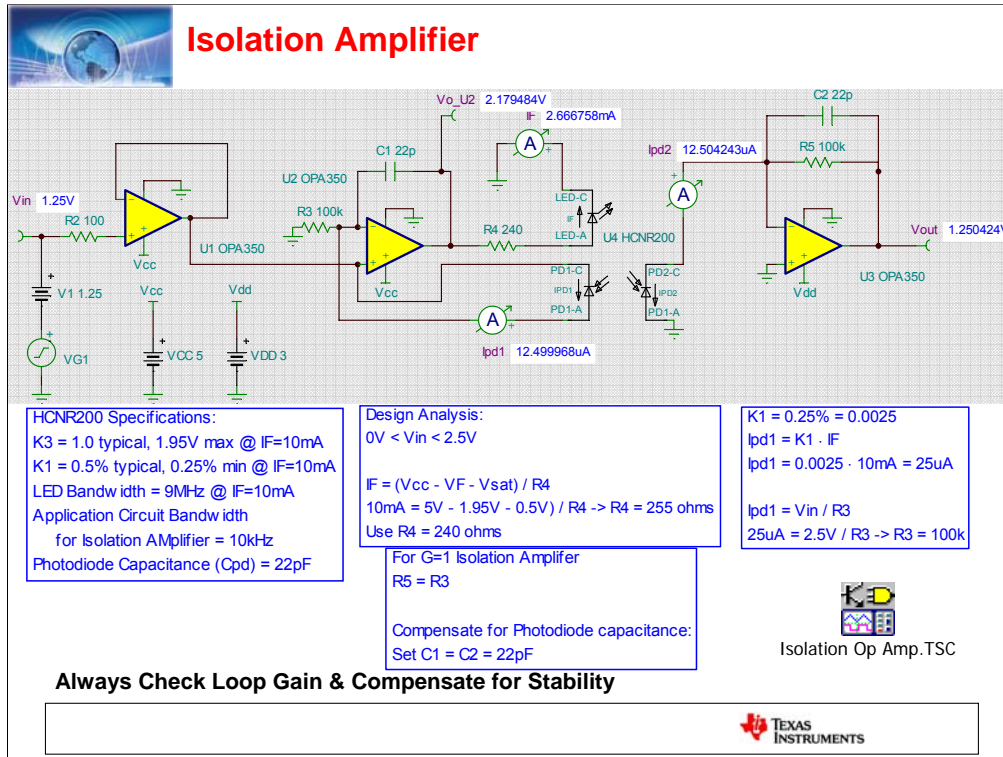
62



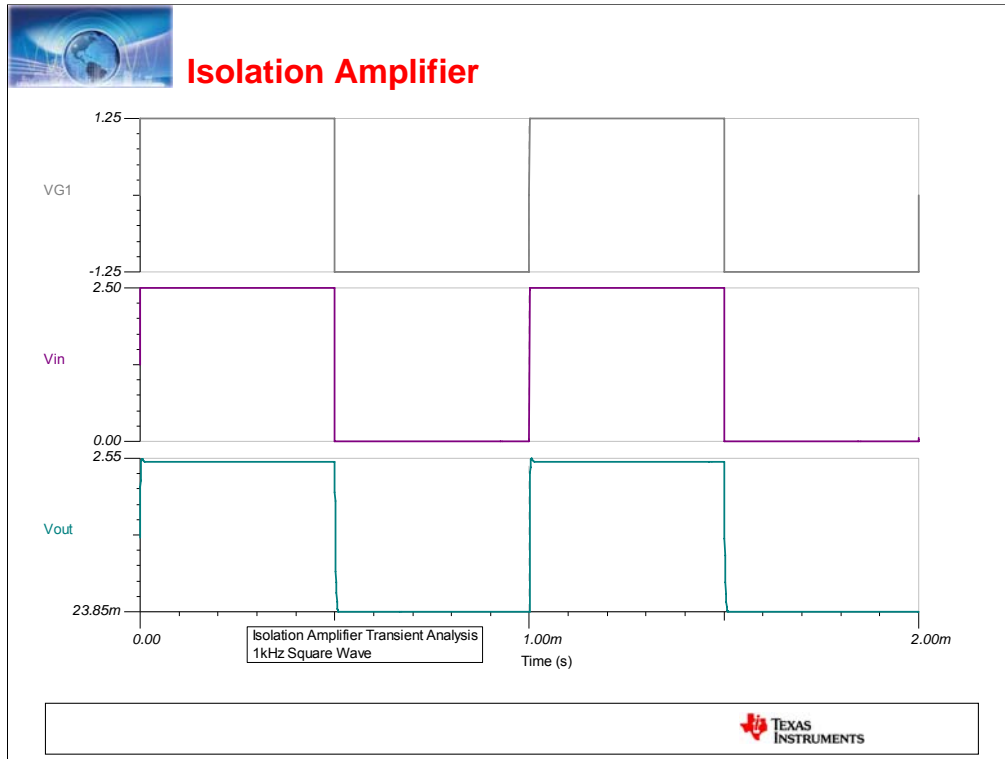
With our Integrator in Feedback we are able to amplify our desired pulsed current of $\pm 50nA$ ($\pm 5mV$ out of U1) by a gain of 200 by rejecting the DC offset out of U1. Now a our $\pm 5mV$ signal becomes a readable $\pm 1V$ signal ! This is all referenced to our 2.5V supply midpoint.



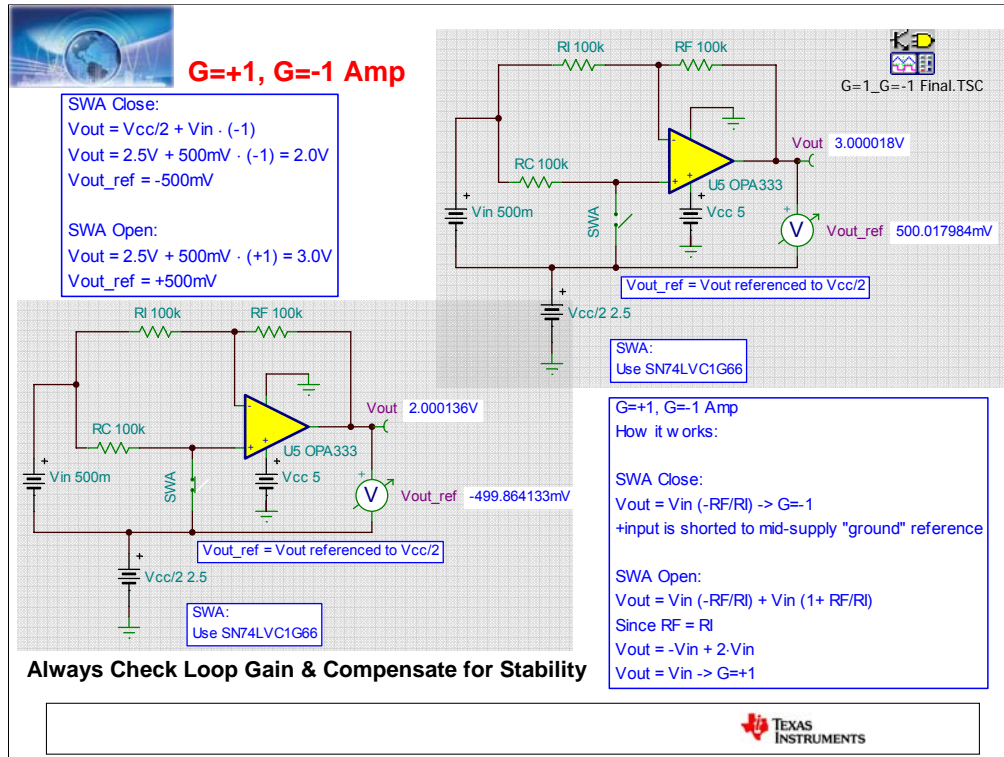
An isolation amplifier is easy to build on a single supply by using a RRIO op amp and an optocoupler. The Isolation Amplifier: Optocoupler Design is detailed in this slide.



A high current drive with close swing to the rail, RRIO, single supply amplifier such as the OPA350 along with a good optocoupler such as the HCNR200 can be used as shown in this slide to build a single supply Isolation Amplifier.



The transient response for our Isolation Amplifier is shown here with excellent results.

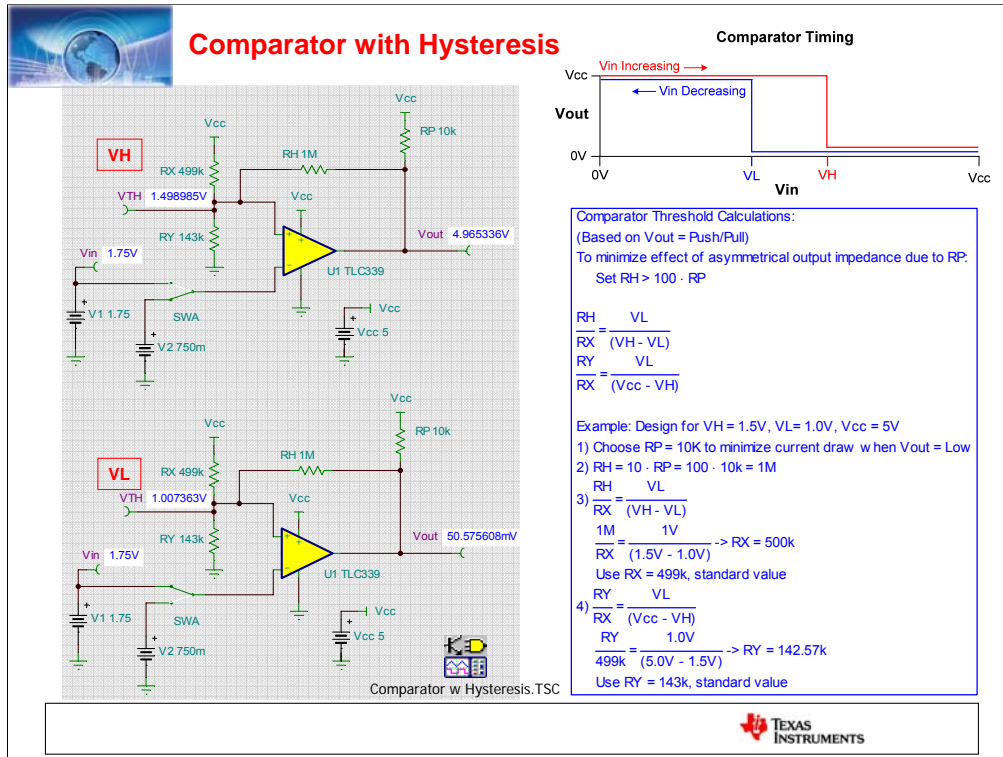


This handy circuit uses a single supply op amp, OPA333 and one single supply, single gate switch, SN74LVC1G66 to create a digitally controlled G=1, G=-1 Amp. For our single supply application Vcc/2 can be viewed as ground. With SWA closed no input signal is driven into the +input of Y5 and therefore we have an inverting amplifier with G=-1. When SWA is opened signal is available on the +input of U5 and we having a summing amplifier that yields a net gain of G=+1 !

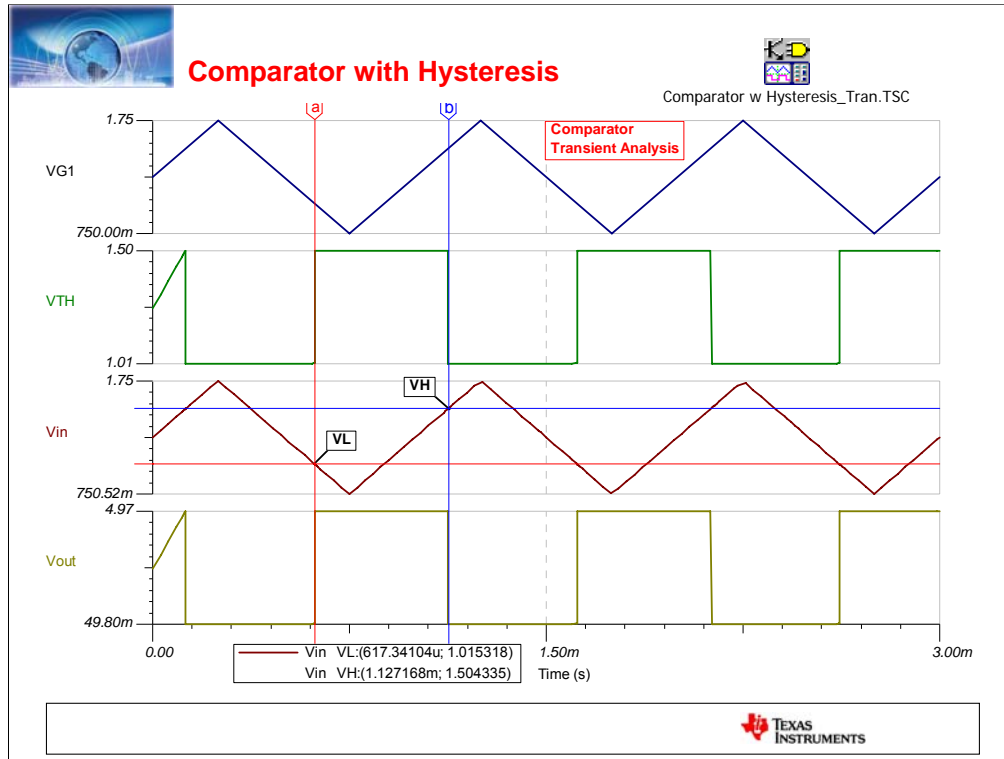


Comparator Circuits

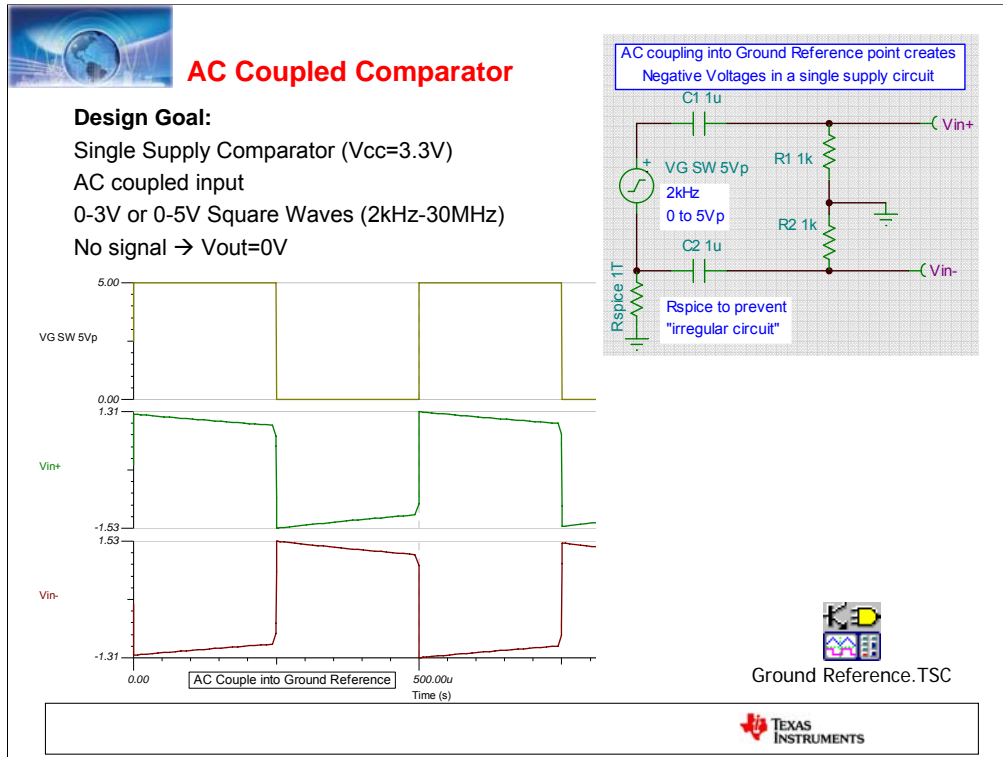
Comparator with Hysteresis
AC Coupled Comparator



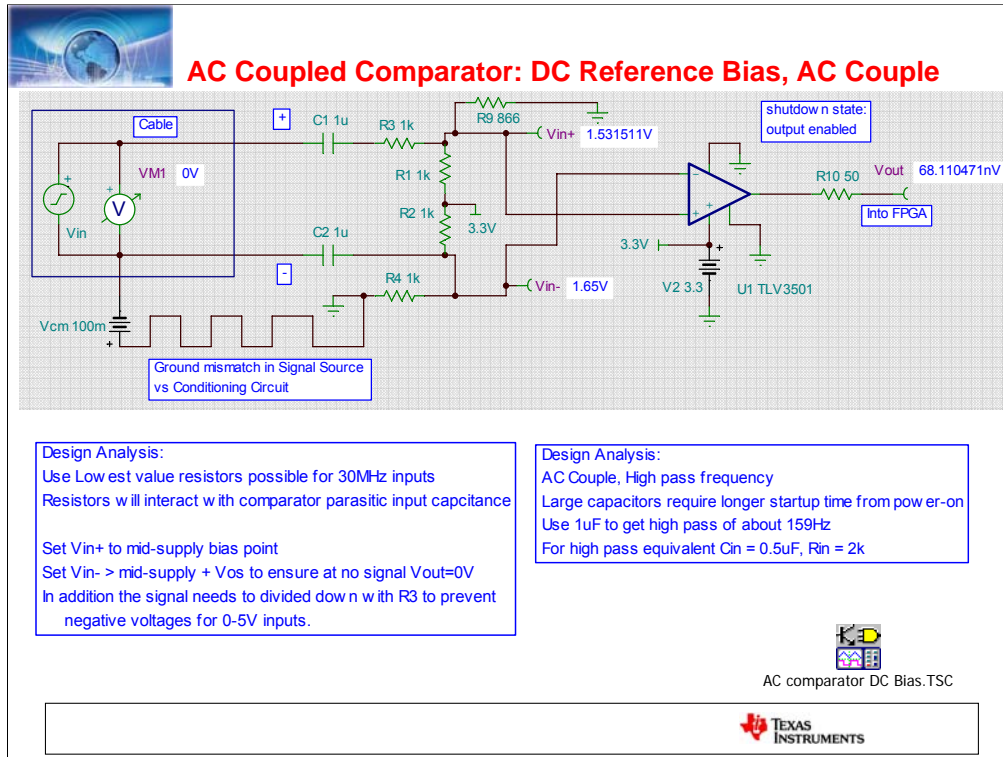
A common comparator circuit is shown here. Easy to use formulae are given to compute the positive and negative going thresholds. The formulae are based on a push-pull comparator output which is low impedance with respect to R_H , the resistor used to add hysteresis to the circuit. However, the formulae can be used to produce very good results when using an open drain comparator with a pull-up resistor, R_P . If R_H is set 10 to 100 times greater than R_P then the accuracy of the formulae will be sufficient for most applications. If not a more detailed analysis will be required.



The results of our transient analysis test for our comparator with hysteresis circuit are shown above.



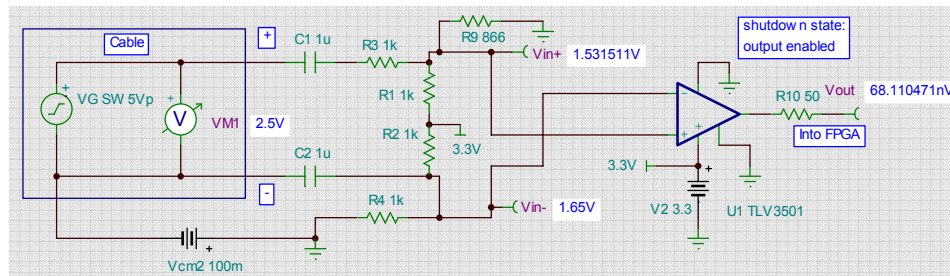
Sometimes a single supply comparator is required to use AC coupling to detect sine waves or square waves. Whenever AC coupling is involved into single supply circuitry negative voltages become a concern. Excessive negative voltages on comparators can cause the to trip erroneously or to stay stuck at unpredictable levels. For our AC Coupled Comparator example our design goals are detailed in this slide.



There are two design concerns in our AC Coupled Comparator circuit: DC Reference Bias circuitry and AC Couple circuitry. The design details of how to accommodate each of these concerns is shown in this slide.

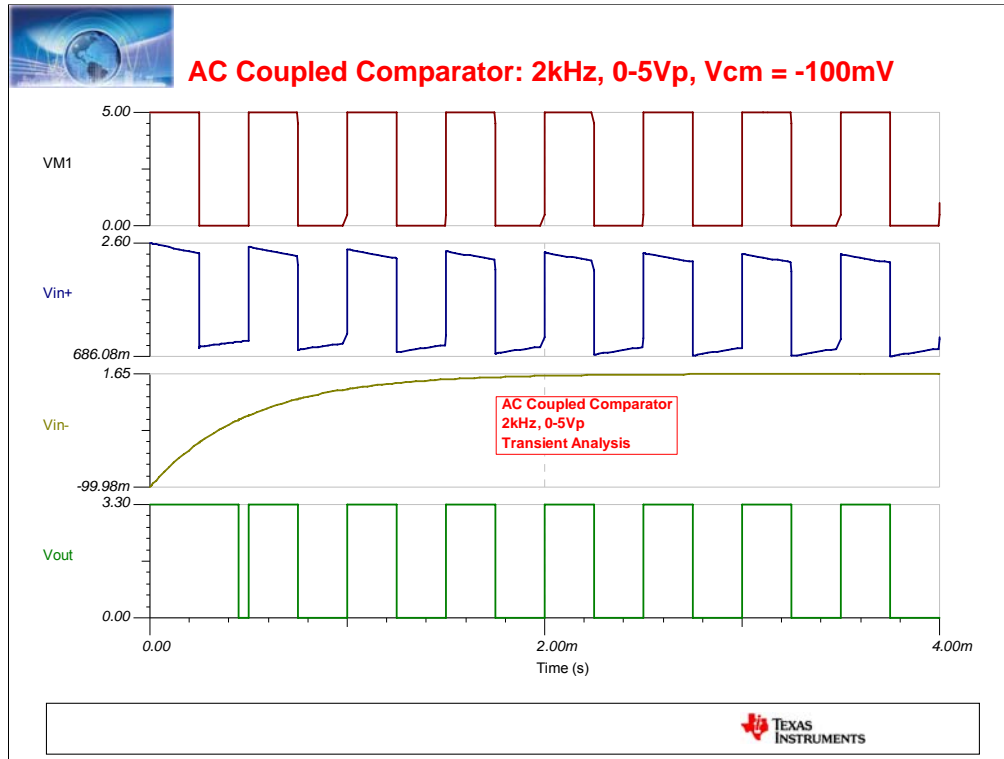


AC Coupled Comparator: Transient Test Circuit

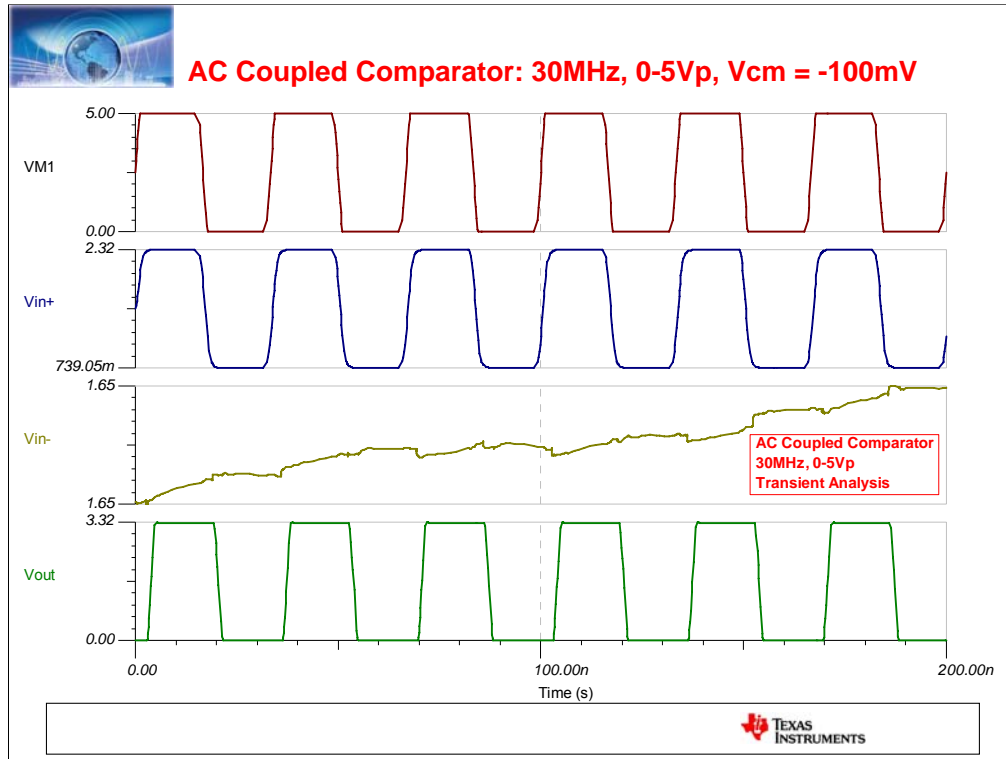


AC comparator couple_Square.TSC





The transient analysis results of our AC Coupled Comparator for 2kHz, 0-5Vp, Vcm = -100mV are shown here.



The transient analysis results of our AC Coupled Comparator for 30MHz, 0-5Vp, Vcm = -100mV are shown here.



Want More Op Amp Stone Soup?

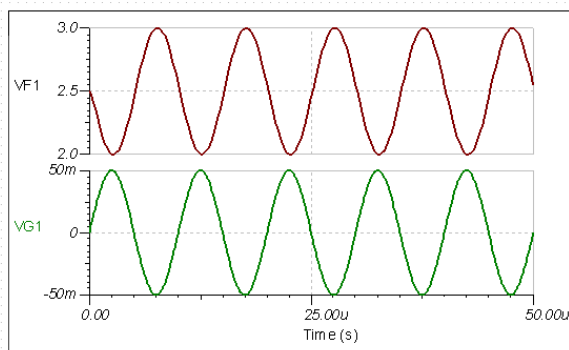
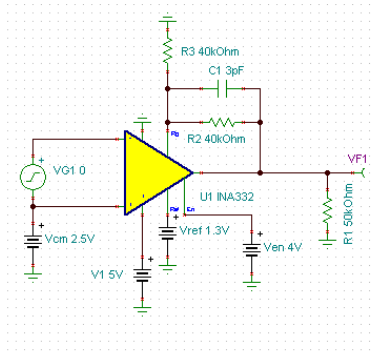
TINA-TI is free and waiting for you !





TINA-TI SPICE Simulator

Unlimited Op Amps
Unlimited Nodes
150+ "Canned" Application
Circuits



Free Download at:

<http://focus.ti.com/docs/toolsw/folders/print/tina-ti.html>

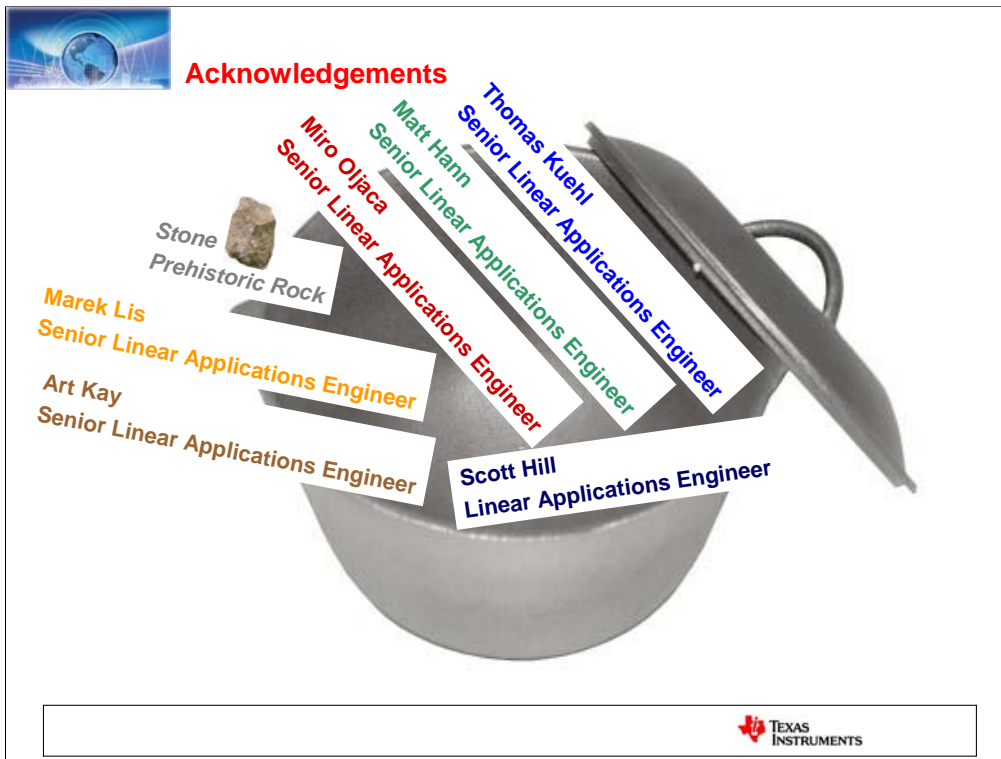
Or Type "TINA-TI" in Keyword Search





Acknowledgements

References





References

Neil Albaugh, Senior Applications Engineer (Retired), Texas Instruments

David Jones, Vice President - Precision Analog (PA), Texas Instruments

"Precision Full Wave Rectifier, Single Supply" Internal design idea

University College of Engineering & Technology Malaysia

"Chapter 5 FET" – MOSFET and JFET detailed operation and curves

notes.ump.edu.my/fkee/BEE2213%5BBEN%20AND%20BEP%5D/Lecture%20notes/Chapter%205%20FET.ppt

Hewlett Packard

"High-Linearity Analog Optocouplers; HCNR200/HCNR201 Technical Data" - Datasheet
Isolation Amplifier Design and Operation Details.

Dave Van Ess, Principal Applications Engineer, Cypress Semiconductor

"Comparator Hysteresis In A Nutshell"

<http://www.analogzone.com/index2.htm>

