Why Use a 24-Bit Converter When You Only Need 12-Bits?

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The initial approach for an Analog to Converter system is to look at the resolution that you need and use an ADC which gives you comparable resolution. To get the required accuracy or precision, you add to the system the necessary gain modules so that the analog range of interest covers the dynamic range of the ADC.

This presentation will explain how you can use a 24-bit converter to eliminate input amplifiers as well as their contributed offset, drift, and noise for a 12-bit system. The 24-bit converter leads to a simpler solution that is easier to lay out and achieve better performance for about the same or better cost. The 24-bit converter gives an immediate system gain advantage of 2048 for the same resolution as well as a PGA function, which can increase the gain by another factor of 64 to 128. You might finish your design by only using a portion of the 24-bit ADC range, but you will still achieve the same resolution and accuracy of the 12-bit system.

Discussion Agenda

- Review the design process
- Why 12-bits might be our initial expectation
- Types of low speed measurements
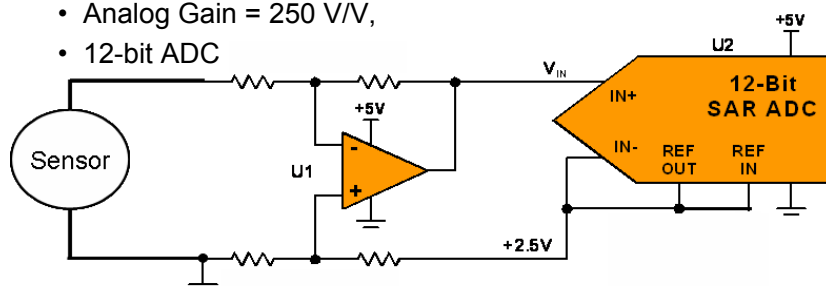- Comparison of 12-bit and 24-bit systems

TEXAS INSTRUMENTS

Many times a low cost, high performance system can be built by using a 24-bit converter as opposed to using the combination of amplifiers and 12-bit solution. Some typical applications for a load cell and temperature sensor will be evaluated and both approaches compared. We will find that the wide dynamic range of the 24-bit solution eliminates external amplification with lower noise results.

We will look at the design process and why a 12-bit converter might be our initial targeted device. By evaluating a few different types of low speed measurement circuits, we will make some comparisons between a 12-bit application or 24-bit bit implementation.

Standard Design Process

- Examine Sensor Output Range
- Design Gain to Match ADC
- Effective LSB = FS voltage / Gain / 2^N
  - Effective System LSB = 4.88 μV if
    - Full-Scale Voltage Range = 5V,
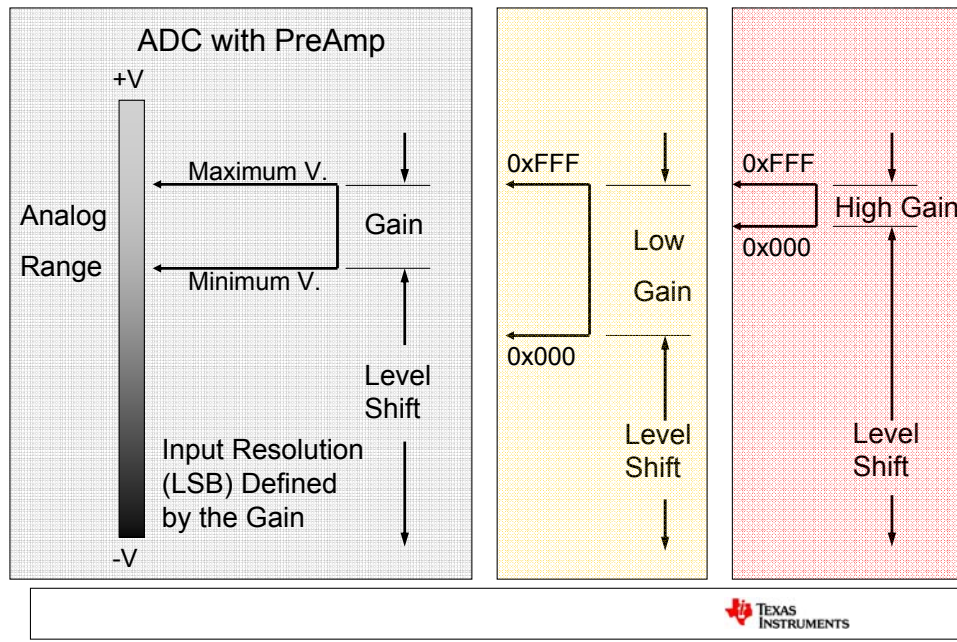   - Analog Gain = 250 V/V,
    - 12-bit ADC

As a first step in your design process, you often look at the sensor that you are going to use and then look at the sensor's output range. You then match the sensor's output range to the A-D converter input. In this process, you may find that you need to use an analog gain cell to make the sensor/ADC match-up work. With this approach you will have an effective system LSB, which comes from your full scale voltage divided by the analog gain and the number of ADC bits.
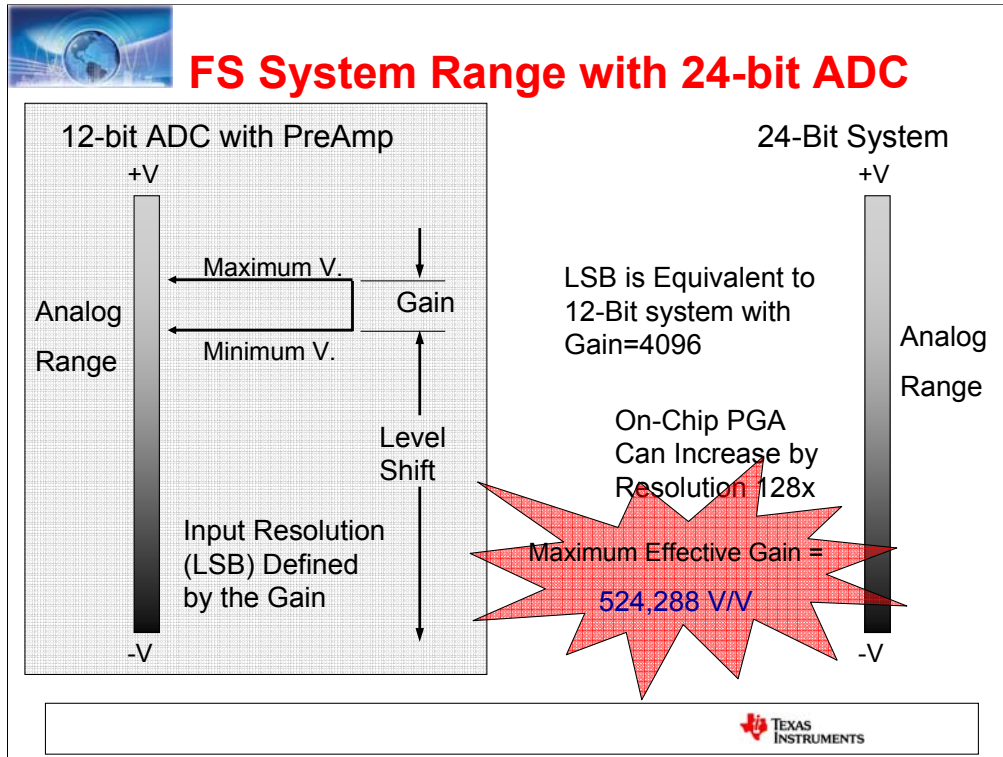
If for instance, you have a 5V range with an analog gain of 250 V/V with a 12-bit system, the system LSB is equal to 5V /250 / 2^{12} or 4.88 μV. In this slide, an example of a 12-bit system shows a sensor connected through an amplifier that has gain, a 2.5V signal level shift, and a 12-bit SAR converter.

FS System Range vs Gain

ADC with PreAmp

+V

Maximum V.

Analog Range

Gain

Minimum V.

Level Shift

Input Resolution (LSB) Defined by the Gain

-V

0xFFF

Low Gain

0x000

Level Shift

0xFFF

High Gain

0x000

Level Shift

TEXAS INSTRUMENTS

Another way to look at this is to think of the analog output voltage range of your sensor. The gain and an analog level shift brings out a portion of the signal range. That signal range becomes the minimum and maximum output codes for your A to D converter. If you have low gain, you use a bigger portion of the sensor signal range and your system LSB would represent a larger sensor voltage step. If you have a higher gain, your system LSB is smaller and you are looking at a very small portion of the sensor output range. In these examples, all of the ADC codes will fit within the range allowed by the analog level shift that comes before the ADC.

FS System Range with 24-bit ADC

12-bit ADC with PreAmp

+V

Analog Range

Maximum V.

Gain

Minimum V.

Level Shift

Input Resolution (LSB) Defined by the Gain

-V

24-Bit System

+V

LSB is Equivalent to 12-Bit system with Gain=4096

On-Chip PGA Can Increase by Resolution 128x

Maximum Effective Gain =

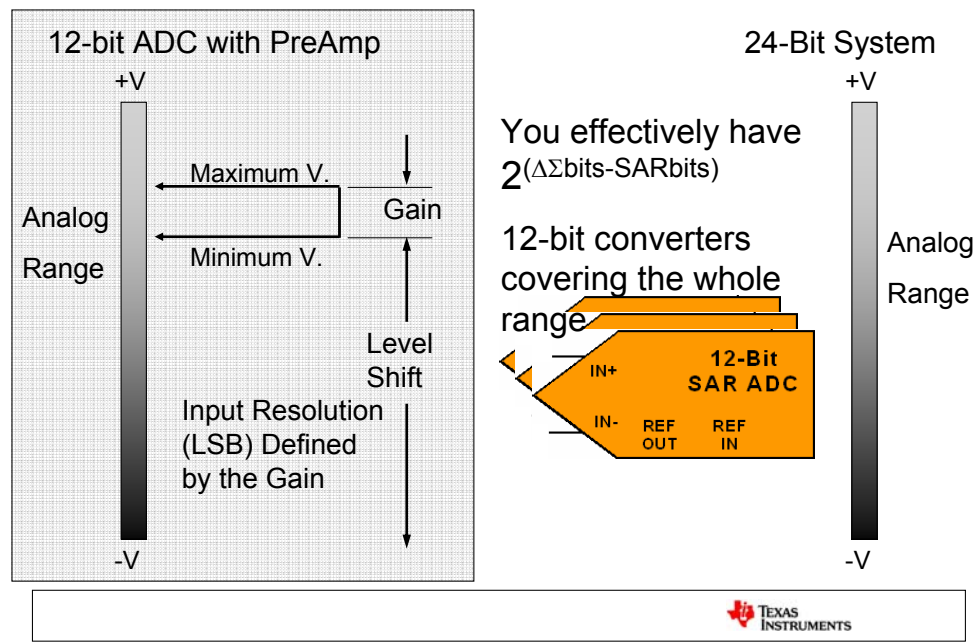524,288 V/V

Analog Range

-V

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Now put the sensor signal into a 24-bit system, with no gain. You can do this because the LSB size of the 24-bit system is equivalent to having an analog gain of 4096. In addition, many of the 24-bit ADCs have on-chip programmable gain amplifiers (PGA). With ADC devices that have an on-chip PGA, you can increase the gain by another factor of 64 to 128 (product specific). When you use the on-chip PGA, you can subtract out the affects of an analog level shifting if you use the differential inputs of the ADC.

This allows you to apply a voltage to your negative ADC input while positioning your positive ADC input with the output of your sensor. Although the total range of the 24-bit ADC is operational, your sensor might only cover a portion of the ADC output codes. By selecting that portion of the ADC range, you can focus on just the area of the signal response.

You will have the full resolution of 2^{24} bits at our disposal, but you can stand to lose some dynamic range, because the goal is only for a 12-bit measurement.

Level Shifting and Gain

12-bit ADC with PreAmp

+V

Maximum V.

Gain

Analog
Range

Minimum V.

Level
Shift

Input Resolution
(LSB) Defined
by the Gain

-V

24-Bit System

+V

Analog
Range

-V

You effectively have
$2^{(\Delta\Sigma bits-SARbits)}$

12-bit converters
covering the whole
range

12-Bit
SAR ADC

IN+

IN-   REF   REF
       OUT   IN

TEXAS
INSTRUMENTS

Having a 24-bit ADC that has an effective resolution of 23 bits is like having 2048 individual, 12-bit converters placed across the range of the converter.

Sensors and Measurements

Sensor	Sensor Resolution	Measurement Goal
Weigh Scale (Load cell)	10mV FS @ 5V excitation	1/1000FS = 10uV
Thermocouples	10-60uV/°C	0.1°C = 4uV (type K)

TEXAS INSTRUMENTS

We are going to look at two sensor applications: a weigh scale (load cell),
and a thermocouple.

A high quality load cell will have a 2mV/V output. This means that for each volt of excitation you will get 2 mV of the full-scale output. With an excitation of 5V and a full sensor deflection, the maximum output is 10mV. If you want the reading to be stable, the measurement goal must also be noise-free.

Since we are only looking at 12-bit applications, this full-scale 10mV might represent 250 lbs for a bathroom scale. If we want ¼ pound resolution, we will have 1000 points of measurement output. That's not a very big signal, and if we want to look at something that is 1000th of the full-scale range, we need to distinguish a change of 10 µV. This is done by keeping the peak-to-peak noise to be less than 10 µV for 99.999% of the time.

Effective Number of Bits (ENOB)

- **Effective Number of Bits (ENOB) :**
  - Specification for AC signals
- **ENOB ⇔ SINAD ⇔ THD+N ⇔ SNR+D**

- **IEEE-1241 says**

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

$$SINAD_{(dB)} = -20\log_{10}\sqrt{10^{-SNR/10} + 10^{+THD/10}}$$

- **Ideal converter**
  - **SINAD = SNR = 6.02N + 1.76dB**
    - **SNR ⇒ Signal-to-Noise Ratio**
    - **THD ⇒ Total Harmonic Distortion**

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INSTRUMENTS

For AC input signals, ENOB (or SINAD) is one of the critical specifications for applications such as digital oscilloscopes, video, or wideband digital receivers.

If you are testing with an AC input, IEEE-1241 and some manufacturers use ENOB numbers to describe an ADC's performance. In the AC environment ENOB is calculated from the converter's SINAD, which is the same as THD+N or SNR+D.

SINAD is the calculated combination of the converter's signal-to-noise ratio or SNR and Total Harmonic Distortion or THD. In this simple formula for ENOB, the 6.02 is a multiplier of a 20 log base ten of the converter's bits and 1.76 is the quantization noise. In this instance, RMS stands for the signal's root-mean-square.
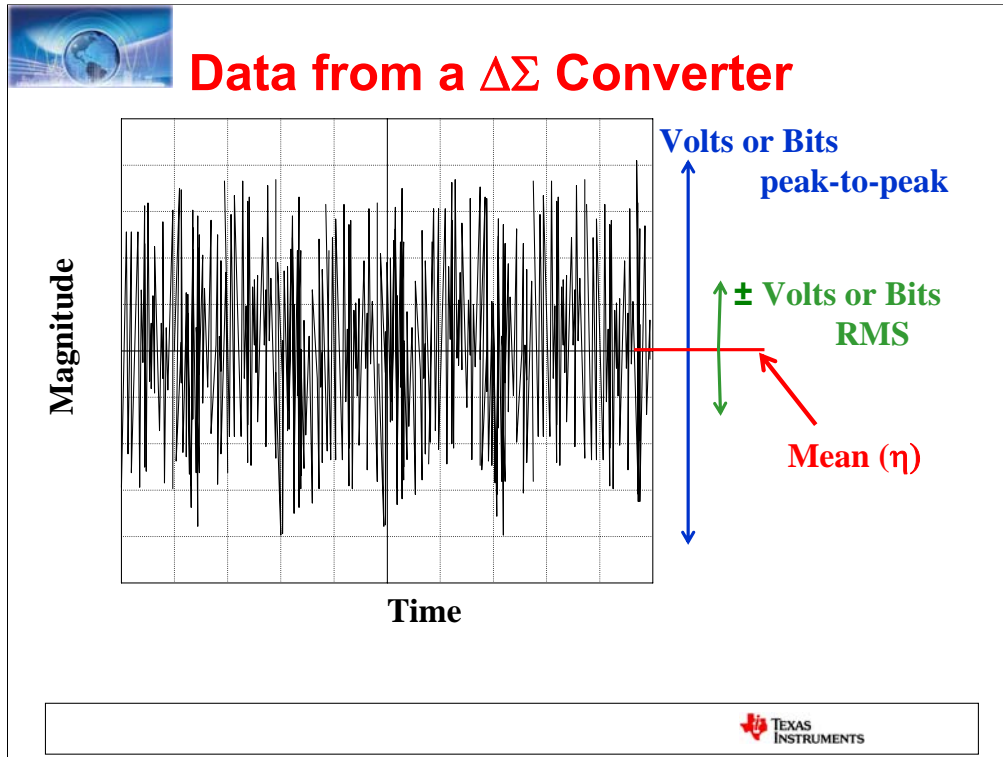
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Effective Resolution (ER)

- Effective Resolution (ER) :
  - Specification for Oversampling Systems

- ER $\Leftrightarrow$ standard deviation (σ) $\Leftrightarrow$ RMS

  - ER = N - $\log_2(\sigma)$

    where σ = standard deviation of data
    and N = number of converter bits

TEXAS INSTRUMENTS

Another technique you can use to find the ENOB of a converter is to measure a DC input signal. The most common measurement for oversampling converters or a Delta-sigma ADC is to look for the RMS noise. In this case RMS is equal to one standard deviation of a set of data. Another term that is used to describe the delta-sigma converter's ENOB is Effective Resolution (ER). This is a critical specification with load cells and thermometers.

Both ENOB and ER are usually specified as RMS numbers.

As we go forward, be aware of the ENOB and ER pitfalls. ENOB and ER are only a figures of merit. These specs do not describe the operation of the entire converter over the ranges of sampling frequencies and power supplies. In particular, you are going to find that we exclude the DC specifications such as INL, DNL, offset error, and gain error. The ENOB spec doesn't even differentiate the AC specifications and you will find that SFDR doesn't fit into the calculation of ENOB at all.

Every time you describe a converter with an RMS number you're talking about the range that spans plus and minus standard deviation limits of several output data points.
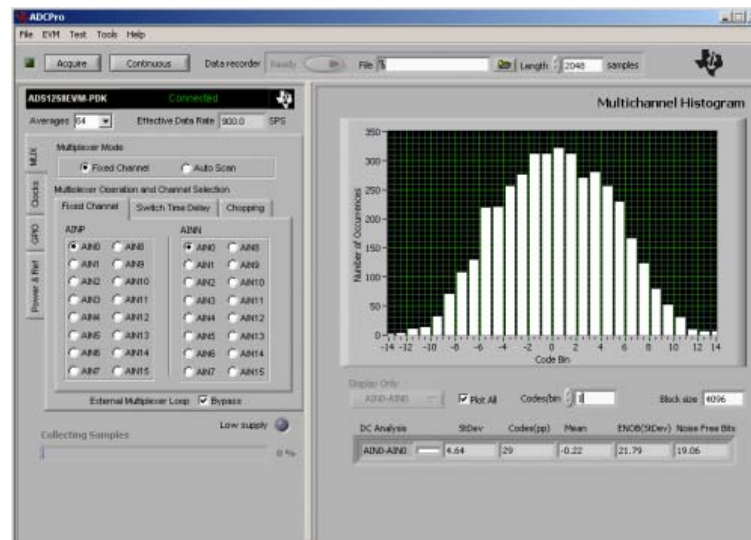
In this diagram you can see a group of a converter's results. There are three points that are interesting in this graph.

The first is the mean value. The mean, or average value of the data, is a reference point and you need it when you calculate the standard deviation of the data. The volts-RMS or bits-RMS are equivalent to a span from the negative standard deviation to the positive standard deviation of the data.

If you are going to place the converter results in a display, volts peak-to-peak or bits peak-to-peak determine how often the lower digits in your display change.
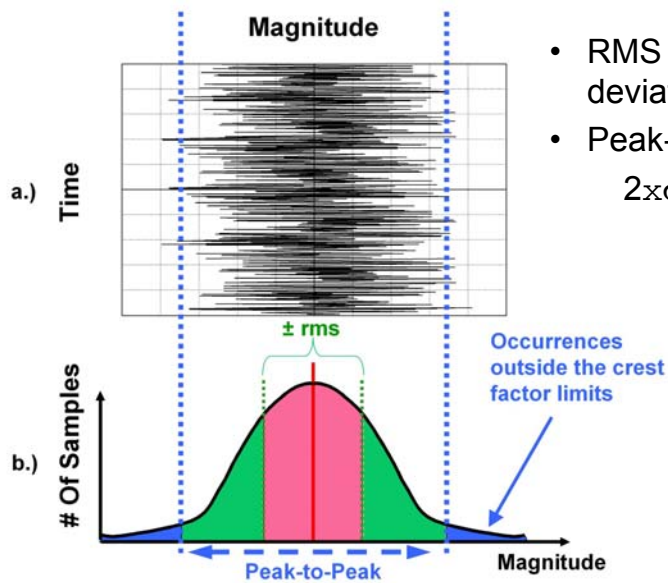
Histogram of Data

Device or converter noise is a random event, but it does follow probability theories. If you plot the output data from a converter that has a DC input, you can build a histogram. If you collect over 1000 data points, this histogram will approach the shape of a Gaussian distribution or a bell shaped curve. Your histogram contains the noise that is generated by the converter.

If you apply a DC signal to the ADC and record a large number of samples, the result will be a distribution of codes. This measurement is taken by appling 0V and shorting the differential inputs of the converter together. That's why the center code in this hystogram is zero. You can find the standard deviation of the data and ER underneath this hystogram plot.
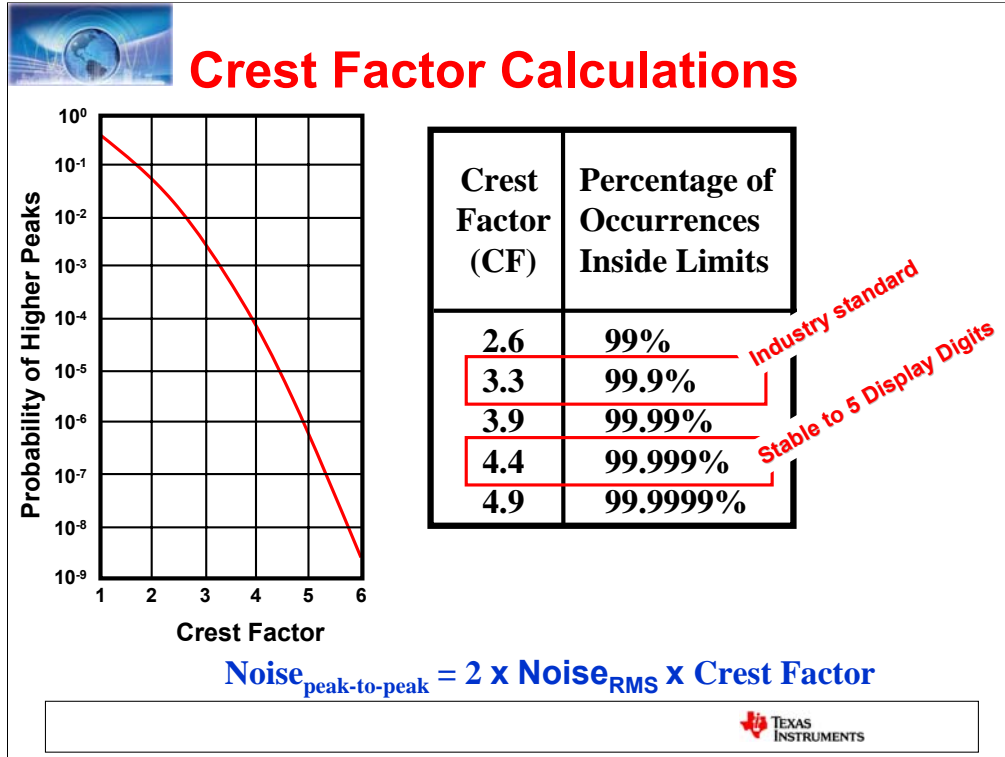
Statistical Terms Defined

- RMS $\Leftrightarrow$ standard deviation (σ)
- Peak-to-peak = $2 \times \sigma \times$ Crest Factor

With the Gaussian distribution in our histogram plot you can see that your RMS limits exclude a lot of data. If you look at the number of converter output results between the two standard deviation limits you account for 68% of the occurrences, but if you multiply the doubled standard deviation by a constant or "crest factor", you can expand the percentage of occurrences underneath the curve. The crest factor allows you to define your peak-to-peak limits.
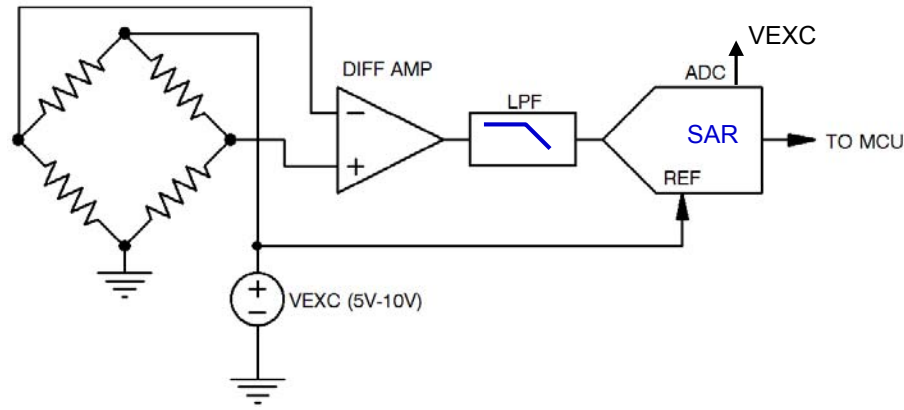
Crest Factor Calculations

Crest Factor (CF)	Percentage of Occurrences Inside Limits
2.6	99%
3.3	99.9%
3.9	99.99%
4.4	99.999%
4.9	99.9999%

Industry standard

Stable to 5 Display Digits

$$\text{Noise}_{\text{peak-to-peak}} = 2 \text{ x Noise}_{\text{RMS}} \text{ x Crest Factor}$$

The crest factor for noise occurrences is a statistical estimate that determines the probability that an occurrence of a noisy event will remain within a defined boundary.

The technique of predicting the allowable fluctuation in your data display is relatively simple. After you choose your crest factor, which is based on the number of noise events that will remain within your limits, you multiply the value of two standard deviations times your selected crest factor. This is how you define the peak-to-peak noise response of your system. With this technique you actually determine the percentage of output data results that will keep below your display digits and out of sight. The industry standard crest factor is 3.3 which is appropriate for a three digit display. If you want to keep a five digit display stable, you would use a crest factor is 4.4.

In our examples sensor circuits we will use a crest factor of 4.4.

12-bit System Amplifier + ADC

This is common circuit for bridge measurements uses a SAR converter. The signal is amplified with a difference or instrumentation amplifier. The gain stage converts the sensor signal from 0-10mV to the converter's input range of approximately 0-5V. The signal is then filtered.

If you look at this 12-bit system, you have an amplifier that provides gain. In this circuit, the level shifting is taken care of with the bridge set up. After the gain stage we go through a low pass filter and then into a SAR converter.
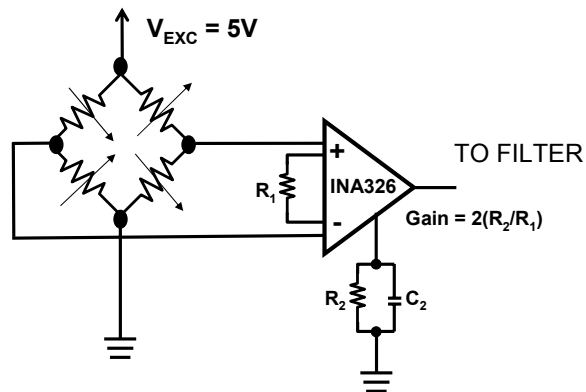
This is your standard type of configuration for a 12-bit system. You notice this is arranged for a ratiometric measurement. This is done by connecting the bridge excitation voltage to reference voltage pin on the ADC. In this configuration, if your reference voltage changes, the error of that change cancels out in the measurement process.

Even though this schematic is shown as a ratiometric design, the actual layout and implementation can destroy the ratiometric benefit. For example, if the excitation voltage is placed next to the REF input of the ADC and a long wire carries the signal to the load cell, the load cell will not see the same voltage as the ADC. Similarly, if the ground connection between the load cell and the ground input of VEXC has additional impedance and ground currents, that also will defeat the ratiometric benefit.

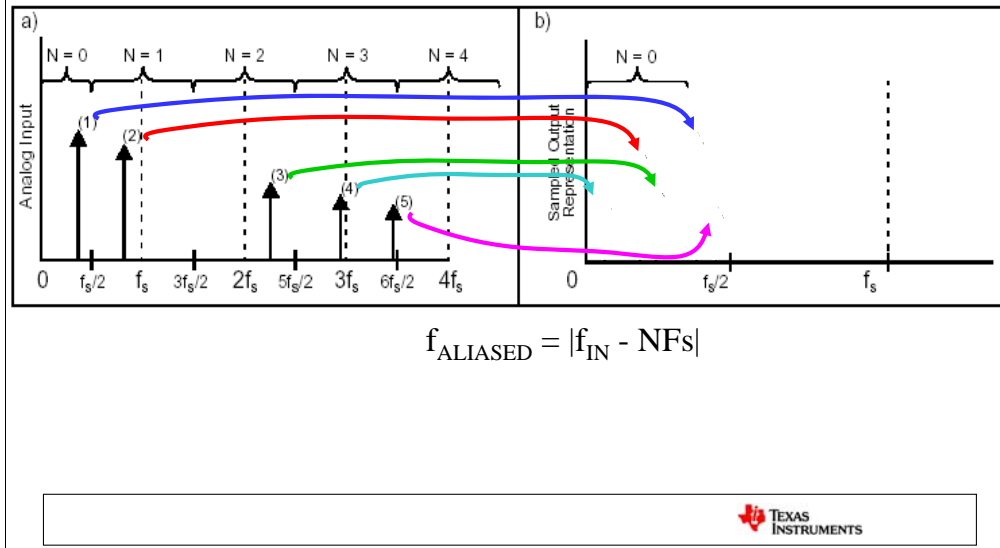**12-Bit ADC + INA326 Load Cell System**

- Load Cell FS = 5×2 mV/V = ±10 mV
- System Full Scale = 10 mV $\times$ 250 = ± 2.5 V
- System LSB = 2.44 uV

V_{EXC} = 5V

TO FILTER

R_1

INA326

Gain = $2(R_2/R_1)$

R_2 C_2

In this slide, the load cell bridge has an excitation voltage of 5 V. As the load cell operates with a 2 mV/V specification, the maximum output range is ±10 mV. The INA326 follows the load cell with a gain of 250 V/V. Our system full scale voltage (250 x ±10 mV) produces a ±2.5 V full scale signal.

Nyquist Theorem

$$f_{ALIASED} = |f_{IN} - NFs|$$

A/D Converters are usually operated with a constant sampling frequency when digitizing analog signals. By using a sampling frequency (f_S), typically called the Nyquist rate, all input signals with frequencies below $f_S/2$ are reliably digitized. If there is a portion of the input signal that resides in the frequency domain above $f_S/2$, that portion will fold back into the bandwidth of interest with the amplitude preserved. The phenomena makes it impossible to discern the difference between a signal from the lower frequencies (below $f_S/2$) and higher frequencies (above $f_S/2$).
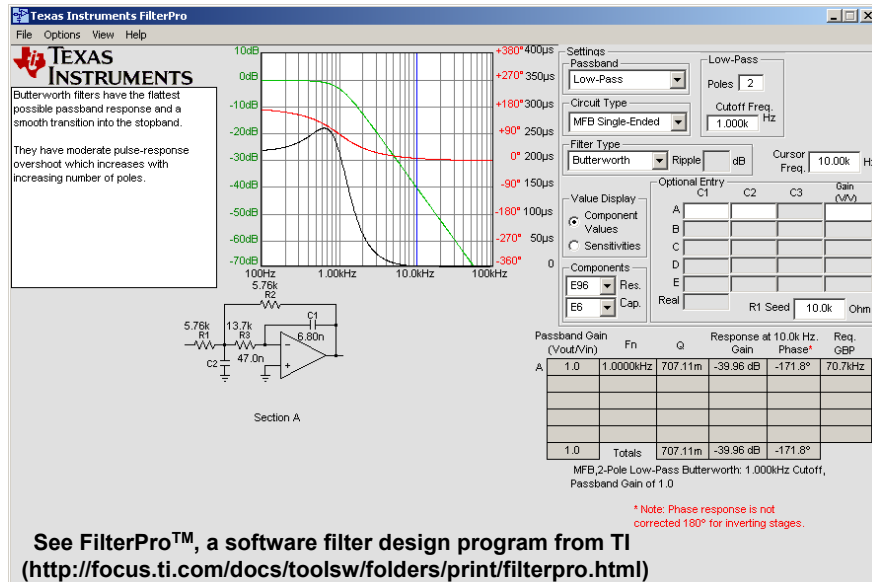
In both parts of this slide, the x-axis identifies the frequency of the sampling system, f_S. The left portion shows five segments of the frequency band. Segment N =0 spans from DC to one half of the sampling frequency. In this bandwidth, the sampling system will reliably record the frequency content and magnitude of an analog input signal. In the segments where N > 0 the frequency content of the analog signal will be recorded by the digitizing system in the bandwidth of the segment N = 0 on the left side of this slide. Mathematically, the higher frequencies (#2, 3, 4, 5) will fold back with the following equation:

$$f_{ALIASED} = |f_{IN} - Nf_S|$$

This fold-back phenomena is illustrated in this slide where signal #2, 3, 4, and 5 appear at lower frequencies.

FilterPro : Filter Design Software

See FilterPro™, a software filter design program from TI
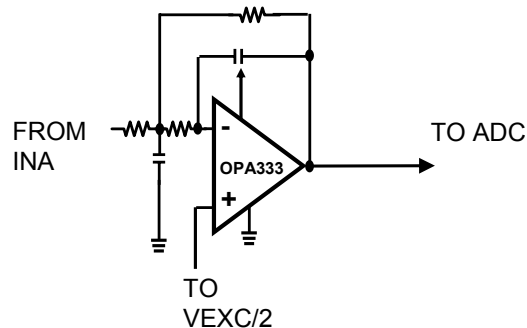(http://focus.ti.com/docs/toolsw/folders/print/filterpro.html)

The good news is that there are a variety of tools available to get you through the logistics (or painful calculations) of implementing discrete low-pass filters. In this slide you see the front page of FilterPro from Texas Instruments. This software is free and downloadable from TI's web site.

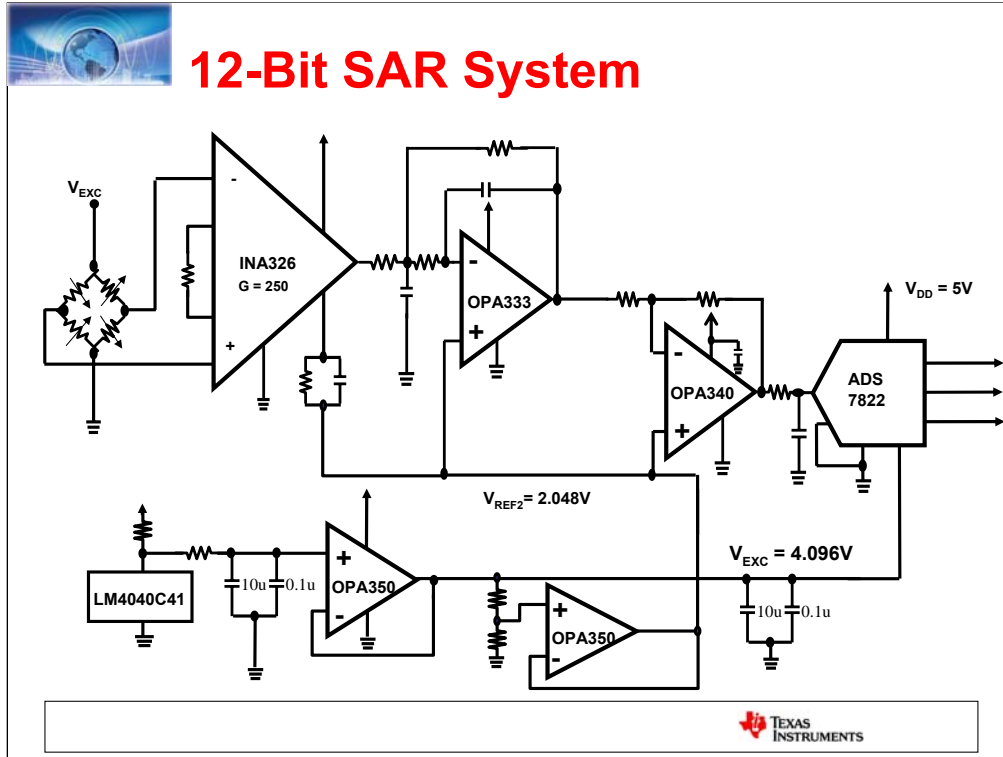http://focus.ti.com/docs/toolsw/folders/print/filterpro.html

Low Pass Filter Design

- 2nd order low-pass filter sufficient
- Filter design program – FilterPro

FROM INA — OPA333 — TO ADC

TO VEXC/2

TEXAS INSTRUMENTS

A system with a 12-bit converter must have an analog filter. The analog filter is always implemented in the signal path prior to the analog-to-digital converter.

The primary function of the low pass analog filter is to remove the high frequency components of the input signal to the A/D converter. If these high frequencies pass to the A/D converter, they will contaminate the conversion data by aliasing during the conversion process.

A second function of the analog filter in our circuit is to reduce noise that exists outside our bandwidth of interest. The load cell in our circuit operates near DC. Limiting the bandwidth with a 10 Hz low-pass filter further reduces the noise in our system.

12-Bit SAR System

This is the final circuit for the 12-bit SAR system. This system includes the sensor, an instrumentation amplifier (INA326), a 2nd order filter (OPA333), ADC driver amplifier (OPA340), and a 12-bit SAR A-D converter (ADS7822).

12-Bit ADC Load Cell System

System Errors (RTI, CF = 4.4)
- INA326
  - Gain = 250V/V
  - Noise (0.1 to 10Hz) =
    1.07 μVp-p
- OPA340, OPA333
  - Noise (0.1 to 10Hz) <
    20 nVrms
- ADS7822
  - Noise = 1.16 μVp-p

- Cost (budgetary)
  - INA326 - $2.40
  - OPA333 - $1.20
  - OPA340 - $0.80
  - ADS7822 - $1.55
- Total - $5.95

TEXAS INSTRUMENTS

In this 12-bit ADC weigh scale system, the load cell bridge has an excitation voltage of 5 V. As the load cell operates with a 2 mV/V specification, the maximum output range is ±10 mV. The INA326 follows the load cell with a gain of 250 V/V. Our system full scale voltage (250 x ±10 mV) produces a ±2.5 V full scale signal. The analog signal is digitized with the ADS7822.
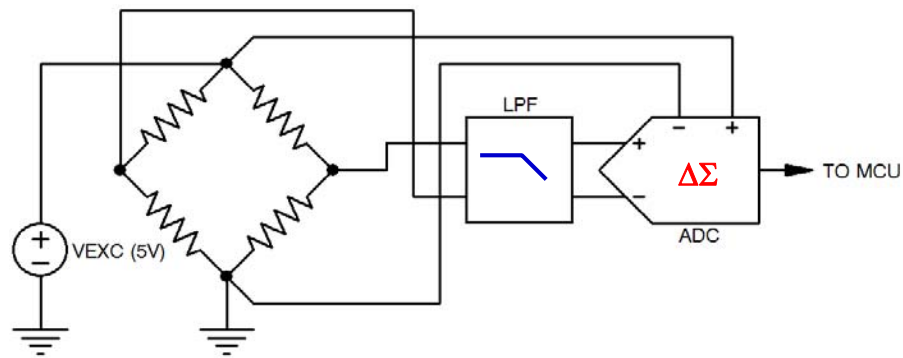
We can scale the load cell excitation voltage to 0.5 volts so that our reference is 0.5V going into our A/D. By doing this our LSB size is 122 µV. By using the 0.5V reference we avoid increasing our offset and other errors by another factor of 10x, however be aware that the ADC noise does not lessen with lower reference voltages.

Looking at some of the errors in the system, the noise of the INA326 (referred to input, RTI) from a 0.1 to 10 Hz bandwidth is about 1.07 μVp-p. The 12-bit converter, ADS7822, dominates the noise figure in this application with a 1.16μVp-p specification over the same frequency range, minimizing the affect of the noise from the INA.
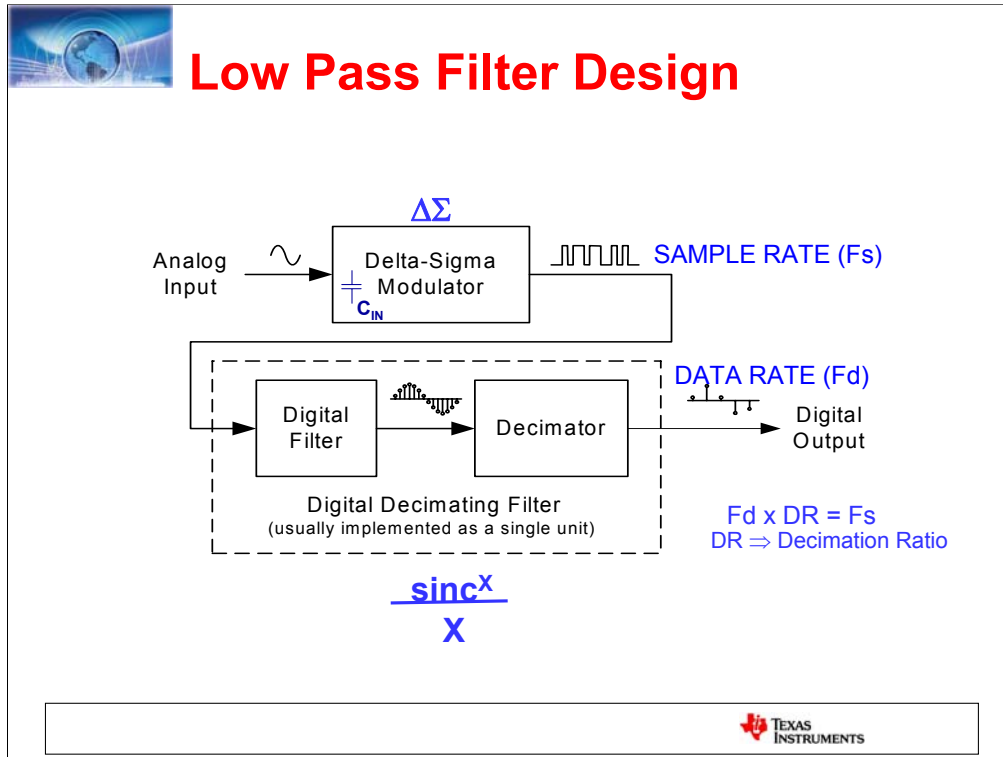
24-Bit System
With Only a Low-Pass Filter

Now lets look at load cell measurement with a 24-bit system. In this case we can take that load cell signa through a low pass filter and into the $\Delta\Sigma$ Analog-to-Digital converter.

Again, this connection is ratiometric. Very few delta-sigma ADCs can accept a reference higher than 5V, so the excitation voltage to the bridge is 5V.

We will talk about the low pass filtering the next slides.

Low Pass Filter Design

$\Delta\Sigma$

Analog Input → Delta-Sigma Modulator C_{IN} → SAMPLE RATE (Fs)

Digital Filter → Decimator → DATA RATE (Fd) → Digital Output

Digital Decimating Filter
(usually implemented as a single unit)

$$\frac{sinc^X}{X}$$

$$Fd \times DR = Fs$$
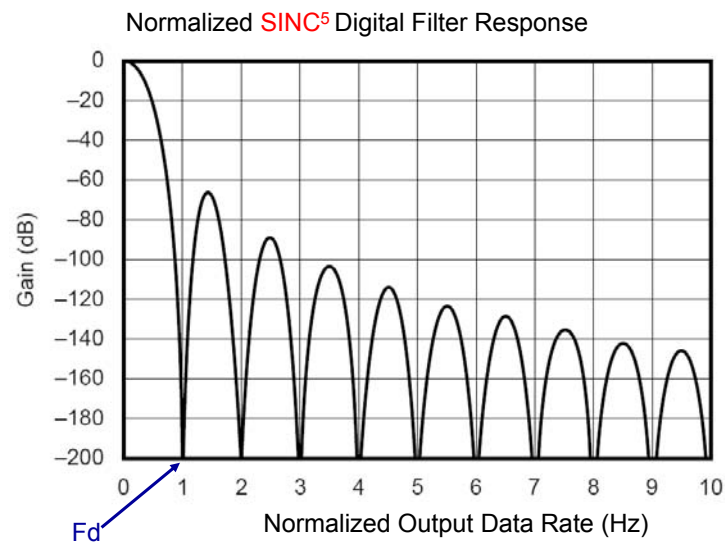$$DR \Rightarrow Decimation\ Ratio$$

TEXAS INSTRUMENTS

This is a block diagram of a delta-sigma A-D converter. For this anti-aliasing filter design we will talk about delta-sigma converters that have SINC digital filter.

As we design our anti-aliasing filter, our focus will be centered on reducing the system signal and noise around the modulator's sampling rate.

The ADC elements that we are going to use in this filter design will be the input capacitance, modulator sampling rate, digital filter characteristics, data rate, and the decimation ratio.
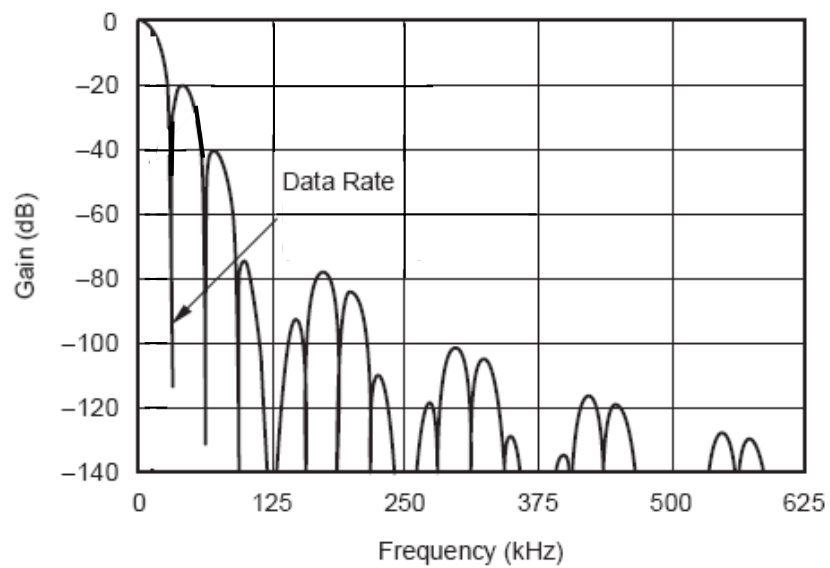
SINC Digital Filter Response

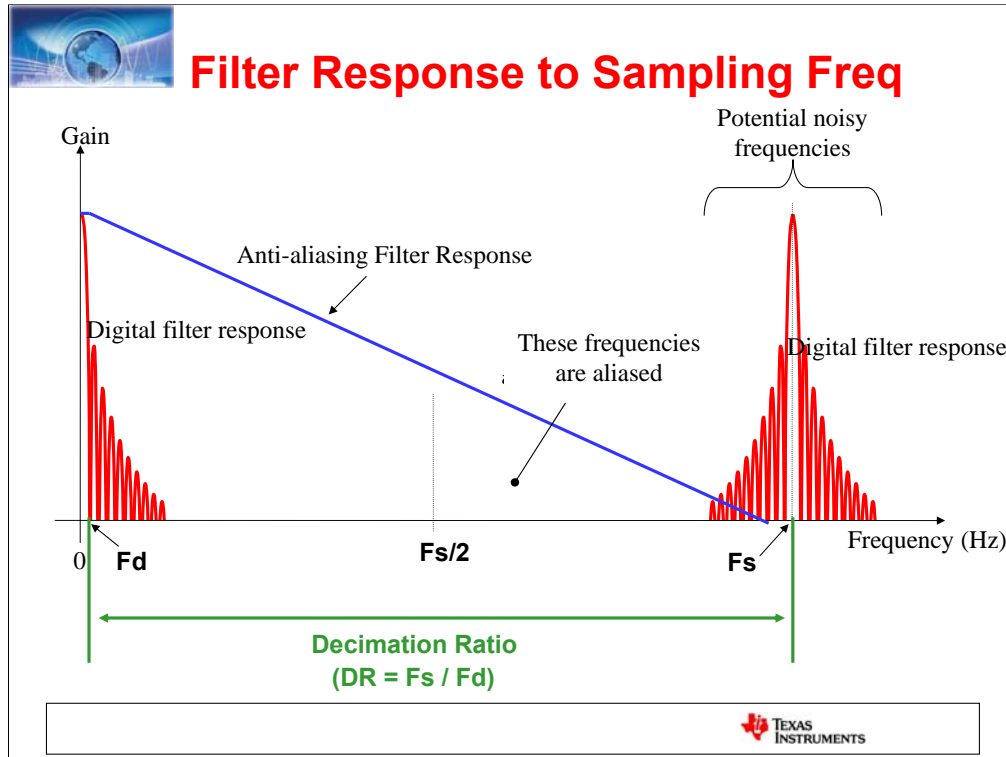Normalized SINC^5 Digital Filter Response

The frequency response of a SINC digital filter looks like a comb. This filter response is from a converter that has a 5th order SINC filter. The frequency of the first null in this diagram is equal to the output data rate of the converter or Fd.
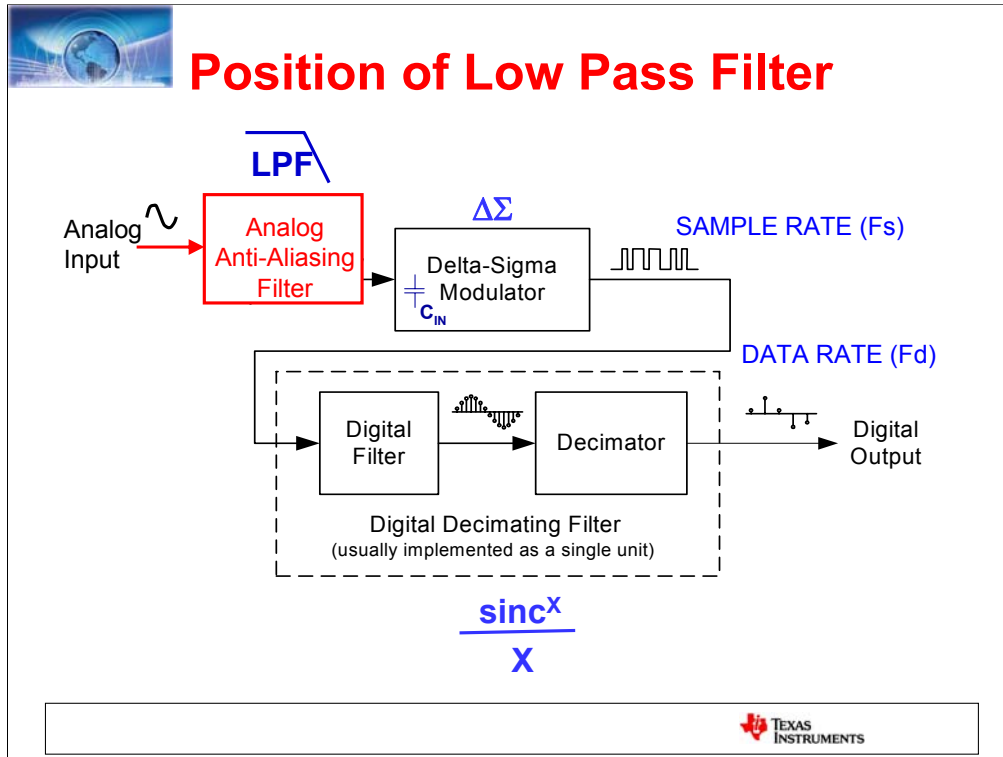
SINC + Averaging Filter Response

This digital filter response is from a converter that has a 5th order SINC filter followed by a four point averaging filter. Once again, the data rate at the output of the converter occurs at the frequency of the first notch.

Filter Response to Sampling Freq

Since a delta-sigma converter is a sampling system, all noise and signals above ½ of the modulator's sampling frequency are aliased back into the bandwidth below the output data rate. The digital filter attenuates a lot of the noise in this area except around the sampling frequency. Usually the amplitude of the noise and signals hovering around the sample rate is small, but noise is a reality and it will be present in your circuit and to make this interesting you are using a high resolution converter that shows that noise in its lower bits.

This is why you'll need a continuous-time filter in front of the delta-sigma converter. The lowest value for your analog filter corner frequency should be Fd. Fortunately, the required strength of this filter is low and a simple RC filter is usually good enough. If your system has a lot of noise or signal around the region of the modulator sampling frequency or if your decimation ratio is less than 100 you may want to consider using a second-order low-pass filter.

Position of Low Pass Filter

We are going to place the analog anti-aliasing or low-pass filter before the input of the converter.

Bridge with Anti-Alias Filter

V_{EXC} (5V)

R_1 R_2 R_5 C_{FLT} $\Delta\Sigma$

R_3 R_4 R_6 R_{FLT}

ADC

to MCU

$$f_{CORNER} = 1 / (2\pi \times C_{FLT} \times R_{FLT})$$

$$R_{FLT} = ((R_1||R_3 + R_5) + (R_2||R_4 + R_6)$$

TEXAS INSTRUMENTS

This is the best option for a passive, 1st order, low-pass filter for a bridge circuit followed by a single channel ADC. This filter has a differential input and output. The filter capacitor (C_{FLT}) not only helps to filter noise, it also reduces charge dumping from the input sampling structure of the delta-sigma converter.

With this filter the corner frequency is equal to 1/ (2 pi (($R_1||R_3 + R_5$) + ($R_2||R_4 + R_6$) * C_{FLT}). With $R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = 350 \Omega$ and C_{FLT} = 2.2 μF, the corner frequency equals 209 Hz. If you increase the values of R_5 and R_6 (which should equal each other) you will reduce the impact of bridge resitance variation on the corner frequency as the sensor responds to its environment.
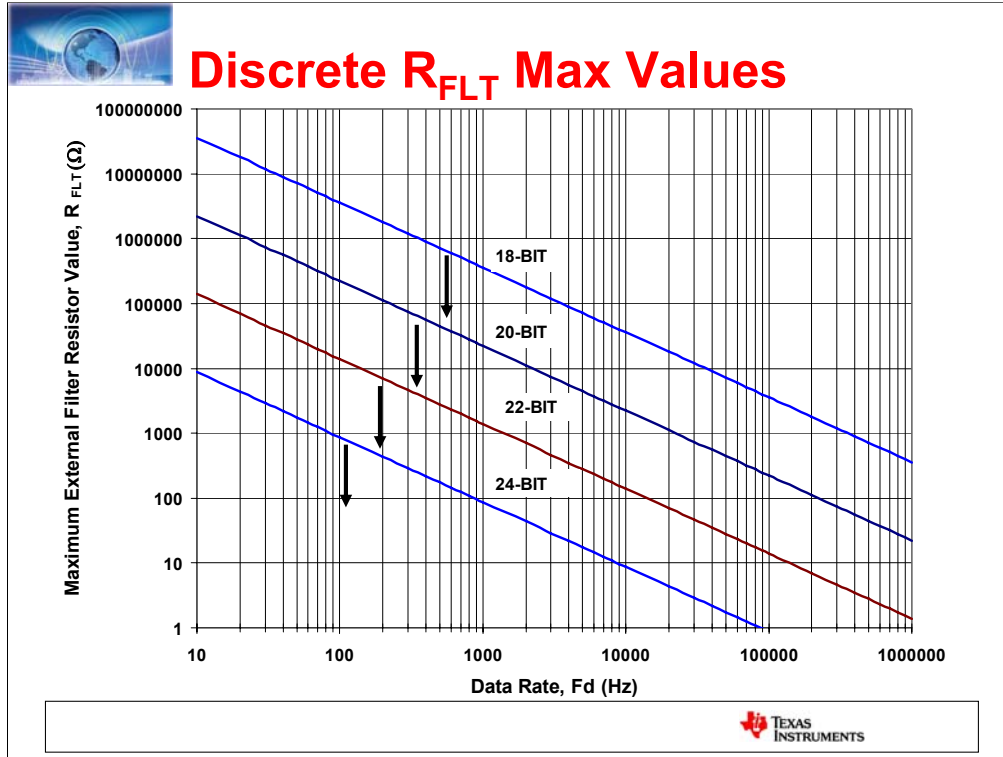
Filter Design Equations

$$f_{CORNER} = 1 / (2\pi \times C_{FLT} \times R_{FLT})$$

$$R_{FLT} = ((R_1||R_3+R_5) + (R_2||R_4 + R_6)$$
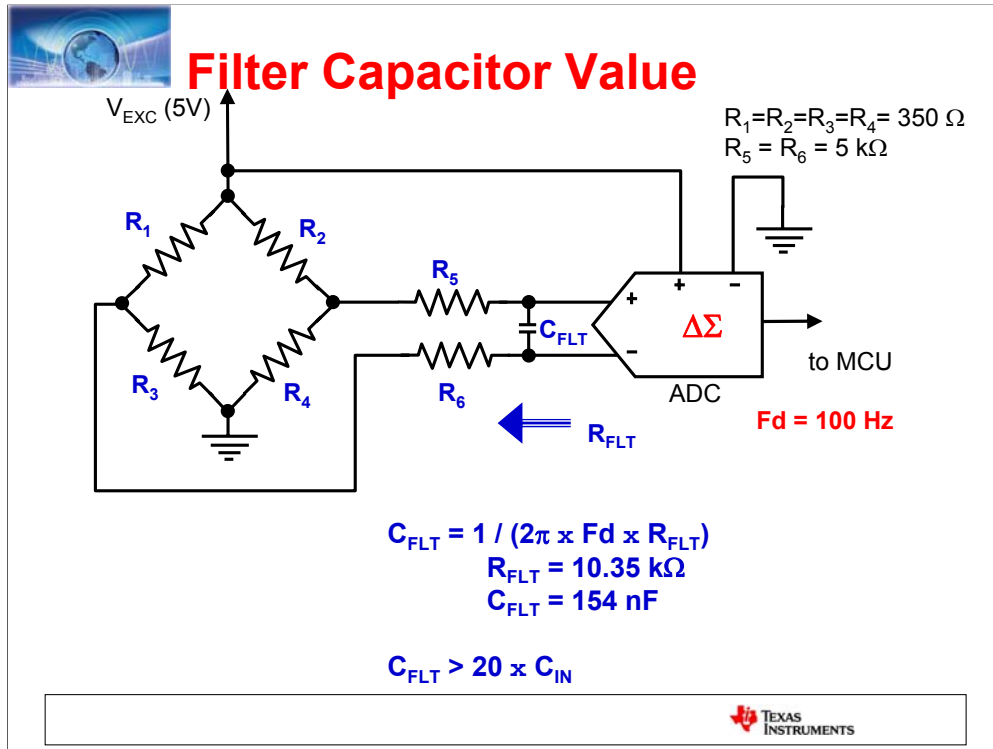
- Limits for R_{FLT}
  - Resistance rms-noise = $\sqrt{(4 \times K \times T \times R \times BW)}$
    - Where K = Boltzman's constant or 1.38×10^{-23}
      - T = Temperature in Kelvin
      - R = Effective Filter resistance
      - BW = Bandwidth
- Parallel resistance noise = $\sqrt{(4 \times K \times T \times (R_1||R_2) \times BW)}$

- R_{FLT} Noise = $\sqrt{(N_{R1||R3}{}^2 + N_{R5}{}^2 + N_{R2||R4}{}^2 + N_{R6}{}^2)}$

  - R_{FLT} noise < 1/3 rms noise

TEXAS INSTRUMENTS

Since our low pass filter can be simplified to a simple R|C pair, the noise contribution of the filter resistors is easy to calculate. As you calculate this value, be aware that the resistors you select will create noise. Basically, the noise contribution of the resistors should be equal to or less than one third of the noise from the converter.

Discrete R_{FLT} Max Values

The noise generated by the resistors over the bandwidth from dc to the your filter's corner frequency should be less than the noise generated by the delta-sigma converter. This diagram gives you the maximum values for your resistor versus the effective resolution of your converter. If your resistors are too high, consider increasing the external filter capacitor and then recalculating the resistor value or changing your corner frequency.

Filter Capacitor Value

V_{EXC} (5V)

$R_1 = R_2 = R_3 = R_4 = 350 \ \Omega$
$R_5 = R_6 = 5 \ k\Omega$

R_1 R_2

R_5

C_{FLT}

$\Delta\Sigma$

$+$ $+$ $-$

$-$

to MCU

R_3 R_4

R_6

ADC

R_{FLT}

Fd = 100 Hz

$$C_{FLT} = 1 / (2\pi \times Fd \times R_{FLT})$$
$$R_{FLT} = 10.35 \ k\Omega$$
$$C_{FLT} = 154 \ nF$$

$$C_{FLT} > 20 \times C_{IN}$$

TEXAS INSTRUMENTS

In this diagram, we show a typical delta-sigma converter bridge circuit. Notice that resistance of the bridge is equal to 350 Ω. Fd determines the filter corner frequency. C_{FLT} can be as large as needed, however, it must be larger than the input capacitance of the converter (C_{IN}).

24-bit ΔΣ Load Cell System

This is the final circuit for the 24-bit ΔΣ system. This system includes the sensor, a 1st order passive filter, and a 24-bit ΔΣ A-D converter (ADS1232).

Load Cell: 24-Bit System Errors

- ADS1232 (CF = 4.4)
- Gain = 1
- Range = ±2.5 V
- Noise = 3.7 μVp-p

- Cost: $3.90

TEXAS INSTRUMENTS

If we look at the errors for the 24-bit $\Delta\Sigma$ system, we are using ADS1232, which is a low-cost 24-bit converter. If we look at the input range of 5 V, this device produces noise at 3.7 μVp-p. This is well below the system resolution that we're trying to achieve in our circuit. The cost of the ADS1232 is $3.90. If we compare these specifications with our 12-bit system, remembering our measurement goal of 10 μV, we can see that the 24-bit system gets us to our goal quite well. The 3.7 μV of noise is the only thing that comes close to being a limitation.

Measurement Goal = 10uV (RTI)

System Errors (CF = 4.4)
- ADS1232
  - Gain = 1
  - Range = ±2.5 V
  - Noise = 3.7 μVp-p

- Cost (budgetary)
  - ADS1232 - $3.90

- Total - $3.90

System Errors (RTI, CF = 4.4)
- INA326
  - Gain = 250V/V
  - Noise (0.1 to 10Hz) = 1.07 μVp-p
- OPA340, OPA333
  - Noise (0.1 to 10Hz) < 20 nVrms
- ADS7822
  - Noise = 1.16 μVp-p

- Cost (budgetary)
  - INA326 - $2.40
  - OPA333 - $1.20
  - OPA340 - $0.80
  - ADS7822 - $1.55
- Total - $5.95

TEXAS INSTRUMENTS

The 12-bit converter system ends up costing us more than the 24-bit system. The INA/OPA combination is $4.40 and the 12-bit ADC is $1.55 which equals a total of $5.95. So for $3.90 with the 24-bit system, which also meets the specification, we have a lower cost.

Sensors and Measurements

Sensor	Sensor Resolution	Measurement Goal
Weigh Scale (Load Cell)	10 mV FS @ 5V excitation	1/1000FS = 10 μV
Thermocouples	10-60 μV/°C	0.1°C = 4 μV (type K)

The different types of thermocouples have outputs that range from 10 to 60 µV/°C and we want to measure a 0.1°C. This would mean that the measurement goal for the type K thermocouple (which is a 40 µV/°C), will be 4 µV (40 µV/°C * 0.1 °C) .

Seebeck Coefficients for Thermocouples

Thermocouples are constructed of two dissimilar metals such as Chromel and Constantan (Type E) or Nicrosil and Nisil (Type N). The two dissimilar metals are bonded together on one end of both wires with a weld bead. This bead is exposed to the test thermal environment. If there is a temperature difference between the bead and the other end of the thermocouple wires, a voltage will appear between the two wires at the end where the wires are not soldered together. This voltage is commonly called the thermocouple's Electromotive Force (EMF) voltage. This EMF voltage changes with temperature without any current or voltage excitation.
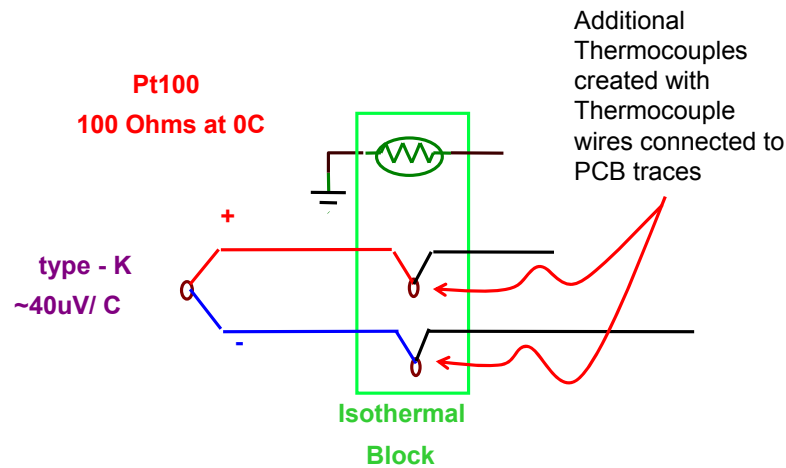
The K-type thermocouple exhibits very good linearity over most of its operating range and the accuracy can be specified to within a fraction of a degree.

There are a number of ways to correct the thermocouple's nonlinearity, but all rely on applying linearization coefficients to the measured voltage. The coefficients are often mathematically derived or acquired from look-up tables. Categorization and fast algorithms can be used to speed up the process. The choice depends on the capabilities of the processor or controller in the measurement system.
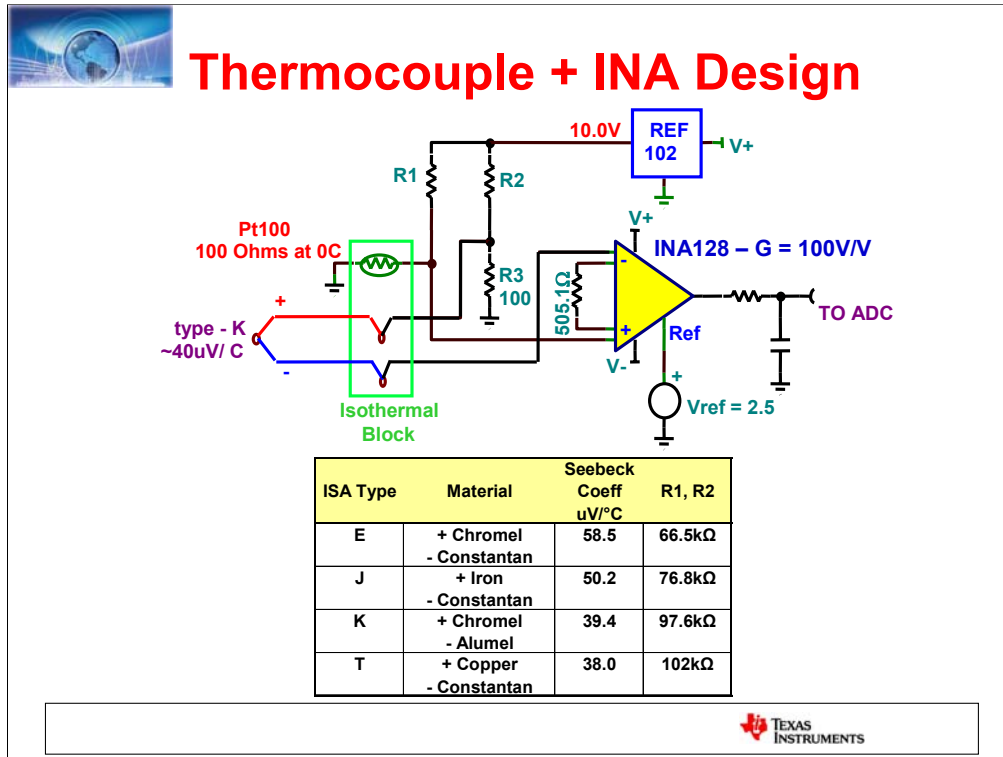
You can see the Seebeck Coefficient (or temperature coefficient) of the type K thermocouple is about 40µV/°C. You can also see that the type K thermocouple is flat over a fairly wide temperature range from zero to 1000°C.

Isothermal Block

Pt100
100 Ohms at 0C

Additional Thermocouples created with Thermocouple wires connected to PCB traces

type - K
~40uV/ C
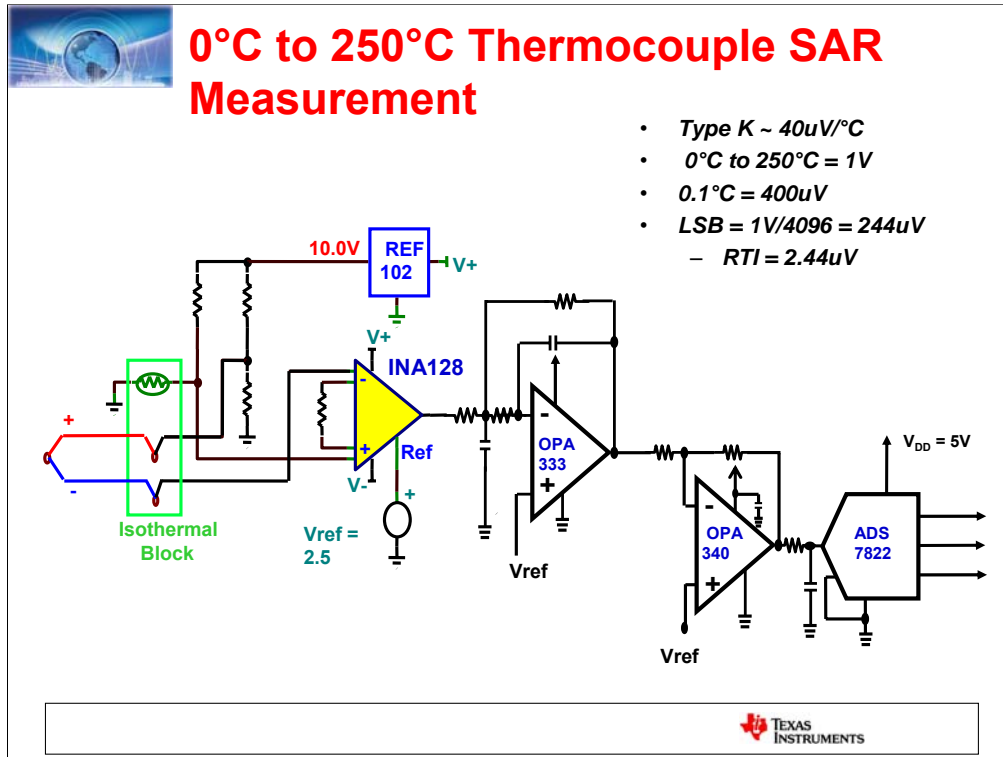
+

-

Isothermal
Block

TEXAS INSTRUMENTS

An absolute temperature reference is required in most thermocouple applications. This is used to remove the EMF error voltage that is created by thermocouples created with the connection of the thermocouple wires to the PCB traces. The two metals of these thermocouples come from the temperature sensing element and the copper traces of the PCB. The isothermal block in slide is constructed so that the Thermocouples that are created when the sensor wires are connected to the PCB traces are kept at the same temperature as the absolute temperature sensing device (RTD). These elements can be kept at the same temperature by keeping the circuitry in a compact area, analyzing the board for possible hot spots, and identifying thermal hot spots in the equipment enclosure. With this configuration, the known temperature of the copper junctions can be used to determine the actual temperature of the thermocouple bead.

Thermocouple + INA Design

ISA Type	Material	Seebeck Coeff uV/°C	R1, R2
E	+ Chromel - Constantan	58.5	66.5kΩ
J	+ Iron - Constantan	50.2	76.8kΩ
K	+ Chromel - Alumel	39.4	97.6kΩ
T	+ Copper - Constantan	38.0	102kΩ

There are as many varieties of thermocouples as there are metals, but some combinations work better than others. The list of thermocouples shown in Table 1 are typically used in industry. Their behaviors have been standardized by the National Institute of Standards and Technology (NIST). The particular document from this organization that is pertinent to thermocouples is the NIST Monograph175, "Temperature-Electromotive Force Reference Functions and Tables for the Letter-Designated Thermocouple Types Based on the ITS-90". Thermocouple manufacturers use these standards to qualify the thermocouples that they ship.

This thermocouple amplifier circuit uses the INA128 precision instrumentation amplifier in a gain of 100V/V. The circuit is connected with the type K-thermocouple and uses the PT100 (RTD) for the cold junction compensation.

The table lists the resistor values for R1 and R2 associated with various thermocouples. These resistors establish the RTD bias such that the associated voltage corresponds to the temperature of the isothermal block.

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0°C to 250°C Thermocouple SAR Measurement

- *Type K ~ 40uV/°C*
- *0°C to 250°C = 1V*
- *0.1°C = 400uV*
- *LSB = 1V/4096 = 244uV*
  - *RTI = 2.44uV*

This thermocouple amplifier circuit uses the INA128 precision instrumentation amplifier in a gain of 100V/V. The thermocouple circuit provides cold junction compensation with the PT100 RTD. The PT100 exhibits very good linearity over most of its operating range and the accuracy can be specified with a fraction of a degree C. Therefore, from one RTD batch to the next, the temperature accuracy performance can be duplicated.

The 2nd order, low-pass filter (OPA33 circuit) is again designed for a cut-off frequency of 10 Hz. This filter is followed by an amplifier and RC circuit. This combination is used to drive the 12-bit A/D converter (ADS7822).

We are going to limit our particular test to 250°C. With the 40 µV/°C times a gain of 100 the full scale voltage range over that 250°C range is equal to 1V. This also provides the measurement of 0.1 °C equal to 400 µV at the output of the INA into the A/D. If you calculate the value of this voltage at the thermocouple input, the LSB size is 2.44 µV.
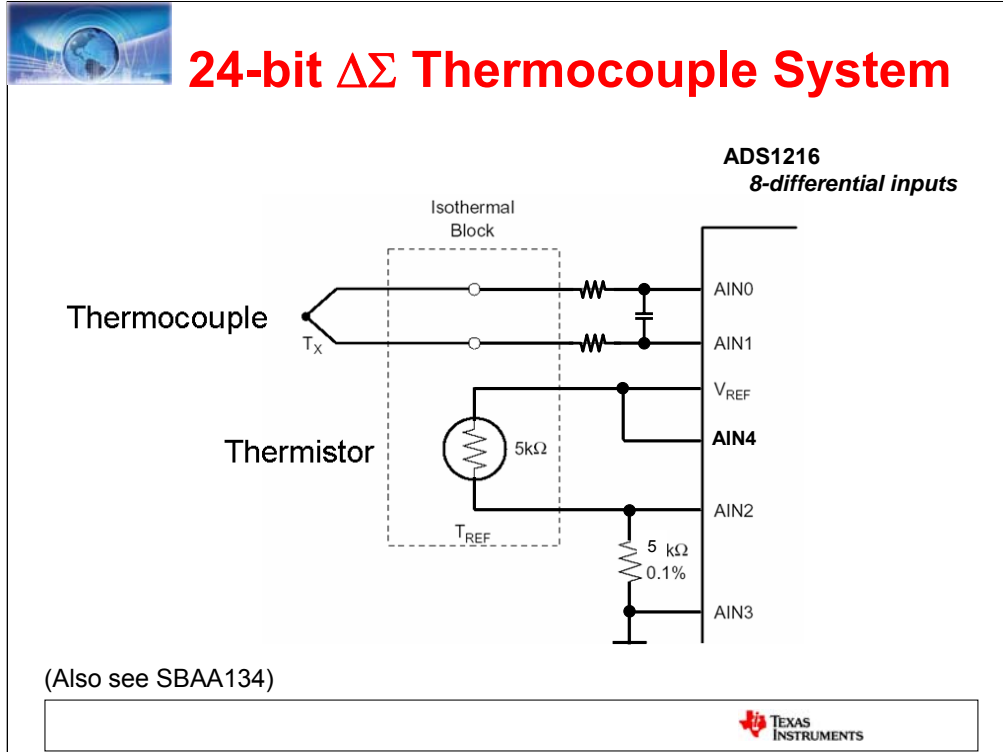
INA128 + ADS7822 Measurement System

System Errors (RTI, CF = 4.4)
- INA128
    - Gain = 100 V/V
    - Noise (0.1 to 10Hz) = 0.27 μVp-p
- OPA340, OPA333
    - Noise (0.1 to 10Hz) < 20 nVrms
- ADS7822
    - Noise = 1.16 μVp-p

- Cost (budgetary)
    - INA128 - $3.05
    - OPA333 - $1.20
    - OPA340 - $0.80
    - ADS7822 - $1.55
- Total - $6.60

TEXAS INSTRUMENTS

The errors of this 12-bit system shows a the worst case noise figure of 0.27 µVp-p using a crest factor of 4.4. You will notice that these specifications are quite a bit better than the earlier ones with the bridge circuit and the INA128, but this improvement does come at a price.

24-bit $\Delta\Sigma$ Thermocouple System

ADS1216
8-differential inputs

Isothermal Block

Thermocouple
T_X

AIN0
AIN1
V_{REF}
AIN4
AIN2

Thermistor
5kΩ
T_{REF}

5 kΩ
0.1%

AIN3

(Also see SBAA134)

For the 24-bit system we are going to use the ADS1216 delta-sigma converter.

In this circuit, you can see where the ADC reference is driving the voltage to a thermistor in stead of an RTD. You measure the voltage across that thermistor with AIN4 and AIN2. and measure the current through with AIN2 and AIN3. With the voltage and current you know the resistance of the thermistor. From the resistance value of the thermistor you can determine the temperature of the isothermal block from calculations or a look-up table in the MCU.

This circuit does not use a linearization circuit for the thermistor, it simply uses a general-purpose equation to convert the resistance into a temperature. That temperature is then used to calculate the voltage for the thermocouple in the Isothermal Block, which are at that same temperature. This procedure calculates the voltage from 0°C to T_{REF}. The voltage is then added to the voltage measured from the thermocouple. The total voltage is then used to calculate the temperature at the end of the thermocouple.

See TI applications report SBAA134 for an extensive treatment of thermocouple temperature measurements with ΔΣ ADCs.

Thermocouple: 24-Bit System Errors

- System Errors (RTI, CF = 4.4)

- ADS1216
  - 2.5V Full Scale
  - Noise = 4.4 μV

- Cost (budgetary)
  - $6.25

TEXAS INSTRUMENTS

With the thermocouple 24-bit $\Delta\Sigma$ system, we have a noise error of 88 μVp-p.

Thermocouple: Measurement Goal = 4uV

- System Errors (RTI, CF = 4.4)
- ADS1216
  - 2.5V Full Scale
  - Noise = 4.4 μV

- Cost (budgetary)
  - $6.25

- Total - $6.25

System Errors (RTI, CF = 4.4)
- INA128
  - Gain = 100 V/V
  - Noise (0.1 to 10Hz) = 0.27 μVp-p
- OPA340, OPA333
  - Noise (0.1 to 10Hz) < 20 nVrms
- ADS7822
  - Noise = 1.16 μVp-p

- Cost (budgetary)
  - INA128 - $3.05
  - OPA333 - $1.20
  - OPA340 - $0.80
  - ADS7822 - $1.55
- Total - $6.60

TEXAS INSTRUMENTS

If you compare these $\Delta\Sigma$ numbers against our 12-bit system with the measuring goal of 4 µV, you see that this 24-bit system nearly achieves the 4 µV for the lower cost of $6.25.

"But, I only need 12 bits!"

- 12-bit ADC circuits usually require external gain
- External amplification increases errors from offset gain, noise, and drift
- For 12-bit measurement and 5V range LSB = 1.22mV
- With a gain of 250 the LSB = 4.88 uV

- For 24-bit system and 5V range LSB = 298 nV
- With PGA=64 LSB = 4.65 nV
  - x1000 compared to 12-bit system with gain = 250.

- Inherent gain of 2^{12} (4096) with no offset or noise penalty. PGA can provide additional gain.

TEXAS INSTRUMENTS

In review, we may hear "I don't need 24-bits." A 12-bit system is not simple to build. You've got to do everything right with the layout and everything else. But the system usually requires a little external gain, which actually may compound the problem. External amplification increases the offset, gain, noise and drift errors. If we look at a 12-bit system with a 5 V range we have a 1.22 mV LSB with a gain of 250 that LSB is down to 4.88 µV. For a 24-bit system with a 5V input range the LSB is 298 nV. If you have an on-chip PGA, the LSB size gets down to 4.6 nV. This is 1000 times better compared to a 12-bit system with a gain of 250. So the gain of the 24-bit system is another 2^{12} or 4096 higher, with no offset and noise penalty. Plus with the PGA there is even more gain if needed.

Possible Advantages with 24-bits

- Improved offset, gain, noise and reduced drift
- Increased accuracy
- Fewer Precision Components Required
- Reduced Parts Count – Improved Reliability
- Smaller Size
- Lower Cost

TEXAS INSTRUMENTS

Why use a 24-bit system if all you want is a 12-bit system? It depends on the situation but you can get some improved offset, gain, better specs with increased accuracy, fewer components to take up less boards space, smaller size, and possibly lower costs.

Why Use a 24-Bit Converter When You Only Need 12-Bits?

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