



PoE Plus – IEEE 802.3at The New Standard for Ethernet Power

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Abstract

- **The current generation of Power over Ethernet (PoE) was released in 2005 as IEEE-802.3af, and subsequently as IEEE-802.3-2005 clause 33.**
 - This standard provides for up to 12.95W of usable plug-and-play power at any twisted-pair cabled Ethernet enabled device (PD).
 - Since its inception, it is estimated that there are over 57 million PoE enabled switch ports, with continued growth.
 - Virtually all major manufacturers of enterprise IP Phones, surveillance cameras, and access points provide PoE enabled products.
- **Soon after the market embraced the technology, a movement for more delivered power arose and the IEEE-802.3at (PoE Plus) project was initiated. This standard will provide up to 25.5W at the powered device (PD) and provide a framework for dynamic power allocation as well.**
- **This topic will present key aspects of the yet-to-be-released standard, how it relates to the existing standard, and TI's PoE solutions.**



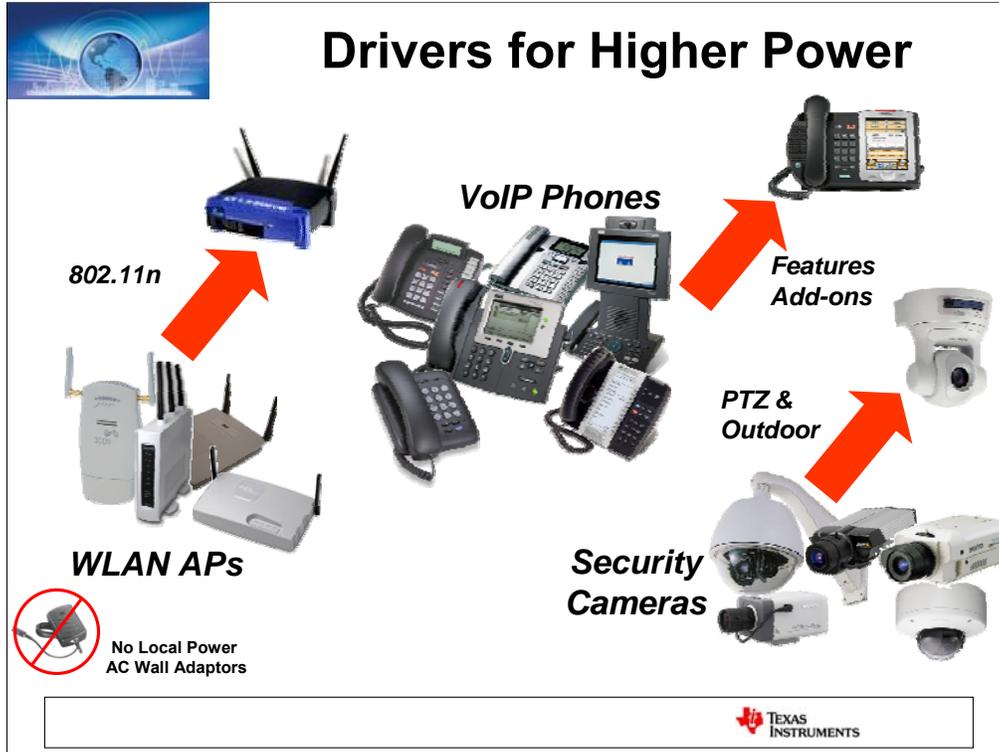
Agenda

- **Intro**
 - PoE Plus Drivers, Principles
- **PoE Warm-up / Review**
 - Description, Power Loop, Power Topologies, Basic Specs, PoE Process
- **PoE Plus**
 - Type 1 & Type 2, Hardware Class, PD Startup
 - DLL, Current/Power, Current Imbalance, Transients
- **PD and PSE Roadmaps**
- **Questions**



Introduction

- **Power over Ethernet defined in IEEE 802.3-2008 (clause 33)**
- **Standard was released in 2003**
 - Initial IEEE discussions in 1999
- **Initial PoE Plus (802.3at) discussion was 2004**
- **Estimates are >57M PSE ports shipped (to mid 2008)**
- **TI has shipped >20M PD ports**
- **All major router/switch vendors, IP Phone, Access Point, and Camera vendors support for enterprise products**
- **Initially, PD designers of some devices struggled to stay within 13W**
 - Eventually market designed to power limitations
 - Base phone and access point ~ (6W – 7W)
- **Increasing power is believed to enable a new class of devices and improve the market size**



PoE Motivations

Location - Wireless access point and security cameras are located far from power outlets

Security - One wire for data and power is perceived to be more reliable

Cultural - Some applications (e.g. telephones) are expected to be one wire devices

Reliability - One UPS can backup the network infrastructure and the end devices

Uniformity - One PoE standard worldwide with no need for 110-220 VAC, 50-60Hz and dozens of plugs

Maintainability - IT department can monitor and manage from central location



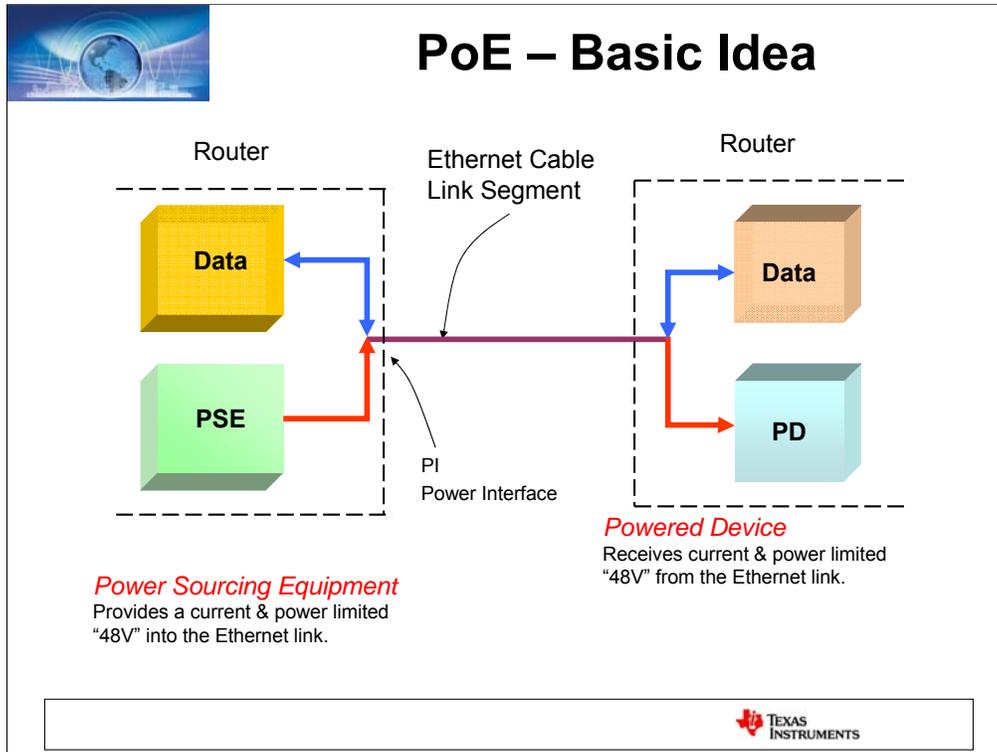
PoE Plus Guiding Principles

- **New standard interoperates with the existing standard to extent possible**
- **Implemented by IEEE as an update to existing clause 33 – evolution**
- **Power levels increased to a level felt “practical” considering efficiency, broad market appeal, benefit to the stakeholders**
 - IEEE standards balance cost increase vs. market gain
 - There are some applications that want upwards of 60W
 - These are a very, very small percentage of the total market
- **Maintain plug-and-play nature of Ethernet.**
 - No measuring or qualification
 - Graceful method of handling power mismatch
- **Nearly-finished IEEE 802.3at standard can be seen as a scaling of existing technology**
- **This level of current increase required buy-in and extensive work from international cabling bodies**
 - Data cable never used as a high-current power distribution network
 - The shift from 13W larger than it seems due to I²R effect
 - Cable is rated at 60°C – often operated to > 50°C
 - Cabling bodies perceive risk in premature ageing in installations where there is high temperature and/or large cable bundles



While “get as much power as possible” sounded like a good idea, it turns out it is not.

- 1) Delivery of power over 100m of AWG24 gets very inefficient
- 2) It was agreed that market went down steeply as power went up
- 3) The goal is to create a single solution to a single problem and cost is proportional to power delivered
- 4) In order to be practical, an optimal point that powers the most applications at the lowest cost is necessary
- 5) What sounds OK for one port begins to look untenable when you consider 8 (or more), 48 port routers per rack.
- 6) The market will drive vendors to the highest solution but won't pay proportionately – forcing suppliers to provide a large unused capacity at low margin

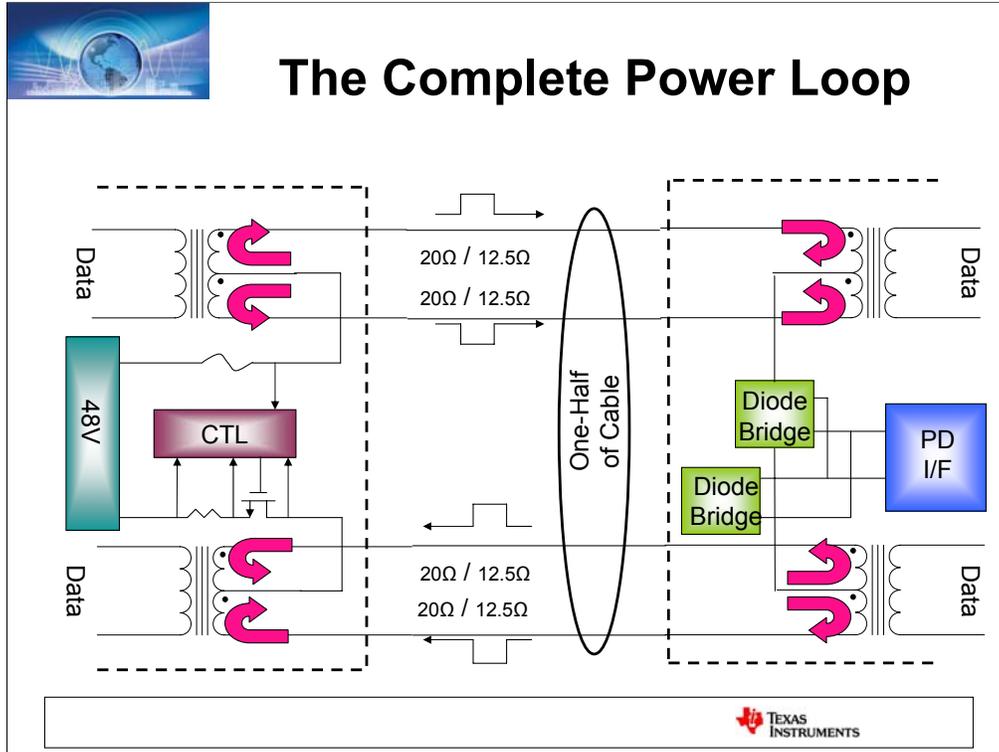


Power and data are combined in a router. There is also a midspan configuration that injects power into the cable between the endpoint data termination.

Power is a floating "48V" that is 1500V isolated from ALL other potentials.

Cable for existing 13W (delivered power) systems is CAT3 – CAT6. Cable for 802.3at (25.5W) systems is CAT5 or higher.

IEEE specifies the interface at the PI of each end. EIA/TIA and IEC control cable specs.



The PSE has the “smarts” and drives the loop with voltage.

The PD is intentionally a simple device. As a load the PD controls the loop current. This is true during startup protocols as well as powered operation.

The DC current loop is overlaid on the existing data loop by using “phantom power.”

The dc current flows into the xfmr center-taps and equal amounts flow into and out of “dots.”

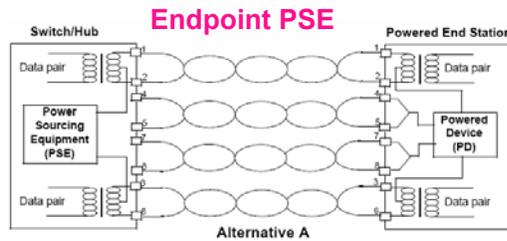
This results in flux cancellation, eliminating increased flux withstand of the xfmr core.

Resistance imbalance within the pair cause a dc current imbalance and thus a dc flux offset in the xfmr core.



Endpoint and Midspan PSEs

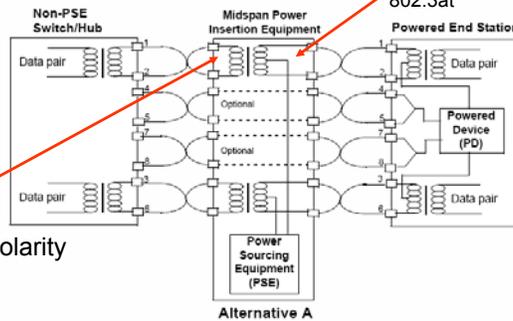
High power systems use the same topologies as currently used.



Shown midspan topology newly recognized. Previously commonly used in practice.

Midspan PSE

Newly recognized configuration in 802.3at



Midspan blocks path back to router
Use only two of four pairs
Power over either pair set of either polarity

802.3at recognizes 1000BaseT



These are two example configurations of end-point PSE and midspan PSE.

Midspan provides a mechanism for upgrade of a power-less installation to a PoE installation without discarding the existing equipment.

Midspan PSE can be an independent box, or combined in a cross-connect panel.

Endpoint and midspan PSEs may power on either pair set, and polarity.

PD must accommodate all combinations.

Midspan PSE must block voltage from appearing on the router to avoid damage.

Block could just as well be capacitive as transformer – a center-tapped inductor would still be used for insertion



High-Level Specifications

	IEEE 802.3-2008, clause 33	IEEE 802.3at
Delivery method:	2 Pair	2 Pair
Cabling	Class C (40Ω loop)	Class D (25Ω loop)
Min. PSE Power sourced	15.4W	30W
Max. PD Power drawn	12.95W	25.5W
Min. PSE voltage	44V	50V
Min. PD voltage	37V	42.5V static V_{PSE}
Max PD current	350mA	600mA
PSE output protection	I_{LIM} (400 – 450mA)	Template
Minimum delivery eff.	84% (12.95/15.4)	85% (25.5/30)



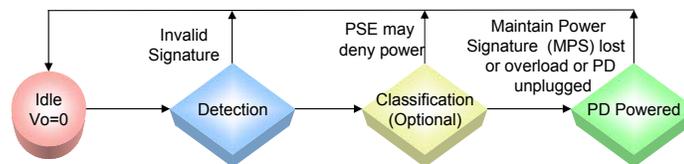
Link segment resistances are specified as the round-trip resistance of a single pair including intra-link connections (up to 5), horizontal cable, and patch cords.

The power loop consists of two pairs in series, with each conductor in the pair paralleled resulting in a power loop of $\frac{1}{2}$ the pair loop resistance.



PoE – The Process

- **Simple hardware-based protocol**
- **Idle – Unpowered state for PD unplugged or not requesting power**
- **Detection – Low voltage probing for PD-specific signature**
- **Class (hardware) – Determine load power before power up**
- **Class (DLL) – Negotiate power between PSE & PD after power up and data link is established**
 - New for 802.3at
- **Powered (MPS) – Line must appear loaded to maintain power application**
- **Return to Idle when unplugged or not requesting power**



The basic process hasn't changed with the new standard.

Detection assures that a PD that can accept power is connected, so powering up the link does not damage non-PoE equipment

Hardware Class was optional for a type 1 PSE. It would be irrelevant for a single-port PSE that could supply full power.

IEEE 802.3at adds DLL (data link layer class) that is mandatory for type 2 end-point PSEs and optional for type 1 end-point PSEs

Since Hardware Class 0 required 0mA, a PD without active class circuitry still provided a class. Type 2 PDs are required to provide class4 – was previously not allowed.

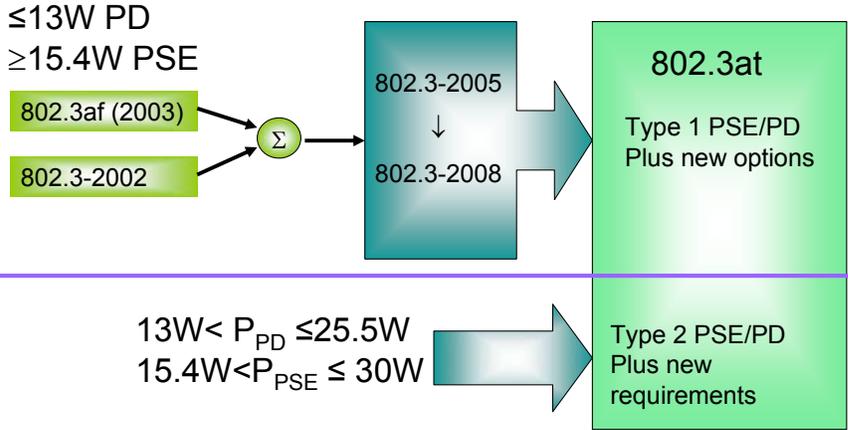
MPS stands for Maintain Power Signature. Its presence tells the PSE that a PD is still present.

MPS consists of a a minimum current, or an ac impedance below a particular level
DC MPS limits are <5mA @ PSE powers down, PD must draw >10mA. PD can also draw pulsed current.

For AC MPS, the PSE adds a "ripple" on the provided DC and measures the ripple current to get an ac impedance.



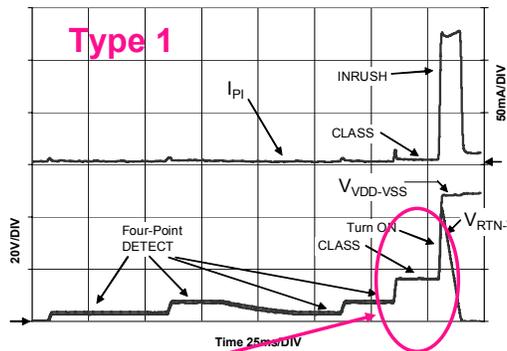
Relationship of Standards



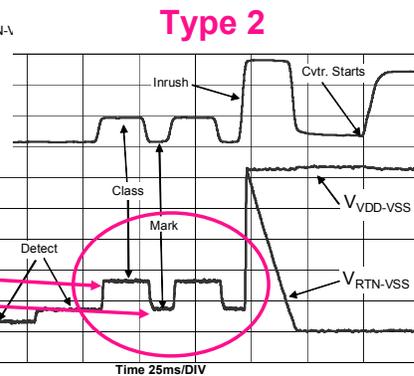
- **802.3-2008 devices become 802.3at compliant type 1 devices.**



Classification - Hardware



- T2 PSE sees class 4 ⇒ T2 high power PD
- T1 PSE sees class 4 ⇒ class 0 PD
- PSE sees class 0 – 3 ⇒ T1 low-power PD
- PD probed 1-event ⇒ T1 or T2 endspan PSE
- PD probed 2-event ⇒ T2 midspan PSE



- 1-event
- 2-event class
- 2-event mark



- 1) Type 1 PSE need not perform class
- 2) Type 2 PSE must do at least 1-event hardware class (plus DLL)
- 3) Type 2 PSE that cannot do DLL (midspan) must do 2-event class
- 4) 2 event system is meant to avoid false sequence detect when PD plugged in during detect
- 5) PD mark resistance does not conform to 25K detection signature to keep PSE from being fooled



Classification DLL (New)

- Purpose of DLL (data link layer) is to allow dynamic allocation of PSE power and better 48V source utilization.
- Hardware class commits PSE to providing full requested power
- DLL communication takes place as Ethernet messages using 802.1AB LLDP (Link Layer Discovery Protocol)
 - This is point-point communication that is transparent to higher layers such as TCP & IP
 - Message does not travel beyond the router
- In a request/echo protocol, the PSE has the ultimate control of supplied power
- Protocol resolves wattage to 0.1W referred to the PD PI
- *The applications processor in the PD owns this function and it is not handled by the PD PI interface hardware*
- DLL provides further features like minimum required power and a graceful method of PSE load shedding during power outages



Type 1 & Type 2

- **PD must request maximum power on hardware class.**
 - More than likely, PSE manufacturers will permit PDs that use DLL to break this rule
 - PSE is permitted to turn off PDs that violate their power class.
- **Mutual identification**
 - PD needs to know if PSE is type 2 so it can draw more power
 - PSE needs to know PD load so it can make sure power is available
 - At a system level *avoid* having power *mismatch look like faulty hardware*
- **Data Link Layer (DLL) negotiation permits dynamic power allocation**
 - Worst-case power allowance to cable loss is brought forward into IEEE 802.3at because it assures plug-and-play with no knowledge of the link resistance
 - Concept of “lost power”
- **New standard permits type 1 devices to do DLL**
 - Many manufacturers can update designs to use this



Mutual identification permits a PSE to know if it is dealing with a high-power PD.

It also lets a PD know what kind of PSE it is connected to and how much power it can draw. This avoids the situation where a high-power PD starts from a type 1 PSE and immediately crashes it – looking like a failure.

Adding DLL for power management (works with routers) meant that the router hardware could be simplified (no 2-event class h/w).

This did place a burden high-power PDs. Since relatively few PDs will be type 2, this avoided burdening the bulk of the market with the extra cost and shifted it to where it was needed.

The cost is associated with having to control the load power until DLL comes up. This also provides a method for some type of graceful operation between type 2 PDs and type 1 PSEs.

Lost power is that part of a PSE input supplies power that is allocated to active PDs that either will not or cannot be used but is blocked from allocation to other PDs.



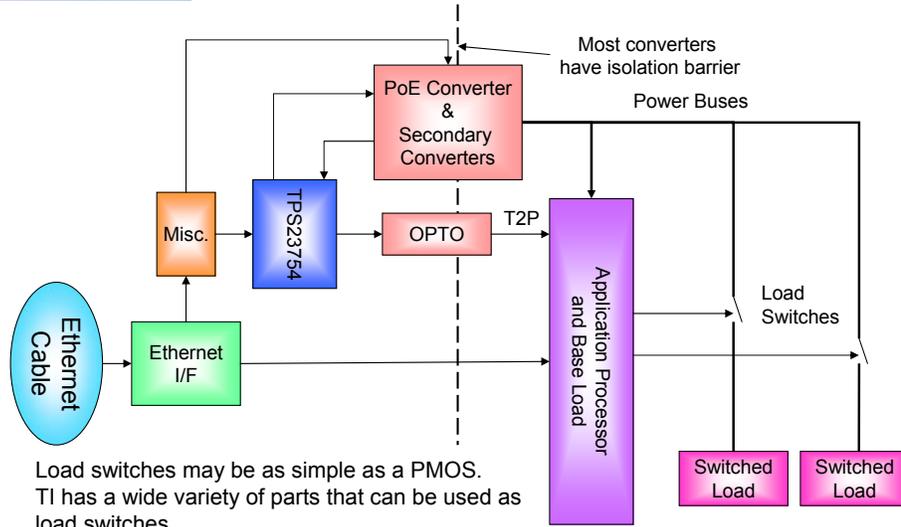
Startup Behavior

- **Type 2 PSE must provide type 1 startup current & time profiles**
 - May have foldback which is formally recognized in IEEE 802.3at
 - Assures type 1 startup compatibility with type 2 PSE
- **Type 1 PD just starts up constrained to its declared hardware class and may go to full power immediately**
- **Type 2 PD must startup like a type 1 PD**
 - Either self-limit current to $< 400\text{mA}$ or rely on PSE limit of 400mA to 450mA
- **Type 2 PD that does not see type 2 h/w class must draw $\leq 13\text{W}$ until DLL communication permission**
- **Type 2 PD that sees type 2 h/w class can draw up to 25.5W after startup period ($>80\text{ms}$)**

- *The standard implies a hardware signal from the PD PI interface to the applications processor*
- *The standard implies that a PD applications processor must be able to turn power up and down on blocks of circuit*



Type 2 PD Power Topology



Load switches may be as simple as a PMOS. TI has a wide variety of parts that can be used as load switches.

[Power Switches](#), [Load Switches](#), [MOSFETs](#)



Current/Power Levels

- 25.5W rating based on current derating provided by EIA/TIS (TSB-184) and ISO/IEC JTC 1/SC 25/WG 3
- Rating is based on every pair in a 100-pair bundle carrying 600mA results in a derating of 10°C
 - Hotspot in the middle of the cable
 - Maximum ambient temperature is at any position along the cable
 - Most data cable rated to 60°C
 - Derating is consistent with standards requiring 50°C ambient operation of equipment
 - Cabling bodies chose a conservative approach so as to “do no harm” to installations and avoid engineering analysis at each installation.

Table 1 - Current capacity for a category 5 100-cable bundle

Temperature rise °C	Current carrying capacity mA
5	420
7.5	550
10	600
12.5	680
15	720

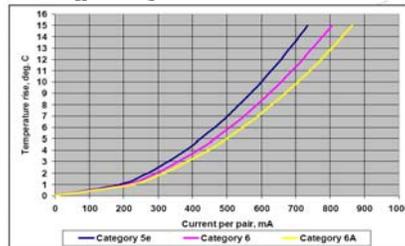


Figure 5 - Temperature rise in bundle of 100 4-pair cables of various categories.



The cabling groups are responsible for putting out standards that result in good operation and long life regardless of the installation specifics.

Adding a lot of power dissipation results in new regions of operation for this transport medium.

Cable was specified and used to 60C before, although transmission performance gets worse at high temperature.

This degradation was handled by the IEC as a recommended shorter loop for high-temperature operation.

To meet the operational performance, temperature derating was required to get the cable within its specified operating range.

The standards bodies tested a number of cable samples under relative worst-case conditions to establish limits.

Other issues lurk relating to plasticizer migration from the outer jacket to the inner conductor insulation impairing transmission parameters.



Current/Power Levels

- **IEEE decided to use 600mA with 10°C derating even though the current plan is to specify 2 pairs.**
 - This reduces end-customer concerns about using other values, and covers countries where 2 Ethernet links per cable are supported
- **Most real installations will experience only a few degree rise**
 - Real world is statistical ...
- **IEEE raised the minimum PSE voltage to 50V**
 - Router vendors wanted this tolerance
 - Gets some extra watts at no cost
- **Type 2 operation is limited to Class D (CAT5, 25Ω)**
 - Lower resistance reduces the “lost power” to the cable
 - Cables didn’t change, the restriction gets this virtually free
 - Some vendors have been known to use the difference between 25Ω and 40Ω cables to get their type 1 PDs some extra power.



In the real world, not all conductors will be energized. The PoE take in a large cable will not be 100%, and not all PDs will draw full power 24/7.

Bundles will not typically be 100 cables.

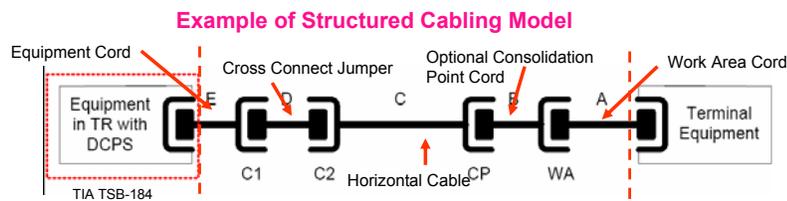
On the other hand, there may be areas where the cable runs through a floor-floor conduit or other warm location.

So the system has lots and lots of margin in real installations.



Current Unbalance

- **Current imbalance between conductors of a pair causes a shift in data xfmr properties**
 - Unbalanced resistances in the wires and connections are the cause
 - If allowed to go too far data integrity may be effected (unsatisfactory BER) – esp. older solutions
 - Parameter shift is magnetizing inductance reduction
 - This is worse for the magnetics at high temperature
 - Part of the problem is the dynamic base-line wander correction
- **Data patterns also contribute up to 7mA of imbalance**
- **Channel models owned by EIA/TIA and IEC**



Channel model includes conductors and connections between the end-devices. The end-device connection resistance is not in the channel model.

Horizontal cable is the solid-conductor wire in ceilings, walls, and cable trays. Cords or Jumpers are made from stranded wire that have higher resistance per unit length. Proportions are 90m total horizontal to 10m total cord/jumper.

The key to the unbalance problem is that resistance differences can add up to result in current offsets. Shorter cables have worse issues due to a relatively large difference in small numbers.



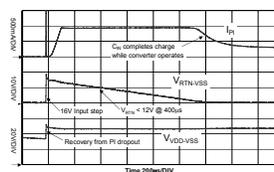
Current Unbalance

- **Type 2 I_{unb} value is 20.4mA (3% of I_{peak})**
 - I_{unb} is the unbalance current, or difference between the current in the two conductors of a pair.
 - Value considers some statistics to get real-world values
 - Else existing PoE wouldn't work (and it does)
 - Else the data coupling transformers get uncomfortably large
- **A number of manufacturers have this figured out**
 - Pulse, Bel Stewart, Coilcraft
- **PD has to follow PSE requirement**
 - PD neglected to specify I_{unb}
- **Midspans have special requirements/considerations**



Power Feed Transients

- New for IEEE 802.3at are specs describing dynamic PI performance (e.g. PSE voltage droops and recovery) and permissible PD current draw during transient
 - Previously undocumented
- Type 2 PSE permitted 7.6% drop for 250 μ s (redundant supply switch)
- PSE permitted turn off if PD exceeds permitted current value (no time limit)
- PSE has to provide power for a period (Tlim) *if it causes* the overload by changing its output voltage
 - Example 50V \rightarrow 56V or 44V \rightarrow 57V
- PD behavior during PI transients defined
 - PSE & loop considerations cover type 1 PDs – current is not necessarily bounded by 450mA
 - New criteria are set for PDs to assure they “recharge” within the PSE support window
- Almost all PD ICs shipped will be glitched by these PSE transients (e.g. 44V \rightarrow 57V)
 - TI new family of PD ICs designed to accommodate step voltage transients



In Poe, an overload is a current level between the max average and the maximum peak value.

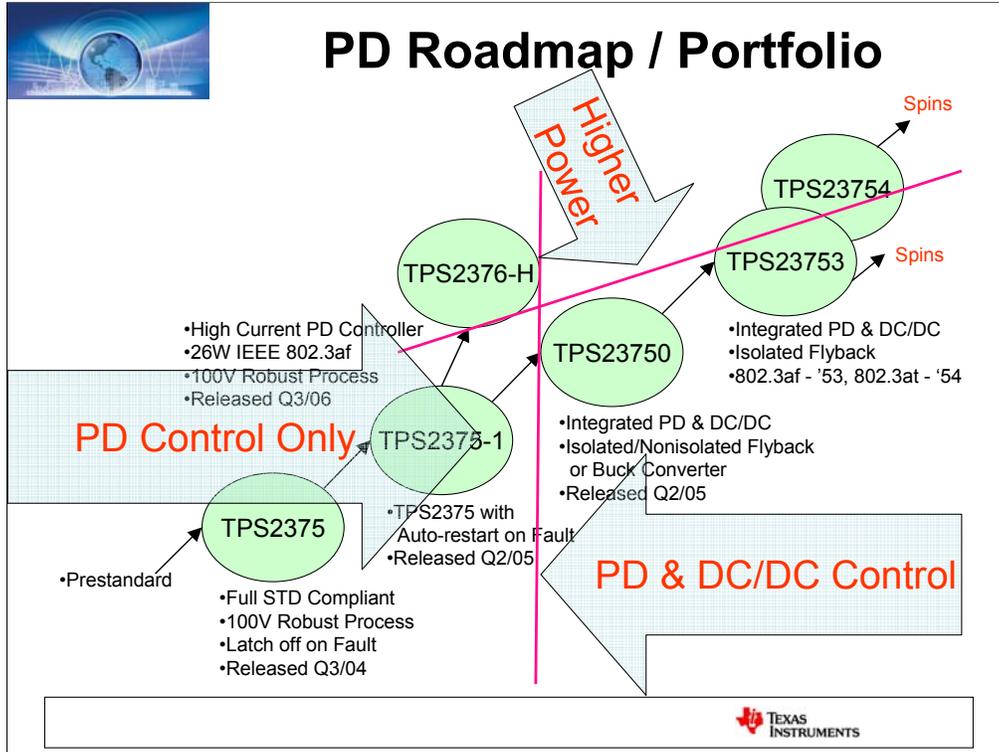
A short is a condition drawing current above the permitted peak.

Type 1 PSEs were specified to provide short current for 50ms, and most vendors went into foldback as the output voltage fell below 30V.

Since PDs are not permitted to draw short circuit currents, the new standard lets the PSE cut them off.

There is one exception to this rule, when the PSE output voltage steps up. Type 2 PSEs will provide current for 10ms, type 1 for 50ms.

Most manufacturers will provide some period of current limit and foldback for type 2 devices to provide robust service.



The PD portfolio is growing. Pulls are customer request and the new standard. Probable future additions are “green feature”



Additional PD Offerings

- **TPS23756**
 - 802.3at Type 2 Compliant
 - 12V Converter startup version of TPS23754
- **TPS23754-1**
 - 802.3at Type 2 Compliant
 - Eliminated PPD for pin-pin spacing
- **TPS23757**
 - 802.3at Type 1 Compliant
 - 13W Solution with '754 controller to provide native support for high-efficiency solutions



TPS23754

IEEE 802.3at PoE Interface & PWM Controller

Features

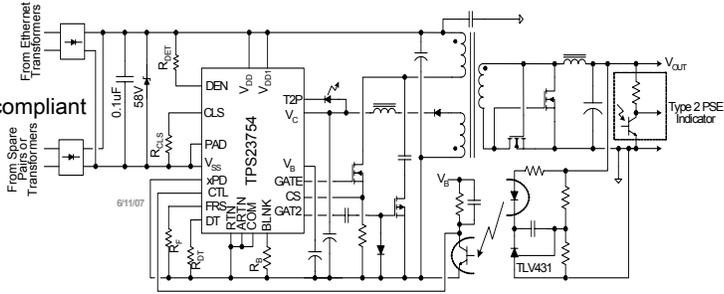
- Integrated control for PD power
- Optimized for 25.5W** isolated converter topologies
- Adapter **ORing support**
- Current and inrush limit, output overload and thermal protection
- Support for high efficiency designs

Benefits

- Compact, unified solution provides **predictable, compliant (draft), and reliable** operation
- Application specific** solution yields cost effective designs
- Defined powering preference
- Maximum device protection
- Higher operating efficiency and improved reliability

Applications

- IEEE 802.3at draft compliant
- VoIP telephones
- Access points
- Security cameras





The TPS23754 shares many characteristics with the TPS23753. Basics of ORing, slope, and synch are the same.

The TPS23754 has a second gate driver to support active clamp and synchronous rectifier applications.

This topology eliminates discretes, and makes the operation simply adjustable and repeatable.

The 2-event class is supported. The T2P (type 2 pse) output indicates that either an adapter is plugged in, or the 2-event class has occurred.

Application notes exist for PoE EMI, and TPS23753 (includes a lot of 754 apps) ORing available from the web page.

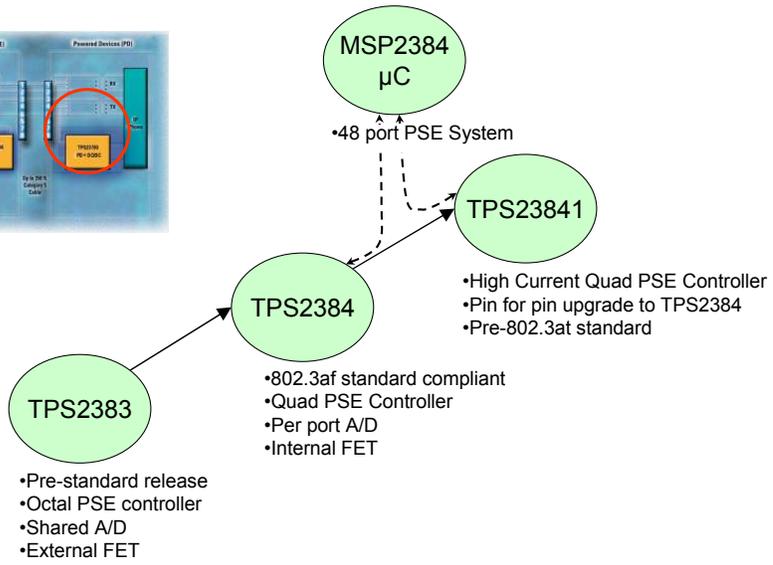
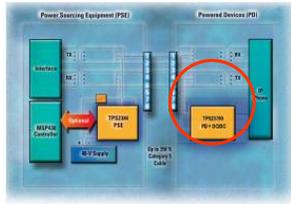
There will be several EVMs.

The TPS23754 was designed to permit input currents higher than the standard – and will run reliably at inputs right up to the current limit.

Higher power may be obtained with the “booster” circuit previously applied to the TPS2375/76-H family.



PSE Portfolio





Questions

Thank you for your time