Understanding
Power Supply Efficiency

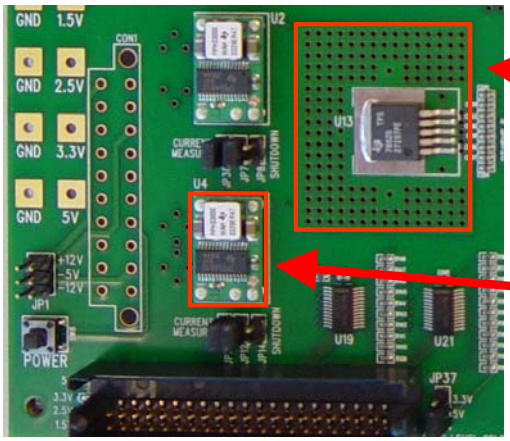
AGENDA

- **Why Use a Switching Power Supply**
- **Efficiency Examples**
- **Design Tradeoffs**
- **Ideal LDO Efficiency**
- **Ideal Switcher Efficiency**
- **Proper Power Dissipation Calculation**
- **Switcher Power Loss Contributions**
- **Typical Application Power Loss**
- **Efficiency vs Output Voltage**
- **Synchronous vs non-synchronous Switcher**
- **Efficiency Measurement**

Why Switchers?

- Best Efficiency – Less Heat Dissipation
- Reduce system level costs
  - May eliminate cooling costs
    - heat sink, fans, and their assembly
  - Can use a smaller battery for the same run time
    - For same battery – longer run time
- Longer Run Times
  - Pulls less current from the battery
- Smaller overall solution size
- Better suited for high input voltage to output voltage ratios

More Power Dissipation = Larger Area



1A LDO +
ground plane
as heat sink
(2.5W output power)

6A PTH3000
(6W output power)

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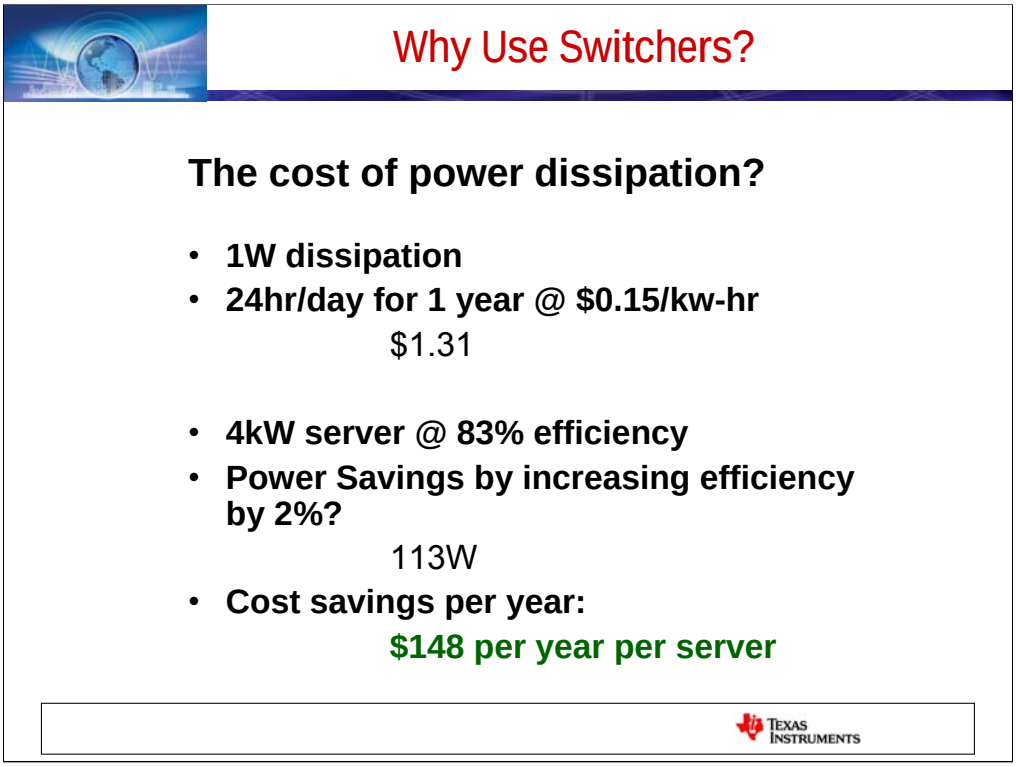
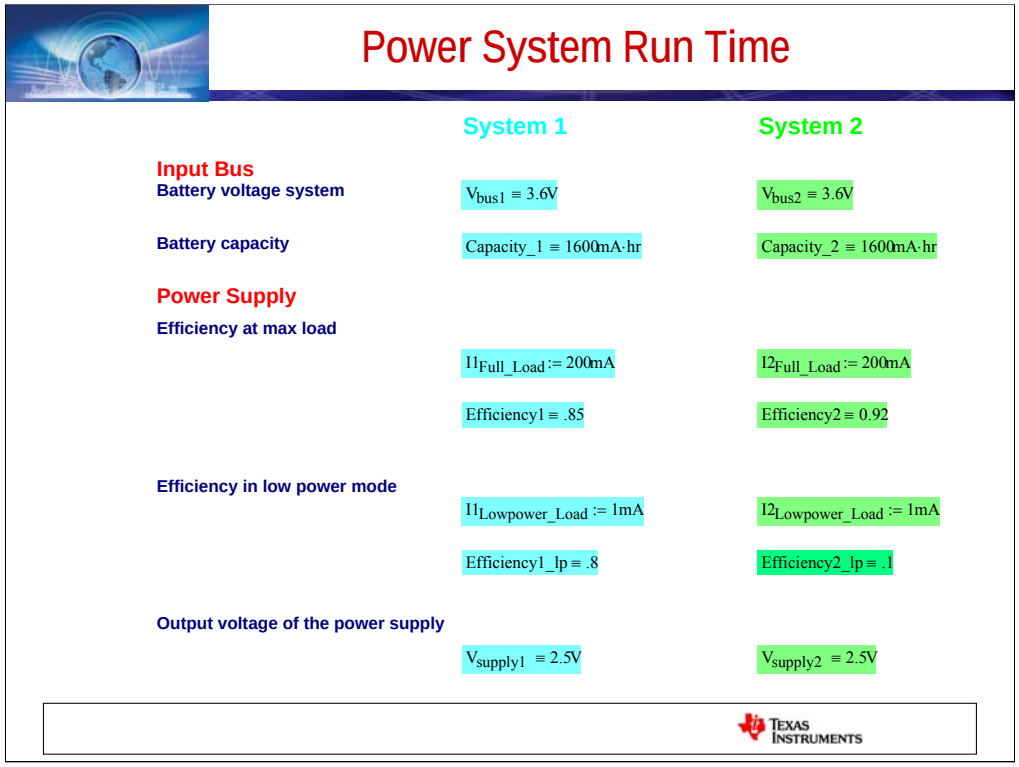
LDO is 2.5W output. PTH is probably close to 6W output.



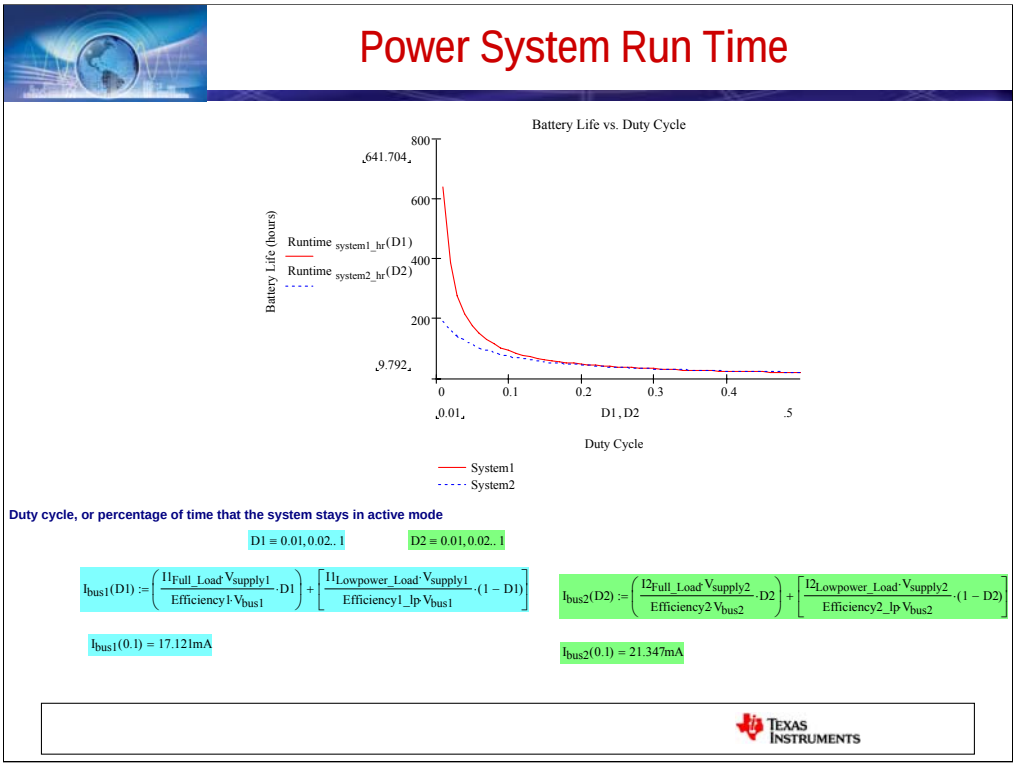
Paying attention to efficiency and power dissipation affects overall cost of operation.

Total 2% is not extreme – example: an efficiency gain at the POL converter will be seen at the AC input compounded by the upstream bus converter 92% + main DC/DC 92% + PFC 92% efficiencies… 1.5% needed

Paying an extra couple of dollars for a higher efficiency switcher doesn't sound too bad anymore does it?



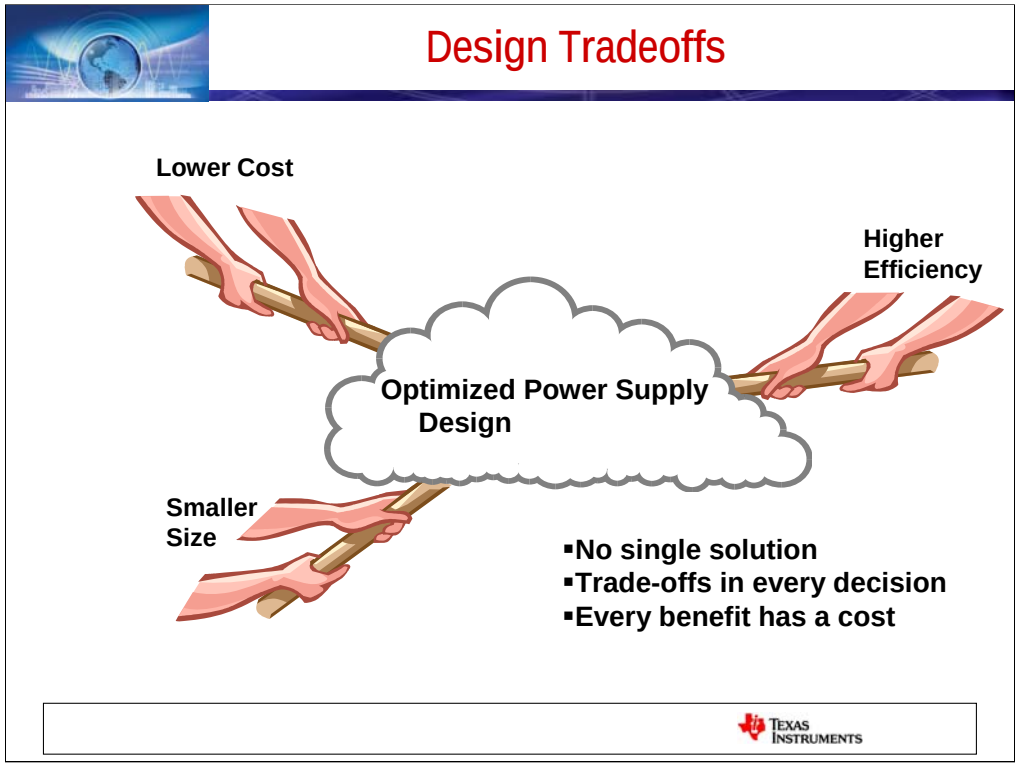
This compares system run time (or battery life) with two converters, one with PFM mode and one without. System 1 has a lower efficiency at high currents, but has PFM mode, so it has a high efficiency at light loads. System 2 has much higher high current efficiency, but doesn't have PFM mode, so it's 1mA efficiency is 10%. 10% efficiency is representative of many low power converters without PFM mode.



The top equation calculates the average current from the battery as a function of the percentage of times the system is in high power mode vs low power mode.

Note that system 1, which has lower efficiency at high current has the longer run time when the system stays in low power mode for longer amounts of time. This is because the efficiency in low power mode starts to dominate. TI's low power DC/DC converters all have PFM mode, which allows for very high efficiency at light loads to significantly extend battery life.

You need to pay attention to the efficiency that corresponds to your system's actual operating conditions



Customers want all three, but the actual optimized design is a tradeoff somewhere in the middle. You need to understand what's most important for the customer.

Design Tradeoffs

	Size	Efficiency	Cost
LDO	**Small (high power dissipation)**	**Low**	**Low**
High Frequency Switcher	**Small**	**Medium**	**High**
High Efficiency Switcher	**Medium-Large**	**High**	**Medium**

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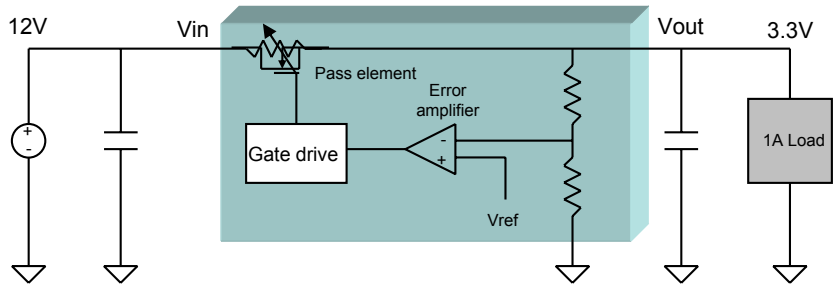
Unfortunately, you can't optimize size, cost, and efficiency

Linear Regulator Power



$$Power = V_{pass\_element} \times I_{load}$$
$$Power = (V_{in} - V_{out}) \times I_{load}$$
$$Power = (12V - 3.3V) * 1A$$
$$Power = 8.7W$$

Let's look at the difference between the power dissipation of an LDO an a switcher. An LDO, as the name implies, operates in the linear region. The pass element, which can be either a FET or a transistor dissipates power in order to regulate the higher input voltage to a lower output voltage. Under steady state operating conditions shown, the pass element can be represented with a resistor. The equation shows how much power is dissipated under these operating conditions. Voltage across the pass element is 8.7V with 1A flowing through it.

Linear Regulator Efficiency

$$Efficiency = \frac{P_{out}}{P_{in}}$$

$$= \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}}$$

$$= \frac{V_{out} \times I_{out}}{V_{in} \times (I_{out} + I_{quiescent})}$$

$$\approx \frac{V_{out} \times I_{out}}{V_{in} \times I_{out}}$$

$$= \frac{V_{out}}{V_{in}}$$

$$= \frac{3.3V}{12V}$$

$$= 27.5\%$$

What's the Li-Ion to 3.3V conversion efficiency?

91.7%

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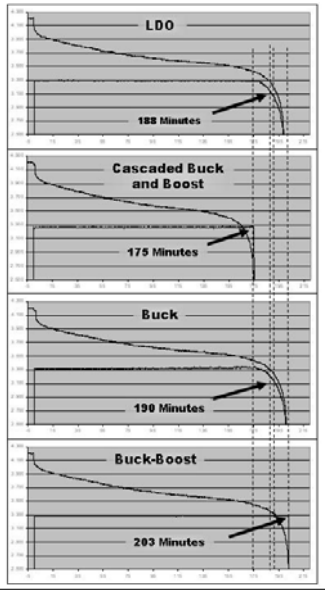
Because the pass element is dissipating power, even an ideal LDO is not 100% efficient. The following equations derive the efficiency for an LDO. Note that the quiescent current is assumed to be negligible when compared to the output current, so the quiescent current term goes to zero. Don't assume that all LDO applications have poor efficiency. What's the efficiency of a LDO that's converting a Li-Ion battery to 3.3V? (calculated with Vbat=3.6V)

Li-Ion to 3.3V run times

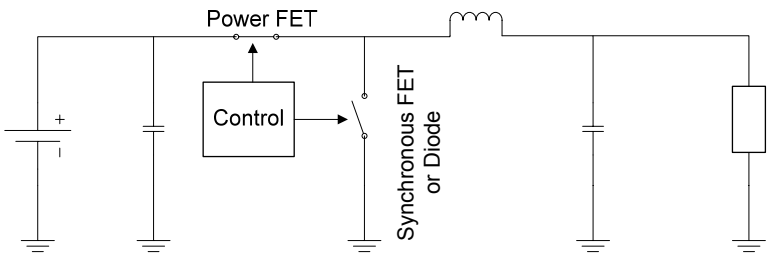


Buck-Boost Converters for Portable Systems, One Solution Does Not Fit All
by Michael Day and Bill Johns

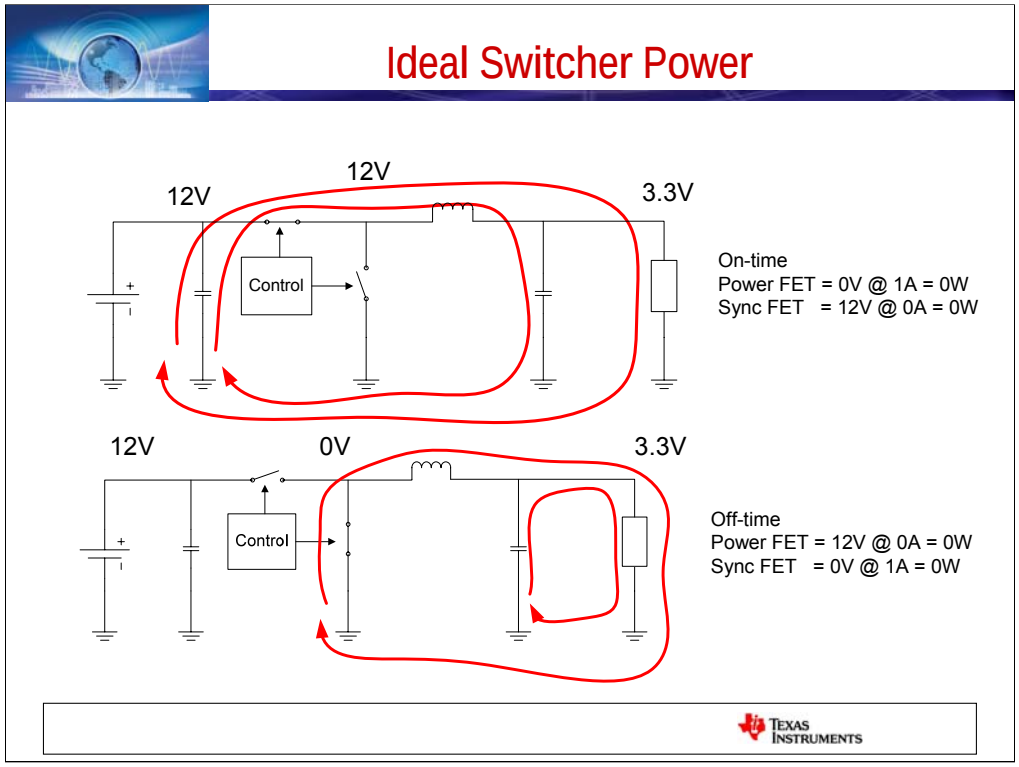
EETimes Asia
Portable Power Online

Texas Instruments

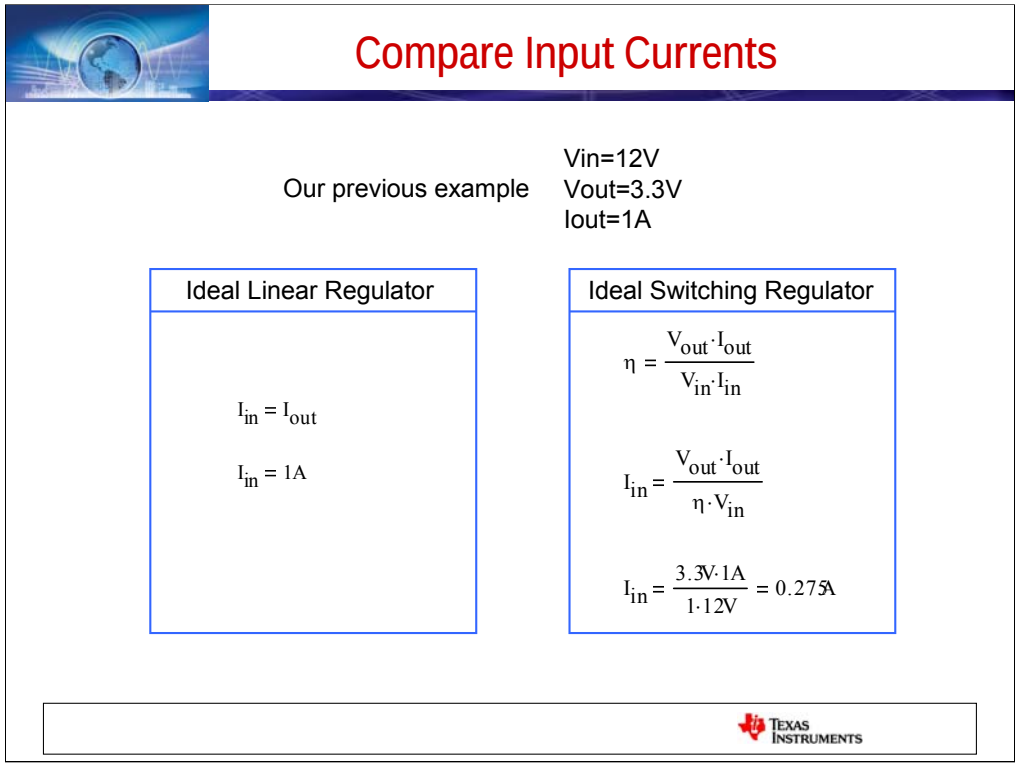
Ideal Switcher Power



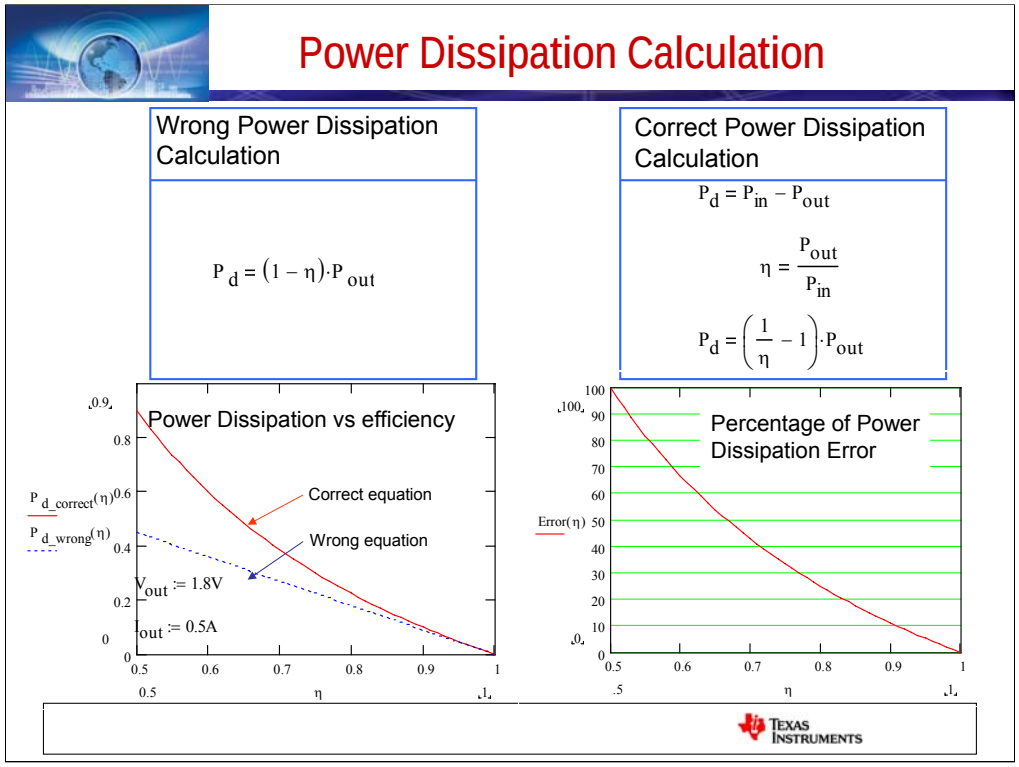
This is the simplified topology for a buck converter.



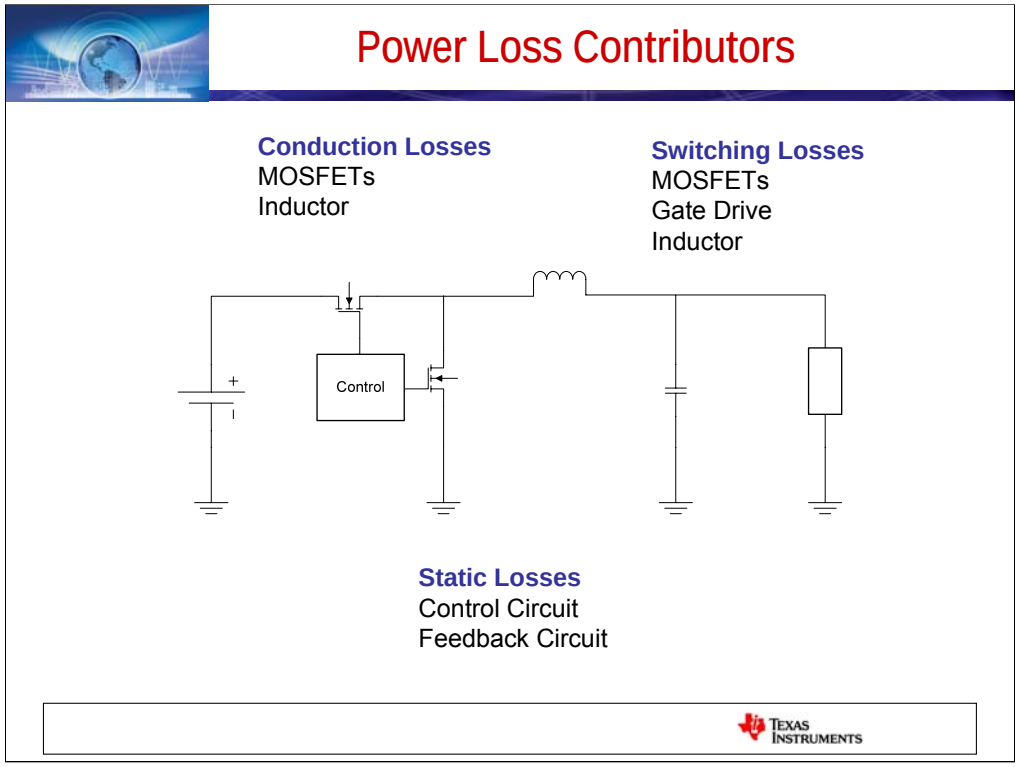
Let's look at the voltages and currents of the buck converter with the same operating conditions that we had for the LDO. During the on-time, the power FET is on and the synchronous FET is off. The output current is flowing through the power FET, but since we are considering the ideal case, the power FET's resistance is zero ohms, so the voltage across it is 0V, and therefore had no power dissipation. The synchronous FET is off, so no current flows through it and it has no power dissipation. During the off-time, the same logic applies and we still have no power dissipation. With no power dissipation, the efficiency is 100%.



Comparing input currents of the ideal LDO and switcher shows how important efficiency is to battery life. The LDO draws 4 times as much current from the battery as the switcher. The result is either much less run time or a much larger (and expensive) battery to achieve the same run time.

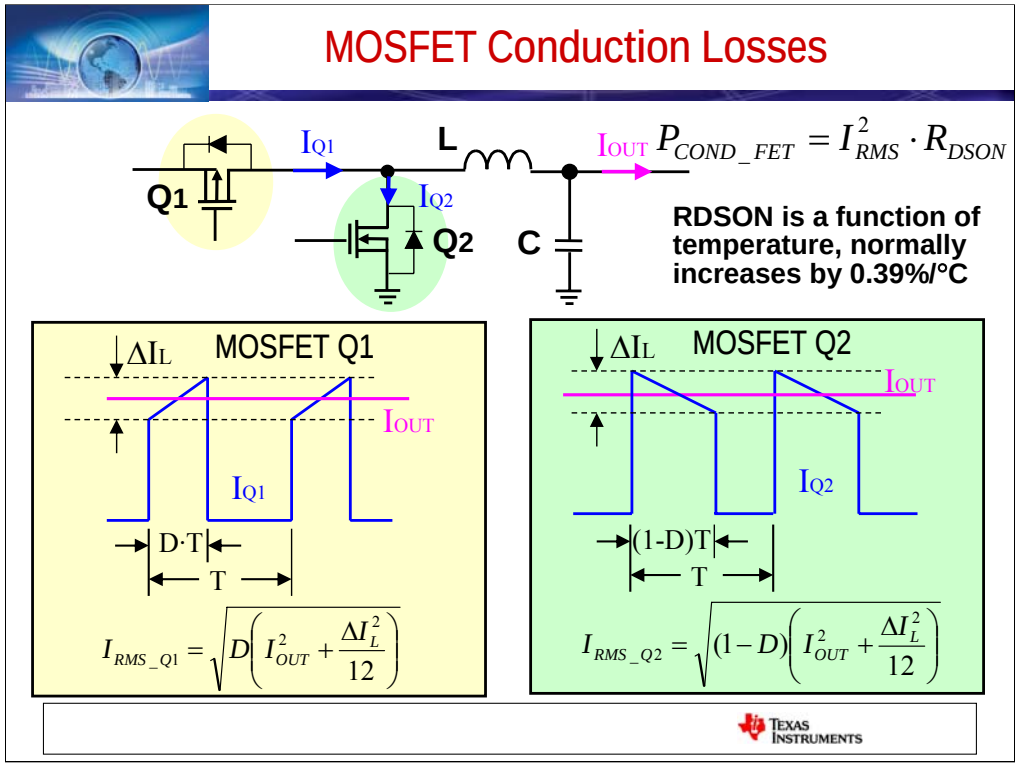


Let's take a closer look at calculating the power dissipation. Many times, we know the load conditions, or output power, and an estimated efficiency from the datasheet. Knowing the output power and the efficiency, we can calculate the power dissipation. However, experience shows that many designers incorrectly calculate the power dissipation. The graph on the left shows the power dissipation calculated with the correct and with the incorrect equation. Using the incorrect equation results in much less power dissipation than the supply actually has. This results in the designer thinking that the system will run longer than it really will. Note that this problem has much more error with lower efficiencies. This is especially important with Linear Regulators



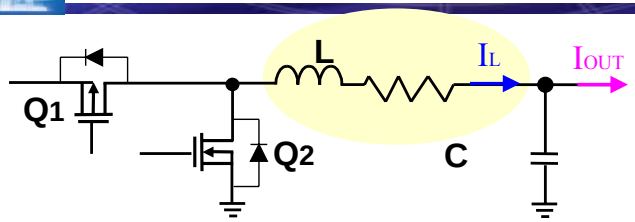
We've been discussing the ideal power supply up to this point. Now let's look at the losses in a real power supply. The actual losses can be broken into three categories: Conduction losses, switching losses, and static losses.

Switching losses come from the currents switching between the power FET and the synchronous FET. Switching losses in the inductor come from the core losses. Gate drive losses are also switching losses because they are required to turn the FETs on and off.

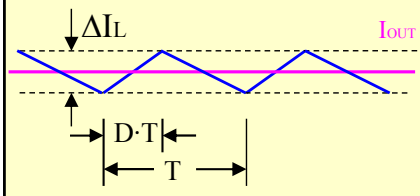


These equations give the Mosfet conduction losses. Note that these are not a function of switching frequency

Inductor Losses



Inductor Current



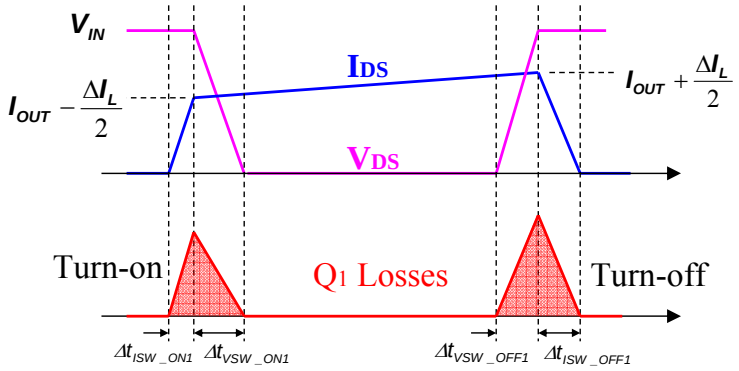
$$I_{RMS\_L} = \sqrt{\left(I_{OUT}^2 + \frac{\Delta I_L^2}{\sqrt{12}}\right)}$$

$$P_{COND\_L} = I_{RMS}^2 \cdot R_{DCR}$$

+ Core Losses?

This equation is very similar to the MOSFET conduction losses. These are also not a function of switching frequency.

MOSFET Switching Losses



$$P_{swon\_Q1} = 0.5 \cdot V_{IN} \cdot (I_{OUT} - \frac{\Delta I_L}{2}) \cdot (\Delta t_{ISW\_ON1} + \Delta t_{VSW\_ON1}) \cdot f_{SW}$$

$$P_{swoff\_Q1} = 0.5 \cdot V_{IN} \cdot (I_{OUT} + \frac{\Delta I_L}{2}) \cdot (\Delta t_{VSW\_OFF1} + \Delta t_{ISW\_OFF1}) \cdot f_{SW}$$

The total switching losses of Q1: $P_{sw\_Q1} = P_{swon\_Q1} + P_{swoff\_Q1}$

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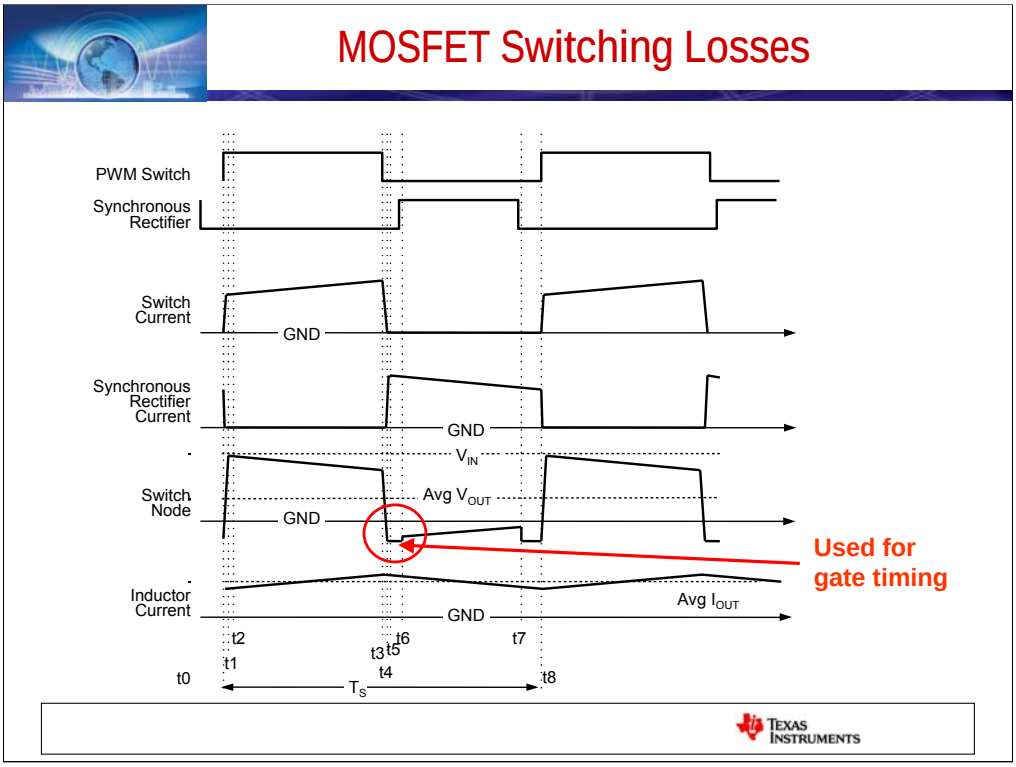
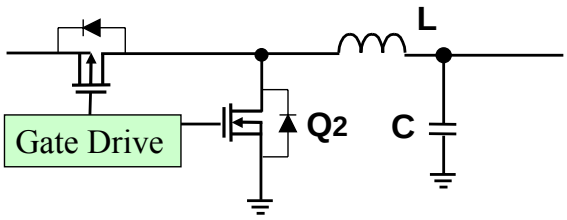
Note that the MOSFET switching losses are a function of load current and the power supply's switching frequency.

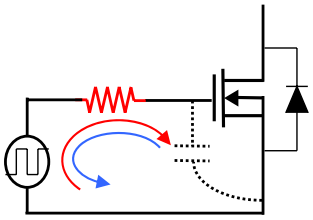
Controller drive capability as well as FET's gate characteristics and circuit parasitics affect tsw



Sync FET diode conduction losses are controller dependent – cross-conduction avoided by drive added delays or by controller automatic adjustment… predictive, adaptive

Gate Drive Losses





$$P_{DRV\_Q1} = Q_{g\_Q1} \cdot V_{DRV\_Q1} \cdot f_{SW}$$

$$P_{DRV\_Q2} = Q_{g\_Q2} \cdot V_{DRV\_Q2} \cdot f_{SW}$$

$$P_{DRV} = P_{DRV\_Q1} + P_{DRV\_Q2}$$

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Gate drive losses are frequency dependent and are also a function of the gate capacitance of the MOSFETS. The higher the switching frequency, the higher the gate drive losses. This is another reason why efficiency goes down as the switching frequency goes up. Larger MOSFETs with lower Rdson provide lower conduction losses, at the cost of higher gate capacitances and therefore higher gate drive losses. These losses can be significant for power supply controllers (with external mosfets) at very high switching frequencies in the multiple MHz region.

Qg represent total gate losses – including Miller efect

Inductor Switching Losses

- **Caused by core loss in the inductor and winding AC losses (skin effect and proximity effect)**
- **Higher ripple current = higher losses**
- **Higher switching frequency = higher losses**
- A higher inductance in the same package reduces AC losses due to reduced Ipk-pk swing but increases the copper DC losses
- AC and DC losses decrease as volume increases…

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Take it with a grain of salt, check the inductor losses in the datasheet – if available

Inductor Switching Losses

TPS62510 inductor losses and efficiency

		SIZE			LOSSES				
Part Number	Inductance	L (mm)	W (mm)	**VOLUME (mm3)**	Rdc (Ohms)	AC Loss (mW)	DC loss (mW)	**Total Loss (mW)**	**Converter Efficiency at full load**
ME3220	2.2µH	3.2	2.5	**16.0**	0.104	21.32	234	**255.32**	**77.9%**
LPS4012	2.2µH	4	4	**19.2**	0.1	14.75	225	**239.75**	**78.2%**
LPS4012	3.3µH	4	4	**19.2**	0.1	12.62	225	**237.62**	**78.3%**
DO1608C	2.2µH	6.6	4.45	**85.8**	0.07	6.63	157.5	**164.13**	**80.0%**
DO1608C	3.3µH	6.6	4.45	**85.8**	0.08	3.88	180	**183.88**	**79.5%**
DO1813H	2.2µH	8.89	6.1	**271.1**	0.035	3.95	78.75	**82.7**	**82.0%**
DO1813H	3.3µH	8.89	6.1	**271.1**	0.04	2.42	90	**92.42**	**81.7%**

A higher inductance in the same package reduces AC losses. However, this example has high DC current so DC losses dominate

AC and DC losses decrease as Volume increase

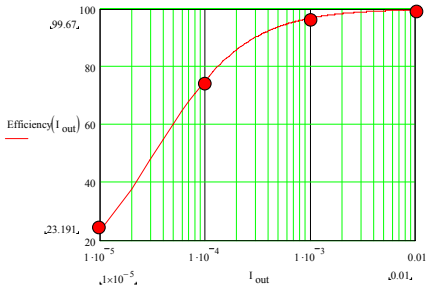
Need to compromise between the inductor size and efficiency

Controller Quiescent Losses

- **Fairly constant with load current.**
- **Becomes significant at light loads**

$$I_{q\_Efficiency\_reduction} = \frac{P_{out}}{P_{out} + V_{in} \cdot I_q} \cdot 100$$

Maximum efficiency assuming all losses = 0 except Iq losses



Iout=10 mA
Effic = 99.%

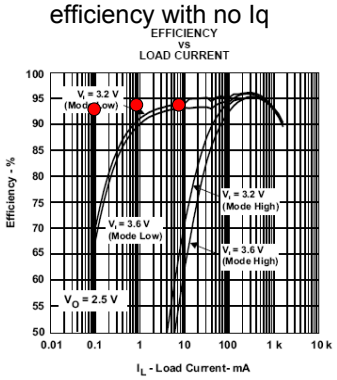
Iout=1 mA
Effic = 96.7%

Iout=0.1 mA
Effic = 75.1%

Iout=0.01 mA
Effic = 23.2%

Vin=3.6V, Vout=2.5V, Iq=23uA

Red dots would be efficiency with no Iq



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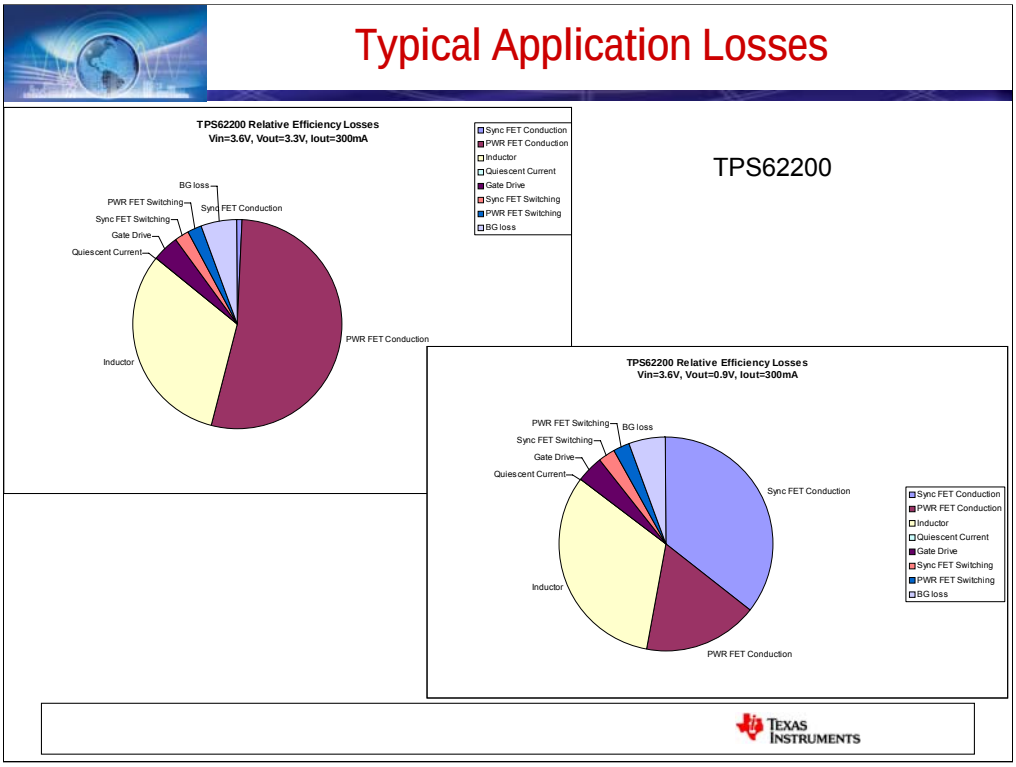
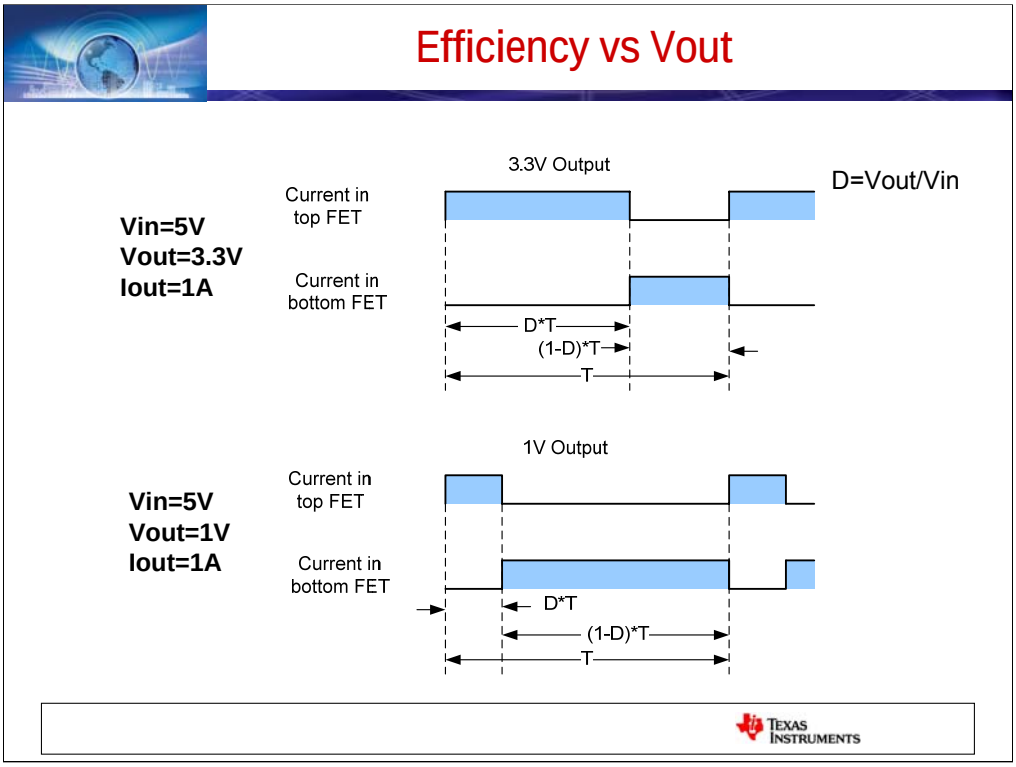
Static losses, such as the quiescent current required to power the control circuitry, are usually ignored because they are relatively low compared to the other losses in the system. However, with very light loads, these losses can be significant. The graph on the left shows the theoretical maximum efficiency assuming zero losses except for quiescent current losses. The graph on the right shows actual measured efficiency. The red dots on the right show what the efficiency would be without the quiescent current.

TI's switching power supplies that are designed for battery applications have a mode of operation called PFM mode. This mode reduces the switching frequency of the converter to minimize switching losses. The graph on the right shows a significant improvement in efficiency in PFM mode at light loads. For instance, with a 10mA load, the efficiency is 60% in PWM mode, but improves to 94% in PFM mode.

Typical Application Losses



Let's look at how the loss terms compare to each other. The TPS62200 Operating with Vin=3.6V, Vout=3.3V and 0.9V, and Iout=300mA has these relative losses. Note the big change in the PWR and Sync FET conduction and switching losses due to the change in duty cycle between 3.3V out and 0.9V out.



Your customers typically want more efficiency in a smaller space at a lower cost than is possible. This example will help show some of the limitations on maximum efficiency. This will show why efficiency drops with lower output voltages. The top waveform is the current through a switcher's power FET. The bottom waveform is the current in the synchronous FET. Current is always flowing through one or the other. The amount of time that current flows through each is a function of the duty cycle. The top example is a 3.3V output, so the duty cycle is 66%. The lower 1V output in the bottom example results in a 20% duty cycle.

Efficiency vs Vout

	3.3V Output	1V Output
Power FET Conduction Losses	$P_{FET\_PWR} = (I_{out} \cdot \sqrt{D})^2 \cdot R_{dson}$ $P_{FET\_PWR} = (1A \cdot \sqrt{0.67})^2 \cdot 0.200\Omega$ $P_{FET\_PWR} = 0.132W$	$P_{FET\_PWR} = (I_{out} \cdot \sqrt{D})^2 \cdot R_{dson}$ $P_{FET\_PWR} = (1A \cdot \sqrt{0.2})^2 \cdot 0.200\Omega$ $P_{FET\_PWR} = 0.040W$
Sync FET Conduction Losses	$P_{FET\_SYNC} = (I_{out} \cdot \sqrt{1-D})^2 \cdot R_{dson}$ $P_{FET\_SYNC} = (1A \cdot \sqrt{0.33})^2 \cdot 0.120\Omega$ $P_{FET\_SYNC} = 0.041W$	$P_{FET\_SYNC} = (I_{out} \cdot \sqrt{1-D})^2 \cdot R_{dson}$ $P_{FET\_SYNC} = (1A \cdot \sqrt{0.8})^2 \cdot 0.120\Omega$ $P_{FET\_SYNC} = 0.096W$
Total FET Losses (does not include other circuit losses)	0.173 W	0.136 W

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Using the equations from earlier in the presentation and simplifying them by assuming zero ripple current, results in the power dissipations shown. Note that the Rdsons are different for the Power FET and the Sync FET. This is usually true for low power parts. The Power FET is typically a P-ch FET which has a much larger resistance per unit area than the N-ch sync FET. The relative Rdson's will be designed for optimum die size and efficiency for the IC's typical application.

If we ignore all other losses, we see that the power dissipation is slightly higher for the 3.3V output. If this is true, we might expect the 3.3V efficiency to be slightly lower than the 1V efficiency. Is this true?

Efficiency vs Vout

3.3V Output

$$\eta = \frac{P_{out}}{P_{out} + P_d}$$

$$\eta = \frac{3.3W}{3.3W + 0.173W}$$

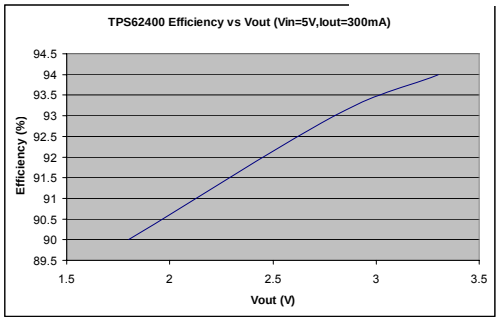
$\eta = 95.0\%$

1V Output

$$\eta = \frac{P_{out}}{P_{out} + P_d}$$

$$\eta = \frac{1W}{1W + 0.136W}$$

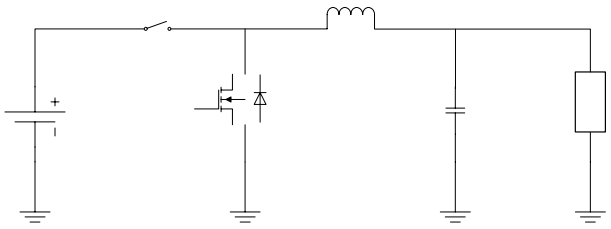
$\eta = 88.0\%$



The answer is “NO!” We can see that although the 3.3V power dissipation is higher, the power dissipation is a much smaller percentage of the output power for the 3.3V output. With this knowledge, you can help your customer understand why their 1.2V core supply is not as efficient as their 3.3V I/O supply. The power dissipation may actually be lower on their 1.2V output, but the efficiency will also be lower.

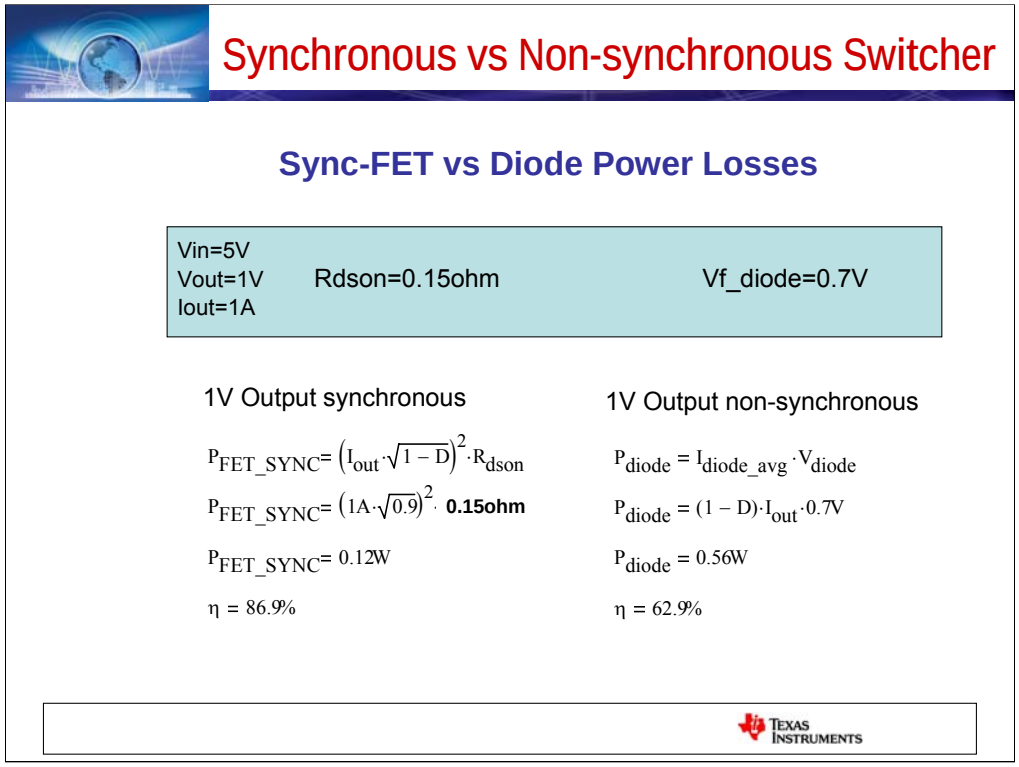
Synchronous vs Non-synchronous Switcher

Synchronous = FET
Non-synchronous = Diode



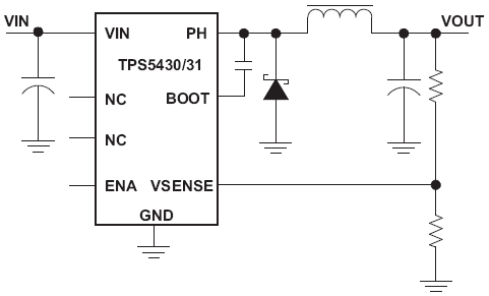
Non-synchronous
1. Diode voltage drop is fairly constant with output current
2. Less efficient

Synchronous Switcher is more efficient
1. Requires additional control circuitry
2. Costs more



For this example, we see that the diode losses are much higher than the FET losses. This results in a much lower efficiency for the non-synchronous converter. Also, note that the losses in the diode are calculated differently than the losses in the FET. Diode losses are calculated with the average diode current rather than the RMS current.

Why use the non-synchronous TPS5430 ?

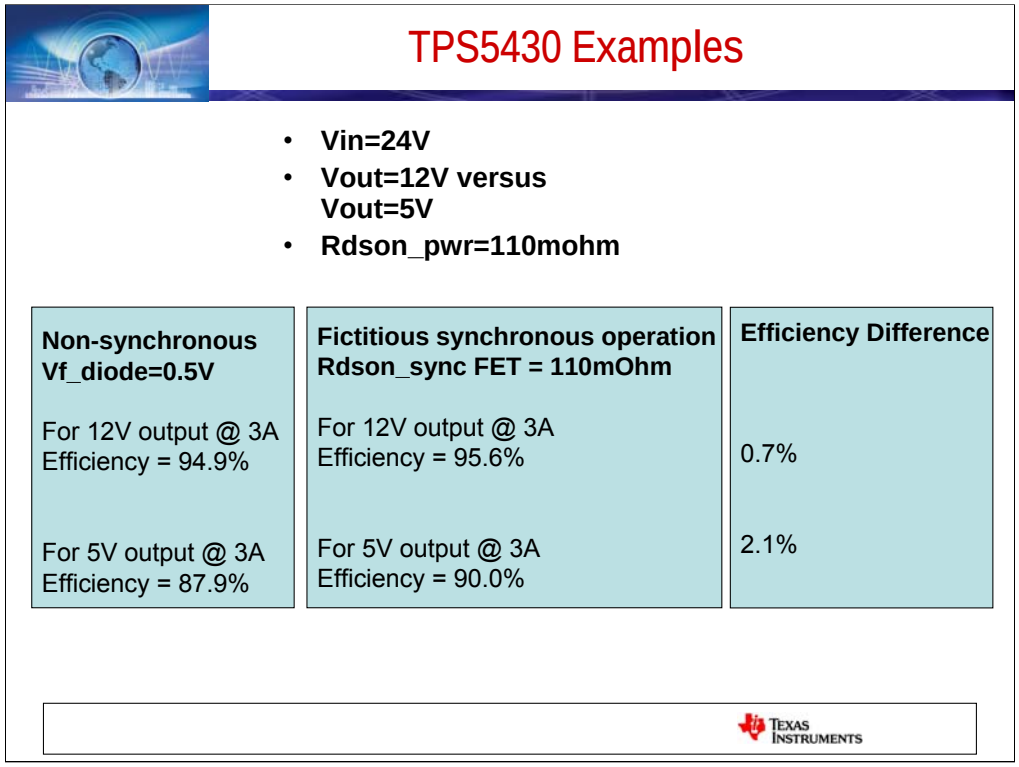


Typical Application

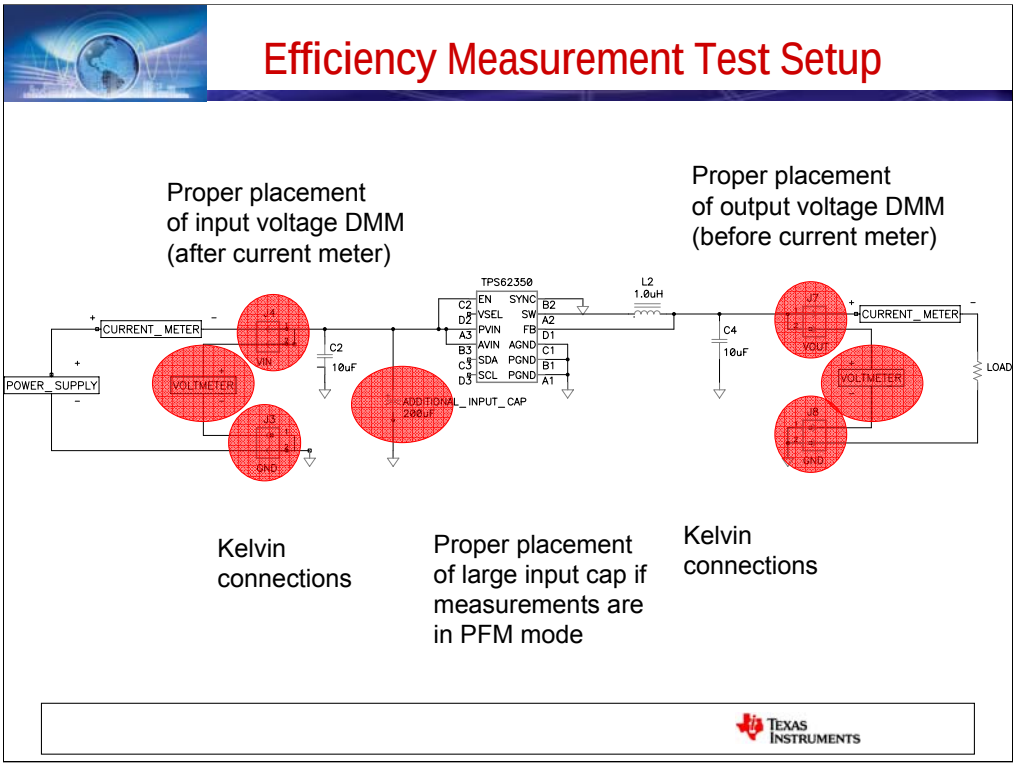
- **High Vin (24V bus)**
- **Med to High Vout (12V distributed, 5V POL)**
- **Med output currents (2-3A)**

- **Keeps duty cycle relatively high**
- **Keeps power relatively high compared to diode losses**

If the non-synchronous switcher is less efficiency than the synchronous switcher, then why do we use non-synchronous switchers? One reason is cost. The diode is cheaper than a FET, and it doesn't require control circuitry. With the right conditions, such as these, the output power stays relatively high compared to the losses, so there isn't that big of a hit on efficiency. That's a system level tradeoff of efficiency vs cost, and most customers choose the cost.

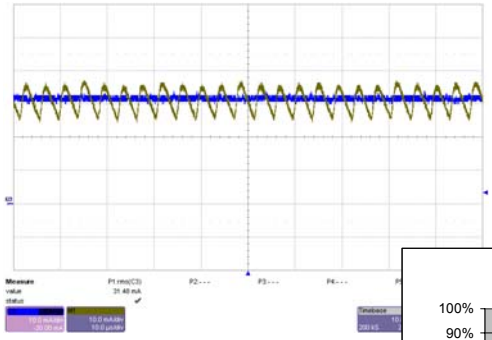


In this example, we assume the TPS5430 is used with a Schottky diode with a 0.5V drop. In the fictitious synchronous, we assume a 110mohm FET. This is a realistic FET rdson that may be chosen for these operating conditions. The synchronous example is more efficient, but not by much. Couple this with the fact that this is a line powered system, not a battery powered system, and the cheaper non-synchronous topology is the clear winner.



We are very concerned about the efficiencies of our power supplies, but often don't pay much attention to how we measure efficiency. There are some basic rules to follow when measuring efficiency that will help ensure accurate measurements. 1st, proper placement of the input DMM. This must be after the current meter. The current meter has a voltage drop across it. Measuring the voltage on the left side of the current meter results in a higher voltage measurement, therefore a higher input power, therefore a lower efficiency calculation. 2nd is the output voltage measurement. It must be measured before the current meter to ensure that the voltage drop and power dissipation in the output current meter are considered part of the output power. Taking the output voltage measurement on the right side of the current meter would place the current meters power into the power dissipation portion of the efficiency equation. 3rd is to ensure that the voltage measurements are made with kelvin connections. This ensures that the voltage drop and power loss in the connectors does not affect the efficiency measurement. 4th is relevant to low power supplies. The test setup must have a large input capacitor. The next slide shows why.

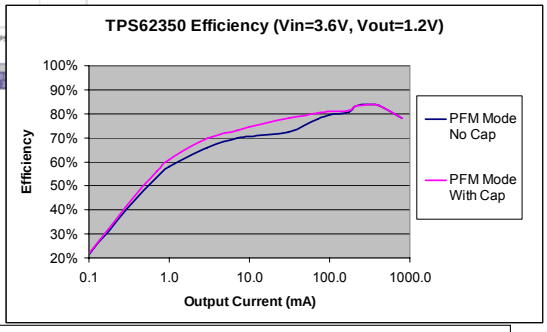
PFM Efficiency Measurement



Sawtooth is input current through DMM in PFM mode with no input cap

Flat waveform is input current through DMM in PFM mode with a large input cap

The DMM measures the RMS current, which shows larger input power than the acutal average input current.



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In PFM mode, the input current waveform is a sawtooth rather than a DC waveform. The current meter displays the RMS value of the current flowing through it. The sawtooth waveform has a higher RMS value than average value, but we need the average value for our efficiency measurement. Using the higher RMS value results in a lower efficiency calculation. Adding the large capacitor allows the power supply to pull the AC component of the sawtooth current out of this cap. Then, only DC flows through the current meter. The graph shows that without the additional input capacitor, low power efficiency measurements may be a much as 8% lower than the actual efficiency.

Conclusions

- **Power supply efficiency is important**
  - Cost, power dissipation, and run time
- **Power loss terms**
  - Conduction vs switching vs static
  - Size, efficiency, and cost can't all be optimized
- **Efficiency drops with lower Vout**
  - How this is affected by synchronous vs asynchronous
- **Proper efficiency measurements are critical to getting the correct low power efficiency measurement**