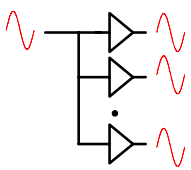
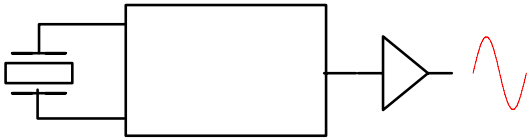
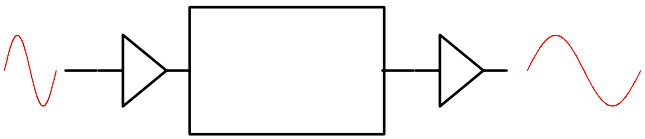
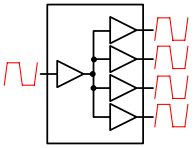
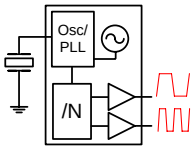
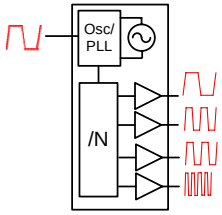
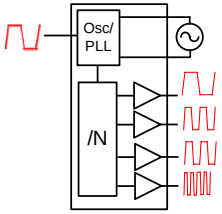
# TI's Clocking Solutions

# Timing Devices – Basic Functions

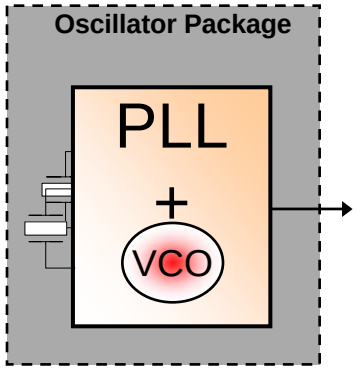
| | |
|---|---|
| **Buffer**  | **Jitter Cleaner**  |
| **Control Skew**  | **Spread Spectrum**  |
| **Multiply**  | **Generate Clocks from XTALs**  |
| **Divide**  | **Combinations** |

# New Product Offering at a Glance

| Product Category | Typical Block Diagram | Key Parameters | Applications | | | | | Newly Released Products | Near Future Product Releases | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Specialty Clocking | XO Replacement | Jitter Cleaning | Data Clocking | ADC/DAC Clocking | | Family | Samples | Production |
| Fan-Out Buffers |  | Skew<br>Residual Jitter | | | | ✓ | ✓ | CDCE18005<br>CDCLVP110<br>CDCLVP111<br>CDCLVP215 | **CDCLVP1xxx**<br>**CDCLVP2xxx**<br>**CDCLVD1xxx**<br>**CDCLVD2xxx** | **Q2 '09**<br>**Nov '09** | **Q3 '09**<br>**June '10** |
| Clock Generators |  | Spurious Jitter/Phase Noise | ✓ | ✓ | | ✓ | | CDCE421A<br>CDCM6100x<br>CDCE(L)9xx<br>CDCE706<br>CDCE906<br>**CDCS50x** | | | |
| High Performance Jitter Cleaners/ Clock Generators |  | Skew<br>Spurious Jitter/Phase Noise | | | ✓ | ✓ | ✓ | CDCE62005 | CDCE62002<br>CDCE6xxxx | Apr '09<br>Q4 '09 | July '09<br>Q4 '10 |
| Ultra-High Performance Jitter Cleaners/ Clock Generators |  | Skew<br>Spurious Jitter/Phase Noise | | | ✓ | ✓ | ✓ | CDC7005<br>CDCM7005<br>CDCE72010 | CDCEHxxxx<br>CDCE72005 | Q3 '09<br>Q4 '09 | 'Q4 '10<br>Q4 '10 |

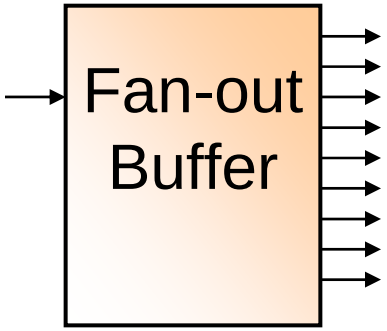
# Typical Clock Chain

## *Oscillator IC*



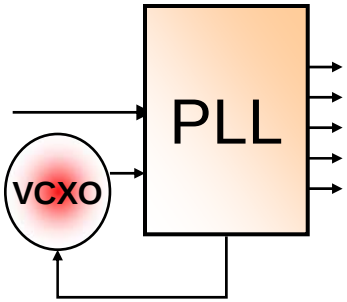

- *Data Com*
- *General Purpose*

## *Clock Buffers*



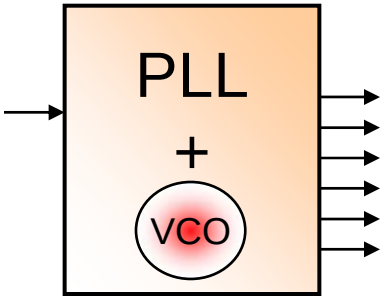

- *SONET*
- *Wireless BTS*
- *Data Com*
- *Medical*
- *Test Equipment*

## *External VCO Clock Generators*



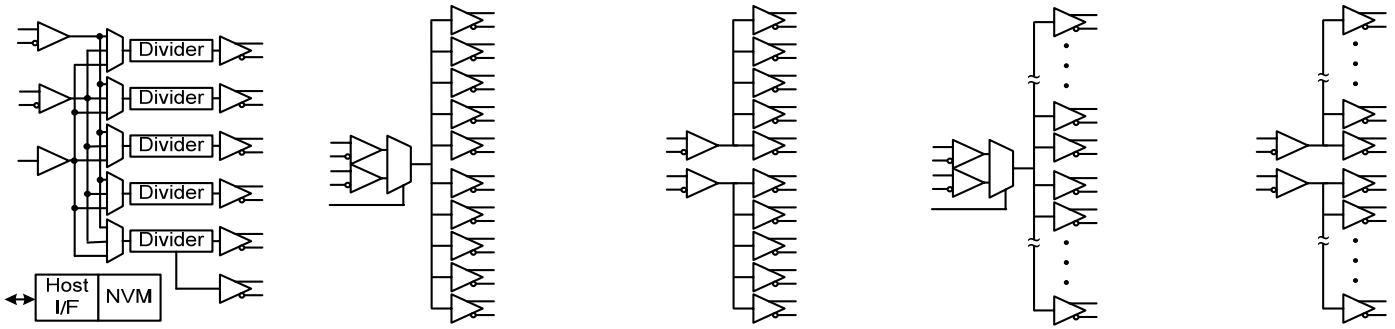

- *SONET*
- *Wireless BTS (macro)*
- *Test Equipment*
- *Data Com*

## *On-Chip VCO Clock Generators*




- *Wireless BTS (pico/WiMax)*
- *Data Com*
- *Medical*
- *Test Equipment*

# Buffer Portfolio



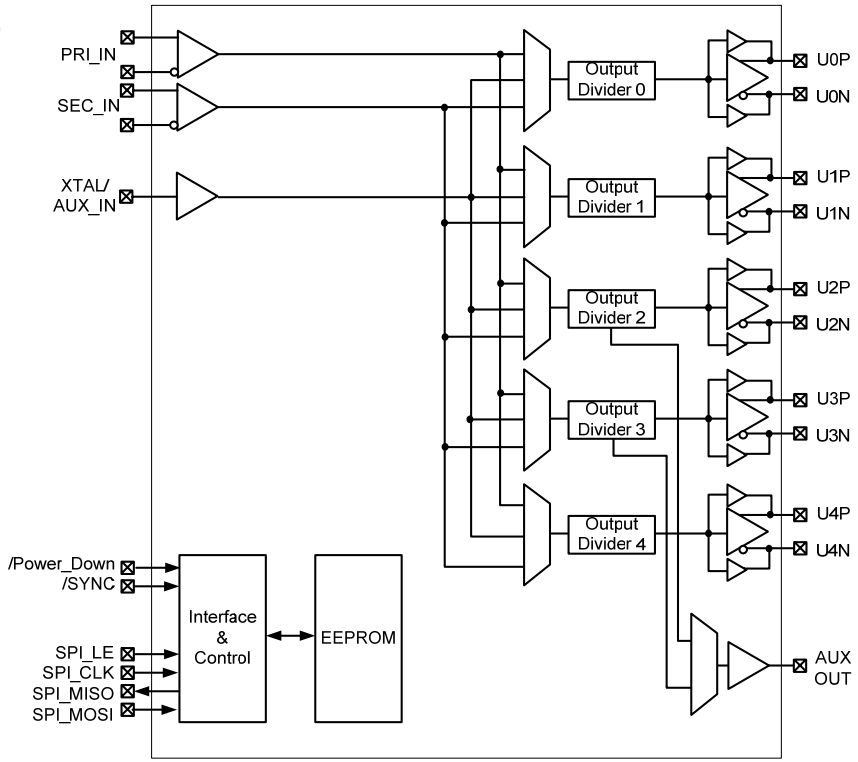

| Product | CDCE18005 | *CDCLVP110/111* | CDCLVP215 | CDCLVP12xx | CDCLVP21xx |
|---|---|---|---|---|---|
| **Input** | Dual Universal:<br>LVPECL: 1500 MHz<br>LVDS: 800 MHz<br>LVCMOS: 250 MHz<br>Auxiliary:<br>LVCMOS or XTAL | Up to 3.5 GHz<br>CDCLPV110:<br>LVPECL or HSTL<br>CDCLVP111:<br>LVDS, CML, SSTL | Up to 3.5 GHz<br>LVPECL | Up to 2.0 GHz<br>LVPECL;<br>LVDS or<br>LVCMOS/<br>LVTTL | Up to 2.0 GHz<br>LVPECL;<br>LVDS or<br>LVCMOS/<br>LVTTL |
| **Output**[1] | Five Universal with dedicated divider stage (LVPECL, LVDS, or two LVCMOS) up to 1500 MHz | Ten LVPECL | Ten LVPECL | LVPECL:<br>CDCLVP1204 2:4<br>LCDLVP1208 2:8<br>CDCLVP1212 2:12<br>CDCLVP1216 2:16 | LVPECL:<br>CDCLVP2102: Dual 1:2<br>CDCLVP2104: Dual 1:4<br>CDCLVP2106: Dual 1:6<br>CDCLVP2108: Dual 1:8 |
| **Additive Jitter**[2] | < 100 fs RMS | < 1 ps cy-cy | < 800 fs RMS<br>(20k – 20M) | < 100 fs RMS | < 100 fs RMS |
| **Skew** | < 75 ps | 15 ps | 15 ps | 15 ps | 15 ps |
| **Topology** | Smart Buffer<br>3:5 | *2:10* | Dual 1:5 | 2:N | *Dual 1:N* |
| **Power**[3] | 1,000 mW | 280 mW | 300 mW | 180 mW (1204)<br>360 mW (1216) | 180 mW (2102)<br>360 mW (2108) |
| **Special Features** | EEPROM, SPI, Dividers, Skew Control | *Drop in replacement for industry standard* | *Drop in replacement for industry standard* | Ultra low jitter, skew, and power, 60dB ch-ch isolation | Ultra low jitter, skew, and power, 60dB ch-ch isolation |
| **Package** | *QFN48* | *QFN32*<br>*LQFP32* | *QFN32* | *QFN16,28,40,48* | *QFN16,28,40,48* |
| **Availability** | NOW | *NOW* | *NOW* | *Summer '09* | *Summer '09* |

[1]Unless otherwise noted, frequencies are listed in MHz.
[2]RMS Jitter calculated over an integration bandwidth of 10 kHz to 20 MHz.
[3]Typical configuration, all outputs enabled.

# CDCE18005

## *Programmable 3:5 Smart Buffer*

- Smart Clock Distribution Device with universal I/O, output dividers, and skew control.
- Low Additive Jitter
- Two Universal Inputs, One Auxiliary Input
  - Differential or Single Ended Modes: LVPECL (up to 1500 MHz), LVDS (up to 800 MHz), LVCMOS (up to 250 MHz)
  - One Auxiliary Input accepts single ended signal up to 75 MHz or a crystal (2 MHz – 42 MHz)
  - Use of XTAL on Auxiliary port enables holdover and SERDES startup modes.
- 5/10 Outputs (5 differential, 10 single-ended)
  - LVPECL Mode up to 1500 MHz, LVDS mode up to 800 MHz, LVCMOS mode up to 250 MHz
  - Adjustable Skew
  - Dedicated Divide Ratio per Channel
- On-chip EEPROM determines default state at power up
- Offered in a QFN-48 package.
- ESD Protection exceeds 2 kV HBM.
- Fully programmable via SPI port.



# CDCLVP111

*2:10 LVPECL Clock Buffer with selectable Inputs*

## • Features

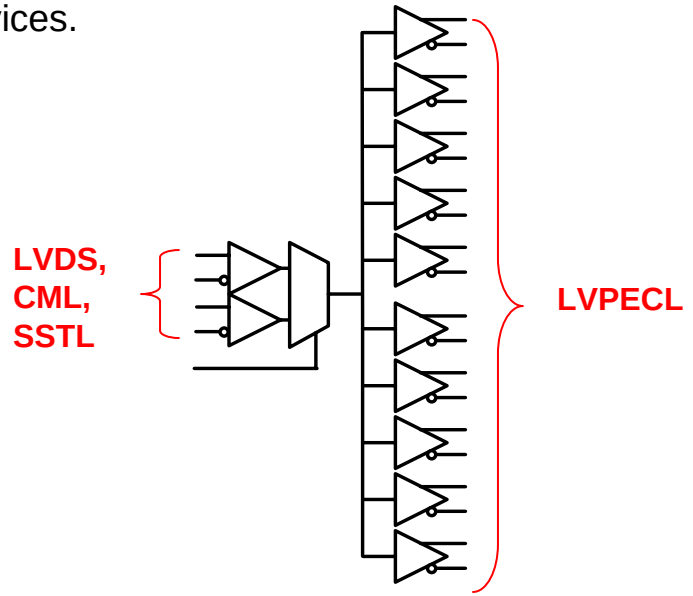
- •Frequency range form DC to 3.5 GHz
- •Supply Voltage Range 2.375V – 3.8 V
- •Low Output Skew (15 ps)
- •LVDS, CML, SSTL Input Compatible
- •VBB Reference Voltage Output for Single-Ended Clocking
- •Available in QFN32 or LQFP32 Package

## • Benefits

- •Wide range supports various applications and can be used across multiple designs.
- •Wide supply voltage saves cost on LDO.
- •Low skew insures high quality clock distribution.
- •Flexible inputs
- •Enables good quality single ended distribution for design flexibility
- •Small package saves board space.
- •Drop in replacement for industry standard devices.

## • Applications

- •Wireless BTS
- •Data Communications
- •Medical
- •Test Equipment




1Ku / $5.55

Texas Instruments

# CDCLVP215

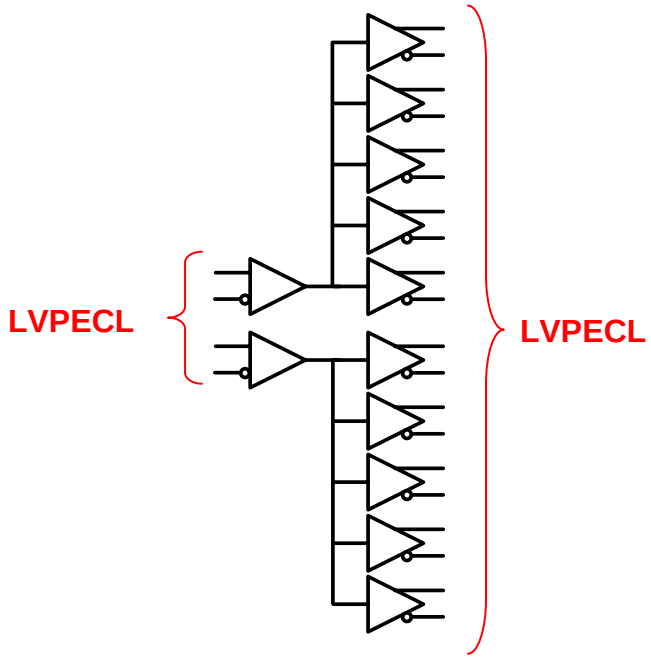
*Dual 1:5 High Speed LVPECL Fan Out Buffer*

- **Features**
  - •Frequency Range from DC – 3.5 GHz
  - •Supply Range from 2.375V – 3.8V
  - •Low Output Skew (typ 15 ps)
  - •VBB Reference Voltage Output supports single ended clocking
  - •Available in QFN32 Package
  - •Pin to Pin Compatible with ON Semi MC100 Series

- **Benefits**
  - •Wide range supports various applications therefore one device can be used in multiple designs.
  - •Wide supply voltage saves cost on LDO
  - •Low skew insures high quality clock distribution.
  - •Small package saves board space
  - •Drop in replacement for industry standard.

- **Applications**
  - •Telecommunications
  - •Data communications
  - •Medical Imaging
  - •Device using High-End A/D
  - •Wireless BTS

1Ku / $6.10



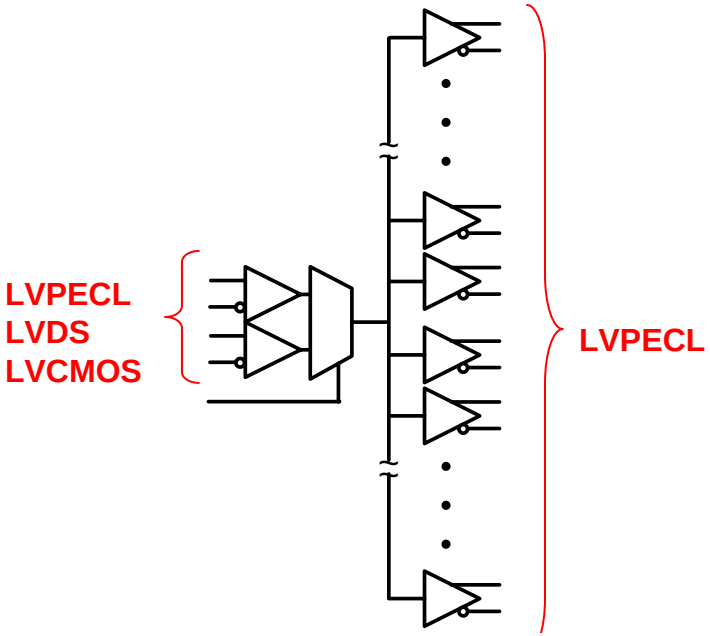

Texas Instruments

# CDCLVP1102/1204/1208/1212/1216

## *2:4/8/12/16 Universal-to-LVPECL Fan-out Buffer*

- **Features**
  - •Total Additive Jitter <100 fs, RMS
  - •Distributes one of two Clock/Data Inputs to 4/8/12/16 LVPECL Outputs
  - •Signaling Rate Up to 2.0 GHz
  - •Operating conditions of 2.375 to 3.6 V, -40 to 85 C
  - •Low core current of 60/80/100/120 mA
  - •Universal Inputs (LVDS, LVPECL, LVCMOS/TTL)
  - •VBB pin for single ended operation

- **Applications**
  - •Router/Switch
  - •Datacom/Telecom
  - •Wireless Infrastructure
  - •Networking
  - •General Purpose Differential clock buffering



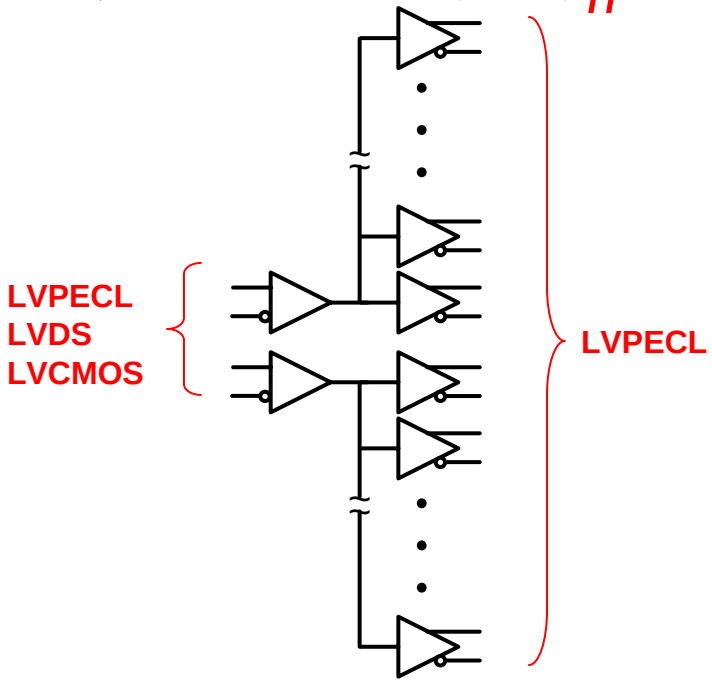

**Q2 Samples**
**RTM Summer '09**

| | CDCLVP1204 | CDCLVP1208 | CDCLVP1212 | CDCLVP1216 |
|---|---|---|---|---|
| Frequency(Max) (MHz) | 2000 | 2000 | 2000 | 2000 |
| VCC(V) | 3.3 | 3.3 | 3.3 | 3.3 |
| Input Level | LVPECL, LVDS, LVCMOS | LVPECL, LVDS, LVCMOS | LVPECL, LVDS, LVCMOS | LVPECL, LVDS, LVCMOS |
| No. of Outputs | 4 | 8 | 12 | 16 |
| Output Level | LVPECL | LVPECL | LVPECL | LVPECL |
| Pin/Package | 16QFN | 28QFN | 40QFN | 48QFN |
| Operating Temp Range(Celsius) | | | | -40 to 85 |
| Tsk(o)(ps) | 20 | 20 | 25 | 30 |
| | Samples | Samples | Samples | Samples |

# CDCLVP2102/2104/2106/2108

## *Dual 1:2/4/6/8 Universal-to-LVPECL Fan-out Buffer*

- **Features**
  - •Total Additive Jitter < 100 fs, RMS
  - •Dual Buffers distribute one clock input to 2/4/6/8 outputs each
  - •Signaling Rate Up to 2.0 GHz
  - •QFN-16/28/40/48 Package
  - •Operating conditions of 2.375 to 3.6 V, -40 to 85 C
  - •Low core current of 60/80/100/120 mA
  - •VBB pin for single ended operation
- **Applications**
  - •Router/Switch
  - •Datacom/Telecom
  - •Wireless Infrastructure
  - •Networking
  - •General Purpose Differential clock buffering




| | CDCLVP2102 | CDCLVP2104 | CDCLVP2106 | CDCLVP2108 |
|---|---|---|---|---|
| Frequency(Max) (MHz) | 2000 | 2000 | 2000 | 2000 |
| VCC(V) | 3.3 | 3.3 | 3.3 | 3.3 |
| Input Level | LVPECL, LVDS, LVCMOS | LVPECL, LVDS, LVCMOS | LVPECL, LVDS, LVCMOS | LVPECL, LVDS, LVCMOS |
| No. of Outputs | 4 | 8 | 12 | 16 |
| Output Level | LVPECL | LVPECL | LVPECL | LVPECL |
| Pin/Package | 16QFN | 28QFN | 40QFN | 48QFN |
| Operating Temp Range(Celsius) | | | | |
| Tsk(o)(ps) | 20 | 20 | 25 | 30 |
| | Samples | Samples | Samples | Samples |

**Q2 Samples**
**RTM Summer '09**

Texas Instruments

# New LVPECL Buffer Drop-in Replacement

| Device Package | TI Device | ON Semi Device | IDT | NXP | Maxim | Pericom |
|---|---|---|---|---|---|---|
| 32-QFP | CDCLVP111VF | MC100LVEP111FAG | MC100ES6111AC | PTN1111BD | MAX9311ECJ | X |
| | CDCLVP111VFR | MC100LVEP111FARG | MC100ES6111ACR2 | PTN1111BD | MAX9311ECJ | X |
| 32-QFN | CDCLVP111RHBT | MC100LVEP111MNG | X | X | MAX9311EGJ | X |
| | CDCLVP111RHBR | MC100LVEP111MNRG | X | X | MAX9311EGJ | X |
| 32-QFN | CDCLVP215RHBT | MC100LVEP210MNG | X | PCK210BS | MAX9312EGJ | X |
| | CDCLVP215RHBR | MC100LVEP210MNR2G | X | PCK210BS | MAX9312EGJ | X |
| 32-QFP | CDCLVP110VF | X | ICS853111AY-02LF | X | X | PI6C4853111FAE |
| | CDCLVP110VFR | X | ICS853111AY-02LFT | X | X | PI6C4853111FAE |

CDCLVP111: 2.5V/3.3V 1:10 LVPECL buffer with input mux and input termination resistors

CDCLVP110: 2.5V/3.3V 1:10 LVPECL buffer with input mux

CDCLVP215: Dual channel 1:5 LVPECL buffer

**Slight difference between 111 and 110:**

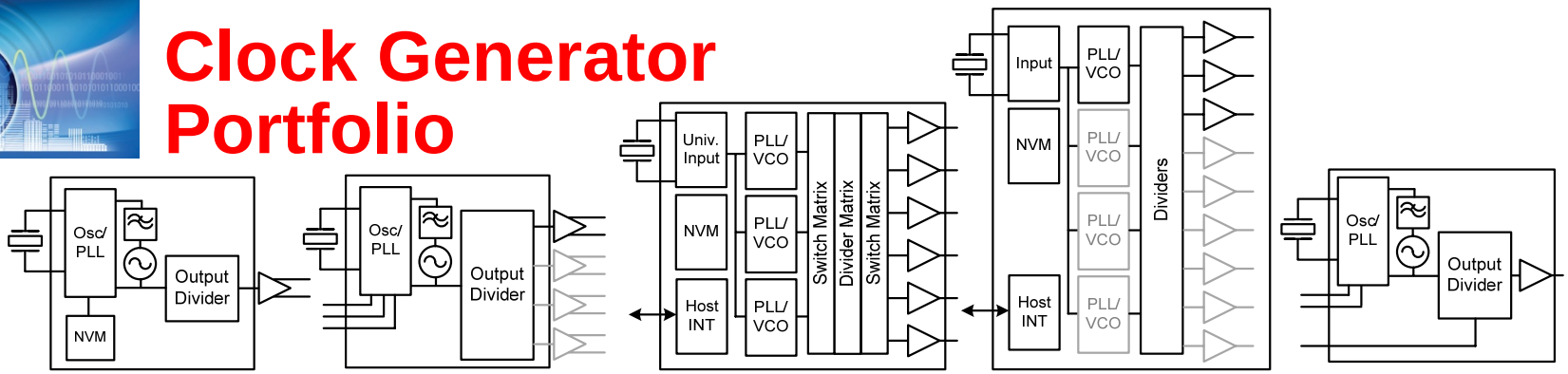
**1. CDCLVP111 provides integrated pull-up/pull down resistors at the input for proper DC bias when there is no active signal being transmitted. CDCLVP110 does not have this.**

**2. CDCLVP111 has both QFN and LQFP packages to competition equivalent while CDCVP110 only has LQFP package**

# New PECL Translation Logic

| ON Semi Device | | Mircel Device | | TI Device | |
|---|---|---|---|---|---|
| **98 (100) Units / Rail** | **2500 / Tape & Reel** | **98 Units / Rail** | **2500 / Tape & Reel** | **80 Units / Tube** | **2500 / Tape & Reel** |
| MC10(0)LVEP11D(G) | MC10(0)LVEP11DR2(G) | SY10(0)EL11VZG | SY10(0)EL11VZGTR | SN65LVEP11D | SN65LVEP11DR |
| MC10(0)LVEP11DT(G) | MC10(0)LVEP11DTR2(G) | - | - | SN65LVEP11DGK | SN65LVEP11DGKR |
| MC10(0)EL11D(G) | MC10(0)EL11DR2(G) | - | - | SN65EL11D | SN65EL11DR |
| MC10(0)EL11DT(G) | MC10(0)EL11DTR2(G) | - | - | SN65EL11DGK | SN65EL11DGKR |
| MC100LVEL11D(G) | MC100LVEL11DR2(G) | - | - | SN65LVEL11D | SN65LVEL11DR |
| MC100LVEL11DT(G) | MC100LVEL11DTR2(G) | - | - | SN65LVEL11DGK | SN65LVEL11DGKR |
| MC10(0)EL16D(G) | MC10(0)EL16DR2(G) | SY10(0)EL16VZG | SY10(0)EL16VZGTR | SN65EL16D | SN65EL16DR |
| MC10(0)EL16DT(G) | MC10(0)EL16DTR2(G) | SY10(0)EL16VKG | SY10(0)EL16VKGTR | SN65EL16DGK | SN65EL16DGKR |
| MC10(0)ELT22D(G) | MC10(0)ELT22DR2(G) | SY10(0)ELT22LZG | SY10(0)ELT22LZGTR | SN65ELT22D | SN65ELT22DR |
| MC10(0)ELT22DT(G) | MC10(0)ELT22DTR2(G) | - | - | SN65ELT22DGK | SN65ELT22DGKR |
| MC100EPT22D(G) | MC100EPT22DR2(G) | SY100EPT22VZG | SY100EPT22VZGTR | SN65EPT22D | SN65EPT22DR |
| MC100EPT22DT(G) | MC100EPT22DTR2(G) | SY100EPT22VKG | SY100EPT22VKGR | SN65EPT22DGK | SN65EPT22DGKR |
| MC100LVELT22D(G) | MC100LVELT22DR2(G) | - | - | SN65LVELT22D | SN65LVELT22DR |
| MC100LVELT22DT(G) | MC100LVELT22DTR2(G) | - | - | SN65LVELT22DGK | SN65LVELT22DGKR |
| MC10(0)ELT20D(G) | MC10(0)ELT20DR2(G) | SY100ELT20VGZ | SY100ELT20VGZTR | SN65ELT20D | SN65ELT20DR |
| MC10(0)ELT20DT(G) | MC10(0)ELT20DTR2(G) | - | - | SN65ELT20DGK | SN65ELT20DGKR |

# Clock Generator Portfolio



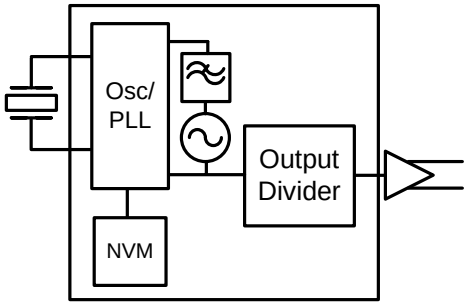

| Product | CDCE421A | *CDCM61001,2,4* | CDCE706/906 | CDCE(L)9xx | CDCS502 |
|---|---|---|---|---|---|
| **Input** | Crystal or LVCMOS (27MHz to 38 MHz) | *Crystal or LVCMOS 25MHz, 26.5625 MHz, and 24.8832 MHz* | Differential/LVCMOS up to 200 MHz, XTAL up to 54 MHz | LVCMOS up to 160 MHz, XTAL 8 MHz - 32 MHz | XTAL 8 MHz -32 MHz |
| **PLL** | 1 X Integer | *1 X Integer* | 3 X Fractional | 1,2,3, or 4 Fractional | 1 X Integer |
| **Output**[1] | 10.9 MHz – 1175 MHz LVDS or LVPECL | *One, Two, Four Outputs: 62.5, 74.5, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625 MHz LVDS, LVPECL, or LVCMOS (LVCMOS < 250 MHz)* | Six LVCMOS/LVTTL Outputs: Up to 167 MHz (CDCE906), Up to 300 MHz (CDCE706) | 3, 5, 7, or 9 LVCMOS Outputs: Up to 230 MHz | LVCMOS 8MHz – 110 MHz (clock multiplier pin selectable between 1X and 4X) |
| **Jitter**[2] | < 1 ps RMS < 40ps pk-pk | *< 1 ps RMS ~25 ps pk-pk* | 60 ps pk-pk | 60 ps pk-pk | 60 ps pk-pk |
| **Configuration** | Serial Interface | *Configuration Pins* | SMBus | SMBus | *Configuration Pins* |
| **Power**[3] | 360 mW | *360 mW* | 300 mW | 50 mW | 30 mW |
| **Special Features** | Low Jitter, EEPROM | *Very Low Jitter* | EEPROM, SSC | Low Power, EEPROM, SSC | SSC (Spread Spectrum) |
| **Typical Applications** | *XO Replacement, General Clocking* | *XO Replacement, Communications &, Network Clocking* | *Audio, Video, General Clocking* | *DSP Clocking, Portable Systems, General Clocking* | *Consumer, Portable Systems Industrial* |
| **Availability** | NOW | *NOW* | *NOW* | *NOW* | *NOW* |

[1]Unless otherwise noted, frequencies are listed in MHz.
[2]RMS Jitter calculated over an integration bandwidth of 10 kHz to 20 MHz.
[3]Typical configuration, fewest number of outputs enabled.

Texas Instruments

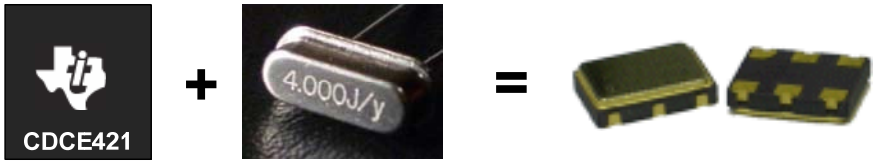
# CDCE421A

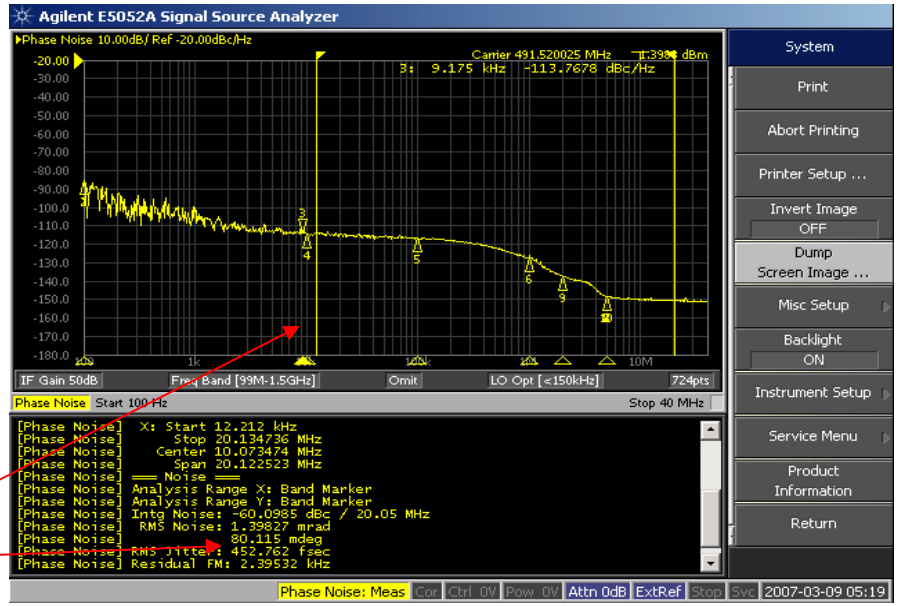
## *Programmable Low Noise Clock Synthesizer*




- Output Frequency from 10.9MHz up to 1175MHz
- Accepts 27.35MHz to 38.33MHz input crystal and LVCMOS input
- Integrated loop filter
- Low jitter design (< 1ps RMS) 10K – 20MHz,

  < 40ps, pk-pk period jitter
- LVDS or LVPECL selectable output
- ~2x~2mm die size, 4x4mm QFN Package
- On-chip EEPROM
- Power 360 mW for LVPECL




453 fs
10k-20M

# CDCM61001/2/4

## *Pin Programmable Clock Generator Family*


### Features

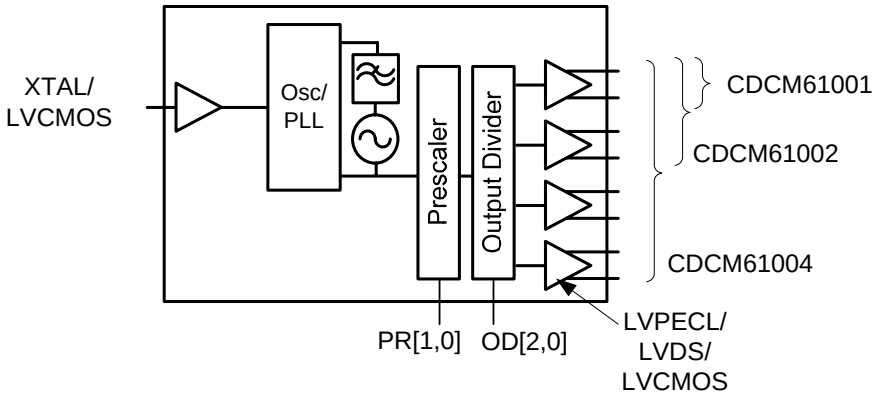
- Allowable crystal/LVCMOS input frequencies include25MHz, 26.5625MHz and 24.8832MHz
- Allowable LVPECL/LVDS output frequencies include 62.5MHz, 74.25MHz, 75MHz, 100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 212.5MHz, 250MHz, 311.04MHz, 312.5MHz, 622.08MHz, 625MHz; LVCMOS output frequency up to 250MHz
- Output divider selectable by /1, /2, /3, /4, /6, /8
- Prescaler divider selectable by /3, /4, /5
- Feedback divider selectable by /20, /24, /25, /15
- Integrated PLL Loop Filter of 400kHz
- Low jitter (< 1ps RMS, 10k-20MHz), ~ 25ps, pk-pk

### Applications

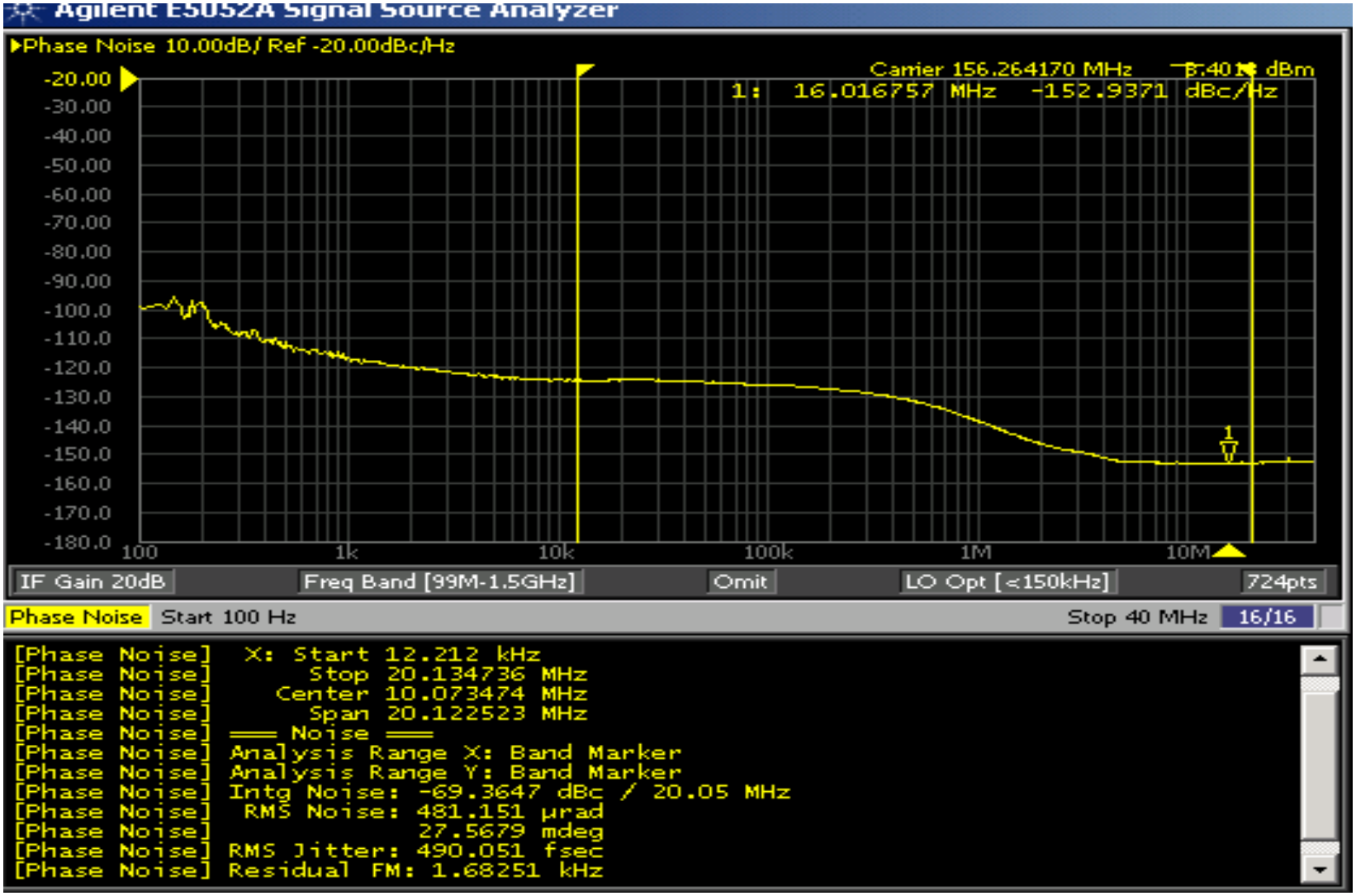
- Router/Switch
- Datacom/Telecom
- Wireless Infrastructure
- Medical
- Networking
- General Purpose Differential clock buffering

### Benefits

- Fully Integrated single VCO support Data Com/Networking Clocking Frequencies
- Integrated loop filter provides best jitter performance for crystal/clean input
- Configuration changes through control pins eliminate software programming cycle in production
- Each output selectable between LVPECL, LVDS and 2-LVCMOS
- QFN-20 5mm x 5mm package, Tem -40 to 85 C



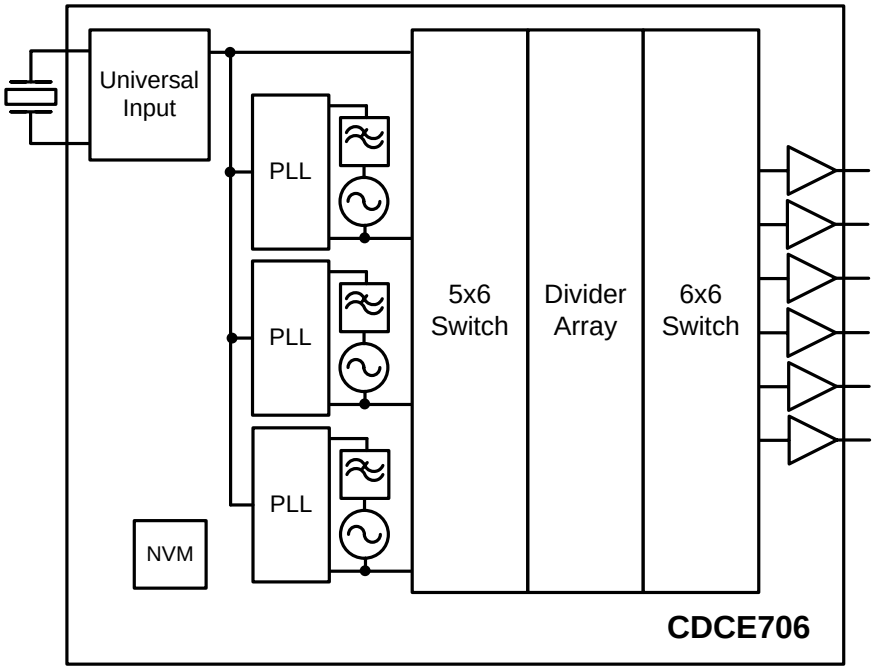
# Phase Noise Performance of CDCM6100x



# CDCE706/906

## *Six Output Flexible Clock Synthesizer*

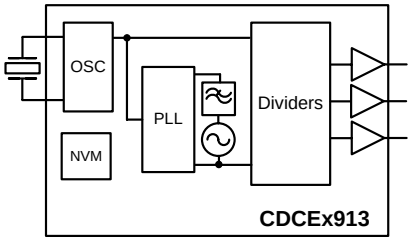
- Universal Input:
  - SE, Diff, or Crystal (8-54 MHz)
- Low Noise Fractional PLLs
  - Period Jitter 60 ps typ
  - SSC (one PLL)
- Highly Flexible Clock Driver:
  - Output frequencies up to 300 MHz
  - Programmable Slew Rate Control
  - Innovative crosspoint / divider array for maximum flexibility
- SMBus Interface
  - In System Programmability
- On-Chip EEPROM stores customer defined default settings

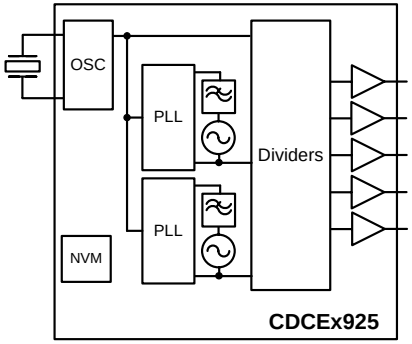


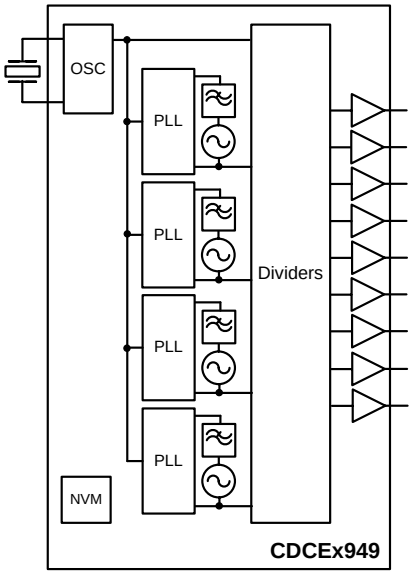
# CDCE9xx

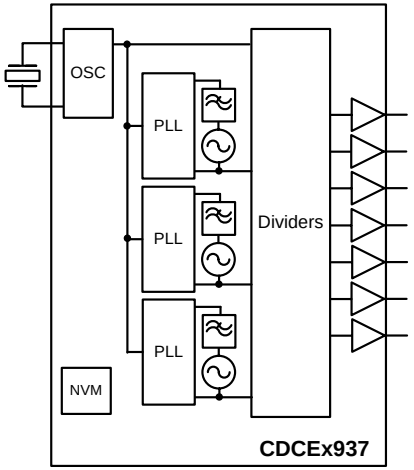
## *Flexible Clock Synthesizer Family*

- Flexible Input Clocking
  - External XTAL, On Chip VCXO, Single Ended LVCMOS up to 160 MHz
- LVCMOS Outputs support frequencies up to 230 MHz
- Low Noise Fractional PLLs
  - Period Jitter 60 ps typ
  - Spread Spectrum Clocking
- Highly Flexible Clock Driver:
  - Output frequencies up to 230 MHz
  - 2.5V and 3.3V (CDCE9xx)
  - 1.8V (CDCEL9xx)
- SMBus Interface
  - In System Programmability
- On-Chip EEPROM stores customer defined default settings

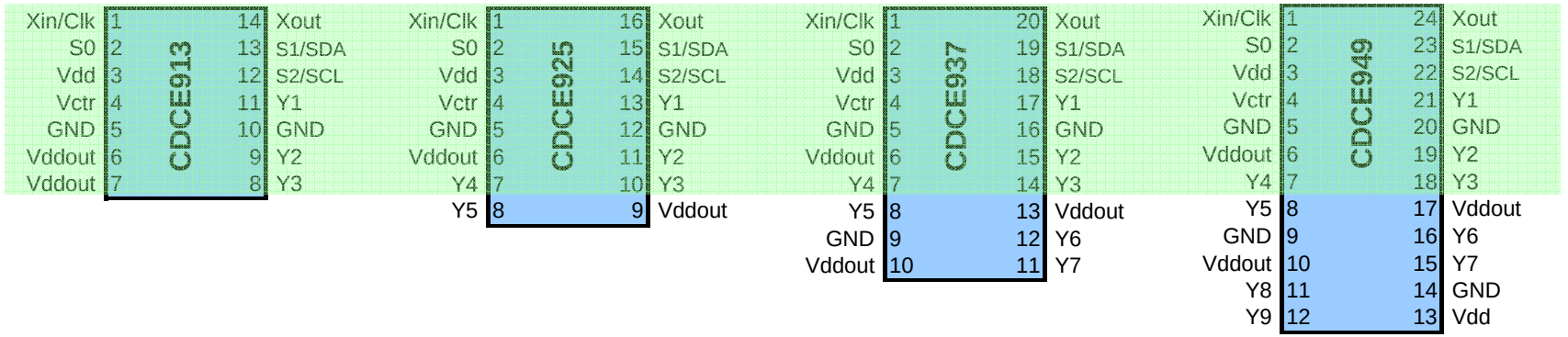


# Modular Design and Pin-Out Concept



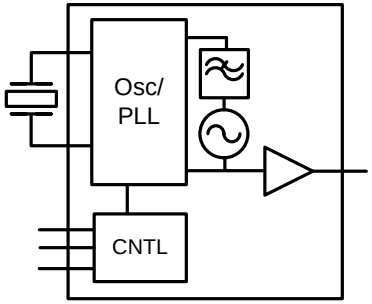

**Easy and Quick Upgrade**

# CDCS502

## *Spread Spectrum Clock Multiplier*

- **Features**
  - •Generates a spread spectrum clock for output frequencies ranging from 8 MHz to 110 MHz derived from a crystal input.
  - •Spread spectrum setting controlled via 2 pins.
  - •Frequency multiplication selectable between X1 or X4 via control pin
  - •Single 3.3V Device Power Supply
  - •Wide operating temperature range (-40 - + 85 $^{o}$C)
  - •Offered in 8 pin TSSOP Package

- **Benefits**
  - •Reduces EMI
  - •Selectable SSC modulation
  - •Very small board space required.

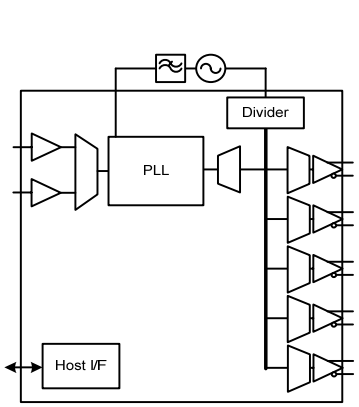


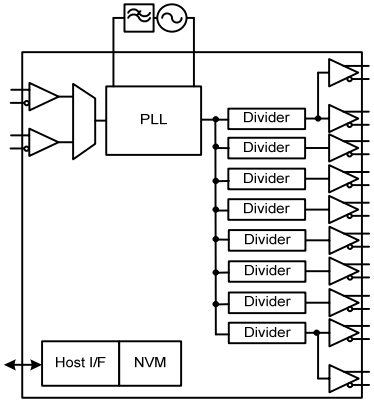

- **Applications**
  - •Consumer Audio and Video Systems
  - •Computer Peripherals
  - •Industrial

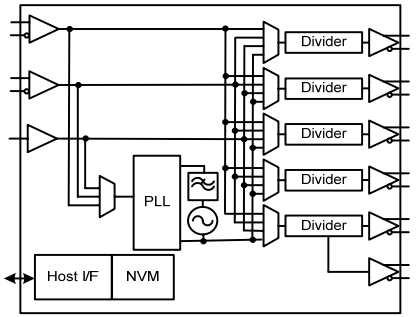
| FS | SSC_SEL0 | SSC_SEL1 | SSC Amount | Fout/Fin |
|---|---|---|---|---|
| 0 | 0 | 0 | 0.00% | 1 |
| 0 | 0 | 1 | 0.50% | 1 |
| 0 | 1 | 0 | 1.00% | 1 |
| 0 | 1 | 1 | 2.00% | 1 |
| 1 | 0 | 0 | 0.00% | 4 |
| 1 | 0 | 1 | 0.50% | 4 |
| 1 | 1 | 0 | 1.00% | 4 |
| 1 | 1 | 1 | 2.00% | 4 |

1Ku / $0.95

# Jitter Cleaner Portfolio



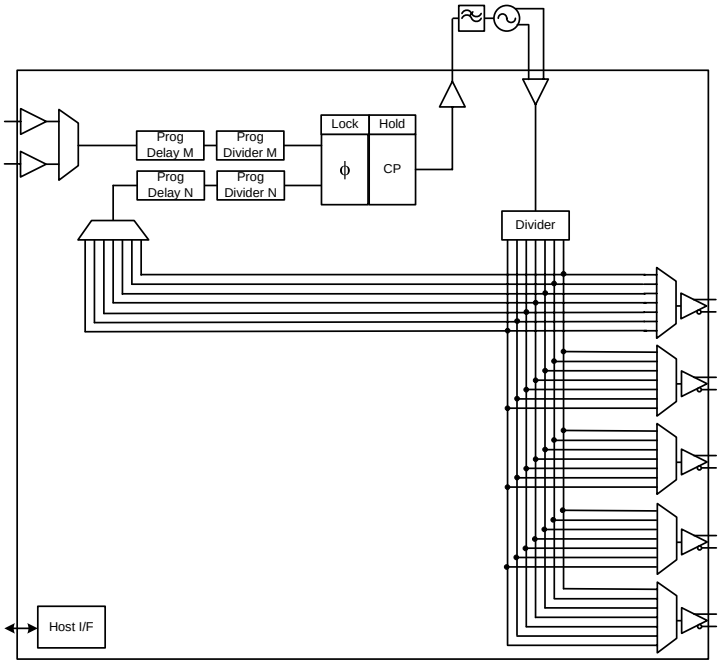

| Product | *CDCM7005* | *CDCE72010* | CDCE62005/CDCE62002 |
|---|---|---|---|
| **Input** | Two LVCMOS:<br>up to 200 MHz | Two Differential<br>(LVPECL, LVDS) up to<br>500 MHz; Single ended<br>up to 200 MHz | Two Universal: LVPECL (1500 MHz),<br>LVDS (800 MHz), LVCMOS (250 MHz)<br>One Auxiliary:<br>LVCMOS (75 MHz) or XTAL (2-42 MHz) |
| **Output**[1] | Five LVPECL (1500 MHz) or<br>Ten LVCMOS (250 MHz)<br>Outputs share common<br>divider providing /1-/16<br>inclusive | Ten Universal Outputs:<br>LVPECL (1500 MHz)<br>LVDS (800 MHz)<br>LVCMOS (250 MHz)<br>Eight dedicated dividers (/1 - /80) | Five Universal Outputs (CDCE62005), Two<br>Universal Outputs (CDCE62002):<br>LVPECL (1500 MHz)<br>LVDS (800 MHz)<br>LVCMOS (250 MHz)<br>Five/Two dedicated dividers (/1 - /80) |
| **PLL** | Integer | Integer | Integer |
| **VCO/VCXO** | External | External | Internal |
| **Jitter**[2] | < 200 fs | < 200 fs | < 1 ps |
| **Power**[3] | 1,000 mW | 2,000 mW | 1,700 mW/1,100 mW |
| **Special Features** | SPI Interface, Skew<br>Control via PLL | SPI Interface, EEPROM,<br>Smark Input Multiplexer<br>Skew Control via Dividers | SPI Interface, EEPROM,<br>Smark Input Multiplexer<br>Skew Control via Dividers |
| **Applications** | High Performance ADC<br>clocking, high speed serial<br>links, general clocking | High Performance ADC<br>clocking, high speed serial<br>links, general clocking | High Performance ADC<br>clocking, high speed serial<br>links, general clocking |
| **Availability** | NOW | NOW | NOW |

[1]Unless otherwise noted, frequencies are listed in MHz.
[2]RMS Jitter calculated over an integration bandwidth of 10 kHz to 20 MHz. Jitter performance of devices employing an external VCO/VCXO is greatly influenced by phase noise of external VCO/VCXO.
[3]Typical configuration. Vdd = 3.3V.

Texas Instruments

# CDCM7005

- Clock Generator, Jitter Cleaner Modes
- Integrated PLL
  - External VCO/VCXO and loop filter
  - Holdover Mode Supported
- Dual LVCMOS reference inputs support manual or automatic switchover.
  - Up to 200 MHz
- VCO/VCXO input port supports up to 2200 MHz.
- 5 LVPECL / 10 LVCMOS Outputs
  - Programmable output format per output
  - LVPECL up to 1500 MHz, LVCMOS up to 250 MHz.
  - Programmable phase offset between reference inputs and outputs.
  - Divider values include: /1, /2, /3, /4, /6, /8, and /16.
- Very low output jitter (< 200 fs)
- Offered in a 64 BGA or QFN48.
- Fully programmable via SPI port.



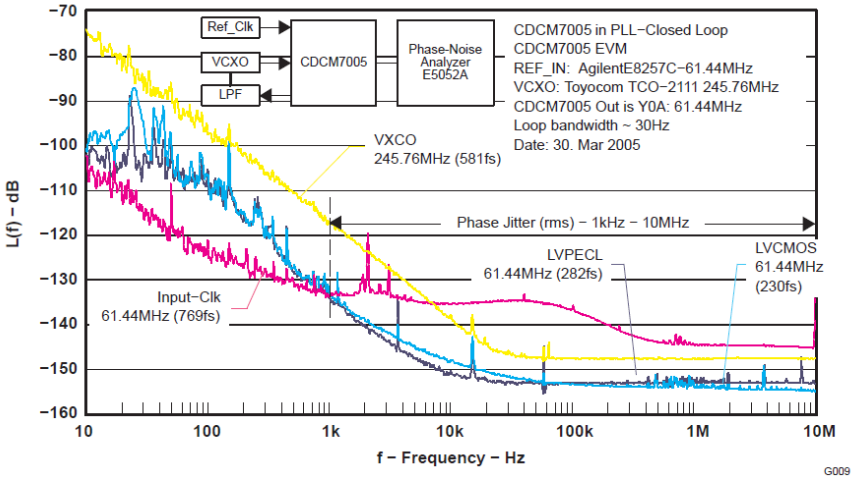
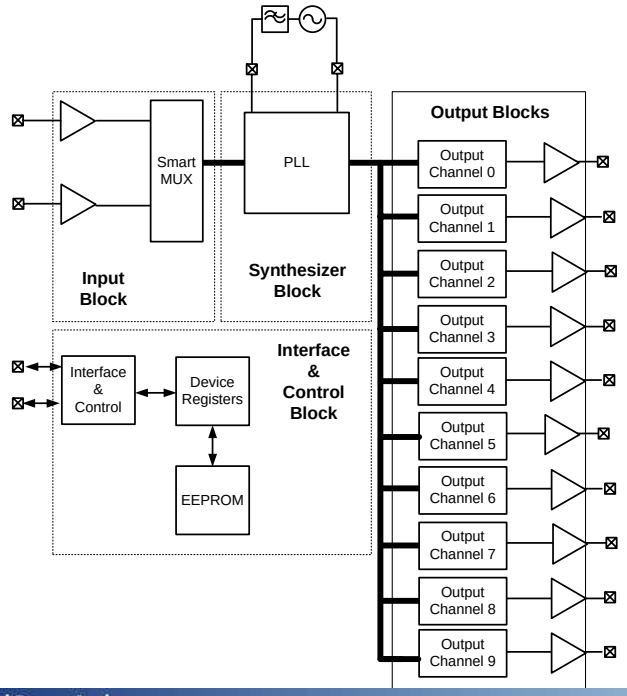
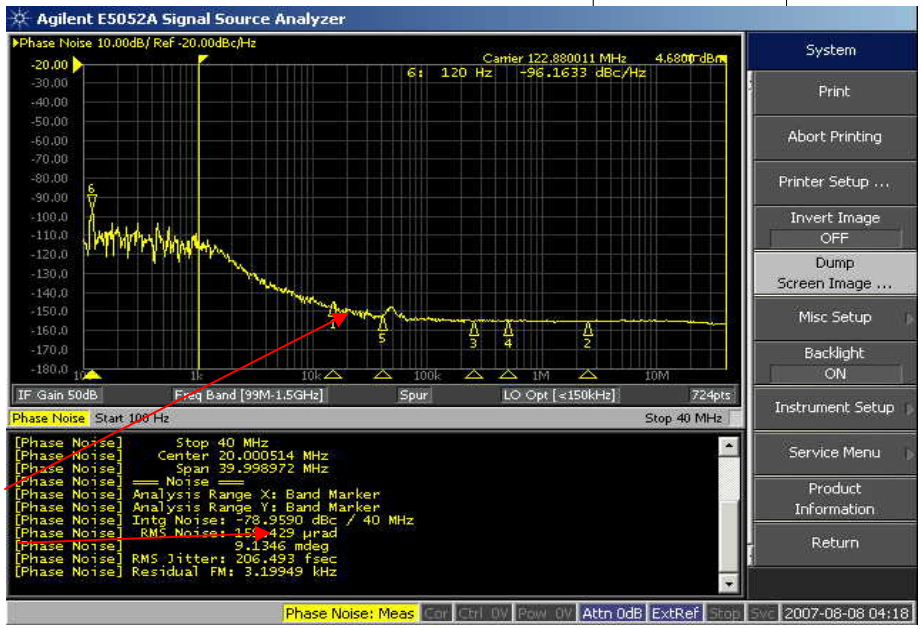




**Figure 25. Phase Noise (61.44-MHz REF_IN and 61.44-MHz Output Frequency)**

# CDCE72010

- Clock Generator, Jitter Cleaner Modes
- Integrated PLL
  - External VCO/VCXO and loop filter
  - Holdover Mode Supported
- Two Universal Inputs
  - Differential Mode (LVPECL,LVDS) up to 1500 MHz
  - Single Ended up to 250 MHz
  - Smart Multiplexer - Automatically switches between inputs
- 10/20 Configurable Outputs (10 differential, 20 single-ended)
  - LVPECL mode up to 1500 MHz, LVDS mode up to 800 MHz, LVCMOS mode up to 250 MHz.
  - Adjustable Skew
  - Dedicated Divide Ratio per Channel (/1 - /80) – 8 Channels
- < 50 fs Residual Jitter (distribution section)
  - 200 fs RMS Jitter with good VCO
- On-chip EEPROM determines default state at power up
- Offered in a 64 pin PQFP
- Fully programmable via SPI port.

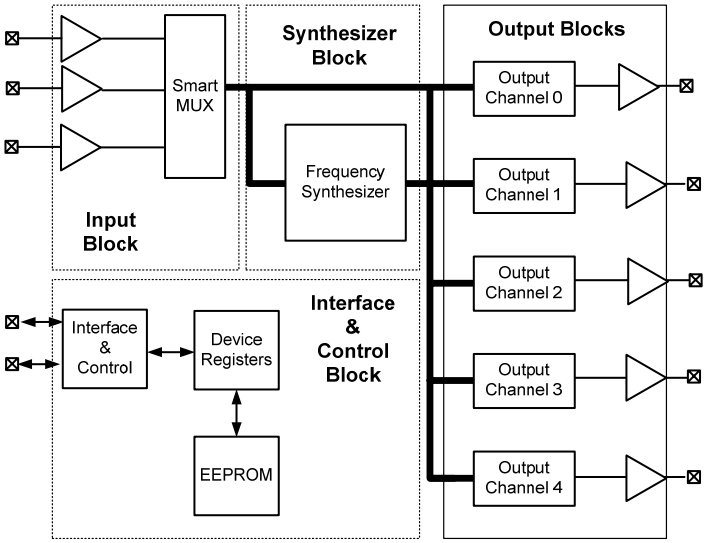


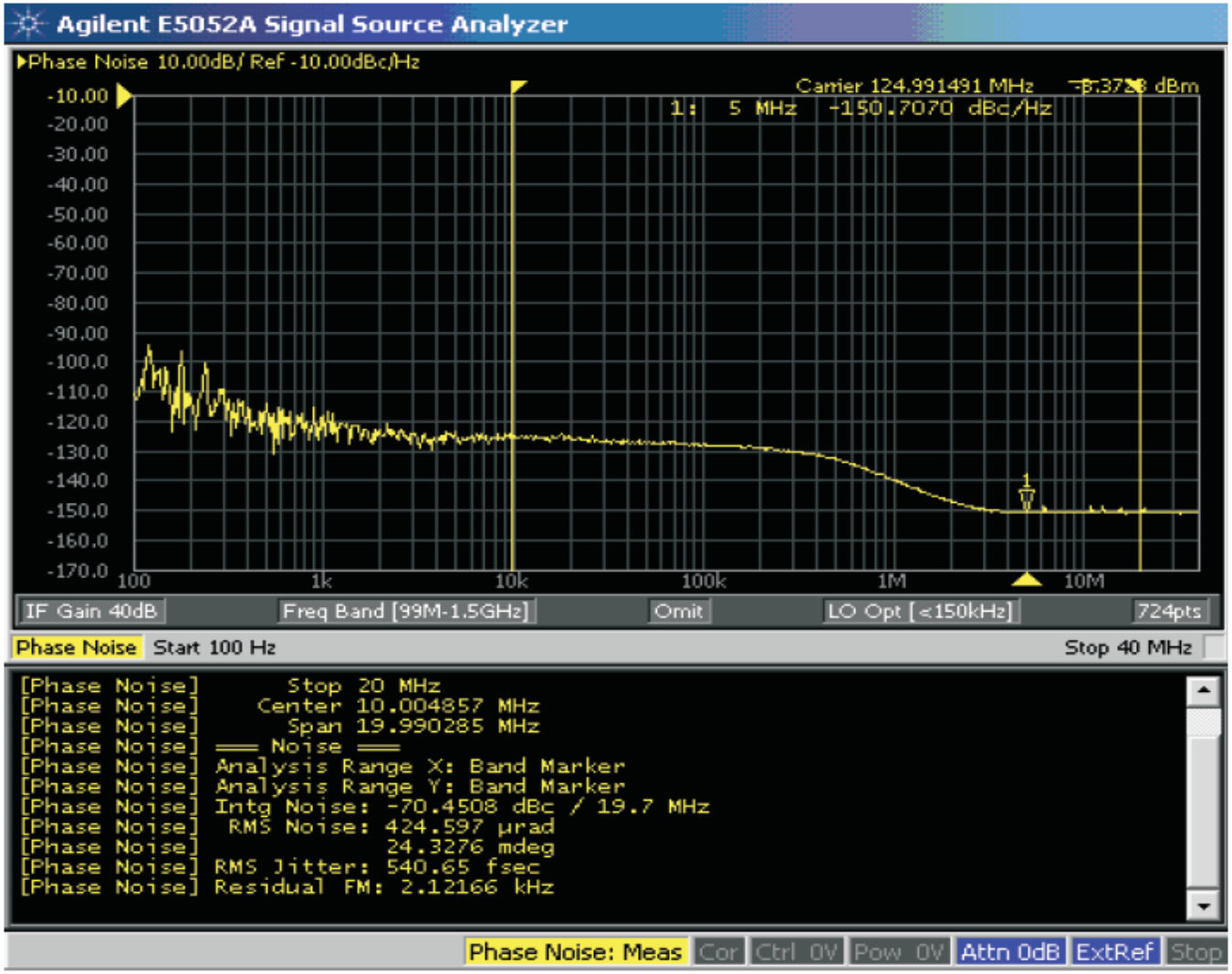

206 fs
1k-40M

# CDCE62005 (1)

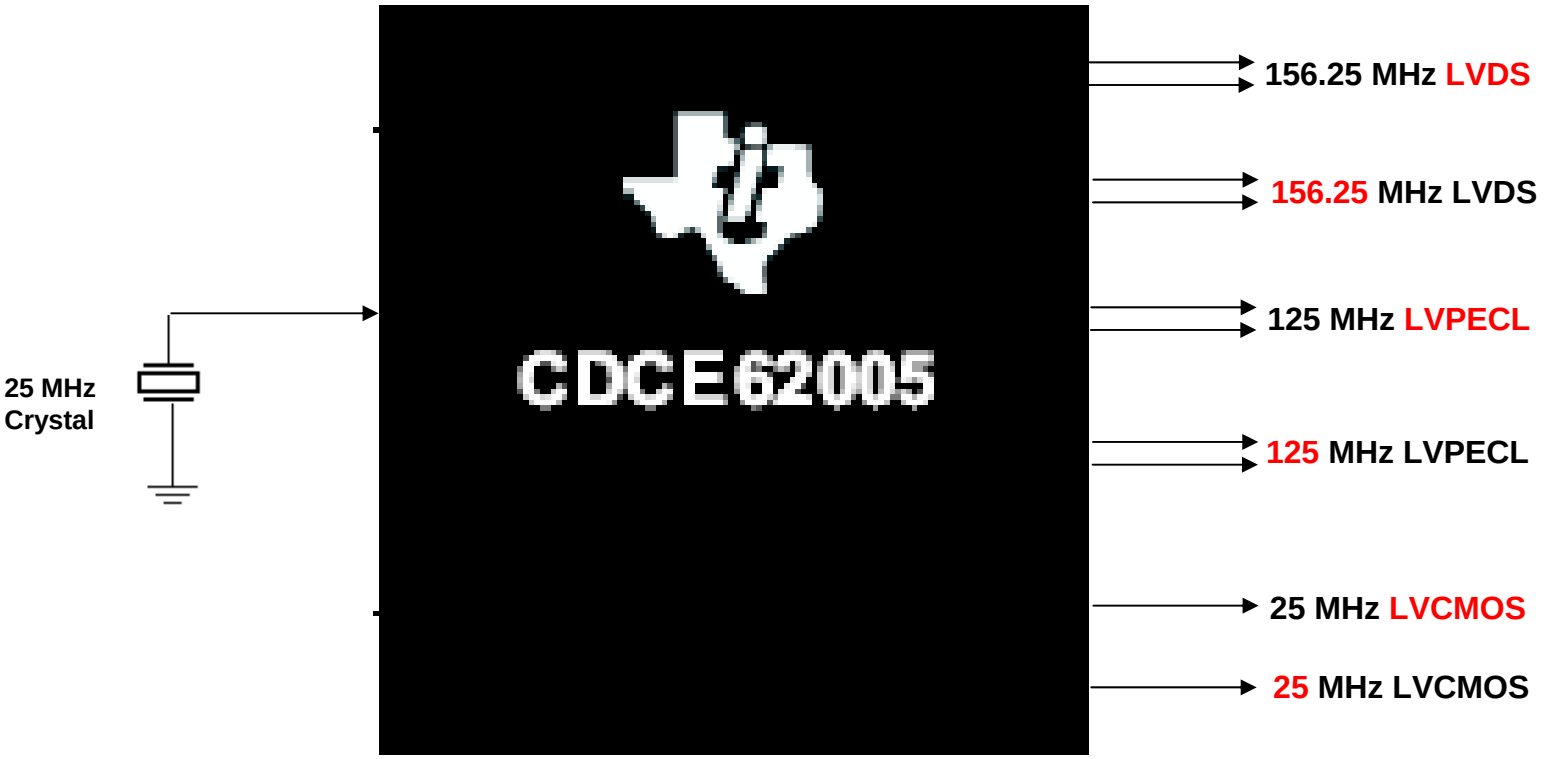
- Clock Generator, Jitter Cleaner, and Fan-out Buffer Operational Modes
- Fully integrated synthesizer including PLL, VCO, and partially integrated loop filter
  - Jitter Performance < 1 ps RMS (12kHz – 20MHz)
- Two Universal Inputs, One Auxiliary Input
  - Differential or Single Ended Modes: LVPECL (up to 1500 MHz), LVDS (up to 800 MHz), LVCMOS (up to 250 MHz)
  - One Auxiliary Input accepts single ended signal up to 75 MHz or a crystal (2 MHz – 42 MHz)
  - Use of XTAL on Auxiliary port enables holdover and SERDES startup modes.
  - Smart Multiplexer - Automatically switches between inputs
- 5/10 Outputs (5 differential, 10 single-ended)
  - LVPECL Mode up to 1500 MHz, LVDS mode up to 800 MHz, LVCMOS mode up to 250 MHz
  - Adjustable Skew
  - Dedicated Divide Ratio per Channel
- On-chip EEPROM determines default state at power up
- Offered in a QFN-48 package.
- Fully programmable via SPI port.



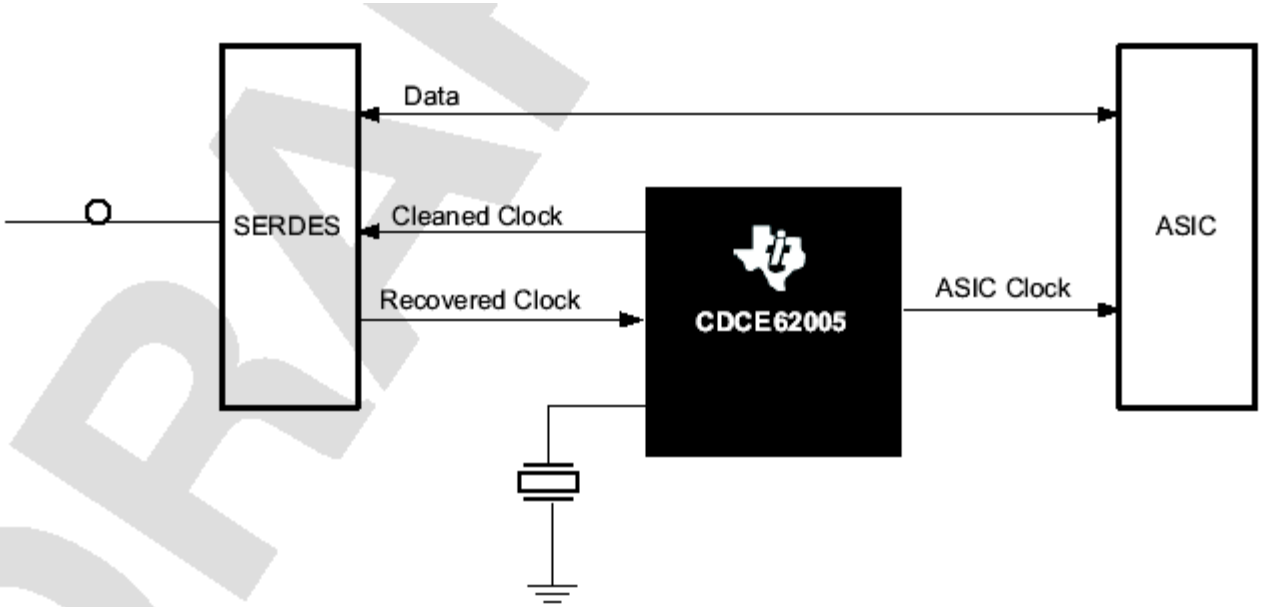
# Phase Noise Performance of CDCE62005



# Application Example: Frequency Generation



# Application Example: Jitter Cleaning



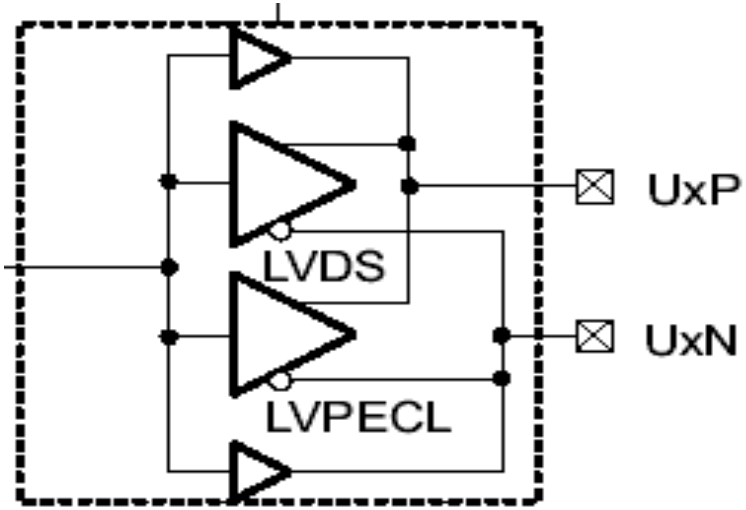
# Value Proposition

- Internal VCO and flexible loop filter options provide high level of integration
- Low jitter frequency multiplication from low frequency crystal or system clock
- High jitter cleaning ability of dirty system clock
- On-chip EEPROM allows for stable clock at start-up without programming
- External crystal provides holdover functionality
- Option of external loop filter
- Output MUXs allows simultaneous device operation in bypass mode and PLL mode
- Smart PLL Input MUX provides automatic reference switch-over

# CDCE62005

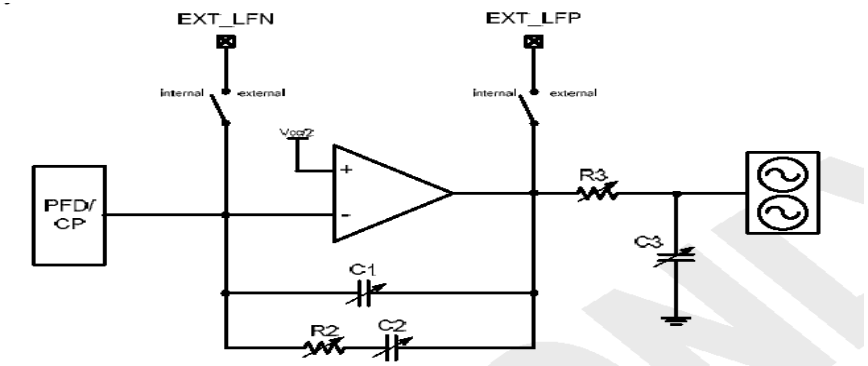
## Output Options

- CDCE62005 supports 5 pairs of mixed outputs, 5 LVPECL, 5 LVDS or 10 LVCMOS/LVTTL or any combination of these.
- The single-ended LVCMOS outputs are arranged in pairs, so each pair has the same function, i.e. same frequency and also 180 deg out of phase relationship
- The outputs can be switch on (active) or off (3-State or Low) and support a coarse phase adjustment whose granularity depends on the output divider



# CDCE62005
## Loop Filter Options

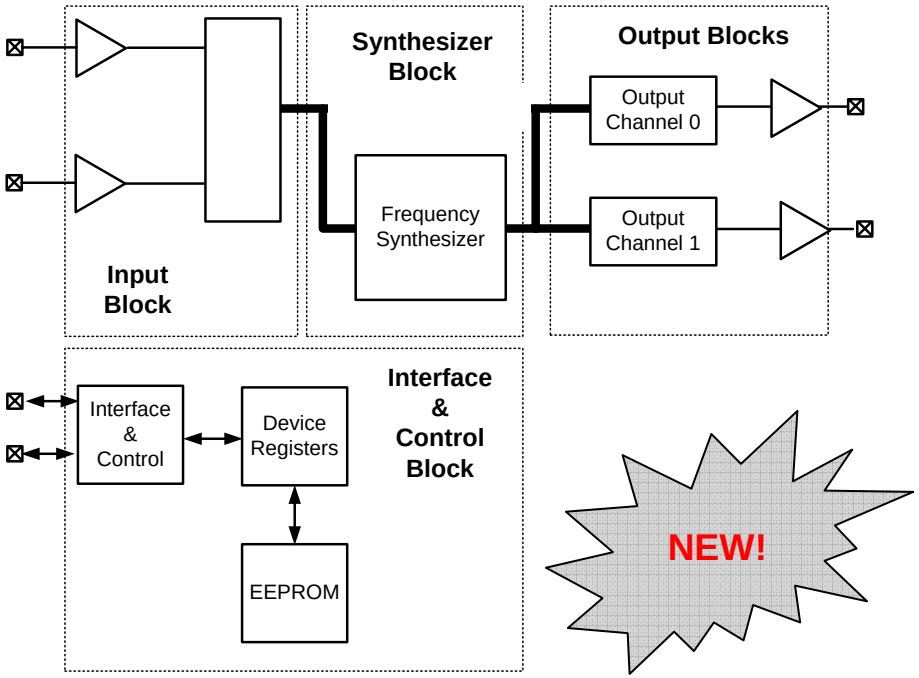
- CDCE62005's loop filter can be set as
  - Fully internal (50 kHz to 400 kHz)
  - Combination of internal and external (< 50 kHz)
- CDCE62005's PFD frequencies can be set as
  - 40 kHz to 40 MHz
- CDCE62005 supports charge pump current settings of 50 uA to 3.75 mA
- Rules of thumb for the PLL settings are
  - For a given PFD frequency, the necessary loop filter bandwidth is < (PFD/10) kHz
  - As loop filter bandwidth lowers, charge pump current should be increased for improved loop stability




**CDCE62005 PLL loop filter**

# CDCE62002

- Clock Generator, Jitter Cleaner, and Fan-out Buffer Operational Modes
- Fully integrated synthesizer including PLL, VCO, and partially integrated loop filter
  - Jitter Performance < 1 ps RMS (12kHz – 20MHz)
- One Universal Inputs, One Auxiliary Input
  - Differential or Single Ended Modes: LVPECL (up to 1500 MHz), LVDS (up to 800 MHz), LVCMOS (up to 250 MHz)
  - One Auxiliary Input accepts single ended signal up to 75 MHz or a crystal (2 MHz – 42 MHz)
  - Use of XTAL on Auxiliary port enables holdover and SERDES startup modes.
  - Smart Multiplexer - Automatically switches between inputs
- 2/4 Outputs (2 differential, 4 single-ended)
  - LVPECL Mode up to 1500 MHz, LVDS mode up to 800 MHz, LVCMOS mode up to 250 MHz
  - Adjustable Skew
  - Dedicated Divide Ratio per Channel
- On-chip EEPROM determines default state at power up
- Offered in a 32 pin PQFP.
- Fully programmable via SPI port.



# THANK YOU!

**www.ti.com**