The flexible dynamics of power management in multimedia processors

Arthur Musah

October 7, 2008

Texas Instruments

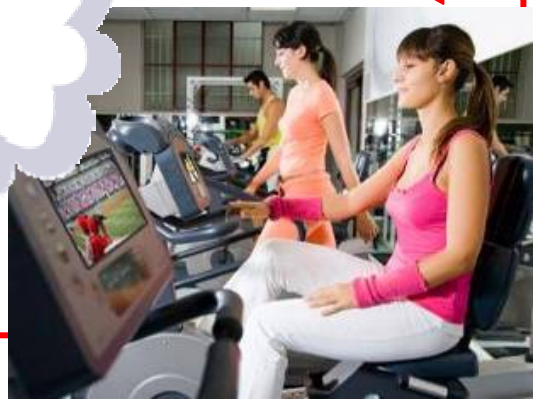
Outline

- The need for low power devices
- Texas Instruments SmartReflex™ technology power management in OMAP35x processors
- Realizing power savings

Drive for smarter devices reaches across product categories to improve effectiveness

Simultaneous:

Advanced user interfaces
Enhanced productivity
Full web browsing
Multimedia
Green
Connectivity



Multimedia device trends impact power

1) Convergence of communications, computing and entertainment	More transistors and migration to smaller, leakier geometries
2) New applications and extended usage	Requires higher performance, power-hungry processing
3) Increasing on-chip memory for frame buffer and high-speed caches	Memory consumes more power than logic and must be retained
4) Users demand increased usage/standby times	Battery technology not keeping up with power needs, need other methods to meet expectations
5) Smaller, sleeker devices	Size limits battery capacity; more aggressive thermal requirements

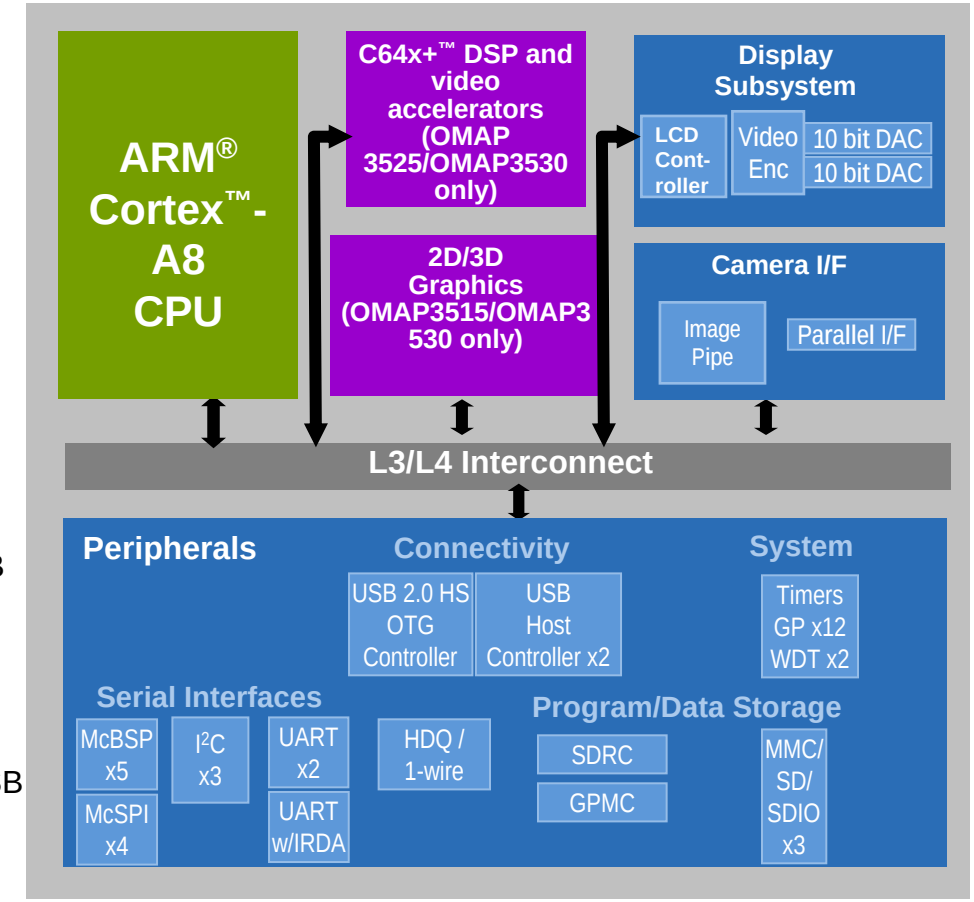
Outline

- The need for low power devices
- TI SmartReflex™ technology power management in OMAP35x processors
- Realizing power savings

TI OMAP35x applications processor based on ARM® Cortex™-A8

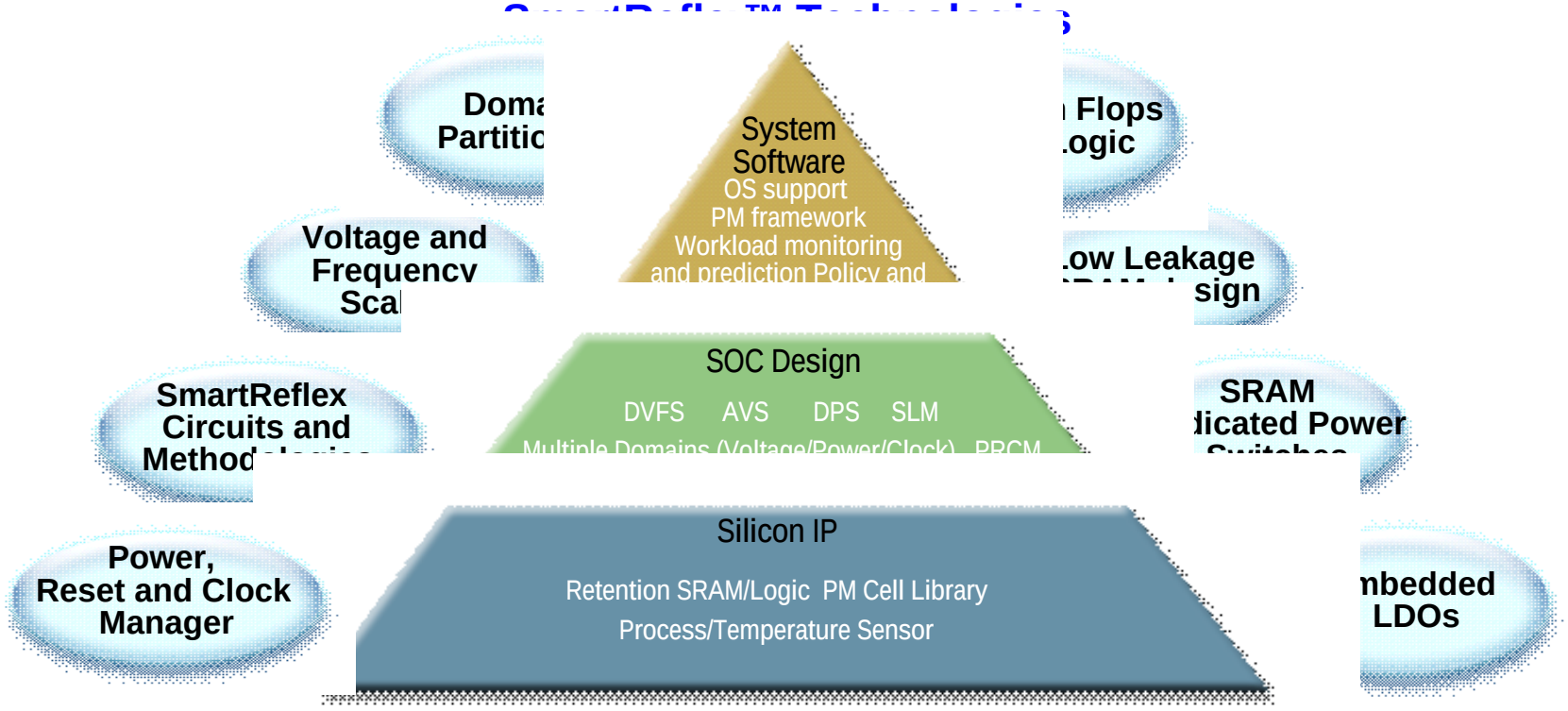
Features

- **Cores**
  - Cortex™-A8 with NEON™ SIMD coprocessor
  - TMS320C64x+™ DSP and video accelerators
    - 600 MHz / 430 MHz @ 1.35V
    - 550 MHz / 400 MHz @ 1.27V
    - 500 MHz / 360 MHz @ 1.2V
  - 2D/3D Graphics Engine (PowerVR SGX)
    - Up to 10M polygons per second
- **Memory**
  - ARM:
    - 16 KB I-Cache; 16 kB D-Cache; 256kB L2
  - TMS320C64x+ DSP and video accelerators
    - L1 32kB Program Cache/32kB Data Cache + 48kB SRAM
    - L2 64kB Program / Data Cache + 32 kB SRAM; 16 kB ROM
  - On chip: 64kB SRAM; 112kB ROM
- **Peripheral highlights**
  - Support for LPDDR
  - Support for NOR, NAND, SRAM, Pseudo SRAM
  - USB 2.0 HS compliant OTG Controller w/ 2 additional USB Host Controllers
  - Display subsystem with LCD and TV interface. Supports PIP, color space conversion, resize and rotation.
  - Camera I/F with CCD controller and Image-pipe (Preview, Resize, Statistics)



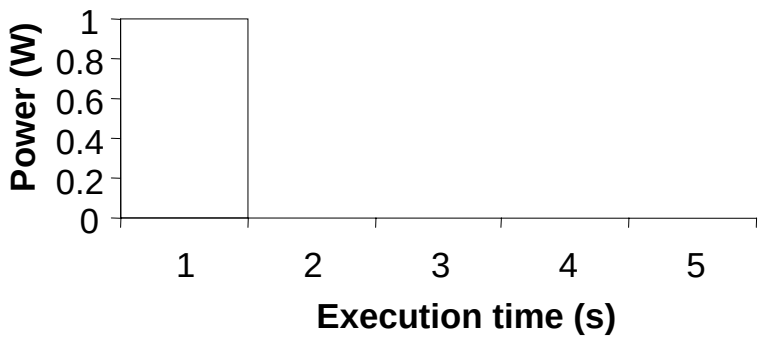
TI SmartReflex™ technology in OMAP35x processors address low power challenges

- Aggressive power management involving all system components - silicon technology , SoC design and software
- Reductions in both active *and* static power

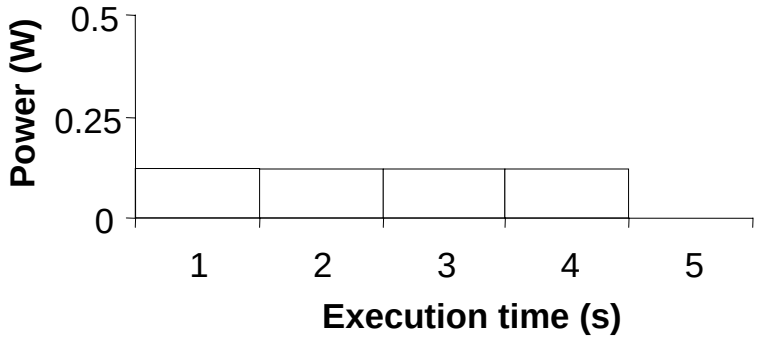


TI SmartReflex™ technology Dynamic Voltage and Frequency Scaling (DVFS)

Normalized power without DVFS (F,V)



Normalized power with DVFS (0.25F, 0.7V)



- **DVFS:**
  - It dynamically adjusts the device voltage and frequency to the minimum necessary to meet application performance requirements
  - It saves active power consumption (CV^2F) primarily

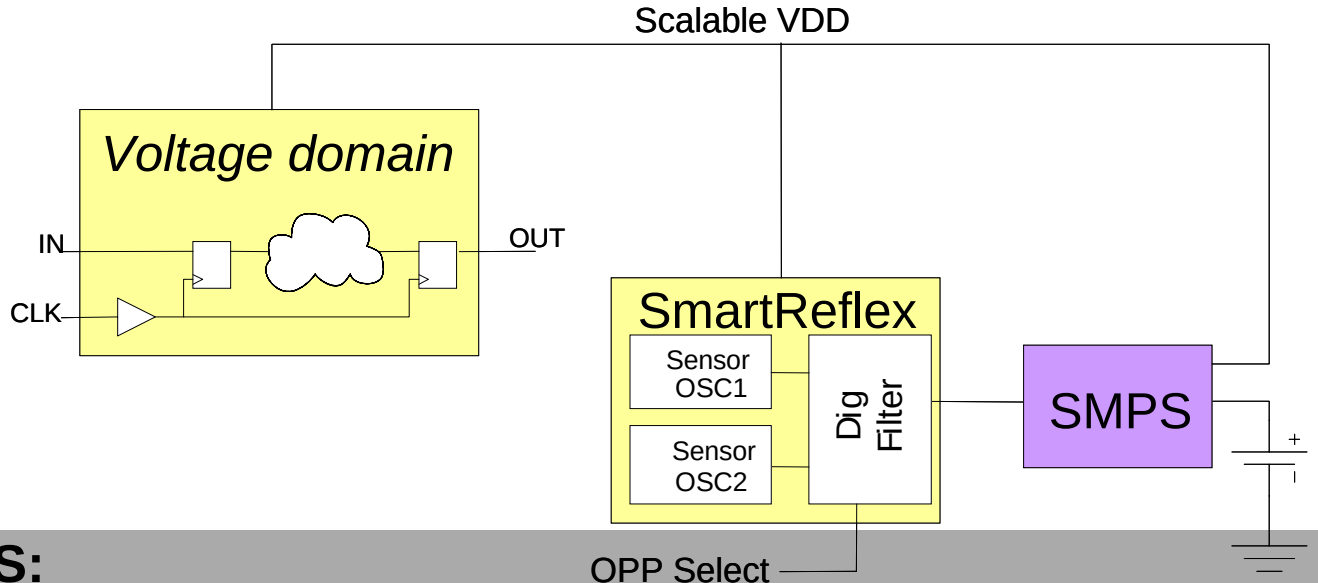
TI SmartReflex™ technology DVFS - 2

- Discrete Operating Performance Points (OPPs)
  - V,F pair - min voltage at which all devices can meet at most the specified frequency
- Applicable to two highest power-consuming voltage rails/domains:
  - VDD1 supplying the processor subsystems (ARM and DSP)
  - VDD2 supplying the peripherals and interconnects in OMAP35x
- Scaling separately allows flexibility
- Load prediction and transition management by software

	OPP	ARM® MHz	DSP MHz	Vdd1
OMAP 35x	5	600	430	1.35
	4	550	400	1.27
	3	500	360	1.2
	2	250	180	1
	1	125	90	0.95

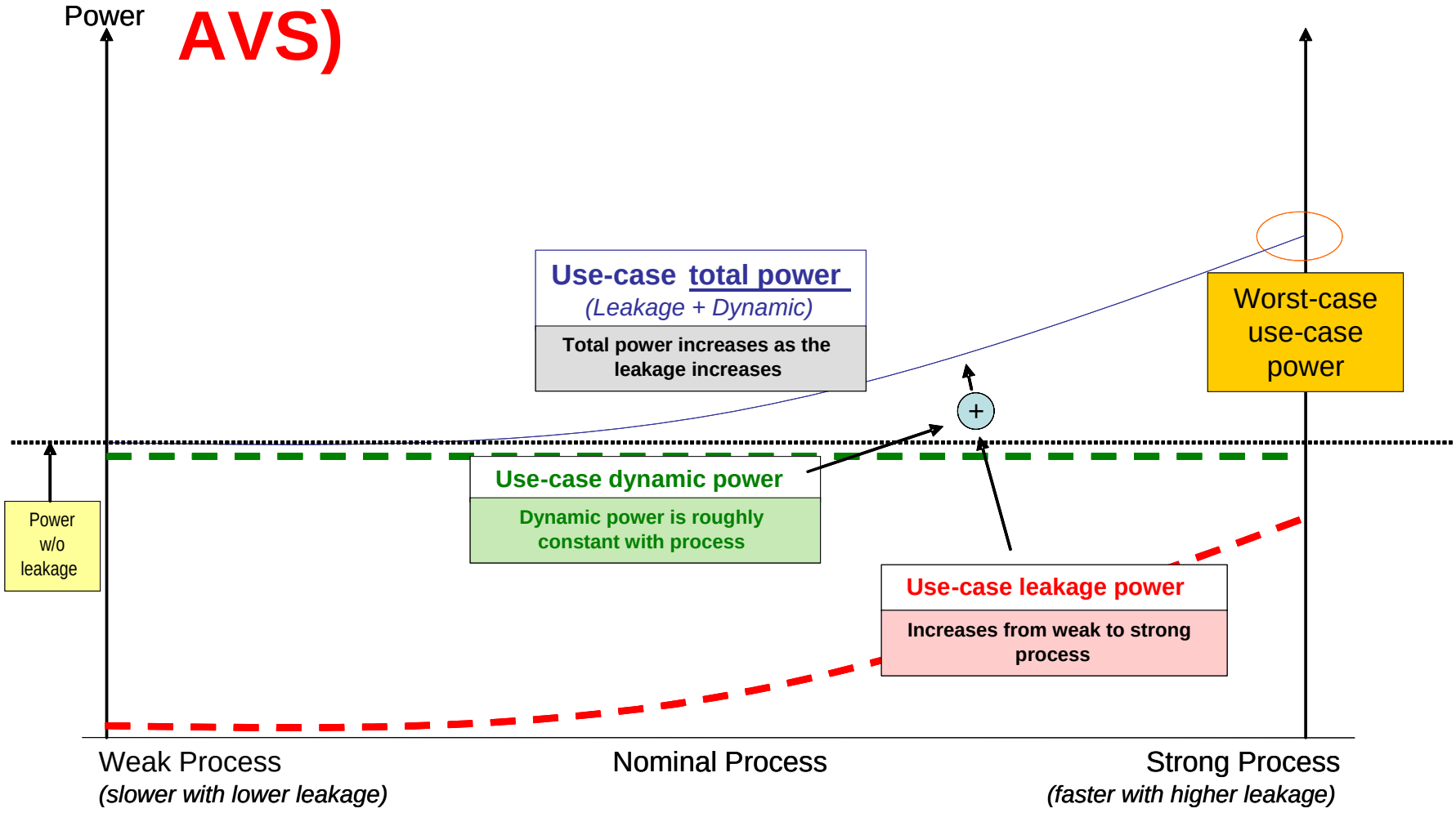
OPP	L3 MHz	Vdd2
3	166	1.15
2	100	1
1	41.5	0.95

TI SmartReflex™ technology
Adaptive Voltage Scaling (AVS)

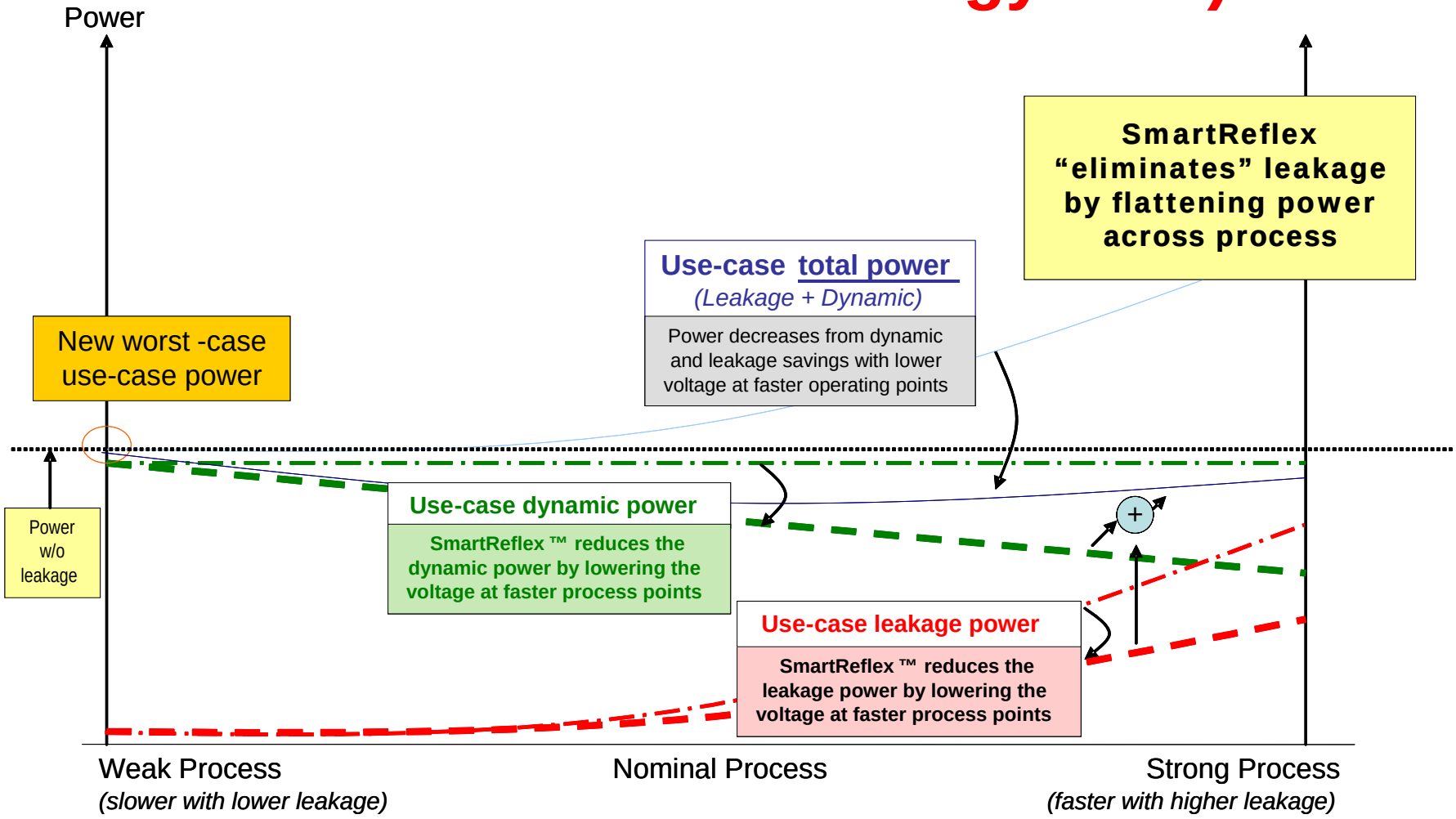


- **AVS:**
  - Vdd is adaptive and determined by performance of the silicon within the current environment
  - Gauges the performance of the silicon and ensures the design can maintain target performance while guaranteeing the **minimum required voltage** for a defined performance

Power vs. process (without SmartReflex™ technology AVS)



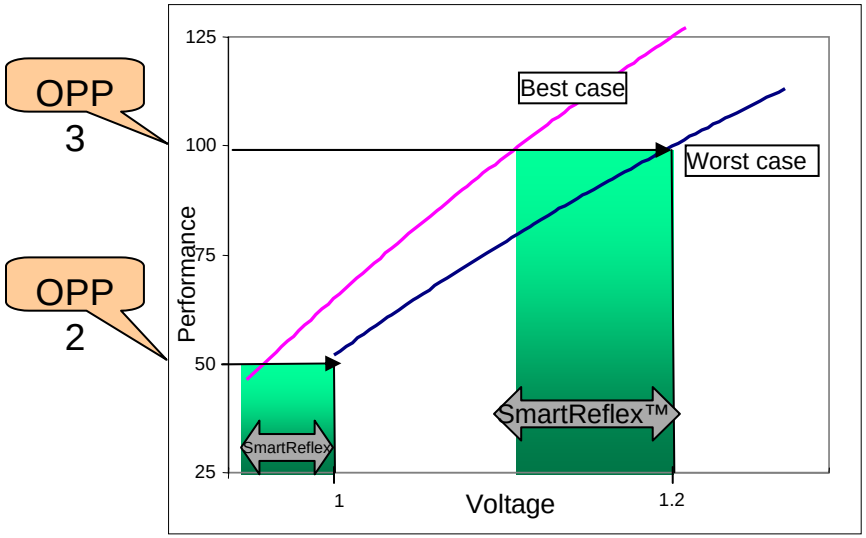
Power vs. processor (with TI SmartReflex™ technology AVS)



Dynamic Voltage Frequency Scaling (DVFS) vs. Adaptive Voltage Scaling (AVS)

DVFS

- Choose OPP based on frequency requirement in scenario
- Lower frequency requirement ➔ lower voltage
- All die treated the same



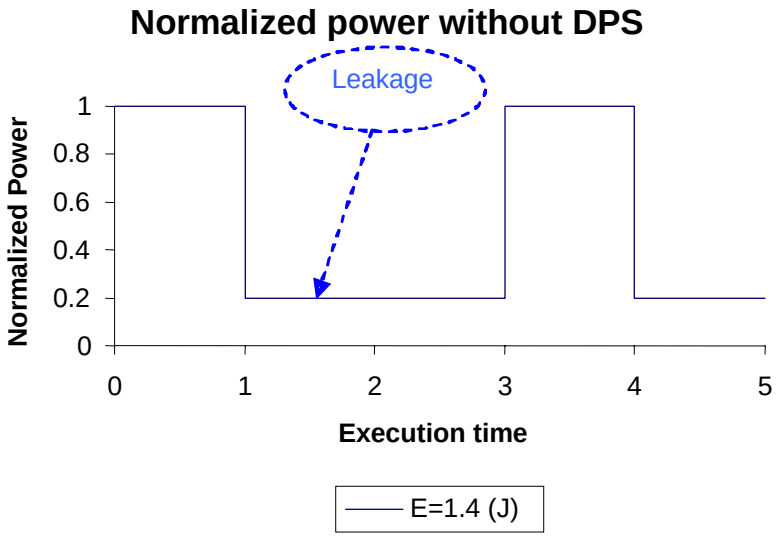
	OPP	ARM® MHz	Vdd1
OMAP 3503	5	600	1.35-1.12
	4	550	1.27-1.07
	3	500	1.2-1.00
	2	250	1.0-0.9
	1	125	0.95-0.8

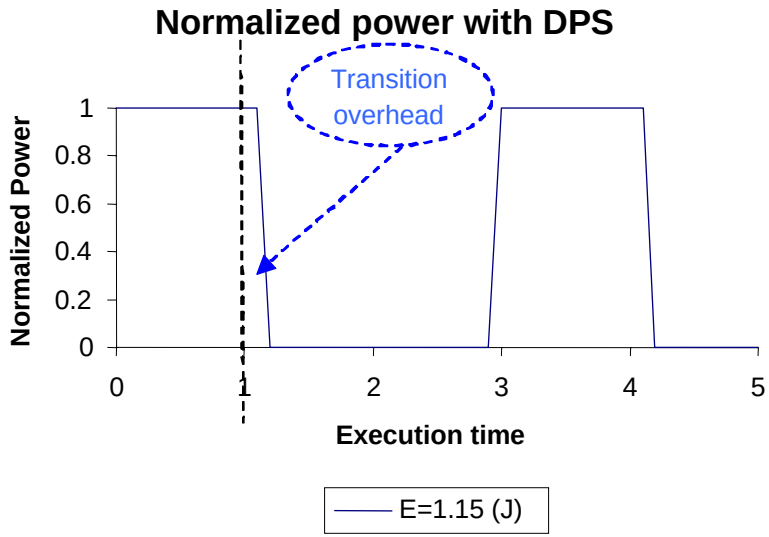
OPP	L3 MHz	Vdd2
3	166	1.15-0.95
2	100	1.0-0.85
1	41.5	0.95-0.8

AVS

- Scale selected OPP voltage based on device-specific properties (process, temperature)
- Stronger process ➔ lower voltage
- Each die treated differently

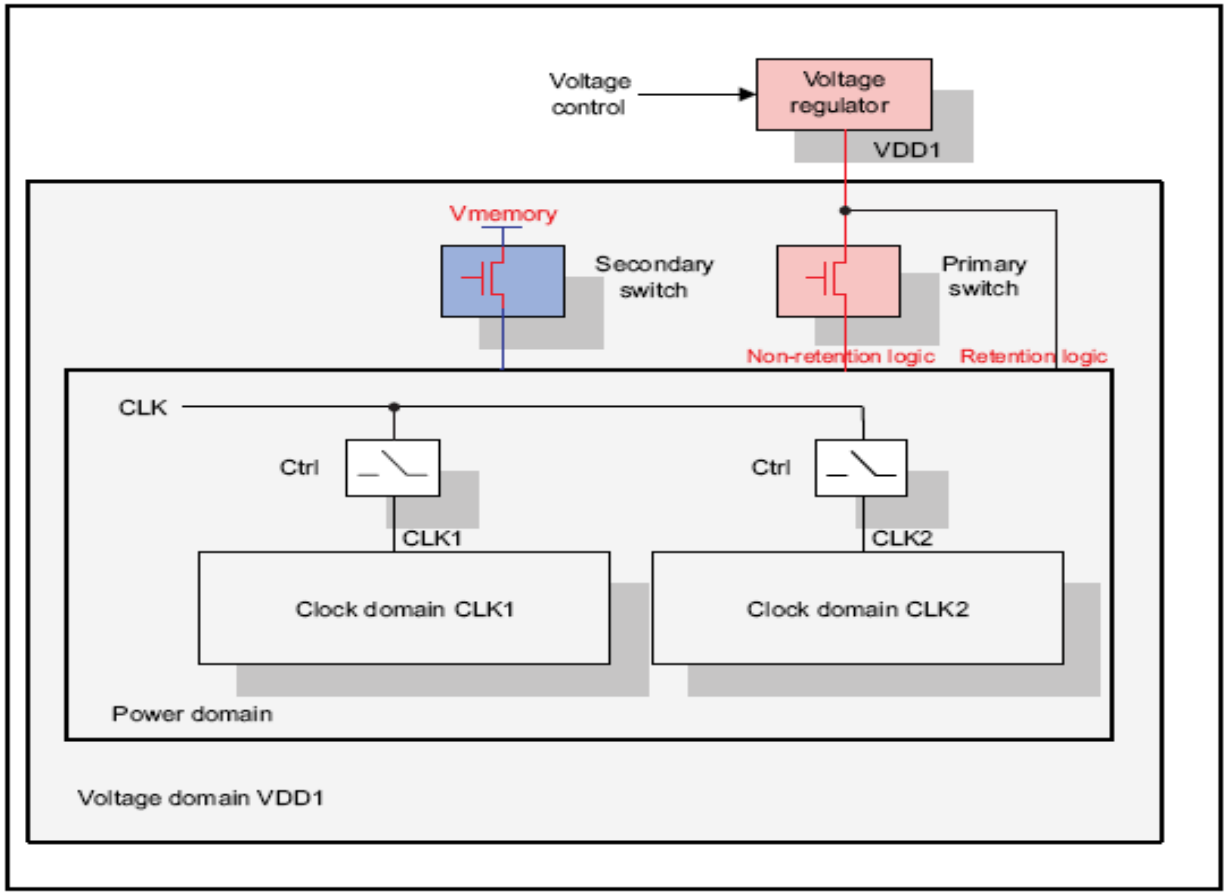
TI SmartReflex™ technology Dynamic Power Switching (DPS)





- **DPS:**
  - It dynamically switches the device between high and low consumption power modes. Processor or system always runs as fast as possible to complete its tasks and then switches to a retention or off state
  - It saves leakage power consumption

Hierarchy of domain partitioning



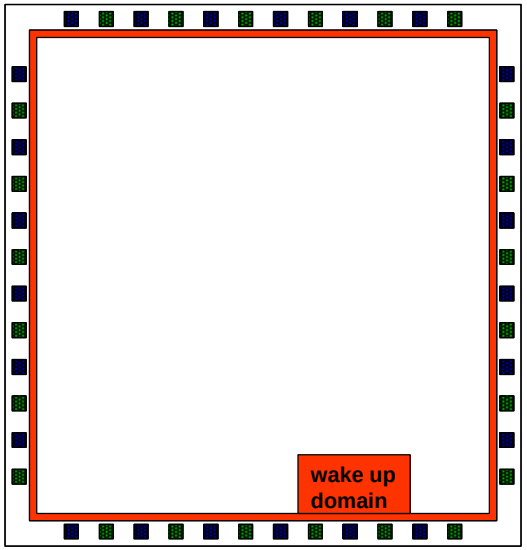
TI SmartReflex™ technology
Static Leakage Management (SLM)

- **SLM:**
  - Whole device automatically or under user request enters standby mode when no application is running
  - Several standby modes possible (combinations of Inactive/Retention/Off states of power domains)
  - Special device off mode in OMAP35x

DPS	SLM
Section of device in low power state	Entire device in low power mode
Some part of system active	Full system inactive
Smaller transition latencies (us)	Larger transition latencies (ms)

TI OMAP35x processor off-mode

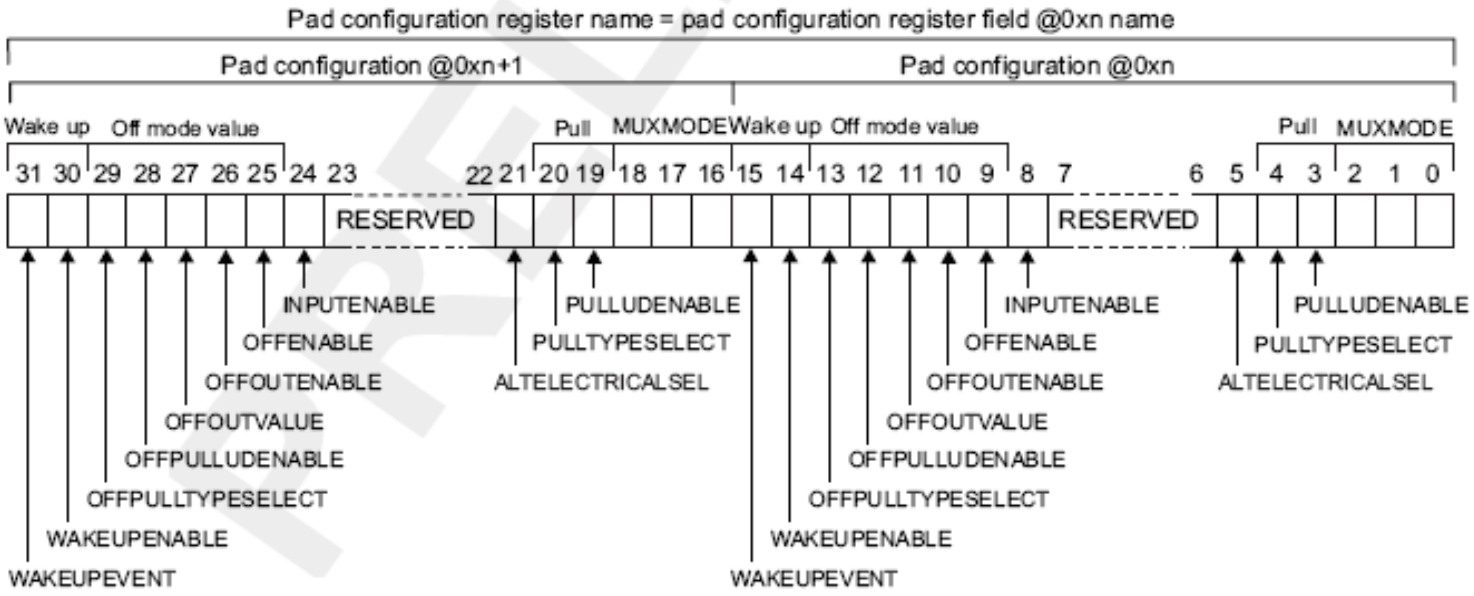
- Only wakeup domain on
- External regulators supplying VDD1, VDD2, DPLL and VDAC can be turned off
- Internal memory LDOs off
- System clock off; Wakeup domain at 32kHz
- No internal memory or logic retained
  - except logic and small backup memory in wakeup domain
- I/Os maintain consistent state
- System state saved in external memory
  - SDRAM in self-refresh
- Faster wake-up than cold boot



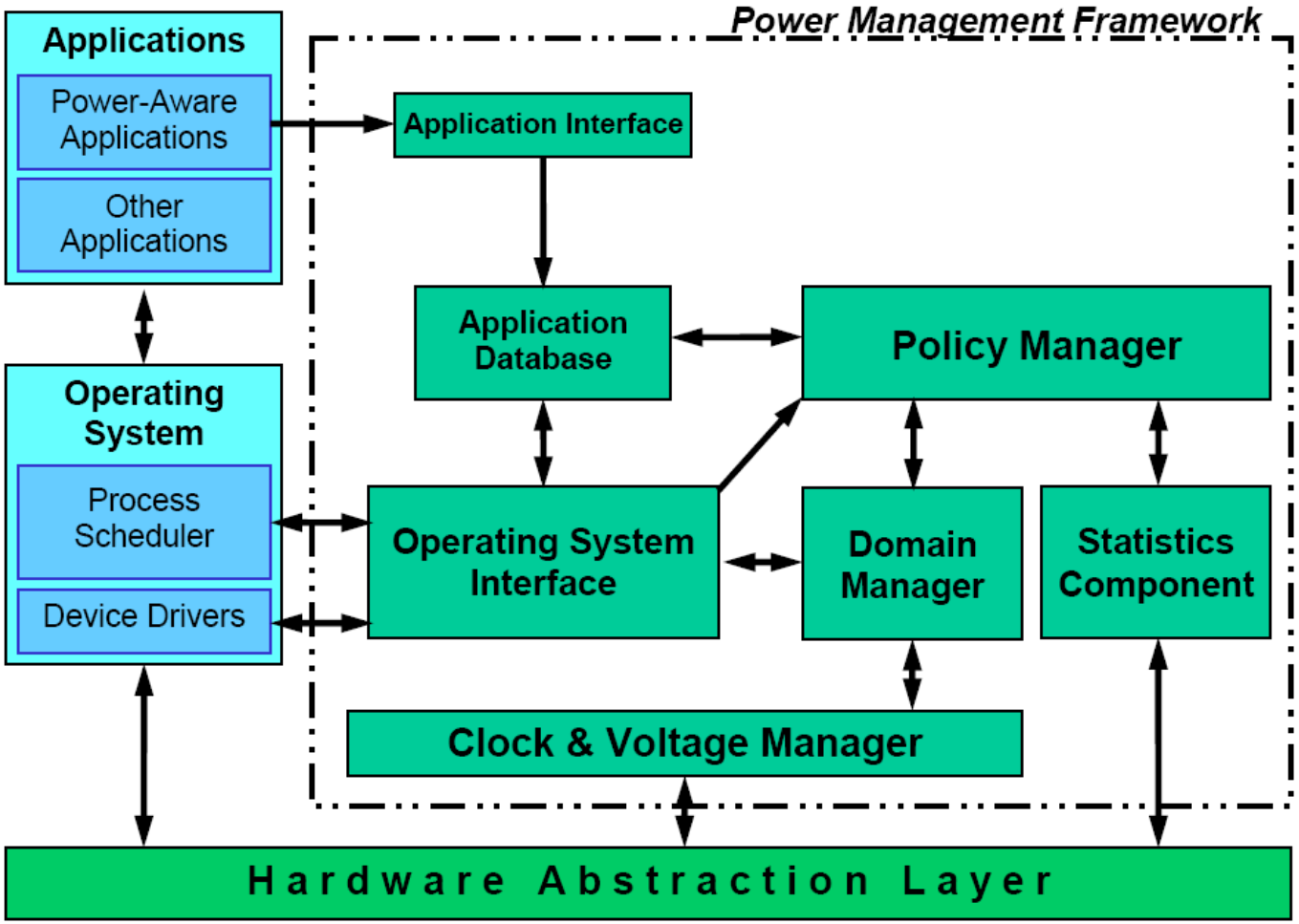
Power consumed is
IO and wakeup leakage

Off-mode I/O control

- Configure I/O functionality when device is active
- Define separate off-mode I/O state for optimal I/O leakage power dissipation
- Enable wakeup detection on I/O in device off-mode



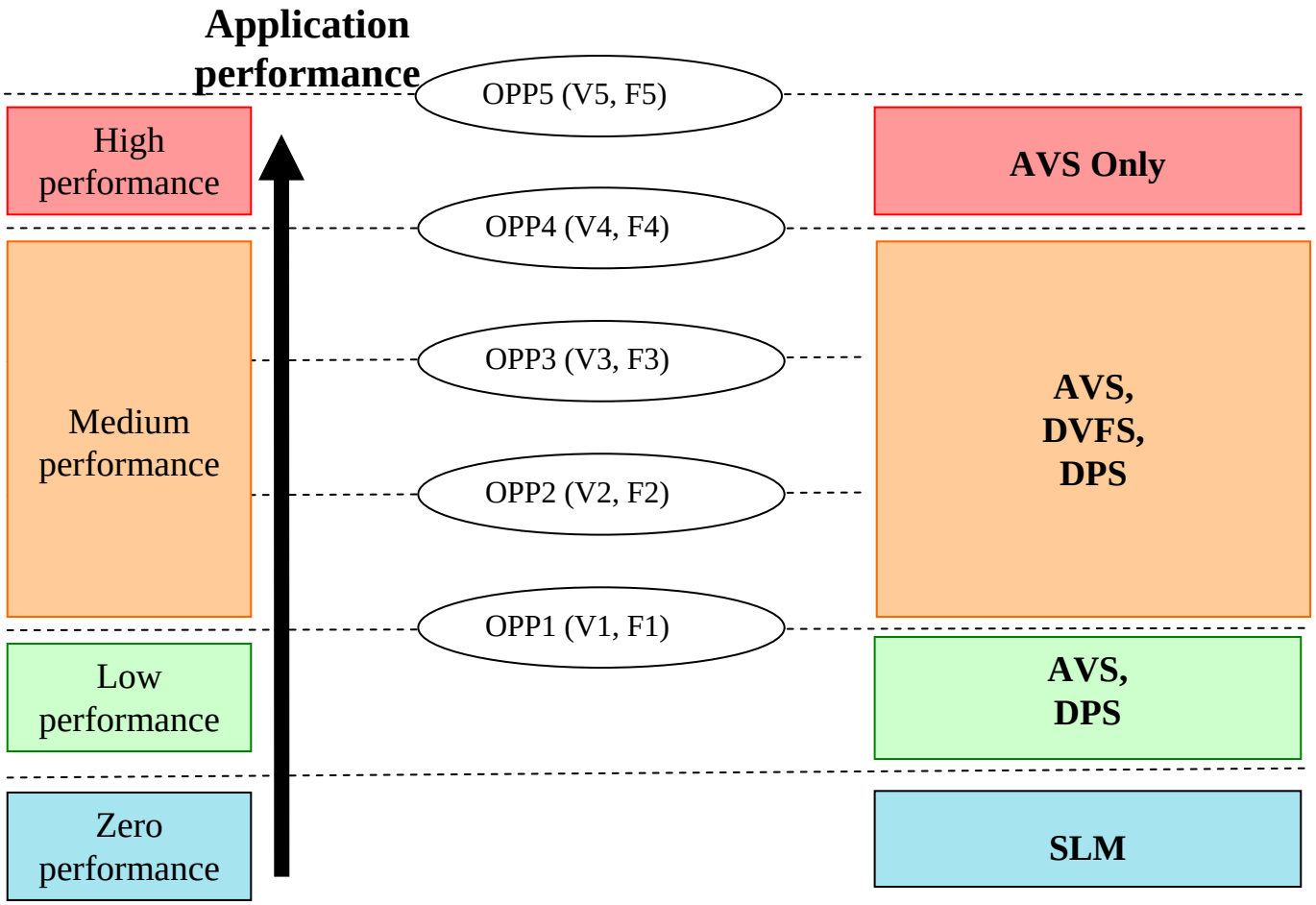
Power management software



Outline

- The need for low power devices
- TI SmartReflex™ power management technologies in OMAP35x processors
- Realizing power savings

Power and performance management



NOTE: OPP is “Operating Performance Point”

Measured power savings – Adaptive Voltage Scaling (AVS) example

- MP3 decode on ARM®Cortex™-A8
  - Linux OS, Gstreamer framework, open-source codec
  - VDD1 OPP1, VDD2 OPP2

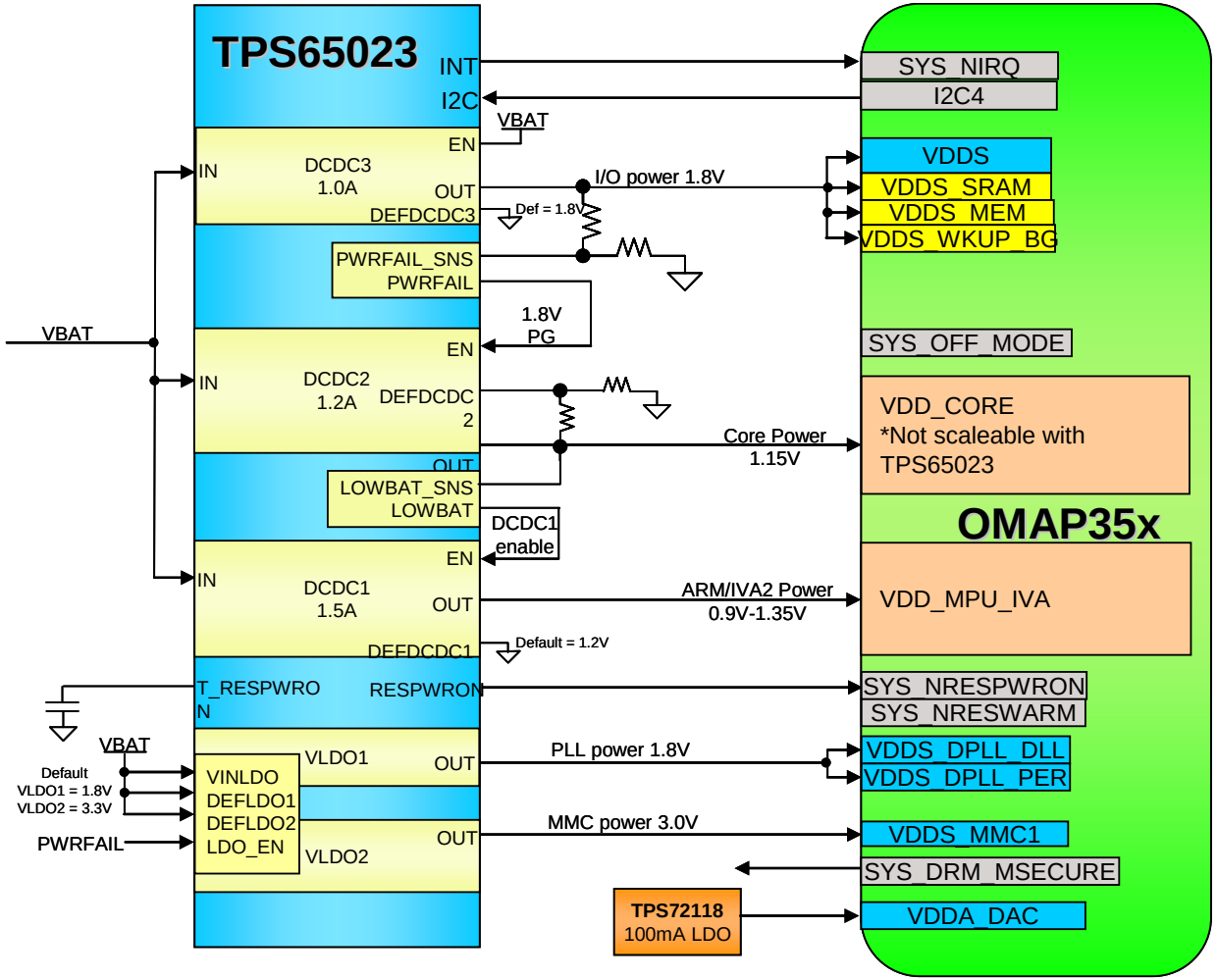
Device type	VDD1+VDD2 without AVS (mW)	VDD1+VDD2 with AVS (mW)	Power savings from AVS (%)
Hot	51.7	42.6	18%
Cold	49.2	46.4	6%

- MPEG-4+MP3 decode (video on IVA, audio on ARM Cortex-A8)
  - Linux OS, Gstreamer framework, open-source codecs, VGA LCD
  - VDD1 OPP3, VDD2 OPP3

Device type	VDD1+VDD2 without AVS (mW)	VDD1+VDD2 with AVS (mW)	Power savings from AVS (%)
Hot	363.3	260.0	28%
Cold	349.7	280.2	20%

NOTE: ES2.1 silicon; Power measurements performed on preliminary Gstreamer demos on TI Board with codecs software not optimized.

TI OMAP35x processor and power regulator connectivity



Voltage domains allow:

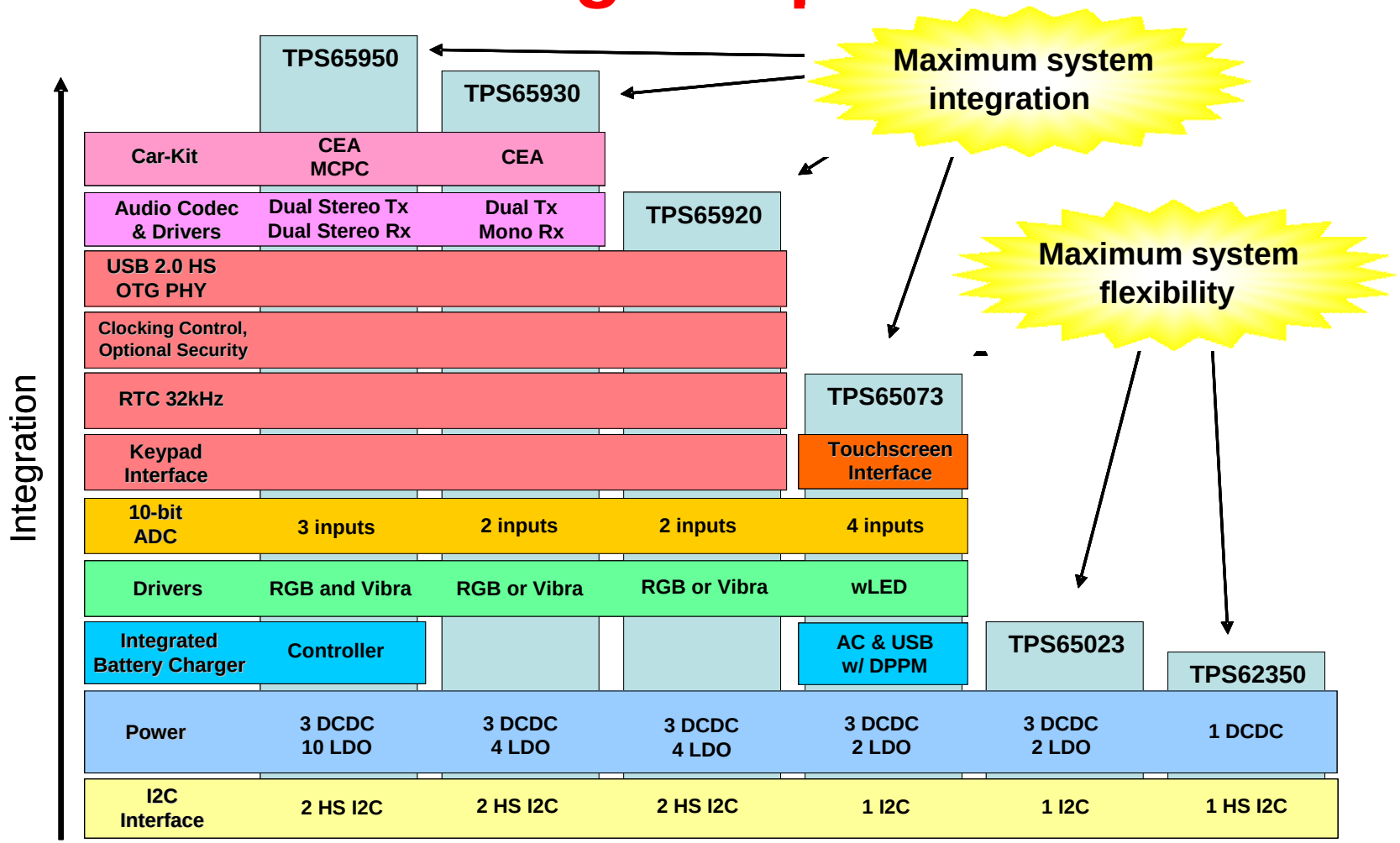
- Separate supplies
- Separate control of sources
- Targeting different power saving methods at different sections of SOC

Simple requirements on power regulator

KEY:

- Scaleable Voltage
- Internal LDO Automatically Scaled
- Fixed Voltage
- Control Signal

Flexible range of power solutions



Summary

Demanding applications and increasing processor performance are driving power

Battery technology and supply efficiency are not enough to address the problem

Holistic approach of silicon IP, SoC design and system software provides the solution

TI “product-proven” SmartReflex™ technology portfolio is based on this strategy

Questions?

Thank you

Arthur Musah
Texas Instruments

www.ti.com\omap35x