Design Considerations for High Performance Audio Analog-to-Digital Converters

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Texas Instruments

Topics

- Introduction
- Key Specifications
- Power Supplies and Bypassing
- Voltage Reference Decoupling
- Input Buffer / Filter
- Clock Jitter
- PCB Layout
- Q & A

Introduction

It’s one thing to say “We Have the Worlds Best Audio ADC”. But how do you go about making it perform to the published specs in a real world application ?

The goal of this presentation is to provide guidelines and food for thought which will help you and your customers achieve the best performance from our high performance audio A/D converters.

Throughout this presentation, data and test results using the PCM4222 and the corresponding EVM are utilized to reinforce principles and illustrate what is possible when the right choices are made.

Key Specifications

- Total Harmonic Distortion and Noise (THD+N)
- Dynamic Range (i.e. SNR in the Presence of Signal)
- Common Mode Rejection
- Power Dissipation

Key Specifications

Total Harmonic Distortion and Noise (THD+N)

•Harmonic distortion and noise is the ratio of the ADC output noise and distortion levels to the output signal level. This includes harmonic, inharmonic, and noise components.

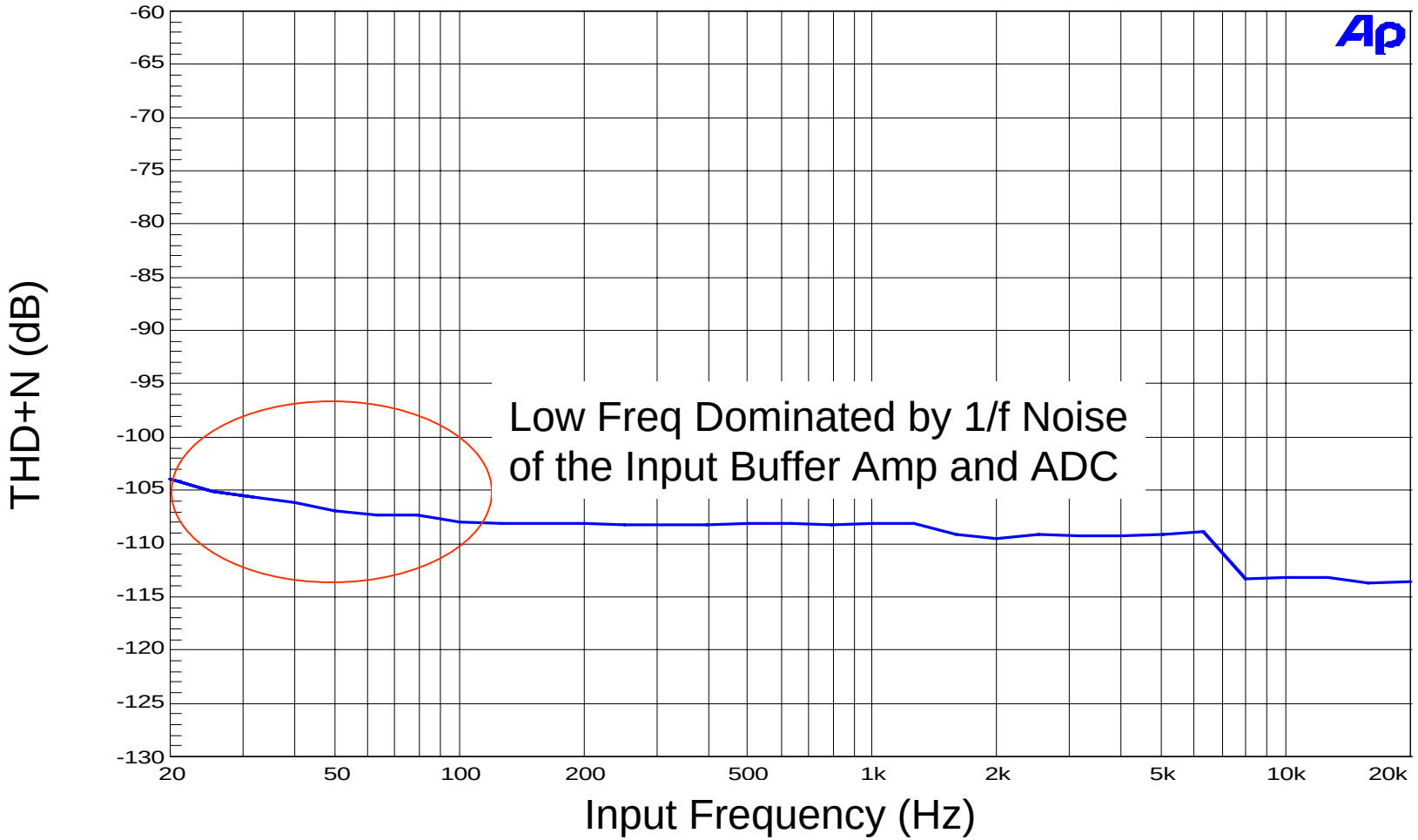
•THD+N is typically measured with a -1dBFS sine wave at a frequency of 997Hz over a specified bandwidth.

•Plots for THD+N vs. Input Frequency, as well as THD+N vs. Input Level, may be included in the device datasheet.

•Examples from the PCM4222 datasheet are shown on the following slides.

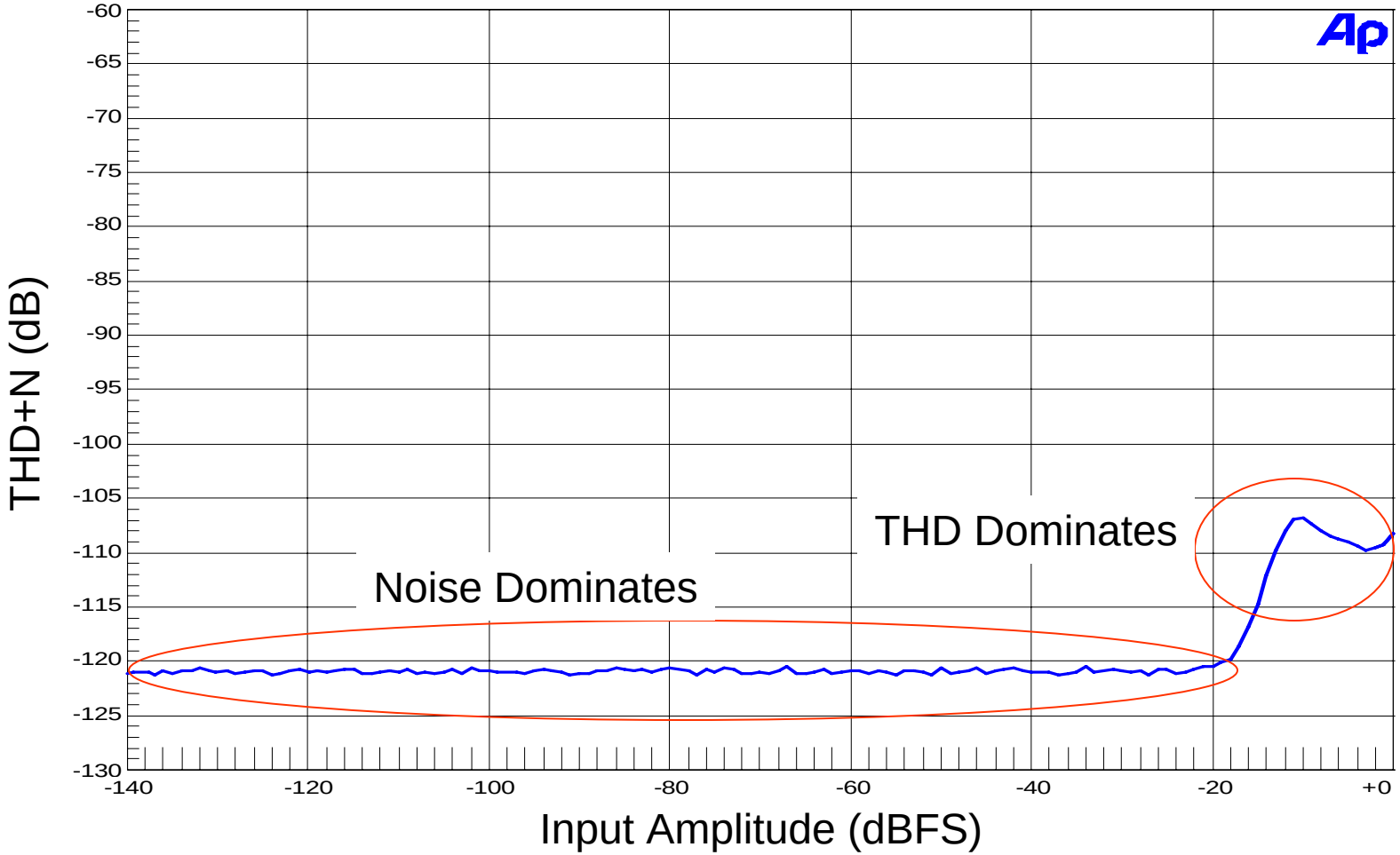
Key Specifications

THD+N vs. Frequency Plot



Key Specifications

THD+N vs. Input Amplitude Plot



Key Specifications

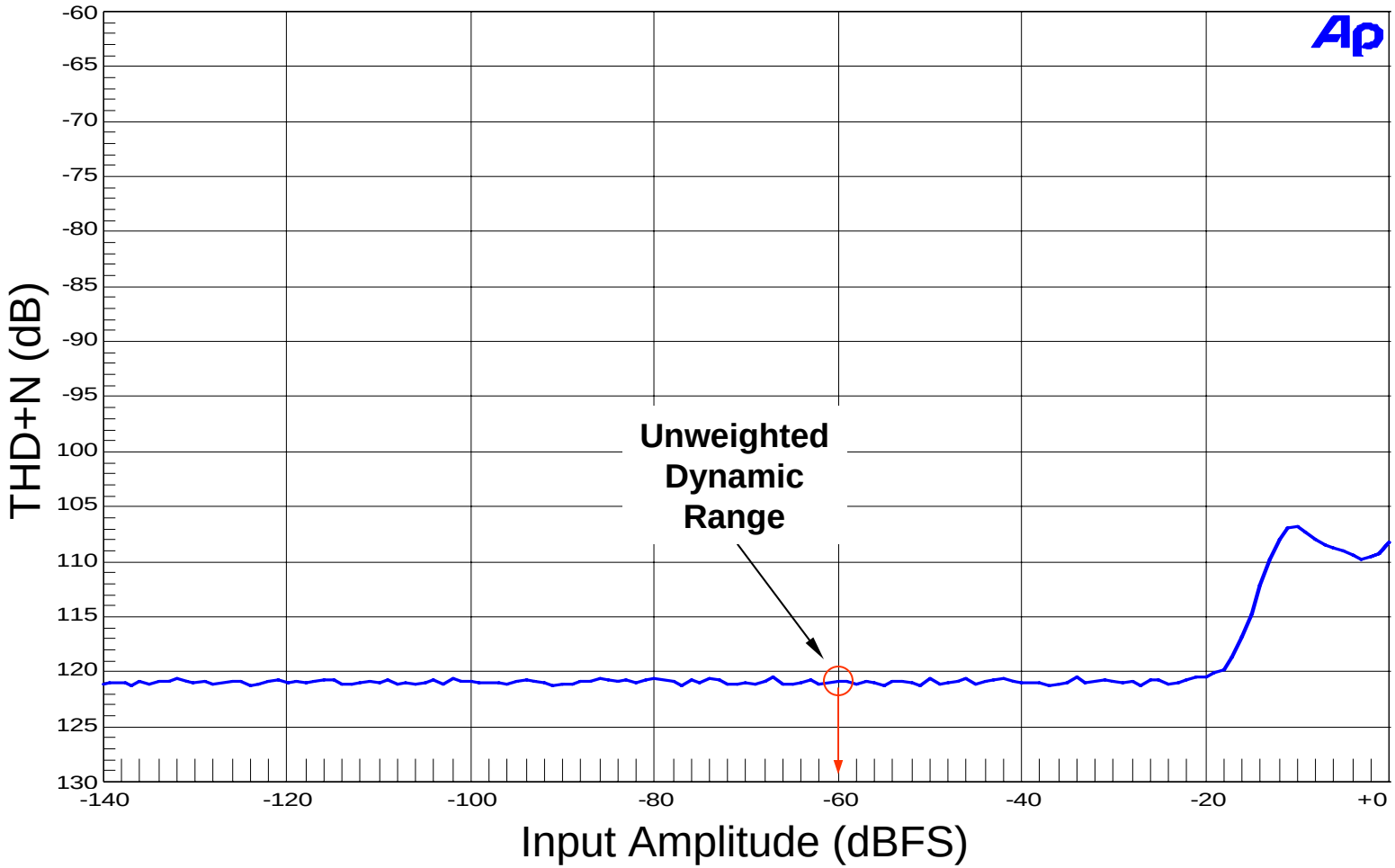
Dynamic Range

Dynamic Range is the ratio of the weighted or unweighted ADC output r.m.s. noise and distortion, referenced to the full-scale output signal level.

Dynamic Range is measured with a -60dBFS sine wave at a frequency of 997Hz over a specified bandwidth, or with a specific weighting filter applied to the captured data (typically an A-weighting, or CCIR weighting function).

Key Specifications

The unweighted Dynamic Range may be derived from the THD+N vs. Input Amplitude Plot, as shown below.



Key Specifications

Common Mode Rejection

For the purposes of this session, common mode rejection refers to the suppression of a signal that is applied simultaneously to both the inverting and non-inverting pins of a differential input to an ADC.

The ratio of the suppressed signal level to the full scale signal level is referred to as the Common Mode Rejection Ratio, or CMRR.

The ADC will have good CMRR (85dB to 100dB). The input buffer/filter passive component matching is critical to maintaining CMRR through the signal chain.

Key Specifications

Power Dissipation

This is a key factor in systems with many channels. Here's how we stack up against the competition.

Manufacturer	Part Number	Dynamic Range (dB)	Total Power Dissipation (mW)
AKM	AK5394A	123	**665**
Cirrus Logic	CS5381	120	**260**
TI	PCM4220/2	123/124	**305**

Power Supplies and Bypassing

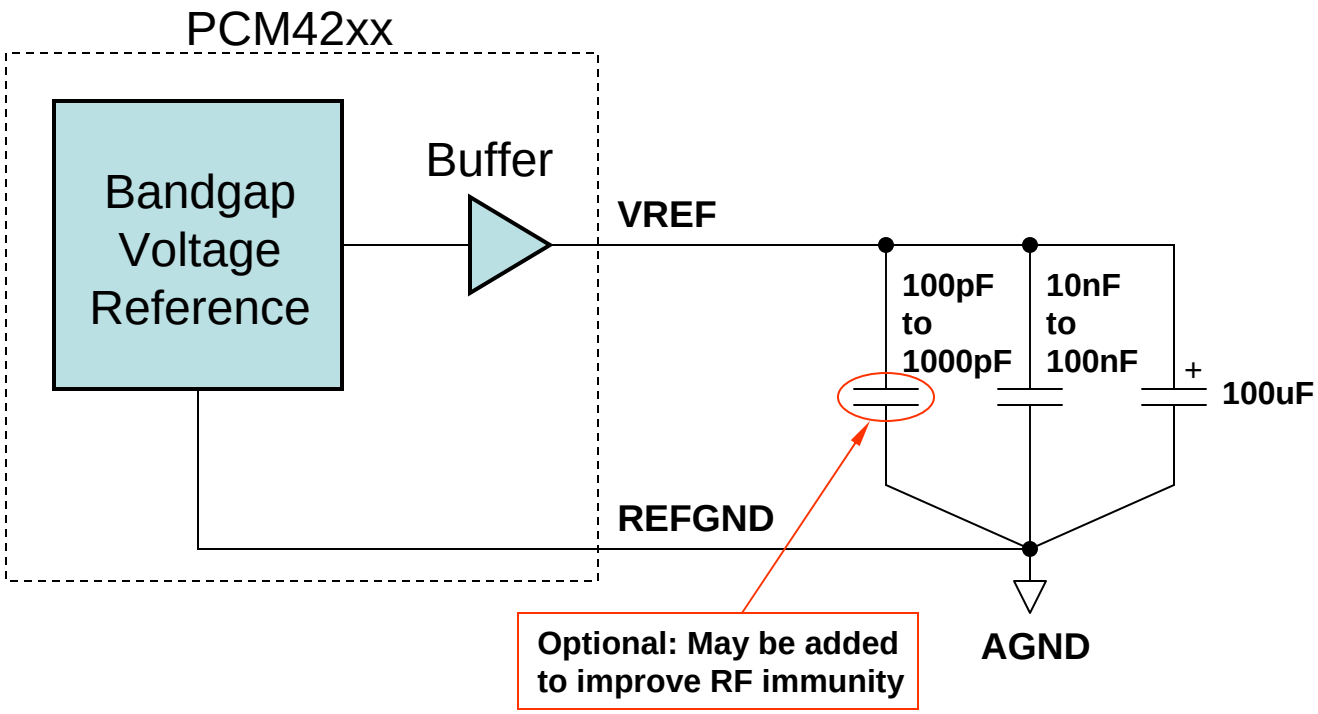
Make Use of Distributed Regulation & Bypassing

• Use low noise LDO devices for local regulation of analog and digital supplies. Advantages include improved power supply noise rejection, lower ripple, shorter current return loops, and simplification of bypassing and filtering.

• Bypassing will include a small capacitor (1nF to 100nF)in parallel with a larger value capacitor (47uF to 100uF). The smaller value cap can be a ceramic C0G/X7R or PPS film chip cap. The larger value cap can be a polymer tantalum chip or aluminum electrolytic. Low ESR caps are recommended.

Voltage Reference Decoupling

Reference Configuration for the PCM420x, PCM4220, & PCM4222.
The buffer output is connected internally to the modulator sampling network.



Recommendations
- The smaller valued chip capacitors are C0G ceramic.
- The 100uF capacitor is a polymer tantalum chip or aluminum electrolytic.
- Low ESR caps are preferred.

Voltage Reference Decoupling

Simple Rules for Best Results

- Use Surface Mount Components. Lower Profile Reduces EMI Pick-Up.
- Mount Capacitors as Close to the ADC Pins as Possible.
- Mount Smaller Valued Capacitors Closest to the ADC.
- Minimize Loop Area for Return Currents.
- Use Low Equivalent Series Resistance (ESR) Capacitors.
- Do Not Connect Additional Circuitry to the VREF Pin !!

Input Buffer / Filter

- Functional Requirements
- Amplifier Selection Criteria
- Noise Budget
- Noise Simulation Using TINA
- Actual Buffer Measurements
- EMI Filtering Considerations

Input Buffer / Filter

Functional Requirements for the Input Buffer

- Anti-Alias Filtering (1st Order Minimum)
- Input Signal Scaling (Gain or Attenuation)
- Input Clamping / Limiting
- EMI Filtering

Input Buffer / Filter

Amplifier Selection Criteria

- Low Noise: Less than 1µV RMS total output noise over the 20Hz to 20kHz bandwidth.

- Low THD: 0.0002% or less

- Low Output Impedance

- Adequate Slew Rate: 10 V/µS or faster

- Output Drive/Stability: Must be able to drive a large anti-alias filter capacitor (2700pF) without stability issues.

Input Buffer / Filter

Total Noise Budget

$$V_{N\ (total)} = (V_{NADC}^{2} + V_{NBUF}^{2})^{1/2}$$

Maximum Input Buffer Noise

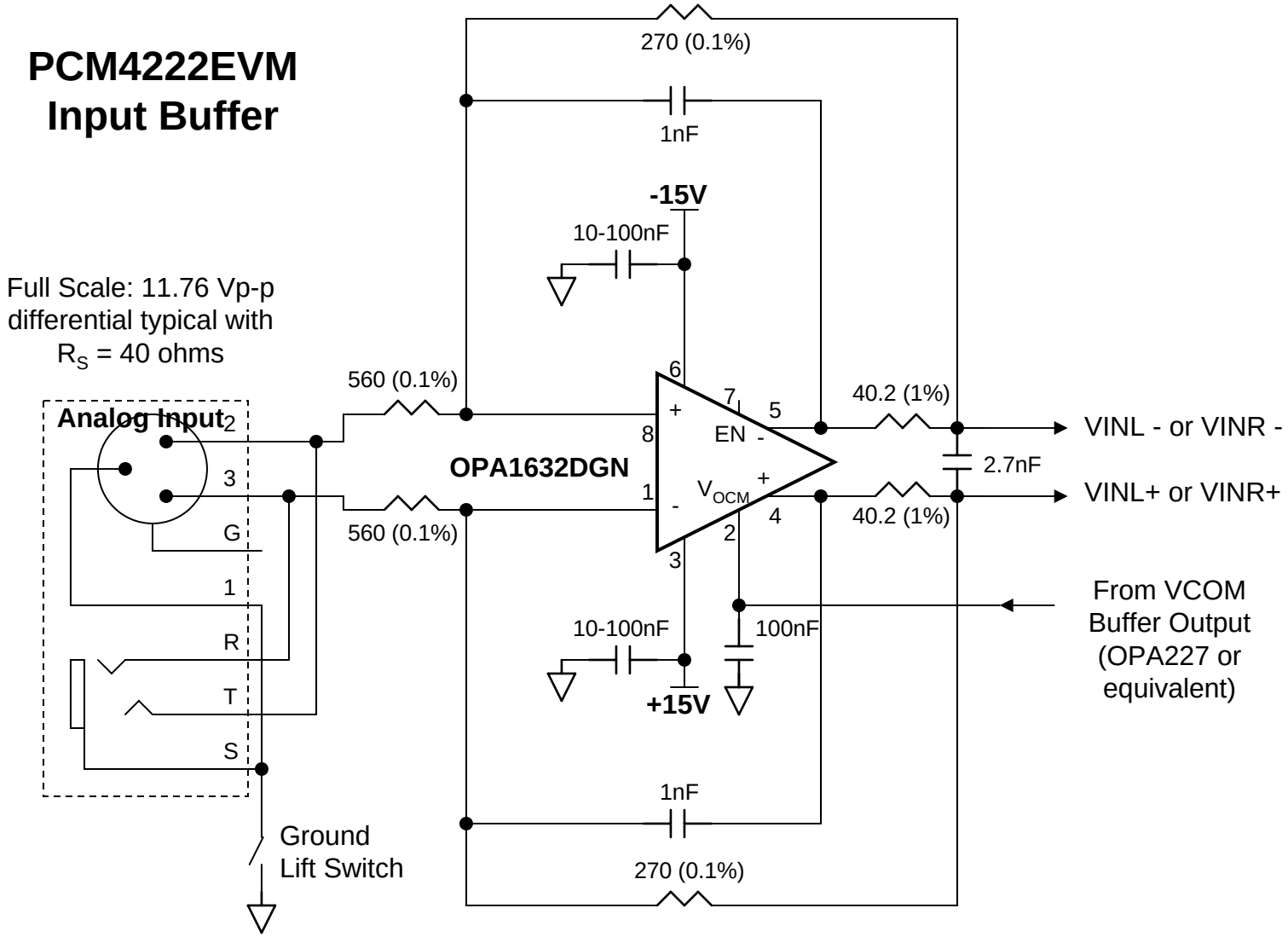
$$V_{NBUF\ (max)} = (V_{N\ (total)}^{2} - V_{NADC}^{2})^{1/2}$$

Equating ADC Noise Voltage to ADC Dynamic Range (DR)

$$V_{NADC} = (10^{(DR\ /\ -20)})\ V_{FS\ (RMS)}$$

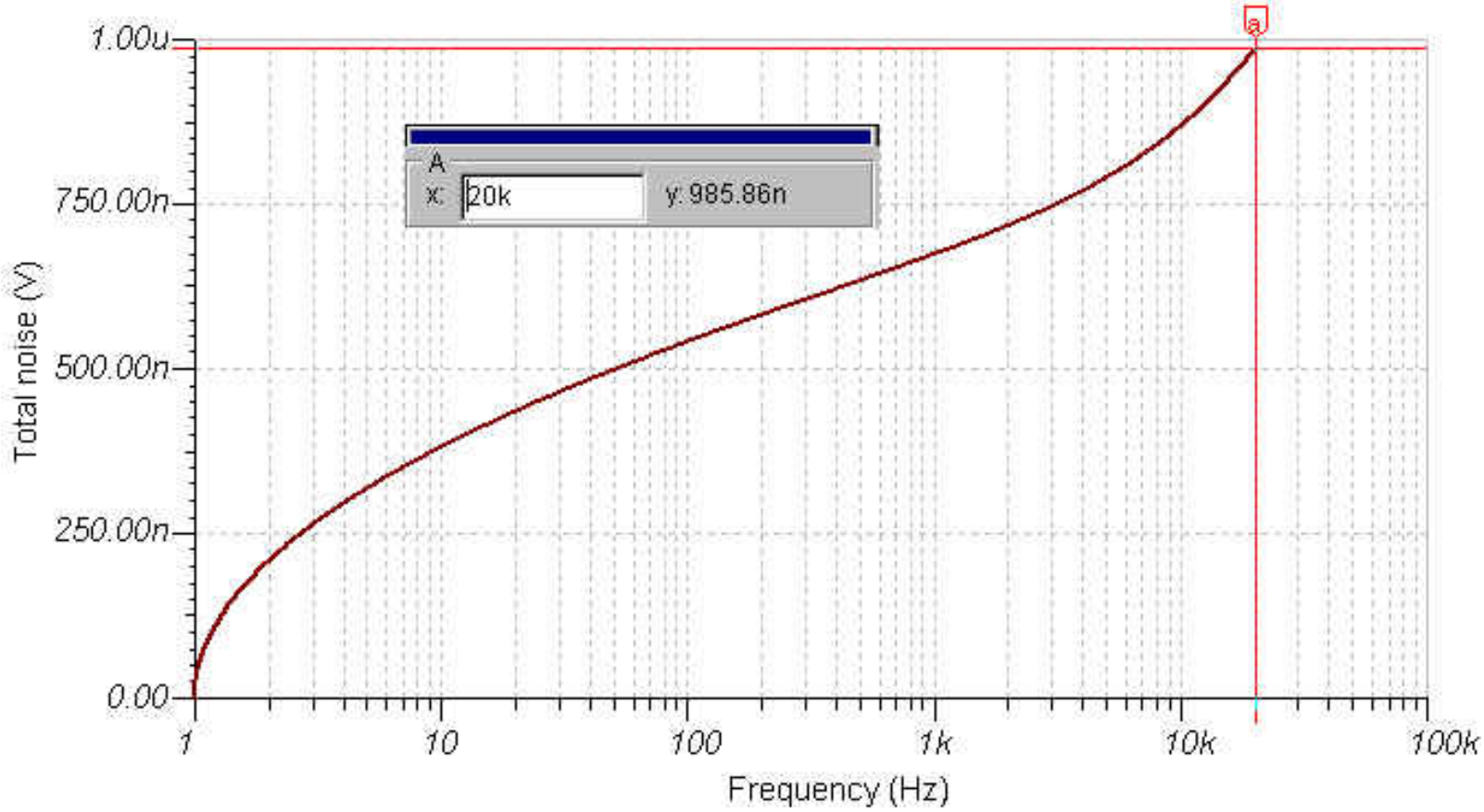
Where DR = unweighted dynamic range of the ADC for a given measurement bandwidth

Input Buffer / Filter



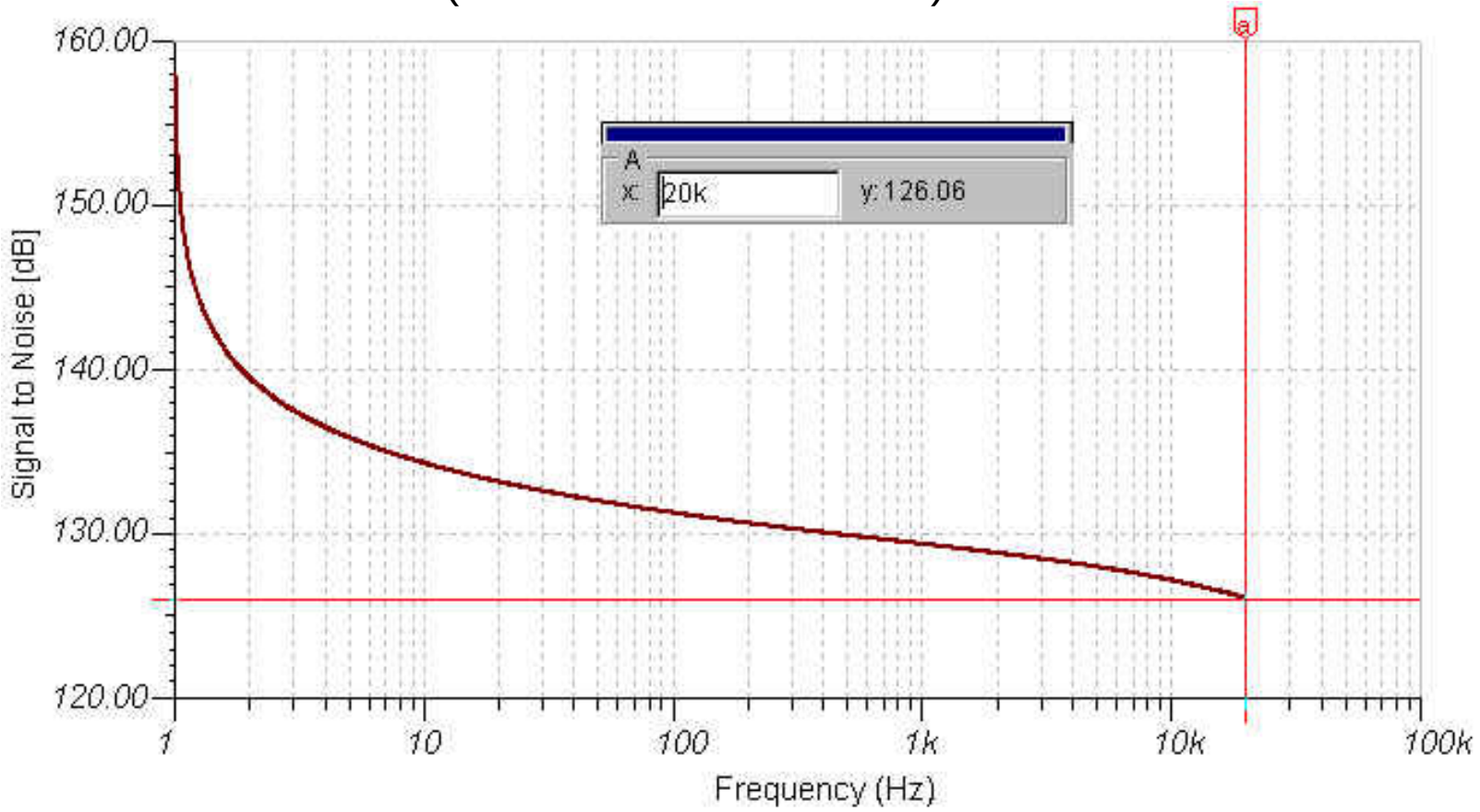
Input Buffer / Filter

Results for the TINA 7 Noise Analysis for Input Buffer Circuit
BW = 20kHz, Total Output Noise = 0.98586µV RMS



Input Buffer / Filter

Results for the TINA 7 Noise Analysis for Input Buffer Circuit
BW = 20kHz, Signal-to-Noise (SNR) = 126.06dB
(Full Scale = 1.98V RMS)



Input Buffer / Filter

Input Buffer Circuit Output Noise Measurements (Unweighted)
Measured with an Audio Precision SYS-2722

Measurement Bandwidth	Output Noise (Microvolts RMS)	SNR (dB) Full Scale = 1.98V RMS
22Hz to 20kHz	0.89	126.95
22Hz to 40kHz	1.26	123.93
22Hz to 80kHz	1.80	120.83

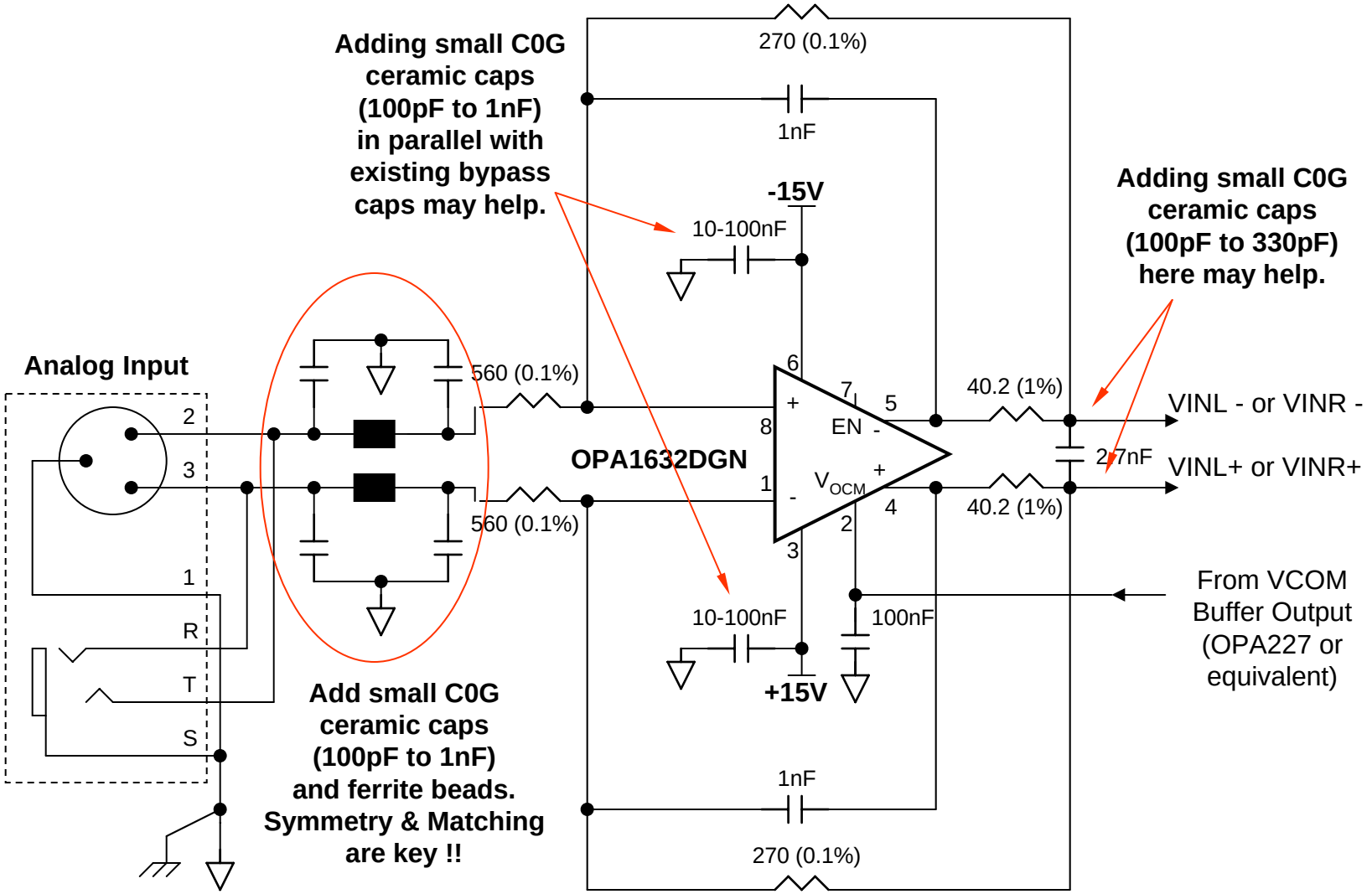
EMI Filtering

- The selected amplifier IC will provide band limiting for for anti-aliasing, but will not provide the necessary filtering for rejecting electromagnetic interference (EMI).

- Additional filtering is required for EMI, and must be added prior to the input buffer, and in some cases, at the output of the input buffer.

- The next slide illustrates a few simple additions to our existing buffer circuit that can help to mitigate EMI.

Input Buffer / Filter



Clock Jitter

What is Jitter, and Why Should I Worry About It ?

- Jitter is defined as the cycle to cycle variation in the master or sampling clock edge transitions, due to intrinsic (or internal) and externally induced error sources.

- All Nyquist sampling and oversampling data converters (including delta-sigma types) are susceptible to errors caused by master or sampling clock jitter.

- Jitter can degrade the distortion and signal-to-noise specifications of a data converter. The effects are best understood through measurement examples.

Clock Jitter

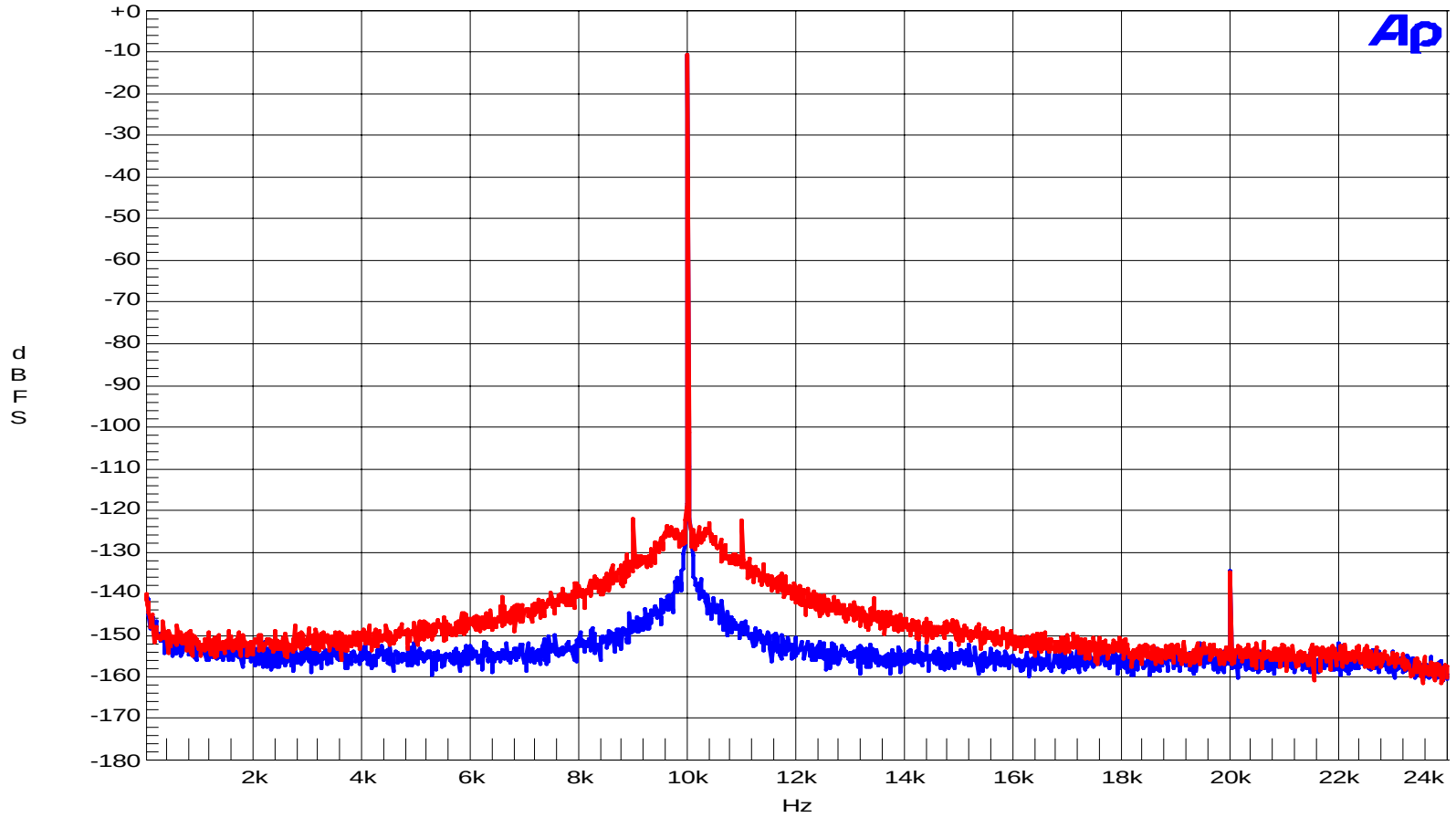
Measurement Results Using Sinusoidal and Wideband Random Jitter Injection

Sinusoidal jitter modulates the master clock edges with a sine wave at a specified frequency and jitter amplitude. The results are dependent upon both the jitter frequency and amplitude, as well as the ADC input signal amplitude and frequency.

Wideband Random jitter modulates the master clock edges with a jitter signal that is a non-Gaussian probability density function, where the first null is at the sampling rate (Fs). This jitter function has peaks at plus and minus the jitter amplitude, as well as a -3dB point at 0.44 × Fs.

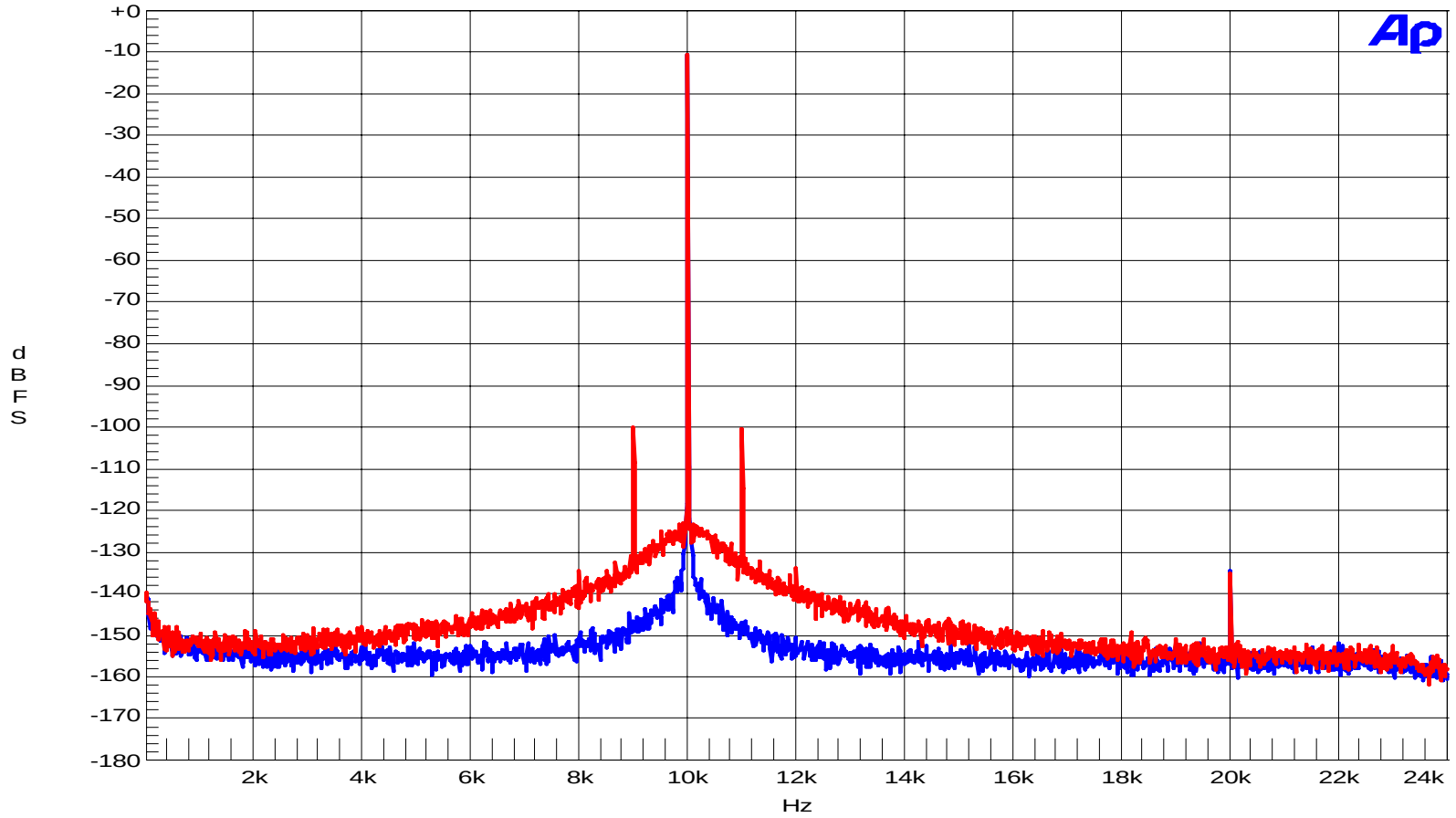
Clock Jitter

Blue Plot: 24.576MHz Master Clock with less than 30ps intrinsic jitter.
Red Plot: 100ps Peak Jitter (1kHz Sinusoidal) added to the Master Clock.



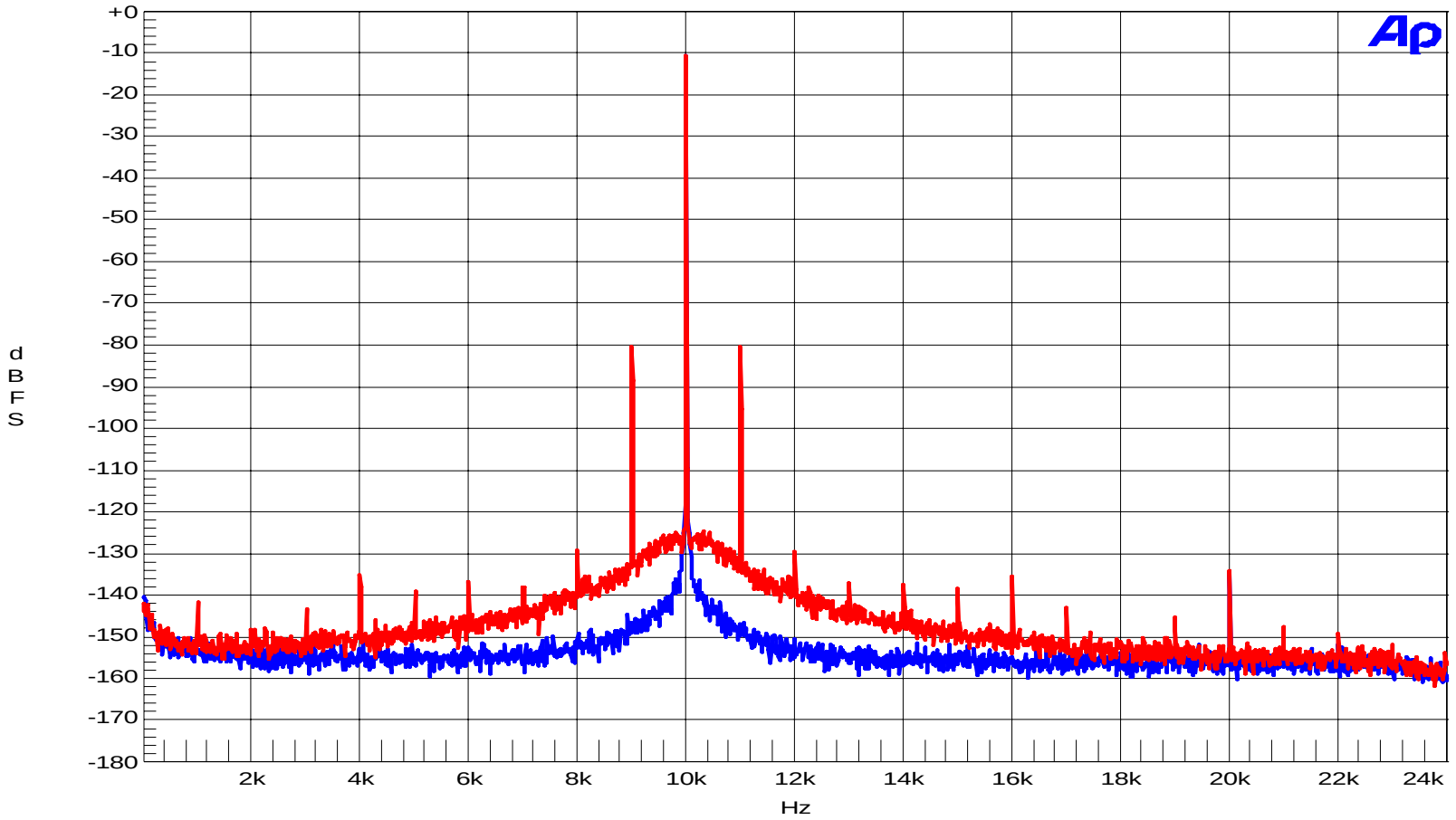
Clock Jitter

Blue Plot: 24.576MHz Master Clock with less than 30ps intrinsic jitter.
Red Plot: 1ns Peak Jitter (1kHz Sinusoidal) added to the Master Clock.



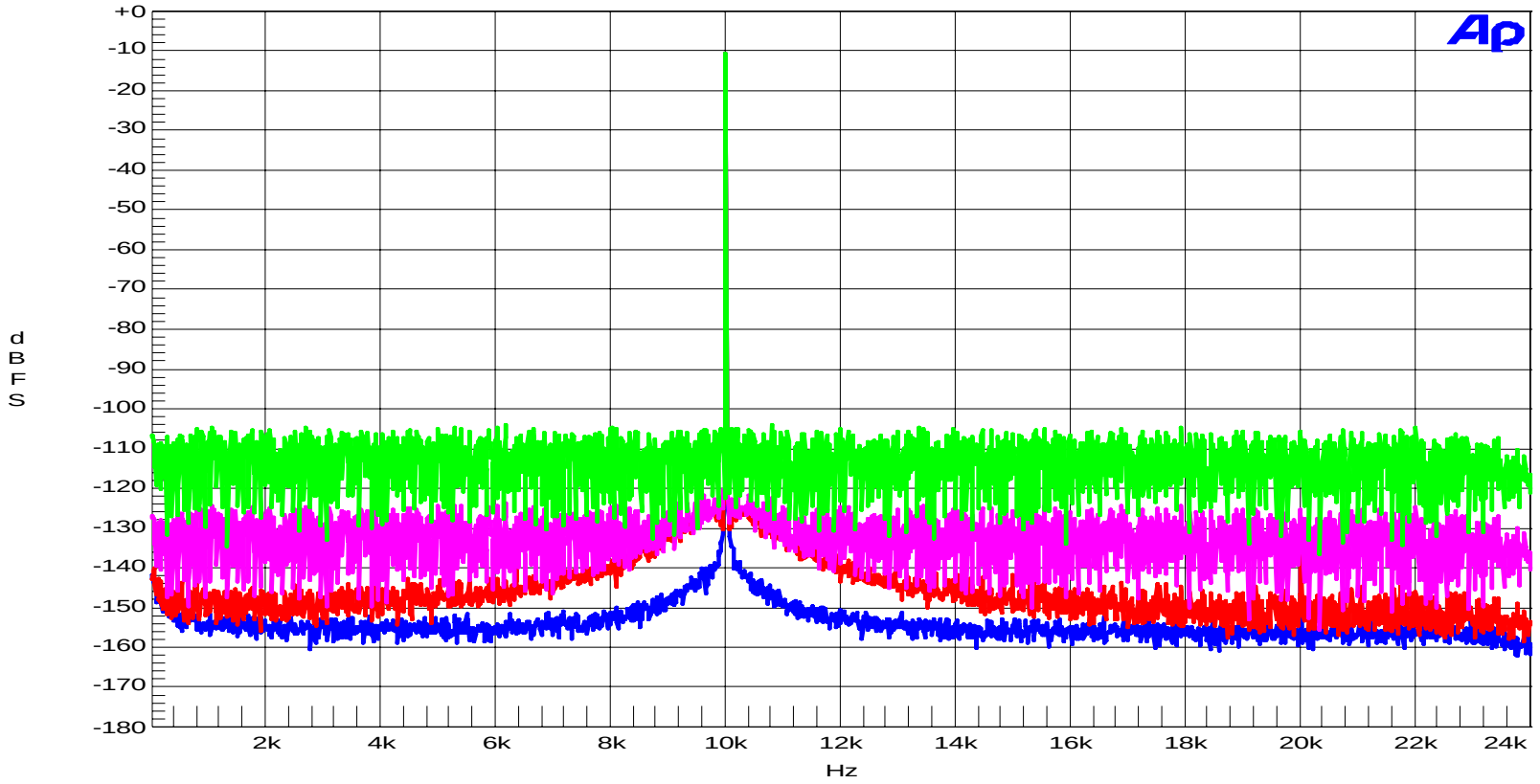
Clocking Jitter

Blue Plot: 24.576MHz Master Clock with less than 30ps intrinsic jitter.
Red Plot: 10ns Peak Jitter (1kHz Sinusoidal) added to the Master Clock.



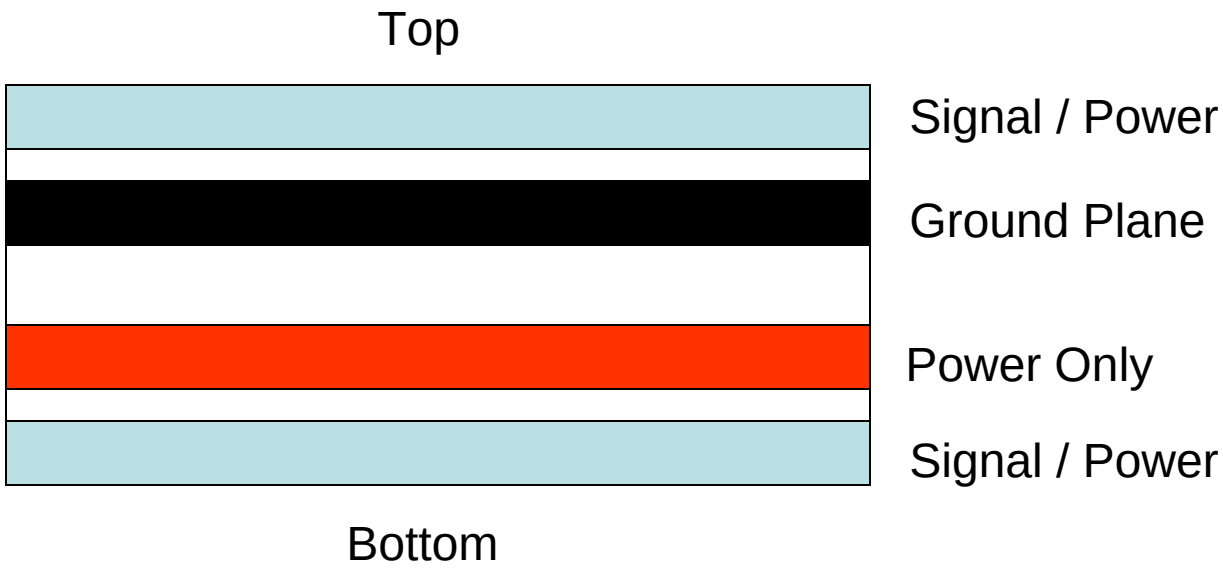
Clocking Jitter

Blue Plot: 24.576MHz Master Clock with less than 30ps intrinsic jitter.
Red Plot: 100ps Peak of Wideband Jitter added to the Master Clock.
Magenta Plot: 1ns Peak of Wideband Jitter added to the Master Clock.
Green Plot: 10ns Peak of Wideband Jitter added to the Master Clock.



PCB Layout

Four Layer Design with Common Ground Plane



PCB Layout

Basic Guidelines

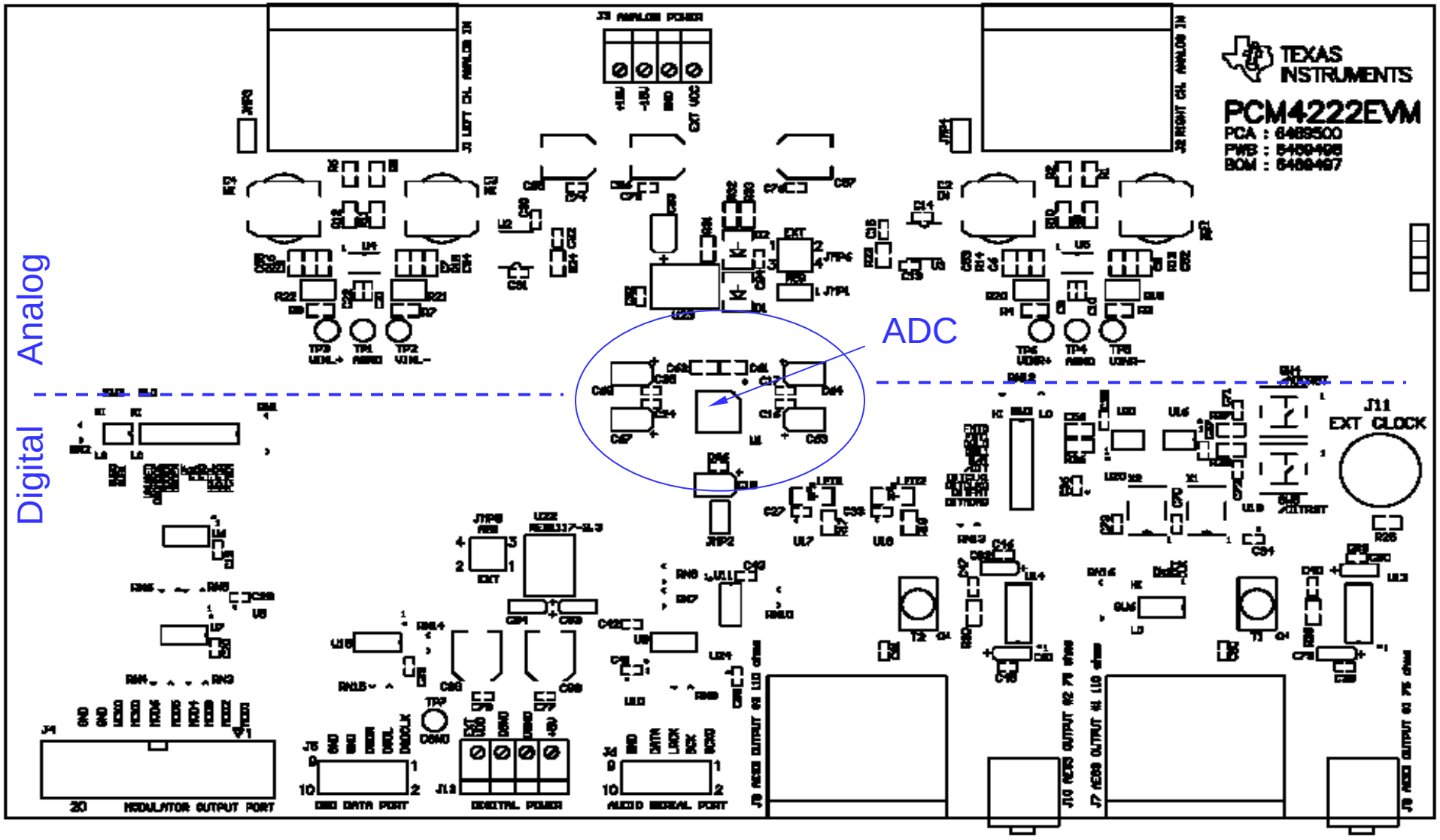
- Use a single ground plane.

- Routing for the analog signal path should be on one layer (top or bottom). The ground plane should be the next layer down from the analog signal layer.

- If a split plane is required for isolation, mount the ADC over the analog plane, and utilize digital couplers for digital I/O routes across the split. If necessary, utilize an LDO to derive the ADC digital supply from the +5V analog supply.

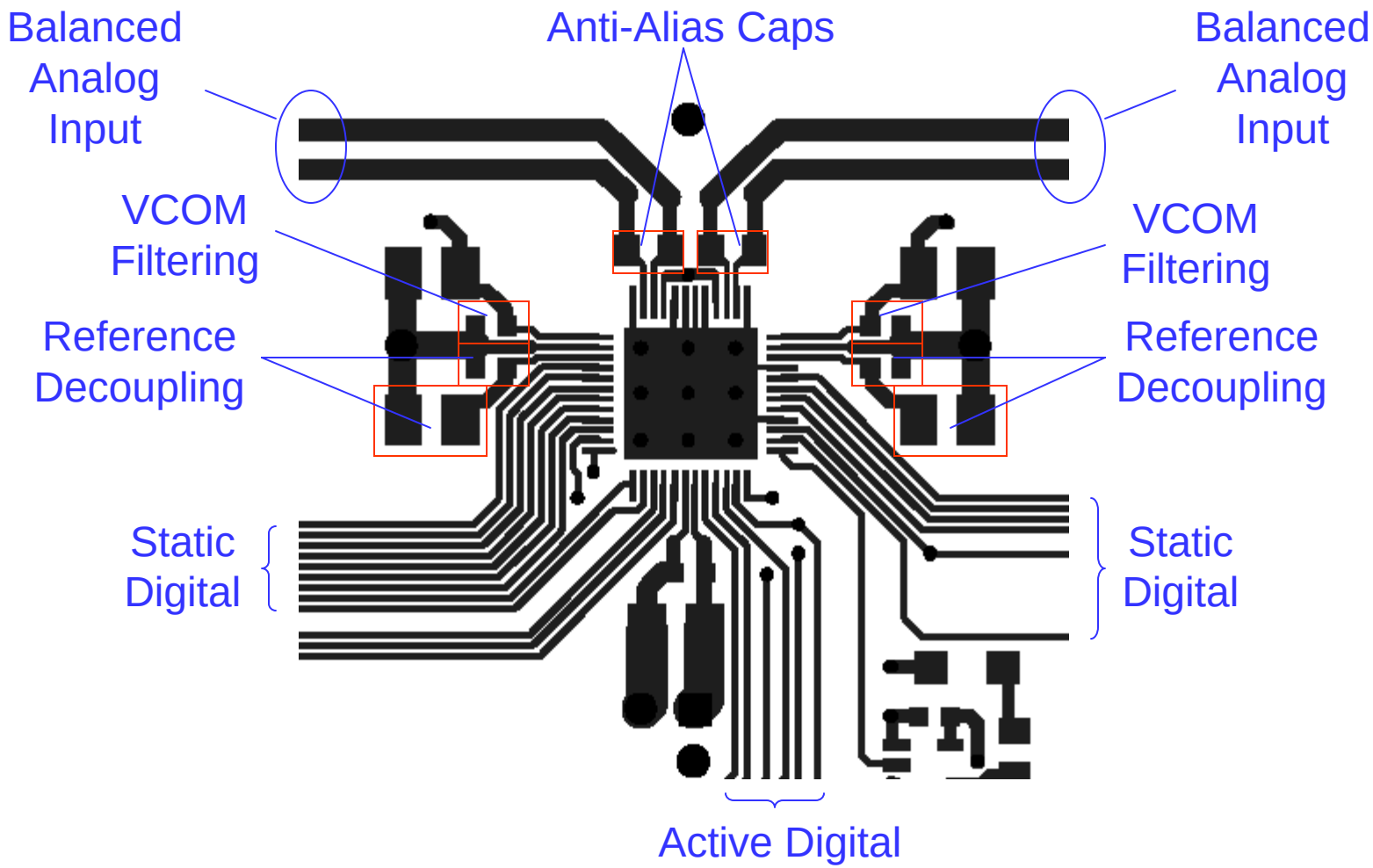
- Floor planning is key. See the next slide …

PCB Layout


Analog
Digital
ADC
TEXAS INSTRUMENTS
PCM4222EVM
PCA : 6489500
FWB : 6489498
BOM : 6489497
J11
EXT CLOCK
MODULATOR OUTPUT PORT
DSD DATA PORT
DIGITAL POWER
AUDIO SERIAL PORT

PCB Layout

Critical Component Placement & Routing



Thank You!

Questions ?