Basic PWM Techniques for Audio Amplifiers

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Home Audio Amplifiers
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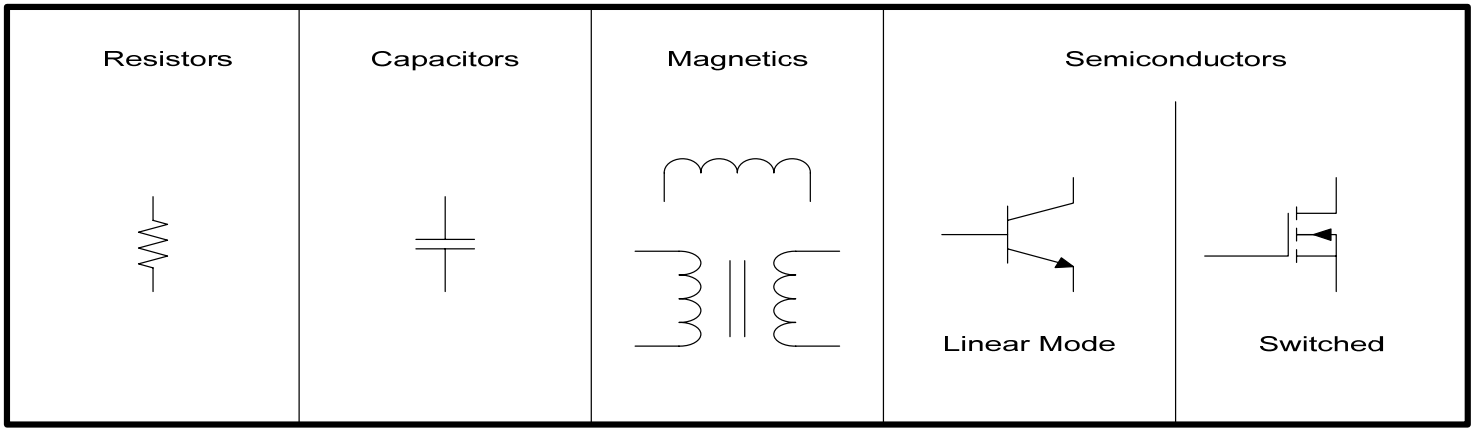
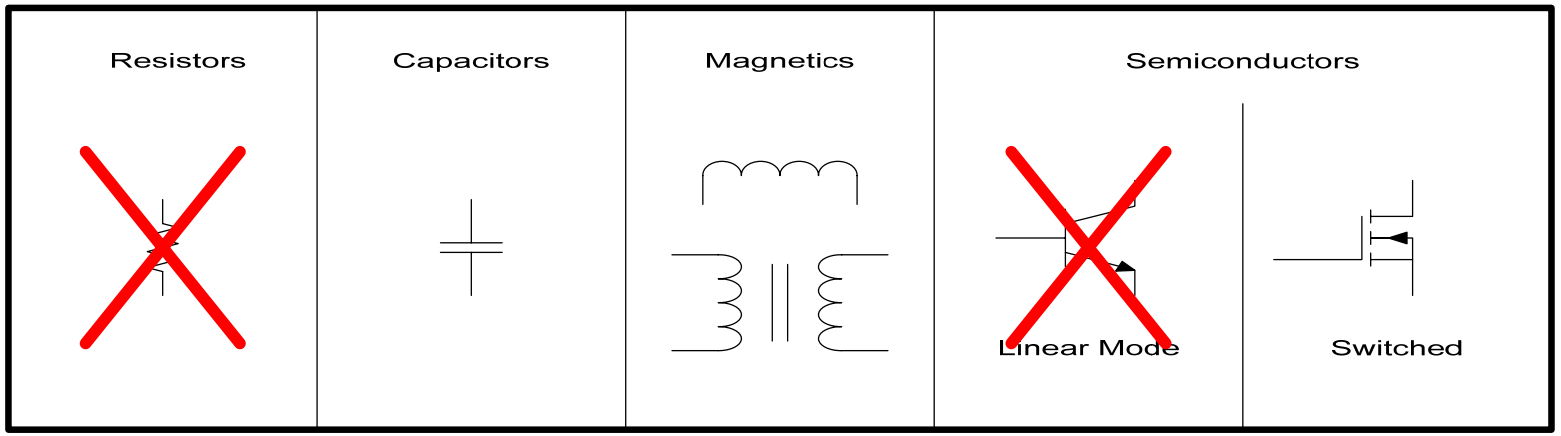
Class D Components

Basic components available to a designer



Class D Components

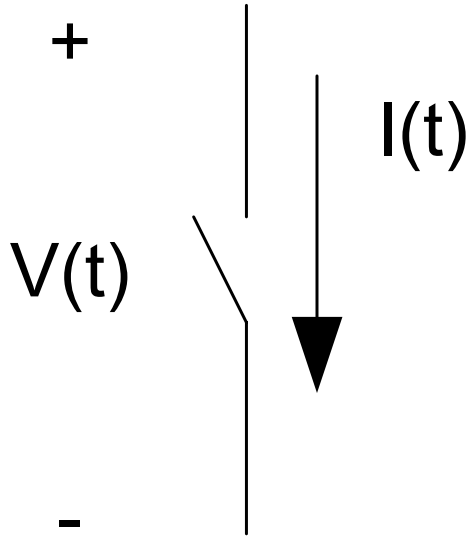
Components used for Class D amplifiers must have low losses



Class D Components

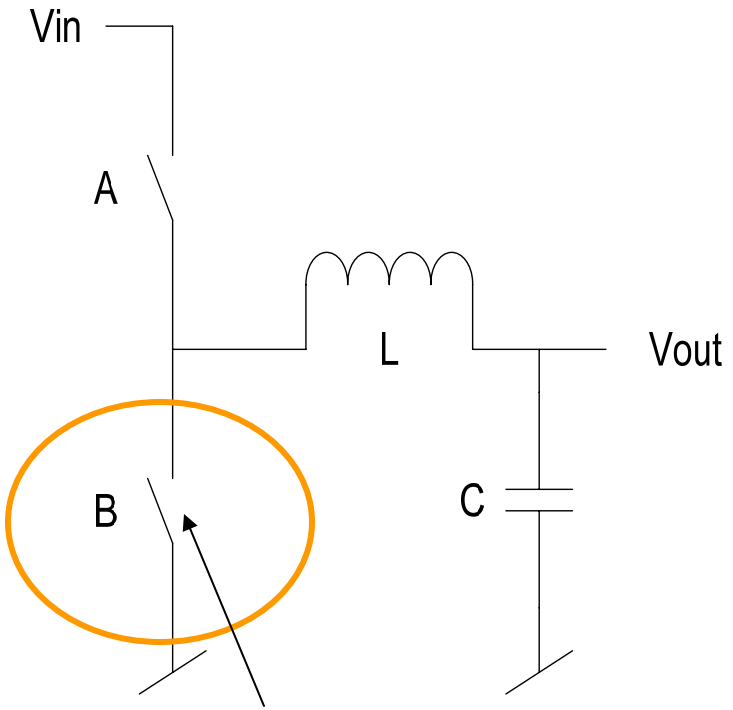
The Perfect Switch, an ideal component:

- Switch Open: I(t) = 0
- Switch Closed: V(t) = 0
- Ploss(t) = V(t) * I(t) = 0

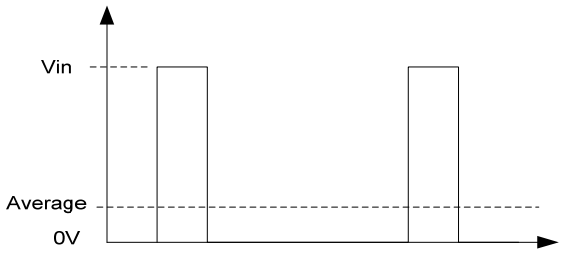


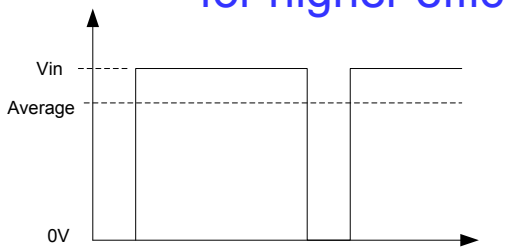
Synchronous Buck Converter

- Switches A and B are alternately on ON and OFF, whereby the midpoint forms a PWM signal with a high frequency
- Duty Cycle, d = Ton / (T_{ON} + T_{OFF})
- The average of the PWM signal is reconstructed with the LC output filter removing the high frequency carrier.
- $V_{OUT}(t) = V_{IN} * d(t)$



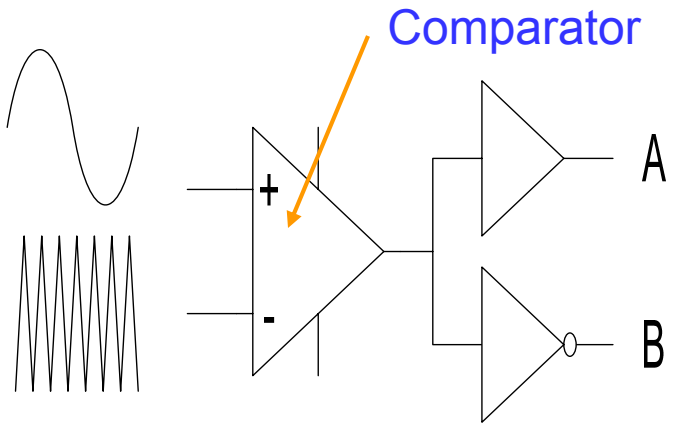
Replaces catch diode for higher efficiency

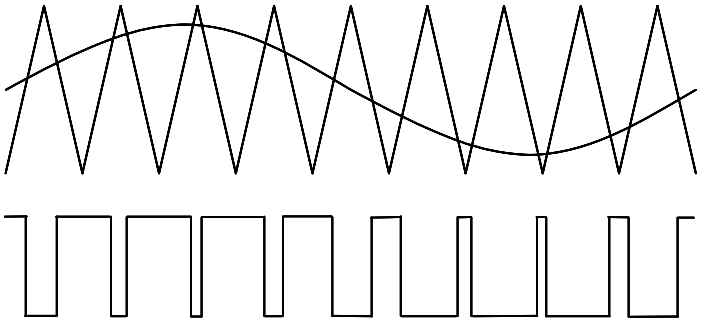




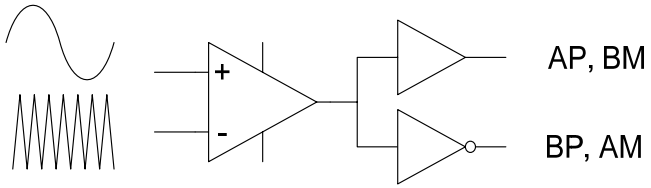
Simple Analog PWM Generator

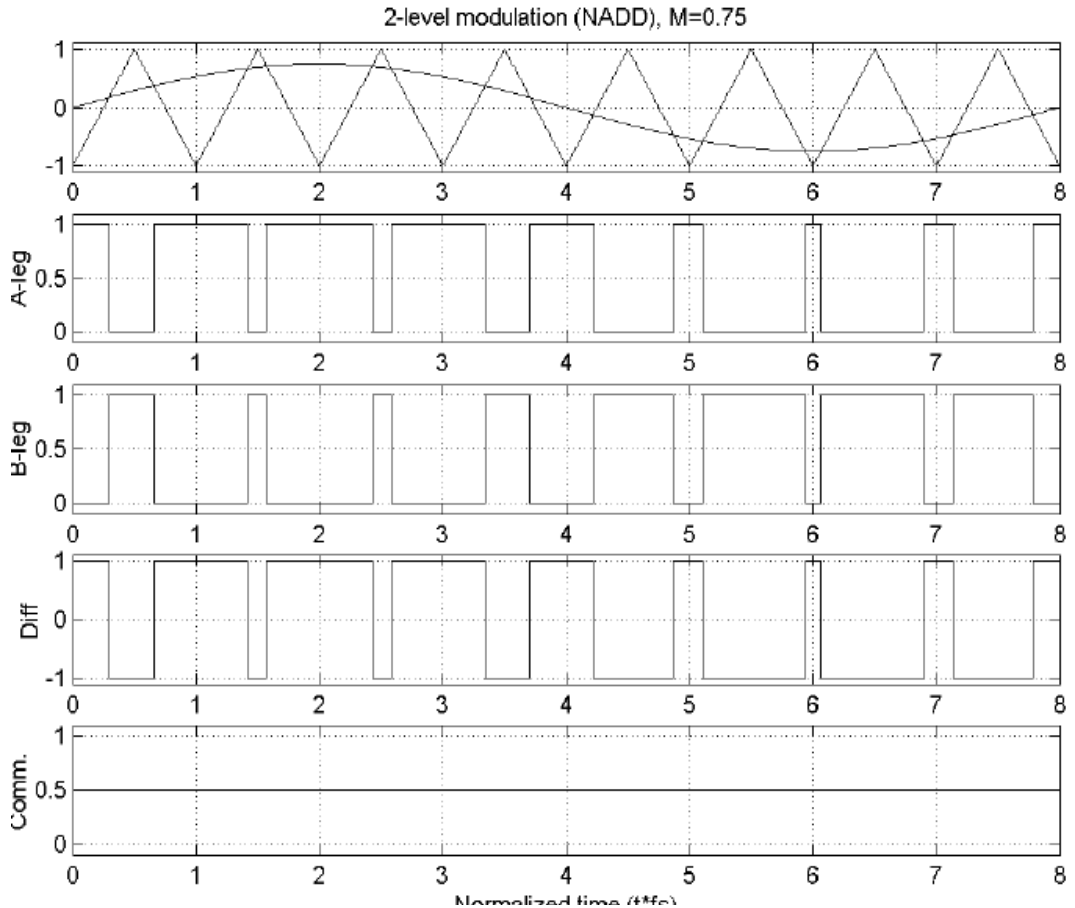
- **The PWM signal can be generated by comparing the audio signal with a triangle wave**
- **Switching frequency is determined by the frequency of the triangle wave**
- **This modulation is called Natural Sampling**



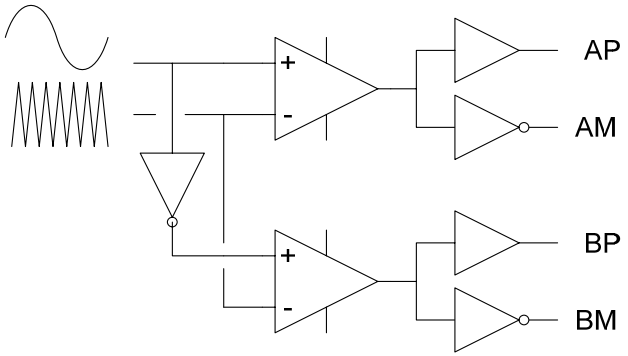


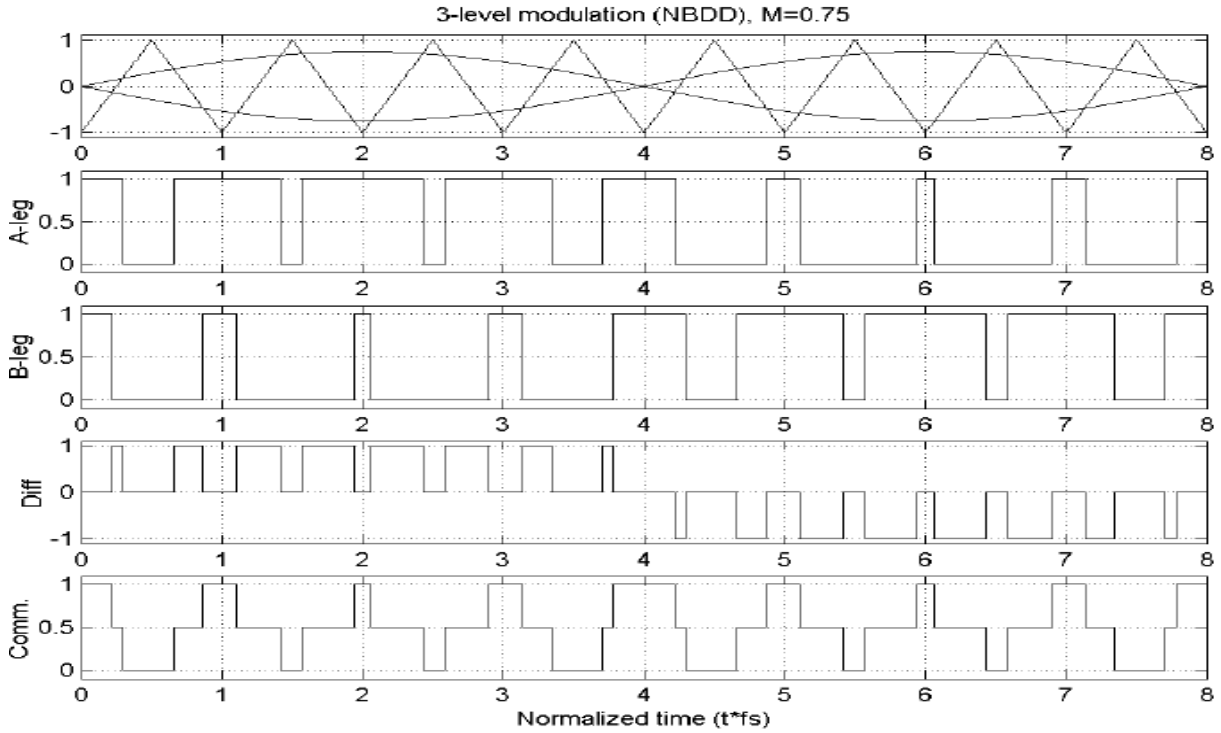
AD Mode Control





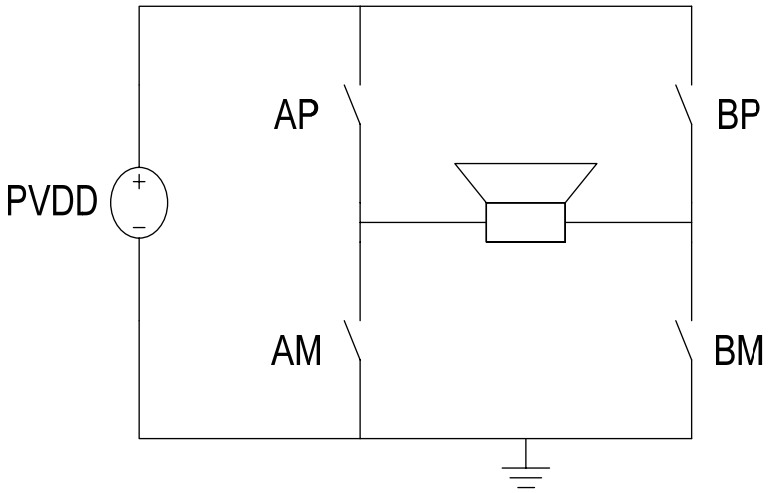
BD Mode Control





BD Mode Control

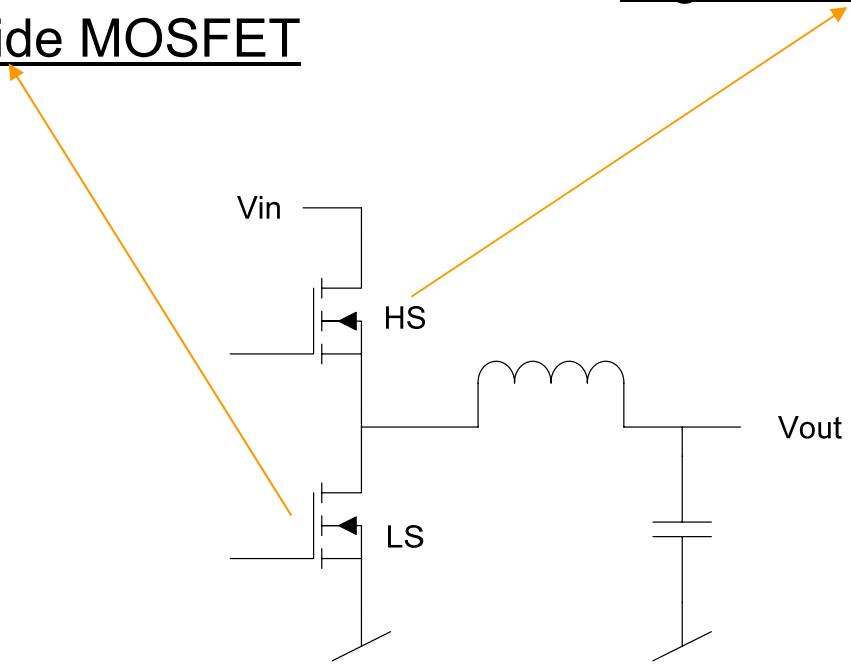
- BD mode only relevant in Bridge Tied Load (BTL)
- There are 4 switches to control
- Switches AP (BP) and AM (BM) must switch alternately to avoid shoot through
- Or be both open, Hi-Z



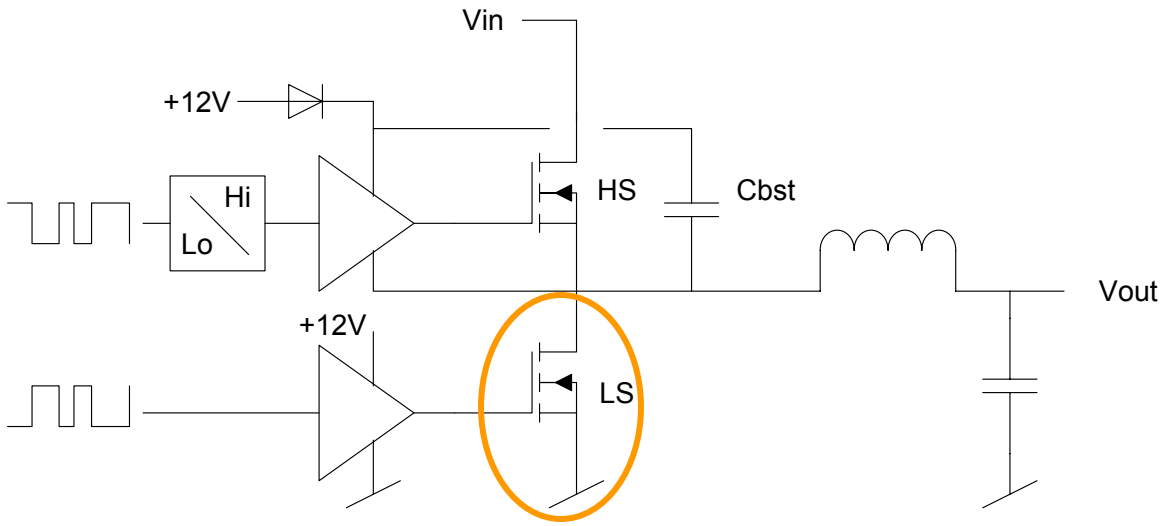
Power Stage

- Ideal Switches are implemented as less than ideal N-Channel MOSFETS
  - R_{DSON} is finite changes with temperature
  - Gates have capacitance and must be driven, hard, to switch correctly

- The MOSFETS are identified as High-side MOSFET and Low-side MOSFET

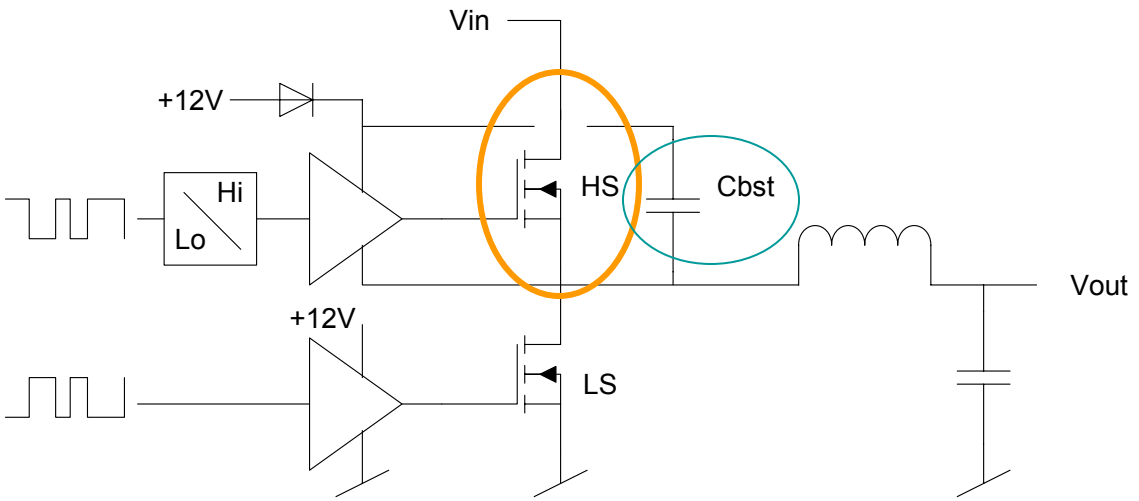


Gate Control (Low Side)



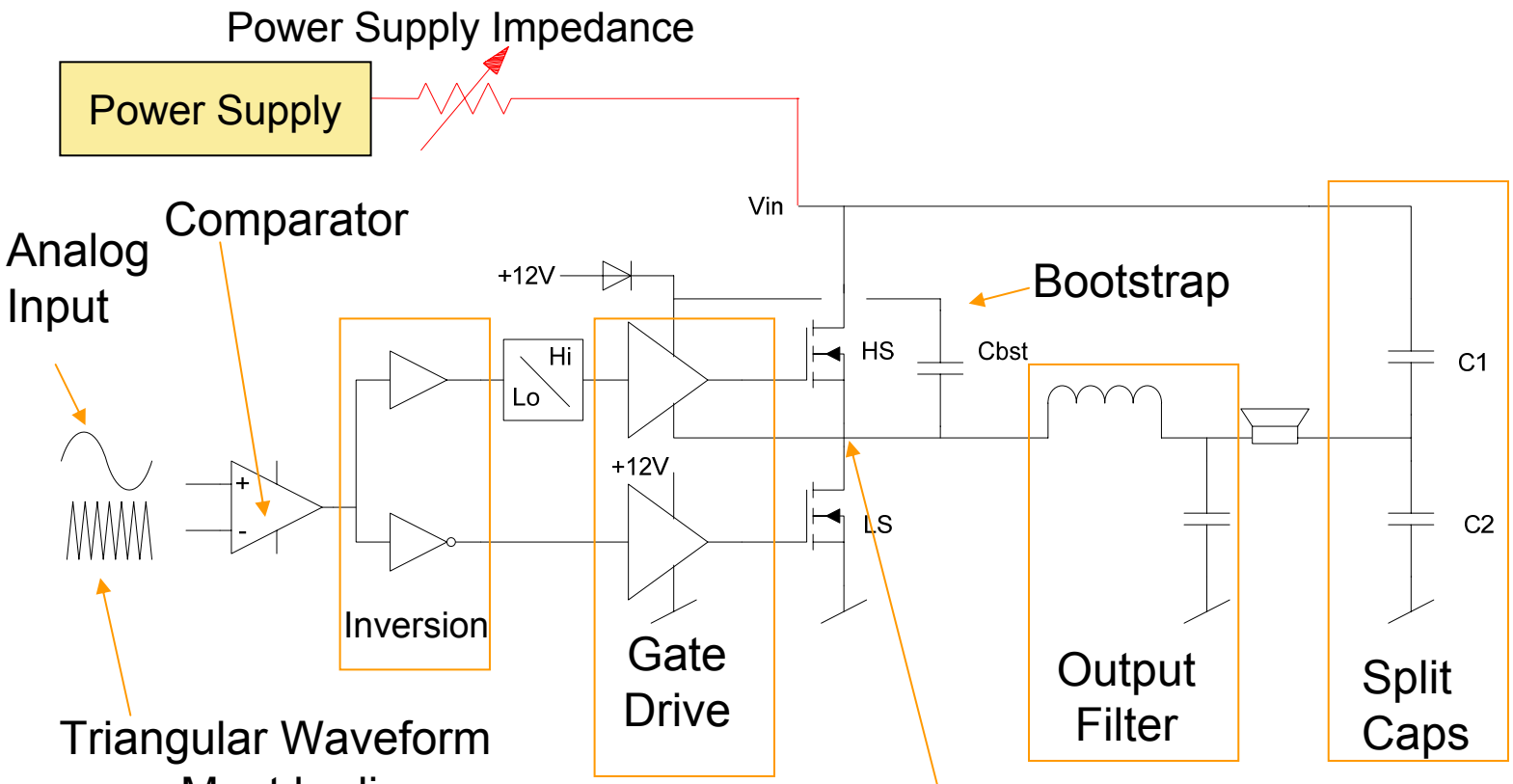
- Control of low-side MOSFET is relatively easy - it is referenced to ground
- Gate drive circuit can therefore be connected directly to the gate

Gate Control (High Side)



- High Side MOSFET is referenced to the PWM output node, and the gate drive circuit must therefore be supplied from a Boot-Strap Capacitor
- Input to the high-side gate driver must be made through a level shifter

Complete Analog Class D Amplifier (in theory)



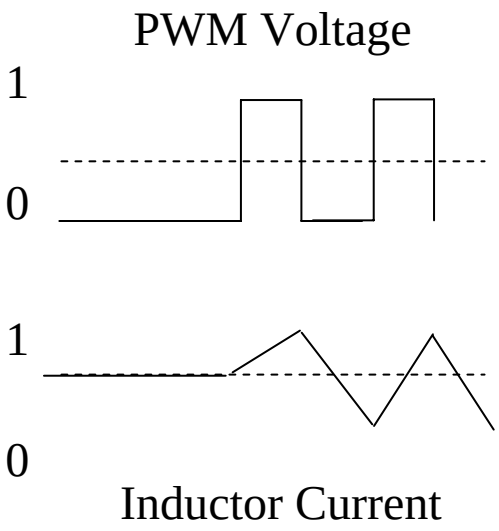
PWM Start and Stop

- Click and Pop occur at start and stop of PWM
- It can consist of DC voltage step and AC voltage ripple
- Best test is a listening test using a system applicable speaker
  - But what speaker and who is listening?
- Listening test is difficult to compare across regions – therefore a standardized test set-up is proposed in SLEA044

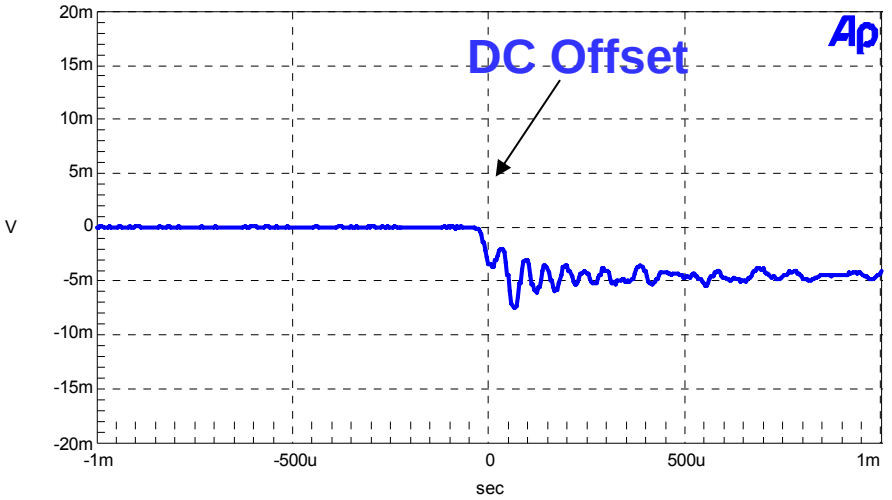
PWM start and stop

Start sequence

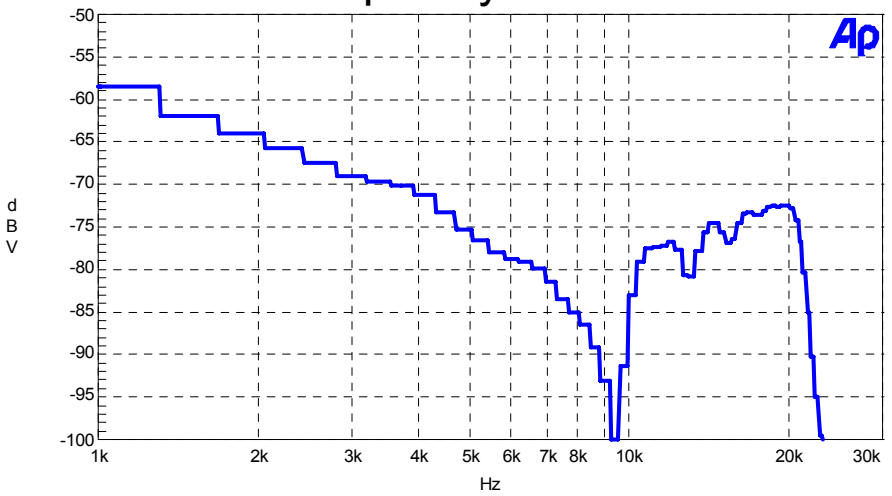
An example



Time Domain



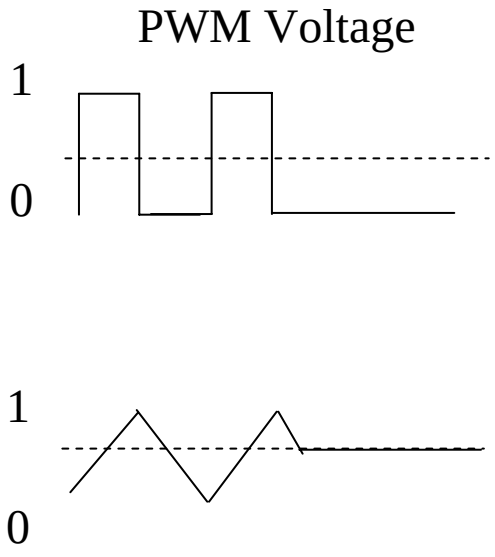
Frequency Domain

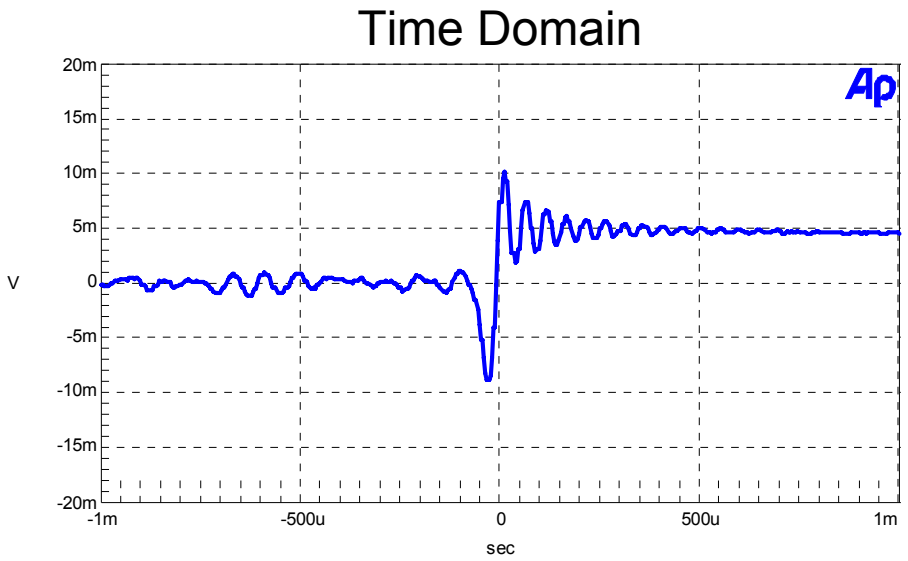


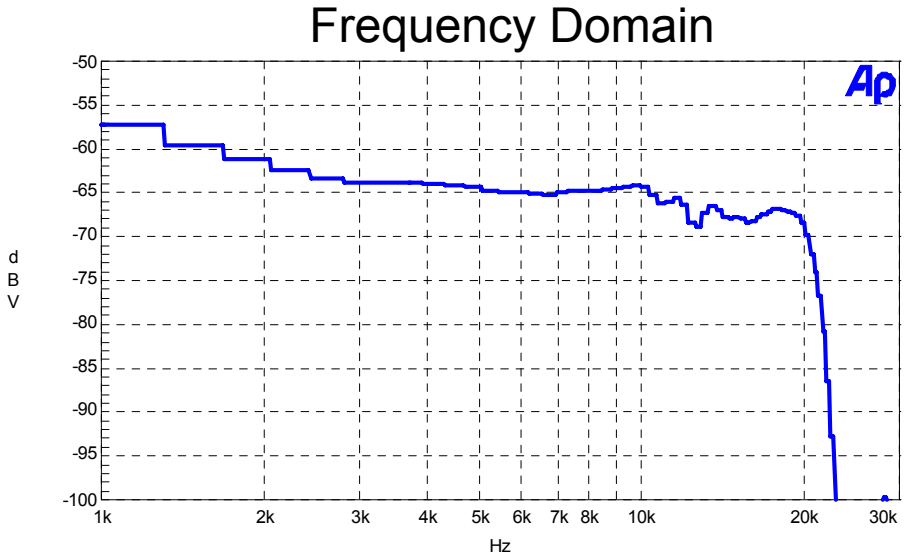
PWM start and stop

Stop sequence

An example

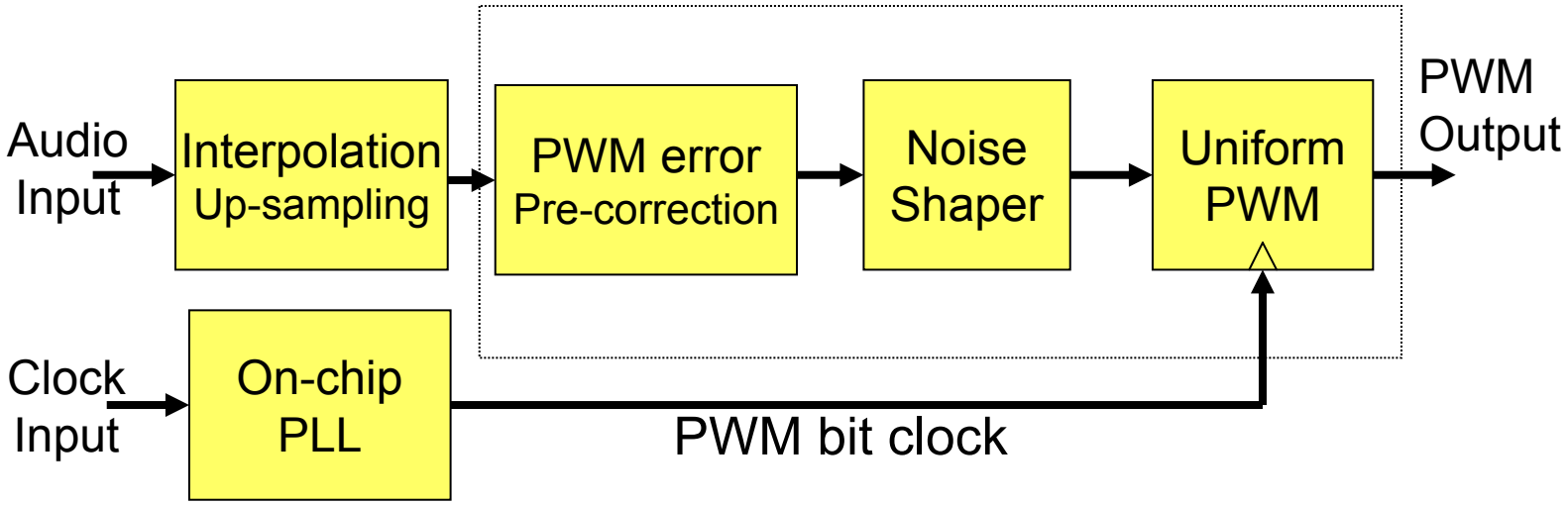






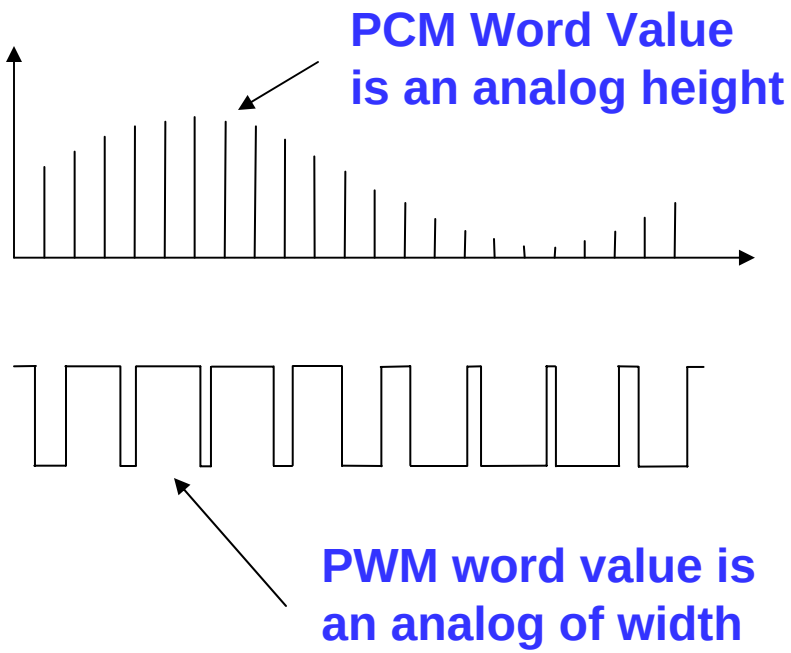
PurePath – Class D goes All Digital

Equibit Processor



PurePath – Class D goes All Digital

- The audio input signal is Digital I2S
- Digital I2S is in Pulse Code Modulation format organized as “words”
- Conversion from PCM to PWM is done in a DSP
- PWM signals controlled be a digital clock
- PWM signal frequency
  8 * 48kHz = 384kHz
- Conversion from PCM to PWM is non-linear and demands pre-compensation



Digital Input Source, I2S

- **Definition from Wikipedia, the free encyclopedia:**
  - **I2S**, or **Inter-IC Sound**, or **Integrated Interchip Sound**, is an electrical serial bus interface standard used for connecting digital audio devices together.
  - It is most commonly used to carry PCM information between the CD transport and the DAC in a CD player.
  - The I2S bus separates clock and data signals, resulting in a very low jitter connection.
  - Jitter can cause distortion and noise in a digital-to-analog converter. The bus consists of at least three lines:
    - BCLK, Bit clock line (64 x Fs)
    - LRCLK, Word clock line (also called word select line) (@ Fs)
    - SDCLK, at least one multiplexed data line

- **For TI PWM modulators, and most DACs and ADCs**
  - MCLK, Master Clock (256 x Fs)

Digital PWM Generator

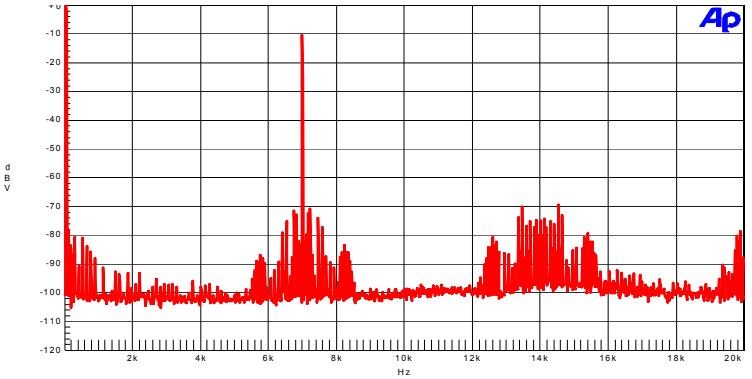
- PWM errors:
  - Harmonic + IM Distortion (rising with signal frequency)
  - Intermodulation noise due to interactions with the noise shaper (we will explain later)

- Errors are corrected by digital signal processing in PCM domain prior to PWM (Equibit® algorithms):
  - Harmonic + IM Distortion
  - Inter-Modulation (IM) Noise
  - Quasi-Symmetry (QS) Noise

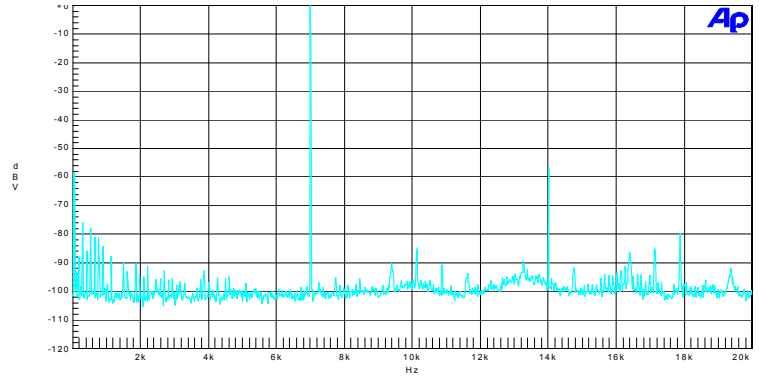
Intermodulation Noise

Intermodulation or **intermod** is the result of two or more signals of different frequencies being mixed together, forming additional signals at frequencies that are not in general at harmonic frequencies (integer multiples) of either.

IM Noise

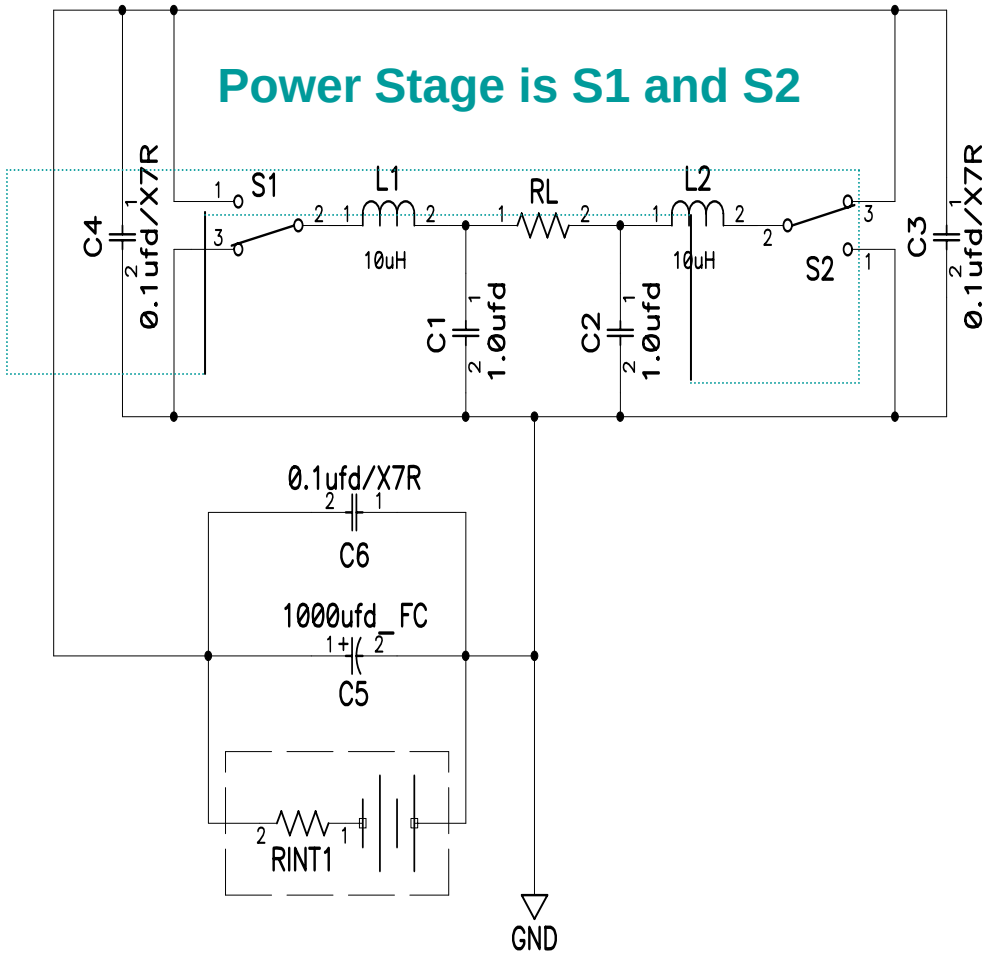


The largest intermodulation products appear at $f_1 + f_2$ or $f_1 - f_2$ (second-order intermodulation), and less so at $2f_1 + f_2$ or $2f_1 - f_2$ (third order intermodulation).



Normal

Simplified Amplifier Diagram



Amplifier Component Considerations

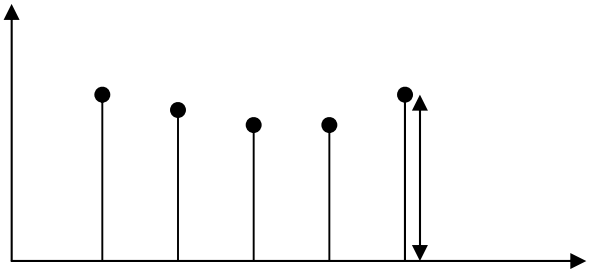
- Choice of components sets the audio performance
- MOSFET Switches (taken care of by the power stage)
- PWM Filter Capacitor (Use a film capacitor)
  - Stability with voltage
  - Ripple Current
- Inductor (Use TI recommended)
  - Series resistance (dc), skin effect (ac)
  - Parallel resistance (hysteresis loss)
  - Parallel capacitance
  - Saturation in core material
- Decoupling capacitor
  - Use X7R
  - Series resistance
  - Series inductance
- Bulk Capacitor
  - Use low ESR
  - ESR
  - ESL
  - Ripple Current
- PSU
  - Output impedance
  - Current limitation
  - Current Slew-rate
  - Surge Capability

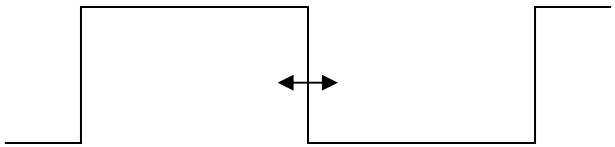
Amplifier Components

- Choice of components sets the audio performance
- MOSFET Switches S1 & S2 (Power Stage)
  - TAS5132, 0W to 25W, 2 Channels
  - TAS5142, 0W to 100W, 2 Channels
  - TAS5152, 0W to 125W, 2 Channels
  - TAS5162, 0W to 210W, 2 Channels
  - TAS5261, 0W to 315W, 1 Channel
  - TAS5186, 210W Total Power, 6 Channel
- Modulators
  - TAS5086, Low cost, 6 Channel
  - TAS5508B, 8 Channel, Feature Rich
  - TAS5518A, 8channel, Feature Rich, High Performance
- PWM Filter Capacitor (Use a film capacitor)
  - Generally .47µ for AD Mode Filter
- PWM Filter Inductor (Use TI recommended)
  - Generally 10µH for f_{PWM} = 384 kHz
- Decoupling capacitors (Use X7R)
  - 0.1µF is a good rule of thumb
  - Select voltage for PVDD + Overshoot + Temperature Derating (ABS Max)
- Bulk Capacitors (Use low ESR)
  - 1000µF Good rule of thumb
  - Select voltage for PVDD + Overshoot + Temperature Derating
- PSU Considerations
  - Output impedance
  - Current limited
  - Current Slew-rate
  - Surge Capability

Clock Requirements

- PCM signals are coded in the sample values
  - CD uses 44.1 kHz sampling with 16 bit resolution
- PWM signals are coded in the pulse width
  - Pulse height is fixed by PSU voltage
  - A Dynamic Range of 110dB demands a clock precision of *10ps* !
- Eliminate jitter with good PCB and circuit design!





Conclusion

- PWM and Class-D amplifiers present new solutions and applications with a rich feature set

- *BUT* this technology also requires a high level of system knowledge in digital and power electronics.

Amplifier Diagram

TAS5504-TAS5122 Example