10 Reasons you should use OMAP3 in your Design

Vaibhav Desai

Texas Instruments

Agenda

1. OMAP3 Offerings - Committed Roadmap, Secure Future
2. Laptop-Like Performance at Handheld Power Levels
3. OMAP35x EVM Tools and Software
4. OMAP35x and Open Source
5. OMAP35x block diagram details
    1. OMAP35x Silicon Platform
    2. Industry first CortexA8/Neon/VFP
    3. SGX – Open GL ES1.1, 2.0, VG
    4. Imaging Video Accelerator inside
6. Performance Benchmarks
7. Packages
    1. Various packaging options
    2. Via Channel™ array technology
8. System solutions with OMAP3
    1. OMAP35x Power and Analog Solutions
9. OMAP35x Connectivity
10. Proven solutions – Archos / Garmin / Always innovating / Palm

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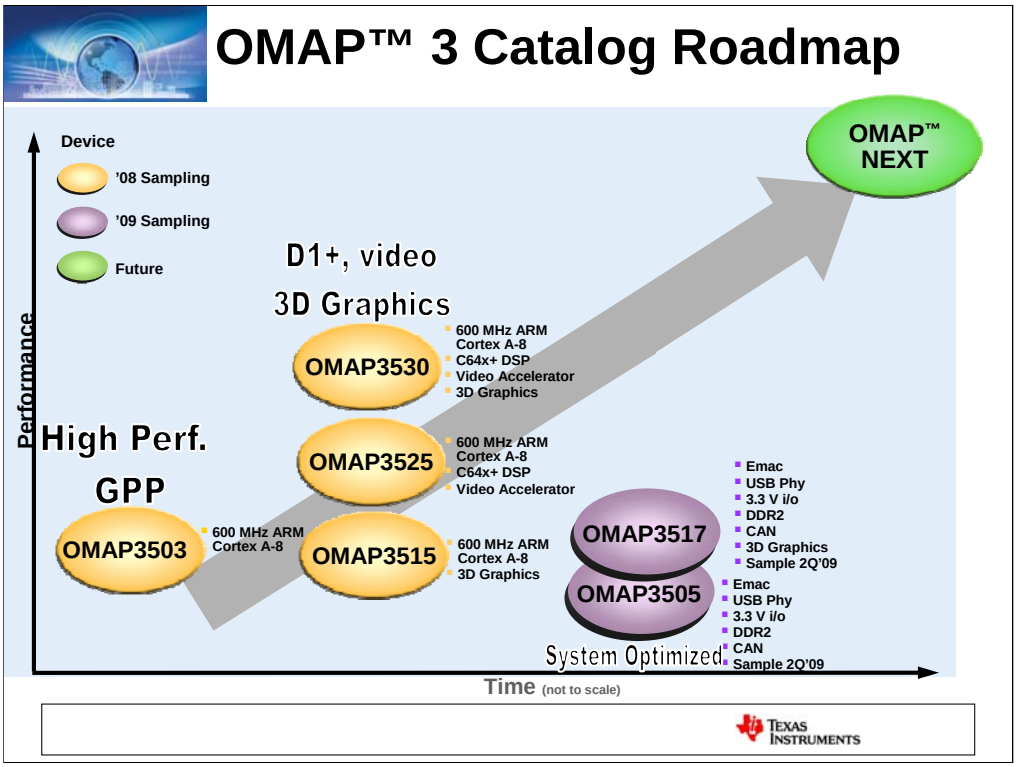


•OMAP3503, 3515, 3525, 3530 are the first in a line of OMAP35x solutions available to the general market

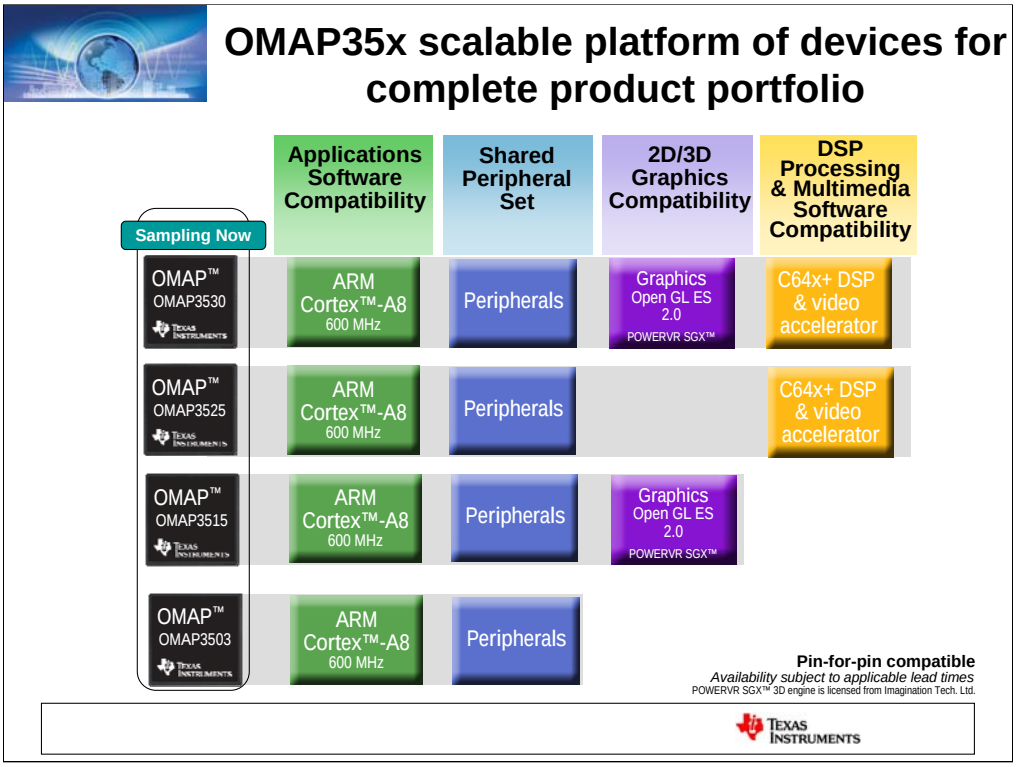
•OMAP3505 and OMAP3517 are targeted to sample in 1Q'09 and include the added features shown. These devices will remain as software compatible and as close to pin compatible as possible given the changes. They will not be 100% pin or software compatible and will not be drop in replacements due to the peripheral changes.

- It is expected that these solutions will offer anywhere from $2-3 in system BOM savings to as much as $9 or $10 depending on the then current memory pricing and additional features utilized

•The OMAP37x devices are planned to sample in 4Q'09. These devices are intended to be drop in compatible with OMAP3503, 3515, 3525, and 3530. THEY ARE NOT DROP IN COMPATIBLE with OMAP3503 and 3517.

- OMAP37x devices will allows customers of OMAP3503, 3515, 3525, and 3530 to easily extend the life of their designs by offering increased performance.

•OMAP NEXT will improve on the performance of the ARM core, increase video performance and add significant peripheral integration for broad markets.



•The OMAP35x platform currently consists of four devices.

•The initially available device was the OMAP3503 which consists of dual issue, superscaler ARM Cortex A8 plus a highly integrated peripheral set.

•The next device in the platform is the OMAP3515 which keeps the same ARM and peripherals and add in an Open GL ES2.0 compatible graphics engine

•The third device in the offering is the OMAP3525 which removes the graphics engine and adds TI's c64x+ DSP and proprietary video accelerators

•The flagship device is the OMAP3530 which integrates all the components shown

•Most importantly all device are pin-to-pin compatible for easy vertical scalability

•All devices are sampling today

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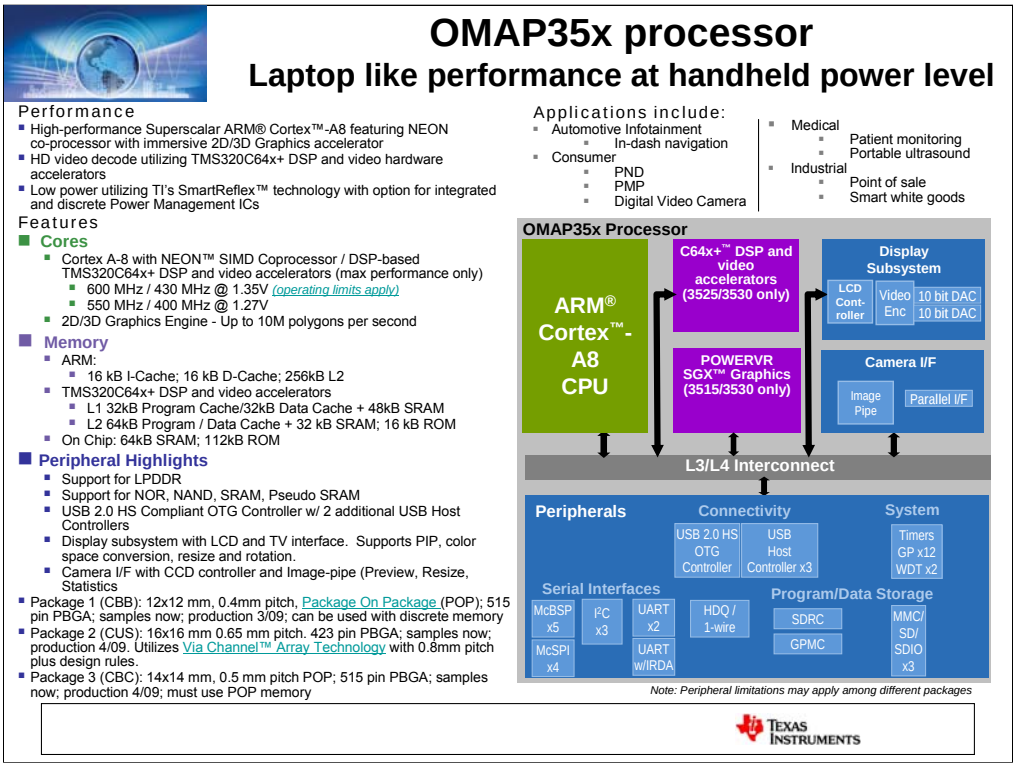
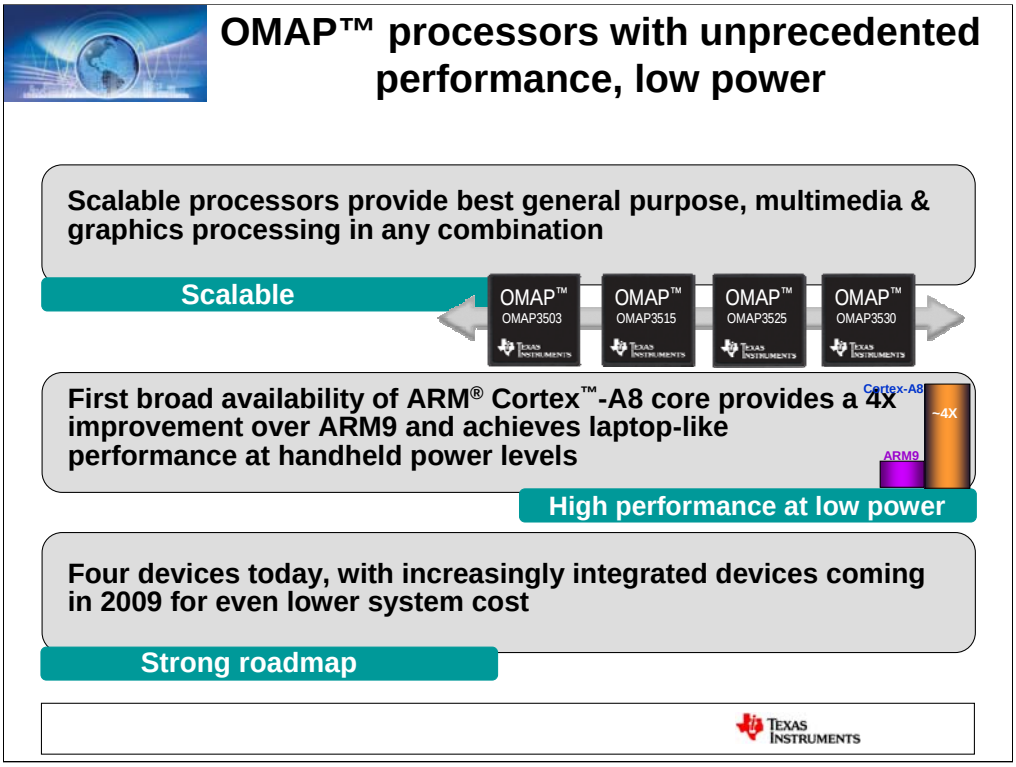


•Notes:

- •Block diagram components are "clickable" to provide additional information on each section
- •It should be stressed to the customer that manufacturing with 0.4mm ball pitch can be very challenging.
- •Customer should discuss with TI before starting a design intending to use 0.4mm and POP



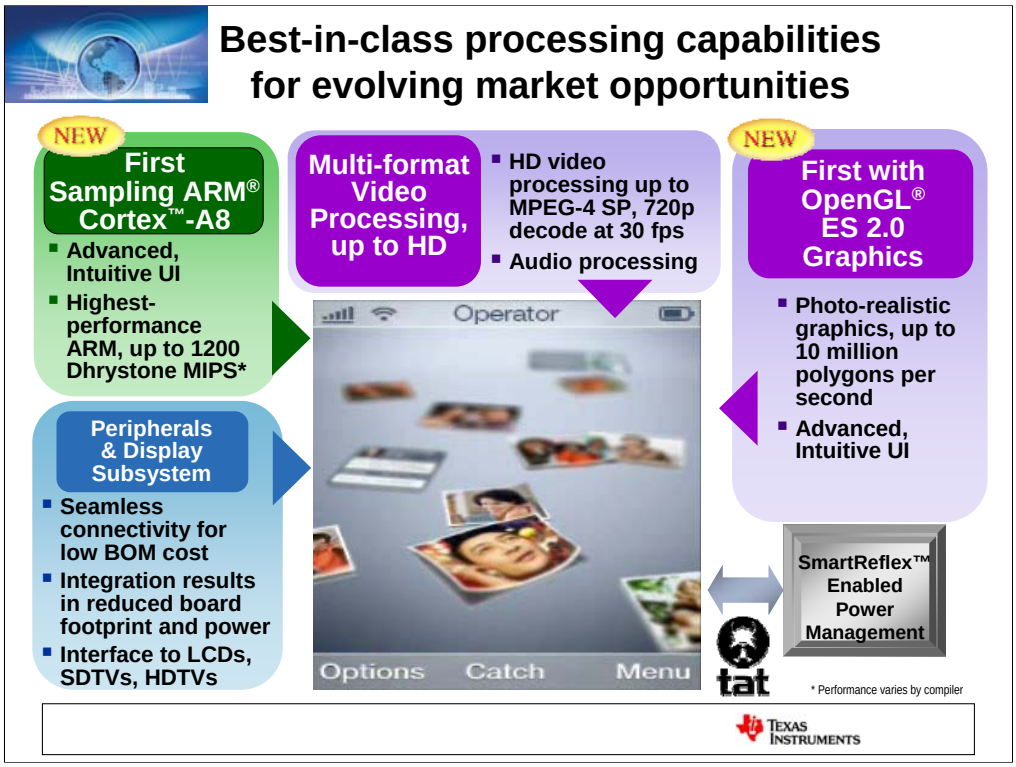
•The OMAP35x platform consists of four devices, the OMAP3503, 3515, 3525, and 3530. Among these four device TI offers very powerful combination of general purpose processing, multimedia, and graphics, in any combination. This overall platform allows scaling to meet just the needs of the product being designed.

•TI has historically been a leader in shipping ARM based solutions to the market. Keeping with this tradition, this is the first broadly available ARM Cortex-A8 offering. The Cortex A8 offers approximately a 4x boost in performance when compared to a 300 MHz ARM 9. 2x is achieved based on increased clock speed and 2x is achieved based on an increase in mips per mhz efficiency.

•When compared to an ARM11 CortexA8 is approximately 2x the efficiency plus any clock speed increase there is.

•While these four devices are extremely competitive, they are just the beginning. Our roadmap devices are already in the works for release in 2009 and include things like emac, 3.3V IO and more.

•Samples of the OMAP35x are available today as well as the OMAP35x EVM.



•OMAP35x brings together the capability to have very high performance general purpose processing, video / multimedia processing, graphics acceleration, and a highly integrated peripheral set all in one very small package.

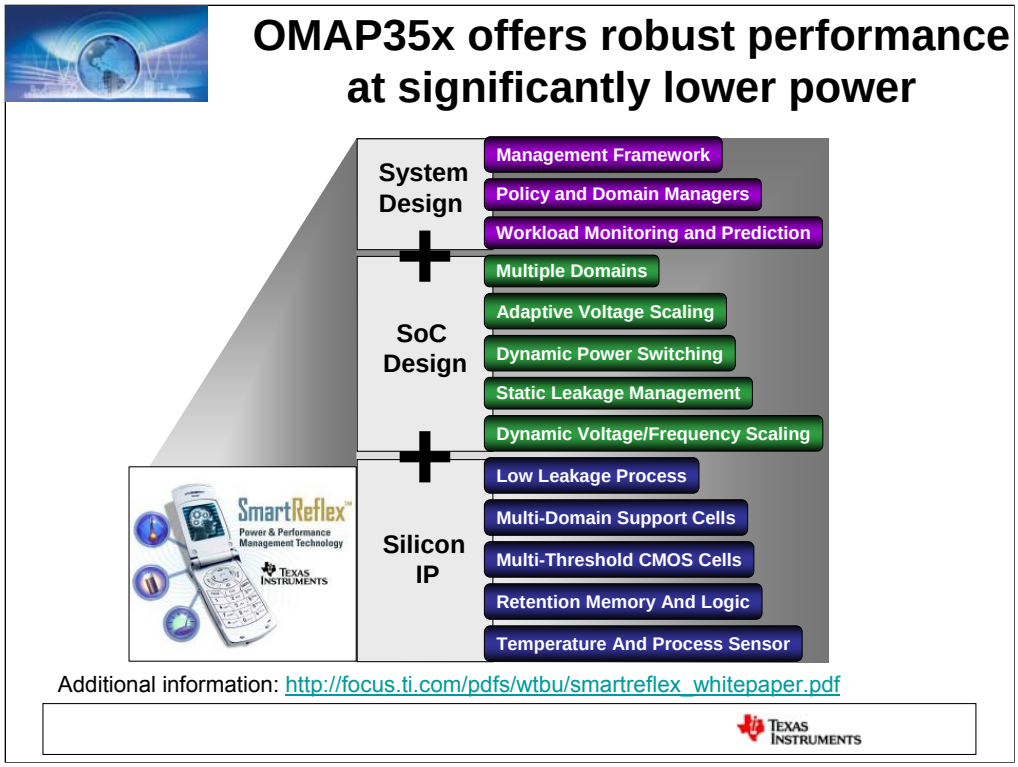
•OMAP35x offers the first generally available CortexA8 solution. It achieves up to 1200 DMIPS and is roughly 4x the performance of an ARM9.

•Enabled along side this core is the c64x+ based video subsystem is capable of processing up to 720 HD resolution video.

•This release of PowerVR SGX graphics accelerator marks the first time an integrated, SOC embedded solution has had OpenGLES2.0 compatibility included in hardware. This is capable of running up to 10 M polygons per second.

•The highly integrated peripheral set includes many system level components that will reduce the overall BOM and PCB size

•All of this combined with TI's Smartreflex power saving technology provide an optimal blend of performance, power, and integration.

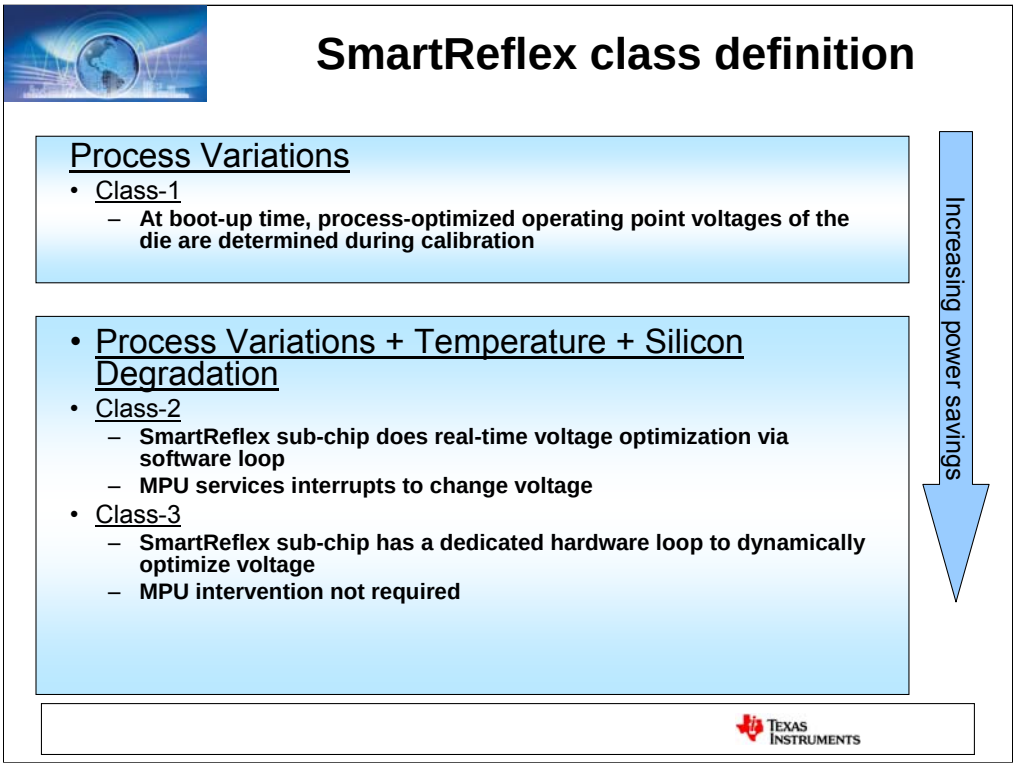


•TI's Smartreflex technology enables TI silicon to operate at low power levels while still being manufactured in increasingly smaller, and "leakier", process technologies

•This technology allows for a system to dynamically compensate for variations in temperature, manufacturing process, and silicon degradation over time to reduce voltage, gate off unused peripherals, and adjust clocks as needed all to lower power consumption.

•Three vectors are required to enable this:

- •Silicon IP
- •SoC (System on a chip) design
- •System design



•Before reviewing companion power offerings from TI it is important to understand some basic definitions associated with Smartreflex

•The “class” associated with a companion power devices identifies to what extent Smartreflex technology can be uses

•There are three classes relative to OMAP35x

•Power savings increase with each subsequently higher class

•Class 1 and Class 2 are software based

•Class 3 is hardware based

Power Management

Goal: Improve equipment's battery life

Minimize power consumed + Guarantee system performance

- Active power consumption & Processing is on-going
- Dynamic power consumption (transistor switching) + Leakage consumption
- Managed by
  - **Dynamic Voltage & Frequency Scaling (DVFS)**: Consume less energy/power in low performance modes by lowering the voltage
  - **Adaptive Voltage Scaling (AVS)**: Lower voltages when the chip process and temperature allow it – technically this is SmartReflex, but the SmartReflex name is commonly used to refer to all power savings techniques listed
  - **Dynamic Power Switching (DPS)**: Splits chip into several power domains that can be put into low power states individually.

$$P_{Dynamic} \alpha C \times V^2 \times f$$

$$P_{Leakage} \alpha V \times I_{Leakage}(V, Temp, Process)$$

Static (also Standby or Idle) power consumption

- Limited/no processing on-going, system awaiting wak
- Very limited dynamic power consumption + Leakage consumption
- **Static Leakage Management (SLM)**: Device switches into low-power system modes automatically or under user requests when no application is running

- OMAP35xx power saving features:
  - Multiple voltage, power, and clock domains
  - 5 Operating Power Points (OPP)
  - Smart Reflex for dynamic voltage scaling without CPU involvement

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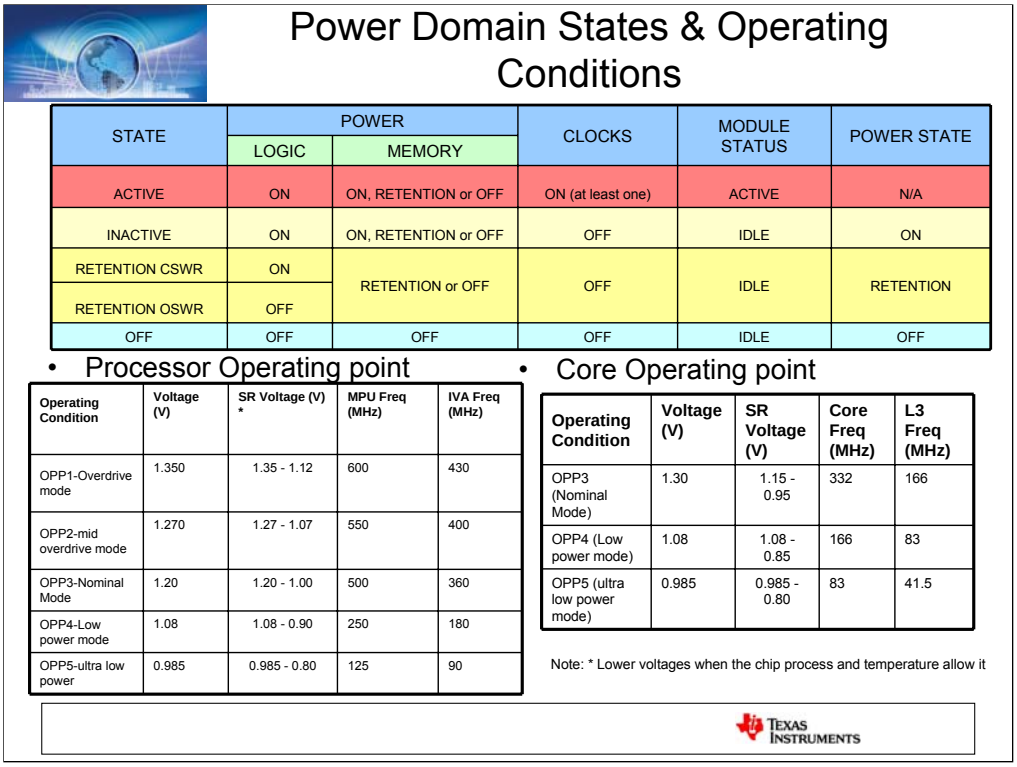
Power domains

OMAP3 is divided into 16 power domains:

- 9 power domains with power switches directly controllable by registers:
  - MPU (Ferrari processor domain)
  - NEON (Ferrari multimedia coprocessor domain)
  - IVA (Audio Video processor domain)
  - GFX (3D graphics engine domain)
  - CORE (Interconnect, memory controllers, peripherals and clock management domain)
  - DSS (Display domain)
  - CAM (Camera controller domain)
  - PER (Low power uses cases peripherals domain)
  - EMU (Emulation domain)

- 5 power domains with power switches not directly controllable by registers:
  DPLL1 (MPU DPLL domain), DPLL2 (IVA DPLL domain), DPLL3 (CORE DPLL domain), DPLL4 (Peripherals DPLL domain) and SR (SmartReflex engine domain)

- 2 "*power domains*" which are always on:
  - WKUP (Wakeup domain)
  - EFUSE (eFuses farm domain)



Power Domain States & Operating Conditions

STATE	POWER		CLOCKS	MODULE STATUS	POWER STATE
	LOGIC	MEMORY			
ACTIVE	ON	ON, RETENTION or OFF	ON (at least one)	ACTIVE	N/A
INACTIVE	ON	ON, RETENTION or OFF	OFF	IDLE	ON
RETENTION CSWR	ON	RETENTION or OFF	OFF	IDLE	RETENTION
RETENTION OSWR	OFF				
OFF	OFF	OFF	OFF	IDLE	OFF

- Processor Operating point

Operating Condition	Voltage (V)	SR Voltage (V) *	MPU Freq (MHz)	IVA Freq (MHz)
OPP1-Overdrive mode	1.350	1.35 - 1.12	600	430
OPP2-mid overdrive mode	1.270	1.27 - 1.07	550	400
OPP3-Nominal Mode	1.20	1.20 - 1.00	500	360
OPP4-Low power mode	1.08	1.08 - 0.90	250	180
OPP5-ultra low power	0.985	0.985 - 0.80	125	90

- Core Operating point

Operating Condition	Voltage (V)	SR Voltage (V)	Core Freq (MHz)	L3 Freq (MHz)
OPP3 (Nominal Mode)	1.30	1.15 - 0.95	332	166
OPP4 (Low power mode)	1.08	1.08 - 0.85	166	83
OPP5 (ultra low power mode)	0.985	0.985 - 0.80	83	41.5

Note: * Lower voltages when the chip process and temperature allow it

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POWER STATE – Setting in the PM_PWSTCTRL_<domain>.POWERSTATE bit field

Closed Switch Retention (CSWR)

- Domain logic supply is maintained, therefore logic retained
- Logic supply voltage can be lowered to minimize leakage
- Domain memories can be retained or switched off

Open Switch Retention (OSWR)

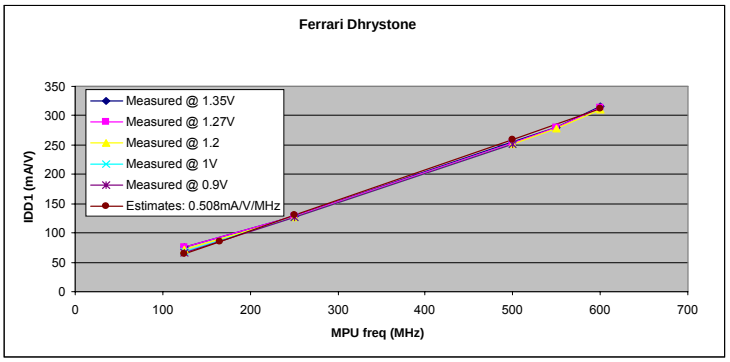
- Domain logic switched off, but context saved in Retention Flip Flops (RFFs) in some modules
- Domain memories can be retained or switched off
- Supported by MPU, CORE (and IVA2 for devices with this features) power domains only

MPU Power Consumption

Silicon Measurements	Conditions
0.520mA/MHz/V	CortexA8 Branch Prediction enabled Laboratory Temperature Dhrystone running in infinite loop built with ARM tools

Estimates

0.508mA/MHz/V



IVA2: H.264 D1 Encode

Silicon Measurements	Conditions
0.365mA/MHz/V	**Video encoding performed by IVA2 + HWA** • Video: H.264 D1 (2 YUVP 420 frames encoded) • H.264 Codec developed by TI & released the 5th of Jan 2007 • HWA: iME, iLF, iVLCD • Power Domains states: MPU/NEON OFF – IVA2 ACTIVE

Results

VDD1 (V)	IVA2.CLK (MHz)	IDD1 (mA)
1.2	360	196
1.2	430	227.6
1.2	520	266.1
1.35	520	298.6

Avg:

508mA peak @ 520MHz (1.35V)

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Power consumption Summary

Use case	PROC OPP	CORE OPP	Power Mgmt Mechanism	Measured	Estimates	Power Rails	Note
AVC Encode	OPP3	OPP3	DVFS & Smart Reflex	305.2mW	641mW	VDD1+VDD2	VGA (MPEG4, 1.341Mbps), mp3 44.1kHz @ 128kbps
Dhrystone	OPP3	OPP3	none	363mW	366mW	VDD1	MPU only
H.264 Encode	OPP3	OPP3	none	235mW	235mW	VDD1	D1 (2 frames), IVA2 only
LPR	OPP3	OPP3	Static Leakage Mgmt	33mW	35mW	All	QVGA, MPU in OFF mode
MP3LP	OPP1	OPP2	DVFS + Static Leakage Mgmt	22mW	28mW	VDD1+VDD2	CORE in CSWR, IVA2 based frame per frame Decoding
MP3LP	OPP1	OPP2	DVFS + Static Leakage Mgmt	41.65mW		VDD1+VDD2	ARM based frame per frame Decoding
STDBY1	0.9V, no clock		Static Leakage Mgmt	7mW	14mW	VDD1..5	Every PD in CSWR
STDBY2	0.9V, no clock		Static Leakage Mgmt	4mW	8mW	VDD1..5	MCU & CORE in CSWR
STDBY3	0.9V, no clock		Static Leakage Mgmt	1.5mW	1.4mW	VDD1..5	CORE in OSWR, other OFF
STDBY4	0.9V, no clock		Static Leakage Mgmt	1.5mW	1.4mW	VDD1..5	Every PD in OFF
OFF Mode	0V, no clock		Static Leakage Mgmt	0.477mW	0.340mW	All	

Conclusion

- OFF mode leakage above expectation for two reasons: Extra IO leakage linked to an isolation issue of some IO cells (fixed on ES3) & WKUP_BG over-consumption
- Global CORE leakage observed on Hot-Hot Material is within range of expectation.
- Dynamic power figures are aligned with estimations for both low power & high power use cases.

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Begin development today with extensible OMAP35x evaluation module

Hardware

- OMAP35x Processor for evaluating all four OMAP35x devices
- 128 MB LPDDR/128 MB oneNAND Flash (or similar capacity and function)
- Touch screen LCD display
- Landscape/Portrait modes

Software

- OMAP35x Linux BSP:
  - Kernel 2.6.26
  - Peripheral drivers
  - U-boot for boot loading
  - Busybox based root file system
- Windows® CE 6.0 BSP available now

[1] *Additional tools support from Microsoft, ARM, GreenHills, Lauterbach, and TI(CCS) will be made available in the future*

- **Evaluate capability**
- **Begin SW development**
- **Use Daughter card expansion to prototype complete system**
- **Easy to Upgrade to New Processors and Power Management Devices**

More information available at
www.ti.com/omap35x

Connectivity

- Daughter card connectivity
- Ethernet, USB 2.0, SDIO, I²C, JTAG, Keypad
- SD/MMC
- S-Video output

Development tools and support[1]

- Code Sourcery Toolchain
- Reference schematics
- Emulator support: TI XDS560

OMAP35x EVM
TMDXEVM3503
$1495

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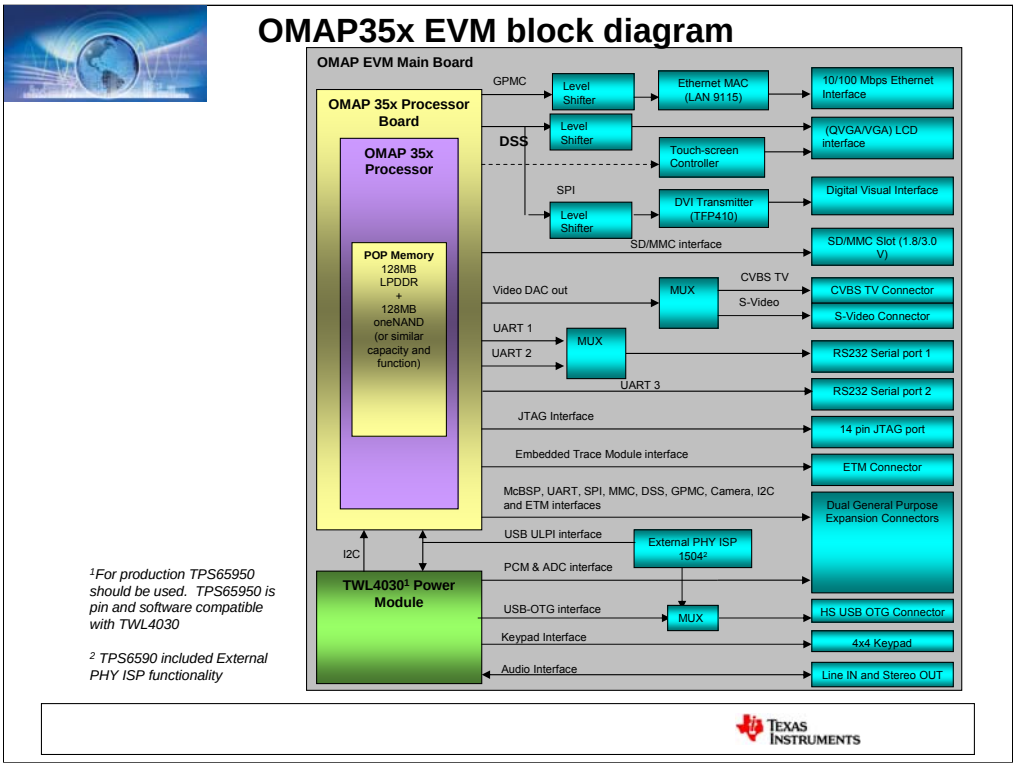
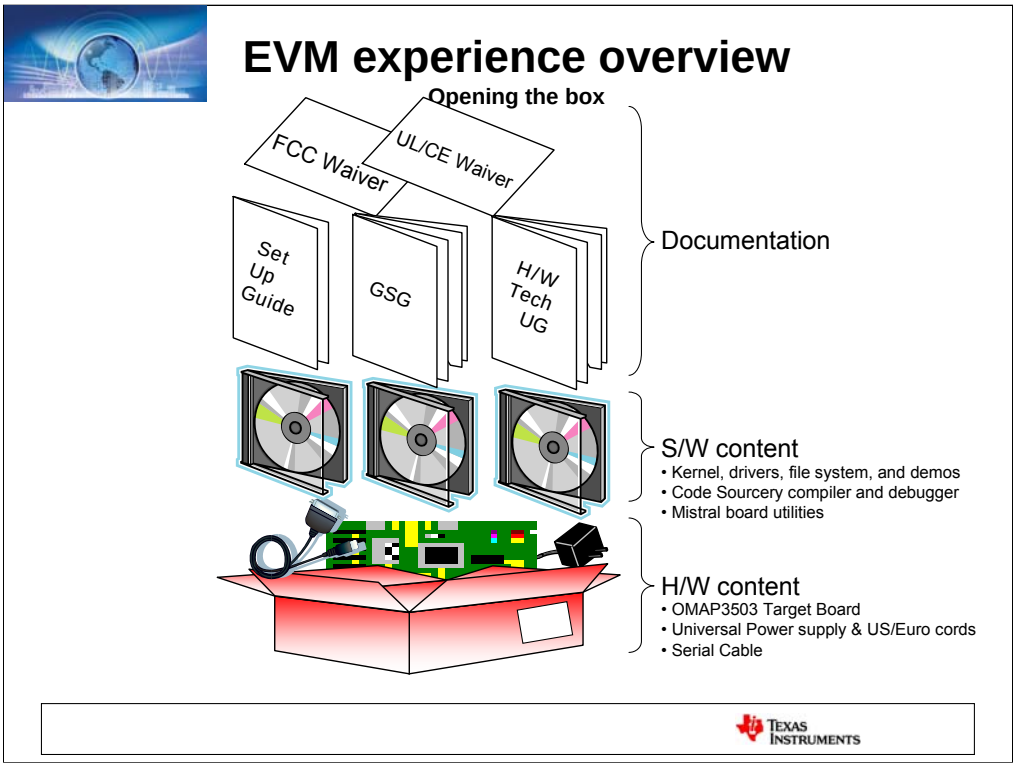
- To facilitate rapid development TI is offering the OMAP35x EVM.
- This board is based on OMAP35x silicon and includes a VGA touch screen LCD and 128 MB of LPDDR and 128 MB of oneNAND memory (utilizes POP technology) – memory may be second sourced over time, but this is the minimum capacity that will be offered
- The EVM is shipping today and includes non commercial Linux OS and drivers along with Code Sourcery tools.
- Reference schematics and Gerbers are available
- This board can be used to evaluate OMAP3503, OMAP3515, OMAP3525, and OMAP3530 silicon
- Additionally WinCE will be made available via software download
- The basic OS and drivers for WinCE, when available, and Linux are offered in source code. No additional licensing fee or royalty is required to TI for use of the code (WinCE requires MSFT license)



•The OMAP35x EVM is based on a three boards to allow easy upgrading and development of power management solutions

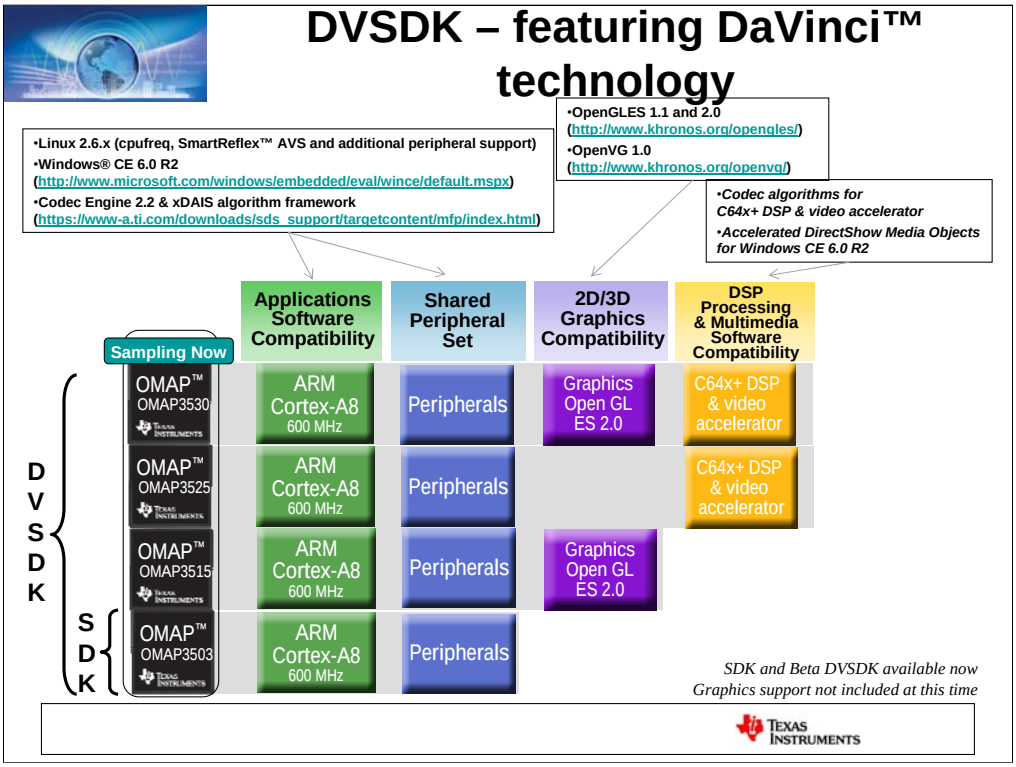
- •The base board, shown in gray, contains all the peripherals, expansion connectors, etc.
- •Connected to this is a processor board shown in yellow. This includes the OMAP35x device (0.4mm pitch) and stacked, POP memory
- •The third board is the power management board. This board is based on the TWL4030 device. TWL4030 is a preproduction device to the TPS65950. TPS65950 is pin and software compatible with the TWL4030



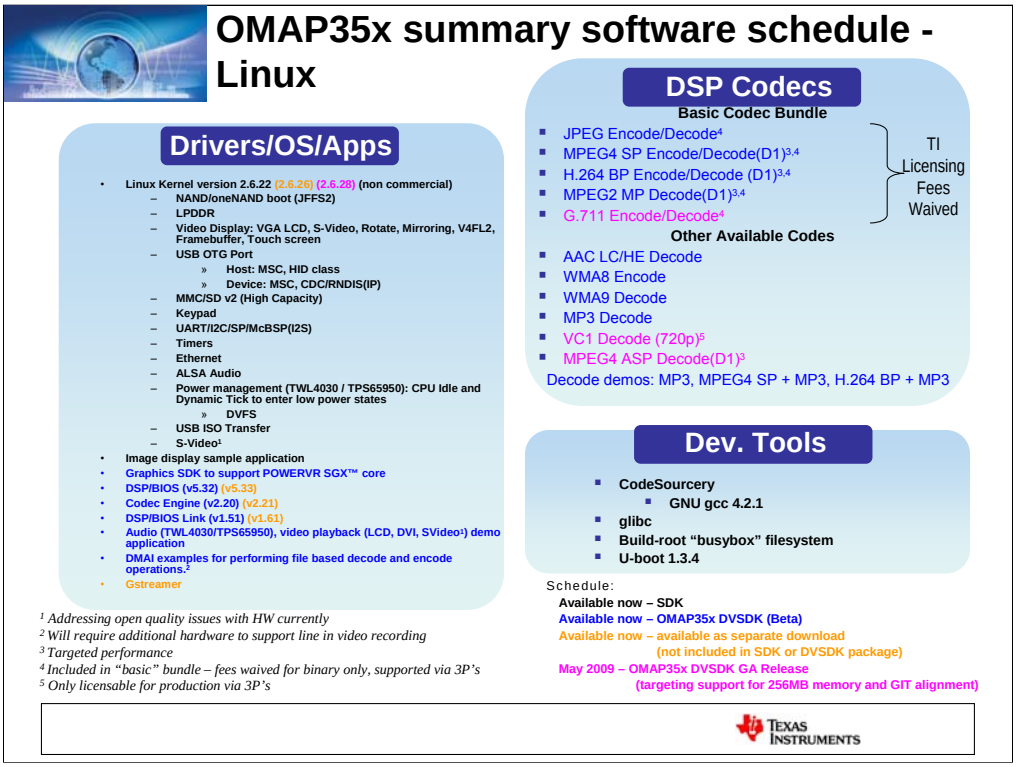
•This is a high level summary of what will be included in OMAP35x EVM

•All software and documentation will be available on the EVM update site.

•It is important that customers register their EVM and download the latest update when getting started



•The available SDK covers the ARM and peripheral drivers only but is usable across all devices.
•The DVSDK featuring DaVinci technology enables video on the OMAP3530 and OMAP3525 and supports all four devices in the platform.
•The DVSDK extends the current Linux support that is included in the SDK
- It will also add in support for WinCE 6.0 SR2
- It is based on Codec Engine 2.2 and utilize our standard API libraries for enabling algorithms



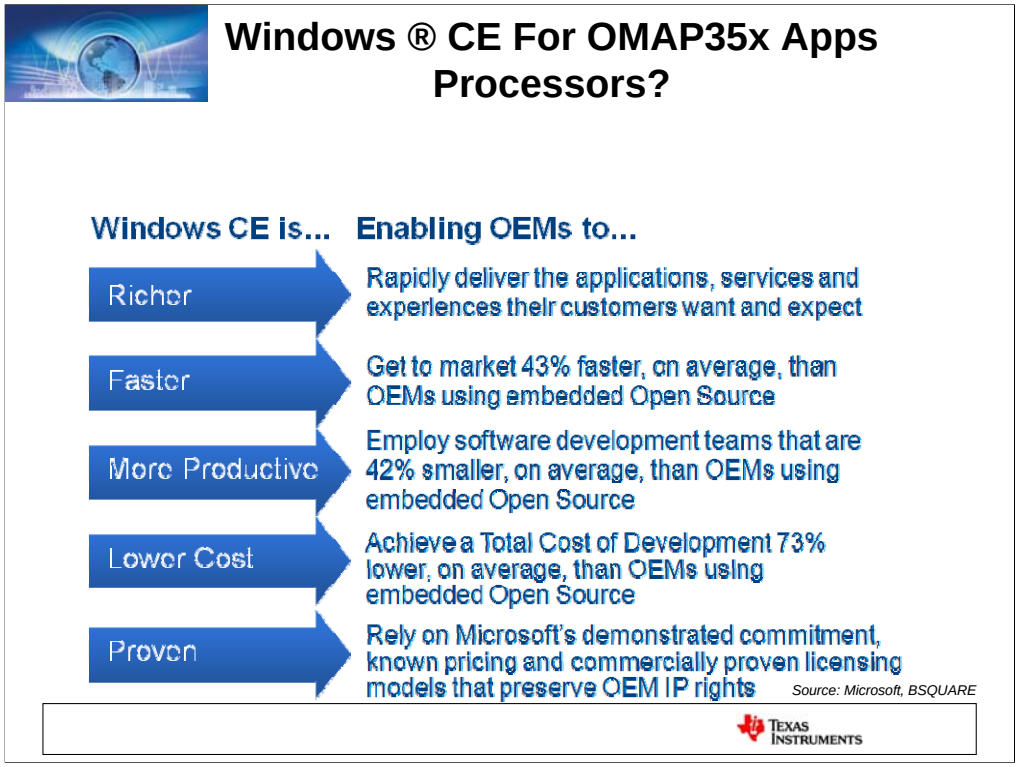
•This slide provides additional granularity on the codecs that are included in the DVSDK as well as drivers, OS, etc.

•All codecs will be included for evaluation use as part of the DVSDK EVM package. Production licensing for codecs are available electronically via TI. For fees to be waived, the electronic licenses must be accepted as is. Any negotiation of licenses will reinstate the applicable license fees.

Notes

•Profile support:

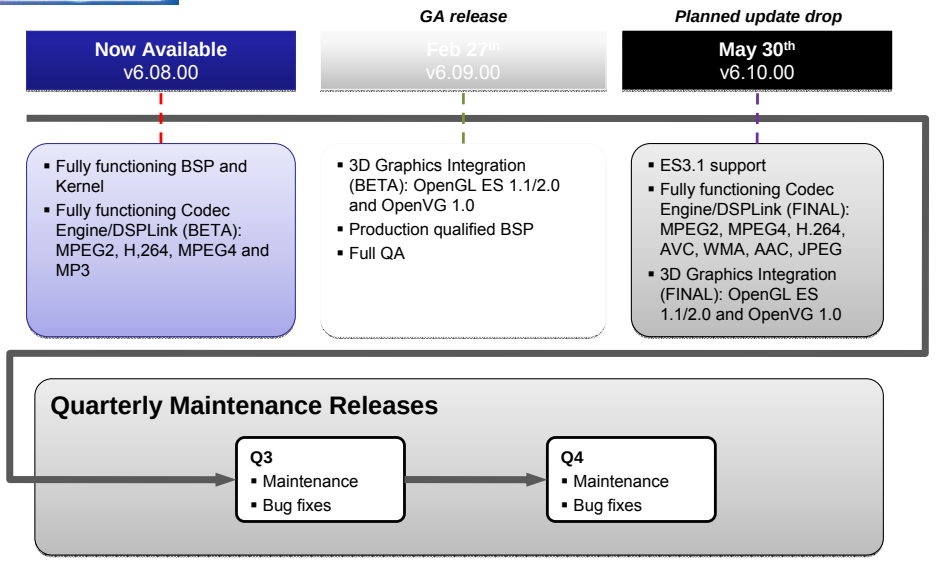
- H.264 BP – baseline profile, primarily for lower-cost applications with limited computing resources, this profile is used widely in videoconferencing and mobile applications



Keywords

WinCE, Windows CE, Windows Embedded, WindowsCE, BSQUARE

OMAP3 WINCE BSP 2009 RELEASE PLAN



** For a full itemize list of each deliverable, see the WinCE BSP Feature list*

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OMAP35x Windows® CE 6.0 DVSDK Overview

TI / BSQUARE's Windows CE 6.0 R2 BSP is a free, source code offering included in the OMAP35x WinCE DVSDK for the TI OMAP35x Evaluation Module (EVM) that helps customers get to market faster with Windows CE O/S based product based on OMAP35x application processor.

Windows CE by bSQUARE

http://www.bsquare.com/omap3/

EVM

- ✓ Hardware based on OMAP3530
- ✓ Features Cortex™-A8 running at 600MHz
- ✓ VGA on-board display with additional DVI and S-Video ports
- ✓ Contains 128 MB LPDDR/128 MB Micron Flash or similar capacity and function
- ✓ Includes touch screen LCD display with landscape/portrait modes
- ✓ Expansion connector provides flexible interface capability

DVSDK

- ✓ Base, tested BSP available now
- ✓ Features DirectShow Filter integration
- ✓ Contains Codec Engine and DSPLink for utilization of DSP and video accelerators inside WinCE – Q1'09
- ✓ Full OMAP35x peripheral support
- ✓ DVI and S-Video support
- ✓ Comprehensive "Welcome Tour" on-screen guide written in Flash
- ✓ Adobe® Flash® Lite™ 3.1 support*
- ✓ POWERVR SGX™ support for high-end graphics capabilities – Q1'09

To get started:

•Get the OMAP35x EVM: www.ti.com/omapdevtools

•Register the board (instructions are in the box)

•Access the Windows CE Demo or Windows CE DVSDK through www.ti.com/omapsoftwareupdates starting November 3

**Available for purchase from BSQUARE*

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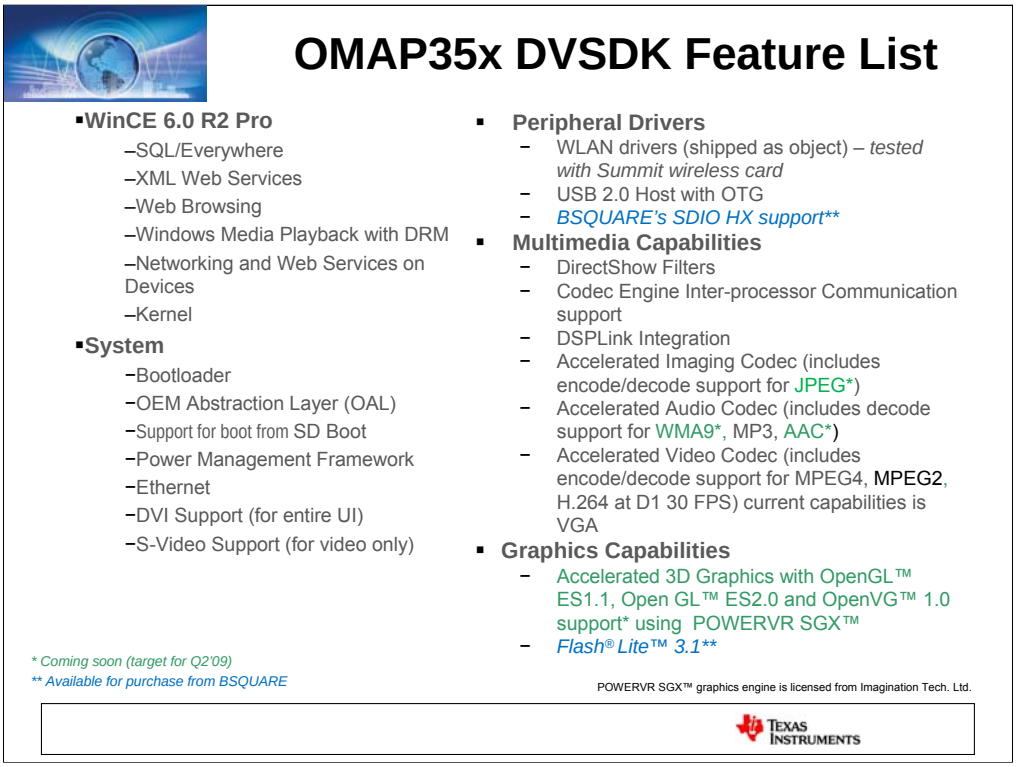
Keywords

WinCE, Windows CE, Windows Embedded, WindowsCE, BSQUARE



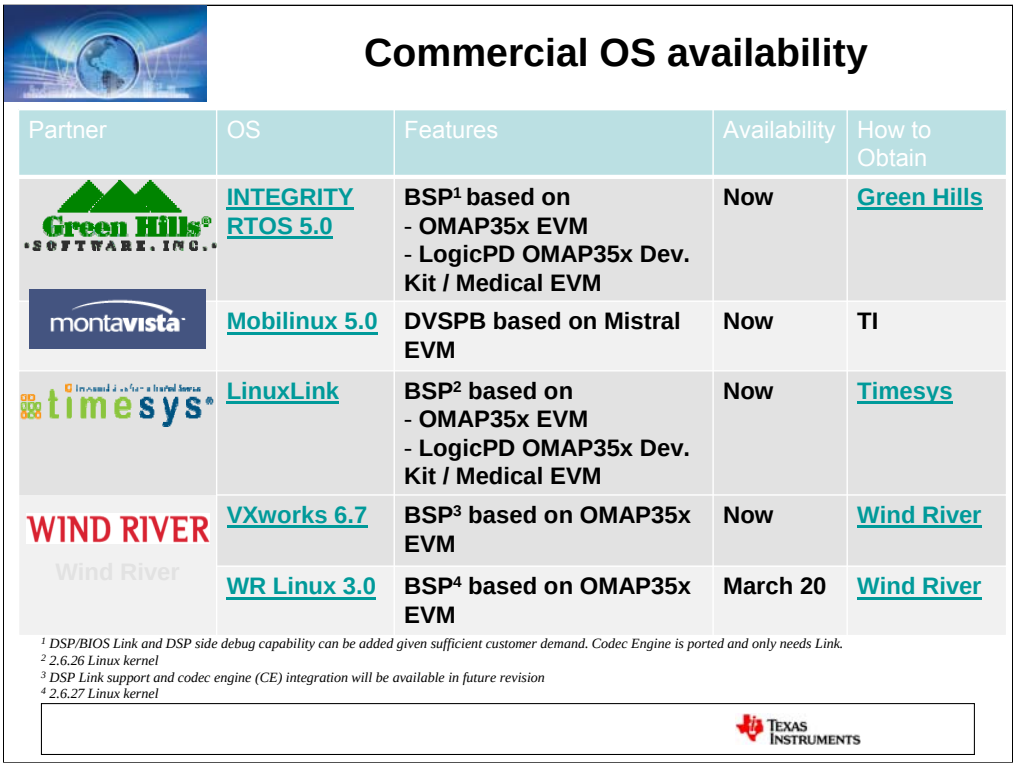
•bSquare will be using the Summit Wireless Radio SDC-MCF10G for the WLAN Drivers

•More info on it can be found here: http://www.summitdatacom.com/product_specs/SDC-MCF10G.html.

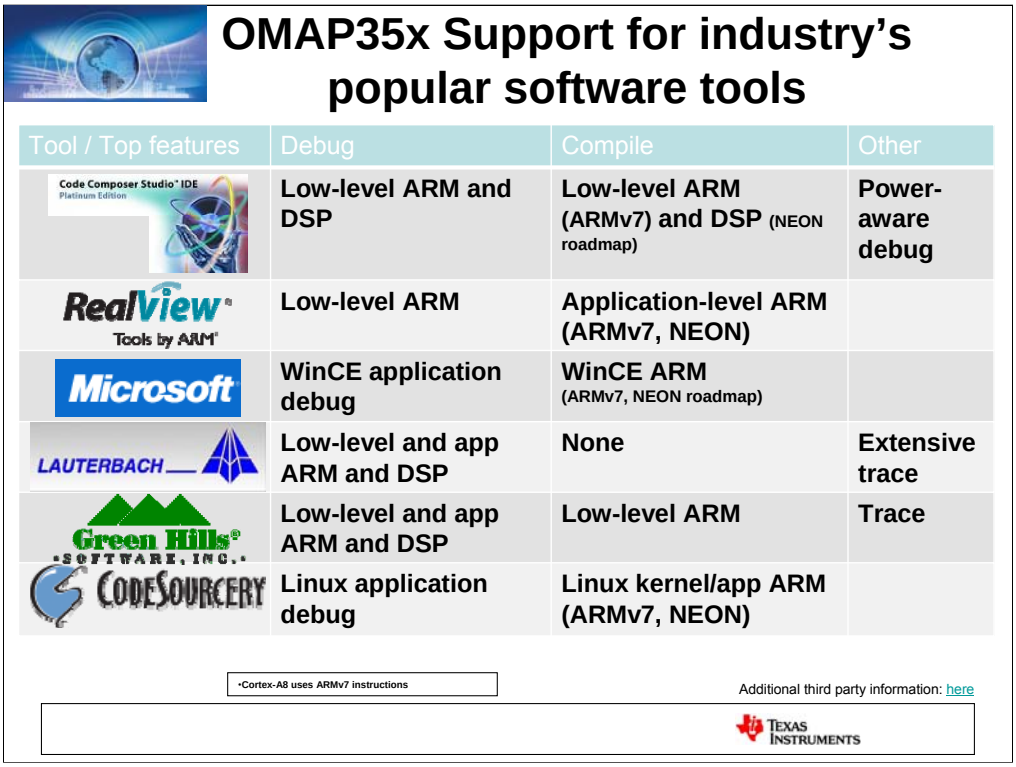
•They are projecting an average Wi-Fi performance throughput range up to 15MBps.

Keywords

WinCE, Windows CE, Windows Embedded, WindowsCE, BSQUARE



This slide shows the Commercial OS availability for OMAP35x. Depending on your needs any one of these partners will be able to supply the listed commercial OS.

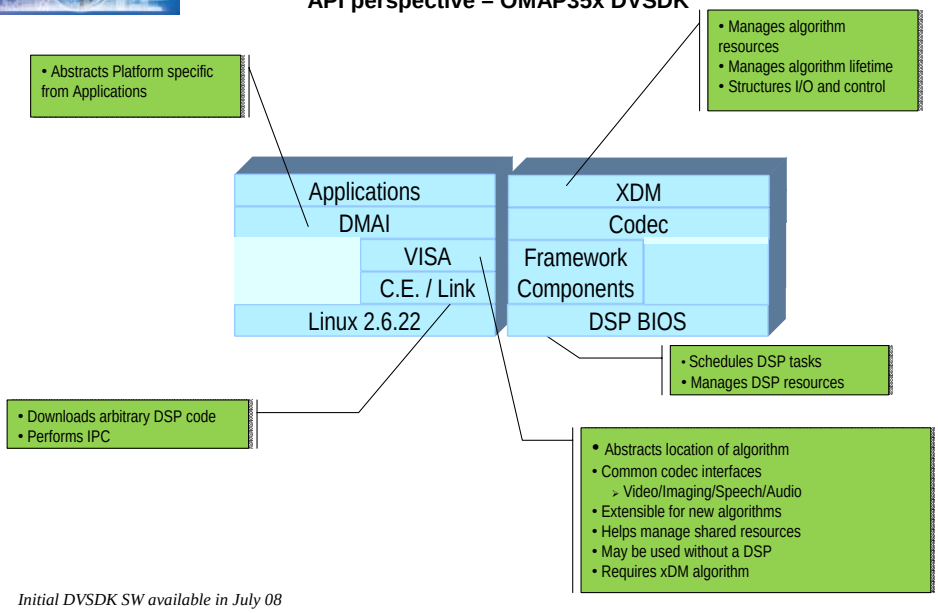


•TI's initial software includes CodeSourcery tools

•Other tools vendors support is either available or in progress

Overview of SW stacks

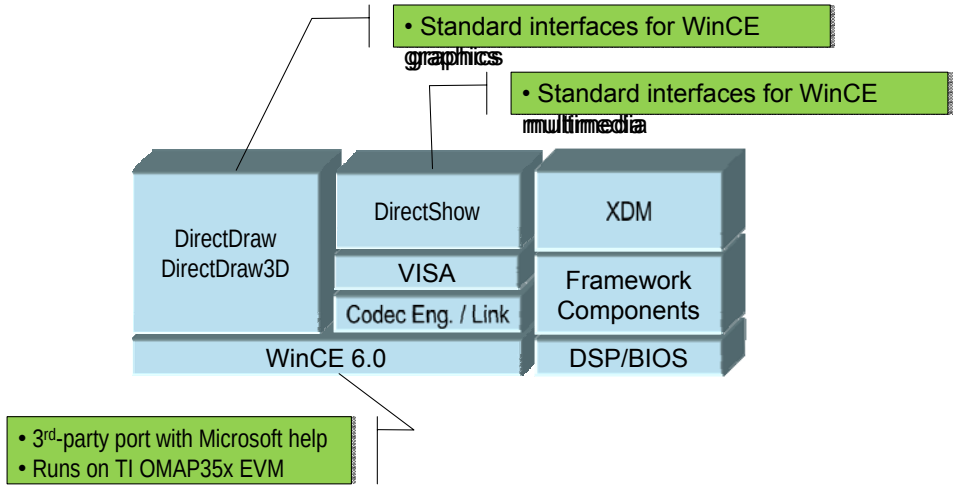
API perspective – OMAP35x DVSDK



Initial DVSDK SW available in July 08

Overview of SW stacks

API perspective - WinCE



Codec and applications blocks omitted for simplicity

Agenda

1. OMAP3 Offerings - Committed Roadmap, Secure Future
    1. Catalog Processors Introduction
2. Laptop-Like Performance at Handheld Power Levels
3. OMAP35x EVM Tools and Software
4. OMAP35x and Open Source
5. OMAP35x block diagram details
    1. OMAP35x Silicon Platform
    2. Industry first CortexA8/Neon/VFP
    3. SGX – Open GL ES1.1, 2.0, VG
    4. Imaging Video Accelerator inside
6. Performance Benchmarks
7. Packages
    1. Various packaging options
    2. Via Channel™ array technology
8. System solutions with OMAP3
    1. OMAP35x Power and Analog Solutions
9. OMAP35x Connectivity
10. Proven solutions – Archos / Garmin / Always innovating / Palm

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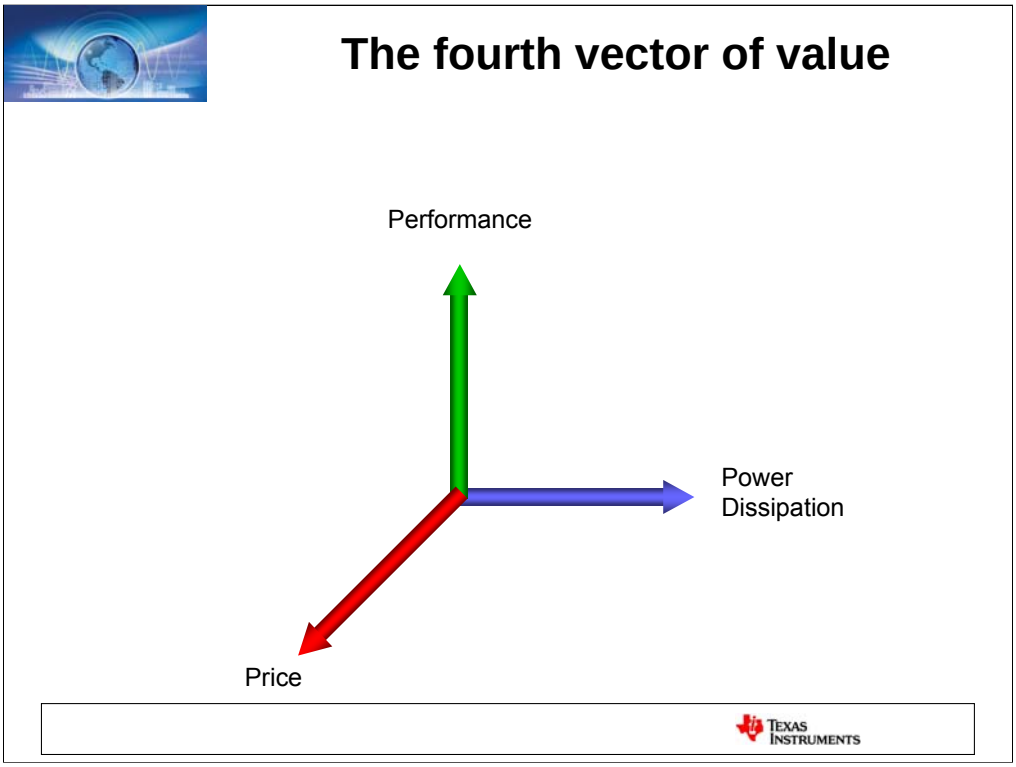
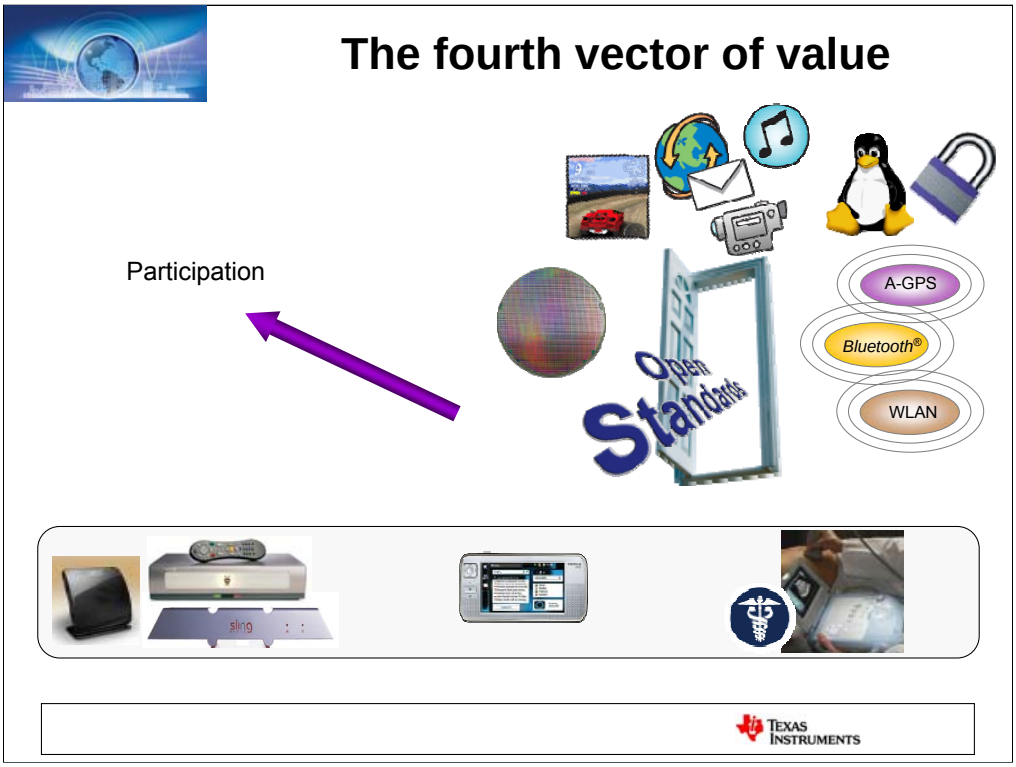


•There are several vectors to value of a solution: price, performance, and power dissipation.

•While software is not explicitly called out it is inherent to the performance, price and power dissipation vectors

•However, there is a fourth vector…



•A fourth vector of value is participation. Through participation, largely via software, the overall value of a solution can be increased.

General benefits of open source

- **Faster Innovation**
  - **Collaborate faster than standard product release cycles**
  - **Engage and fuel passionate innovators/developers**
  - **Peer-to-peer conversation and open idea exchange**
- **Better Solutions**
  - **Software quality through expert peer review**
  - **New preferred peer support through community**
  - **Faster feedback on product requirements and tools**

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•One of the easiest ways to encourage participation is open source software.

•Through the use of open source code and participation TI can enable faster innovation and better solutions on OMAP35x.

Why do people participate?

Simplified view

- **Leverage community to solve own problems, then share for possible benefits**
  - **May develop solution on their own**
  - **Benefits are generally improvements to the code**
  - **Not much benefit required, if no expecting loss**
  - **May utilize community to various degrees**
- **Solve community problems for <u>fame and glory</u>**
  - **Could just like getting a "pat on the back"**
  - **Could get a job or contract**

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TI in open source devices

http://opensource.ti.com

- **Neuros open source devices**
  http://www.neurostechnology.com
- **Nokia Internet tablets**
  http://www.maemo.org
- **OMAP™ 3…**
  - **Archos internet media tablets**
    http://www.archos.com
  - **Pandora handheld gaming devices**
    http://www.openpandora.org
  - **Zoom mobile development kit (cell phone focus)**
    http://www.omapzoom.org/
  - **Beagle board low-power, low-cost computer**
    http://beagleboard.org

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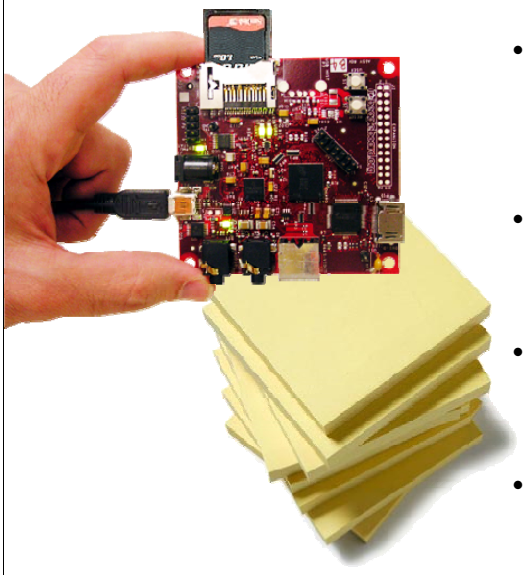
USB-powered Beagle Board unleashes community development



- USB powered board via low power OMAP3530 processor integration and minimal additional devices
- Flexible expansion through USB and standard PC peripherals
- Active and growing open source community at beagleboard.org
- Community supported

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Beagle Board – Delivering laptop-like performance and flexible USB & standard PC expansion

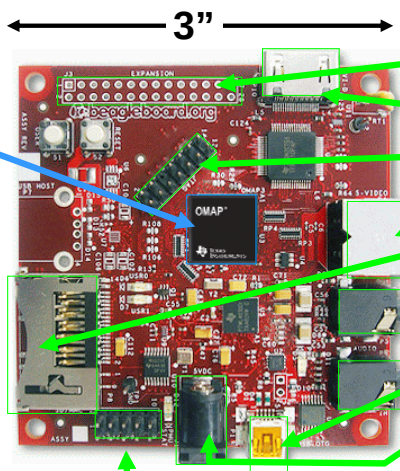
Laptop-like performance

TI OMAP3530

- 600 MHz superscaler ARM® Cortex ™-A8
- More than 1200 Dhrystone MIPS*
- Up to 10 Million polygons per sec graphics
- HD video capable C64x+™ DSP core

Memory

- 128MB LPDDR RAM
- 256MB NAND flash



USB & standard PC expansion

- I²C, I²S, SPI, MMC/SD
- DVI-D
- JTAG
- S-Video
- SD/MMC+
- Stereo Out
- Stereo In
- USB 2.0 HS OTG
- Alternate Power
- RS-232 Serial

* Performance varies by compiler

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CORTEX A-8 : Highlights

- **Dual-issue, in-order, superscalar architecture delivering high performance**
  - **First implementation of the ARMv7 instruction-set architecture, including the advanced SIMD media Instructions (NEON™)**
  - **Advanced dynamic Branch prediction**
- **Integrated, 256 KB unified L2 cache**
  - **Dedicated, low-latency, high-BW interface to L1 cache**
- **NEON™ : 64/128-bit Hybrid SIMD Engine for Multimedia**
  - **Supports both Integer and Floating Point SIMD**
- **Enhanced VFPv3 – doubles number of double-precision registers and new instructions to convert between fixed and floating point**
- **Efficient Run Time Compilation Target**
  - **Jazelle-RCT: Target for Java. Memory footprint reduced up to 3x**
  - **Can also target languages such as Microsoft .NET MSIL, Perl, Python**
- **TrustZone security**
  - **Device integrity, Digital Rights Management, Electronic payment, etc**

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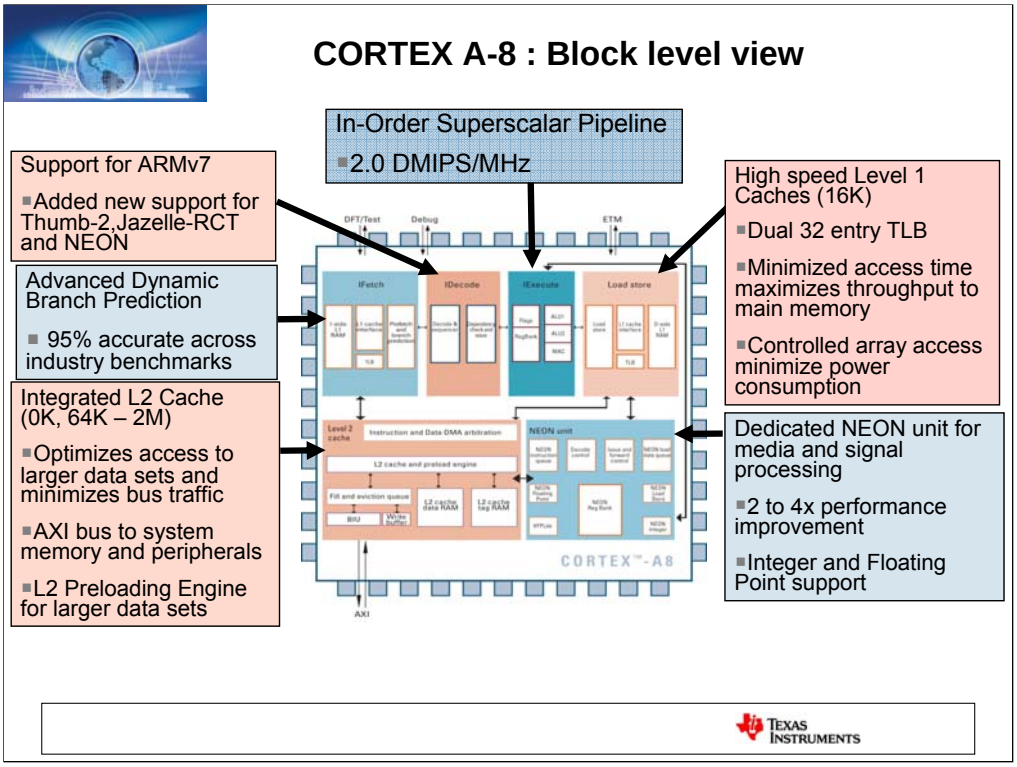
TrustZone adds a parallel world to run secure OS and applications
Normal and Secure worlds have different memory views, enforced by hardware
Memory tagged as secure and non-secure by the system
Only the secure CPU can access the secure memory & peripherals
Secure Monitor is a software “gatekeeper” between the two worlds
Device integrity, Digital Rights Management, Electronic payment, etc
5 Key technologies :-
Device Integrity / Secure Transactions – TrustZone Security
Fast & Responsive Java Applications -Jazelle RCT/ T2 EE
> Performance with < Code Size –T2 Instuctions
Enhanced Multimedia Experience – Neon +VFP3
Highest-performance mobile processor – SuperScalar ARM v7 Core

In-order dual instruction issue
less complex than out-of-order
fewer structures means lower
less need for custom design
can maintain high IPC with
fully symmetric ALU pipelines
all critical forwarding paths supported
dual-issue of dependent instruction pairs
Static scheduling with instruction replay on memory stall
low-power consumption due to early availability of gate enables
fire-and-forget instruction issue removes critical paths from the design
Net result
high-frequency design with out-of-order performance, but in-order clock frequency and power consumption
*Average **IPC** of **0.9** across 150+ ARM and industry benchmarks*



Harvard Level 1 Caches – both 16KByte, 4 way set associative

single-cycle load-use penalty

Virtual index Physically tagged(VIPT)

Level 1 Data cache is blocking

Non-Neon read misses cache cause replay of subsequent instructions

Reduces complexity in later pipeline stages

Good for power and clock frequency

Neon data not allocated to L1 (but will read/update in L1 if necessary)

Integrated 256 KB unified Level 2 Cache, 8-way set associative

Dedicated low latency, high bandwidth interface to the Level-I cache

Line length of 64 bytes

Minimum latency of 8 cycles

Streams to the Neon processing unit; up to 16GByte/s bandwidth

128-bit data streaming from both L1D$ and L2$

64 bit AMBA AXI interconnect to external memory

Supports multiple outstanding memory transactions to minimize memory latencies

The CP14 coprocessor: also known as the *debug coprocessor*

used for various debug functions.

CP15 coprocessor: also known as the *system control coprocessor*

used to control and provide status information for the functions implemented in the processor.

Feature comparison : ARM926, 1176, Cortex-A8

	ARM926	ARM1136	Cortex-A8 w/NEON
Architecture Version	V5	V6	V7
Pipeline type	In-order scalar	In-order scalar	In-order, dual-issue superscalar
Pipeline stages	5	8	13
ISA Efficiency (DMIPS/MHz)	1.07	1.18	2.01
MMU	Yes	Yes	Yes
TLB	8 entry unified	2 µTLB and LB	2x32 full assoc
Core to L1 interface	32 bit	64 bit	64 bit (128 Neon)
L1 $ Set associativity	4	4	4
Line length	32B	32B	64B
Tightly coupled memory	Yes	Yes	No

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Feature comparison: ARM926, 1176, Cortex-A8

	ARM926	ARM1136	Cortex-A8 w/NEON
Integrated L2 $	No	No	YES
Branch prediction	No	128 entry BTB	512 entry BTB
General coprocessor I/F	Yes	Yes	No
External Interface	2 AHB 2.0	5 AHB 2.5 – 3 x 64 bit, 2 x 32 bit	1 AXI – 64/128
TrustZone Support	No	No	Yes
Non-Cacheable Fill Buffer	4 word	8 word	16 word
Java support	Jazelle DBX	Jazelle DBX	Jazelle RCT
Floating Point / Media	No (coprocessor available, VFP9)	VFP11 attached, V6 Integer SIMD	NEON Integer and FP SIMD, VFP Lite
Per-Cycle Multiply-accumulate throughput (fixed point)	1 x 32 bit 1 x 16 bit	1 x 32 bit 2 x 16 bit	2 x 32 bit 4 x16 bit 8 x 8 bit Float: 2 x 32 bit

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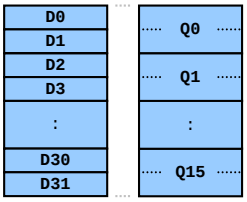
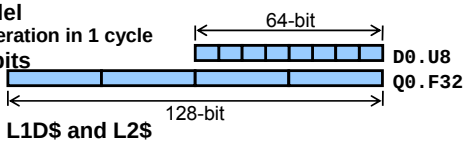
NEON™: Advanced SIMD

- **64/128-bit Hybrid SIMD architecture**
  - *A single instruction performs the same operation on multiple elements that are packed within registers*
- **Independent Register file with 2 aliased views:**
  - 32 x 64-bit registers (D0-D31)
  - 16 x 128-bit registers (Q0-Q15)



- **Integer and SP Floating-point processing**
  - 8, 16, 32, 64-bit Integers
  - Single-precision Floating-point
- **Encoded in ARM and Thumb-2**
- **Two Integer 64-bit ALUs operating in parallel**
  - Can perform 128-bit length equivalent ALU operation in 1 cycle
- **64-bit data path with data types up to 128 bits**
  - Up to 8-byte SIMD integer
  - 2-way SIMD single-precision FP
- **Supports 128-bit data streaming from both L1D$ and L2$**
  - Byte permute function allows for on-the-fly data shuffling
- **Two Integer Multipliers of 32x16**
  - Each can perform one 32x16, two 16x16 or four 8x8 operations in a single pass
  - Support 32x32 operation in two passes
- **Accelerates audio, video, and 3D-graphics**



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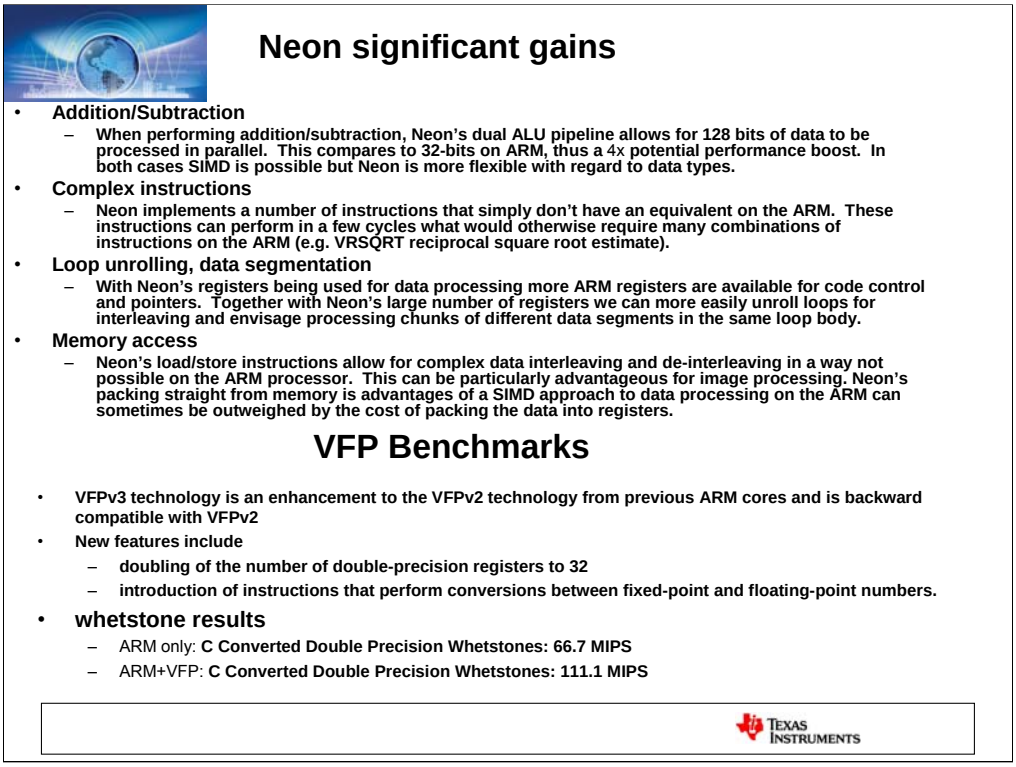


VFPv3 technology is an enhancement to the VFPv2 technology from previous ARM cores and is backward compatible with VFPv2

Fully compliant with the *ANSI/IEEE Std 754-1985, IEEE Standard for Binary Floating-Point Arithmetic*

The VFP coprocessor fully supports single-precision and double-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations

New features include

doubling of the number of double-precision registers to 32

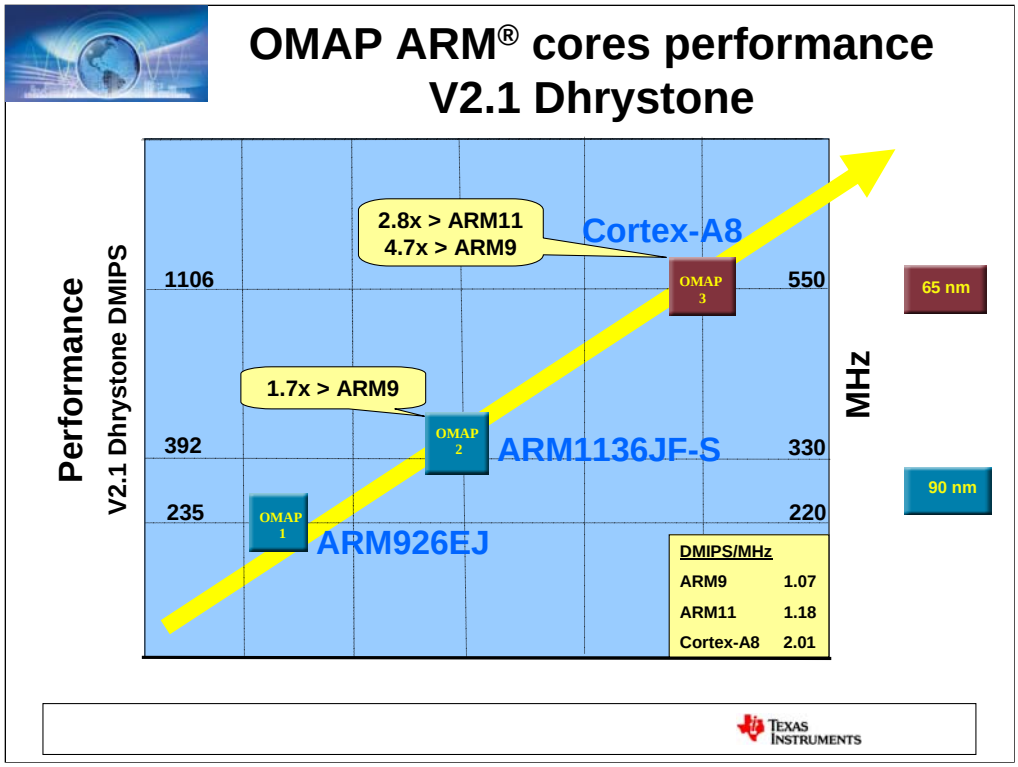
introduction of instructions that perform conversions between fixed-point and floating-point numbers.

Register banks shared with NEON™. Viewed as:

Thirty-two 64-bit double word registers, D0-D31. This view is also available in NEON™

Thirty-two 32-bit single word registers, S0-S31. Only half of the register bank is accessible in this view.

Part of NEON™ Hardware Unit

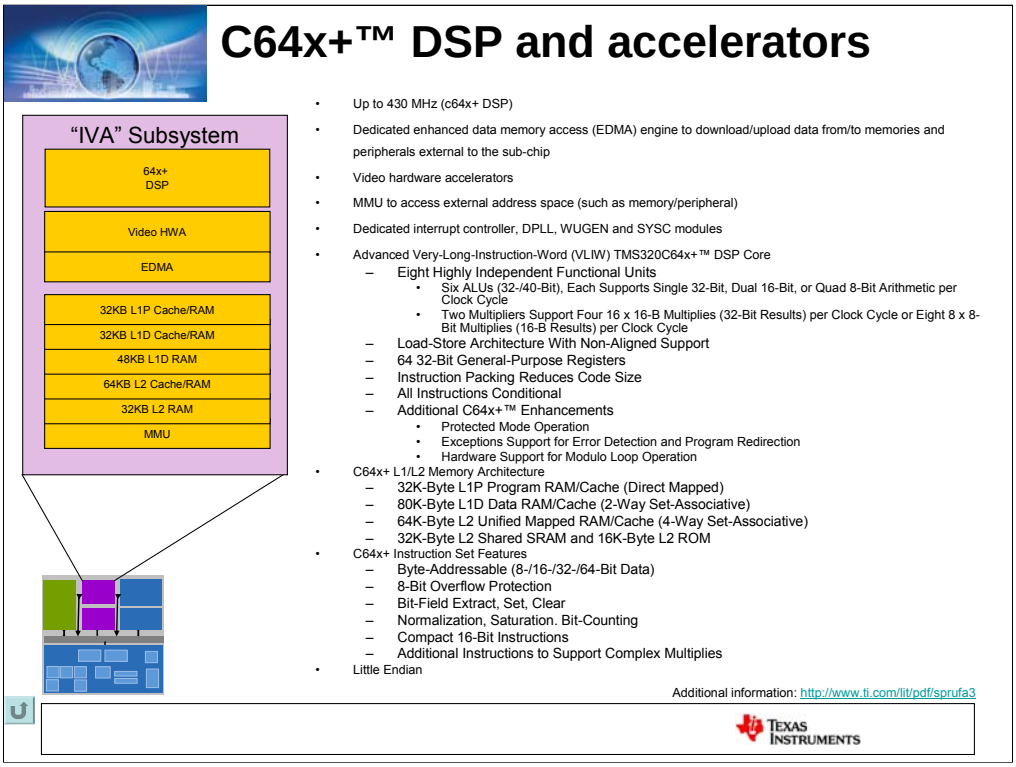


•Dhrystone is a short synthetic benchmark (simple programs that are carefully designed to statistically mimic some common set of programs) program intended to be representative for system (integer) programming.

•The Dhrystone benchmark contains no floating point operations.

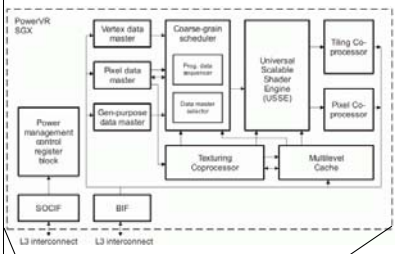
•Dhrystones per second is the metric used to measure the number of times the program can run in a second. Dhrystone tries to represent the result more meaningfully than MIPS (million instructions per second), because MIPS cannot be used across different instruction sets (e.g. RISC vs. CISC) for the same computation requirement from users. Thus, the main score is just

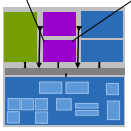
•Dhrystone loops per second. Another common representation of the Dhrystone benchmark is the **DMIPS** - Dhrystone MIPS - obtained when the Dhrystone score is divided by 1,757 (the number of Dhrystones per second obtained on the VAX 11/780, nominally a 1 MIPS machine).



If additional information link does not work, please use this one: http://focus.ti.com/docs/prod/folders/print/omap3530.html#technicaldocuments and select the appropriate doc

PowerVR SGX graphics engine





- Up to ~111 MHz
- Tile Based Architecture Delivering up to 10 MPoly/sec
- Universal Scalable Shader Engine: Multi-threaded Engine Incorporating Pixel and Vertex Shader Functionality
- Industry Standard API Support: OpenGLES 1.1 and 2.0, and OpenVG1.0
- Fine Grained Task Switching, Load Balancing, and Power Management
- Programmable High Quality Image Anti-Aliasing

Additional information: http://www.ti.com/lit/pdf/spruff6
Graphics white paper: http://www.ti.com/lit/pdf/spry110

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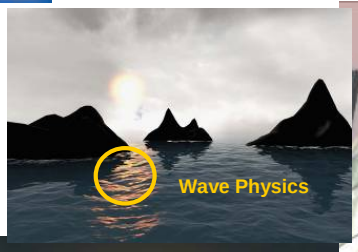
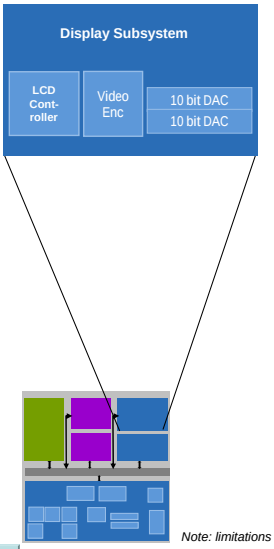
Graphics capability examples



Images provided by Imagination Technologies

Display subsystem (DSS)



- Parallel Digital Output
  - Up to 24-Bit RGB
  - HD Maximum Resolution
  - Supports Up to 2 LCD Panels
  - Support for Remote Frame Buffer
  - Interface (RFBI) LCD Panels
- 2 10-Bit Digital-to-Analog Converters(DACs) Supporting:
  - Composite NTSC/PAL Video
  - Luma/Chroma Separate Video (S-Video)
- Rotation 90-, 180-, and 270-degrees
- Resize Images From 1/4x to 8x
- Color Space Converter
- 8-bit Alpha Blending

Additional information:

Note: limitations may apply among packages

http://www.ti.com/lit/pdf/sprufa4

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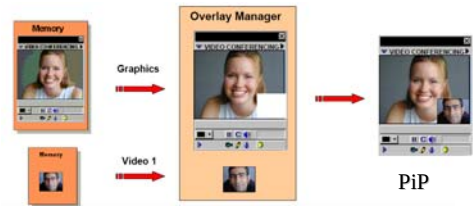
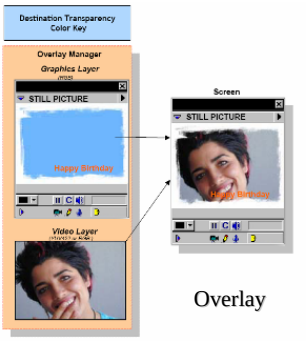
Display subsystem examples

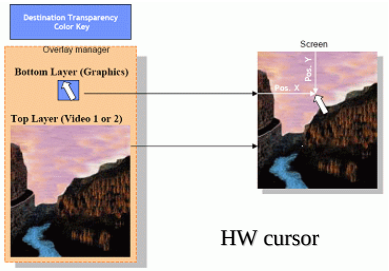


PiP

Scaling

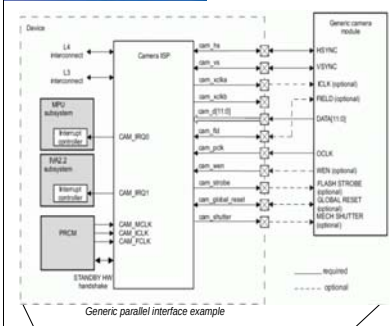


Overlay

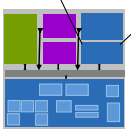


HW cursor

Camera interface subsystem (ISP)



Generic parallel interface example



- CCD and CMOS Imager Interface
- Memory Data Input
- RAW Data Interface
- BT.601/BT.656 Digital YCbCr 4:2:2 (8-/16-Bit) Interface
- A-Law Compression and Decompression
- Preview Engine for Real-Time Image Processing
- Glueless Interface to Common Video Decoders
- Histogram Module/Auto-Exposure, Auto-White Balance, and Auto-Focus Engine
- Resize Engine
  - Resize Images From 1/4x to 4x
  - Separate Horizontal/Vertical Control

Note: limitations may apply among packages

Additional information: http://www.ti.com/lit/pdf/sprufa2

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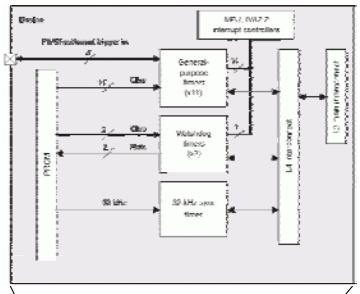
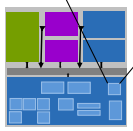
Timers



- 12 32-bit General Purpose Timers
- 2 32-bit Watchdog Timers
- 1 32-bit 32-kHz Sync Timer



Note: limitations may apply among packages

Additional information:

http://www.ti.com/lit/pdf/sprufa9

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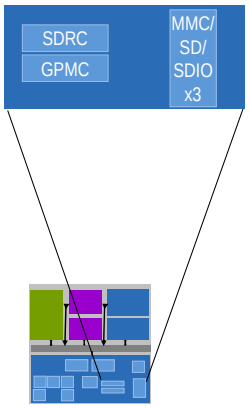
SD / MMC, SDRC, and GPMC interface



- SD / MMC / SDIO
  - Three instantiations
  - Compliant with CE-ATA and ATA for MMCA
  - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards
  - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards
- General Purpose Memory Controller (GPMC)
  - 16-bit Wide Multiplexed Address/Data Bus
  - Up to 8 Chip Select Pins With 128M-Byte Address Space per Chip Select Pin
  - Glueless Interface to NOR Flash, NAND Flash (With ECC Hamming Code Calculation), SRAM and Pseudo-SRAM
  - Flexible Asynchronous Protocol Control or Interface to Custom Logic (FPGA, CPLD, ASICs, etc.)
  - Nonmultiplexed Address/Data Mode Limited 2K-Byte Address Space)
- SDRAM Controller (SDRCM) Subsystem
  - 16, 32-bit Memory Controller With 1G-Byte Total Address Space
  - Interfaces to Low-Power Double Data Rate (LPDDR) SDRAM
  - SDRAM Memory Scheduler (SMS) and Rotation Engine

Note: limitations may apply among packages

Additional information:
SD/MMC: http://www.ti.com/lit/pdf/sprufd2
SDRC / GPMC: http://www.ti.com/lit/pdf/sprufa1

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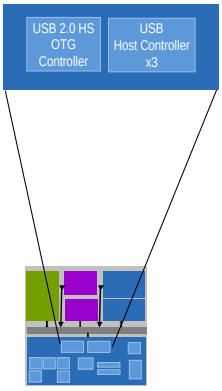
USB



- USB 2.0 HS OTG Controller
  - **USB 2.0 low-speed (1.5M bit/s), full-speed (12M bit/s), and high-speed (480M bit/s) host**
  - **USB 2.0 full-speed (12M bit/s), and high-speed (480M bit/s) peripheral**
  - **OTG Support**
  - **PHY interface – ULPI (HS/FS)**
- USB Host Controller
  - **Host only**
  - **All 3 ports operate in either HS or FS mode (determined by selected PHY connection)**
  - **HS Mode**
    - **480M bit/s**
    - **Available Port – 1 & 2**
    - **PHY interface ULPI**
  - **FS Mode**
    - **12M bit/s**
    - **Available Port – 1, 2, and 3**
    - **PHY interface Serial Asynchronous**

Note: limitations may apply among packages

Additional information: http://www.ti.com/lit/pdf/sprufd4

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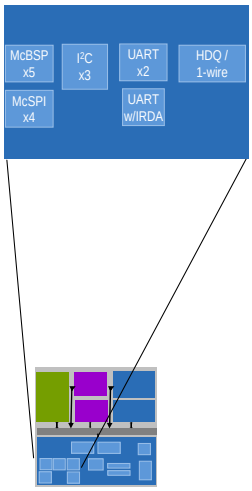
If additional information link does not work, please use this one: http://focus.ti.com/docs/prod/folders/print/omap3530.html#technicaldocuments and select the appropriate doc

Serial interfaces and HDQ/1-Wire



- 3 Master/Slave High-Speed Inter-Integrated Circuit Controllers (I^2C)
- 5 Multi Channel Buffered Serial Ports (McBSP)
  - 512 Byte Transmit/Receive Buffer (McBSP1/3/4/5)
  - 5K-Byte Transmit/Receive Buffer (McBSP2)
  - SIDETONE Core Support (McBSP2 and 3 Only) For Filter, Gain, and Mix Operations
  - Direct Interface to I2S and PCM Device and TDM Buses
  - 128 Channel Transmit/Receive Mode
- 4 Master/Slave Multi Channel Serial Port Interface (McSPI)
- 3 UARTs (One with Infrared Data Association [IrDA] and Consumer Infrared [CIR] Modes)
- 1 HDQ / 1-Wire

Additional information:
I2C: http://www.ti.com/lit/pdf/sprufc6
McBSP: http://www.ti.com/lit/pdf/sprufd1
McSPI: http://www.ti.com/lit/pdf/sprufc9
UART: http://www.ti.com/lit/pdf/sprufc5
HDQ: http://www.ti.com/lit/pdf/sprufd0

Note: limitations may apply among packages

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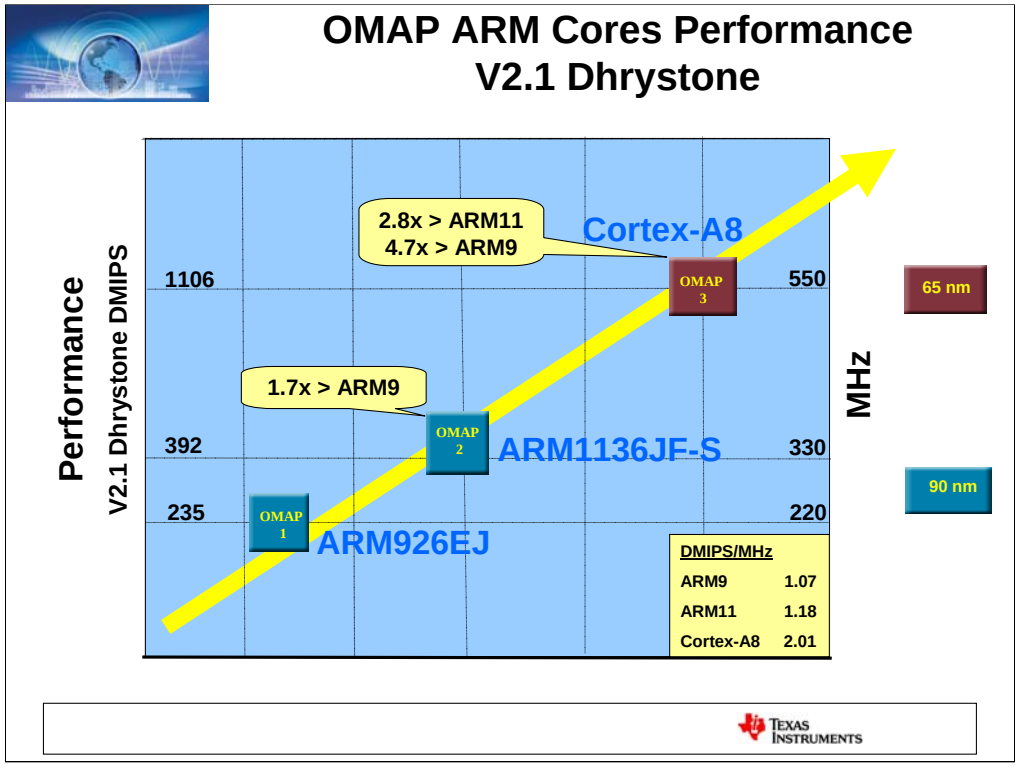

Dhrystone is a short synthetic benchmark (simple programs that are carefully designed to statistically mimic some common set of programs) program intended to be representative for system (integer) programming. The Dhrystone benchmark contains no floating point operations. Dhrystones per second is the metric used to measure the number of times the program can run in a second. Dhrystone tries to represent the result more meaningfully than MIPS (million instructions per second), because MIPS cannot be used across different instruction sets (e.g. RISC vs. CISC) for the same computation requirement from users. Thus, the main score is just Dhrystone loops per second. Another common representation of the Dhrystone benchmark is the **DMIPS** - Dhrystone MIPS - obtained when the Dhrystone score is divided by 1,757 (the number of Dhrystones per second obtained on the VAX 11/780, nominally a 1 MIPS machine).

SDRC Throughput

USE CASE

Monitoring Maximum throughput on SDRC I/F

- $I & $D cache enabled to avoid accesses during measurement.
- Measurement variable put in OCMRAM.
- All the accesses from different initiators are placed in different banks. [camera & LCD are using same bank]
- Traffic on Channel
- Class 0-LCD used to read Data From SDRC
- Class 1-CORTEX used for performance measurement.
- Class 2-SDMA & USB used to Read/Write Data from SDRC at it's maximum capacity.

Conditions

- CORE OPP3 (Core/VDD2): 333MHz / 1.15V
- L3 @ 166 MHz /1.15 V
- Temperature: Laboratory temperature

RESULTS

DMA	MB / s
- 32 Bit 64 Burst Size Read	292
- 32 Bit 64 Burst Size Write	292
Camera	
- 32 Bit 64 Burst Size Read	8
LCD	
- 32 Bit 64 Burst Size Read	206
USB Loopback	
-Read	16.

Design Estimate throughput:- 1000 MB/s

Theoretical throughput :- 1300 MB/s

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SDMA Throughput

RESULTS - Multi Channel

Transfer mode	Access mode	Source	Destination	Notes	Single channel MB/Sec	Multiple Channel Throughput MB/Sec
64B Read/Write	Read-Write	SDRAM	SDRAM	Diff Banks	680.49	653.52
				Same Bank	660.93	625.29
		OCMC-RAM	OCMC-RAM		516.25	516.88
		OCMC-RAM	SDRAM		869.04	865.85
		SDRAM	OCMC-RAM		857.46	855.12
	Transparent Copy	SDRAM	SDRAM	Diff Banks	340.39	325.87
				Same Bank	319.84	302.31
		OCMC-RAM	OCMC-RAM		258.11	258.45
		OCMC-RAM	SDRAM		434.28	431.78
		SDRAM	OCMC-RAM		428.64	427.37
	Constant Fill	SDRAM	SDRAM	Diff Banks	584.55	591.59
				Same Bank	584.01	591.84
		OCMC-RAM	OCMC-RAM		440.73	441.04
		OCMC-RAM	SDRAM		584.03	592.08
		SDRAM	OCMC-RAM		440.25	440.96

EDMA Throughput

USE CASE

Conditions	RESULTS
• CORE OPP3 (Core freq/VDD2): 333MHz / 1.15V • Sample:ES2.0 Lead Lot • Temperature: Laboratory temperature	619.65 MB/s: SDRAM to L2, VRFB OFF Max 777.52 MB/s: L2 to SDRAM, VRFB OFF Max 900 MB/s: L1D to OCMC-RAM, VRFB OFF

Conclusion

✓ **Performance improvement by 33 % was observed on McBSPLP Interface**
- – Increase in number of outstanding transactions at L4PER agent on L3 from 1 to 2 has enabled us to use 1/3 of the max theoretical BW compared to 1/5 previously.
- – Max theoretical BW is 4x83 = 332MB/s. 1/3 of this = 110MB/s 1/5 of this = 66MB/s.

✓ **Performance improvement by 8 -16 % was observed on reading data from SDRAM IF writing to L2/L1 memory of IVA**

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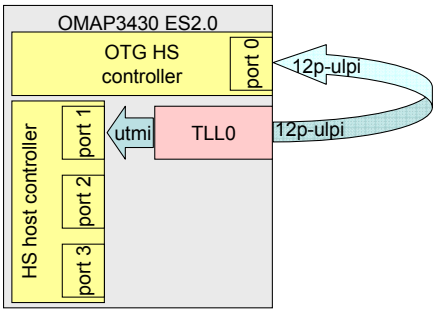
HS-USB Host TLL

USE CASE

Bulk transfer between TLL Host port (1, 2 or 3) & HS-OTG port (0) configured as client

	USBHost - TLL	HSUSB-OTG
Interface	ULPI-TLL / SDR 12bits @ 60MHz	ULPI SDR 12bits @ 60MHz
Speed	HS only	
Type of transfers	Bulk IN (Device sends data to Host) Single endpoint used (not multiple concurrent transfers)	
Transfer size	634800 bytes (1240 packets of 512 bytes)	
Packet Size	512 bytes (Maximum for Bulk transfers)	
Module Specific Options	Built-in DMA (mandatory for EHCI controller)	Built-in DMA activated Double buffer activated



RESULTS

TLL loopback⇨ 325.7 MBits/s

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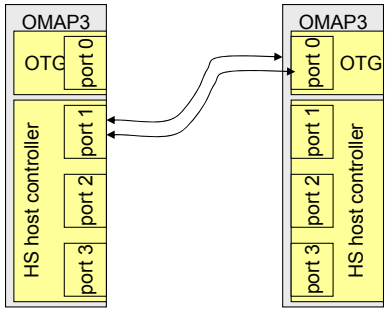
HS-USB Host PHY

USE CASE

Bulk transfer between TLL Host port (1, 2 or 3) & HS-OTG port (0) configured as client

	USBHost - TLL	HSUSB-OTG
Interface	ULPI-TLL / SDR 12bits @ 60MHz	ULPI SDR 12bits @ 60MHz
Speed	HS only	
Type of transfers	Bulk IN (Device sends data to Host) Single endpoint used (not multiple concurrent transfers)	
Transfer size	634800 bytes (1240 packets of 512 bytes)	
Packet Size	512 bytes (Maximum for Bulk transfers)	
Module Specific Options	Built-in DMA (mandatory for EHCI controller)	Built-in DMA activated Double buffer activated



RESULTS

PHY Loopback ⇨ 312.7 MBits/s

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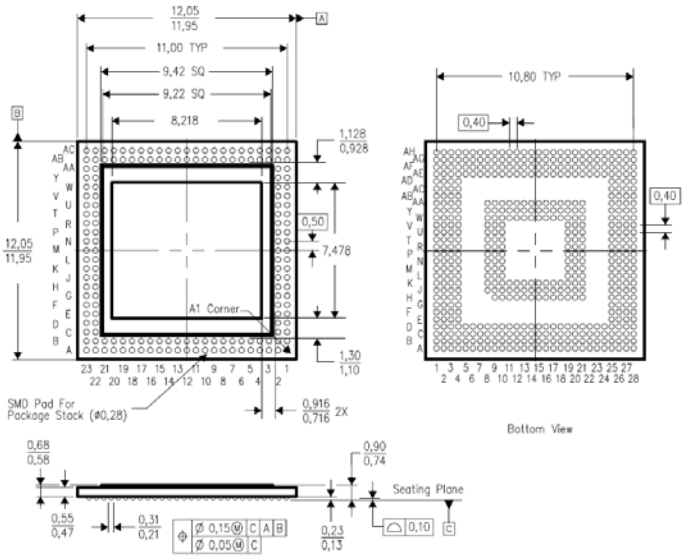
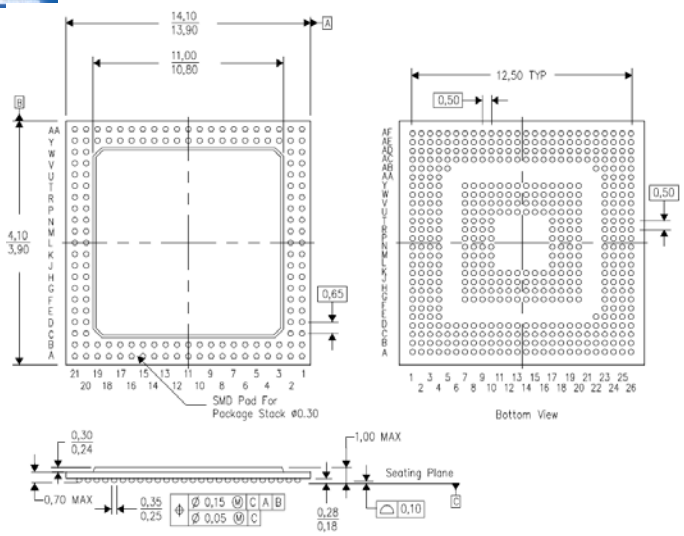
Package (1/3)



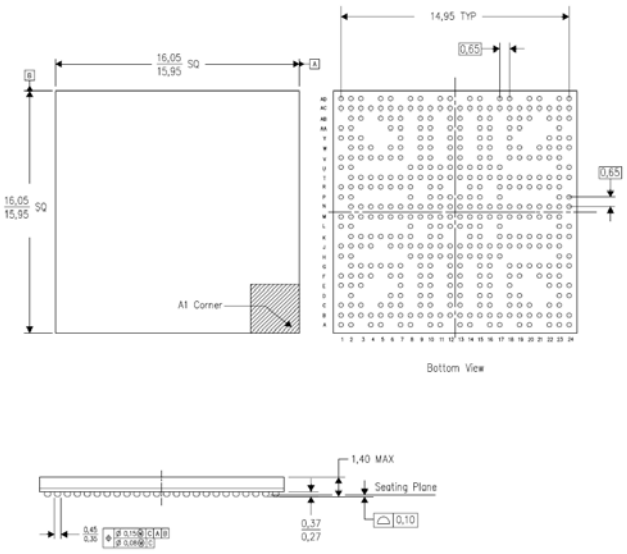
12 x 12 mm 0.40 mm pitch 515 pin plastic BGA

Package (2/3)



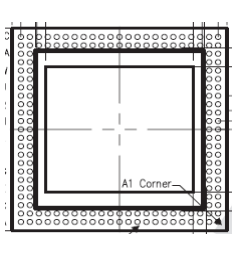
14 x 14 mm 0.50 mm pitch 515 pin plastic BGA

Package (3/3)

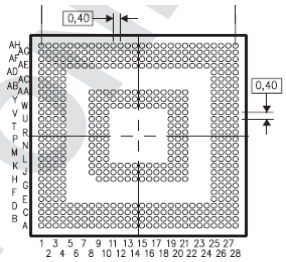


16 x 16 mm 0.65 mm pitch 423 pin plastic BGA

Package On Package (POP)

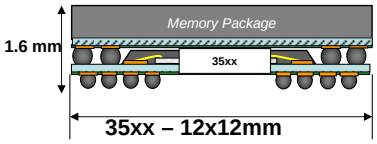


Top View



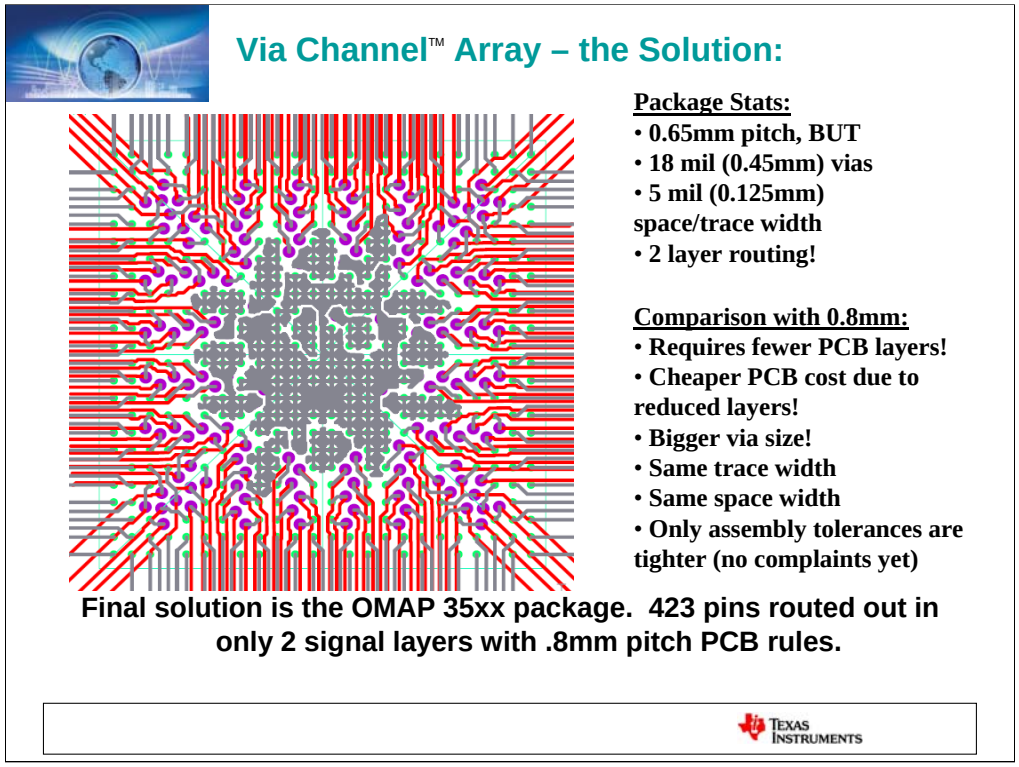
Bottom View

35xx - .4mm pitch



Side view of stacked package

- **POP = Package on Package Technology**
- **Offers advantage of saving PCB area, LPDDR routing and the flexibility of choosing their own Top POP Package memory configuration. The trade off is routing complexity and manufacturing challenges.**
- **Key POP memory suppliers are *Micron, Samsung and Elpida***



I designed the CUS package to do something very few other processors can. It can be completely routed in four layers (total). I don't see a lot of customers going quite this far (they usually assume six layers is minimum, because it always has been for 99% of SoCs) but they will try to reduce the layer count to something between 6-8, depending on their goals of size and complexity, however as more processors get embedded into cheaper systems, I see this as the wave of the future.

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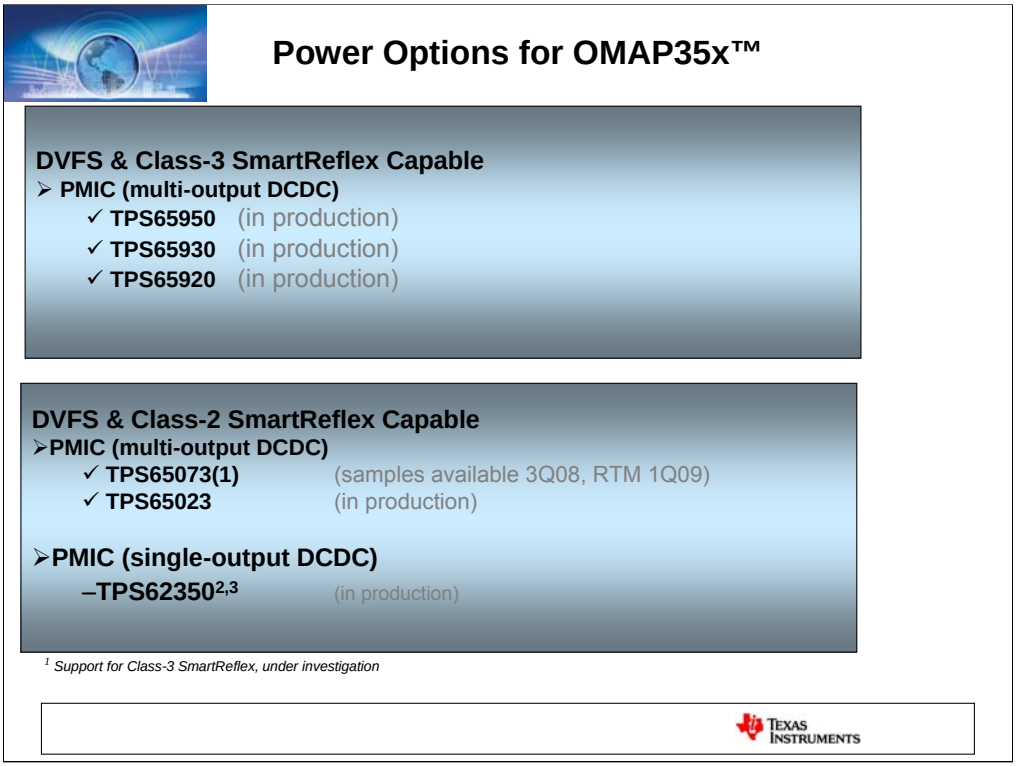


Class-0

At manufacturing test, the device-optimized operating point voltages are permanently fused into each die. A one time optimization to account for process variations.

Class-1

At boot-up time, device-optimized operating point voltages of the die are determined during calibration. Optimization also accounts for process variations.

Class-2

SmartReflex sub-chip does real-time voltage optimization via software loop

MPU services interrupts to change voltage

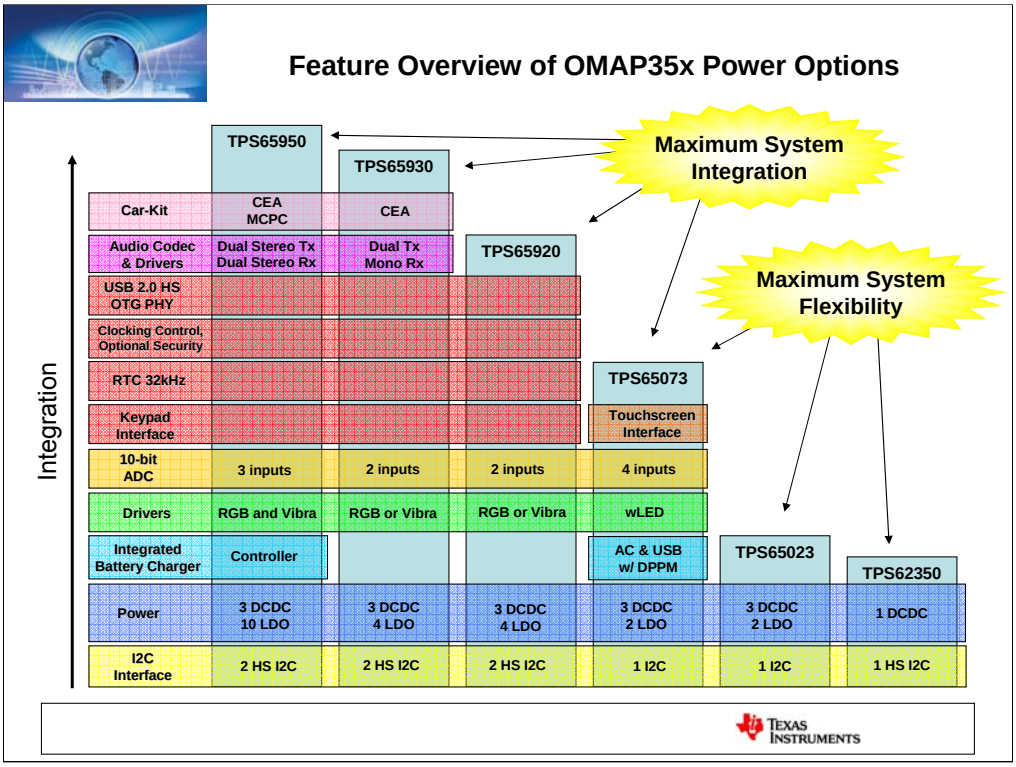
Optimizes for process, temperature and silicon degradation effects

Class-3 (Available on OMAP35xx)

SmartReflex sub-chip has a dedicated hardware loop to dynamically optimize voltage for process, temperature and silicon degradation effects

MPU intervention not required

Optimizes for process, temperature and silicon degradation effects



TPS65023
Outputs: DCDC1 (Core) = 1.5A @ 1.2V (w/ DVM)
DCDC2 (Memory) = 1.2A @ 1.8V/3.3V
DCDC3 (I/O) = 1.0A @ 3.3V/1.8V
LDO = 200mA @ 1.8V/3.3V

TPS65073
3 step-down converters (adjustable via I2C, will be able to do SR class 3, but similarly to T2 spec does not reach the 1.2A on DCDC3)

DCDC1: (used for ?)
- Max current: 600mA

DCDC2: (to OMAP3 VDD2)
- Max current: 600mA
- Default voltage: TBD ????
- Vstep min: 25mV (for Vout b/n 0.725V-1.5V)
- Slew rate: defined by DEFSLEW reg (0.11-7.2mV/us)
- I2C control: 2-register-write for votlage change to happen

DCDC3: (to OMAP3 VDD1)
- Max current: 1100mA
- Default voltage: TBD ????
- Vstep min: 25mV (b/n 0.725V-1.5V)
- Slew rate: defined by DEFSLEW reg (0.11-7.2mV/us)
- I2C control: 2-register-write for voltage change to happen

For all three DCDC converters
- Quiescent current: 15uA
- Vout range: 0.6V to Vin (Vin range is 2.7V – 6V)
- Ramp time (EN to 95% Vout): 170us+750us = 1ms
- Vout accuracy: +/-2% or better
- Enable/Disable: EN-pin AND'ed with EN-bit in I2C register (single register write to disable DCDC)

TPS6235x (Limit to 3503 and "ARM+SGX" only)
Input Voltage: 2.7V to 5.5V
Adjustable Output Voltage:
- TPS62350 (0.75V to 1.5V)
- TPS62351 (0.9V to 1.6V)
- TPS62352 (0.75 to 1.4V)
- TPS62353 (0.75V to 1.5V)
- TPS62354 (0.75V to 1.5V)
- TPS62355 (0.75V to 1.5V)

Output Current: **800mA**

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Potential OMAP35x applications

Digital Signage

Point of Service Terminals

Low Power PC / Web Tablet

Portable Industrial / SDR

Portable Infotainment

Industrial Panel PC/HMI

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