Power Supply
Layout Considerations

Seminar Paper at:

http://focus.ti.com/lit/ml/slup230/slup230.pdf

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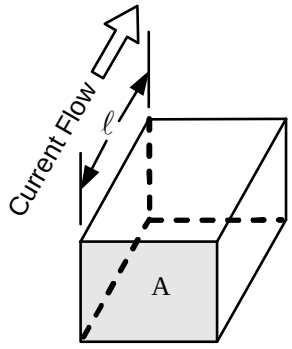
Agenda

- ➔ DC Parasitics (Resistance)
- ◆ AC Parasitics
- ◆ Grounds and Grounding
- ◆ Thermal Considerations
- ◆ Design Examples

You Mean Copper is Not a Perfect Conductor?

- Since it is not, it impacts
  - Regulation
  - Efficiency
  - Temperature rise

Sample Resistance Calculation



Material	μΩ-cm	μΩ-in
Copper	1.70	0.67
Gold	2.2	0.87
Lead	22.0	8.66
Silver	1.5	0.59
Tin -Lead	15	5.91
Palladium	11	4.3

$$R = \frac{\rho l}{A}$$

$$\rho = resistivity$$

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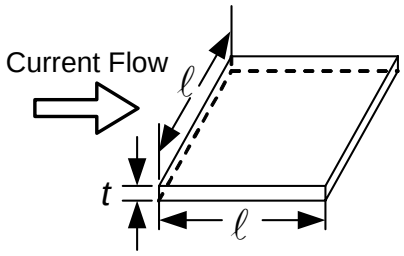
The numbers given for Plated Copper are worst-case values.

Typically, they will lie somewhere between pure copper and these values.

Count Squares to Estimate Trace Resistance

- Copper resistivity is 0.67 μΩ in. at 25°C and doubles for 254°C rise



$$R = \frac{\rho(\ell)}{t(\ell)}$$

$$R = \frac{\rho}{t}$$

Copper Weight (Oz.)	Thickness (mm/mils)	mΩ per Square (25°C)	mΩ per Square (100°C)
1/2	0.02/0.7	1.0	1.3
1	0.04/1.4	0.5	0.65
2	0.07/2.8	0.2	0.26

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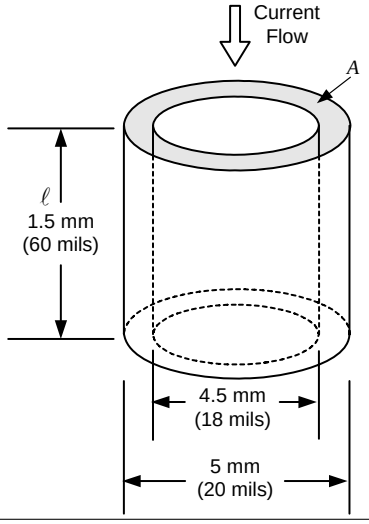
Vias Have Resistance Too

- Typical rule of thumb is 1 A to 3 A per via



$$R = \frac{\rho l}{A}$$

$$R = \frac{\rho l}{\pi(r_o^{\,2} - r_i^{\,2})}$$

$$R = \frac{2.36 \times 10^{-6} \times 0.06}{\pi(0.01^2 - 0.009^2)} = 2.4\ m\Omega$$

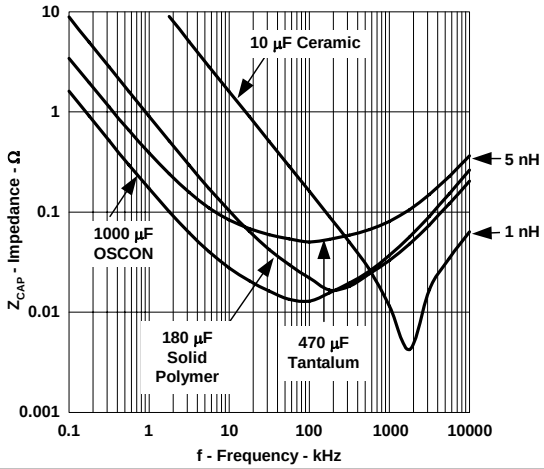
Agenda

- DC parasitics (resistance)
- ➔ AC parasitics
  - When is a capacitor not a capacitor ?
- Grounds and grounding
- Thermal considerations
- Design examples

Capacitors Are Inductive…

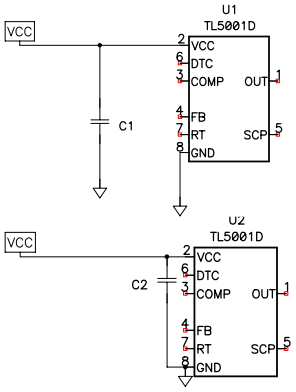
Above Their Self-Resonant Frequency

- Measured ESL correlates well with rule of thumb inductance of 15 nH/inch



Bypass Capacitor Layout

- Minimize lead inductance
  - Minimize bypass loop area
  - Short lengths on high di/dt paths
  - Use ground planes where possible
  - Bring current path across capacitor terminals



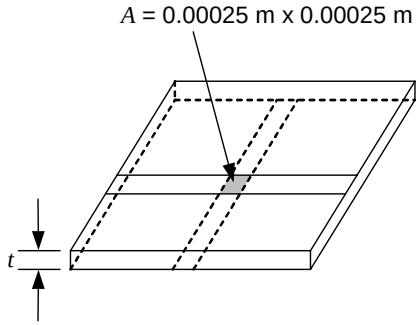
- Parallel different capacitor types for reduced impedance across a frequency band

- Parallel different ceramic capacitors values and sizes to reduce impedance in the 2-20 MHz frequency range (0.1 μF & 0.01 μF)

- Draw your schematic so the layout person knows the critical routes

Sample Capacitance Calculation

Consider two 10 mil traces crossing with 10 mil PWB thickness



Note: 10 mils = 0.00025 m

$$C = \frac{\varepsilon_R \times \varepsilon_O \times A}{t}$$

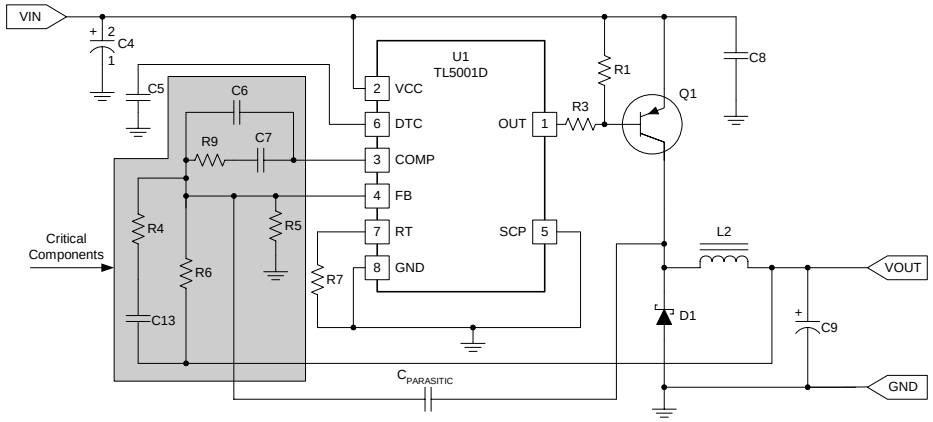
$$C = 5\left(\frac{10^{-9}}{36\pi}\right)\left(\frac{0.00025^2}{0.00025}\right)$$

$$C = 0.01\ pF$$

Not much capacitance but consider the area of all those components connected to the summing node

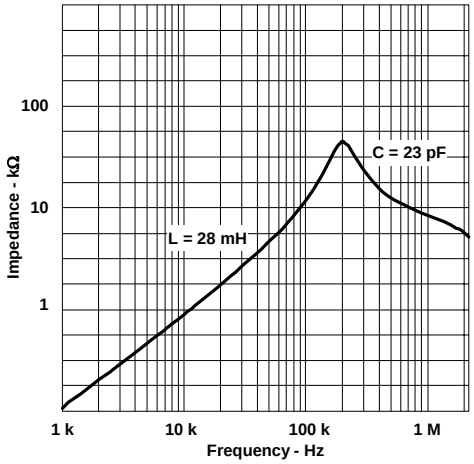
Chaos Created by Noise Injection

Ten 0.05 x 0.02 in^2 pads in summing junction can increase parasitic capacitance to 2 pF



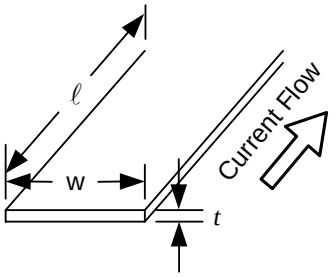
And Inductors Turn Into Capacitors

- Inductive at low frequency
- High frequency, distributed capacitance and μ_r reduction



Self Inductance of PWB Traces

- Due to the natural logarithmic relationship, large changes in conductor width have minimal impact on inductance



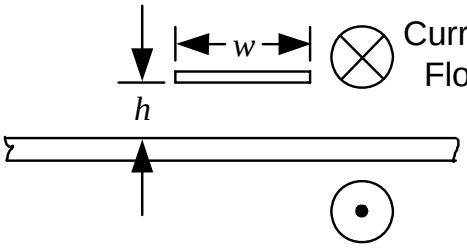
$$L = 2\ell\left(\ell n\left(\frac{\ell}{t+w}\right)+\frac{1}{2}\right)\ nH\ (cm)$$

$$L = 5\ell\left(\ell n\left(\frac{\ell}{t+w}\right)+\frac{1}{2}\right)\ nH\ (in)$$

w (mm/in)	T(mm/in)	Inductance (nH/cm or nH/in)
0.25/0.01	0.07/0.0028	10/24
2.5/0.1	0.07/0.0028	6/14
12.5/0.5	0.07/0.0028	2/6

PWB Traces Over Ground Planes

- Substantial inductance reduction
- Inductance inversely proportional to width



$$L = \frac{2hl}{w} \text{ nH/cm}$$

$$L = \frac{5hl}{w} \text{ nH/in}$$

Metric			English		
h (cm)	w (cm)	Inductance (nH/cm)	h (in)	w (in)	Inductance (nH/in)
0.25	2.5	0.2	0.01	0.1	0.5
1.5	2.5	1.2	0.06	0.1	3.0

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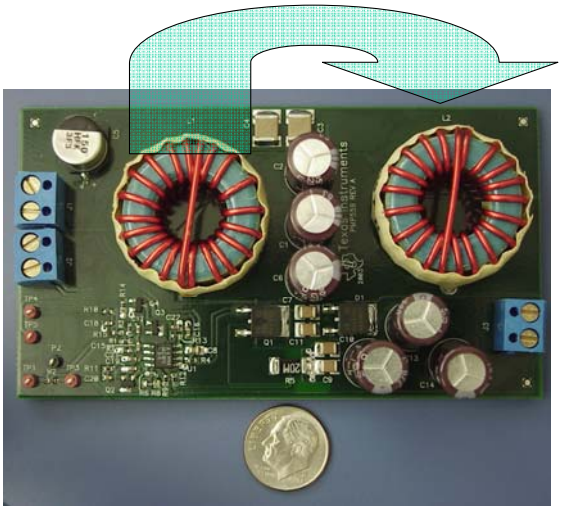
Magnetic Coupling

- Consider alternate orientation of second inductor to minimize coupling



Watch Out for Parasitic Components

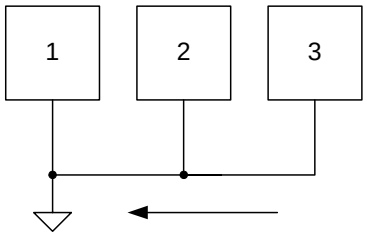
- Wiring inductance
  - Especially low impedance circuits-filters, power switching, timing
  - Use ground planes and wide conductors to minimize
- Board capacitance
  - High impedance or noise sensitive circuits
  - Watch out for coupling between planes and to component pads
- Magnetic coupling
  - Inductor to inductor, especially toroids, consider alternate mounting directions
  - Loop to loop, minimize loop areas, use ground planes

Agenda

- DC parasitics (resistance)
- AC parasitics
- ➔ Grounds and grounding
  - Construction from the ground up
- Thermal considerations
- Design examples

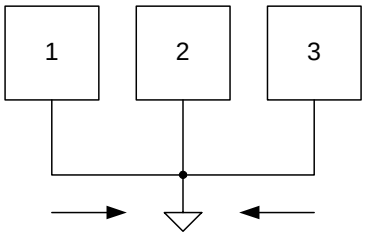
Single Point Grounds

Series



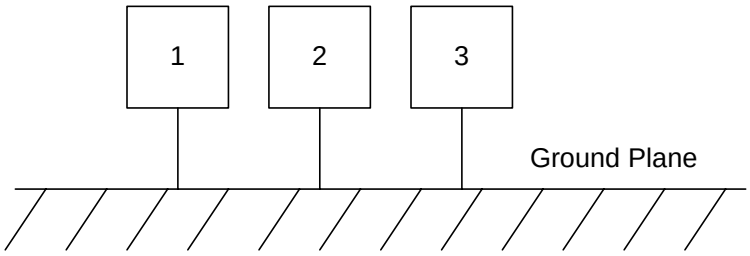
- Simple wiring
- Common impedance causes different potentials
- High impedance at high frequency (>10 kHz)

Parallel



- Complicated wiring
- Low differential potentials at low frequencies
- High impedance at high frequency (>10 kHz)

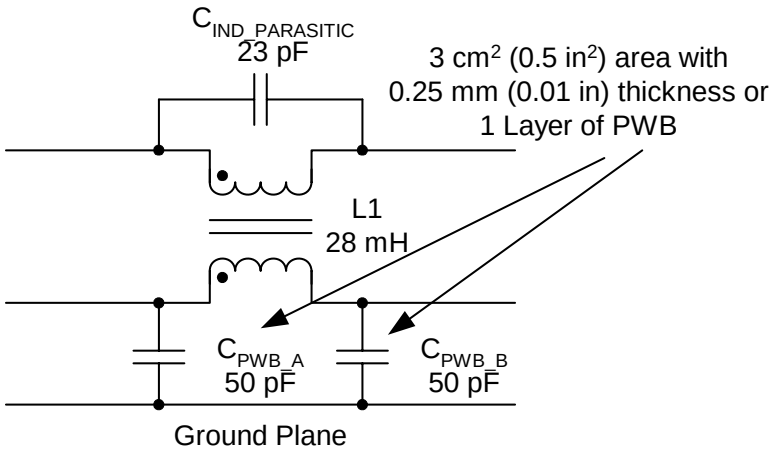
Multipoint Grounding



- Ground plane provides low impedance between circuits to minimize potential differences
- Also, reduces inductance of circuit traces
- Goal is to contain high frequency currents in individual circuits and keep out of ground plane

Ground Planes

Don’t route ground plane under common mode inductors

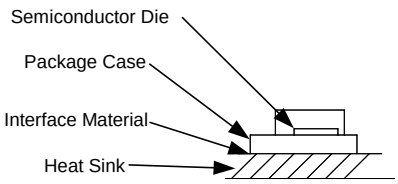


Agenda

- DC parasitics (resistance)
- AC parasitics
- Grounds and grounding
- ➔ Thermal considerations
  - Getting the heat out
- Design examples

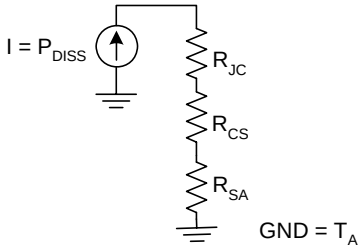
Temperature Rise

- **Rjc:** Junction to case thermal resistance, usually specified
- **Rcs:** Interface resistance, specified for heat sink insulators, negligible for solder connections
- **Rsa:** Sink to ambient resistance, specified for heatsinks, otherwise ill-defined



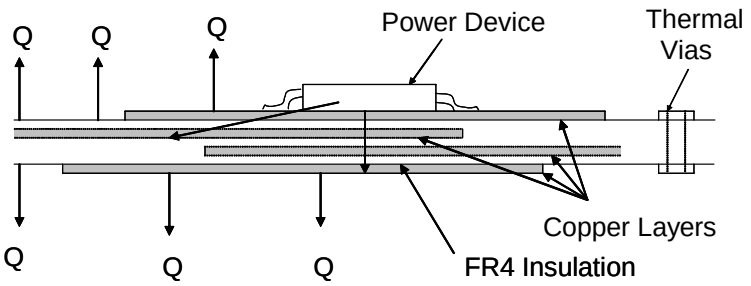
Electrical Equivalent

$T = P_{DISS} \times (R_{JC} + R_{CS} + R_{SA}) + T_A$



Power Supplies Components

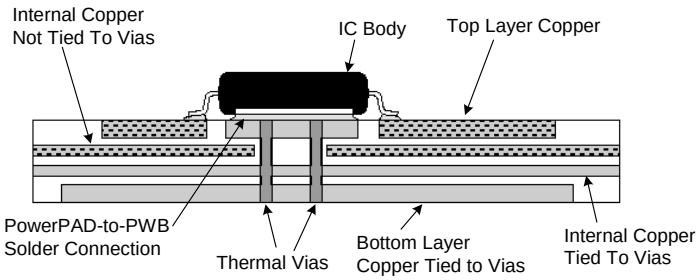
Many Are PWB Mounted and Cooled



- Power is conducted through device base into circuit board
- It spreads laterally through copper conductors
- Final path is convection cooling from board surface to ambient

Typical Thermal Requirements

- Ambient temperature: 70°C, T_A
- Maximum semiconductor: 125°C, Max T_J
- Maximum board temperature: 120°C
- Typical semiconductor loss: 2 W
- PowerPAD™ SO-8 thermal resistance: 2.3°C/W
- Calculated PWB temperature under semiconductor is 125°C – (2 W x 2.3°C/W) = 120°C



Convection Cooling (English Units)

- To a first approximation, temperature rise is proportional to power dissipation and inversely proportional to surface area (Sa)
- The proportionality constant, h, is called heat transfer coefficient and is about 0.006 W/in^2/°C for air

$$\Delta T = \frac{P}{(Sa \times h)} = \frac{P}{(Sa \times 0.006)} \qquad \Delta T = \frac{166 \times P}{Sa} \qquad R_{SA} = \frac{166}{Sa}$$

- Or 1 W over a square inch yields about 166°C rise
- More precise equation accounting for the nonlinearity of h

$$\Delta T = P^{0.8} Sa^{-0.7} (100^{o} C)$$

Convection Cooling (Metric Units)

- To a first approximation, temperature rise is proportional to power dissipation and inversely proportional to surface area
- The proportionality constant, h, is called heat transfer coefficient and is about 0.001 W/cm^2/°C for air

$$\Delta T = \frac{P}{(Sa \times h)} = \frac{P}{(Sa \times 0.001)} \qquad \Delta T = \frac{1000 \times P}{Sa} \qquad R_{SA} = \frac{1000}{Sa}$$

- Or 1 W over a square cm yields about 1000°C rise
- More precise equation accounting for the nonlinearity of h

$$\Delta T = P^{0.8} Sa^{-0.7} (650°C)$$

Convection Cooling Area Calculations (English)

- Applying the simple formula and solving for 50°C rise

$$\Delta T = \frac{166 \times P}{Sa}$$

$$Sa = \frac{166 \times P}{\Delta T}$$

$$Sa = \frac{166 \times 2}{50}$$

$$Sa = 7$$

- The package is much smaller than this dimension and something must be done to provide a larger cooling surface

Convection Cooling Area Calculations (Metric)

- Applying the simple formula and solving for 50°C rise

$$\Delta T = \frac{1000 \times P}{Sa}$$

$$Sa = \frac{1000 \times P}{\Delta T}$$

$$Sa = \frac{1000 \times 2}{50}$$

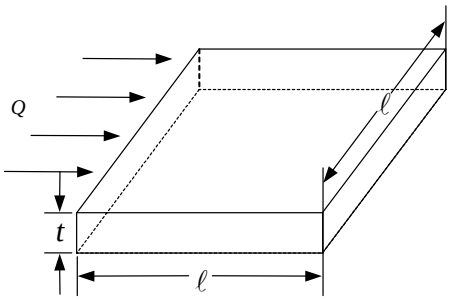
$$Sa = 40$$

- The package is much smaller than this dimension and something must be done to provide a larger cooling surface

Thermal Conductivity of Other Materials

Material	W/(cm ºC)	W/(in ºC)
Air	0.0002	0.0007
Alumina	0.2	0.9
Aluminum	1.8	4.4
Beryllia	1.6	4
Copper (OFC)	3.6	9
Epoxy (PC board)	0.0003	0.007
Ferrite	0.04	0.10
Steel	0.15	0.60
Tin-lead	0.4	1.00

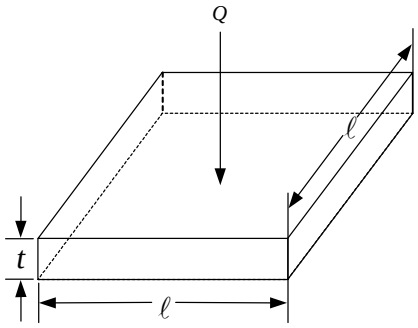
Lateral Heat Flow



Metric	English
2-oz, 0.07-mm thick copper	**2-oz, 2.8-mils thick copper**
$R = \frac{l}{(\sigma \times l \times t)}$ $R = \frac{1}{(0.4 \times 0.07)}$ $R = 40^{\circ}C/W$	$R = \frac{l}{(\sigma \times l \times t)} = \frac{1}{(\sigma \times t)}$ $R = \frac{1}{(9 \times 0.0028)}$ $R = 40^{\circ}C/W$
1.5-mm FR4	**0.06-inch FR4**
$R = \frac{1}{(0.00028 \times 1.5)}$ $R = 2400^{\circ}C/W$	$R = \frac{1}{(0.007 \times 0.06)}$ $R = 2400^{\circ}C/W$

Thermal Resistance

Through board is much less than board-ambient



$$R = \frac{t}{(\sigma \times A)}$$

$$R = \frac{1.5}{(0.0003 \times 25.4 \times 25.4)} \quad \text{Metric}$$

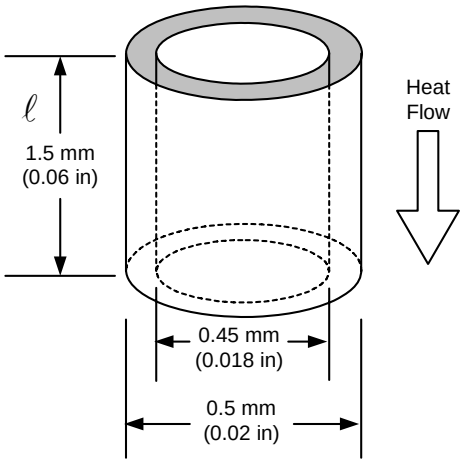
$$R = \frac{0.06}{(0.007 \times 1)} \quad \text{English}$$

$$= 8\,^{\circ}\text{C/W}$$

Calculations based on one square inch of board area.

Thermal Resistance

A single via has about 100°C/W thermal resistance and they can be paralleled



$$R = \frac{l}{(\sigma \times A)}$$

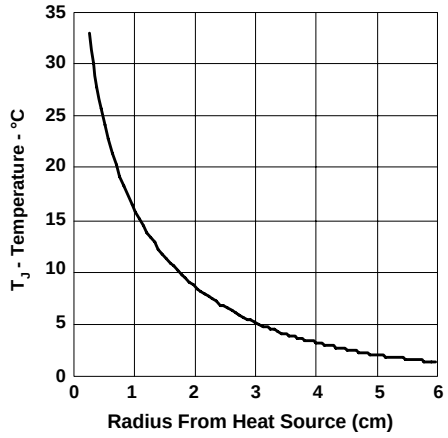
$$R = \frac{l}{\sigma \times \pi \times (r_o^{\,2} - r_i^{\,2})}$$

$$R = 100^{o} C / W$$

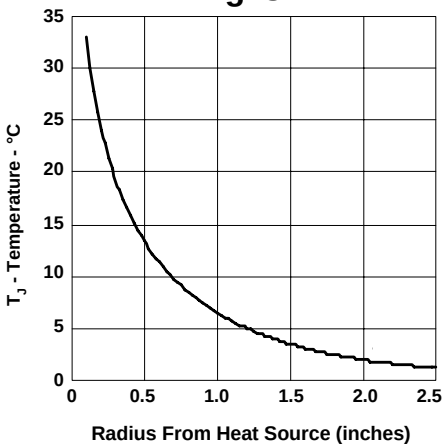
Dissipation on Double-Sided Board

2 W of point source dissipation on double-sided board calculates to ~30°C rise under the source

Metric



English



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Vertical Cools Better Than Horizontal

Surface Orientation	K′ (cm. °C, and W)	K′ (in. °C, and W)
Vertical	650	100
Horizontal plane, top surface	675	104
Horizontal, bottom surface	1375	204

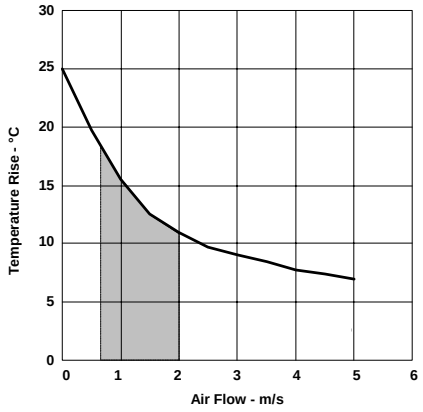
$$\Delta T = Pd^{0.8} \times \frac{K'}{A^{0.7}}$$

PWB Cooling Strategy

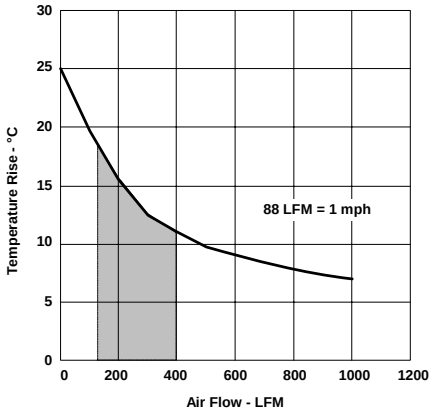
- Use many large, thick copper planes to distribute heat across PWB surface
- Maximize the thermal paths with poured copper wherever practical
- Use both sides of the board to cool
- Reasonably low thermal resistance is possible through the PWB material but substantial improvements can made with thermal vias
- Avoid breaks in planes as they substantially degrade lateral heat flow
- Buried planes can also improve the lateral heat flow
- Cooling strategy often opposed to noise reduction

Even a Whisper of Air can Reduce Temperatures

Metric



English



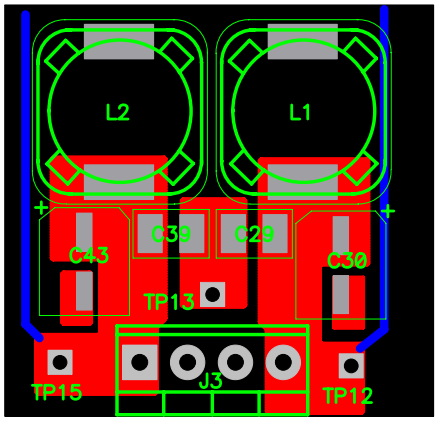
System airflow yields 20% to 60% drops in temperature rise

Agenda

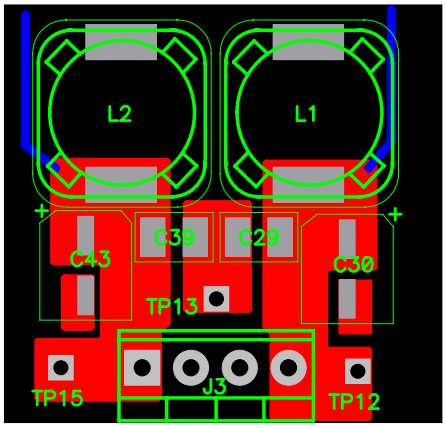
- DC parasitics (resistance)
- AC parasitics
- Grounds and grounding
- Thermal considerations
- ➔ Design examples
  - Let's get real!

Proper Sensing of Output Voltage

Sensing at Output Connector



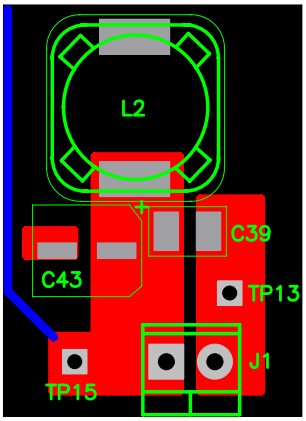
Poor Sense Location



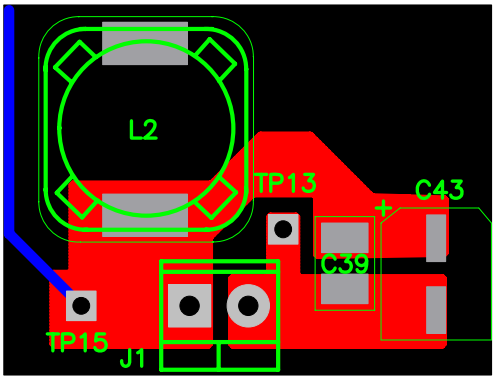
- How many mΩ between L2 and J3?

Output Capacitor Connection

Low Series Inductance



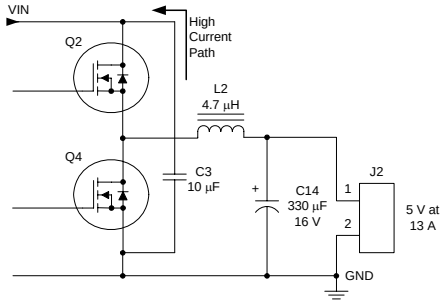
High Series Inductance



- How much inductance in series with C39? (length ~ 1 in.)

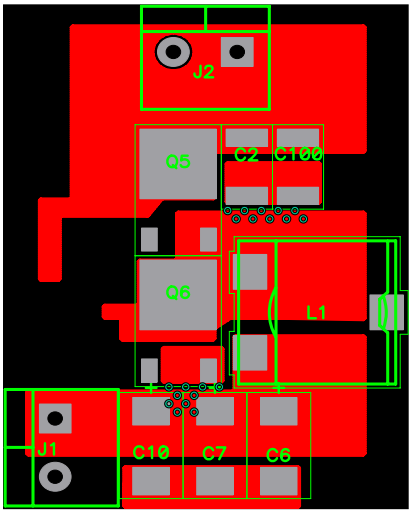
Connect Power Components Properly

- Very high di/dt in current path
- Any inductance in path results in ringing on switched node
- Minimize loop area
  - Draw schematic to reflect this
  - Consider two sided mounting, FET's one side, cap other
  - Make sure components are placed and routed accordingly
- Proper design can eliminate need for snubber



Input Capacitor Placement

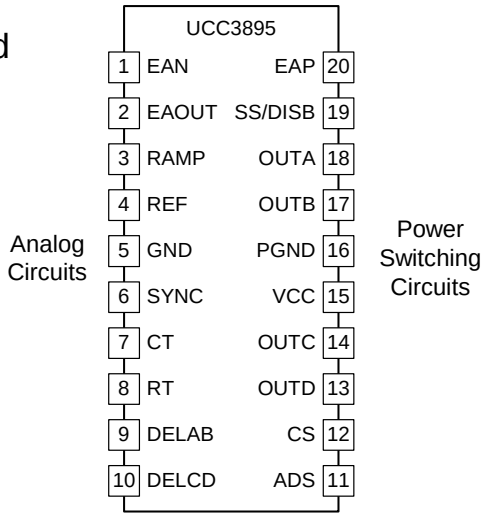
Good input capacitor placement and layout



- Input caps located close to top FET Q5 with large plane
- Input caps GND side drops into GND plane through multiple vias
- Bottom FET Q6 GND drops into GND plane through multiple vias
- Solid uninterrupted GND plane

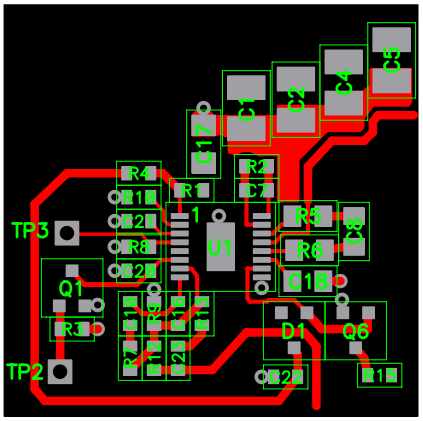
Partitioning Circuits

- Many control ICs recognize noisy/quiet circuit areas and pin out accordingly
- Some even provide a separate pin for power and analog ground
- Good practice plans layout around pin out, uses a ground plane, and keeps high current out of it.

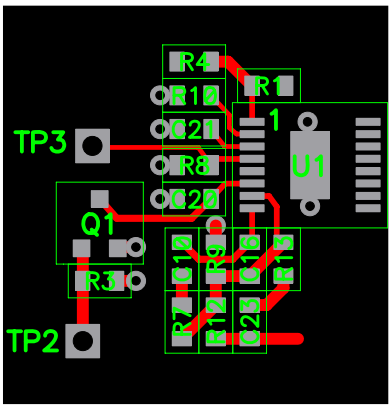


Separate Power Path

Separate power path from control signals

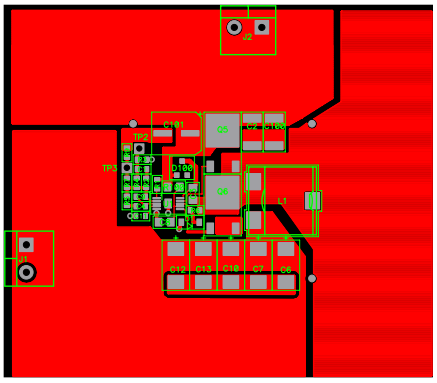


Layout of Controller Small Signals



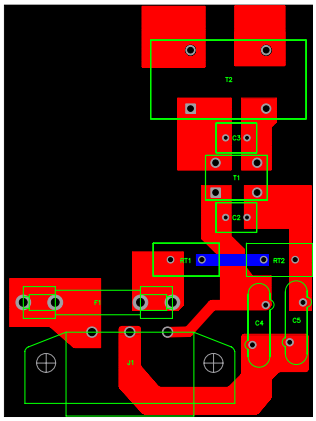
- Very short etch runs
- Error Amp connections (pins - 7,8) are noise sensitive and should be routed carefully
- Use GND plane on layer 2
- Drop returns into GND plane without long etches
- Feedback to output voltage routed away from switching power signals

High Current Layout Example



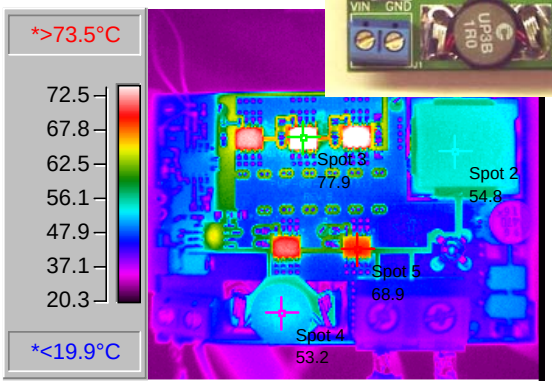
- Maximize copper
- Duplicate on several layers
- Thermal vias near heat sources
- Eliminate bottlenecks
- Use low θ_{JC} components

Good EMI Filter Layout



- Common mode inductor T2 input pins do not cross output pins
- No GND plane under EMI filter
- Wide, short etch used to minimize losses
- Wide spacing between etches meets HV requirements and minimizes coupling capacitance

Thermal Image



- Large power planes help distribute heat
- Thermal vias carry power to inner planes
- Separation between heat sources aids cooling

A Good Layout

Makes For A Successful Design

- Power supply layout is as important as any other design consideration
- The power supply engineer must be involved in parts placement and routing
- But it is not ‘black magic’, it is an understanding of AC and DC parasitics, grounding, and cooling that makes a successful design

Seminar Paper at:

http://focus.ti.com/lit/ml/slup230/slup230.pdf