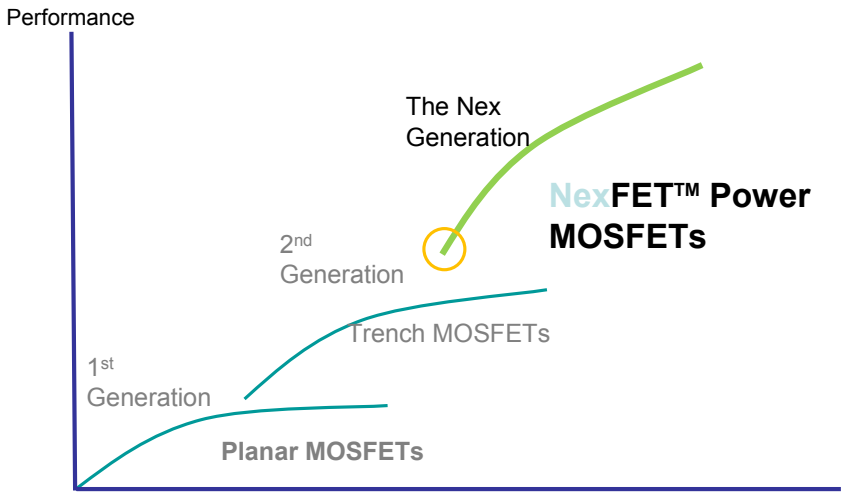
NexFET™

How To Design with Highly Efficient MOSFETs

Texas Instruments

Just the Beginning



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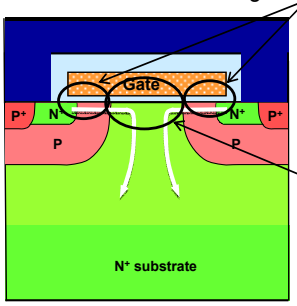
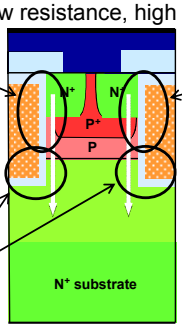
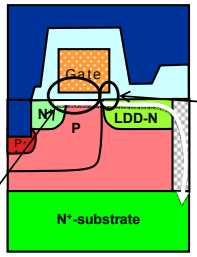
Technology Comparison

Planar
- Commercialized in 1980s
- Lower density structure
- Relative large gate area
- Mid resistance and charge

Trench
- Commercialized in the 1990s
- Very High Density structure
- Large gate area
- Low resistance, high charge







C_{GS} C_{GD} C_{GS} C_{GD}

NexFET™ Technology
- Commercialized in 2007
- High density structure
- Low gate charge
- Low resistance & charge

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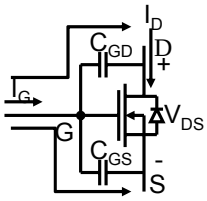
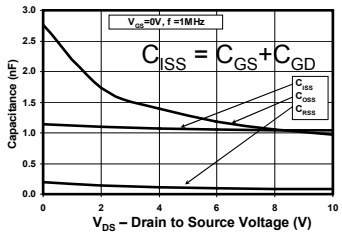
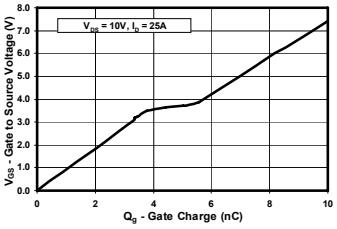
Total Gate Charge
Q_G

- **Total Gate Charge (Q_G) is the charge required to drive the Input Capacitance (C_{ISS}) from 0V to a specified Gate Voltage under specified I_D and V_{DS} Conditions.**
  - **Q_G is the Area under the C_{ISS} vs. V_{GS} curve.** $Q_G = \int_0^{V_{DS}} C_{ISS}\, dV_{DS}$
- **Energy is required to charge the gate, and is lost when it is discharged.** $E_G = Q_G V_{GS}$
  - **In each Charge/Discharge cycle, energy lost is:**

Q_g	Gate Charge Total (4.5V)	4	5.6	nC







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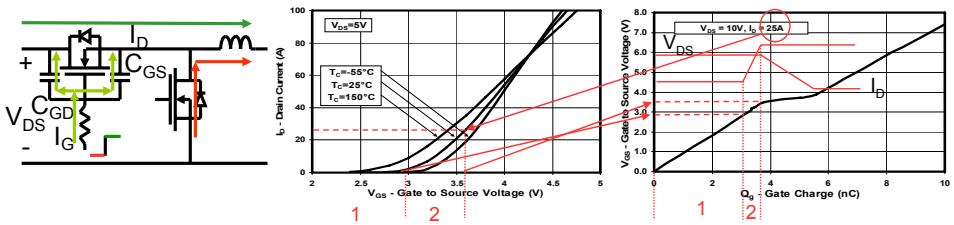
Gate to Source Charge
Q_{GS}

- Gate to Source Charge (Q_{GS}) is the Charge required to Switch a specified Current.
- There are two distinct regions of Q_{GS}:
  1. Pre Conduction – From 0V to the gate voltage where current begins to rise on the Transfer Characteristics curve – Nothing much happens besides an increase in Gate Leakage.
  2. Switching (~1/4 Q_{GS}) – Current rises along transfer characteristics curve to the Drain current while V_{DS} remains high.
- Under an Inductive Load, V_{DS} remains high while the Current is switched with energy loss per cycle as: $E_{SW(GS)} \approx V_{DS} I_D \frac{1}{4} Q_{GS} \div I_G$

Q_{gs}	Gate Charge Gate to Source	V_{DS} = 12.5V, I_D = 17A	2.1	nC



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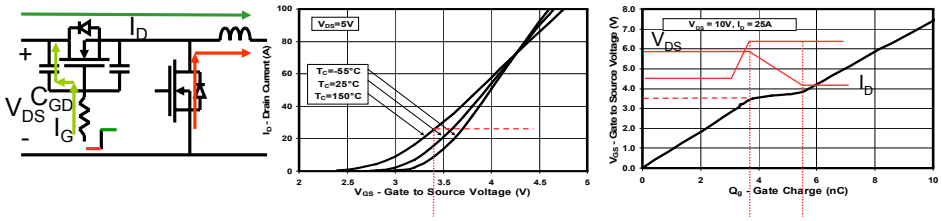
Gate to Drain Charge
Q_{GD}

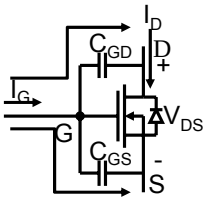
- Gate to Drain (Miller) Charge (Q_{GD}) is the Charge required to Switch a specified Voltage.
- Q_{GD} is typically specified at ½ BV_{DSS}.
  - When V_{DS} is different, Q_{GD} must be adjusted.
  - In the applicable range, Q_{GD} vs. V_{DS} is fairly linear and can be approximated by 1.75% ΔV_{DS} per ΔQ_{GD}.
- Under an Inductive Load, I_D is high while the Voltage is switched with energy loss per cycle as: $E_{SW(GD)} \approx V_{DS} I_D Q_{GD} \div I_G$

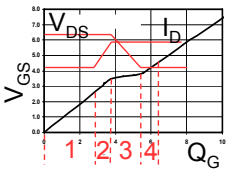
Q_{gd}	Gate Charge Gate to Drain	1	nC

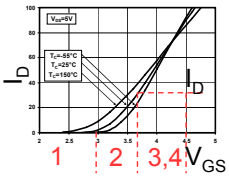


Gate Charge
Q_G, Q_{GS}, Q_{GD}

- Gate Charge is the amount of charge required to be put into or taken out of the Gate to Drain and Gate to Source Capacitances to Switch the MOSFET.
- Gate Charge can be split into:
  1. Gate to Source Charge (Q_{GS}), Pre Conduction – From 0V to the gate voltage where current begins to rise on the Transfer Characteristics curve – Nothing really happens.
  2. Q_{GS}, Switching (~1/4 Q_{GS}) – Current rises along transfer characteristics curve to the Drain current while V_{DS} remains high.
  3. Gate to Drain (Miller) Charge (Q_{GD}), - While Current is high, V_{DS} collapses.
  4. Overdrive Charge – V_{GS} rises to its final value, driving down R_{DSON}.
- Energy required to switch the gate in one cycle (on and off): $E_G = Q_G V_{GS}$
- Energy dissipated in the switching action in one cycle: $E_{SW} = V_{DS} I_D \left(\frac{1}{4} Q_{GS} + Q_{GD} \right) \div I_G$







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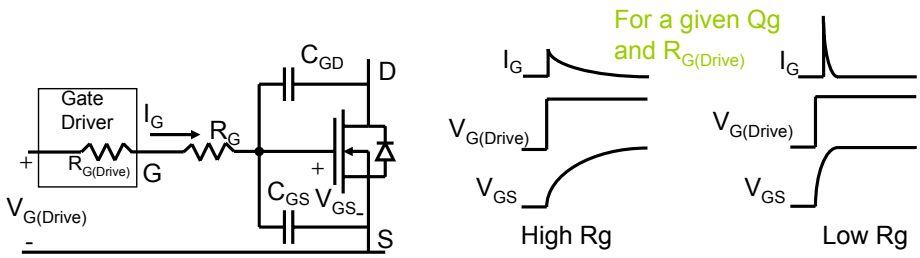
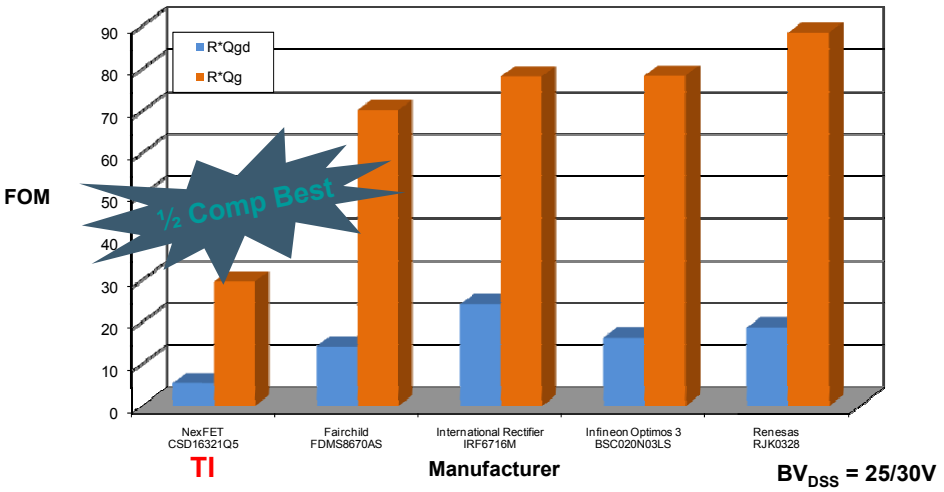
Series Gate Resistance R_G

- **Series Gate Resistance is the internal resistance which impedes the flow of Charge into the gate capacitance, slowing the switching transition.**
- **It is important in High Frequency DC-DC converters.**
- **It is in Series with the Gate Driver's Resistance.**

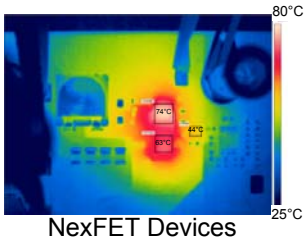
R_g	Series Gate Resistance		0.9	Ω



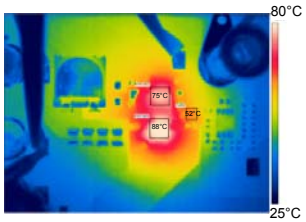
Inherently Better FOM



Efficiency Delivering Cooler Systems



NexFET Devices



Industry Standard Devices

- Up to 30% cooler operation of MOSFET
- Up to 15% cooler driver operation
- Increased Reliability

25A , 500kHz, V_{IN} = 12V, V_{OUT} = 1.3V, V_{GS} = 5V

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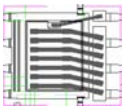
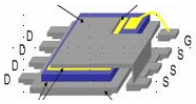
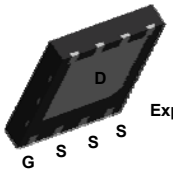
N-Ch devices

Current Package Offering

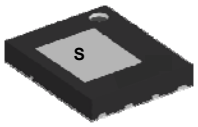
	QxA	Qx
Construction		
Outline	5x6, 2x2	5x6, 3x3
Profile	<1mm	<1mm
RoHS Compliant	Yes	Yes
Package Resistance	0.7mΩ	0.3mΩ
Ls	~0.8nH	~0.4nH

Next Gen: Dual Cool™ QFN



Exposed DRAIN Pad

EXPOSED HEAT SINK



Exposed Source Heat Sink

Part No	V_{DS}	V_{GS}	R @ 10V	R@ 4.5V	Qg	Qgd	Sample	Prod
CSD16407Q5C	25V	16V	1.8mΩ	2.5mΩ	13.3nC	3.5nC	Now	Q3CY09
CSD16325Q5C	25V	10V	-	1.7mΩ	19nC	4nC	Jun 09	Q3CY09
CSD16321Q5C	25V	10V	-	2.1mΩ	14nC	2.5nC	Jun 09	Q3CY09
CSD16322Q5C	25V	10V	-	4.4mΩ	6.2nC	1.3nC	Jun 09	Q3CY09

	Samples	Prod
QFN3x3	Q3 CY09	Q4 CY09

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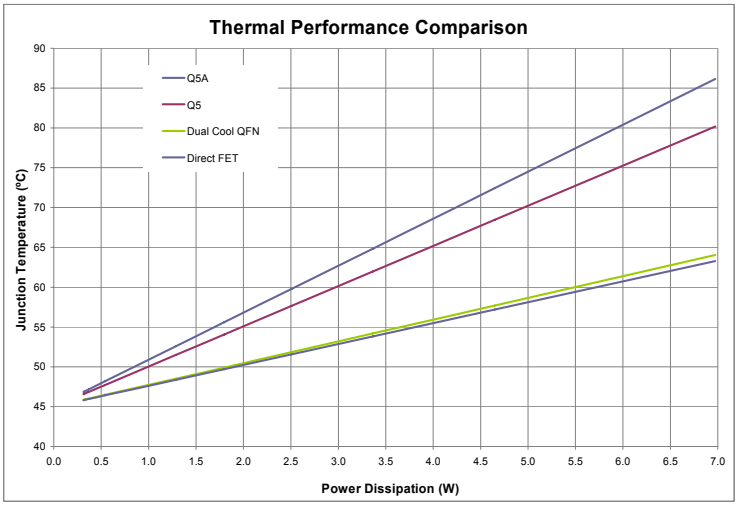
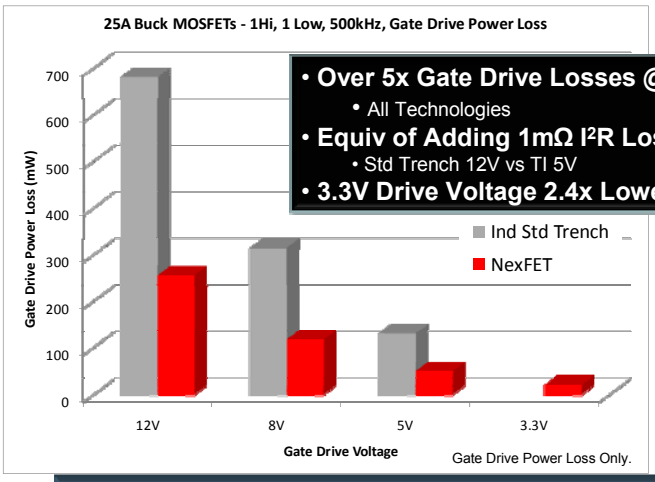
Excellent Thermal Capability



Same Thermal Performance as DirectFET package

Gate Drive Loss Increase with V_{GS}



- **Over 5x Gate Drive Losses @ 12V vs 5V**
  - All Technologies
- **Equiv of Adding 1mΩ I^2R Losses per Phase**
  - Std Trench 12V vs TI 5V
- **3.3V Drive Voltage 2.4x Lower Losses vs 5V**

V^2 Relationship of Drive Voltage to Energy wasted

$E=CV_{GS}^2$

$E=\frac{1}{2}CV_{GS}^2$ for charge and discharge of gate

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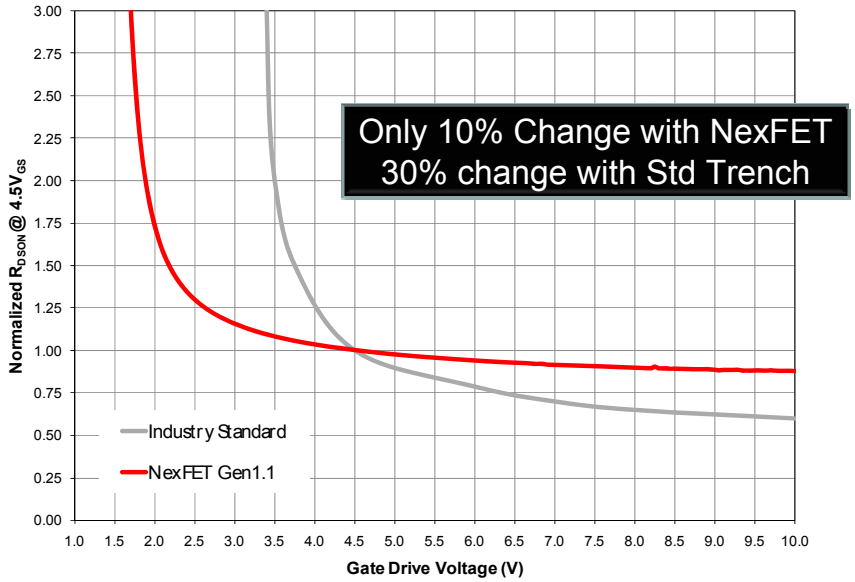
Gen1.1 – Optimized for $5V_{GS}$



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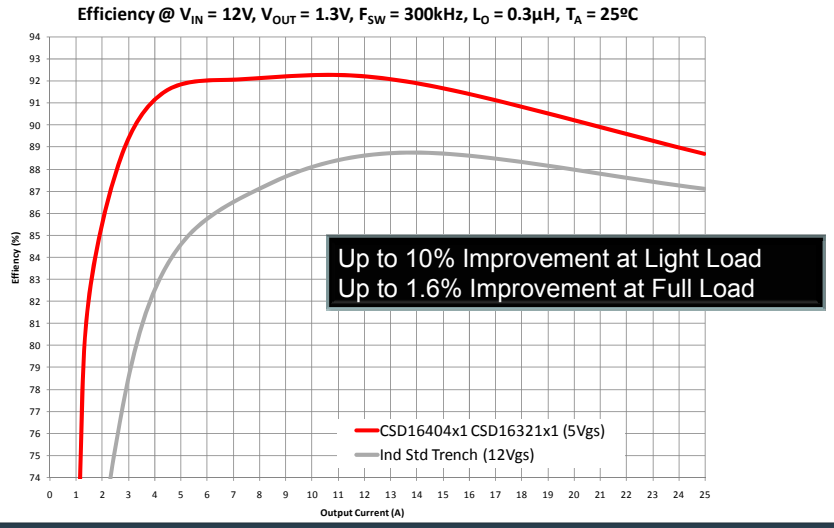
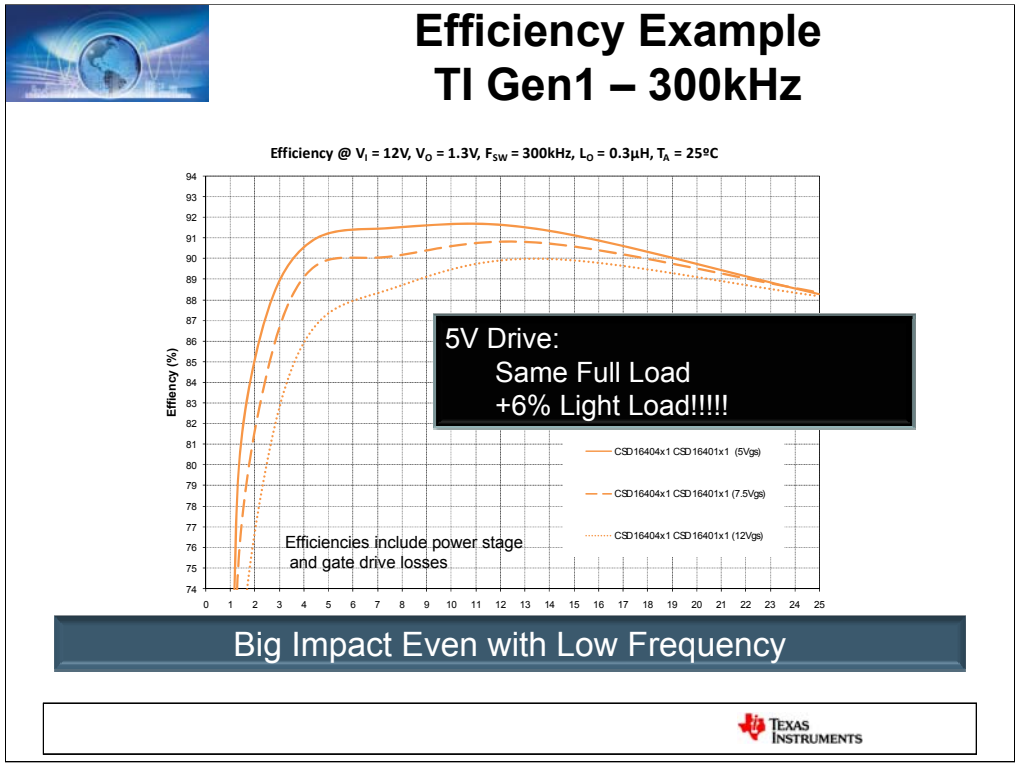
Improved Efficiency Across the Range



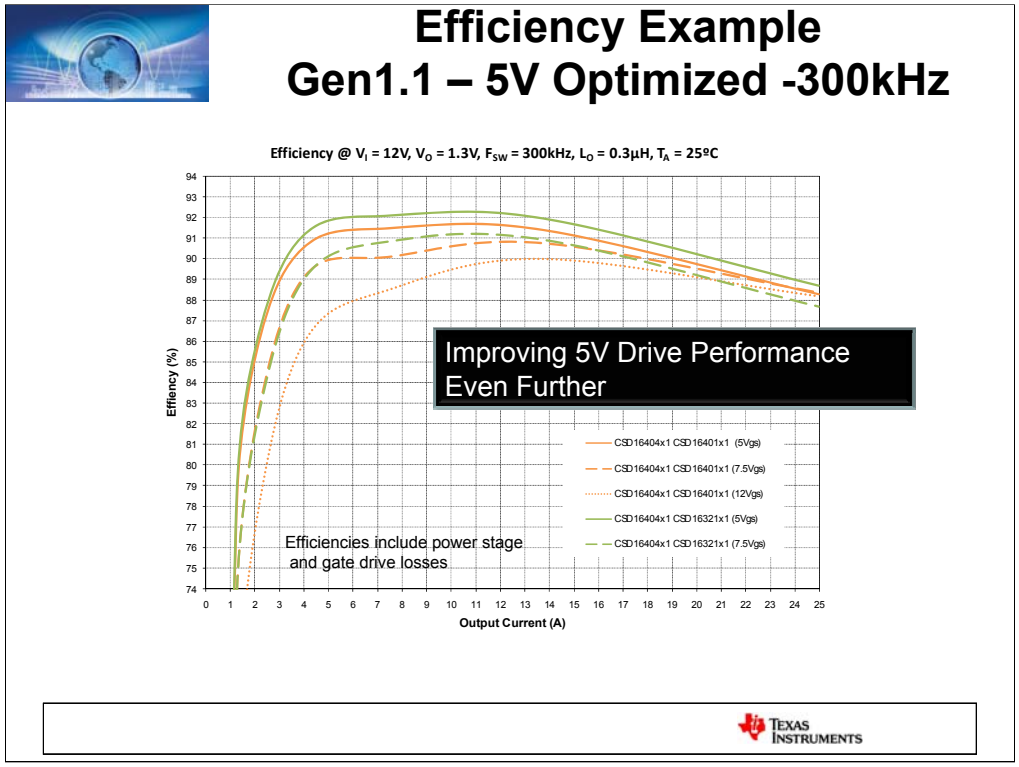
$5V_{GS}$ Better Full Load Even with Comp FET Fully Enhanced @ $12V_{GS}$



This shows that even at low frequencies with TI – 300kHz – the trade-off in going from 5V to 12V is the same, overall 5V is more efficient.

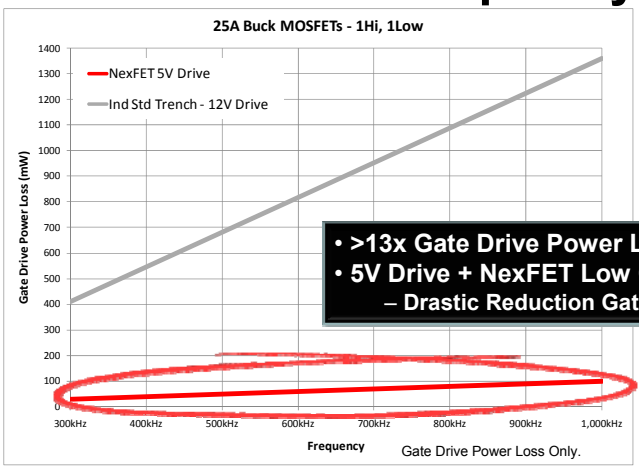
The 12V gate drive begins to cross over the 5Vgs efficiency @ 25A and if the current was extended it would be greater efficiency vs 5Vgs. But most systems today use 25A or less per phase so this is not as relevant, especially as there is a major impact on light and mid loads by going to higher drive voltage.

The 25A cross over is for this specific combination of devices. ~7mOhm high side & ~2-2.5mOhm low side. TI could insert a lower resistance low side or high side that would help extend this past 25A should higher current full load be required.



This shows how TI Gen1.5 performs vs TI Gen1, CSD16321 being an improved cost/performance vs the CSD16401. Even at 300kHz with slightly higher resistance the CSD16321 manages improved full load efficiency and throughout the entire load range. By optimizing for 5Vgs systems TI has pushed the cross over point vs 12V systems out even further beyond 25A.

Gate Drive Loss Increases with Frequency



- >13x Gate Drive Power Loss for 12V
- 5V Drive + NexFET Low Q_G
  - Drastic Reduction Gate Drive Losses

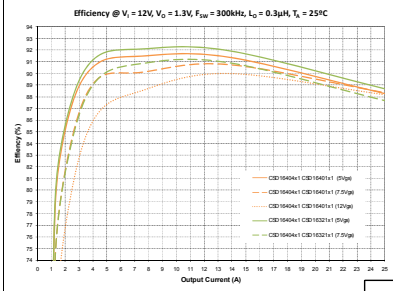
Linear Relationship to Voltage and Charge
Gate Drive Loss = V_{GS} x Freq x Total Q_G

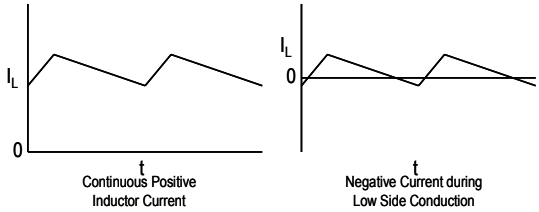
Texas Instruments

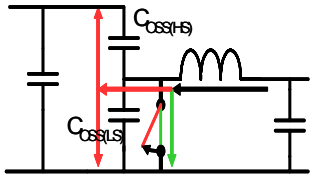
Vgs Summary

- $5V_{GS}$ Systems Delivers Highest Overall Efficiency
- NexFET Devices are Optimized for $5V_{GS}$ Gate Drive Systems
- NexFET Devices Enable Higher System Efficiency or Frequency Running @ $5V_{GS}$ versus @ $12V_{GS}$.
- Gate Drive Losses are Frequently Omitted from Efficiency Measurements.

NexFET™ "Bump"







	Positive Current	Negative Current	
P_{OSS}	½ $(Q_{OSS(HS)}+Q_{OSS(LS)})\ V_{IN}f$	Lossless	Constant with current
Prr	$Q_{RR}V_{IN}f$	Lossless	Decreases with decreasing current
$P_{SW(ON)}$	$\frac{V_{IN}I_{SW(ON)}R_{Drive}Q_{G(SWHS)}}{2V_{GS(SW)}}$	$\frac{V_{IN}I_{SW(ON)}R_{Drive}Q_{G(SWLS)}}{2V_{GS(SW)}}$	Decreases with decreasing current
$P_{SD(ON)}$	$I_{SW(ON)}V_{SD(LS)}DT$	$I_{SW(ON)}V_{SD(HS)}DT$	Decreases with decreasing current

MOSFET Selection

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Power MOSFET Selection

Clear All

Info

Show Selected

Part Number	Package	Ch	Configuration	Vds	Vgs	Rdson(mΩ) 10V	8V	4.5V	> 3V	Vgth (V)	Q10 (nC)	Q4.5 (nC)	Qgs (nC)	Qgd (nC)	Rg (Ω)	Qrr (nC)		
				36		8.91		11.52										
		N	Single	24		5.36		6.43									TI	All
CSD16409Q3	QFN 3x3	N	Single	25	16	6.2		9.5		2	8	4	2.1	1	0.6	22.9	Prod 0.85	
CSD16410Q5A	QFN 5x6	N	Single	25	16	6.8		9.6		1.9	7.95	3.9	1.8	1.1	0.65	24	Prod 0.81	

Select Socket: Cross Reference

Part Number	Package	Ch	Configuration	Vds	Vgs	Rdson(mΩ) 10V	8V	4.5V	3V	Vgth (V)	Qg10 (nC)	Qg4.5 (nC)	Qgs (nC)	Qgd (nC)	Rg (Ω)	Qrr (nC)	Company
BSC080N03LS	QFN 5x6	N	Single	30	20	6.7		9.6		1.6	15.5	7	4	1.8	1	23	Infineon Technologie

Add Manufacturer

BSC080N03LS

Record: 1 of 2 (Filtered)

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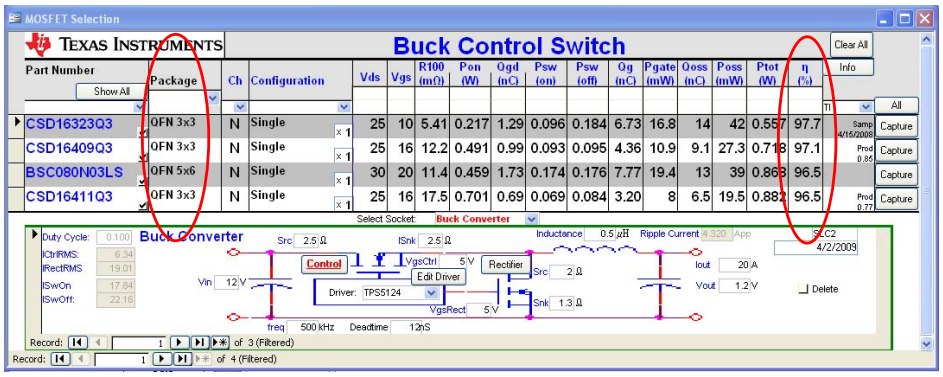
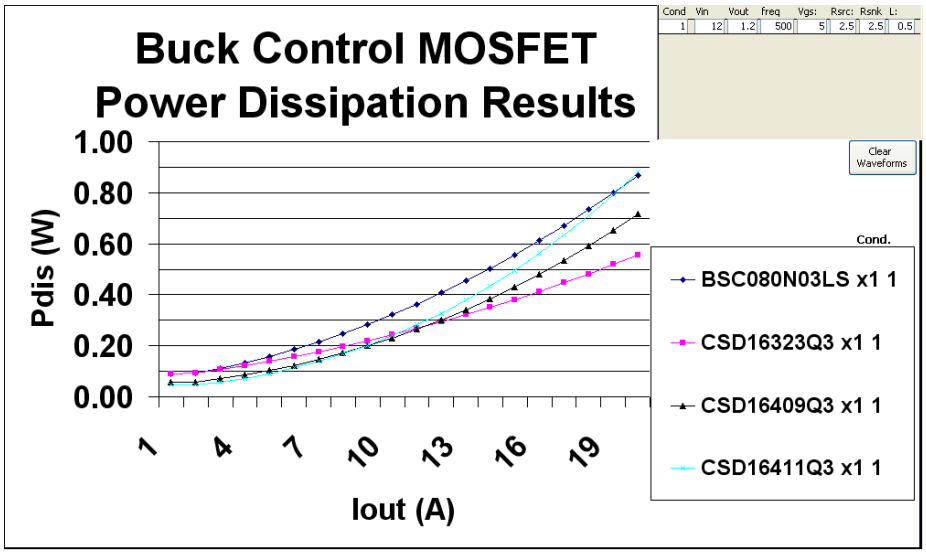
Value!!!



- Efficiency (of this component)
- Size

More Value – Low Current



Before

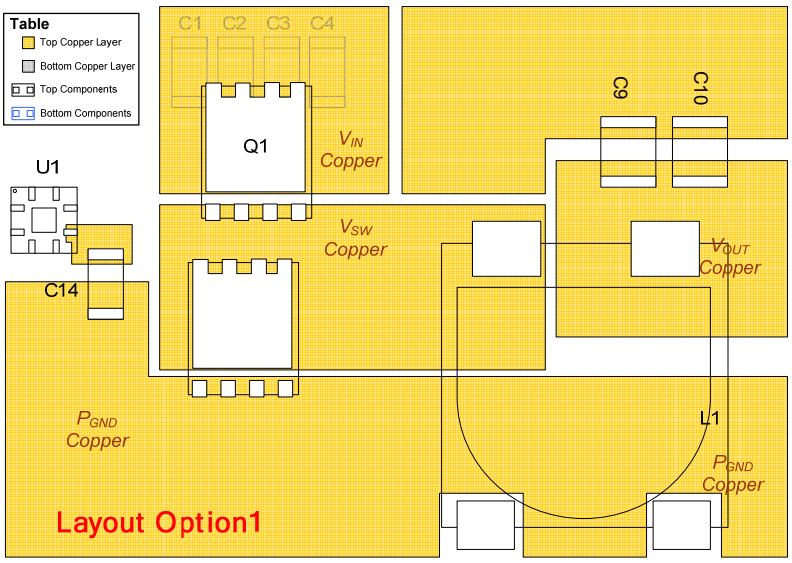
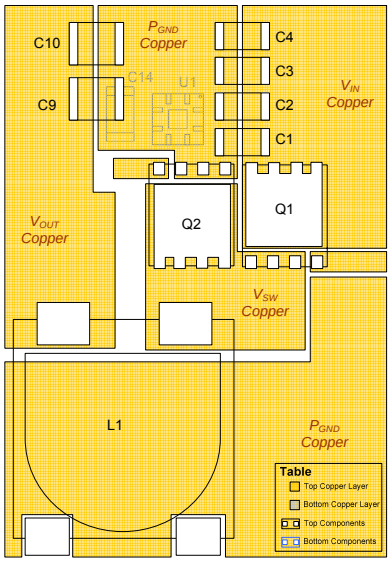


Table
Top Copper Layer
Bottom Copper Layer
Top Components
Bottom Components
C1
C2
C3
C4
Q1
V_{IN} Copper
C9
C10
U1
C14
V_{SW} Copper
V_{OUT} Copper
L1
P_{GND} Copper
P_{GND} Copper
Layout Option1

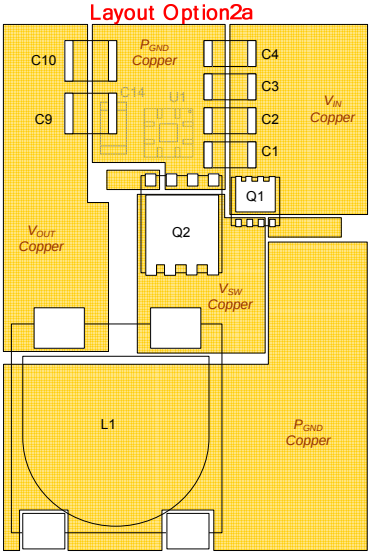
Ideal Power Stage Placement



1. Minimize distance between Positive node of input ceramic cap & Drain pin of Control FET
2. Minimize distance between Negative node of input ceramic cap & Source pin of Sync FET
3. Use minimum 4x 10uF Ceramic capacitors for input caps
   1. TDK # C3216X5R1A106M
4. Continuous flow of Power Planes

3x3mm QFN

Layout Option2a



1. Minimize distance between Positive node of input ceramic cap & Drain pin of Control FET
2. Minimize distance between Negative node of input ceramic cap & Source pin of Sync FET
3. Use minimum 4x 10uF Ceramic capacitors for input caps
   1. TDK # C3216X5R1A106M
4. Continuous flow of Power Planes

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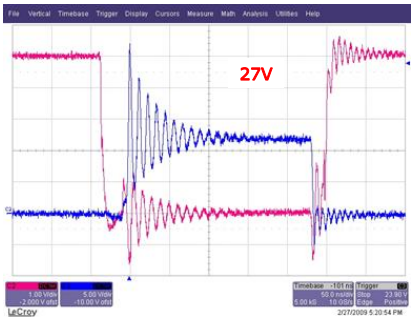
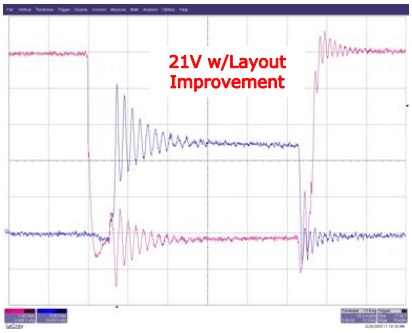
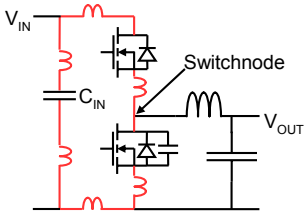
Before and After Effects

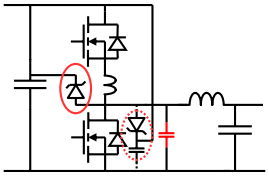




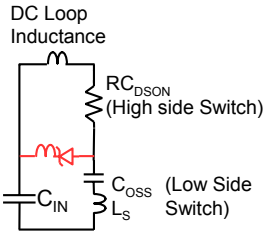
Schottky Clamp



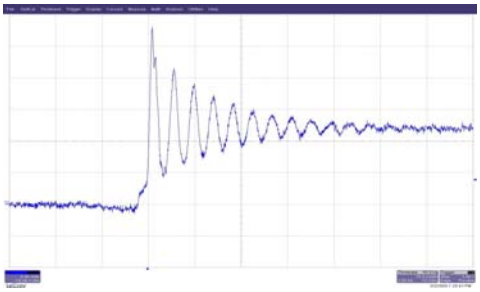
Buck Converter
DC Loop and associated stray inductances in red



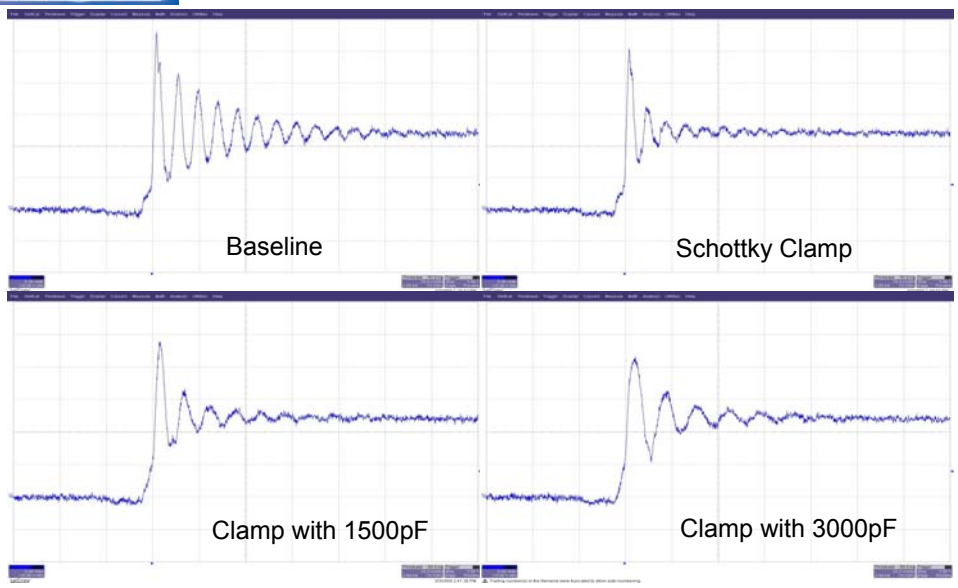
Equivilant Circuit DC Loop After High Side MOSFET turns on



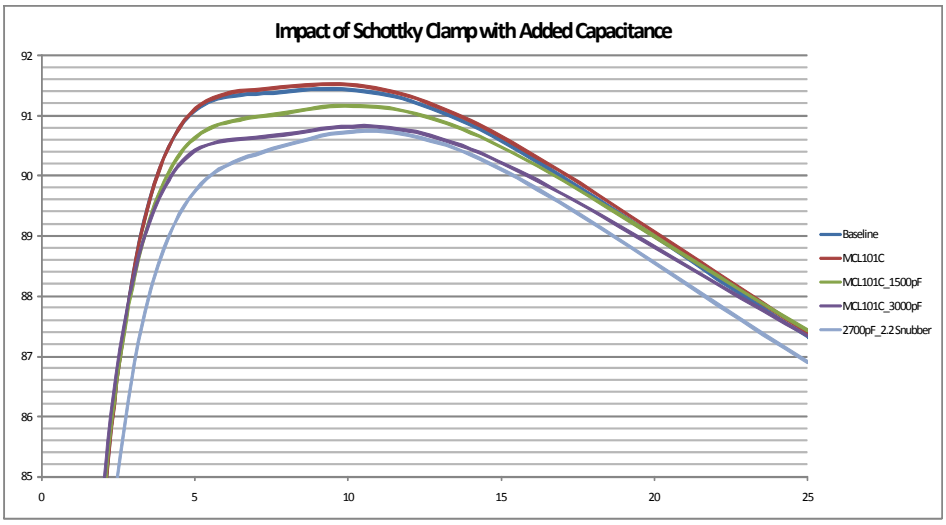
Equivilant Circuit With Schottky Clamp



Switchnode Waveforms

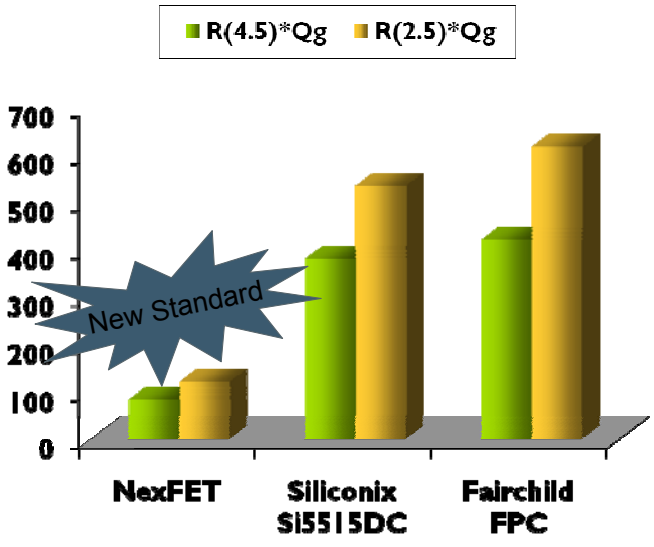


Efficiency – Standard Demo Board



P-Channel DC-DC Switch

6+ Year Technology Lead



BV_{DSS} = 20V

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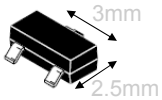
P-Ch devices

Wafer Level Package vs Industry Std Packages

SOT-23



7.8mm^2
25mΩ
Si2333

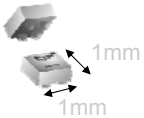
~8x Footprint Reduction
~2x Resistance

Ciclon WLP

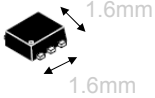
SC-70

4.2 mm^2
70mΩ
Si1417

4x Footprint Reduction
Same Resistance



SC-89



2.56 mm^2
108mΩ
Si1065

2.5x Footprint Reduction
~ ½ Resistance

1mm2
66mΩ
CSD23201

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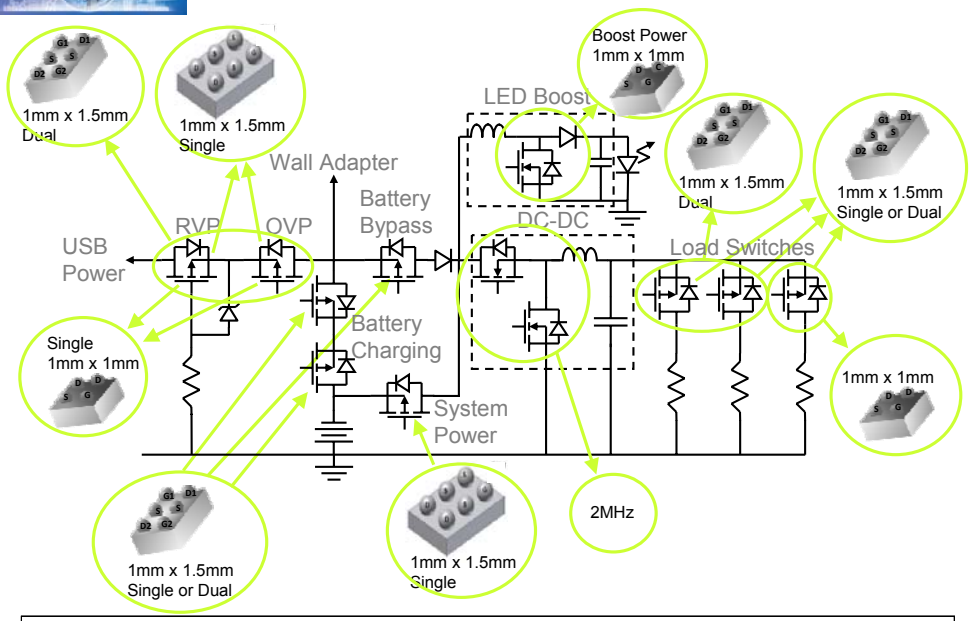
Saving Space & Cost



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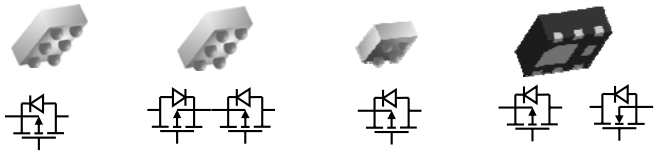
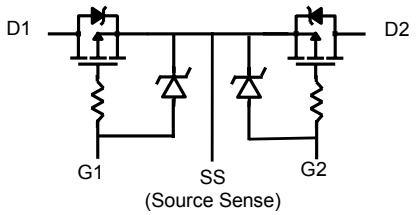
NexFET Discrete Products

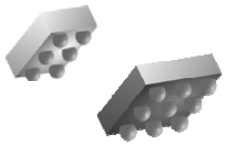
	CSD25301W1015	CSD75301W1015	CSD23201W10	CSD16301Q2* CSD25302Q2*
	Single P	Dual P Common Source	Single P	Single N & Single P 1MHz
	1mm x 1.5mm WLP	1mm x 1.5mm WLP	1mm x 1mm WLP	2mm x 2mm QFN
BV_{DSS}	-20V	-20V	-12V	+25V / -20V
V_{GS}	8V	8V	5V	8V
	$R_{DS(on)}$ typical	$R_{DS(on)}$ Typical	$R_{DS(on)}$ typical	$R_{DS(on)}$ typical
4.5V	62mΩ	80mΩ	66mΩ	28/39mΩ
2.5V	80mΩ	101mΩ	77mΩ	36/56mΩ
1.5V	175mΩ	165mΩ @ 1.8V	110mΩ	Qg 1.9/2.7nC

*- in development



Dual Common Source with Clamp Diode

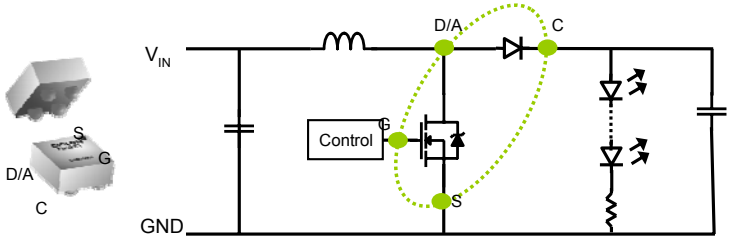




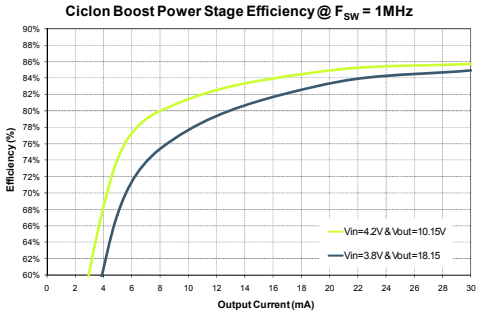
Part Number	Package	$BV_{D1 D2}$	R_{DD}@4.5V	R_{DD}@2.5	Gate Clamp BV_{GSS}	Gate ESD	Samples	Prod
CSD75204W15	WLP 1.5x1.5	20V	100mΩ (50mΩ each)	130mΩ (65mΩ each)	6.1V min	3kV	Now	Q2 CY09
CSD75205W1015	WLP 1x1.5	20V	144mΩ (77mΩ each)	190mΩ (95mΩ each)		3kV	Now	Q2 CY09

Small Scale Integration

Monolithic Boost LED Power Stage



Up to 4x Smaller



24V Power Stage

Part Number	Function	BV_{DSS}	V_{GS}	$R_{DS(on)}$ @4.5V
CSD86301W10	Power Stage	24V	+10V/-6V	315mΩ
Qg @4.5V	Qgd	V_F @ 20mA	Leakage @25°C	Package Size
0.14nC	0.03nC	0.59V	1μA	1mm x 1mm

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Unique NexFET Technology Capabilities

- Extremely low charge MOSFETs with low resistance
  - RF Power LDMOS structure with vertical current flow
  - Enables higher switching frequency and high current
- Low voltage gate drive capabilities
  - Low loss high switching frequency
  - Planar gate. Using standard CMOS Gate Oxides
- Enables integration in a cost effective process
  - Planar structure
  - Chip scale packages
- Technology in early stage of maturity
  - In infancy leading 20 years of trench development

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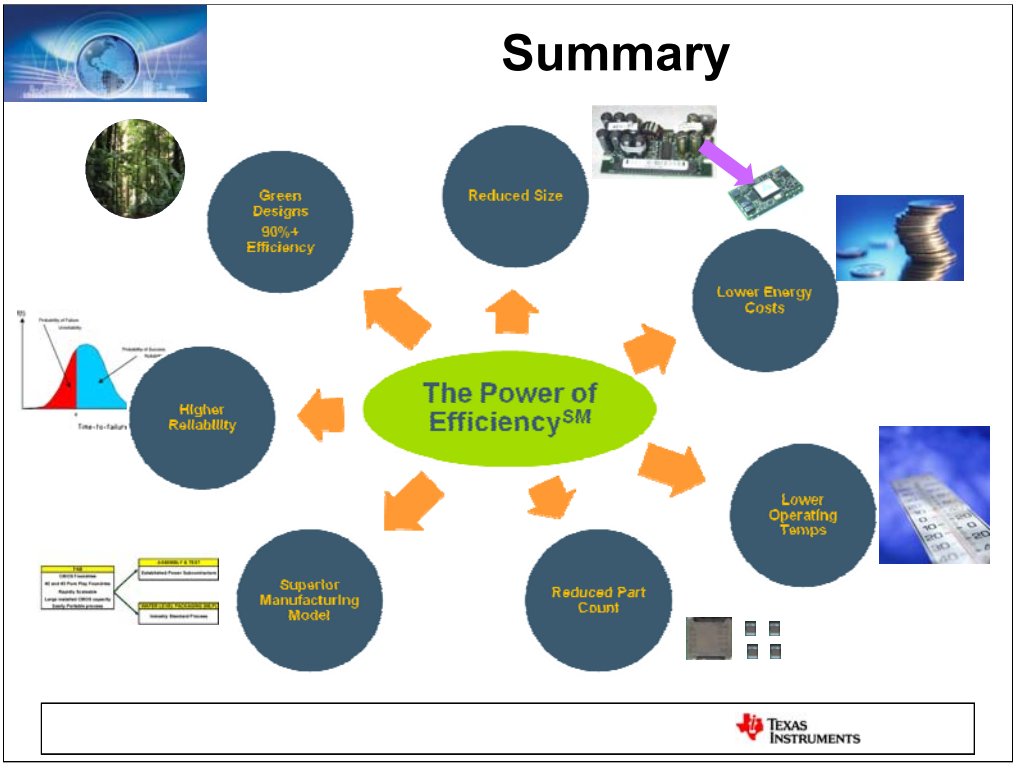
Summary
Green Designs 90%+ Efficiency
Reduced Size
Lower Energy Costs
Higher Reliability
The Power of Efficiency℠
Lower Operating Temps
Superior Manufacturing Model
Reduced Part Count
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THANK YOU!!