



System Level Protection with TI's IPD Solutions September- 2009

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**Utility & Interface Group
SLL, Texas Instruments Inc.**





Agenda

- Brief Summary of ESD & IEC Standards
- Why Do We Need IPD Solutions?
 - Benefits of External ESD/ EMI Solutions
- What are the End-Equipments for IPDs?
- What are the Key Parameters for IPDs?
- How to Select the right ESD Solutions form TI for your Application
- IPD Product Roadmaps
 - How TI Adds More Value to System Designers?



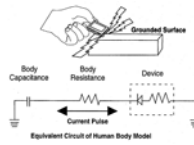
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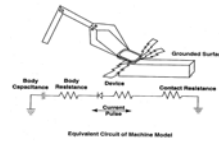


Device Level ESD Testing

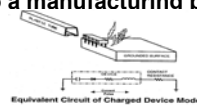
- Human Body Model (HBM)
 - Simulates a human body discharging the accumulated static charge through a grounded device.



- Machine Model (MM)
 - Simulates a robotic arm discharging accumulated static charge through a grounded device



- Charge Device Model (CDM)
 - Simulates a charged device (due to a manufacturing process) that is subsequently grounded.



The ESD threat can come from humans as well as machines and these are represented by the three important stress models: the Human Body Model or HBM, the Machine Model or MM, and the Charged Device Model or CDM. The MM is very similar to the HBM but is losing its relative importance. Meanwhile, CDM, which is caused by the discharge from a package itself, is rapidly becoming a sensitive issue. Even when the chip is in the system it can be subjected to ESD which is represented as the IEC system level simulation. The details of the various models are given in later slides.



Device Level ESD Model Comparison

Model	HBM	MM	CDM
Test Levels (Volts)	500, 1000, 1500 2000, 2500	100, 150, 200	250, 500, 750, 1000
Pulse Width (ns)	~150	~80	~1
Rise Time	2-10 ns	n/a	<400 ps
Typical ESD Failures	<ul style="list-style-type: none">• Junction Damage• Metal Penetration• Metal Melt• Contact Spiking• Gate Oxide Damage		<ul style="list-style-type: none">• Gate Oxide Damage• Charge Trapping• Junction Damage



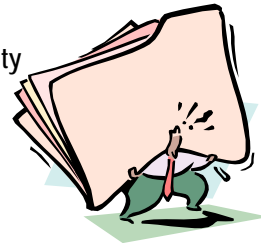
The three models are represented here where HBM has the longest pulse width at 150 ns, followed by MM at 80 ns, and CDM at 1 ns. The rise times are also different. The CDM rise time at <400 ps is much faster than for the other models. Note again that the damage phenomena to HBM and MM are the same but different from CDM.



System Level Specifications

IEC 61000-4-xx is a set of about 25 testing specs from the IEC

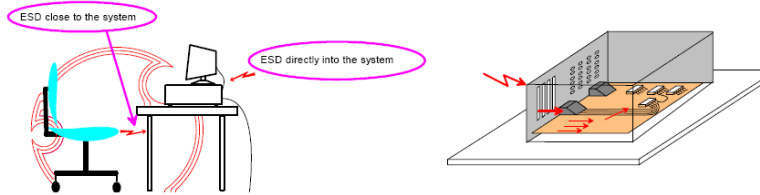
- 2: ESD Immunity
- 3: Radiated RF EM Field Immunity
- 4: Electrical Fast Transient Immunity
- 5: Surge Immunity
- 6: Conducted RF Immunity
- 8 -9 -10: Magnetic Field Immunity
- 11: Voltage Dips & Variations Immunity
- ... many more





How does ESD Enter a System?

Coupling mechanism	Consequences	Possibility
Current/charge injection	Damages the gates of MOSFETs and CMOS devices Triggers latch-up in CMOS devices Causes a voltage pulse on conductors ($V = L \cdot di/dt$)	Very common Common Common
Electric field coupling	Capacitively couples to nets with a large surface area and generates high electric field	Rare
Magnetic field coupling	Induces currents in every wiring loop in the vicinity and causes soft failures	Very common
Electromagnetic coupling	EM field couples into long wires that act as receiving antennas	Rare

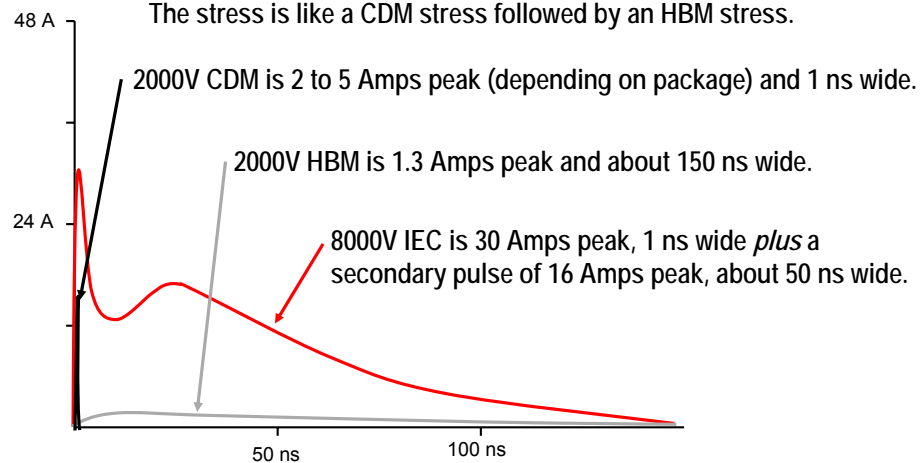




Comparison of Device Level & System Level ESD Specifications

How does the IEC ESD stress differ from the tests we've been doing?

The stress is like a CDM stress followed by an HBM stress.



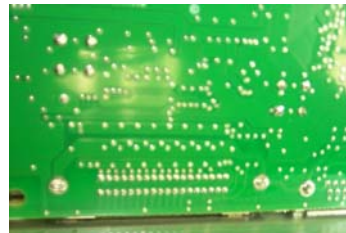


Common Techniques to Protect Systems from ESD/ EMI

- Metallic shielding for both ESD and EMI
- Chassis GND isolation from board GND
- Air gap designed on board to absorb ESD energy
- Capacitors to divert ESD energy
- Meticulous Board Layout Design to suppress ESD/ EMI stresses
- **Stand alone IPD solutions**



Interface with IPD Solutions



Board layout with isolated chassis GND



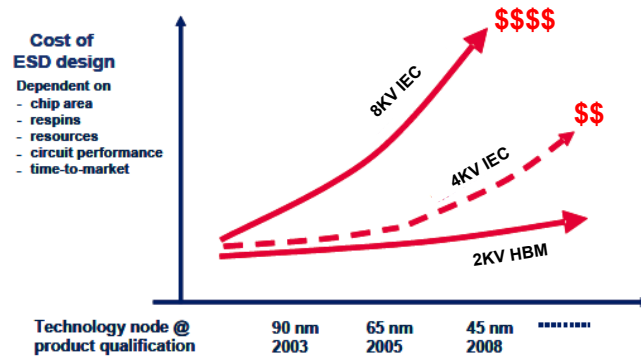
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Why External ESD Protection?

It becomes very expensive to design IEC Clamp at low geometry process

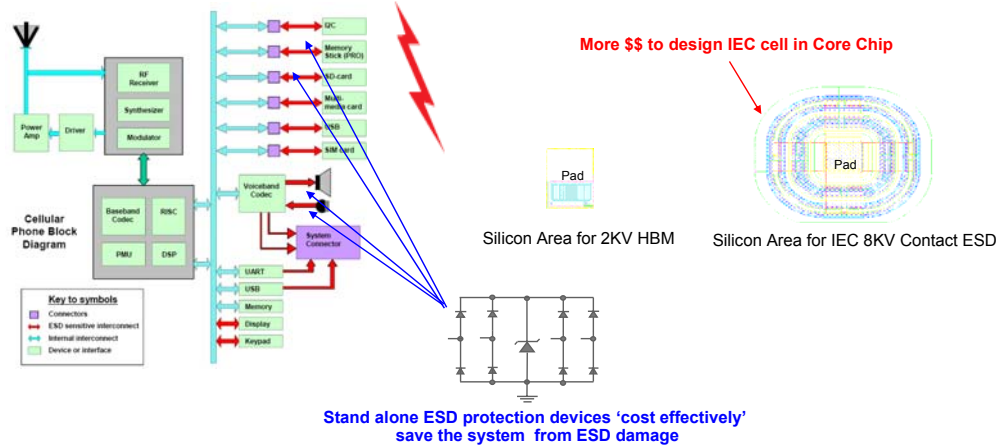


With advanced process we need more die area to design the same IEC Cell
- You can scale down the core design , but you can't scale down the IEC Cell



Why External ESD Protection?

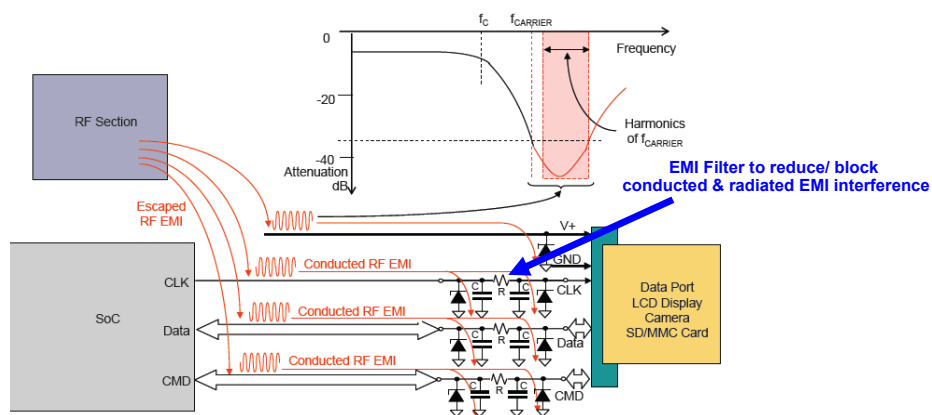
- It is **technically** and **economically** challenging to integrate IEC ESD in core ICs based off advanced process nodes
- External Connectors, Keypad, Side keys, Audio Jack, etc. are sensitive to system level ESD
 - It takes only one ESD stress to damage a system!





Why EMI Filter?

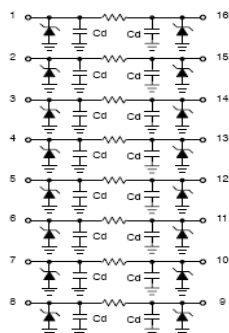
- RF section of portable equipments generate conducted and radiated EMI interference
- Non-optimized board layout often generates EMI interference among signal lines
- EMI interference can cause both functional and reliability failure



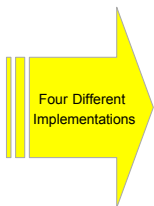


Integrated Protection Devices Vs Discrete Solutions

Board Space Saving



8-Channel EMI Filter



Board Space: Discrete Versus TI IPD Solutions

TI's Integrated Protection Devices provide significant board space saving over discrete:

- 1) Silicon level integration of resistors, capacitors, inductors
- 2) Eliminate the routing through the board except for filter input, output lines



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IPDs Can Be found in Almost any Applications

There is no System without Interface!





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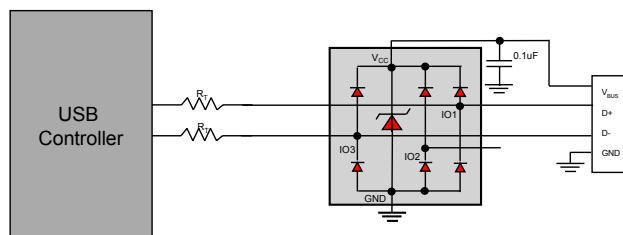
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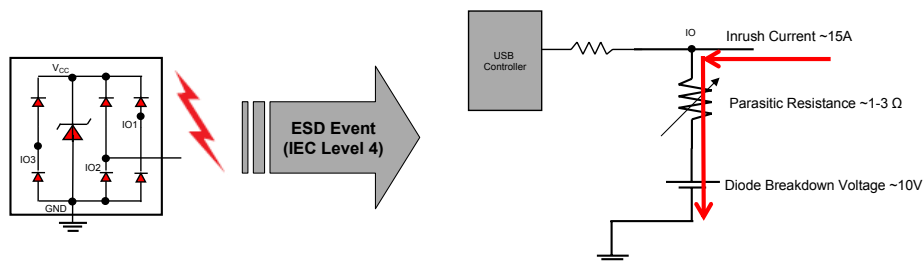
Important Parameters for ESD Clamps

Key Considerations

- ESD Ratings
- IO Capacitance
- Dynamic Resistance
- IO Voltage Tolerance
- Breakdown Voltage
- Package



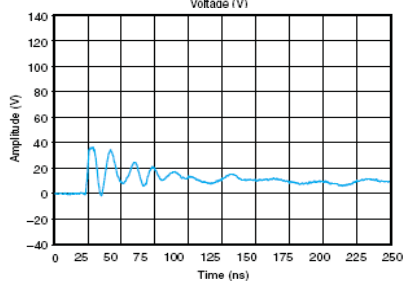
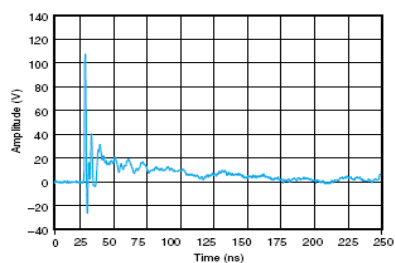
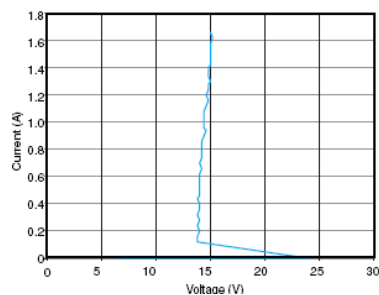
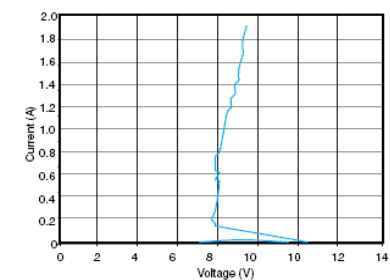
TPD3E001 in USB2.0 (480Mbps) Application



ESD Event: Equivalent Circuit Representation



Example of IPD Plots (TPD4S012)



V-I & IEC Clamp for the D+,D-,ID pins

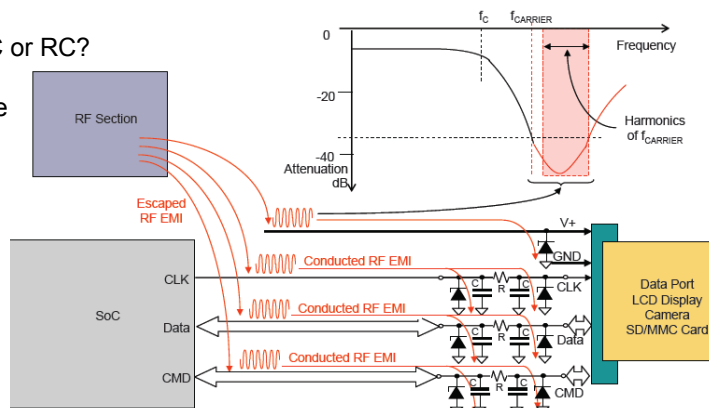
V-I & IEC Clamp for the VBUS pins



Important Parameters for EMI Filters

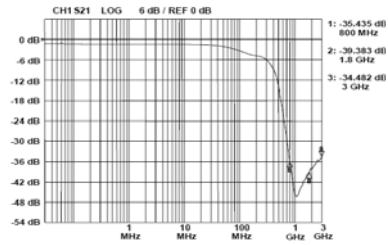
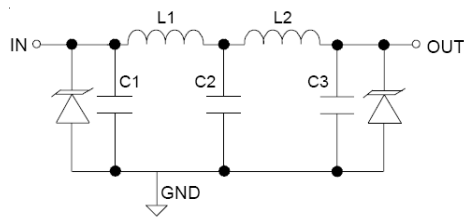
Key Considerations

- Cut-off Frequency
- Pass-band Attenuation
- Stop-band Attenuation
- Package Parasitic
- Filter Topology- LC or RC?
- ESD Ratings
- Breakdown Voltage

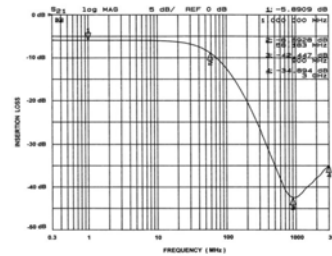
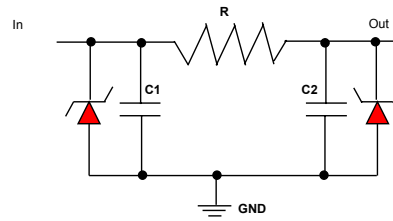




EMI Filter: L-C vs R-C?



More challenging to manage series inductor



Less noisy and easy to design with



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IPD Opportunity By Interface

	Data-Rate	Signal Swing	# of Data Lines	Common Applications	ESD Solutions
USB 2.0	480Mhz	Data swing 0mV to 400mV VBUS = 5V	3 Data lines +1 VBUS	Computing, Portables	TPD3E001 TPD4S012 TPD2S017
USB3.0	5Gbps	Data swing 0V to 400mV VBUS = 5V	6 Data lines +1 VBUS line/ 7 Data lines +1 VBUS line	Computing, Portables	TPD2E009 TPD4S010
VGA	<50Mbps	Data line 0.7V Control line 5V	5 Line (9-pin connector)/ 9 line (15 pin connector)	Consumer, Computing	TPD4E001 TPD6E001, TPD6S019*
DVI/ HDMI/ DisplayPort	3.4Gbps	Data Swing 2.7V to 3.3V Control Lines up to 5V	12 Data Lines	Consumer, Computing	TPD8S009 TPD12S520 TPD12S521
LVDS	1.2Gbps	-4V to 5V	2 Line or multiples	Communication, Industrial	TPD2E007
SDIO	<50Mbps	3.3V	7 Lines	Portables	TPD4E001 TPD4E002, TPDxF003
RS-485/ RS-422/ RS-232 CAN	>200Mbps	-15V to 15V	2 Line or multiples	Communication, Industrial	TPD2E007
LCD Display/ KeyPad/ Memory	<100MHz	0V to 5V	Multiples	Portables, Consumer	TPD6F002, TPDxF003
Audio	<20KHz	-5V to 5V	2 Lines	Portables, Consumer	TPD2F702, TPD2E007
eSATA	6 Gbps	1V	4 Line	Computing	TPD2E009

* IN DEVELOPMENT



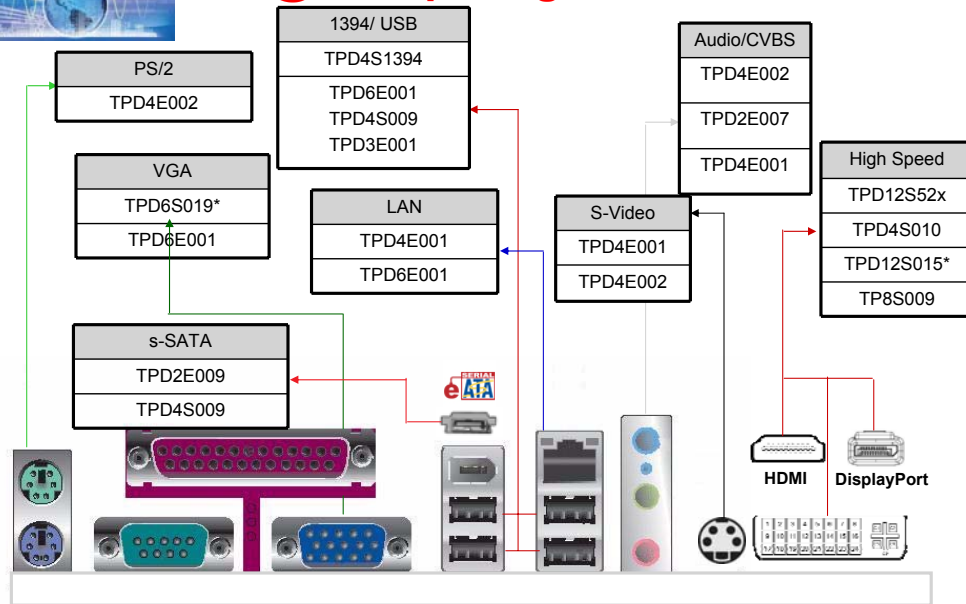


IPD Solution for Portable Applications

		Audio	Keypad	LCD Display	uSD Card	SIM Card	USB Charger	MIPI
ESD Only	TPDxE001 2, 3, 4 & 6 ch, Cin=1.5pF				√	√	√	√
	TPD4E002 4 ch, Cin=11pF, Vbr=6V	√	√					
	TPDxE004 4 & 6 ch, Cin=1.6pF, Vbr=6V			√	√	√		
	TPD2E007 2 ch, Cin=14pF, 0.8x 0.8 mm	√	√					
	TPD2E009 2 ch, Cin=0.7pF, 1.0x 1.0 mm							√
	TPD4S012 4 ch, Cin=0.9pF, 20V Vbus clamp						√	
	TPD4S014 4 ch, Cin=0.9pF, 15V Vbus clamp						√	
ESD+ EMI	TPD6F002 6 ch, Cin=17pF, R=100Ω		√	√				
	TPDxF003 4,6,8 ch, Cin=9.5pF, R=100Ω			√	√	√		
	TPD2F702 2 Ch, Cio = 5nF, R = 15Ω	√						



IPD @ Computing/ TV Interface



*IN DEVELOPMENT





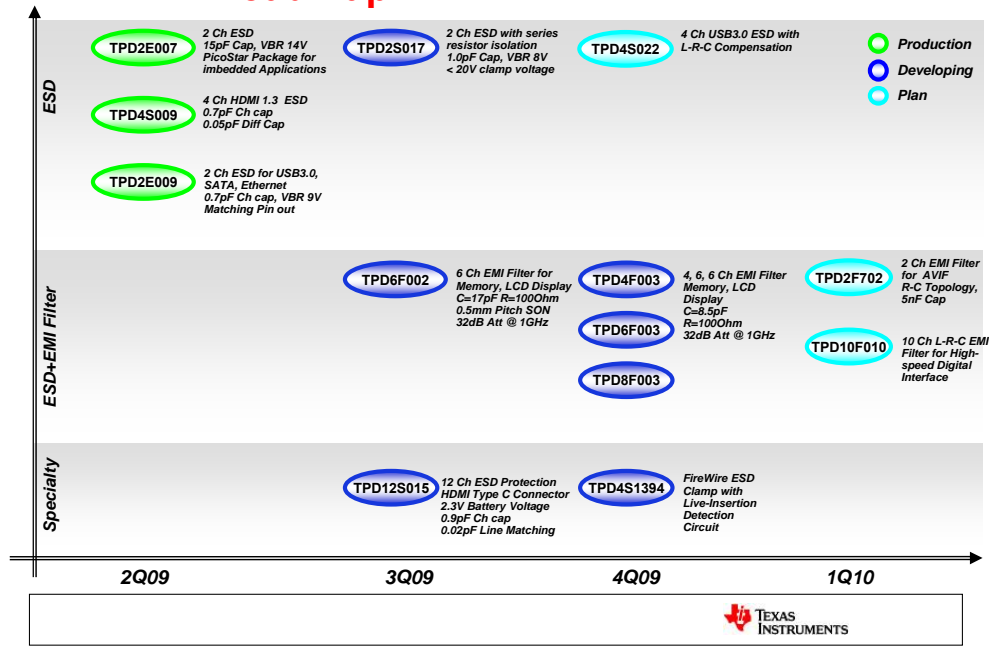
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Integrated Protection Devices Roadmap

Broad Portfolio
20 Released Products
And Growing
www.ti.com/esd





IPD Solutions- Why TI?

Easy Supplier To Work With

- We offer application specific ESD, EMI solutions that are compatible with the core micro-controller or connector interfaces
 - We can demonstrate ESD, EMI compatibility in reference boards based off TI core chip-set
- We can integrate many of the discrete components (active and passive) on your board
- We offer reliable second source options in the ESD, EMI areas

Broad Portfolio

- We Continue to invest in new ESD, EMI solutions as part of the TI-analog strategy
- Pb-Free/Green products

Reliable

- "Best in industry" obsolescence performance (one device ~4 years)



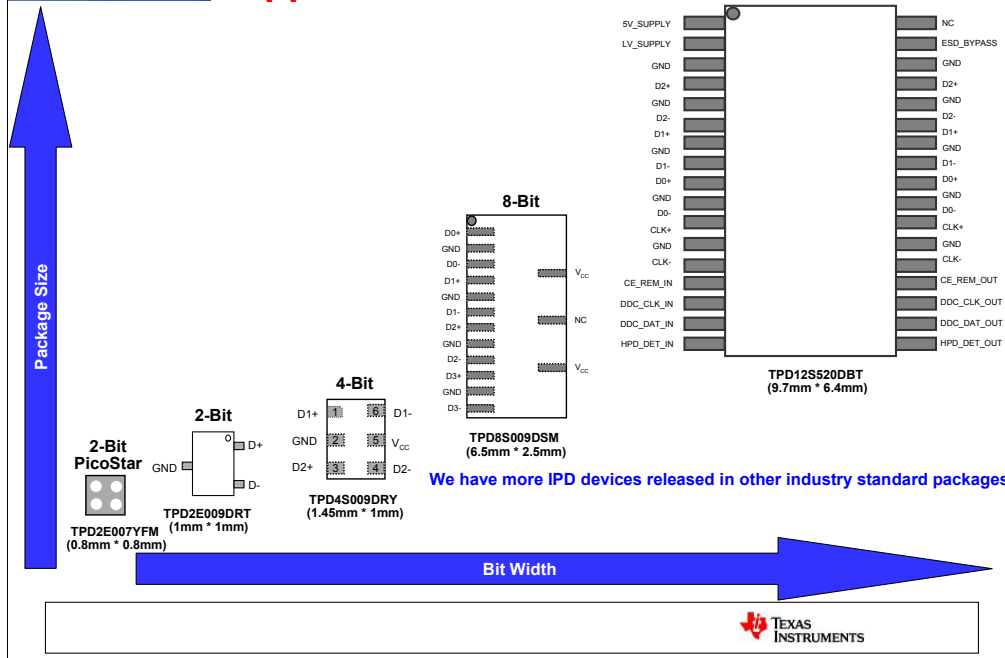
Responsive

RFQ

**Documentation – data sheet, Q/A documentation, etc
problem solving**



We have Wide Package Solutions for Applications



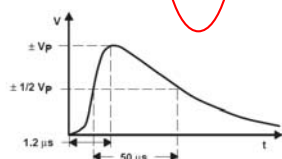
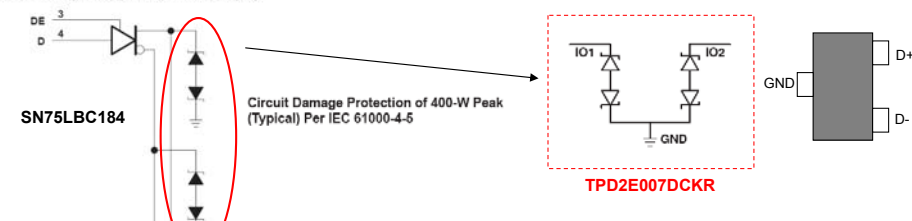


Sample Now

TPD2E007 in DCK Package

- The TPD2E007 can handle interfaces that need to swing both positive and negative signals ($\pm 14V$ min)
- The TPD2E007 has very robust ESD protection which is suitable for industrial interfaces

functional logic diagram (positive logic)



Key Requirements

- We need to pass 15KV Air-gap & 8kv Contact
- We need to check this solution for Surge capability for industrial application

Figure 1. Surge Waveform — Combination Wave



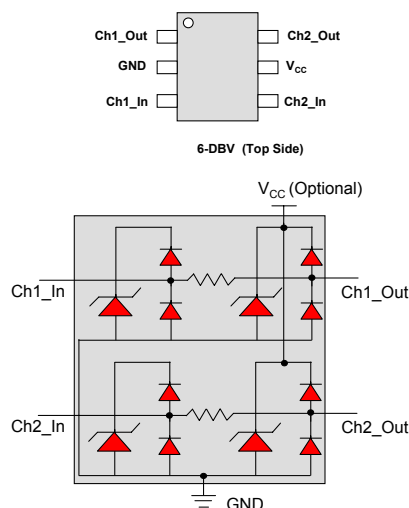


TPD2S017: Dual Channel ESD with Series Resistor Isolation for USB Port

[Sample Now](#)

Key Features:

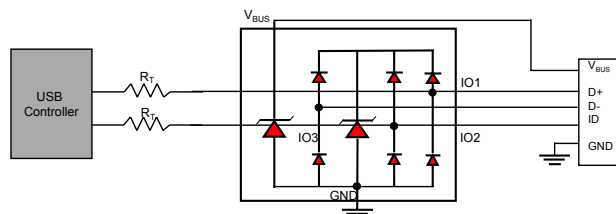
- Ultra low clamp voltage ensures the protection of ultra-low voltage core chipset during ESD events
- Drop-in for the **CM1231**
- Matching-of-series resistor ($R = 1\Omega$) of $\pm 10\text{m}\Omega$ typical
- Differential channel input capacitance matching of 0.05pF typical.
- High speed data rate and EMI filter action at high frequencies (-3dB bandwidth $\sim 2\text{GHz}$)
- Available in a 6-pin DBV package
- Flow-through Single-In-Line Pin Mapping for the High-speed Lines Ensures no Additional Board Layout Burden while Placing the ESD Protection Chip near the Connector





TPD4S012: USB Charger ESD Solution

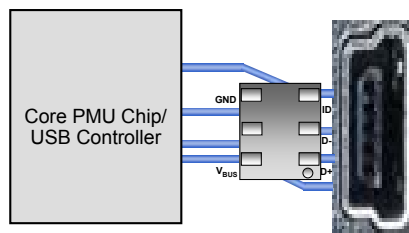
Released



TPD4S012 in USB2.0 Application

Single-chip ESD solution for USB charger port

- System level IEC-61000-4-2 (Level 4) ESD protection
- USB HS Lines (D+, D-, ID)
 - ~0.9pF Line Capacitance for
 - 6-V (min) Tolerance
- VBUS Line (V_{BUS})
 - ~9pF Line Capacitance
 - 20-V (min) Tolerance

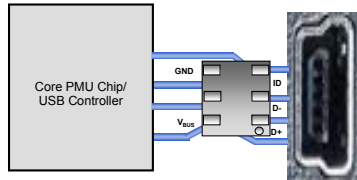


Board Layout with the TPD4S012DRY
DRY (1.45mm × 1mm × 0.55mm)

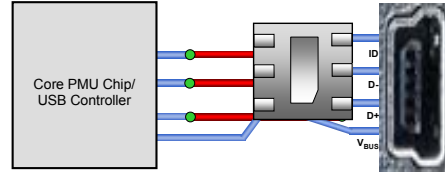




Layout Comparison: TPD4S012DRY & RClamp1654



Board Layout with the TPD4S014DRY (or, TPD4S012DRY)
(1.45mm × 1mm × 0.55mm)



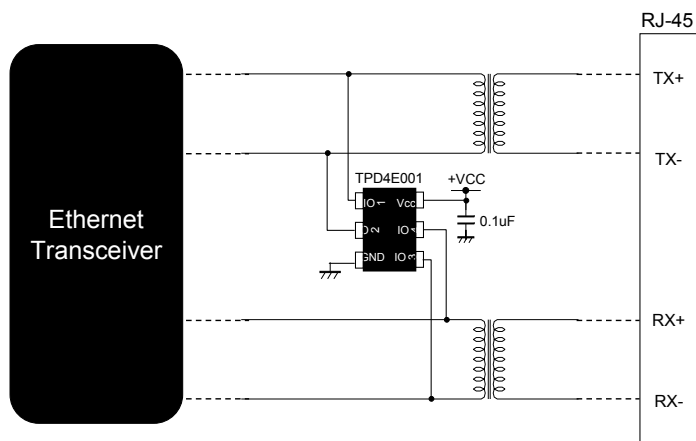
Board Layout with the Competition Package (1.6mm × 1.6mm × 0.58mm)

Parameters	TI TPD4S014	Semtech Rclamp1654	Comments
Package Size	1.45mm × 1mm	1.6mm × 1.6mm	Competition package 75% bigger than TI package
Central GND Pad	No	Yes	<ul style="list-style-type: none">TI package allows flow-through layout while mounted either side of the boardSemtech package needs via to route the high-speed D+, D- lines



TPDxE001: 10/1000BASE-TX PROTECTION

Released





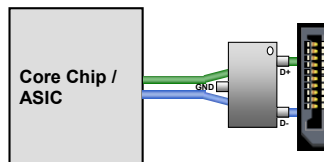
TPD2E009

Two Channel ESD for High-speed Differential Signal

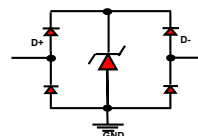
Released

Key Performance Parameters

- 3-db Bandwidth in excess of **4GHz**
- Optimized package, pin-mapping for high-speed differential lines
- System level ESD protection:
 - ✓ IEC 6100-4-2 Level 4 Spec
 - ✓ 5-A Peak Pulse Current (8/20 ms Pulse)
- Differential matching less than 0.05pF
- Pin capacitance Less than **0.7pF**



Layout Example at DisplayPort Interface



Part Number	Package
TPD2E009	SOT-3 (DBZ) SON-3 (DRT)



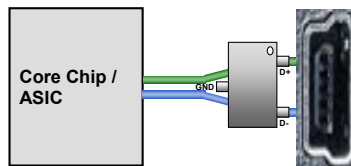


TPD2E4P50

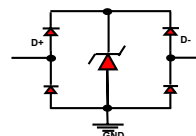
Two Channel ESD with Robust ESD/ Surge Specification

Key Performance Parameters

- 3-db Bandwidth in excess of **1.5GHz**
- Optimized package, pin-mapping for high-speed differential lines
- System level ESD protection:
 - ✓ 15KV IEC Contact ESD
 - ✓ 10-A Peak Pulse Current (8/20 ms Pulse)
- Differential matching less than 0.05pF
- Pin capacitance Less than **1.6pF**



Layout Example at USB2.0 Interface

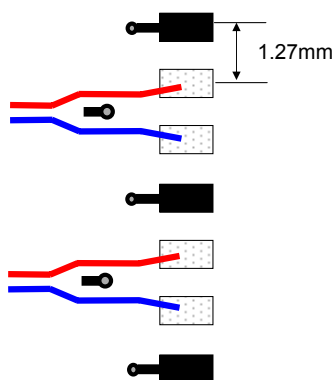


Part Number	Package
TPD2E4P50	SOT-3 (DBZ) SON-3 (DRT)

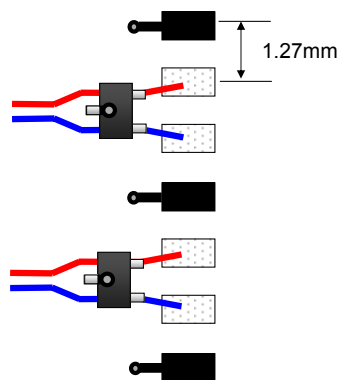




TPD2E009DRTR @ eSATA Connector Interface



Board Layout for DRT Package



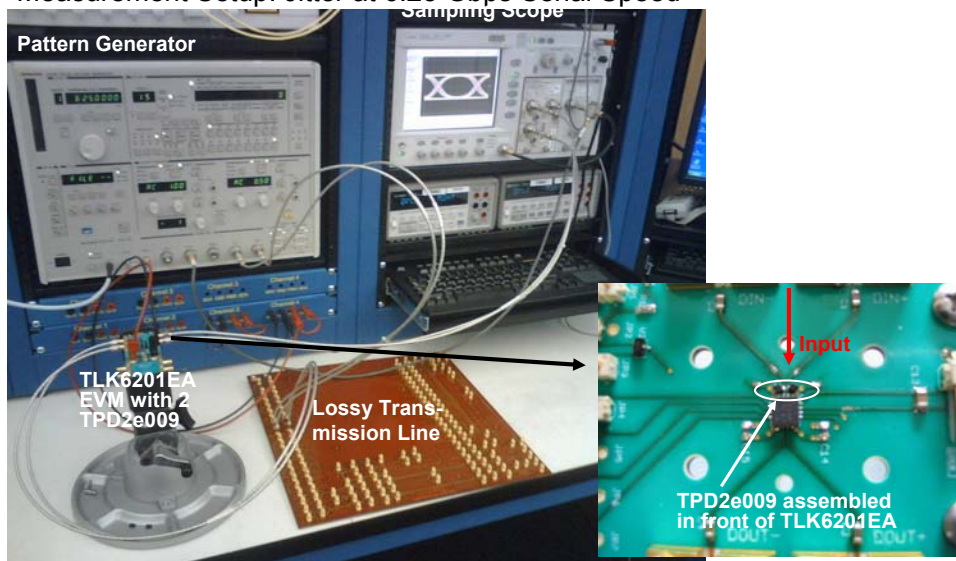
TPD2E009DRTR @ the eSATA Port

LEGENDS: — D+ — D- — GND ● GND VIA



Verification: Combine TPD2E009 and TLK6201EA

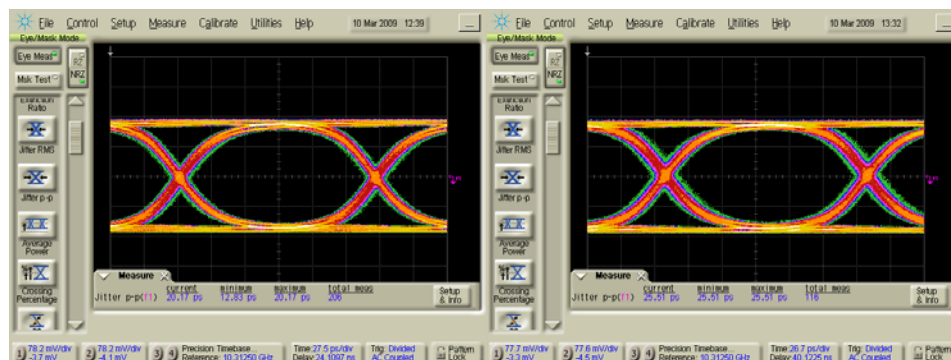
Measurement Setup: Jitter at 6.25 Gbps Serial Speed





Verification: Combine TPD2E009 and TLK6201EA

Measurement Results at 6.25Gbps Serial Speed



Output eye diagram without TPD2e009

Output eye diagram with TPD2e009

Addition of the TPD2e009 in the signal path results in a ~5 ps jitter penalty which is acceptable. The TPD2e009 has a very small impact on signal quality. The output eye quality after the equalization by the TLK6201EA is still excellent!



TPD12S520: HDMI Receiver ESD Solution

Released

Key Performance Parameters

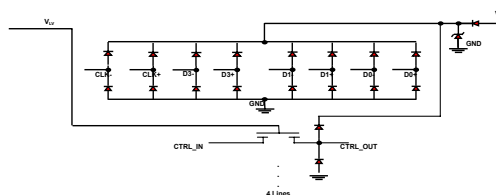
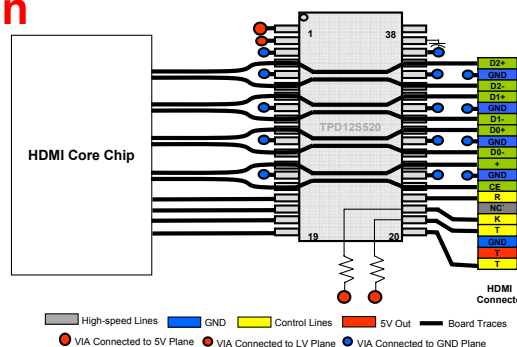
- System level IEC 61000-4-2 (L4)ESD protection:
- Differential matching less than 0.01pF
- Pin capacitance 0.9pF
- Flow-through Package (pitch 0.5mm)
- Level shifting
- I_{off}

Benefits

- Single-chip ESD protection for the HDMI Port.
- Internal Level shifting eliminates the need for additional level-shifting IC
- No Layout skew for the differential pair

Applications:

- Digital TV
- Display Terminal
- Monitor
- Video Console



TPD12S520 Board Layout & Circuit Schematics





TPD12S521: HDMI Driver ESD Solution

Released

Key Performance Parameters

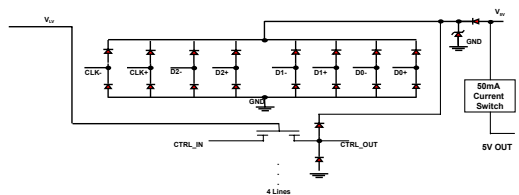
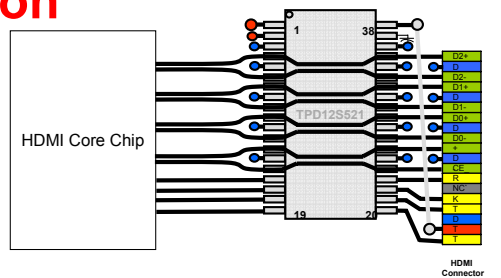
- System level IEC 61000-4-2 (L4) ESD protection:
- Differential matching less than 0.01pF
- Pin capacitance 0.9pF
- Flow-through Package (pitch 0.5mm)
- 50mA current limiting switch
- Level shifting
- I_{off}

Benefits

- Single-chip ESD protection for the HDMI Port.
- Internal Level shifting eliminates the need for additional level-shifting IC
- No Layout skew for the differential pair
- Current switch enables HDMI port detection when the receiver is turned off

Applications:

- Notebook
- Set-top Box
- DVD Player
- Media Player



TPD12S521 Board Layout & Circuit Schematics



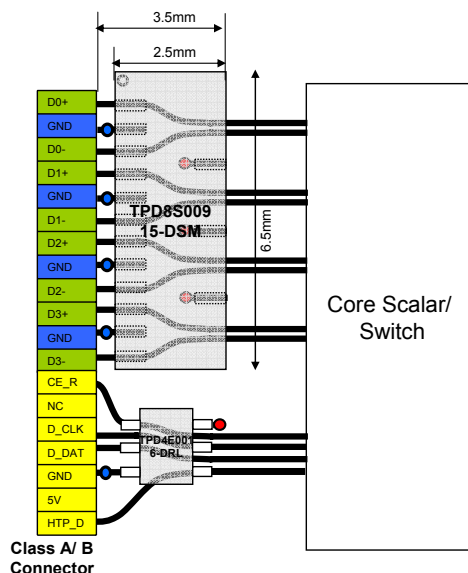


TPD8S009: HDMI/ DisplayPort ESD Solution

Layout Guidelines for High-speed Differential Lines

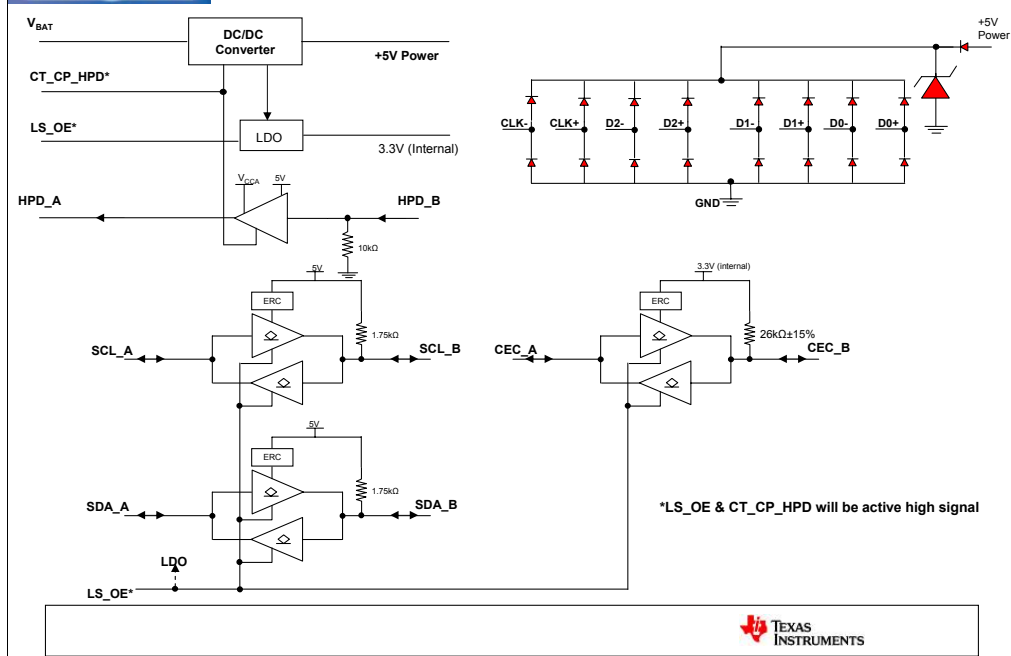
Released

- Recommended trace width 10-mills or higher. It is okay to start with ~103-105 ohm differential impedance target (margin of error on the upper side is preferred). When a narrower trace needs to be selected due to board manufacturing cost or other pre-conditions, it is particularly helpful to start with little over 100-ohms and be still within the 15% trace impedance variations with the ESD capacitance effect.
- Minimum separation needs to be same as the trace width. For example, if the trace width is 10 mills, select the trace separation as 10-mills as well
- It is better practice to couple differential traces together as long as possible (as shown in the right layout figure).
- Use shorter stubs to the vias connected to GND, Power supplies, and by-pass capacitors.





Integration of Active and Passive Components

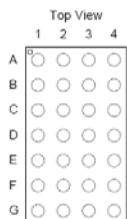




TPD12S015 Pin Mapping in 28-YFF Package

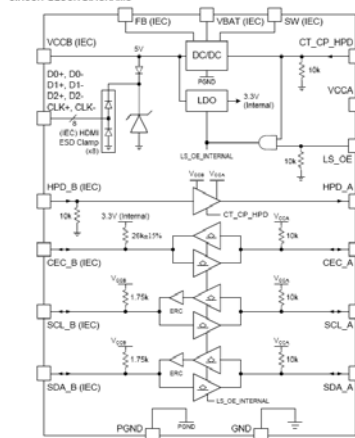
Block Diagram

	1	2	3	4
A	LS_OE	VCCA	D2+	D2-
B	SCL_A	CEC_A	PGND	D1+
C	SDA_A	HPD_A	GND	D1-
D	CT_CP_HPD	GND	CEC_B	D0+
E	FB	GND	SCL_B	D0-
F	VCCB	SW	SDA_B	CLK+
G	PGND	VBAT	HPD_B	CLK-



- WCSP Package Dimensions**
- Ball Count = 28
 - Package Pitch = 0.40mm
 - Package Height = 0.55mm (max)
 - Package Length = 2.8mm (typical)
 - Package Width = 1.6mm (typical)

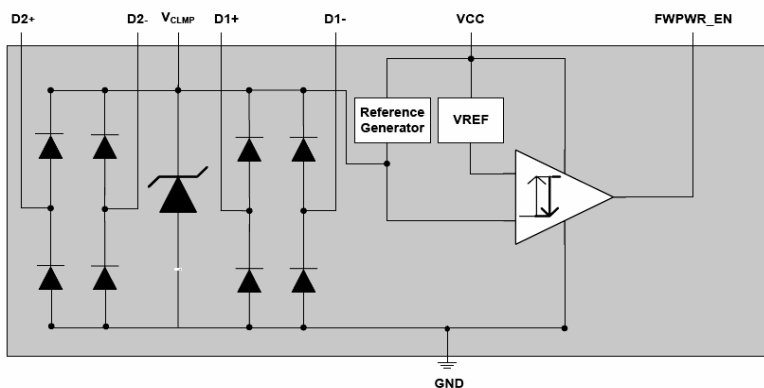
CIRCUIT BLOCK DIAGRAMS





Samples Now

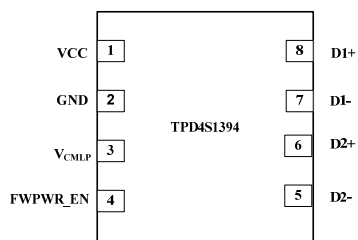
TPD4S1394: Functional Block Diagram



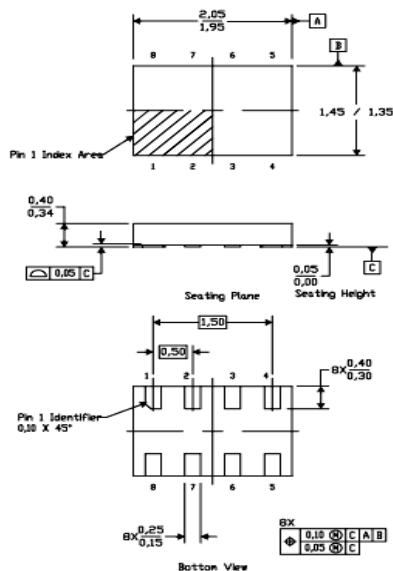
- The TPD4S1394 provides a robust system level ESD solution for the IEEE.1394 port along with a live insertion detection mechanism for high-speed lines interfacing a low-voltage, ESD sensitive core chipset.
- The TPD4S1394 conforms to the IEC61000-4-2 (Level 4) ESD protection and $\pm 15\text{KV}$ HBM ESD protection only for the data lines.(D1 \pm , D2 \pm)



TPD4S1394 Package



- Package option used is a 8-pin DQL package.
- It has a 0.5mm pitch allowing flow through routing.





TPD7S019: Integrated ESD Solution for VGA Port

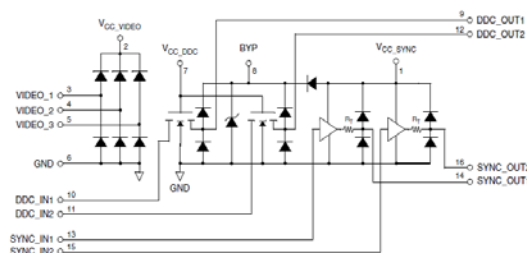
In Work

Key Performance Parameters

- Integrated 7-ch ESD solution with level shifting buffer & back drive protection for DDC signals
- IEC61000-4-2 (Level 4) ESD protection
- Buffer and impedance matching resistors for SYNC signals
- Differential matching less than 0.01pF
- Pin capacitance 0.9pF

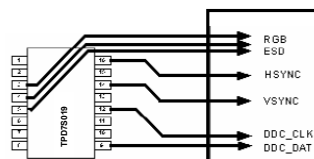
Benefits

- Single-chip ESD protection for the VGA Port.
- Internal Level shifting eliminates the need for additional level-shifting IC
- No Layout skew for the differential pair



Applications:

- PCs
- Notebooks
- Graphics Cards
- Consumer Systems w/ VGA Port & DVI-I ports



TPD7S019 (16-DB Package) Interfacing VGA Port





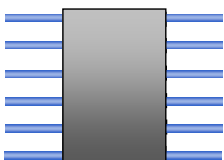
TPD6F002

6-Channel EMI Filter for LCD Display Port

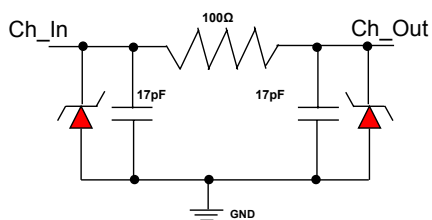
Sample Now

Key Performance Parameters

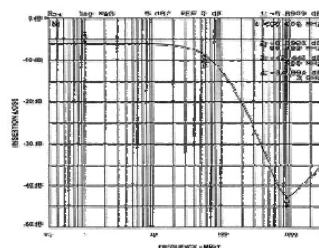
- Six Channel EMI Filtering for Data Ports
- Greater than 32dB attenuation at 1GHz
- -3dB Bandwidth 100MHz
- R-C Topology (R=100Ohm, C=17pF)
- System level ESD protection for high speed application:
 - ✓ $\pm 15\text{kV}$ —Human Body Model
 - ✓ $\pm 8\text{kV}$ —IEC 61000-4-2, Contact Discharge
 - ✓ $\pm 15\text{kV}$ —IEC 61000-4-2, Air-Gap Discharge
- Operating IO Voltage Range up to 5.5V
- Space saving package solutions



3.0-mm × 1.35-mm DSV Package



Schematic Representation



Insertion-loss versus Frequency





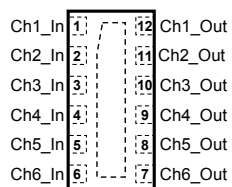
TPD6F003

6-Channel EMI Filter for LCD Display Port

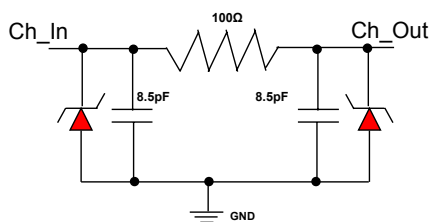
Sample Now

Key Performance Parameters

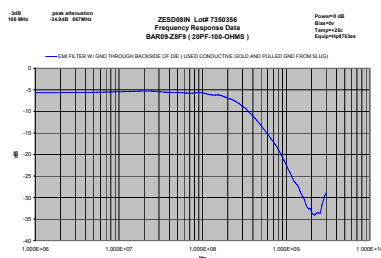
- Six Channel EMI Filtering for Data Ports
- Greater than 32dB attenuation at 1GHz
- -3dB Bandwidth 200MHz
- R-C Topology (R=100Ohm, C=8.5pF)
- System level ESD protection for high speed application:
 - ✓ $\pm 15\text{kV}$ —Human Body Model
 - ✓ $\pm 8\text{kV}$ —IEC 61000-4-2, Contact Discharge
 - ✓ $\pm 15\text{kV}$ —IEC 61000-4-2, Air-Gap Discharge
- Operating IO Voltage Range up to 5.5V
- Space saving package solutions



2.5-mm × 1.35-mm × 0.75mm DQD



Schematic Representation



Insertion-loss VS Frequency



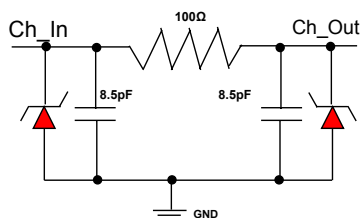


TPD4F003, TPD6F003, TPD8F003

4, 6, & 8-Channel EMI Filter for LCD Display Port

Key Performance Parameters

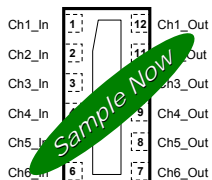
- Six Channel EMI Filtering for Data Ports
- Greater than 32dB attenuation at 1GHz
- -3dB bandwidth 200GHz
- R-C Topology (R=100Ohm, C=8.5pF)
- System level ESD protection for high speed application:
 - ✓ ± 15kV—Human Body Model
 - ✓ ± 8kV—IEC 61000-4-2, Contact Discharge
 - ✓ ± 15kV—IEC 61000-4-2, Air-Gap Discharge
- Operating IO Voltage Range up to 5.5V



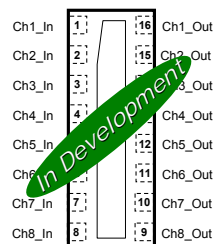
Schematic Representation



1.7-mm × 1.35-mm × 0.75mm SON (0.4-mm Pitch)



2.5-mm × 1.35-mm × 0.75mm SON (0.4-mm Pitch)



3.3-mm × 1.35-mm × 0.75mm SON (0.4-mm Pitch)





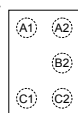
TPD2F702

2-Channel EMI Filter for Audio Headphone

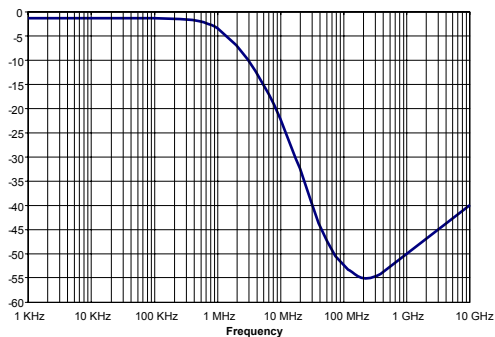
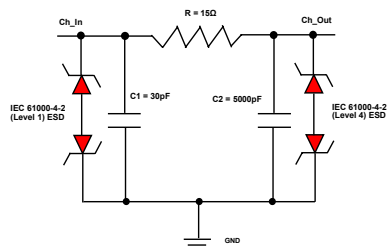
In Work

Key Performance Parameters

- Two Channel EMI Filtering for Audio Ports
- Pi-Style (C-R-C) Filter Configuration (C1 = 30 pF, R = 15 Ω, C = 5000 pF)
- -3dB Bandwidth 3MHz
- ESD Protection Exceeds IEC61000-4-2 (Level 4) on the Connector Side
 - ±8-kV IEC 61000-4-2 Contact Discharge
 - ±15-kV IEC 61000-4-2 Air-Gap Discharge
- Low 10-nA Leakage Current
- Space Saving WCSP Packages and Flow-Through Pin out



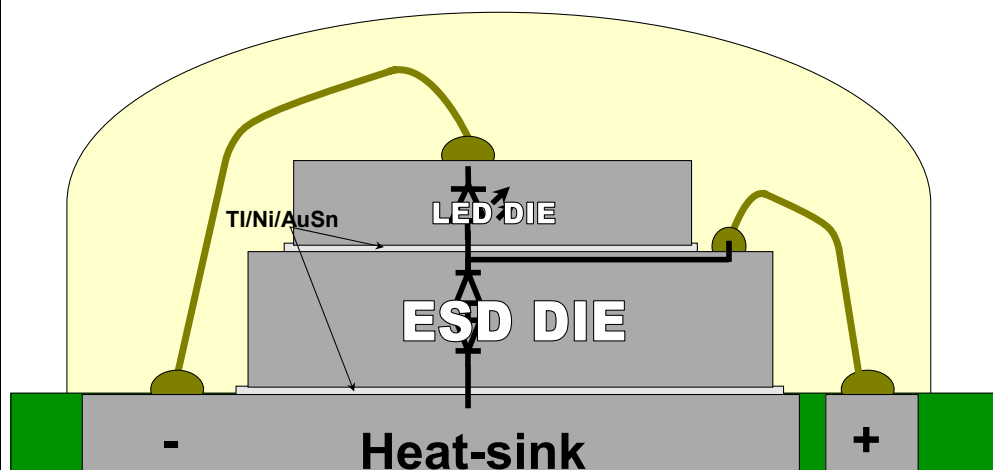
A1	Ch 1 Input, ESD Level 1	A2	Ch 1 Output, ESD Level 4
	Depopulated Ball	B2	Ground
C1	Ch 2 Input, ESD Level 1	C2	Ch 2 Output, ESD Level 4





LED w/ ESD Protection

In Work





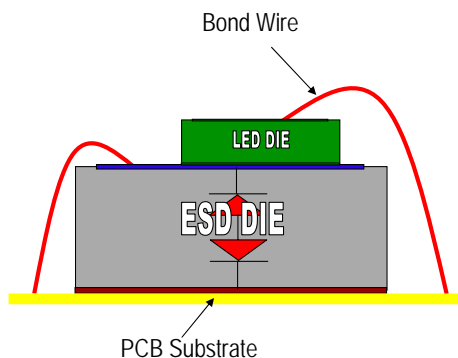
ESD Clamp for LED: TPD1E2510

In Work

Key Performance Parameters

- Bare die ESD solution for ultra space saving applications
- Robust system level ESD protection:
 - ✓ $\pm 20\text{kV}$ —Contact
 - ✓ $\pm 20\text{kV}$ —Air-gap
- Single direction or bidirectional vertical clamp solutions
- Varying breakdown voltage levels to support single or multi-LED products
- Various metallization options to meet most manufacturing requirements

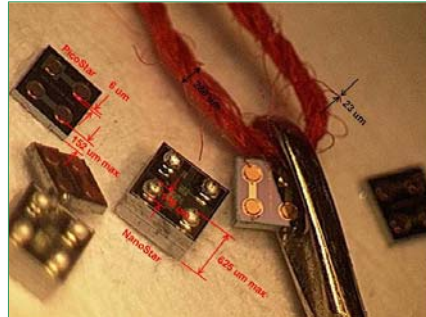
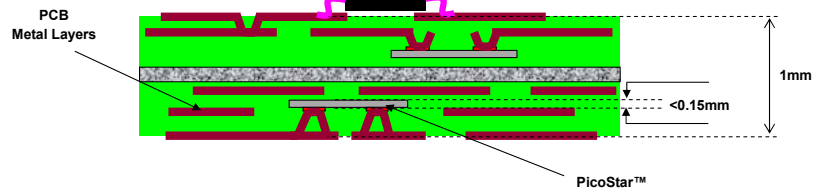
Top PAD Size	1.0mm X 1.0mm
Die Dimensions	1.5mm X 1.1mm X 0.25mm





PicoStar Embedded Package Technology

Board Cross Section



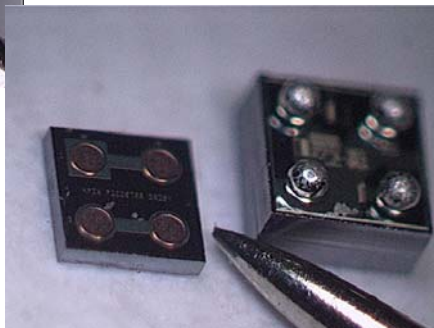
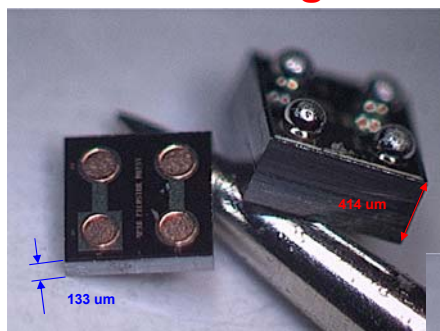


PicoStar (YFM) & WCSP (YZT) Package Comparison

Different concept

(Small as a pin of a needle)

PicoStar (YFM) Comparison
with WCSP (YZT) & provide
thickness





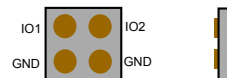
TPD2E007YFM

2-Channel ESD in PicoStar Package

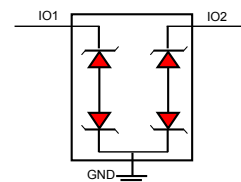
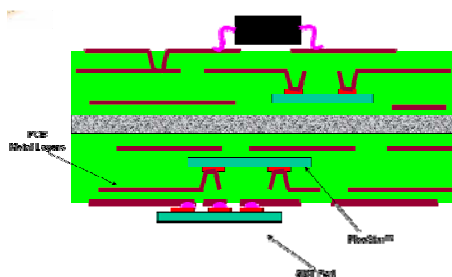
Released

Key Performance Parameters

- System level ESD protection for high speed application:
 - $\pm 8\text{kV}$ —IEC 61000-4-2, Contact Discharge
 - $\pm 15\text{kV}$ —IEC 61000-4-2, Air-Gap Discharge
- Breakdown voltage $> \pm 14\text{V}$ (@ $I_l=1\text{mA}$)
- Pin capacitance $< 15\text{pF}$ (Measured @ $V_l=2.5\text{V}$)
- **Package height less than 0.15 mm**



Length = 0.8 mm
Width = 0.8 mm
Height $< 0.15\text{ mm}$
Pitch = 0.4 mm



PicoStar Package & Circuit Diagram





Thank You!