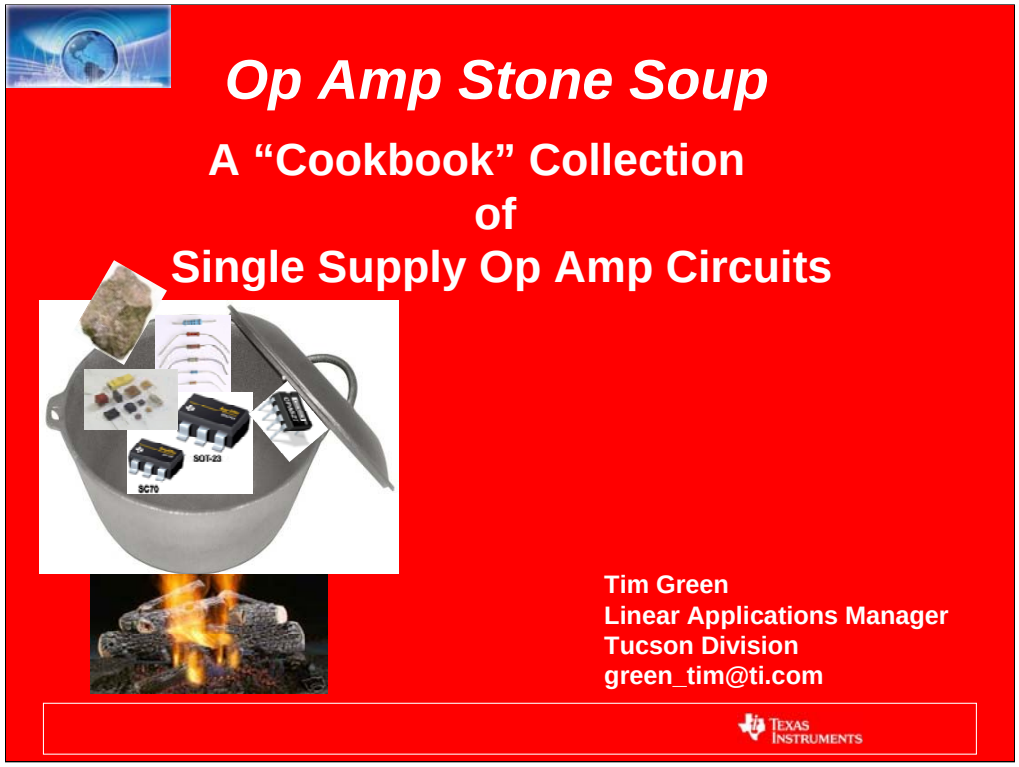

Op Amp Stone Soup:

This presentation will offer a "Stone Soup" collection of useful op amp circuits to solve linear application problems on a daily basis. Each op amp circuit (pre-built in the included TINA SPICE schematic) is presented as a definition-by-example with a brief overview of its functionality, applicable transfer function and/or waveforms and key equations for re-scaling the function to your exact application. A sampling of the ingredients include the following circuits: Voltage-to-Current Conversion, Drive Circuits (Bridge-Tied-Load, Parallel Op Amps, High Current Cascade Reference Buffer), Translation Circuits (Single-Ended to Differential, Differential to Single-Ended, Differential In to Differential Out), Conditioning Circuits (Full-Wave Rectifier, Supply Splitter, Integrator Amp in Feedback, Isolation Amplifier, G=1/G=-1 amp), and Comparator Circuits (AC Coupled, Comparator with Hysteresis).

These are built specifically for single-supply applications which require special considerations often not needed when dual supply op amps are available. Any engineer interfacing with customers will find these op amp building blocks invaluable and ready to run on TINA SPICE right out of the pot.

The Story of Stone Soup

Some travelers come to a village, carrying nothing more than an empty pot. Upon their arrival, the villagers are unwilling to share any of their food stores with the hungry travelers. The travelers fill the pot with water, drop a large stone in it, and place it over a fire in the village square. One of the villagers becomes curious and asks what they are doing. The travelers answer that they are making "stone soup", which tastes wonderful, although it still needs a little bit of garnish to improve the flavor, which they are missing. The villager doesn't mind parting with just a little bit to help them out, so it gets added to the soup. Another villager walks by, inquiring about the pot, and the travelers again mention their stone soup which hasn't reached its full potential yet. The villager hands them a little bit of seasoning to help them out. More and more villagers walk by, each adding another ingredient. Finally, a delicious and nourishing pot of soup is enjoyed by all.

"Stone Soup" is a Grimm Brothers fable. Source: Wikipedia
http://en.wikipedia.org/wiki/Stone_soup

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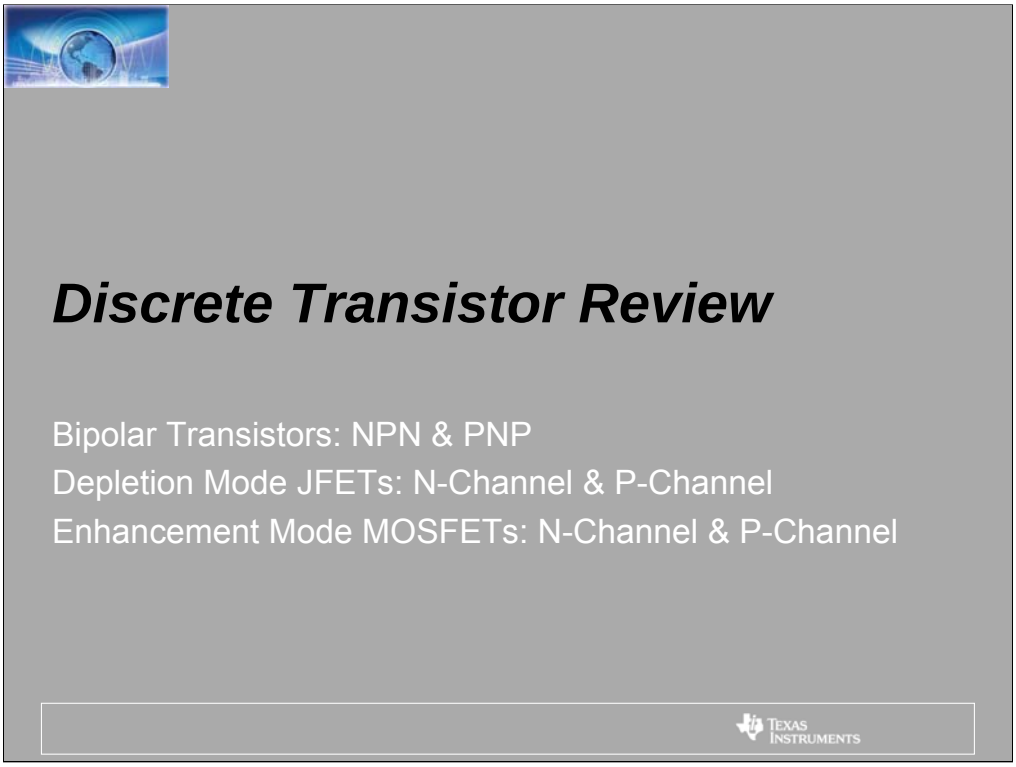
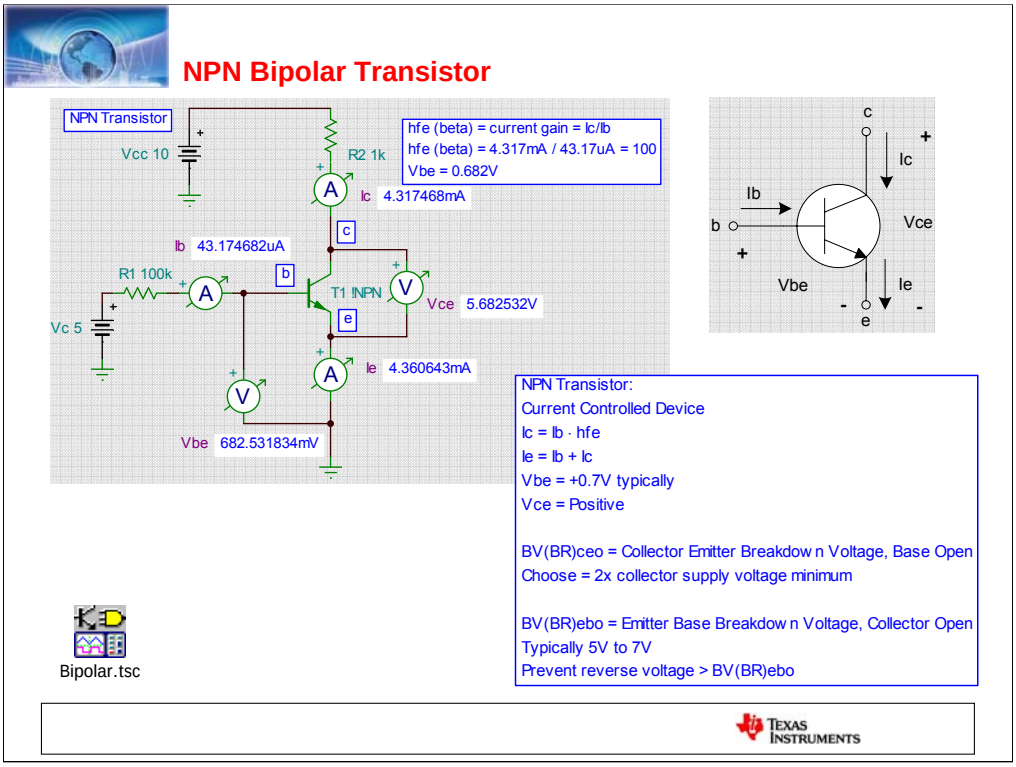
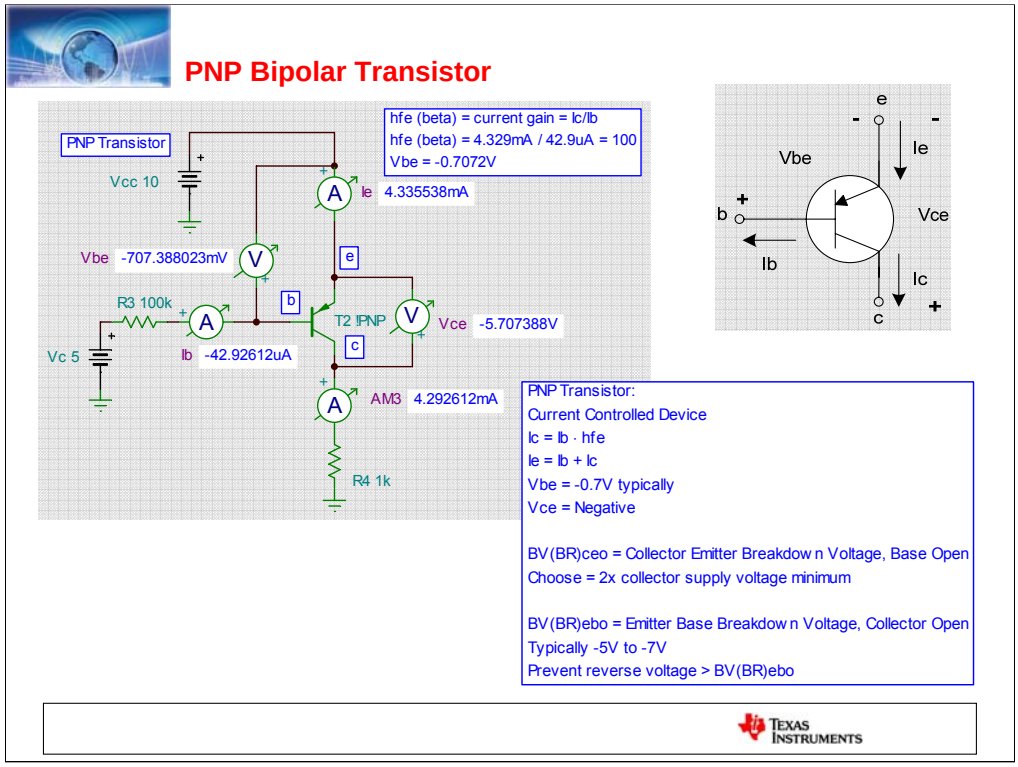
Much like the fable of "Stone Soup" this presentation started as an "empty pot" with many curious villagers (Linear Applications Engineers) eager to through in a special ingredient of their own. Hope you enjoy the resulting pot full of op amp circuits.



Before we look at our single supply circuits we will do a brief overview of common discrete transistors that are often required to help in single supply op amp applications.

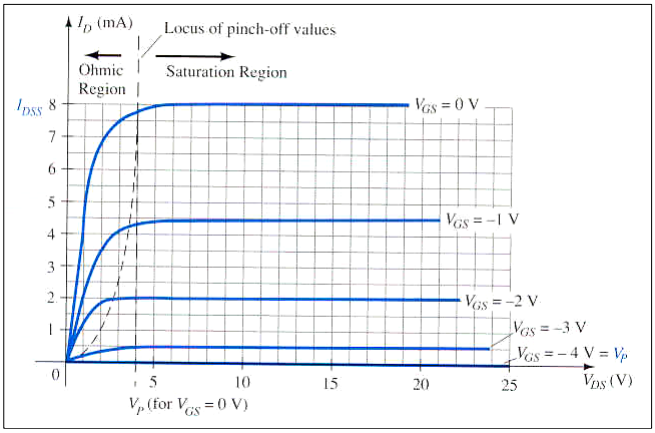


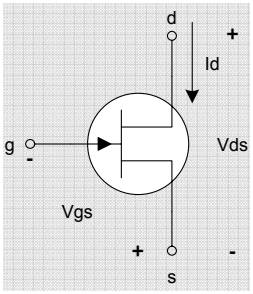
The NPN Bipolar Transistor is a current controlled device. It requires a base-emitter forward voltage drop to begin to conduct current through the base-emitter junction which will then be gained up to the collector. Emitter current is a summation of collector current plus base current. For proper operation the NPN transistor must have a positive base emitter voltage and a positive collector-emitter voltage as current flows from collector through emitter.



The PNP Bipolar Transistor is a current controlled device. It requires a base-emitter forward voltage drop to begin to conduct current through the base-emitter junction which will then be gained up to the collector. Emitter current is a summation of collector current plus base current. For proper operation the PNP transistor must have a negative base emitter voltage and a negative collector-emitter voltage as current flows from emitter through collector.

N-Channel Depletion Mode JFET





Ohmic Region = Triode Region
Saturation Region = Pinch-off Region

N_jfet.tsc

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N-Channel Depletion Mode JFETs are fully turned on with Vgs = 0V and it takes a negative Vgs to turn the device off. They are voltage controlled devices with no gate current flow when they are properly biased. For normal operation the gate-source junction and gate-drain junction must both be reversed biased. In the triode region the JFET can be used as a voltage-controlled resistor.

N-Channel Depletion Mode JFET: Vgs = 0V

N-Channel Depletion Mode JFET
Voltage Controlled Device

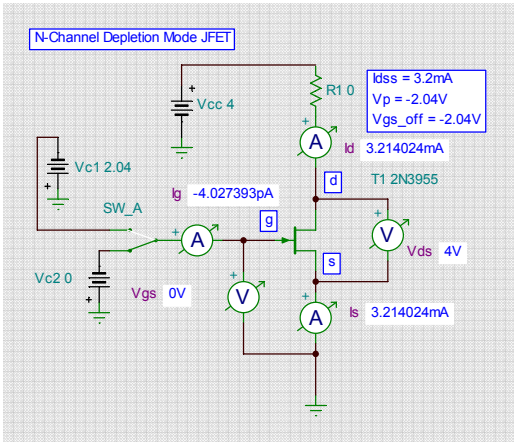
Vgs_off = Negative Voltage
Vgs_on = 0V
Idss = Drain Saturation Current

Vgd must be negative to keep reverse biased

Id is proportional to Vgs and Vds
Id = Is (Current flow from Id to Is)
Ig = 0A

Vp = Negative for N-Channel JFET
Vp = Pinch-off Voltage which determines either:
Triode Region (ohmic): Vp < Vgs < 0V, Vds < Vgs-Vp
Saturation (pinch-off) Region: Vp < Vgs < 0V, Vds > Vgs - Vp

Vgd = Gate to Drain Breakdown Voltage
Vgs(r) Reverse Gate to Source Breakdown Voltage
Usually Vgd = Vgs(r)
Choose = 2x max voltage minimum of:
Maximum of Drain Voltage or Gate Voltage



N-Channel Depletion Mode JFET: Vgs = -2.04V

N-Channel Depletion Mode JFET
Voltage Controlled Device

Vgs_off = Negative Voltage
Vgs_on = 0V
Idss = Drain Saturation Current

Vgd must be negative to keep reverse biased

Id is proportional to Vgs and Vds
Id = Is (Current flow from Id to Is)
Ig = 0A

Vp = Negative for N-Channel JFET
Vp = Pinch-off Voltage which determines either:
Triode Region (ohmic): Vp < Vgs < 0V, Vds < Vgs-Vp
Saturation (pinch-off) Region: Vp < Vgs < 0V, Vds > Vgs - Vp

Vgd = Gate to Drain Breakdown Voltage
Vgs(r) Reverse Gate to Source Breakdown Voltage
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Choose = 2x max voltage minimum of:
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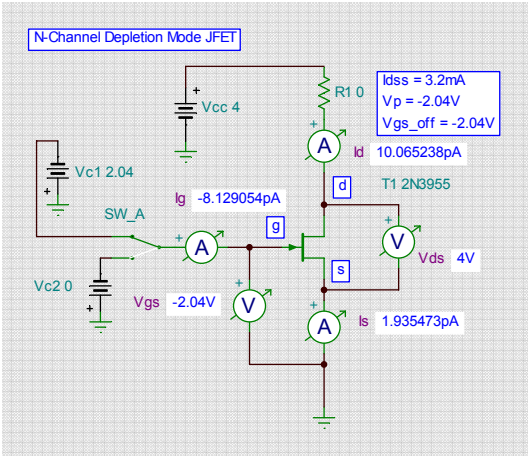
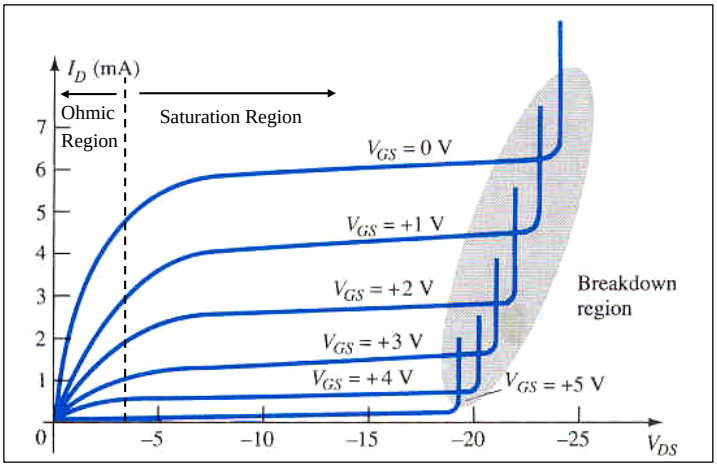
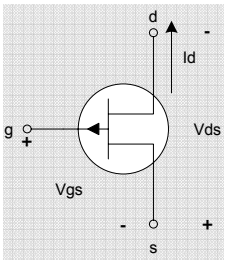


P-Channel Depletion Mode JFET





Ohmic Region = Triode Region
Saturation Region = Pinch-off Region

P_jfet.tsc

Texas Instruments

P-Channel Depletion Mode JFETs are fully turned on with Vgs = 0V and it takes a positive Vgs to turn the device off. They are voltage controlled devices with no gate current flow when they are properly biased. For normal operation the gate-source junction and gate-drain junction must both be reversed biased. In the triode region the JFET can be used as a voltage-controlled resistor.

P-Channel Depletion Mode JFET: Vgs = 0V

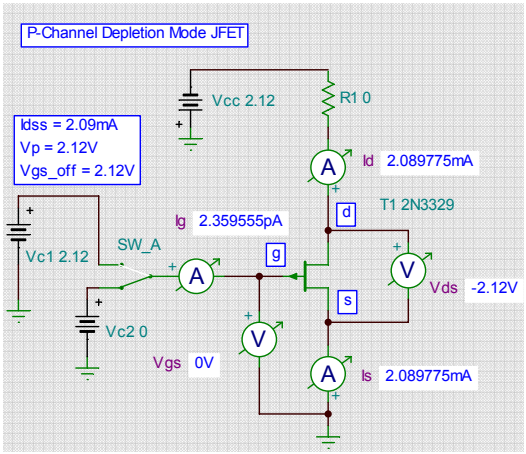
P-Channel Depletion Mode JFET
Voltage Controlled Device

Vgs_off = Positive Voltage
Vgs_on = 0V
Idss = Drain Saturation Current

Id is proportional to Vgs and Vds
Id = Is (Current flow from Is to Id)
Ig = 0A

Vp = Positive for P-Channel JFET
Vp = Pinch-off Voltage which determines either:
Triode Region (ohmic): 0V < Vgs < Vp, Vds > Vgs-Vp
Saturation (pinch-off) Region: 0V < Vgs < Vp, Vds < Vgs - Vp

Vgd = Gate to Drain Breakdown Voltage
Vgs(r) Reverse Gate to Source Breakdown Voltage
Usually Vgd = Vgs(r)
Choose = 2x max voltage minimum of:
Maximum of Drain Voltage or Gate Voltage



P-Channel Depletion Mode JFET: Vgs = 2.12V

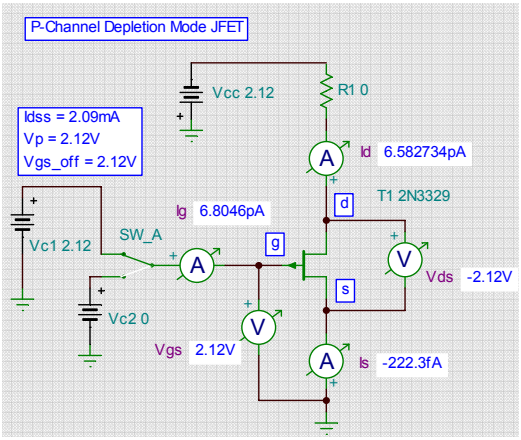
P-Channel Depletion Mode JFET
Voltage Controlled Device

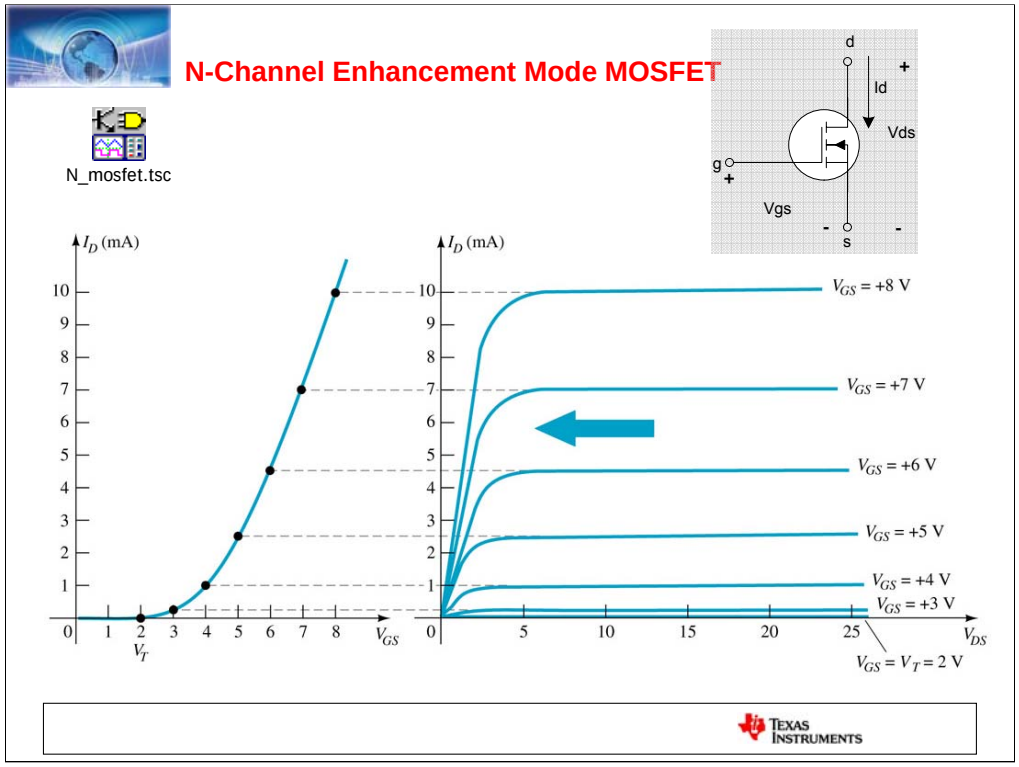
Vgs_off = Positive Voltage
Vgs_on = 0V
Idss = Drain Saturation Current

Id is proportional to Vgs and Vds
Id = Is (Current flow from Is to Id)
Ig = 0A

Vp = Positive for P-Channel JFET
Vp = Pinch-off Voltage which determines either:
Triode Region (ohmic): 0V < Vgs < Vp, Vds > Vgs-Vp
Saturation (pinch-off) Region: 0V < Vgs < Vp, Vds < Vgs - Vp

Vgd = Gate to Drain Breakdown Voltage
Vgs(r) Reverse Gate to Source Breakdown Voltage
Usually Vgd = Vgs(r)
Choose = 2x max voltage minimum of:
Maximum of Drain Voltage or Gate Voltage





N-Channel Enhancement Mode MOSFETs are voltage controlled devices with a positive Vgs turning them on and Vgs = 0 turning them off. The gate-source junction must NOT be subjected to over-voltage or permanent damage can occur. In the triode region the MOSFET can be used as a voltage-controlled resistor similar to the Depletion Mode JFET with the advantage that current does not flow if gate-source or drain-gate junctions are reverse biased.

N-Channel Enhancement Mode MOSFET: Vgs = 0V

N-Channel Enhancement Mode MOSFET
Voltage Controlled Device

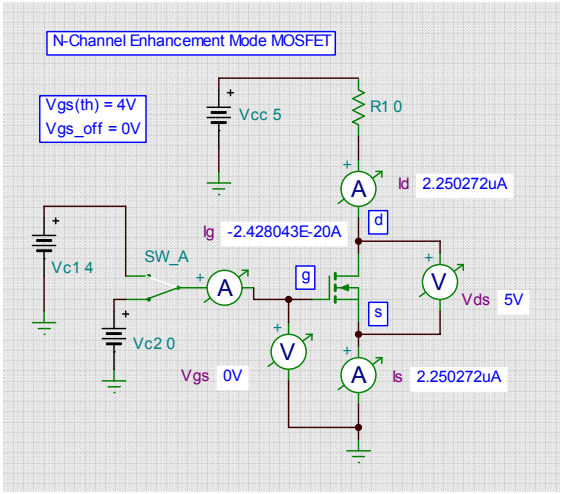
Vgs_off = 0V
Vgs_on = Positive Voltage
Vgs(th) = start of MOSFET turn-on
Idss = Drain Saturation Current
Idss = max current flow for fixed Vgs with varying Vds

Id is proportional to Vgs and Vds
Id = Is (Current flow from Is to Id)
Ig = 0A

Vds(max) = Maximum drain to source voltage
Choose Vds(max) =2x supply voltage

Vgs(max) = maximum gate to source voltage
Do not exceeed Vgs(max) or device is destroyed

Id(max) = maximum drain current
Choose Id(max) =2x maximum load current



N-Channel Enhancement Mode MOSFET: Vgs = 4V

N-Channel Enhancement Mode MOSFET
Voltage Controlled Device

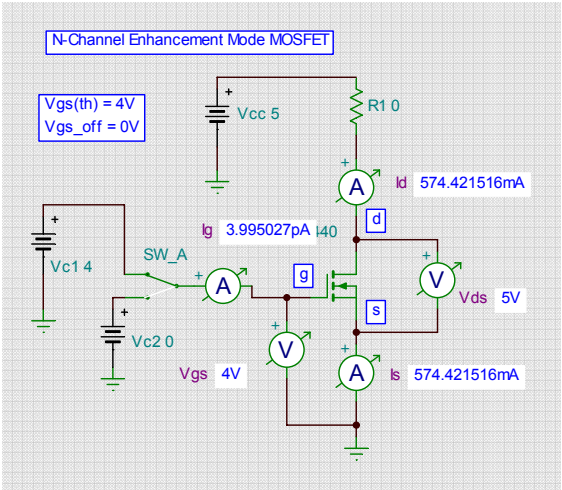
Vgs_off = 0V
Vgs_on = Positive Voltage
Vgs(th) = start of MOSFET turn-on
Idss = Drain Saturation Current
Idss = max current flow for fixed Vgs with varying Vds

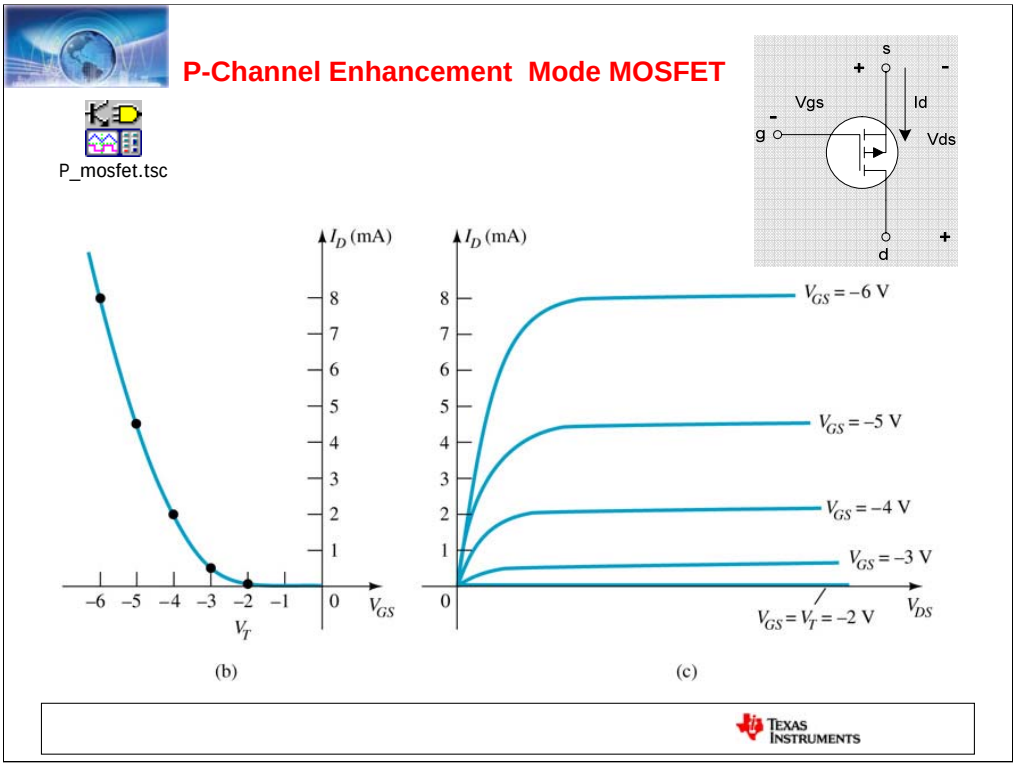
Id is proportional to Vgs and Vds
Id = Is (Current flow from Is to Id)
Ig = 0A

Vds(max) = Maximum drain to source voltage
Choose Vds(max) =2x supply voltage

Vgs(max) = maximum gate to source voltage
Do not exceeed Vgs(max) or device is destroyed

Id(max) = maximum drain current
Choose Id(max) =2x maximum load current





P-Channel Enhancement Mode MOSFETs are voltage controlled devices with a negative Vgs turning them on and Vgs = 0 turning them off. The gate-source junction must NOT be subjected to over-voltage or permanent damage can occur. In the triode region the MOSFET can be used as a voltage-controlled resistor similar to the Depletion Mode JFET with the advantage that current does not flow if gate-source or drain-gate junctions are reverse biased.

P-Channel Enhancement Mode MOSFET: Vgs = 0V

P-Channel Enhancement Mode MOSFET
Voltage Controlled Device

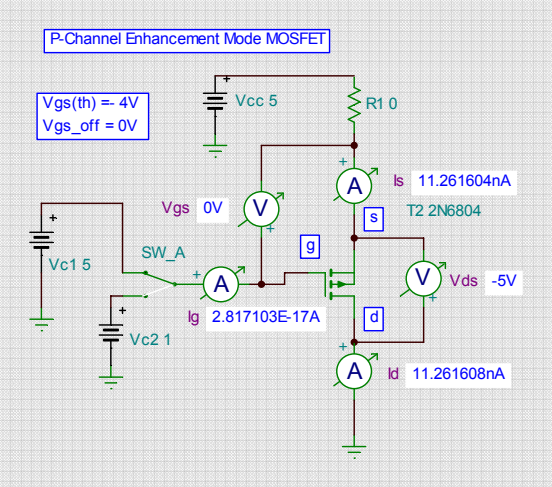
Vgs_off = 0V
Vgs_on = Negative Voltage
Vgs(th) = start of MOSFET turn-on
Idss = Drain Saturation Current
Idss = max current flow for fixed Vgs with varying Vds

Id is proportional to Vgs and Vds
Id = Is (Current flow from Is to Id)
Ig = 0A

Vds(max) = Maximum drain to source voltage
Choose Vds(max) =2x supply voltage

Vgs(max) = maximum gate to source voltage
Do not exceeed Vgs(max) or device is destroyed

Id(max) = maximum drain current
Choose Id(max) =2x maximum load current



P-Channel Enhancement Mode MOSFET: Vgs = -4V

P-Channel Enhancement Mode MOSFET
Voltage Controlled Device

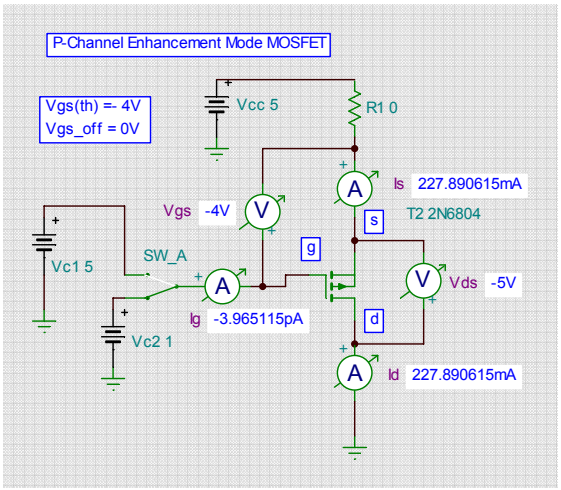
Vgs_off = 0V
Vgs_on = Negative Voltage
Vgs(th) = start of MOSFET turn-on
Idss = Drain Saturation Current
Idss = max current flow for fixed Vgs with varying Vds

Id is proportional to Vgs and Vds
Id = Is (Current flow from Is to Id)
Ig = 0A

Vds(max) = Maximum drain to source voltage
Choose Vds(max) =2x supply voltage

Vgs(max) = maximum gate to source voltage
Do not exceeed Vgs(max) or device is destroyed

Id(max) = maximum drain current
Choose Id(max) =2x maximum load current



Voltage-to-Current Circuits
Drive Circuits
Translation Circuits
Conditioning Circuits
Comparator Circuits

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Voltage-to-Current Circuits

V-I High Side Referenced

V-I Low Side Referenced

V-I Improved Howland Current Pump

V-I High Side Referenced

Design Goal:

Vcc =+5V

Vin = 0V to 1V → Iout = 0 to 100mA

Rload = 40 ohms, Grounded Load

1% FSR accuracy in transfer function (Iout/Vin)

Given:

PPSL (Preferred Parts Selection List) Parts:

Overkill but we can work with them!

MOSFETs:

N-Channel Enhancement Mode MOSFET:
IRFP440
Vgs(th) = 4Vmax
rds(on) = 0.8 ohms
BVdss = 500V
Id(on) = 8.8A

P-Channel Enhancement Mode MOSFET:
IRFU9120
Vgs(th) =- 4V
rds(on) = 0.6 ohms
BVdss = -100V
Id(on) = 5.8A

Design Considerations:

Need to Sense current in High Side

Need to level shift Vin to control High Side Current

Need a Power Device & RRIO op amp for sense and control

Design Preliminary Analysis:

Use N-Channel MOSFET for Level Shifting

Use P-Channel MOSFET for High Side Current Control

Vheadroom = Vcc – [Iout(max) * Rload]

1V = 5V – [100mA * 40 ohms]

Vheadroom is all that is left for MOSFET Vds drop + High Side Current Sense Resistor Drop

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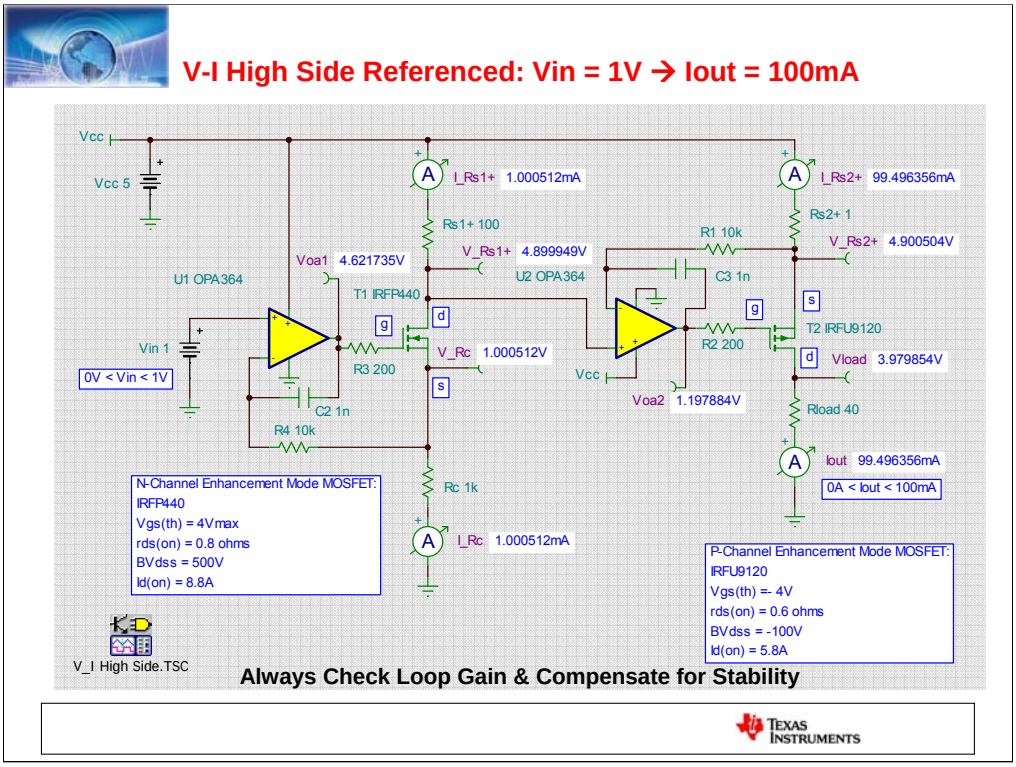
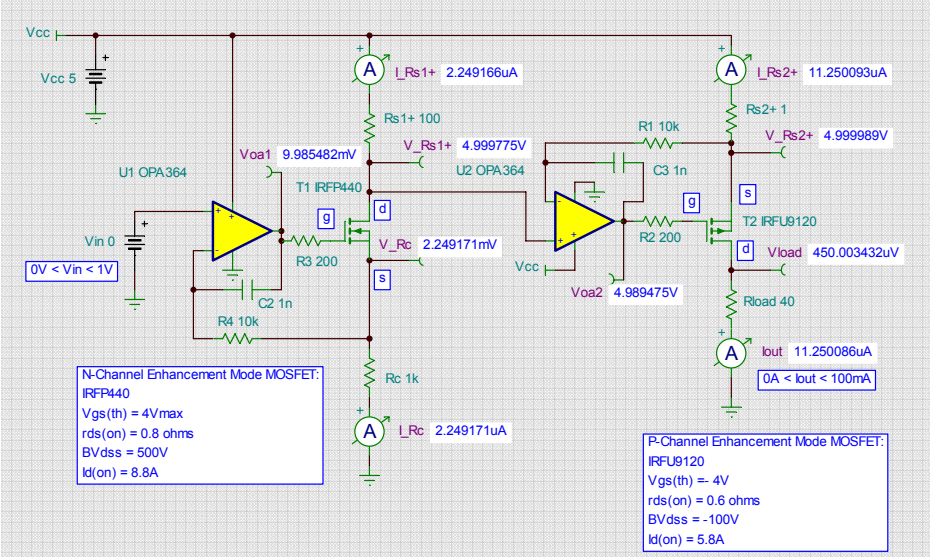


The V-I High Side Referenced circuit is intended to receive a ground referenced command voltage and control current in the high side of the output to drive a grounded load. To level shift he ground referenced Vin up to the positive supply, Vcc, an N-Channel Enhancement Mode MOSFET is used along with U1, a single supply RRIO op amp, OPA364. Vin is impressed across Rc due to the open loop gain of the op amp and feedback across Rc. This wil cause a current I_Rc to flow. Since there is no error gate current the drain current of T1, I_Rs will be the same as I_Rc. I_Rs times Rs1+ will create a voltage drop referenced to Vcc. The output power stage consists of U2, OPA364, and a P-Channel Enhancement Mode MOSFET. The input voltage to U2 is referenced to Vcc as is the feedback across Rs2+ and the op amp loop gain will move the output of U2 to control the gate of T2 until the op amp inputs equal each other. The overall scaling for full-scale is 1V in across Rc creates I_Rc = 1mA. I_Rc = I_Rs+ = 1mA times RS1+ of 100 ohms yields a 100mV drop from Vcc at U2, +input. 100mV at U2, -input means Iout must be equal to 100mV/RS2+ or 100mV/1 = 100mA. Key design considerations are adequate voltage control on single supply for the Vgs of the MOSFETs used. Lower cost, lower MOSFETs can be found that will do equally as well as those used here for demonstration of this often-used design concept. For the level shifting of Vin to be referenced to Vcc a JFET can be used but care must be take to ensure the gate-source and gate-drain junctions do no become forward biased or undesired voltages may occur in the translation circuitry.

V-I High Side Referenced: Vin = 0V → Iout = 0A



Always Check Loop Gain & Compensate for Stability

V-I High Side Referenced: Design Details

Design Details:
1) Rs2+ Selection
Choose Rs2+ to drop 100mV at Iout=100mV
Rs2+ = 100mV/100mA = 1ohm
Small headroom but enough reasonable signal

2) Level Shift:
V_Rc = Vin
I_RC = Vin/Rc
I_Rc = IRs1+ (Use MOSFET-> small error current)
V_Rs1+ = Vcc - (I_Rs1+ · Rs1+)

V_Rs1+ = 100mV for Vin =1V. Choose IRs1+ = 1mA at Vin =1V
Rs1+ = 100mV/1mA = 100ohm
Rc = 1V/1mA = 1kohm

Ensure T1 can provide Vgs(on) with Vcc - V_Rc(max)
Vgs(on) = 5V -1V = 4V -> Okay
Use U1 = RRIO Op Amp

3) Output Current Control
Use P-Channel MOSFET since:
Turn off Voa2 goes to Vcc
Turn on Voa2 can go Gnd -> 5V = Vgs

Feedback around U2 is realtive to Vcc across Rs2+
Use U2 = RRIO Op Amp
Auto-zero will improve accurcay due to Vos on U2

4) Stability considerations on U1 and U2
Both U1 and U2 need to be analyzed for stability and compensated

5) %FSR Accuracy
%FSR Accuray = {[Iout(fs) Ideal - Iout(fs) actual] / [Iout(fs) Ideal]} · 100
%FSR Accuracy = {[100mA - 99.496356ma] / [100mA]} · 100 = 0.5036%

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V-I Low Side Referenced

Given:

PPSL (Preferred Parts Selection List) Parts:

NPN Power Transistor:

NPN Power Transistor:
TIP33
V(br)ceo = 40V
Ic(continuous) = 10A
hfe @ Ic=0.5A = 100
Vbe @ Ic=0.5A = 0.65V
Pd = 80W @ Tc=25C
Roja = 35.7C/W
Tj max = 150C

Design Goal:

Vcc =+12V

Vin = 0V to 4.096V → Iout = 0 to 500mA

Rload = 20 ohms, Floating Load

0.5% FSR accuracy in transfer function (Iout/Vin)

Design Considerations:

Need to Sense current in Low Side

Need to drive high current -> External Transistor

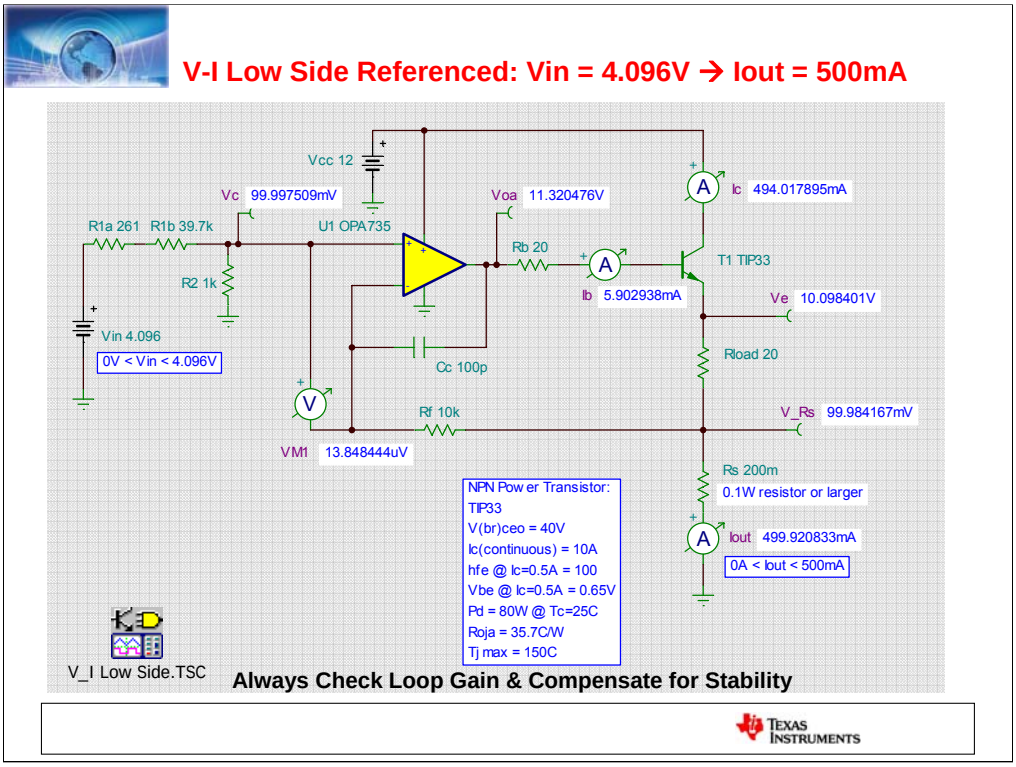
Need RRO Op Amp, Input CM to Ground

Design Preliminary Analysis:

If there is voltage headroom then:

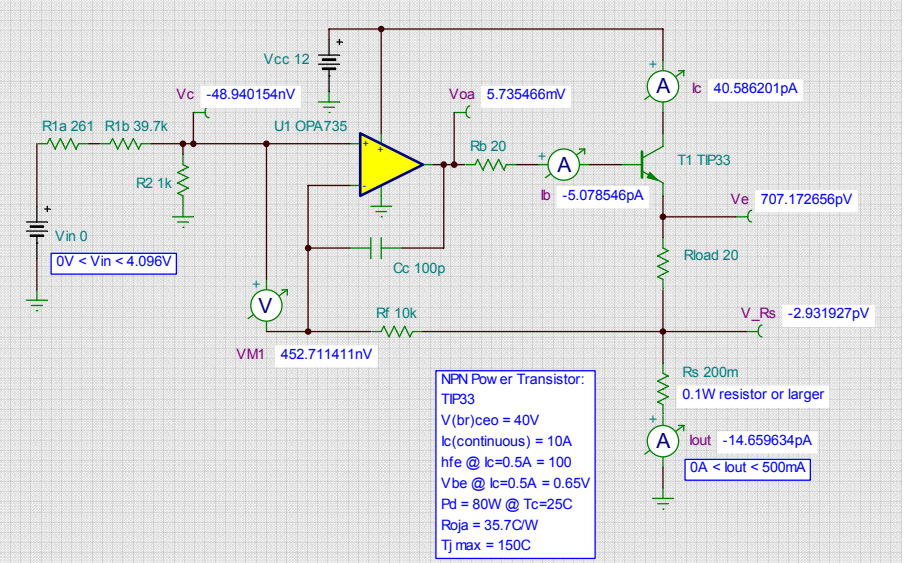
Use Bipolar Emitter-Follower after op amp for simplest design

Low drop across sense resistor -> maximize headroom & minimize power dissipation



This V_I Low Side Referenced circuit simplifies boosting output current in applications where there is adequate voltage headroom to use a familiar emitter-follower current boost stage after a small signal op amp. In this arrangement accurate current control is kept through the floating load as both base current and collector current become emitter current and flow into the load and into the load current sense resistor, Rs. The top of Rs is fed back into the –input of U1. Since this is a non-inverting circuit we must pay attention that we do not have any common mode violations on U1. The OPA735 has common mode input to ground and Vcc-1.5V. For this arrangement and operation we are safe. The only errors in this are resistor tolerances on the Vc divider, tolerance on Rs, and the Vos of U1.

V-I Low Side Referenced: Vin = 0V → Iout = 0A



Always Check Loop Gain & Compensate for Stability

V-I Low Side Referenced: Design Details

Design Details:
1) Select Rs
V_Rs = 100mV at Iout = 0.5A
Help with headroom, minimze power dissipation in Rs, still good signal at full scale.
V_Rs = 100mV/0.5A = 200mohm

2) Scale Vin full scale
Vc = 100mV for Vin = 4.096V
Load Vin with 0.1mA at full scale
R2 = Vc/0.1mA = 100mV/0.1mA = 1kohm
R1 = R1a + R1b
0.1mA = Vin / (R1 + R2)
0.1mA = 4.096 / (R1 + 1k) -> R1 = 39.960kohm
Use standard values:
R1a = 261 ohms
R1b = 39.7kohms

3) Check Iout Current Contorl at Max Iout
V_Rs = Iout(max) · Rs = 500mA · 200mohm = 100mV
Ve = V_Rs + Iout · Rload = 100mV + 500mA· 20ohms = 10.1V
Assume TIP33 Vbe = 0.65V
Assume TIP33 hfe = 100 -> Ib = 500mA/100 = 5mA
Choose Rb to add 100mV or so to headroom, Rb helps limit transient current into TI33 base
Rb also helps isolate transistor parasitic capacitances at high frequency from op amp output
Vdrop across Rb = 20ohms · 5mA = 0.1V
Voa = Ve + Vbe + V_Rb = 10.1V + 0.65V + 0.1V = 10.85V
OPA734 at 5mA out looks like about 0.5V swing to rail so we have 0.65V margin for supply to dip or worst case Vbe to occur, or degradation in hfe requiring more Ib thorugh Rb.

4) %FSR Accuracy
%FSR Accuray = {[Iout(fs) Ideal - Iout(fs) actual] / [Iout(fs) Ideal]} · 100
%FSR Accuracy = {[500mA - 499.920833ma] / [500mA]} · 100 = 0.0158%
This design leaves plenty of margin for resistor tolerances.
The auto-zero accuracy of OPA734 and the simplicity of the design minimizes errors here.

Texas Instruments

V-I Improved Howland Current Pump

Design Goal:

Vcc =+5V

Vin = 0V to 500mV → Iout = 0 to 500mA

Rload = 8 ohms, Grounded Load

1% FSR accuracy in transfer function (Iout/Vin)

Given:

PPSL (Preferred Parts Selection List) Parts:

OPA569 Power Op Amp

OPA569 Power Op Amp:
2.7V to 5.5V supply
Input voltage range includes Vcc & Gnd
2A Output Current Capability
+/-300mV swing from rail at +/-2A out
Input Offset Voltage = +/-2mV max

Design Considerations:

Need to Sense current in High Side

Need to drive high current -> Power Op Amp?

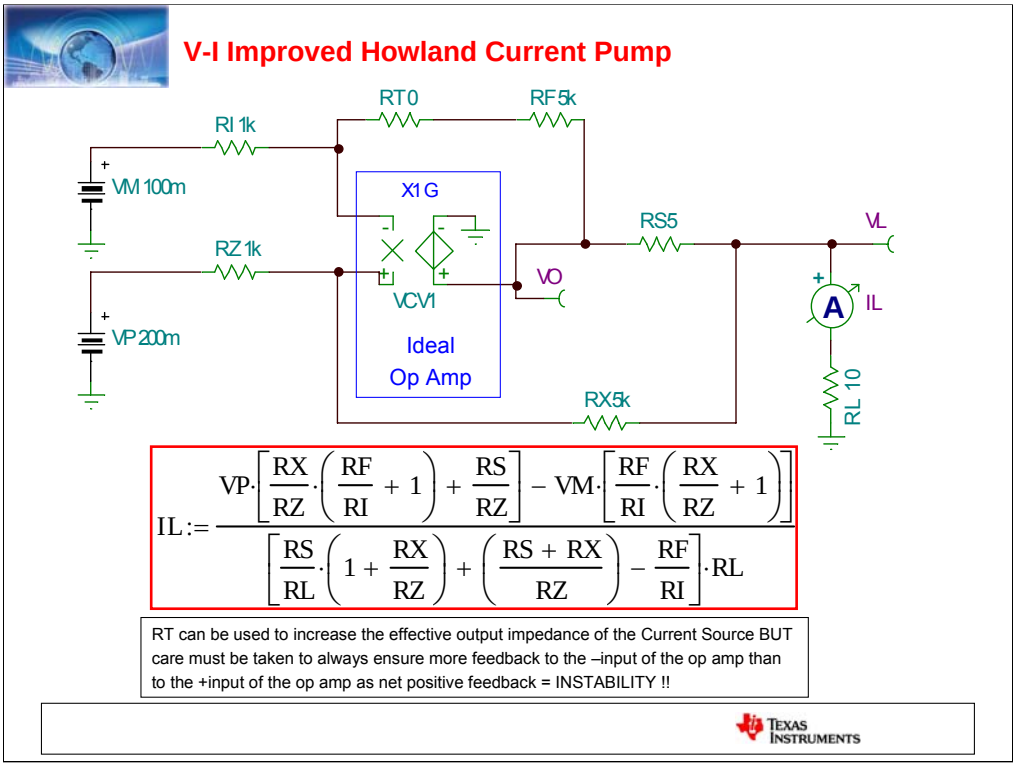
Need RRO Op Amp, Input CM to Ground

Design Preliminary Analysis:

If there is voltage headroom then:

Power Op Amp offers single IC solution

Low drop across sense resistor -> maximize headroom & minimize power dissipation



The Improved Howland Current Pump uses two feedback paths to form a net differential feedback path across a high-side current sense resistor capable of driving a grounded load. In single supply applications this works well for creating bipolar current flow in a load by using the Improved Howland Current Pump in a BTL (Bridge Tied Load).

V-I Improved Howland Current Pump

Set RX=RF and RZ=RI and move all tolerances to worst case for accuracy analysis

RT	RF	RX	RI	RZ	RS	RL	*IL*	*VL*	*VO*	AM1 Sensitivity (%)	Comments
2.858407	**5000**	**5000**	**1000**	**1000**	**5**	**10**	**0.100000052**	**1.000000100**	**1.500667000**	**0.000000000**	Rt adjusted for Ideal IL
0	5000	5000	1000	1000	5	10	0.099866893	0.998668931	1.498669000	0.133158931	Rt=0, Nominal Values
2.858407	***5050***	5000	1000	1000	5	10	0.102371216	1.023712000	1.536255000	-2.371162767	1% Resistor Changes
2.858407	5000	***5050***	1000	1000	5	10	0.098700599	0.987005991	1.481159000	1.299452324	1% Resistor Changes
2.858407	5000	5000	***1010***	1000	5	10	0.097727653	0.977276527	1.466563000	2.272397818	1% Resistor Changes
2.858407	5000	5000	1000	***1010***	5	10	0.101353602	1.013536000	1.520981000	-1.353549296	1% Resistor Changes
2.858407	5000	5000	1000	1000	***5.05***	10	0.099009365	0.990094651	1.490756000	0.990686485	1% Resistor Changes
2.858407	5000	5000	1000	1000	5	***10.1***	0.099999329	1.009993000	1.510665000	0.000723	1% Resistor Changes
0	***5050***	***4950***	***990***	***1010***	***4.95***	***10***	***0.108995522***	***1.089955000***	***1.630222000***	*-8.995465322*	***1% Worst Case w/RT=0)***
2.858407	***5050***	***4950***	***990***	***1010***	***4.95***	***10***	***0.109152449***	***1.091524000***	***1.632570000***	*-9.152392241*	***1% Worst Case w/RT=Nom)***

1% Resistors (w/RT=0) could yield 9% Accuracy at T=25°C

0.1% Resistors (w/RT=0) could yield 0.9% Accuracy at T=25°C

Still useful for V-I control in Motors, Valves, TECs, LEDs, etc

Other system feedback re-adjusts VM or VP for final results

Texas Instruments

A detailed error analysis of the Improved Howland Current Pump shows that for worst case tolerances 1% resistors will only yield a 9% accurate Iout/Vin transfer function. Often this is okay as an outside control loop will re-adjust the Vin command voltage as needed. It its often the critical current control that is need in the overall control loop. If).1% resistors are used the accuracy of the Iout/Vin transfer function can be increased to 1%.

V-I Improved Howland Current Pump

$$IL := \frac{VP \cdot \left[\frac{RX}{RZ} \cdot \left(\frac{RF}{RI} + 1\right) + \frac{RS}{RZ}\right] - VM \cdot \left[\frac{RF}{RI} \cdot \left(\frac{RX}{RZ} + 1\right)\right]}{\left[\frac{RS}{RL} \cdot \left(1 + \frac{RX}{RZ}\right) + \left(\frac{RS + RX}{RZ}\right) - \frac{RF}{RI}\right] \cdot RL}$$

$$IL := \frac{VP \cdot \left[\left(1 + \frac{RF}{RI}\right) + \frac{RS}{RF}\right] - \left(\frac{RF}{RI} + 1\right) \cdot VM}{RS \cdot \left(1 + \frac{RI}{RF} + \frac{RL}{RF}\right)}$$

Set RX=RF and RZ=RI

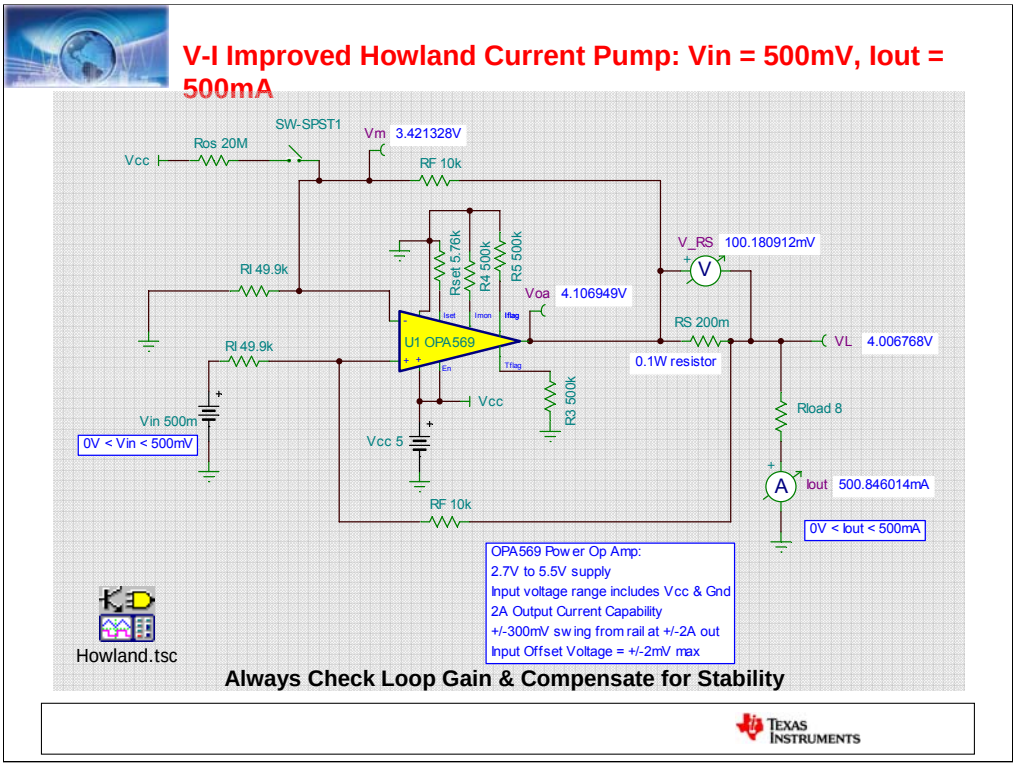
Assume:
RF = RX
RI = RZ
RF>>RS
RF>>RL

$$IL := \frac{(VP - VM) \cdot \frac{RF}{RI}}{RS}$$

Input Voltage is Gained up and Differentially forced across RS

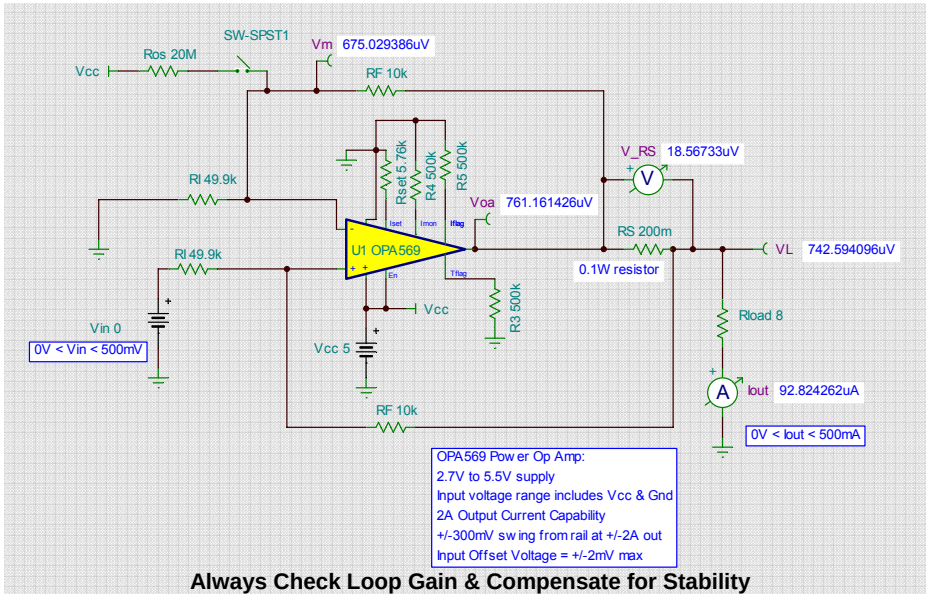
Texas Instruments

By using symmetrical values in the Improved Howland Current Pump and scaling the feedback much larger than the load or sense resistor (which is usually the case in applications using this circuit) the transfer function becomes more manageable and easier to use. The final transfer function clearly shows that this input voltage is gained up and impressed across the current sense resistor.



A high current implementation of the Improved Howland Current Pump is shown here using the OPA569 Power Op Amp. Attention must be paid to ensure adequate voltage headroom on the single supply. RR input on the OPA569 allows accurate current control down to zero volts out. Vin is gained by 10k/49.9k or about 0.2 and impressed across Rs of 200mohm. For 500mV in this means 100mV across 200mohm or Iout=500mA.

V-I Improved Howland Current Pump: Vin = 0V, Iout = 0A

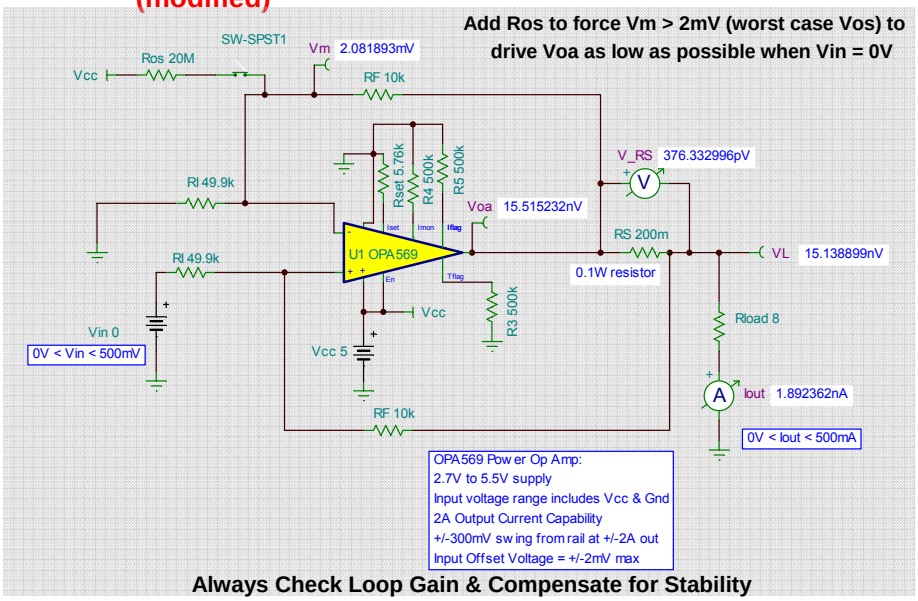


Always Check Loop Gain & Compensate for Stability

TEXAS INSTRUMENTS

For zero Vin we a 92uA current still through the load due to the input offset voltage of the OPA569.

V-I Improved Howland Current Pump : Vin = 0V, Iout = 0A (modified)



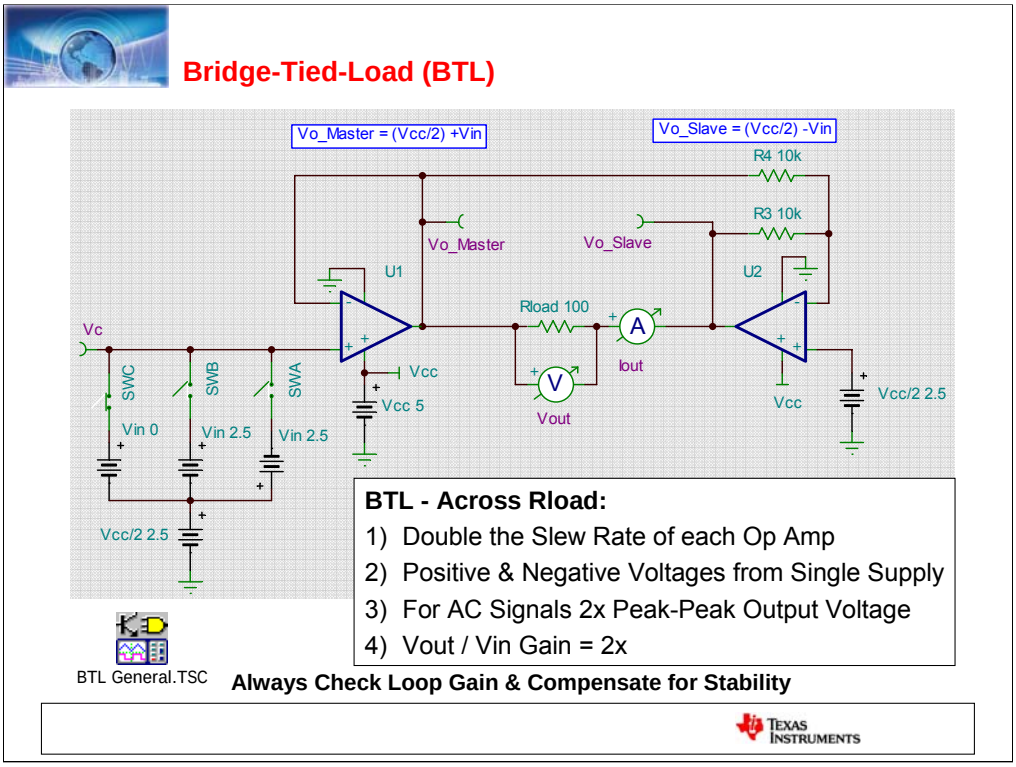
If we add Ros and sum in a 2mV offset into the input of the oPA569 we can ensure we drive the output of the OPA569 off in the case where Vin=0V. This offset should be greater than the worst case Vos of the oPA569. This large value resistor value for Ros will not appreciably degrade the scaling accuracy of the Iout/Vin transfer function.

Drive Circuits

Bridge-Tied-Load (BTL)

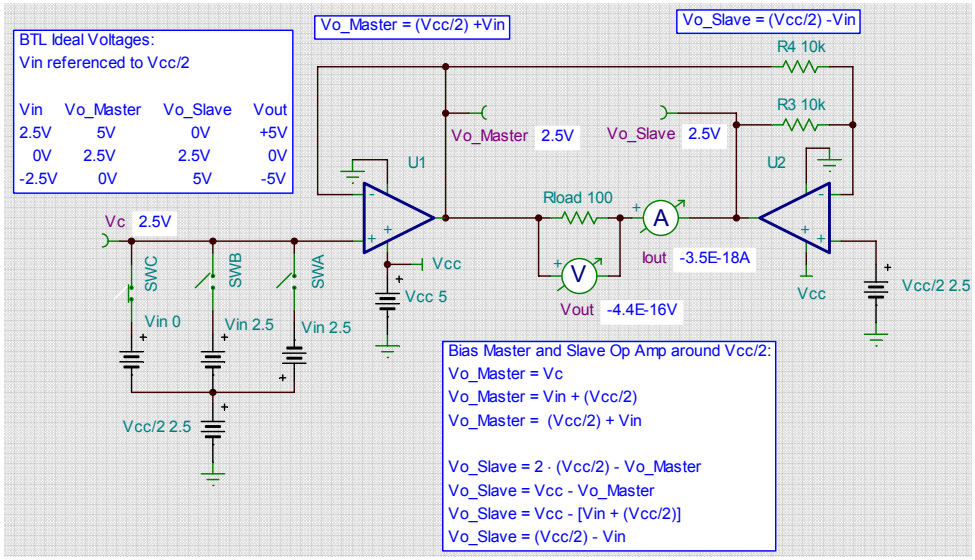
Parallel Op Amps

High Current Cascade Reference Buffer



The Bridge-Tied-Load (BTL) arrangement offers many advantages for single supply applications as long as the load can float (neither end of the load can be ground referenced). With the BTL positive and negative voltages can be created across the load using only a single supply. This occurs because U1 output can be at Vcc while U2 output is at ground creating a “positive” voltage across the load. If U1 output is now taken to ground and U2 output to Vcc we create a “negative’ voltage across the load. This effect allows one to create double the peak-to-peak voltage for an AC excitation application. Likewise the slew rate across the load is doubled. For example if U1 is slewing up at 1V/us then U2 output is slewing down at 1V/us with an effective 2V/us experienced at the load. The Vout/Vin transfer function is doubled for this configuration since a +1V change (relative to mid-supply) out of U1 results in a -1V change (relative to mid-supply) out of U2 yielding a net 2V change across the load.

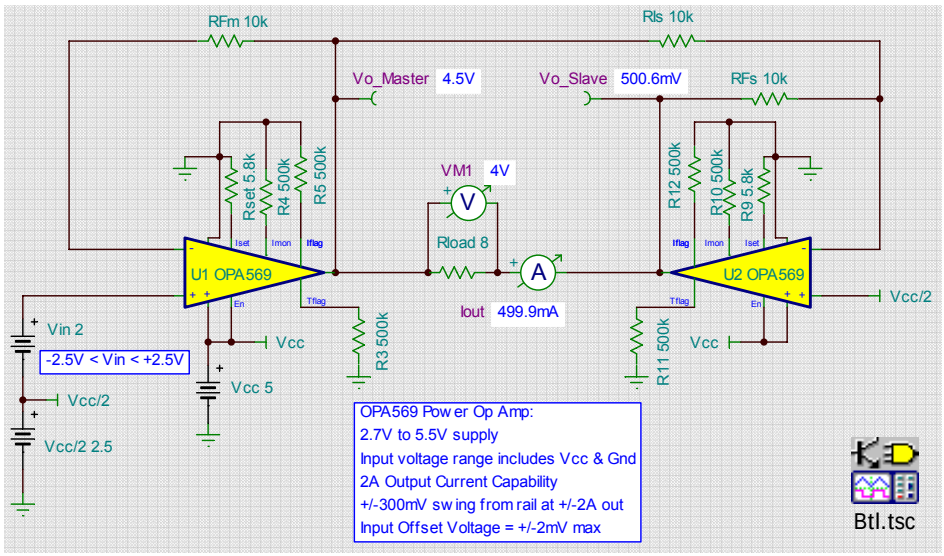
Bridge-Tied-Load (BTL): Vout = 0V



Always Check Loop Gain & Compensate for Stability

The BTL single supply application here is set for Master amplifier G=1, although other gains can be used. If the input Vin is reference to mid-supply as shown then Vin=0V will result in 0V across the load. If U1 and U2 have adjustable output current limits set the Master Amplifier to current limit first for balanced power dissipation in case of a load short between the two outputs.

Bridge-Tied-Load (BTL): Vout = +4V



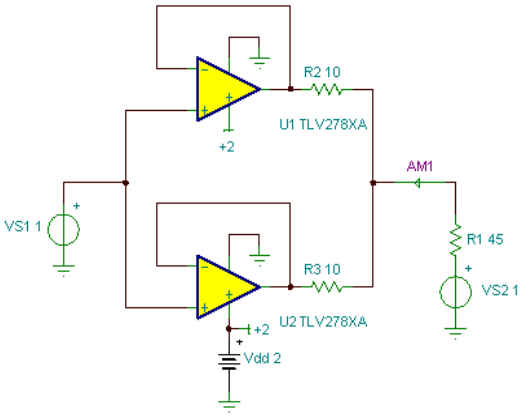
Always Check Loop Gain & Compensate for Stability

Two OPA569 power op amps in a BTL arrangement offer high current and close swing to the rail Here since we are set for G=1 on the Master Amplifier the load sees twice the voltage of Vin. For Vin = 2V the load is commanded to see 4V.

Parallel Op Amps

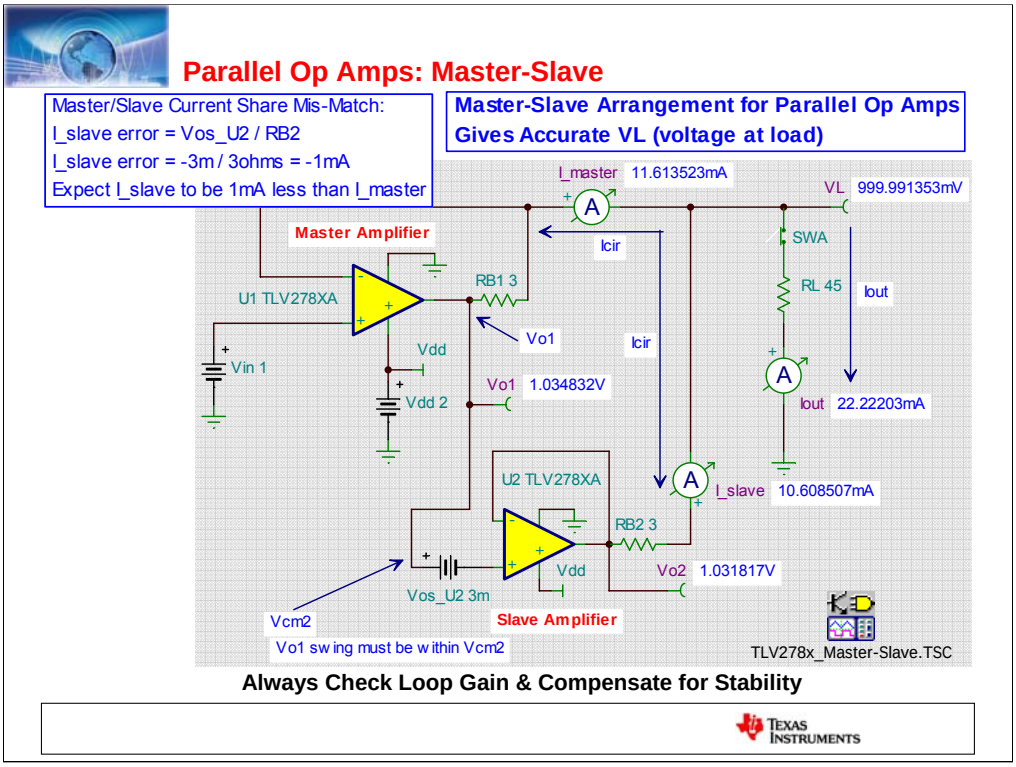
Why Parallel Op Amps?
Increase Current to Load
Keep Class AB Output
Easier than External Devices

Dual Drive Arrangement for Parallel Op Amps Does not Give Accurate VL (voltage at load)

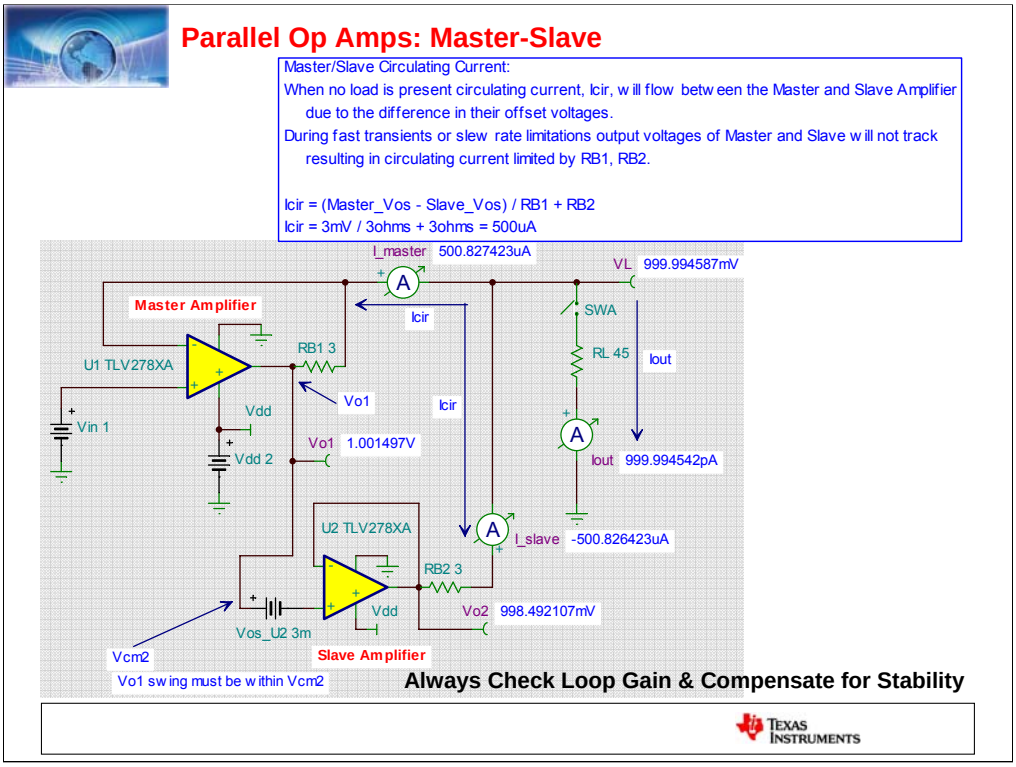


Texas Instruments

Parallel Op Amps offers an easy way to get higher current drive with closer swing to the rail using simple IC Op Amps. Ballast Resistors, Shown here as R2 and R3 are required in this implementation to reduce the effects of different Vos of each op amp which can cause high circulating current between the two op maps. This “Dual Drive” arrangement does not accurately control the voltage at the load.



This Parallel Op Amps: Master-Slave offers a way to get increased current drive but maintain accurate voltage at the load. This arrangement creates only a small load current sharing imbalance caused by the Slave Amplifier Vos divided by its ballast resistor, RB2.

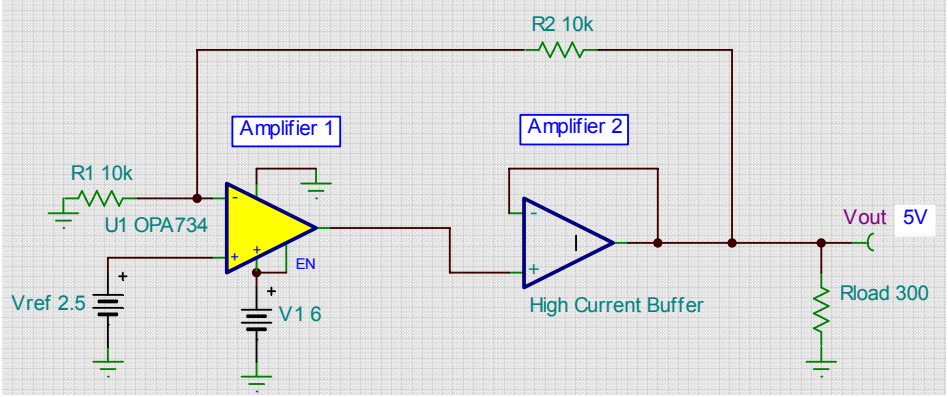


The use of Ballast resistors RB1 and RB2 limit circulating currents between the Master Amplifier and Slave Amplifier when no load is connected. For this arrangement the circulating current will be the difference in input offset voltages of the two amplifiers divided by RB1 + RB2. in addition load transients or fast slewing can cause the output voltages of the Master and Slave amplifiers not to track exactly resulting in circulating currents. As a rule-of-thumb it is recommended to limit the slew rate of parallel op amp configurations to about ½ of the op amp slew rate to prevent large circulating currents in a slew limited condition.

High Current Cascade Reference Buffer

High Current Cascade Reference Buffer:

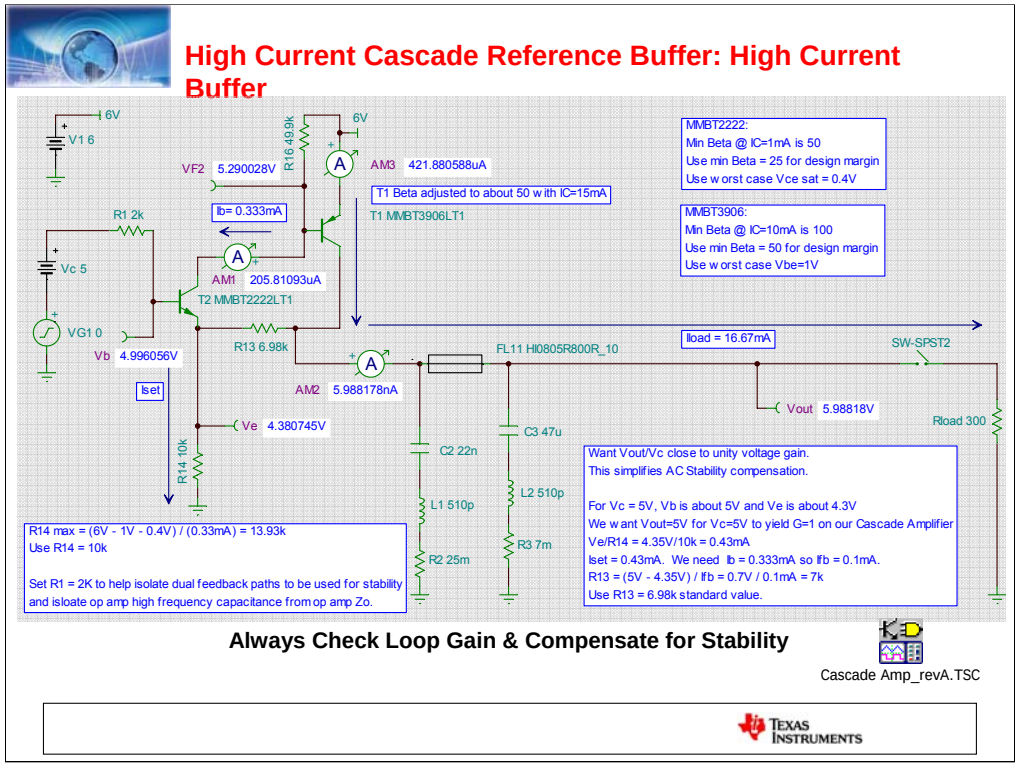
1) Amplifier 1 provides closed loop accuracy
2) Amplifier 2 provides high current & unity gain simplifies AC Stability compensation
3) Single supply demands close swing to rail on Amplifier 1 and Amplifier 2



Always Check Loop Gain & Compensate for Stability

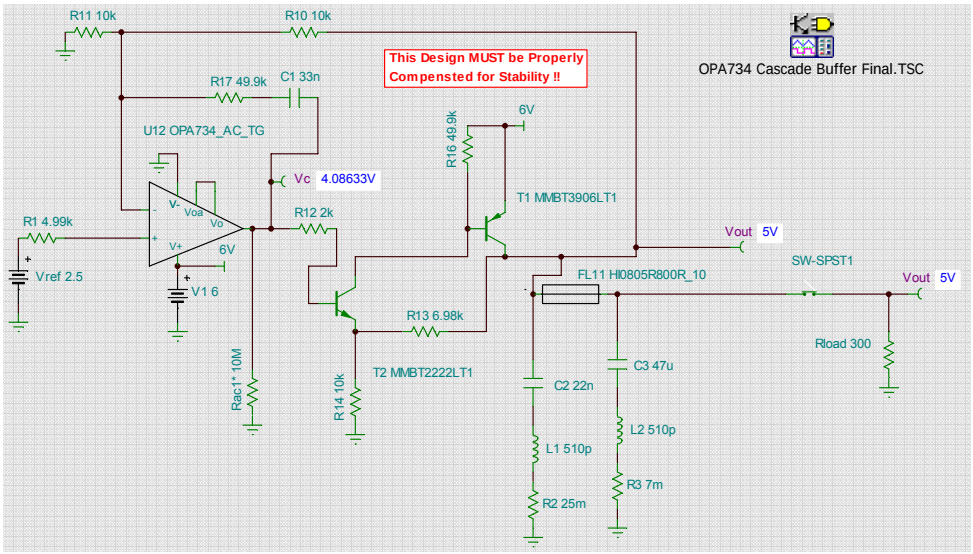
Texas Instruments

Sometimes in single supply applications it is necessary to create a buffered reference which needs to delivery high current. This can be effectively accomplished by the use of a cascade amplifier arrangement as shown above. Amplifier 1 can be an auto-zero accurate amplifier which does not required large drive currents. Amplifier 2 can be a high current unity voltage gain with high current capability. The loop is closed accurately around Amplifier 1. Single supply will require close swing to the rail on both Amplifier 1 and Amplifier 2.



The High Current Buffer is formed by a level shifting NPN transistor, T2, driving a PNP transistor, T1. T1 van swing close to the rail and with 5V to work with there is plenty of drive towards ground with T2 and overcome T1 Vbe plus provide adequate base current drive. In effect T2 can be thought of as a simple op amp with its –input at its emitter. WE use this T2, T1 amplifier instead of controlling a PNP transistor direct out of an op amp to help ease stability compensation with capacitive load. If we just drive a PNP transistor direct we end up with voltage gain in the feedback of the op amp. Voltage gain in the feedback of an op results in a negative 1/Beta, usually -20dB to -40dB depending upon the PNP transistor used. This makes compensating a cascade amplifier arrangement more difficult as direct feedback around an op amp from output to –input can never produce a 1/Beta of less than 1 or 0dB. We wil design our High Current Buffer to have about a gain of 1 for our given load and voltage output.

High Current Cascade Reference Buffer

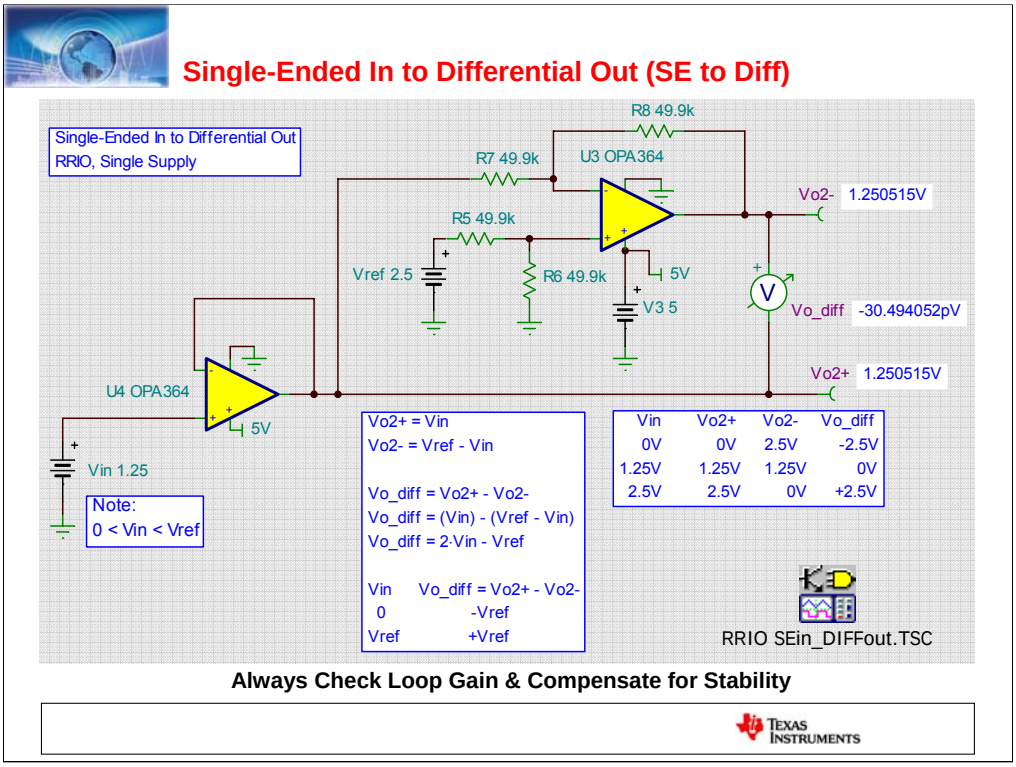


Always Check Loop Gain & Compensate for Stability

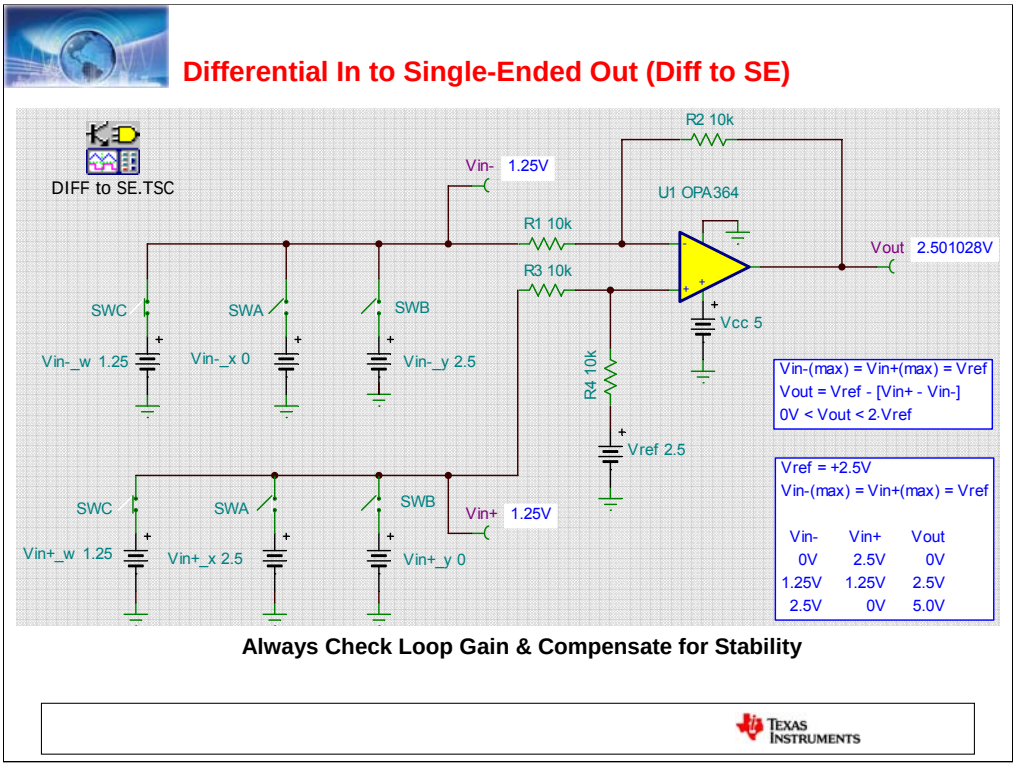
The final High Current Cascade Reference Buffer is shown above. A detailed loop gain AC stability analysis will confirm that this circuit is stable. This exercise is left to the user or contact Linear Applications, Texas Instruments, Tucson Division for assistance.

Translation Circuits

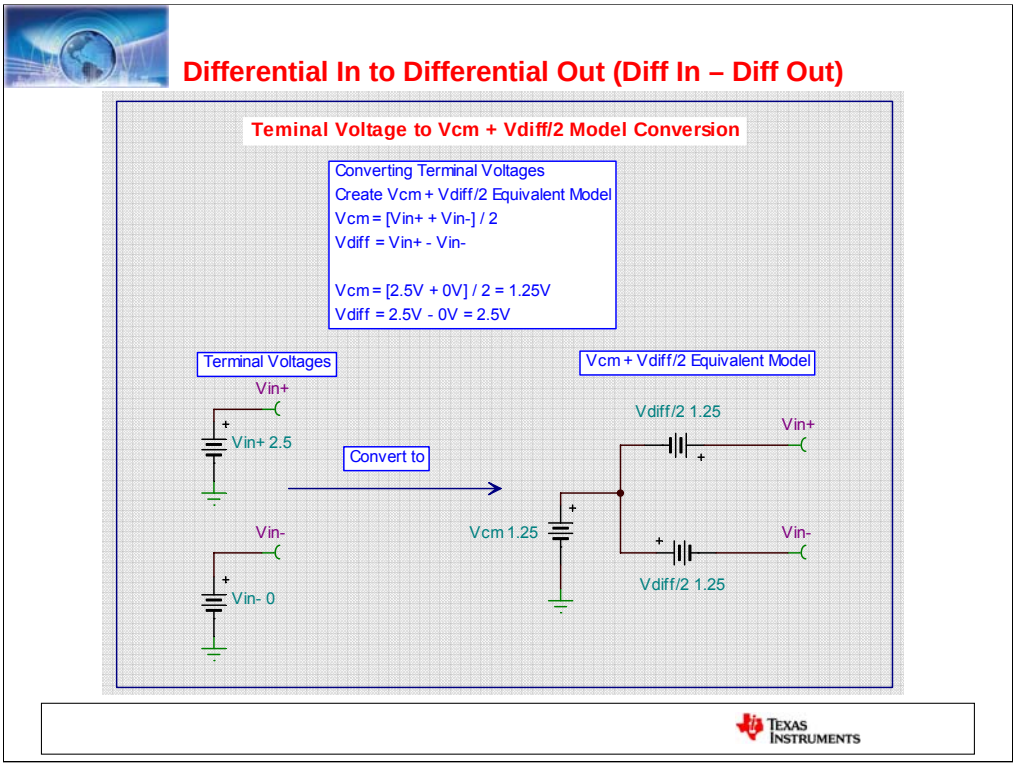
Single-Ended In to Differential Out
Differential In to Single-Ended Out
Differential In to Differential Out



This Single-Ended In to Differential Output circuit will accept input voltage levels from 0 to Vref. Vref here is 2.5V. The details shown above show the proper accurate conversion for single-ended Vin of 0V to 2.5V yielding a differential output of -2.5V to +2.5V. If a good single supply difference amplifier with close swing to the rail and auto-zero for low offset voltage and drift it can replace U3.

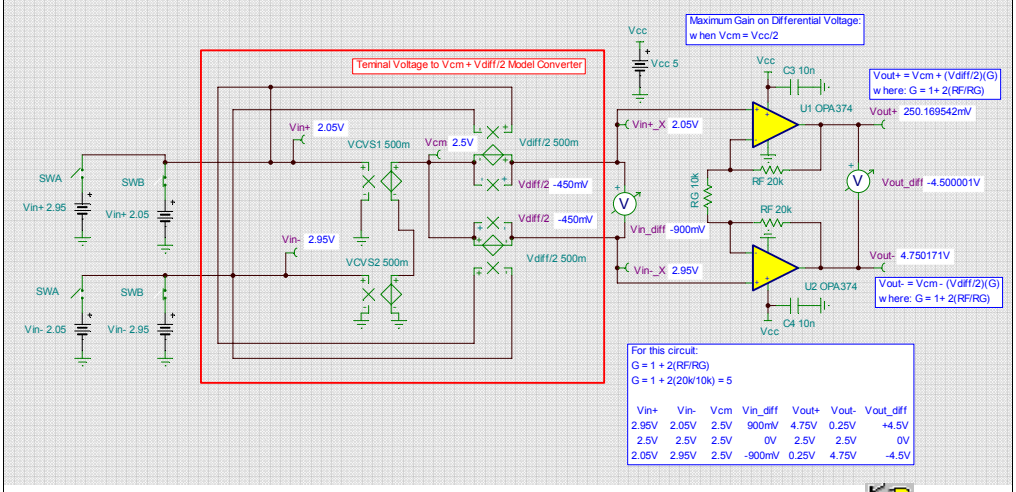


Differential In to Single-Ended Out is easily achieved by a Difference Amplifier as shown here. With the +input of the Difference Amplifier offset by Vref =Vcc/2. With a +/-2.5V (with reference to Vcc/2) differential input a single-ended output of 0V to 5V is provided.



Or analysis of Differential In to Differential Out amplifiers it is convenient to create a mathematical equivalent model of input voltages which will simplify analysis. This "Terminal Voltage to Vcm + Vdiff/2 Model" is shown above.

Differential In to Differential Out (Diff In – Diff Out)



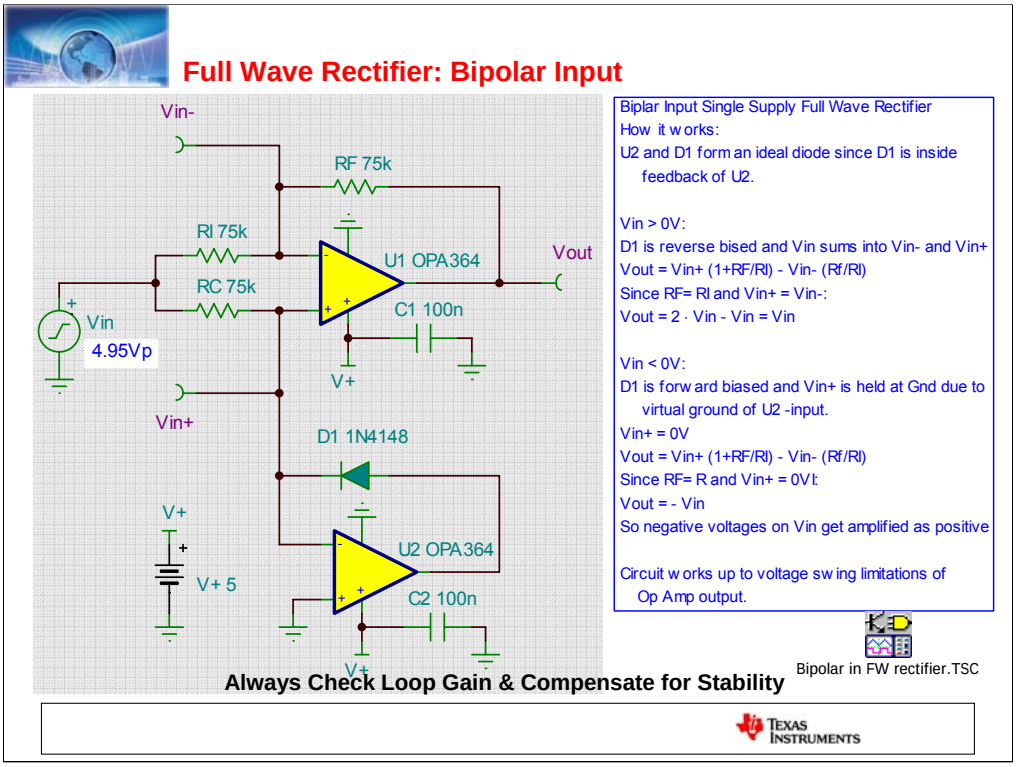
Always Check Loop Gain & Compensate for Stability

DIFF in to DIFF out.TSC

Detailed analysis using the “Terminal Voltage to Vcm + Vdiff/2 Model” will result in the equations Vout+ and Vout- shown in this slide. Note that these voltages swing symmetrically about Vcm which is why, for maximum differential gain, it is desirable to have Vcm = Vcc/2. Here we can translate +/-900mV differential input (with reference to Vcm = Vcc/2) to +/-4.5V differential output (with reference to Vcm = Vcc/2). If we did not want gain (G=1) we could simply remove RG. The TINA SPICE circuit contains a pre-built “Terminal Voltage to Vcm + Vdiff/2 Model” conversion circuit to help with Vout+ and Vout- analysis.

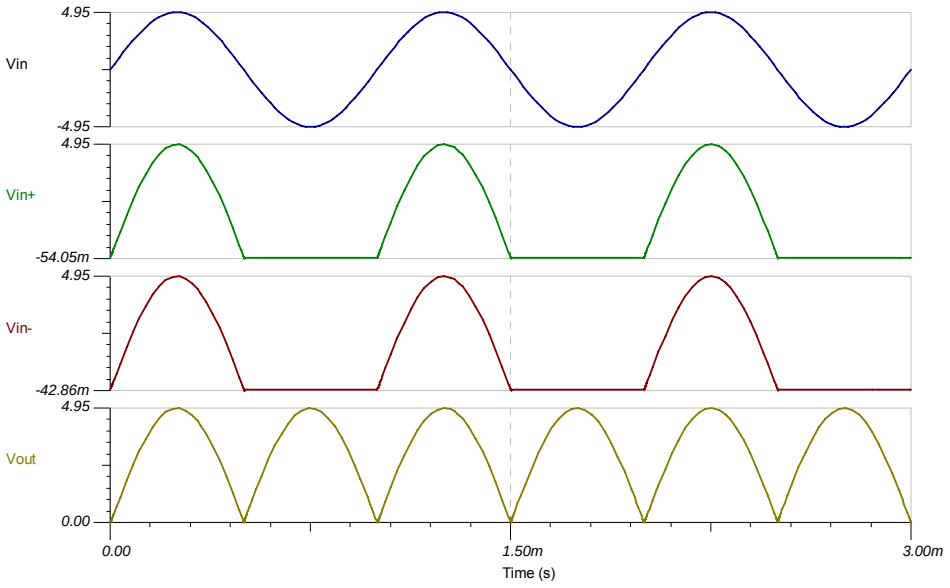
Conditioning Circuits

Full Wave Rectifiers
Supply Splitter
Integrator in Feedback
Isolation Amplifier
G=+1, G=-1 Amp



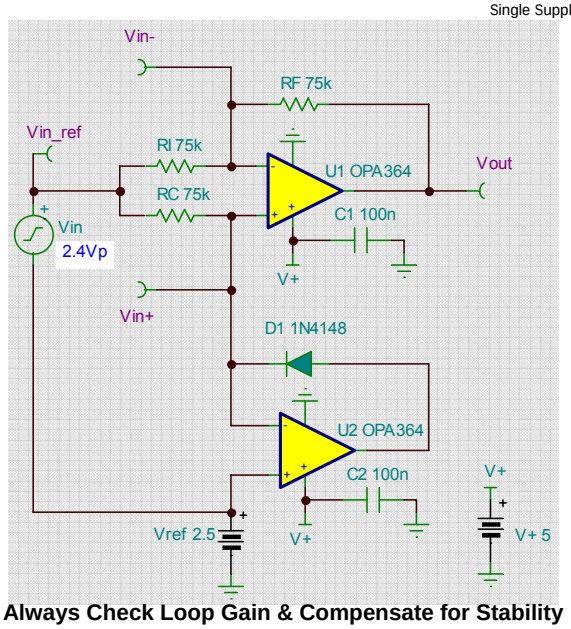
This clever Full Wave Rectifier: Bipolar Input circuit accepts negative peak sine waves (up to the supply rail of the device 5V in this example). For our supply of +5V this circuit will accept up to a 10Vpp sinewave centered on zero volts with +5Vp and -5Vp. For positive peaks (above ground) U1 acts as a summer amplifier and U2 and D1 are out of the picture. For negative peaks (below ground) D1 and U2 form a ground clamp and drive the +input of U1 to be held at 0V or ground. U1 now acts only as an inverting amplifier. The result is a full wave rectified sinewave at Vout.

Full Wave Rectifier: Bipolar Input



Full Wave Rectifier: Single Supply Input

Single Supply mid-ref FW rectifier.TSC

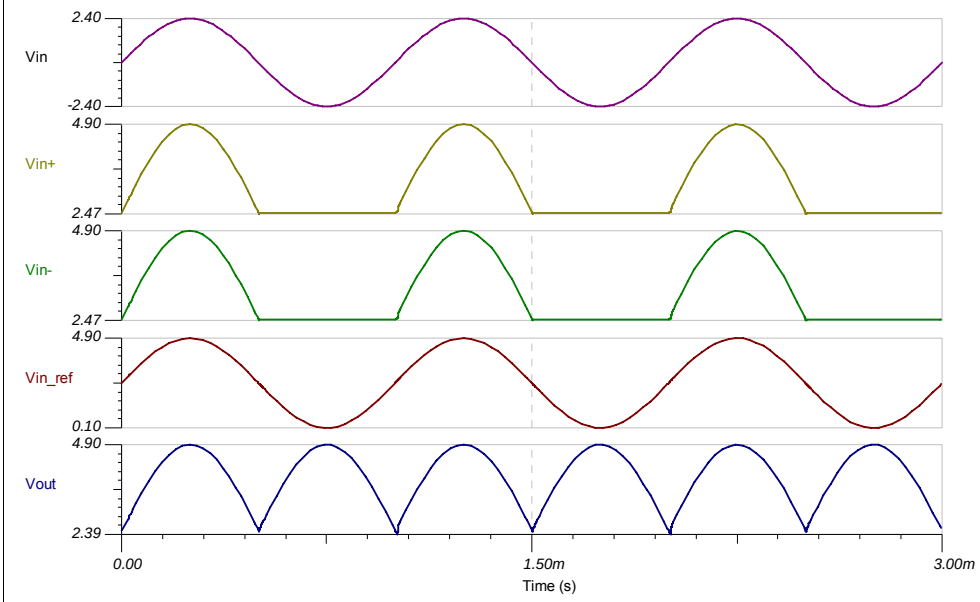


Always Check Loop Gain & Compensate for Stability

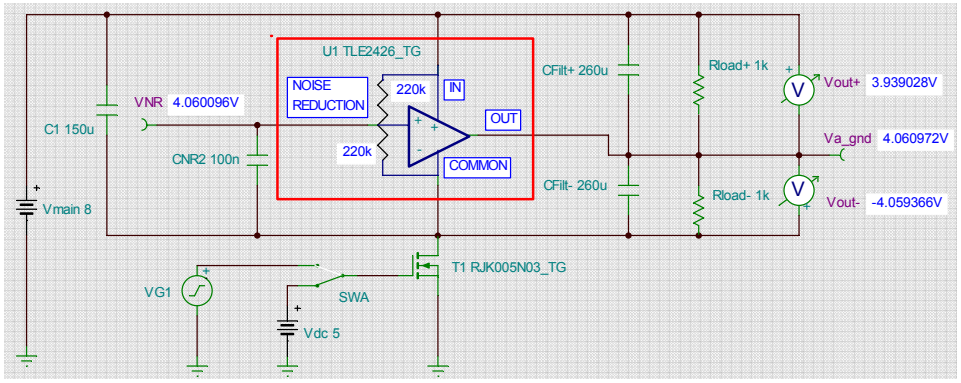
TEXAS INSTRUMENTS

The same Full Wave Rectifier: Bipolar Input circuit can be used for single supply sine waves referenced to mid-supply of Vcc/2 as shown above by simply changing the reference point (+input) of U2 to the mid-supply reference.

Full Wave Rectifier: Single Supply Input



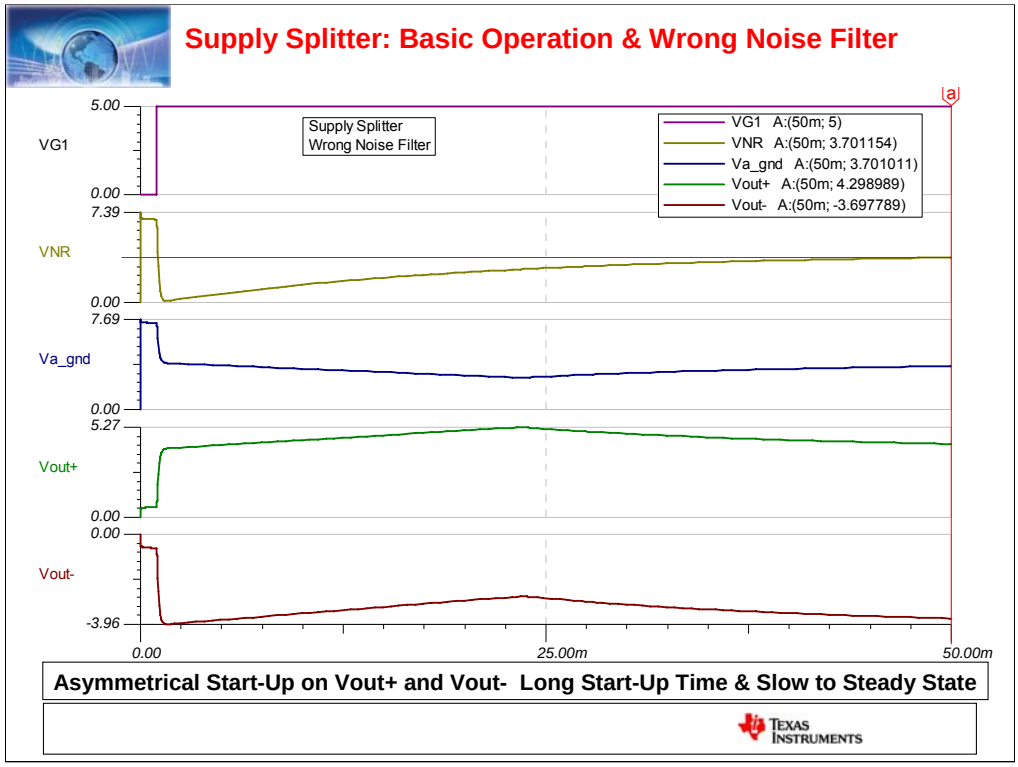
Supply Splitter: Basic Operation & Wrong Noise Filter



Always Check Loop Gain & Compensate for Stability

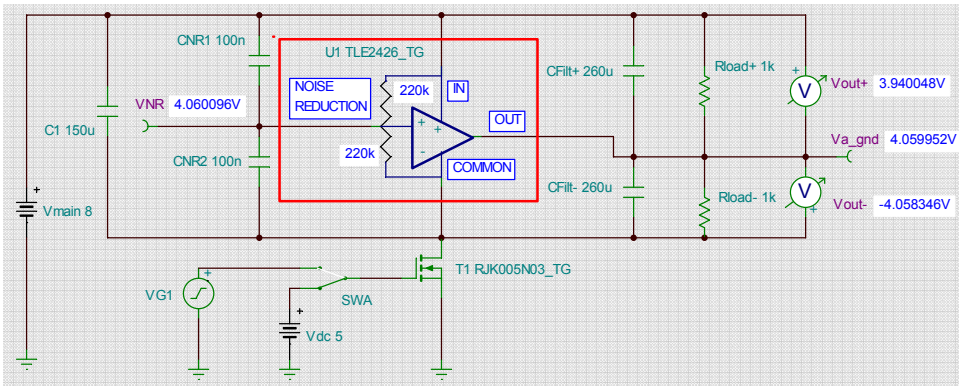
Supply Splitter Wrong.TSC

The TLE2426 is an op amp with two internally matched resistors intended to be used as a supply splitter as shown in this slide. The TLE2426 is designed to drive large capacitive loads. Any single supply op amp can be used as a supply splitter in the arrangement shown in this slide. A noise reduction pin which sets the supply midpoint is brought out to add additional capacitive filtering to lower overall noise on the output of the TLE2426, Va_gnd. As shown here we will add a 100nF noise filter capacitor, CNR2 as shown. Lets now see what type of transient turn-on behavior this circuit will have.



With tour noise reduction capacitor, CNR2, we see an asymmetrical startup on each of our supplies< Vout+ and Vout-. In addition it takes a long time to reach steady state, up to 50ms.

Supply Splitter: Right Noise Filter

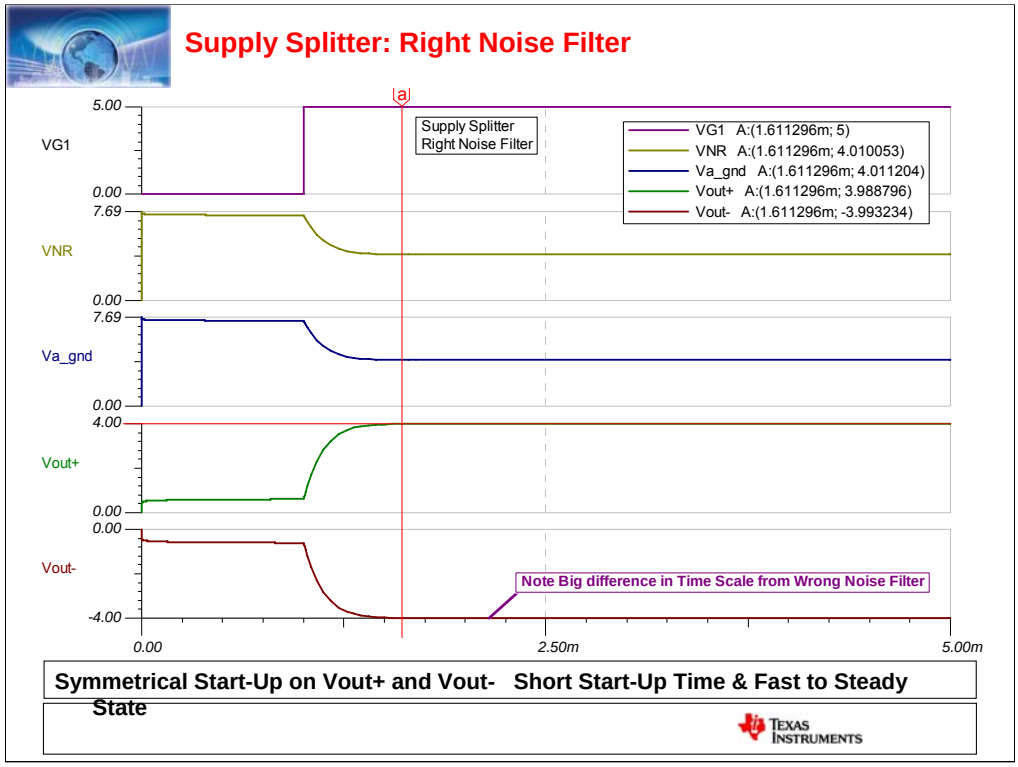


Add CNR1 for symmetrical and rapid start-up of Va_gnd

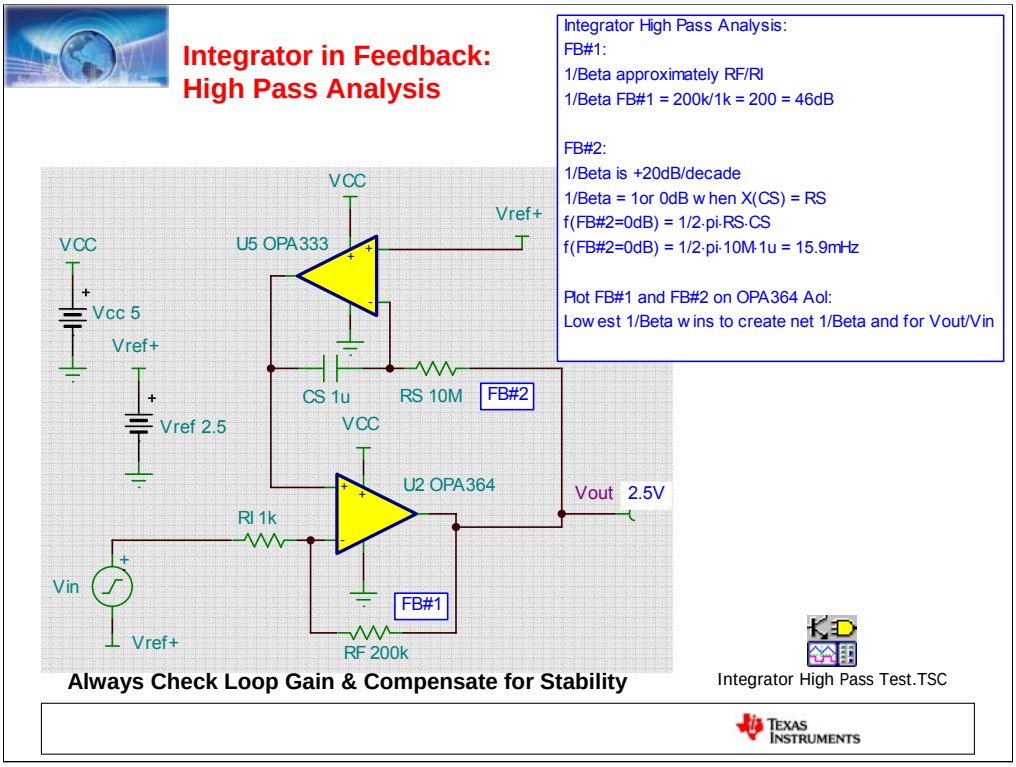
Always Check Loop Gain & Compensate for Stability

Supply Splitter Right.TSC

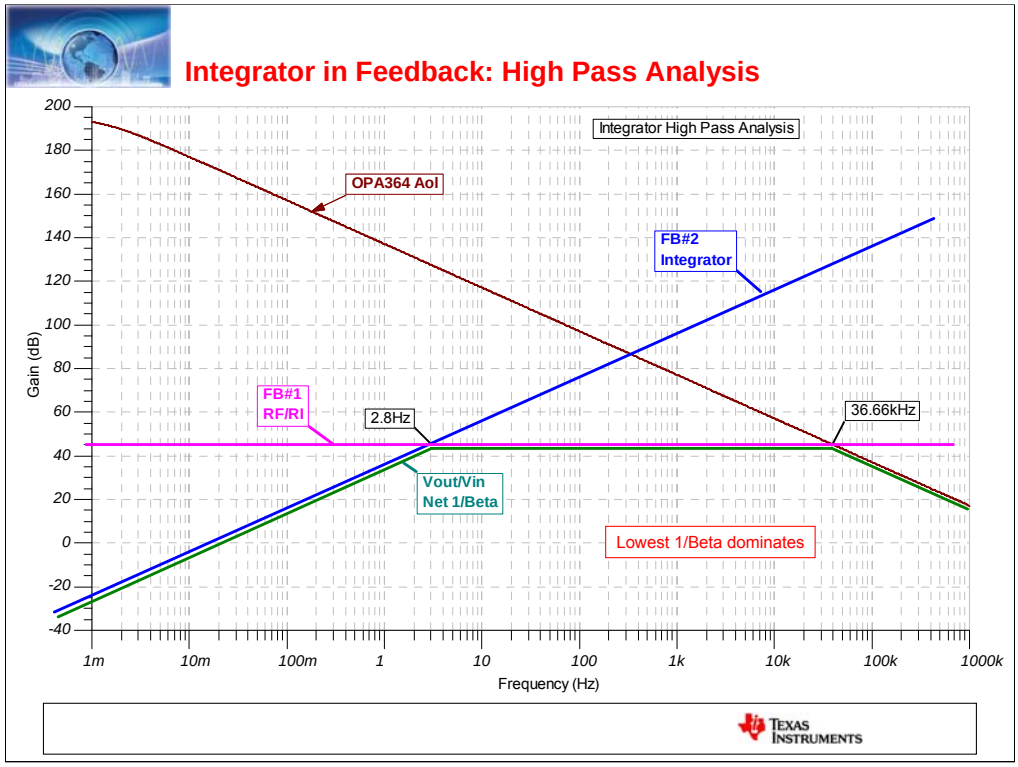
Here we will add CNR1 to quickly charge VNR, the noise reduction pin on the TLV2426 and the mid-supply reference point for Va_gnd in the system.



Results of the additional capacitor CNR1 to the noise reduction pin of the TLV2426, VNR, shows dramatic improvement with symmetrical outputs on Vout+ and Vout- and a short start-up time to steady state of about 1.6ms.

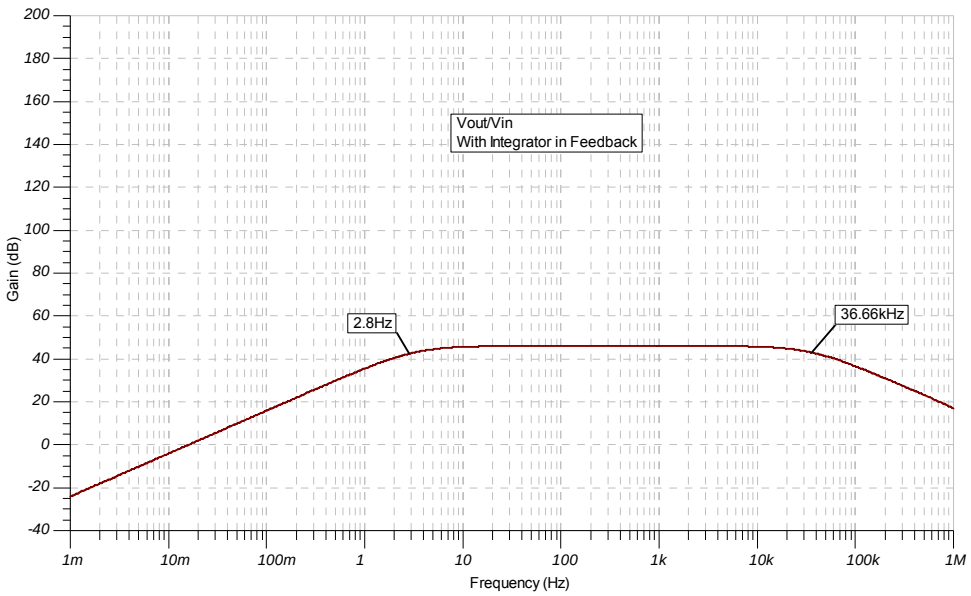


A useful building block for many popular single supply circuits such as Medical ECG and Photodiode Transimpedance Amplifiers is an Integrator in Feedback as shown in this slide. Let's first analyze how this creates a High Pass Filter function for the signal conditioning amplifier U2. Observe that there are two feedback paths around U2, FB#1 and FB#2. FB#1 is composed of RF and RI and is flat for all frequencies. FB#2 is our integrator and at low frequency will feed back large voltages from Vout due the gain created by CS and RS. Large fed back voltage means large Beta or inversely small 1/Beta. As frequency increase Cs goes towards a short and the gain of the integrator decreases meaning smaller voltages fed back. Smaller voltages fed back means smaller Beta or inversely larger 1/Beta. Since there si only one reactive element, CS in the feedback we predict a 1/Beta plot for FB#2 to have +20dB/decde slope.

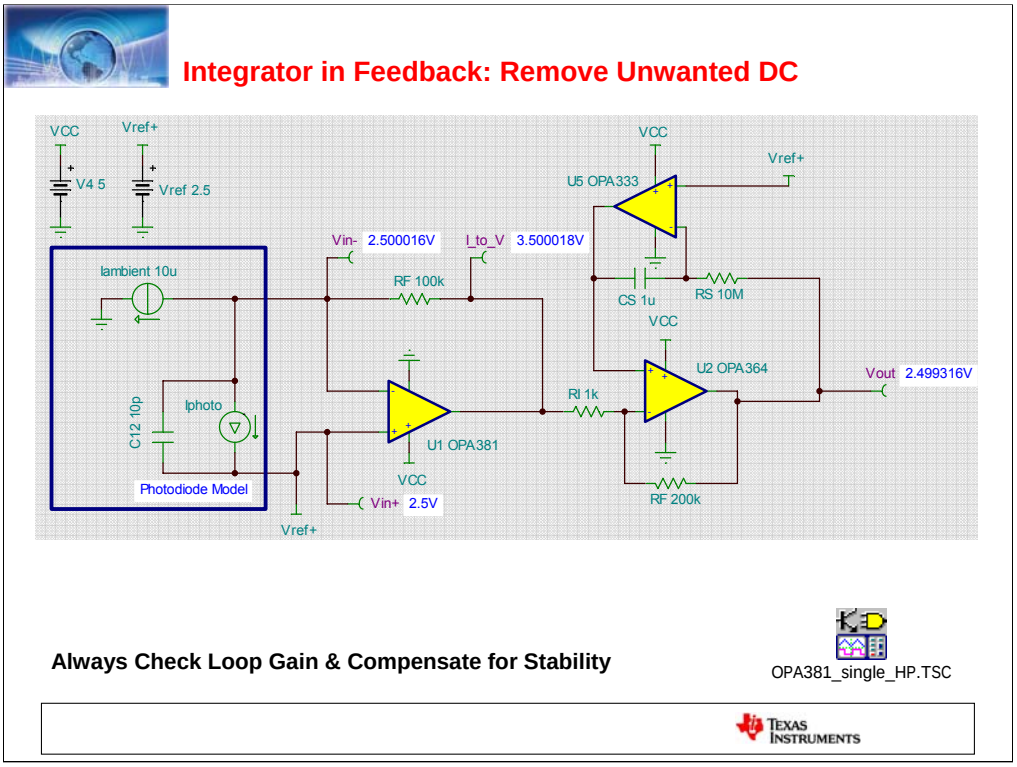


Our hand analysis of FB#1 and FB#2 plotted on the Aol for the signal conditioning amplifier U2 is shown here. Stability Analysis rules tell us when using dual feedback paths around op amp circuits the largest β path will dominate. An easy analogy to remember is that if two people are talking to you in one ear which person do you hear the easiest – the one talking the loudest! So the op amp will “listen” to the feedback path with the largest β or smallest 1/β. The net 1/β plot the op amp sees is the lower one at any frequency of FB#1 or FB#2.

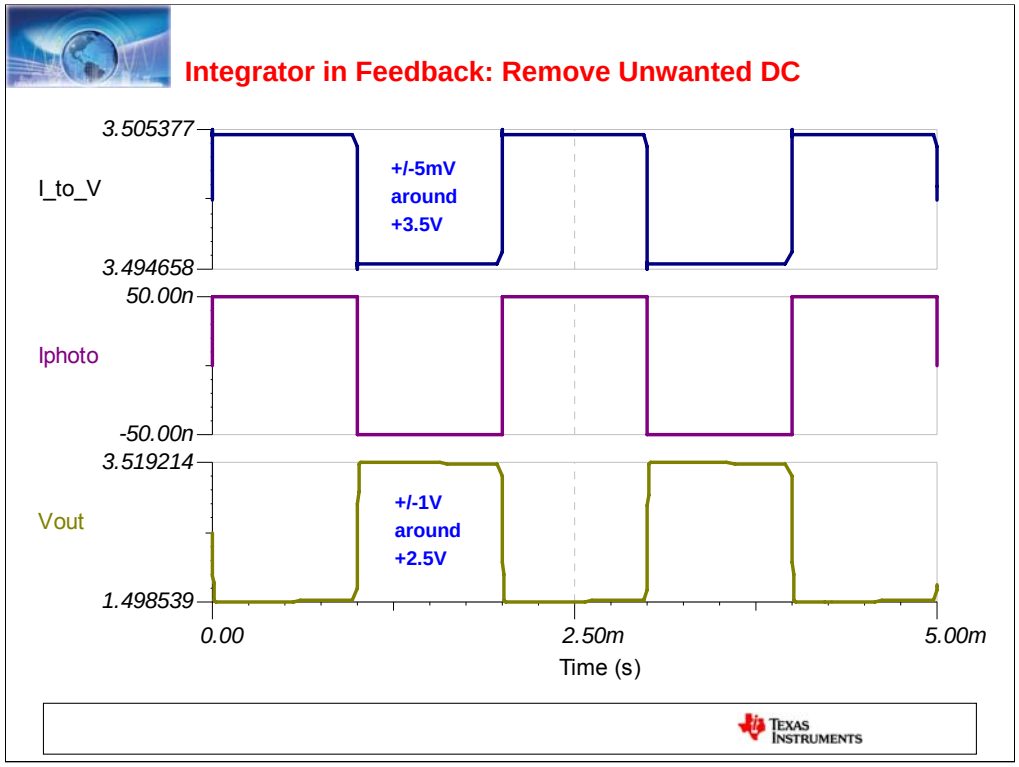
Integrator in Feedback: High Pass Analysis



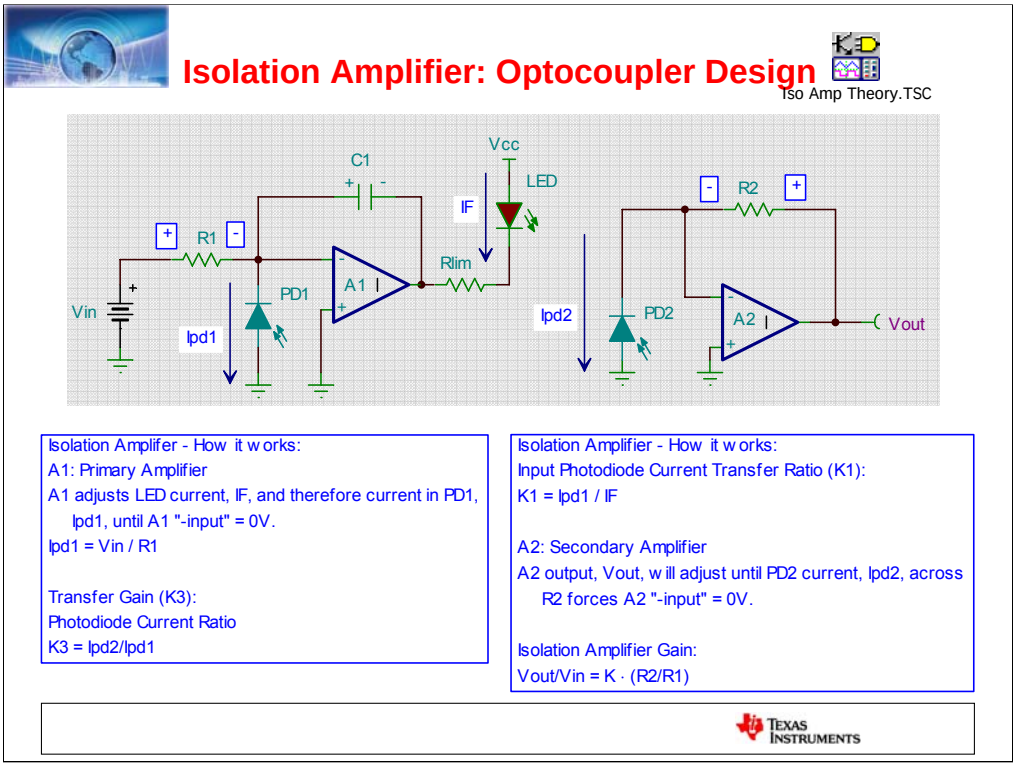
A TINA Spice simulation confirms our hand analysis predictions.



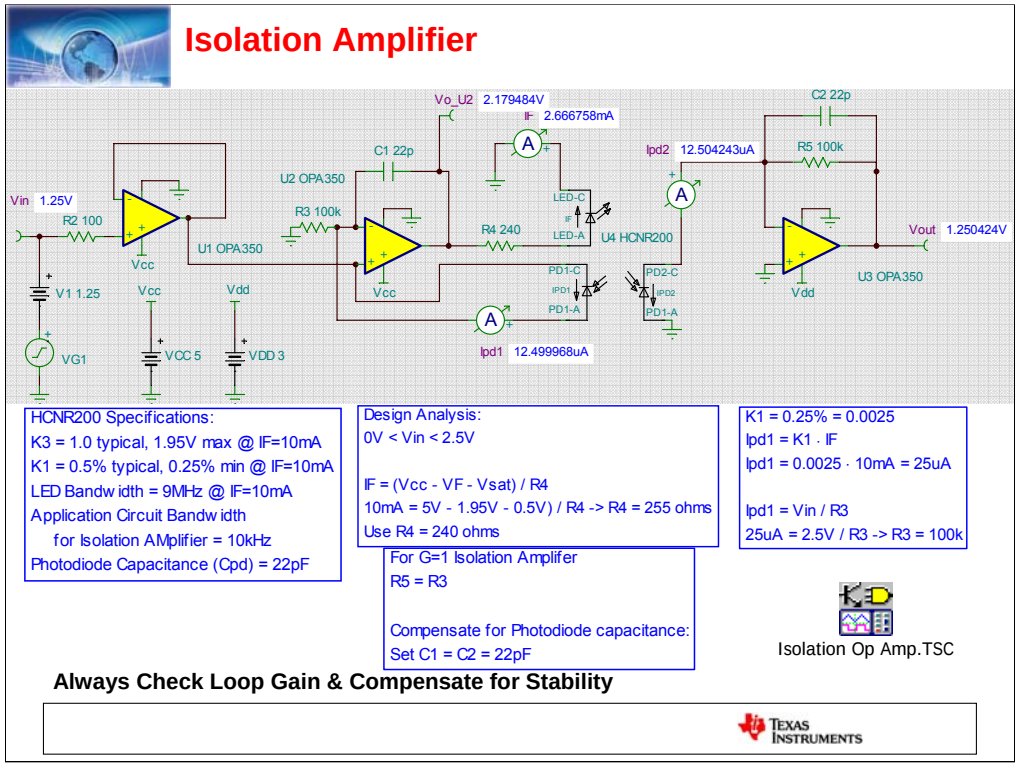
Besides providing a High Pass Filter Function for our signal amplifier an Integrator in Feedback path will also remove unwanted DC components of a signal. In this example a Photodiode Transimpedance Amplifier is formed by U1. This is a pulsed photodiode application in the presence of undesired ambient light represented in the schematic by Iambinet, a DC photodiode current. If we are to gain up the pulsed photodiode current for an accurate reading we need to first remove the unwanted DC component created by the ambient light. U2 will provide a gain of 200 on our desired pulsed photodiode current but remove the unwanted DC by Integrator in Feedback formed by U5, CS, and RS. If removed the integrator we would be unable to achieve any appreciable gain our pulsed signal without saturating the output f U2 do to the large DC offset driving it out of U1.



With our Integrator in Feedback we are able to amplify our desired pulsed current of +/-50nA (+/-5mV out of U1) by a gain of 200 by rejecting the DC offset out of U1. Now a our +/-5mV signal becomes a readable +/-1V signal ! This is all referenced to our 2.5V supply midpoint.

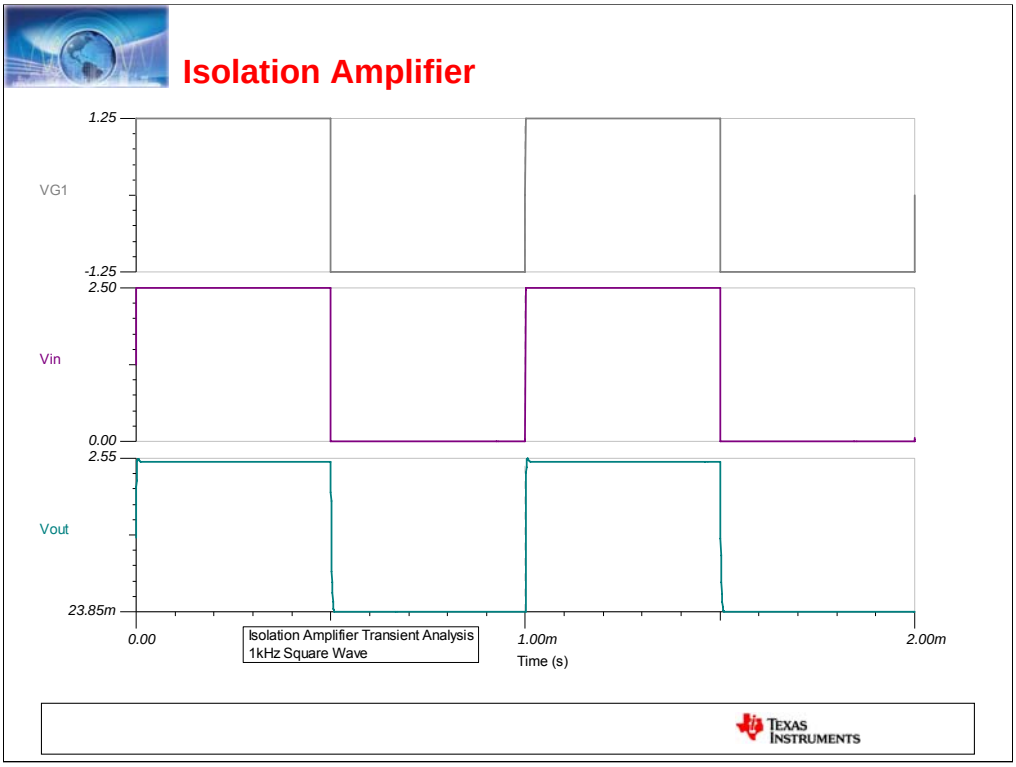


An isolation amplifier is easy to build on a single supply by using a RRIO op amp and an optocoupler. The Isolation Amplifier: Optocoupler Design is detailed in this slide.

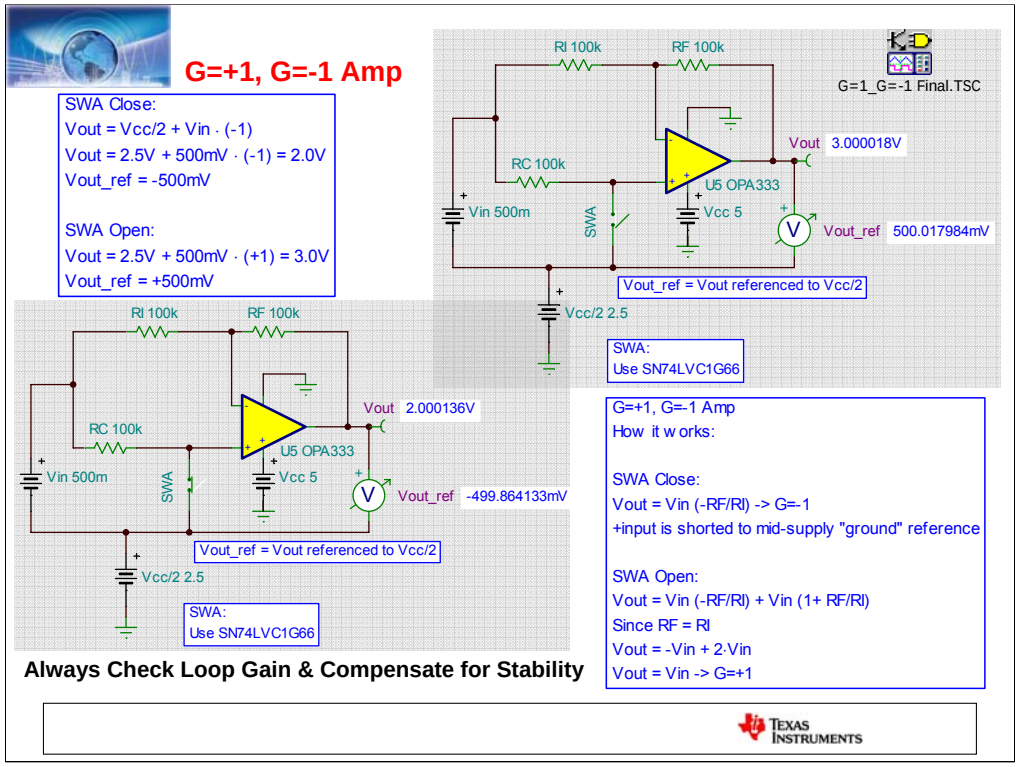


A high current drive with close swing to the rail , RRIO, single supply amplifier such as the OPA350 along with a good optocoupler such as the HCNR200 can be used as shown in this slide to build a single supply Isolation Amplifier.

Isolation Amplifier



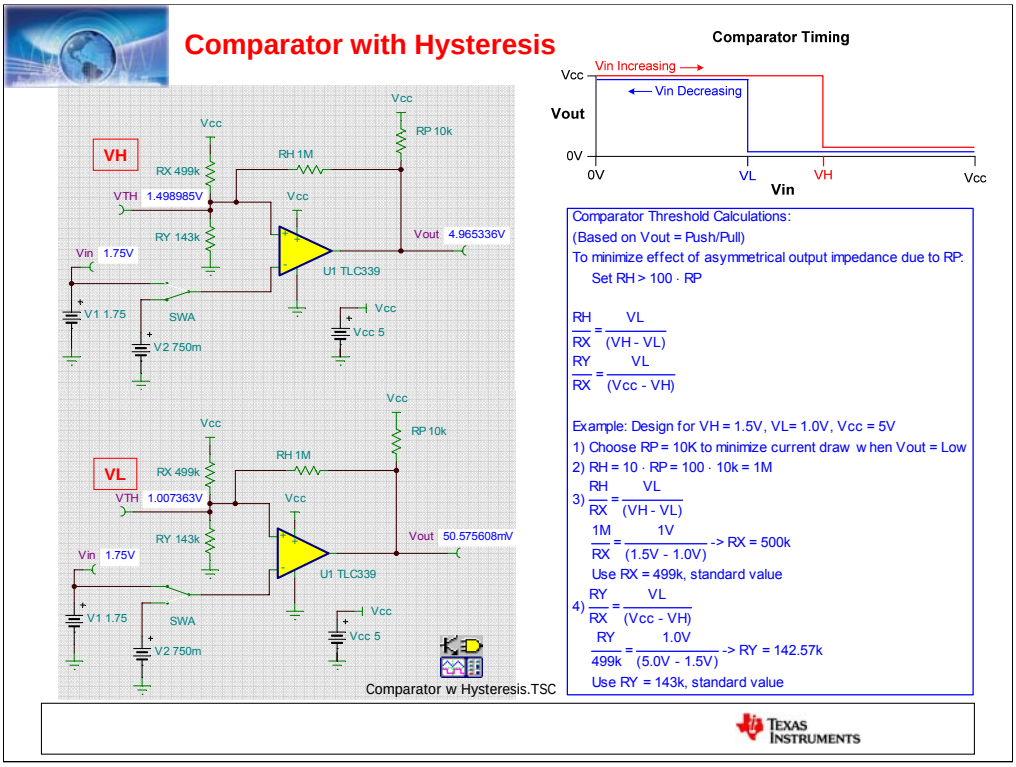
The transient response for our Isolation Amplifier is shown here with excellent results.



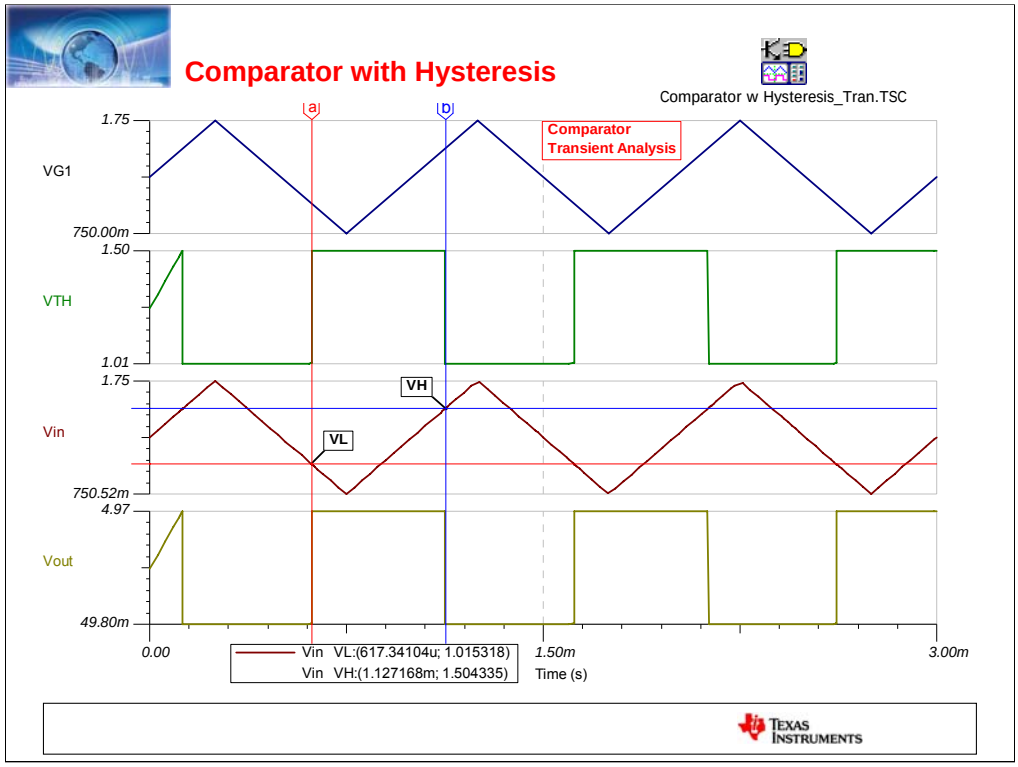
This handy circuit uses a single supply op amp, OPA333 and one single supply, single gate switch, SN74LVC1G66 to create a digitally controlled G=1, G=-1 Amp. For our single supply application Vcc/2 can be viewed as ground. With SWA closed no input signal is driven into the +input of Y5 and therefore we have an inverting amplifier with G=-1. When SWA is opened signal is available on the +input of U5 and we having a summing amplifier that yields a net gain of G=+1 !

Comparator Circuits

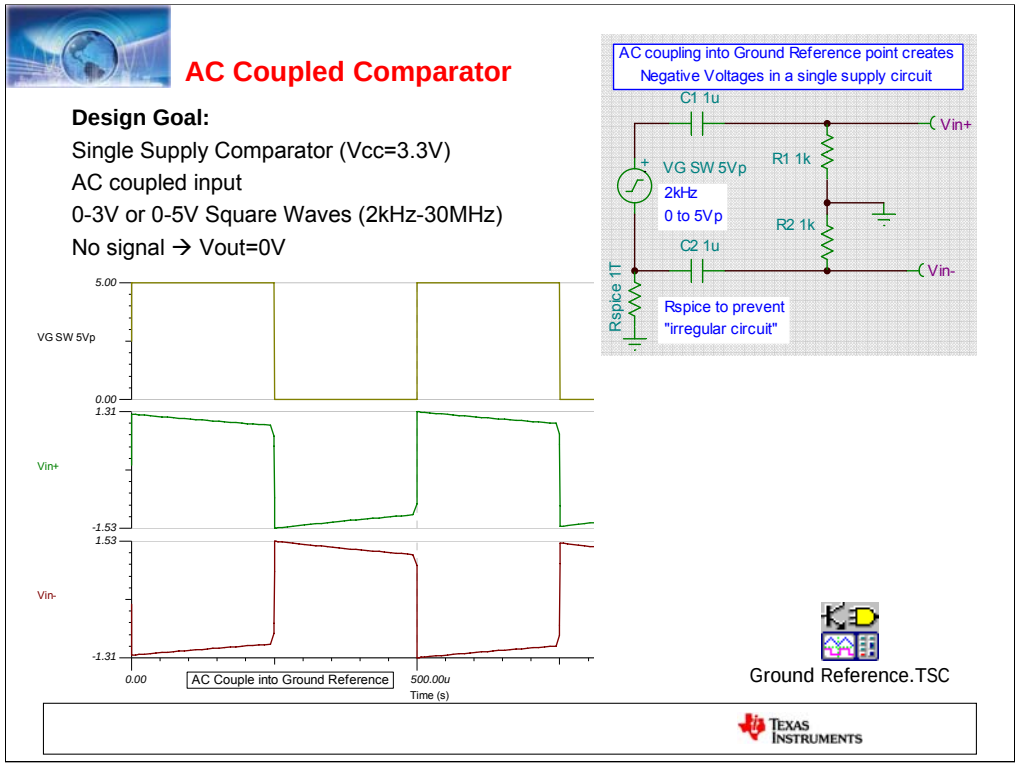
Comparator with Hysteresis
AC Coupled Comparator



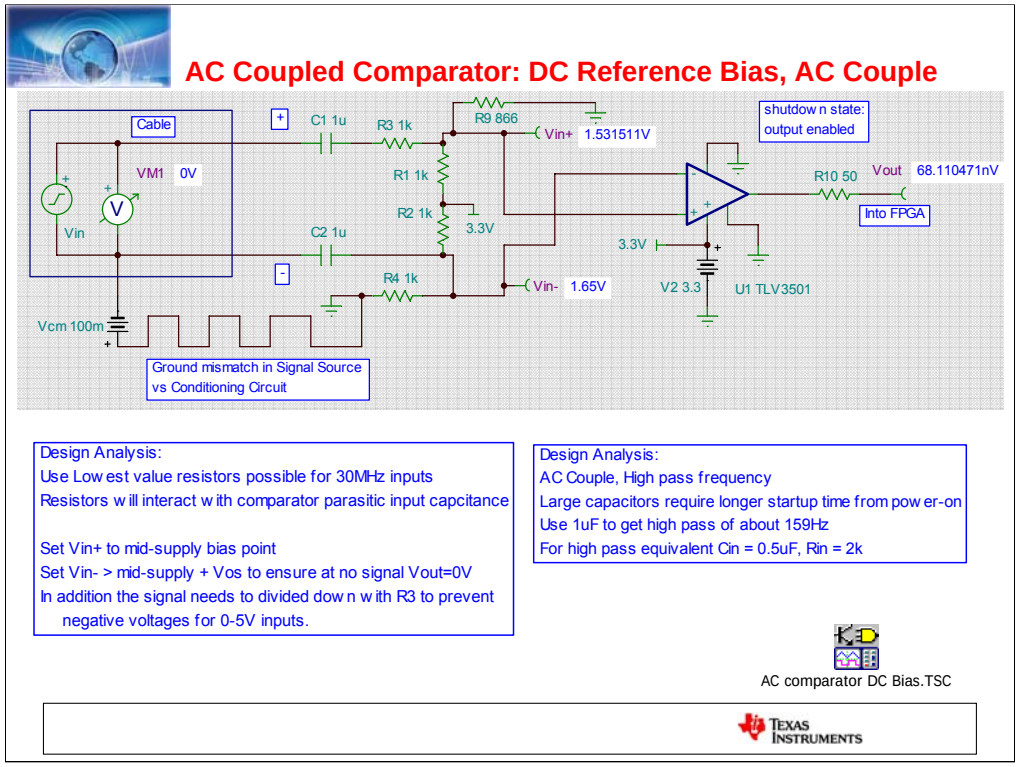
A common comparator circuit is shown here. Easy to use formulae are given to compute the positive and negative going thresholds. The formulae are based on a push-pull comparator output which is low impedance with respect to RH, the resistor used to add hysteresis to the circuit. However, the formulae can be used to produce very god results when using an open drain comparator with a pull-up resistor, RP. IF RH is set 10 to 100 times greater than RP than the accuracy of the formulae will be sufficient for most applications. If not a more detailed analysis will be required.



The results of our transient analysis test for our comparator with hysteresis circuit are shown above.

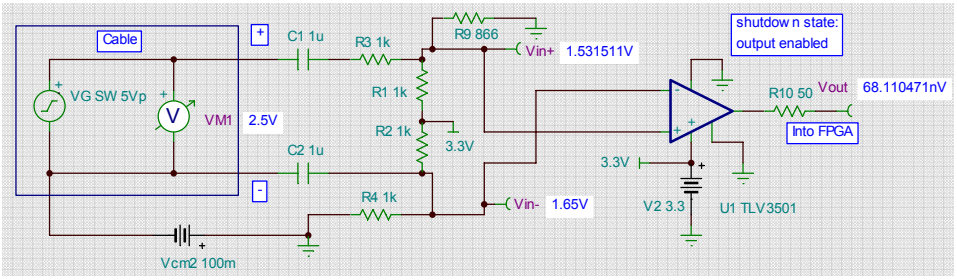


Sometimes a single supply comparator is required to use AC coupling to detect sine waves or square waves. Whenever AC coupling is involved into single supply circuitry negative voltages become a concern. Excessive negative voltages on comparators can cause the to trip erroneously or to stay stuck at unpredictable levels. For our AC Coupled Comparator example our design goals are detailed in this slide.

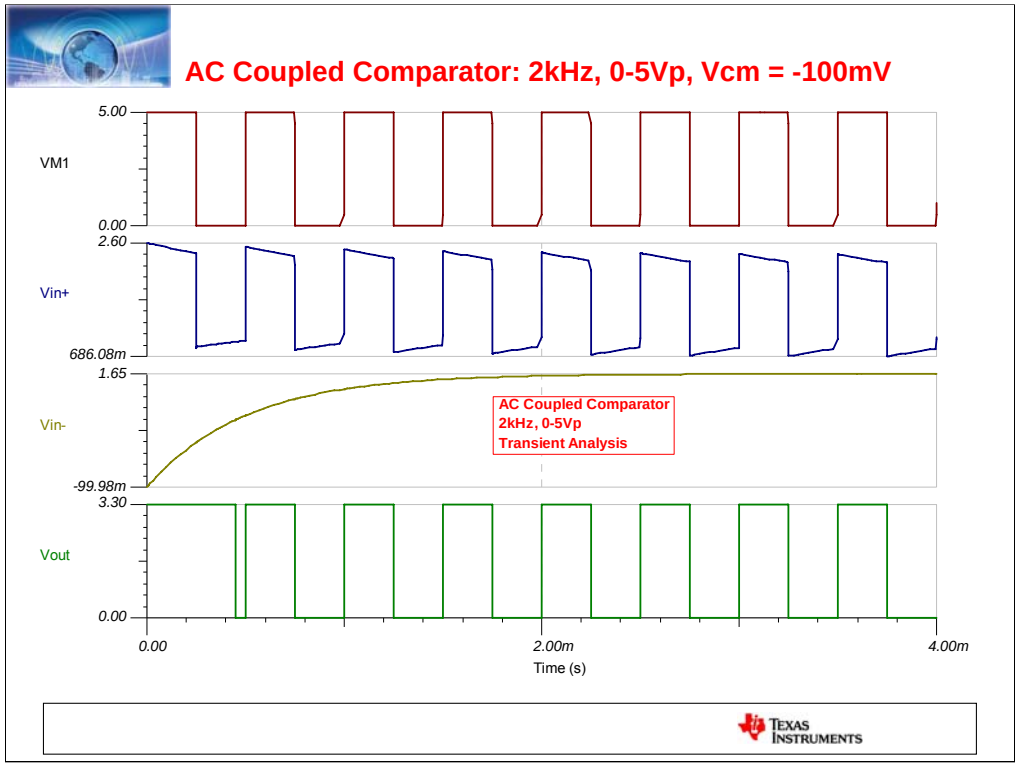


There are two design concerns in our AC Coupled Comparator circuit: DC Reference Bias circuitry and AC Couple circuitry. The design details of how to accommodate each of these concerns is shown in this slide.

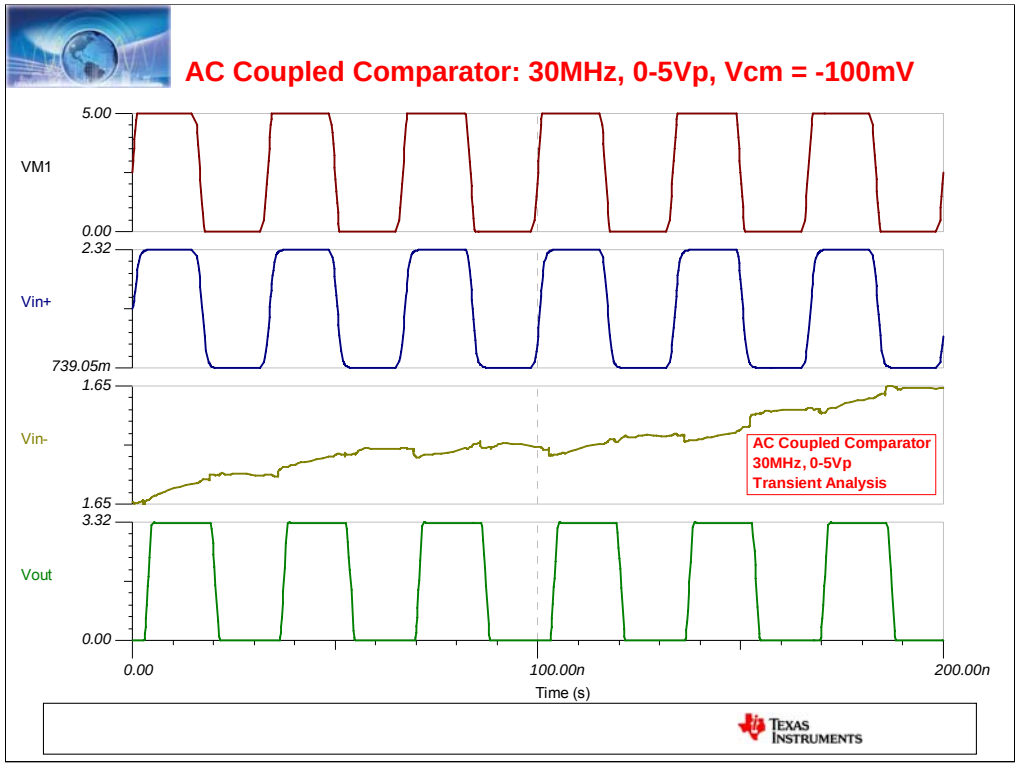
AC Coupled Comparator: Transient Test Circuit



AC comparator couple_Square.TSC



The transient analysis results of our AC Coupled Comparator for 2kHz, 0-5Vp, Vcm = -100mV are shown here.



The transient analysis results of our AC Coupled Comparator for 30MHz, 0-5Vp, Vcm = -100mV are shown here.

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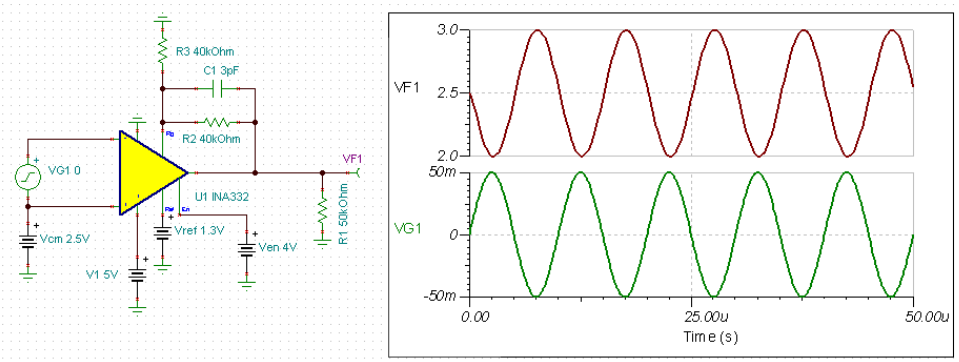

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References

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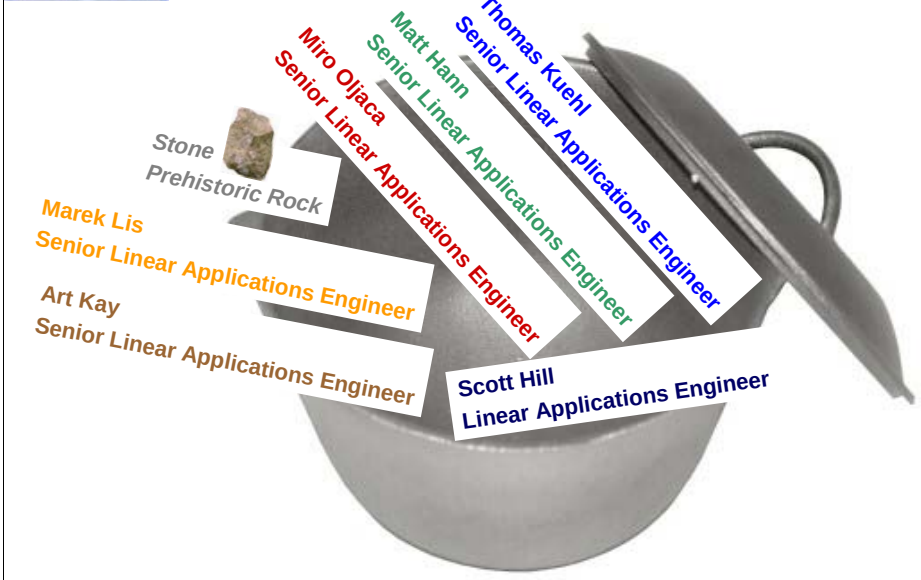

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