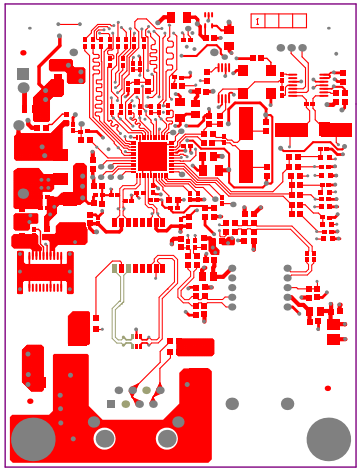
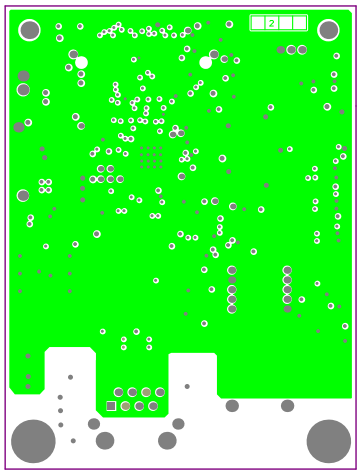
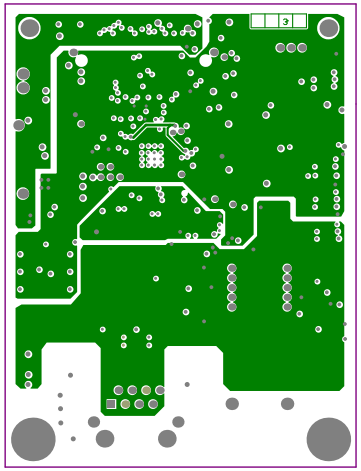


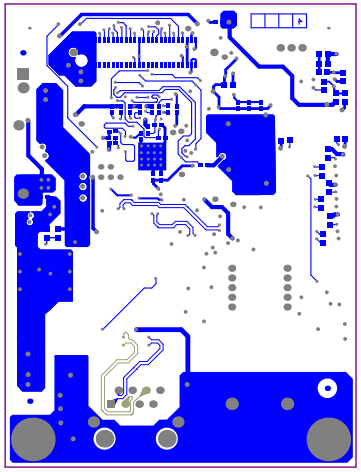
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SVN REV: Not In VersionControl
LAYER NAME = Top Layer			
PLOT NAME = Top Layer	GENERATED : 9/23/2015 9:49:05 AM		TEXAS INSTRUMENTS



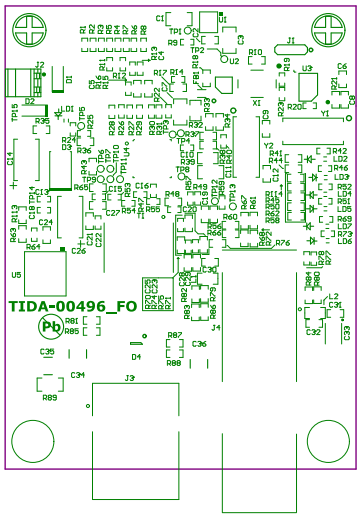
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_FO	REV: E1	SVN REV: Not In VersionControl
LAYER NAME = L2_PI			
PLOT NAME = L2_PI	GENERATED : 9/23/2015 9:49:06 AM		TEXAS INSTRUMENTS



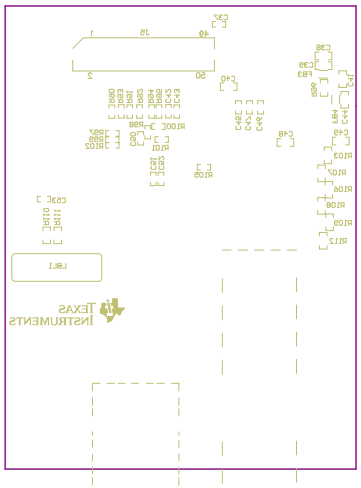
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SVN REV: Not In VersionControl
LAYER NAME = L3_P2			
PLOT NAME = L3_P2	GENERATED : 9/23/2015 9:49:06 AM		TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SVN REV: Not In VersionControl
LAYER NAME = Bottom Layer			
PLOT NAME = Bottom Layer	GENERATED : 9/23/2015 9:49:06 AM		TEXAS INSTRUMENTS

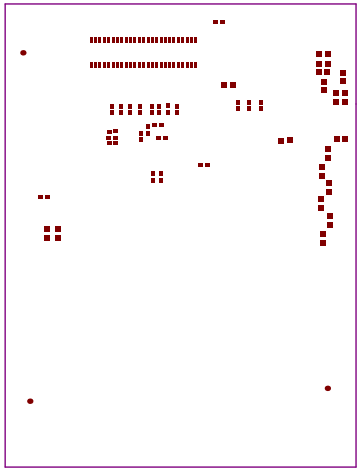


ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_FO	REV: E1	SVN REV: Not In VersionControl	
LAYER NAME = Top Overlay				
PLOT NAME = Top Silkscreen Overlay	GENERATED : 9/23/2015 9:49:06 AM			TEXAS INSTRUMENTS

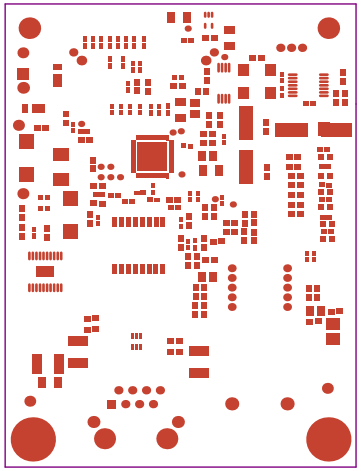


ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SVN REV: Not In VersionControl	
LAYER NAME = Bottom Overlay				
PLOT NAME = Bottom Silkscreen Overlay	GENERATED : 9/23/2015 9:49:06 AM			TEXAS INSTRUMENTS

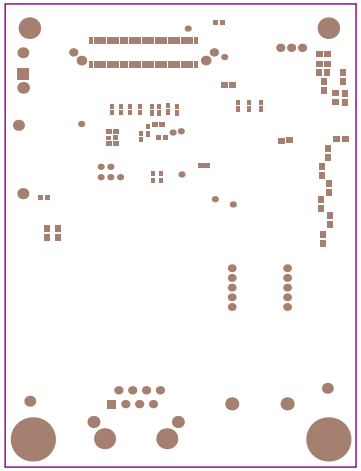
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SVN REV: Not In VersionControl
LAYER NAME = Top Paste			
PLOT NAME = Top Paste Mask Print	GENERATED : 9/23/2015 9:49:07 AM		TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SVN REV: Not In VersionControl
LAYER NAME = Bottom Paste			
PLOT NAME = Bottom Paste Mask Print	GENERATED : 9/23/2015 9:49:07 AM		TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SVN REV: Not In VersionControl
LAYER NAME = Top Solder Mask			
PLOT NAME = Top Solder Mask Print	GENERATED : 9/23/2015 9:49:07 AM		TEXAS INSTRUMENTS



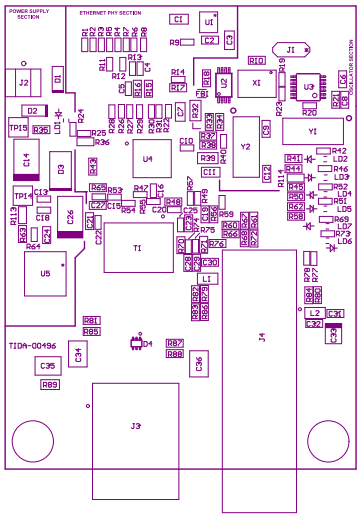
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SVN REV: Not In VersionControl
LAYER NAME = Bottom Solder Mask			
PLOT NAME = Bottom Solder Mask Print	GENERATED : 9/23/2015 9:49:07 AM		TEXAS INSTRUMENTS

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



ASSEMBLY VARIANT:

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

[No Variations]

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SVN REV: Not In VersionControl	
LAYER NAME : ASSEMBLY TOP				
PLOT NAME = M5 Assembly Top	GENERATED : 9/23/2015 9:49:08 AM			TEXAS INSTRUMENTS

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB VIEWED FROM BOTTOM SIDE			
LAYER NAME : ASSEMBLY BOTTOM			
PLOT NAME = M6 Assembly Bottom	GENERATED : 3/23/2018 8:43:08 AM	BOARD #: TIDA-00496_F0 REV: E1	SVN REV: Not In VersionControl
			TEXAS INSTRUMENTS

Layer Stack Up Detail for: TIDA-00496_F0.PcbDoc

Layer Name	Gerber Document	Copper Thickness	Dielectric Material
Top Solder Mask	(.GTS)		Solder Resist
Top Layer	(.GTL)	1.4mil	
L2_P1	(.G1)	1.4mil	FR-408
L3_P2	(.G2)	1.4mil	FR-408
Bottom Layer	(.GBL)	1.4mil	FR-408
Bottom Solder Mask	(.GBS)		Solder Resist

IMPEDANCE TABLE

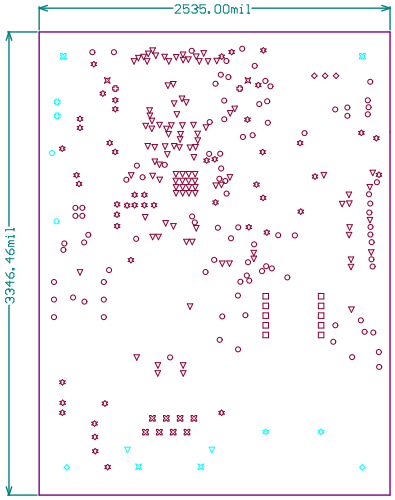
LAYER	TRACE WIDTH	SPACING	IMPEDANCE	REFERENCE LAYER
TOP	7 MIL	16 MIL	100 OHM +/-10%	L2_P1
BOTTOM	7 MIL	16 MIL	100 OHM +/-10%	L3_P2

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
2535.00mil X 3346.46mil

Number of Layers : 4
MIN. TRACK WIDTH: 7 MIL
MIN. CLEARANCE: 7.8 MIL
MIN. VIA PAD SIZE: 26 MIL
MINIMUM ANNULAR RING 0.177mm (7MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
IT IS IMPENDANCE CONTROLLED BOARD

MATERIAL:
[X] FR-408 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 63 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
COPPER THICKNESS (FINISHED):
OUTER: [X] 1.4MIL (1oz) [ ] 2MIL (1.4oz) [ ] 2.8MIL (2oz)
INNER SIGNAL: [X] 1.4MIL (1oz) [ ] 2.8MIL (2oz) [ ] N/A
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR:
[X] GREEN [ ] BLUE [ ] OTHER
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER MECH LAYER 1
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES VIA TENTING: [ ] NONE [X] REQUIRED
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK



Symbol	Hit Count	Tool Size	Plated	Hole Type
▽	107	12mil (0.305mm)	PTH	Round
○	96	16mil (0.406mm)	PTH	Round
✲	49	20mil (0.508mm)	PTH	Round
□	10	31.89mil (0.81mm)	PTH	Round
◇	3	32mil (0.813mm)	PTH	Round
✖	2	33mil (0.839mm)	PTH	Round
⊠	8	35.039mil (0.89mm)	PTH	Round
○	2	40mil (1.016mm)	PTH	Round
◇	2	44mil (1.118mm)	PTH	Round
✲	2	55.118mil (1.4mm)	PTH	Round
○	2	57.087mil (1.45mm)	NPTH	Round
▽	2	62.205mil (1.58mm)	PTH	Round
◇	2	125.984mil (3.2mm)	PTH	Round
✖	2	127.953mil (3.25mm)	NPTH	Round
⊠	2	128mil (3.251mm)	NPTH	Round
	291 Total			

Drill Table

DRILL TOLERANCES:
FOR PTH : +/-3MILS
FOR NPTH : +/-2MILS
FOR 12MIL DRILL VIA : +0/-12MILS
FOR 16MIL DRILL VIA : +0/-16MILS

TEXAS INSTRUMENTS

PROJECT TITLE: IEEE1588 ethernet Brick_Fiber
DESIGNED FOR: Public Release
FILE NAME: TIDA-00496_F0.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SUN REV: Not In VersionControl	
LAYER NAME = Drill Drawing				
PLOT NAME = Drill Drawing For (Bottom Layer,Top Layer)	GENERATED : 9/23/2015 9:49:08 AM			TEXAS INSTRUMENTS

ENGINEER: Srinivas Kallikuppa	LAYOUT BY: Avinash N
SCALE: 1.00	ALTIUM DESIGNER VERSION: 14.3.14.34663