Beyond Quality—Assuring the Reliability of Plastic Encapsulated Integrated Circuits

Uplifting and upscreening commercial components to extended temperatures is a dangerous practice that can adversely affect reliability and maintainability. Instead, look closely at the IC manufacturer’s fabrication, assembly and qualification process, policies and procedures.

Military and commercial advanced COTS (Commercial Off-The-Shelf) ICs are designed for military use requiring uprating or upscreening, depending on the application. The purpose for this discussion, uprating or upscreening, is defined as use beyond the environment and application for which the part was identified.

Upgrading or upscreening, on the other hand, is defined as performing additional testing and applying acceptance to use beyond product data sheet conditions. Other applications such as ground-based communication systems, are more lenient and COTS components may be suitable for use without additional qualification or screening.

Upgrading and upscreening are problematic at best. Very few, if any, IC manufacturers will support this effort, and few upscreening test facilities have the ability to test complex parts. The actual qualification of upscreening has the potential to become component specific. For example, there is the possibility of yield loss and developer inconsistency. In these cases, an electrical overview and catastrophic electrostatic charge removal damage can be observed in these same conditions.

As part of upgrading and upscreening, JEDEC standards rely on device level qualification and testing to ensure delivered product meets the needs of the OEM. While a good start, such practices are not in and of themselves adequate to ensure long-term reliability in harsh environments.

Even when the semiconductor manufacturer performs additional qualification and screening for operation beyond standard temperatures, it only provides a means to facilitate—not replace—JEDEC over temperature (OT) data for COTS devices. Instead, defense system designers may still be required to create their own fabrication, assembly and qualification procedures which may require additional operation over extended temperatures.

Figure 3

Multiple factors of COTS components are important. Defects and assembly defects usually occur out of the mainstream markets targeted by most IC manufacturers.

Figure 4

Electromigration: Life versus Junction Temperature. Maintaining the proper junction temperature plays a critical role in body to tip lifetime. 

JEDEC standards rely on device level qualification and testing to ensure delivered product meets the needs of the OEM. While a good start, such practices are not in and of themselves adequate to ensure long-term reliability in harsh environments.

In response to customer needs, Texas Instruments has released the Enhanced Plastic (EP) product family which is designed for use in a wide range of applications and environments that are often out of scope with defense applications (Figure 1). With military and aerospace components often being very benign while other applications and environments are quite problematic, selection of the product type to ensure system reliability can have different requirements.

In the event a proposed change is needed, the change must be communicated to the internal baseline flow. Processing and qualification testing at the wafer fabrication site often provides the best opportunity to establish that technology over an extended temperature range is comfortable. Additional qualification and screening for operation at extended temperatures is not suitable for extended temperature technology.

In the event a proposed change is needed, the change must be communicated to the internal baseline flow. Processing and qualification testing at the wafer fabrication site often provides the best opportunity to establish that technology over an extended temperature range is comfortable. Additional qualification and screening for operation at extended temperatures is not suitable for extended temperature technology.

In the event a proposed change is needed, the change must be communicated to the internal baseline flow. Processing and qualification testing at the wafer fabrication site often provides the best opportunity to establish that technology over an extended temperature range is comfortable. Additional qualification and screening for operation at extended temperatures is not suitable for extended temperature technology.

In the event a proposed change is needed, the change must be communicated to the internal baseline flow. Processing and qualification testing at the wafer fabrication site often provides the best opportunity to establish that technology over an extended temperature range is comfortable. Additional qualification and screening for operation at extended temperatures is not suitable for extended temperature technology.

In the event a proposed change is needed, the change must be communicated to the internal baseline flow. Processing and qualification testing at the wafer fabrication site often provides the best opportunity to establish that technology over an extended temperature range is comfortable. Additional qualification and screening for operation at extended temperatures is not suitable for extended temperature technology.

In the event a proposed change is needed, the change must be communicated to the internal baseline flow. Processing and qualification testing at the wafer fabrication site often provides the best opportunity to establish that technology over an extended temperature range is comfortable. Additional qualification and screening for operation at extended temperatures is not suitable for extended temperature technology.
A careful evaluation of the technology and the device on quality is required to ascertain if a candidate device will be acceptable to the intended applications. A typical design model is developed for a specific technology node with a device model defined to meet the expected reliability goals. These goals are typically set to meet the expectations of the customer. This model defines a specific set of maximum design conditions required to meet the reliability goals. When a device is in use the actual temperature will be above the ambient temperature. The amount of degradation that occurs will depend on the temperature of use and the actual usage conditions.

Table 2

<table>
<thead>
<tr>
<th>Test Condition</th>
<th>Sample Size</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bias Life Test</td>
<td>1 lot/reactor/run</td>
<td>1 wafer/week</td>
</tr>
<tr>
<td>Autoclave</td>
<td>1 lot/reactor/run</td>
<td>1 wafer/week</td>
</tr>
<tr>
<td>Biased Humidity</td>
<td>1 lot/reactor/run</td>
<td>1 wafer/deposition system</td>
</tr>
</tbody>
</table>

Package Level Reliability

Package related monitors are typically performed to well-established standards by the complexity of the technology and major customers. For periodic electric testing is usually performed to the standard at 25°C. Table 2 is a typical new package qualification program performed to JEDEC standards. After qualification, periodic monitors are typically performed to address customer requirements. Sample sizes and actual testing performed are derived based upon total volume of production and the quality of the assembly process in place. Monitor sample sizes are determined as monitors. Sample sizes and actual testing performed are subject to change.

Table 3

<table>
<thead>
<tr>
<th>Test Condition</th>
<th>Sample Size</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bias Life Test</td>
<td>1 lot/reactor/run</td>
<td>1 wafer/week</td>
</tr>
<tr>
<td>Autoclave</td>
<td>1 lot/reactor/run</td>
<td>1 wafer/week</td>
</tr>
<tr>
<td>Biased Humidity</td>
<td>1 lot/reactor/run</td>
<td>1 wafer/deposition system</td>
</tr>
</tbody>
</table>

Package Materials Design Considerations

Dielectric properties in metal oxide semiconductors. Multiple factors dictate the flow properties during the package itself. Multiple factors dictate the flow properties during the package itself. Multiple factors dictate the flow properties during the package itself. Multiple factors dictate the flow properties during the package itself. Multiple factors dictate the flow properties during the package itself.