Radiation Test Report

SMV512K32HFG 16M SRAM

Introduction: Texas Instruments standard commercial process was modified by SST to produce more robust performance in radiation environments. To validate, a 16M SRAM was manufactured with the two different CMOS process's at Texas Instruments' (TI's) DMOS5 wafer fabrication facility in Dallas, Texas. The wafer lot used one mask set (16M SRAM), generating wafers with and without SST's HardSIL™ enhancement to TI's 180nm C05 process. All wafers were processed in the fabrication line at the same time and in the same lot box with split differences only occurring for wafers manufactured with HardSIL™. There were no flow differences between the 16M SRAM manufactured with the commercial process and the HardSIL™ modified process used in the following radiation test results. Once assembled and tested, a random sample of packaged parts from both control and HardSIL™ processes were tested for:

- Dose-rate (DR),
- Total ionizing dose (TID)
- Single-event effects (SEL, SEU).

Dose-Rate Test: Testing was performed using the Flash X-ray system at the Air Force Research Laboratory, Space Vehicles Directorate on Kirtland AFB, NM. Dose Rate testing protocol consisted of:

1. Writing a memory pattern into the SRAM (without error correction EDAC prior to irradiation),
2. Placing the SRAM in standby mode.
3. Irradiating the part with flash X-Rays of various dose rates ranging from 1e8 to 1e10.
4. After each dose rate event the memory pattern was read to confirm if upset error occurred.
5. Photo currents were recorded each time.
6. No external resistors, capacitors or other modification were added to the SRAM package or test board.
7. Testing was repeated with the same memory pattern until a single bit upset was observed and was noted as the dose rate upset threshold.

After irradiation the data stored in the SRAM was examined for evidence of bit errors, the standby current was measured for evidence of latch-up, and the photocurrent trace from a P-I-N diode was recorded. The number of upset bits, the addresses of the bit upsets, and the standby currents were all recorded as well. At the end of testing, a part was de-lidded so dosimeters could be placed directly on top of the chip before replacing the lid. The part was then inserted into the test board and irradiated while the P-I-N diode recorded the radiation induced photocurrent. The resulting data was used to establish a set of correlation curves which were then used to determine actual dose-rate for each test run from the measured PIN diode photocurrent data. The results are shown below in figure 1.

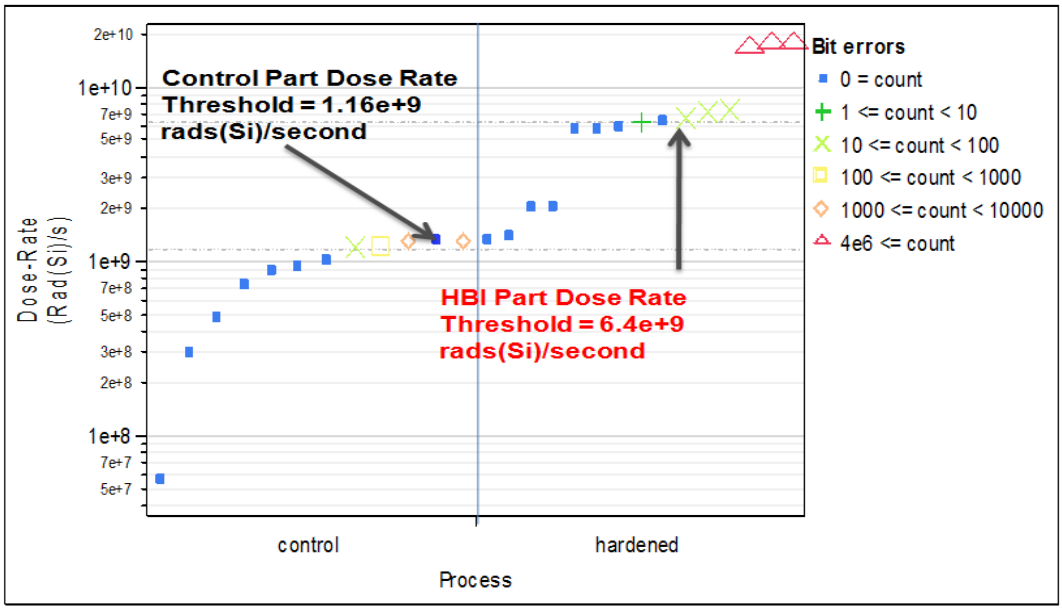

Figure 1: Bit Fails vs. Dose-Rate for control and hardened DUT

Total Ionizing Dose Test: Testing was performed using the Cobalt 60 gamma-ray source at the Air Force Research Laboratory, Space Vehicles Directorate on Kirtland AFB, NM. Four test boards were designed and fabricated that could each hold 4 DUT's (16M SRAMS). Each DUT could be addressed individually by the tester. The four test boards were populated with four parts, and the positions of each part were noted to associate the data with the correct device. The four boards were carefully arranged around the gamma source so that each DUT was equi-distant from the source and would receive the same dose. The slant range for each part was calculated and the dose rate of 82 rads(Si)/s was obtained using a calibrated software package (WINDOSE) provided by AFRL personnel. Testing protocol consisted of

- Writing a checker-board (CB) pattern into the SRAM prior to irradiation.
- Placing the SRAM in standby with both EDAC and scrub disabled (off) to prevent repair of any TID generated bit errors.
- Irradiating the part to pre-determined TID dose levels which were typically (50K, 100K 300K, 500K 750K and 1M rad-sil).

Irradiation was performed using a dose-rate of 83rad(Si)/s to predetermined total ionizing dose (TID) levels. After the predetermined doses were achieved, irradiation was suspended and the DUT was electrically tested to determine the impact of the cumulative TID on the electrical characteristics of the DUT. Testing details of the DUT included:

1) Reading the data stored in the DUT, checking for bit upset errors
2) Measurement of the standby current of the DUT at:
   a) Irradiation CB data pattern with EDAC & Scrub off for both bias pattern and inverse bias pattern.
   b) After writing the inverse of the CB pattern (CB Bar) with the EDAC & Scrub off, and again with the EDAC on & Scrub @ 156 KHz.
3) Measurement of the write current
4) Measurement of the read current

Once the testing of the DUT was completed, irradiation was resumed until the next predetermined TID level was achieved. The electrical test time between irradiation for each DUT was kept under 20 minutes. Figure 2 contains the

DUT standby vs. TID curves respectively for the Pat and Pat* patterns stored in the array. The parts were tested at each TID dose level and repeated until the final TID levels reached.

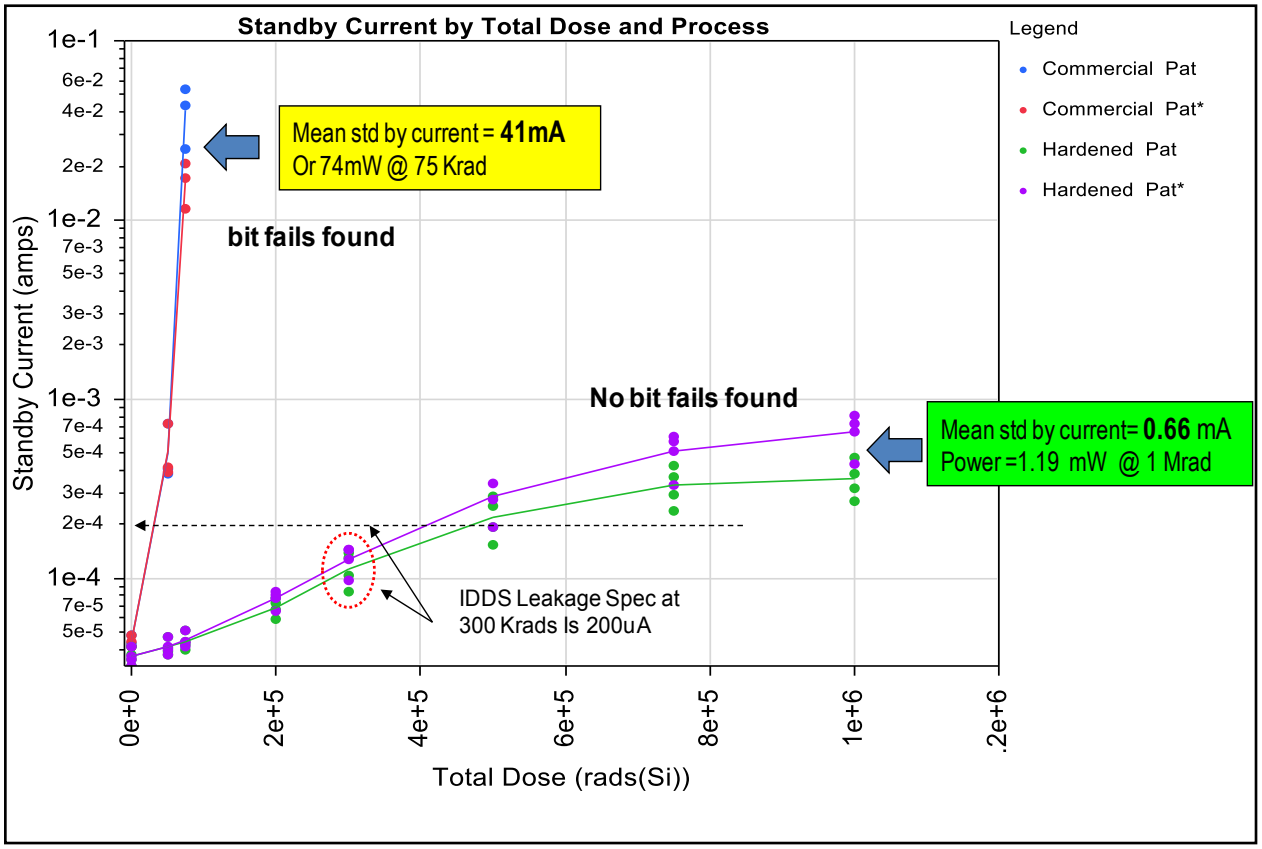

Figure 2: Pat and Pat* standby current w/o scrub vs. TID for control and hardened DUTs

Heavy Ion Single Event Effect (SEE) Test: Testing was performed using the 88-inch cyclotron at Lawrence Berkeley National Laboratory (LBNL) in CA. A single DUT board was used for the heavy ion testing. The DUT package was de-lidded prior to SEU testing to allow for penetration of the heavy ion beam into the DUT. The following tests were performed on the DUT's at various LET/flux/fluence combinations:

1) Static Upset, CB
   a) EDAC & SCRUB disabled
      i) V_{DD1}= 1.6V and 1.8V, incident beam (normal to the surface)
      ii) V_{DD1}= 1.8V, 30° from incident beam, X-axis
      iii) V_{DD1}= 1.8V, 30° from incident beam, Y-axis
   b) EDAC enabled & SCRUB disabled
      i) V_{DD1}= 1.8V, incident beam
      ii) V_{DD1}= 1.6V, incident beam

2) Static Upset, All Ones, EDAC & SCRUB disabled, 1.8V, incident beam

3) Dynamic Upset, continuous Write/Read CB then Write/Read CB BAR patterns, EDAC & SCRUB disabled

The bit error counts for each test were recorded and the resulting data was used to generate SEU cross-section vs. LET response curves for the various test conditions and for each process split. The resulting SEU cross-section vs. LET

response curves were then fitted to a Weibull curve with a nonlinear regression algorithm. The cross sections vs. LET for native, EDAC enabled, and scrub enabled for a static checkerboard pattern are shown in figure 3. A scrub rate of 111 kHz was used in this test. From the figure it can be seen that the used of EDAC and scrub greatly reduces the soft error rate.

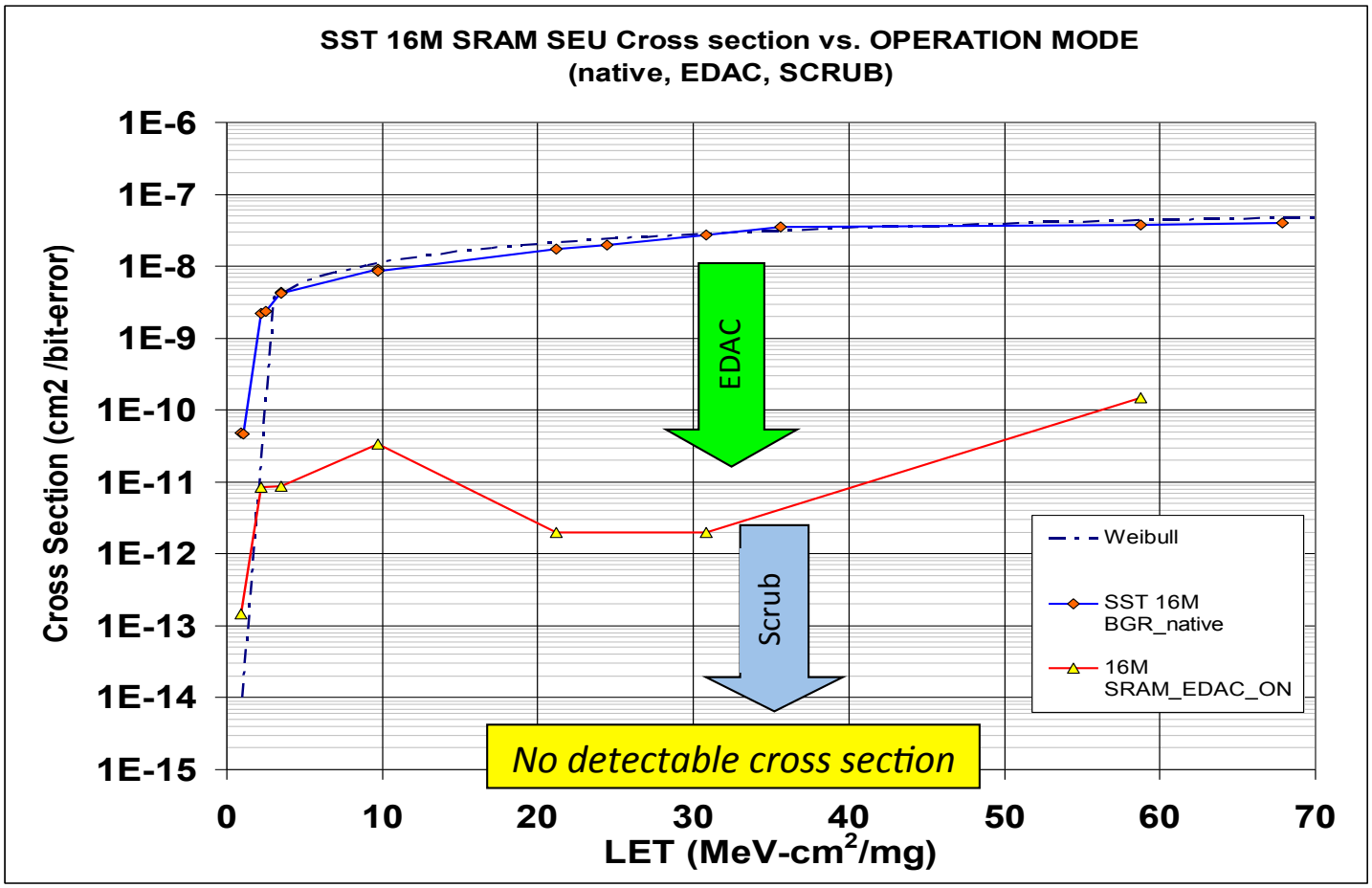

Figure 3: Static CB (EDAC & SCRUB disabled) SEU Cross-Section/Bit vs. LET

Heavy Ion Testing: High Angle of Incidence: The purpose of this test was to determine the parasitic charge spreading response for the SST's 16M SRAM, fabricated to high angle single particle strikes in the control and hardened processes. The SRAM was exposed to the ion beam at two orientations, "against the well" (vertical or 0°) and "along the well" (horizontal or 90°) to characterize die orientation effect and determine the spacial extend of parasitic charge spreading out from a single particle strike. The angle of beam incidence was measured with respect to the Z-axis of the SRAM, with 0° being defined as normal incidence. To avoid the chance of multiple strikes within a micro region of the memory array the beam particle flux was reduced as low as possible to approximately < 10-20 particles/sec-cm2, so the charge spreading from a single particle strike could be observed. The test program was set up to write a pattern to the SRAM before the ion beam was turned on. After the ion beam was activated (on), the program would read the SRAM address space until the first error was found. Once an error was found, the program would log the total memory bit upset error patterns and bit addresses to a file after which the program would re-write a new start pattern to repeat the read / error sense cycle again. After approximately 200 error events at various particle ion angles (0 to 82 deg) and die orientations, the ion beam would then be turned off and the error log would be stored. The run log that was maintained during testing contained all specific information concerning a given test run such as ion, LET, beam flux, beam fluence, bit upset map.. etc. A low value for flux was chosen for each run of the experiment to result in about one read cycle per second.. After the data were collected, the row and column locations of each failure were identified. A custom C program was written to identify and catalog the various MBU shapes. Using the bit map information along with the SRAM bit-cell size the length and width of the

bounding boxes were calculated in microns. A "bounding box" is defined as the largest box in dx and dy that can contained 98% the failing bits associated with a given SEU→MBU. Figures 4 and 5 show an example of these plots for "along the well" and "against the well" with an incident angle of 80°.

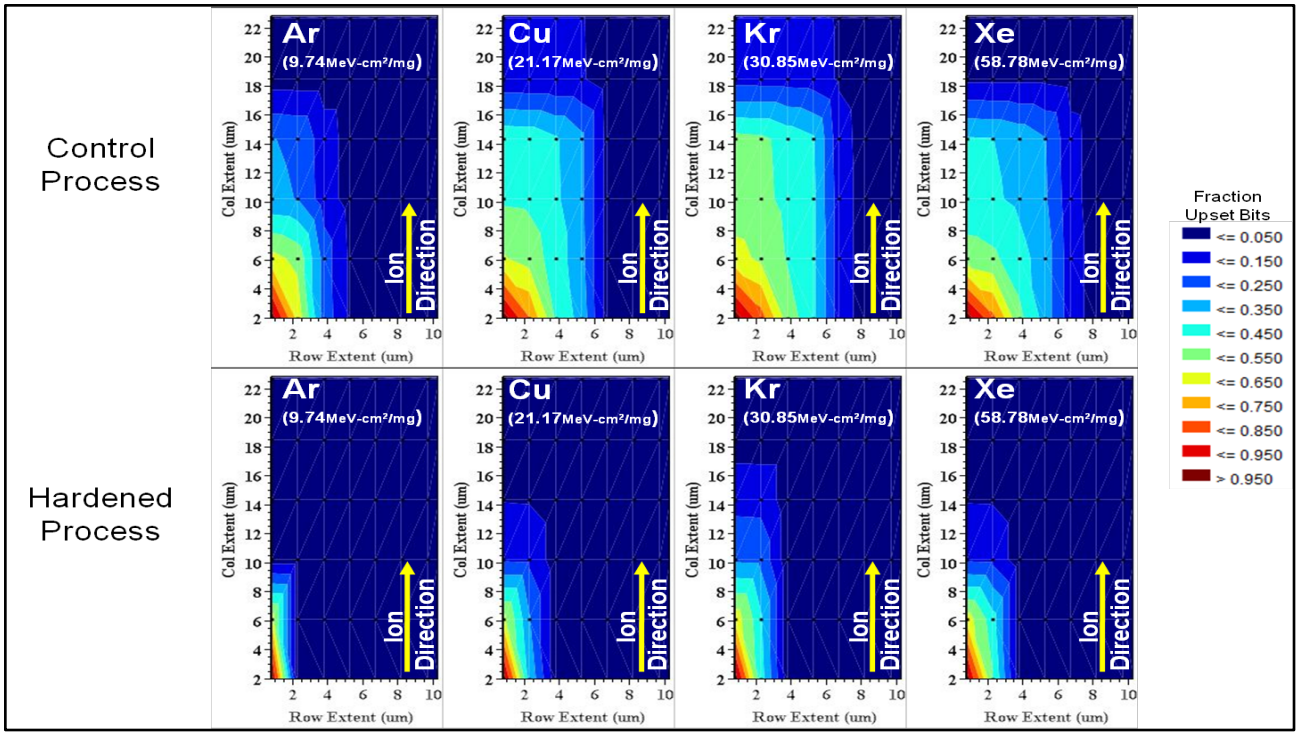

Figure 4: Above plot shows bounding box contour plots for 80° ion incidence against wells.

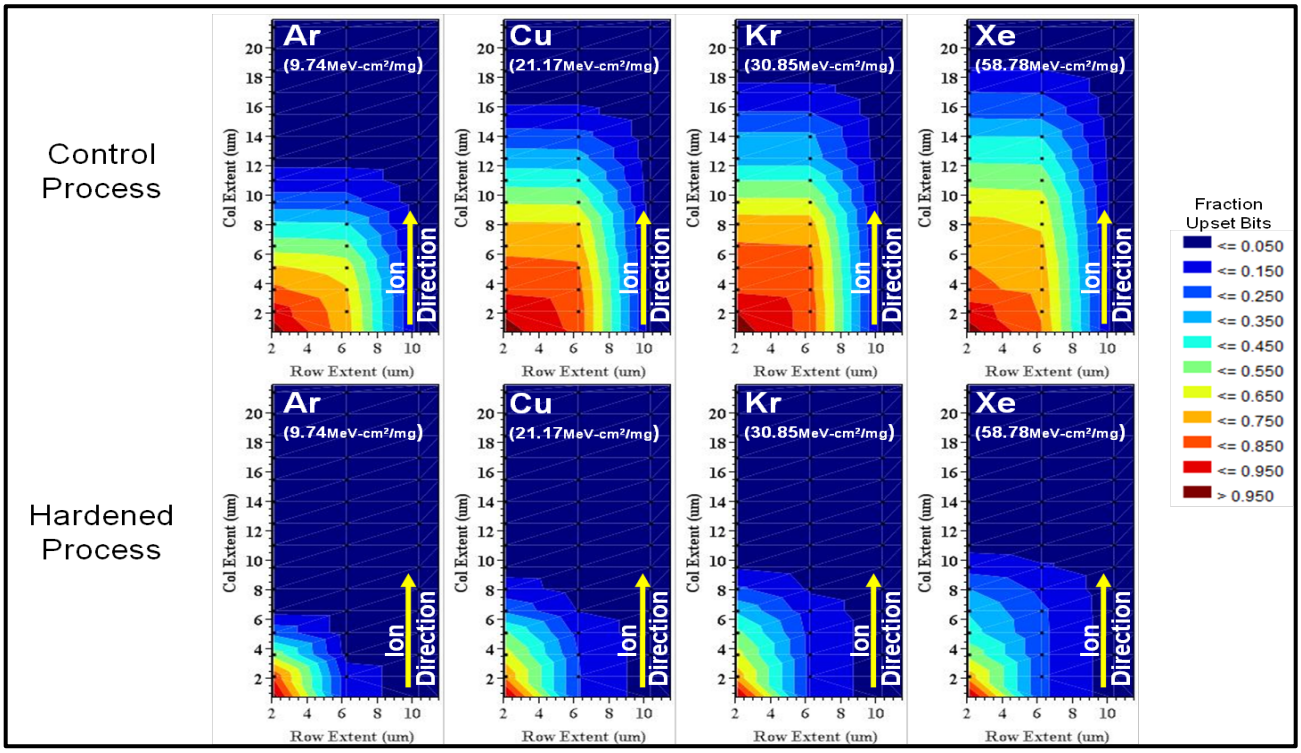

Figure 5: Bounding box contour plots for 80° ion incidence along wells.

The boxes for the ***length*** (in the direction of the ion strike) shown above are significantly less (>half the size) for the hardened process compared to the control process in both the "against wells" and "along wells" cases. While the boxes for the ***width*** are also significantly reduced (less than half the size) for the hardened process compared to the control process in the "against wells" case confirming the improved hardening of the silicon by HardSIL™.

Latch-up Testing: Latch-up testing was performed by first writing a checkerboard pattern to the memory. The samples were then heated to either 125 or 150º C and exposed to ions with various particle LET's to a total fluence of $>1x10^7$ ions/cm^2. The 16M SRAM standby current was monitored during irradiation and ***latch-up was noted*** when the standby current ***exceeded 100X*** the pre-radiation value. The samples were tilted to higher angle to increase the LET of various ions and the core power supply was set to an overvoltage condition for Vdd =1.98 volts, which is 10% above the nominal value (1.8V). The results for these tests are shown in figure 6. The control sample showed evidence of latch-up at an LET of 79 MeV cm^2/mg and at a temperature of 125º C. In contrast, the hardened sample showed no evidence of latch-up even up to a temperature of 150º C and at an LET of over 117 MeV cm^2/mg. The hardened sample was then rotated 90º and tested for latch up again. Still no indication of latch-up was observed. These results are shown in figure 6. The chip stand by current as a function of time (during the irradiation) for the 150º C test of the hardened part is shown in the right side of figure 6. The data shows that the current reaches a maximum of slightly over 1 mA while the chip is in overvoltage, @ 150C, and being irradiated by > 1e7 ions and is rock solid stable at these extreme conditions. The SRAM remained functional at this temperature indicating it could be used in high temperature applications. The in line heating unit was not capable of higher temperatures otherwise high temperatures would have been investigated.

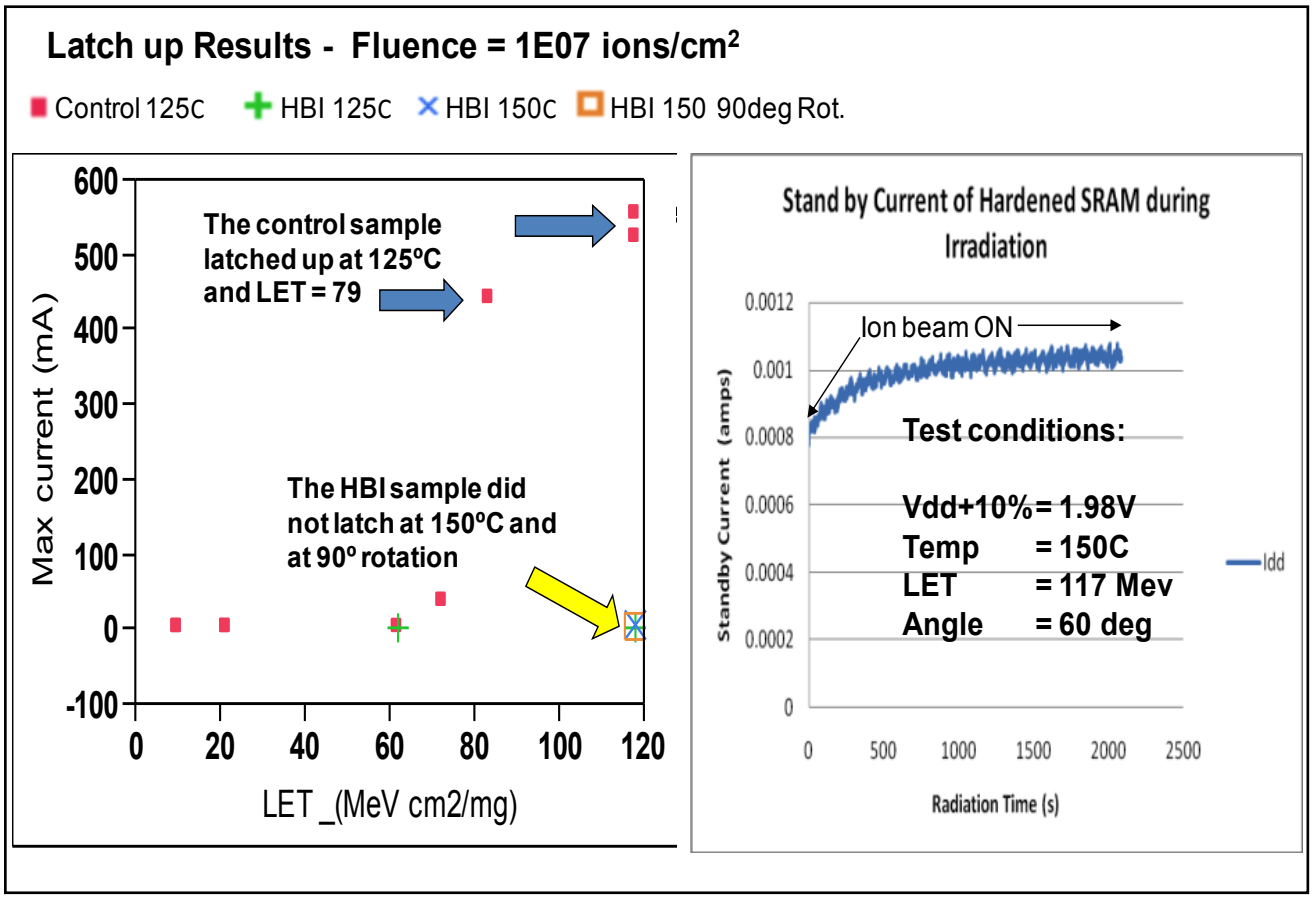

Figure 6: Results from 16M SRAM latch-up testing, control vs. HardSIL™

Final Conclusions:

Texas Instruments and SST has introduced its first RHIC product which is a low power, high performance radiation hardened monolithic single port 16M bit SRAM which has demonstrated robust die yield at first silicon. The TI 16M SRAM features EDAC, variable frequency SCRUB capability, spatial-bit-within-word-separation and its proprietary HardSIL™ techniques. The 16M SRAM has been electrically characterized and radiation tested for both TID and SEE and found to achieve:

1) A high dose-rate threshold of ~6.4e+9 rad(Si)/s
2) Total ionizing dose performance of ~1Mrad(Si) ***with no bit fails and < 1mA post radiation stand-by current.***
3) The SER rate with EDAC and Scrub frequency of 111 KHz is calculated at less than 5e-17 errors/bit-day.
4) SEU elimination with Scrub running in 100% duty cycle for any LET and high angle.
5) HardSIL™ process provides single event latch up immunity to 16M SRAM for any LET at any angle, and confirmed up to 150C while operating at 110% of core voltage, and LET >117 Mev.
6) Regionally uniform suppression of SEU parasitic charge coupling for all LET's, and high angles.
7) Large reduction of large MBU occurrences for SRAMS manufactured with hardened-by-process techniques in contrast to SRAMs manufactured with the commercial process (exact same SRAM design).