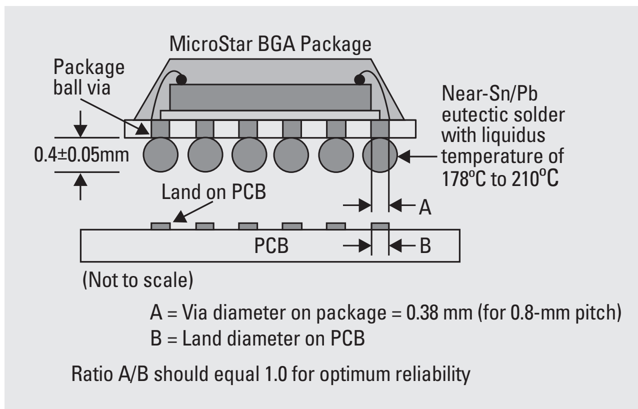
The following information applies to Logic Products "ONLY"

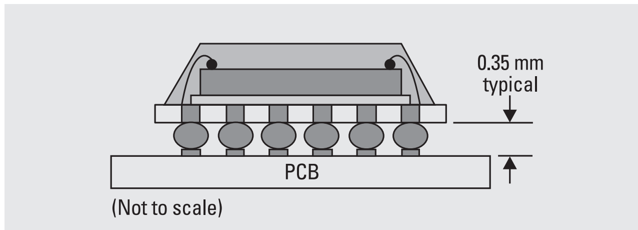
Design Summary for 96GKE/114GKF MicroStar BGA™ Packages

PCB Design Guidelines

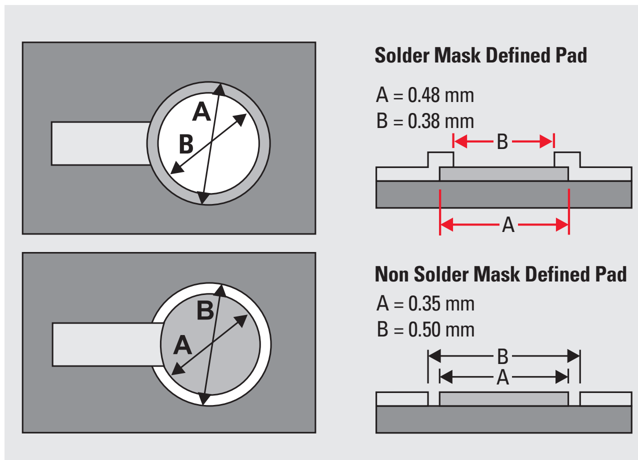
Package Via to Board Land Area Configuration



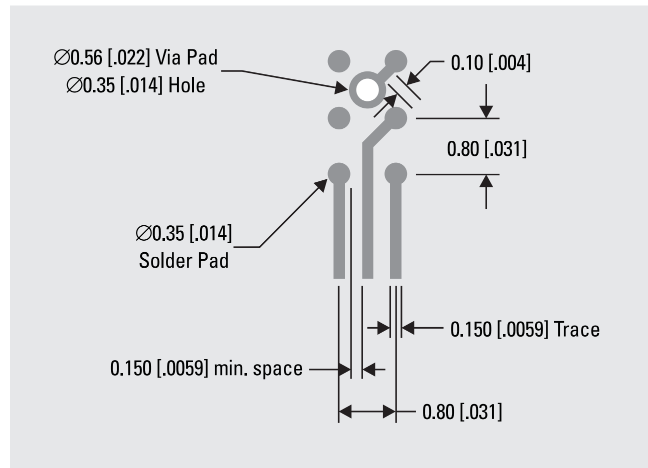
Solder Ball Collapse



LFBGA Recommended Land Pad Design



Trace Width/Spacing Dimensions (mm [in.]) Non-Solder Mask Defined Pad



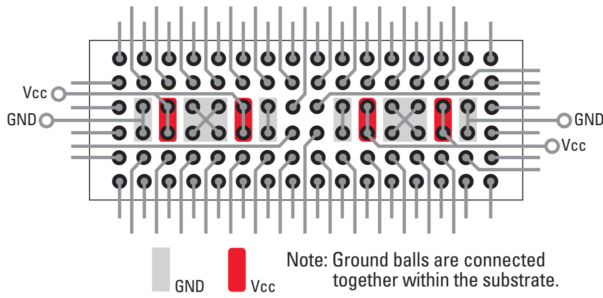
Maximum Via Diameter

	Solder Mask Defined Land Pad	Non-solder Mask Defined Land Pad
Trace width/spacing	0.107 mm (4.2 mil)	0.150 mm (5.9 mil)
Drill bit diameter	0.23 to 0.25 mm (9 to 10 mil)	0.35 to 0.38 mm (14 to 15 mil)
Unplated hole	0.23 to 0.25 mm (9 to 10 mil)	0.35 to 0.38 mm (14 to 15 mil)
Finished via size (plated)	0.178 to 0.2 mm (7 to 8 mil)	0.30 to 0.33 mm (12 to 13 mil)

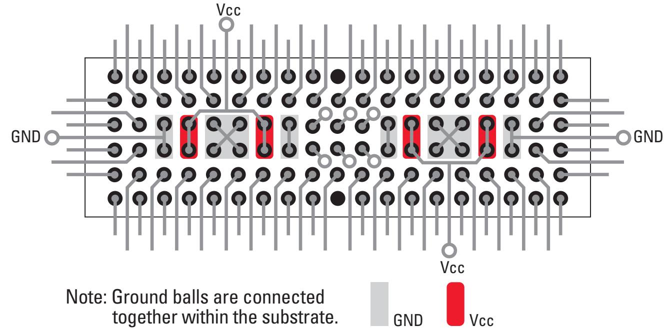
Note: Unplated via diameter assumes a 0.2 mm (8 mil) via land dimension and a 0.1 mm (4 mil) clearance between the via land to the adjacent land pad.

PCB Design Guidelines *(Continued)*

LFBGA-96 Recommended Routing



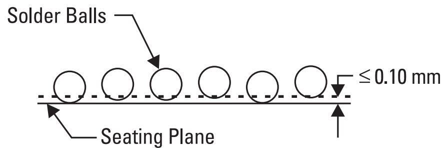
LFBGA-114 Recommended Routing



Geometric Dimensional Tolerances

Coplanarity

This Geometric Dimensioning and Tolerancing (GD & T) term [⌓ | 0.10 mm] means:
This package meets a Coplanarity of 0.10 mm as shown below. Coplanarity is defined as a unilateral tolerance zone measured upward from the seating plane. (Reference ASME Y14.5-1994).



Position Tolerance

This GD & T term [⊕ | ∅ 0.08 Ⓜ] is described below:

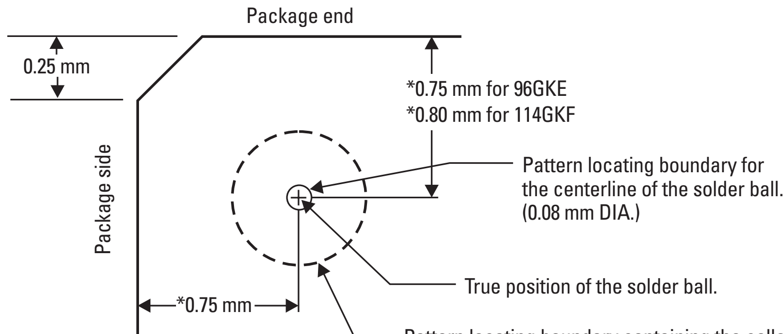
⊕ This is the symbol for True Position. True Position is defined as the theoretically exact centerline location of the solder ball(s).

∅ 0.08 This symbol/number represents how much the centerline of the solder ball(s) is allowed to vary from it's True Position.

Ⓜ This symbol/letter is defined as the maximum material condition of the solder ball(s) which is 0.55 mm DIA.

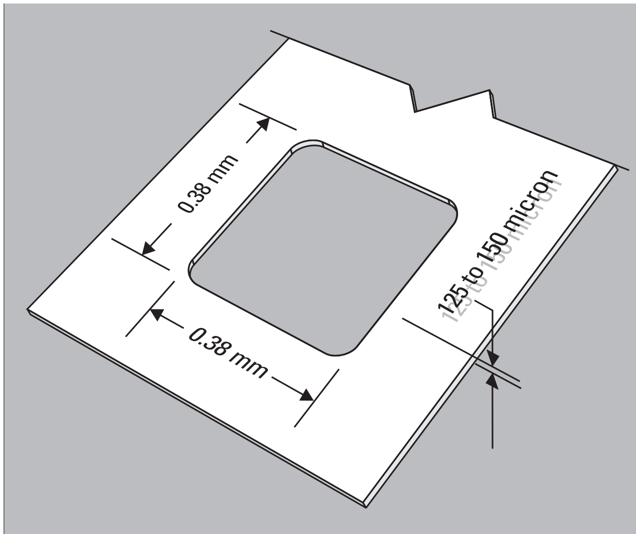
Position Tolerance *(Continued)*

A graphic representation is shown below for the top, left solder ball of this package.



* These 2 dimensions are calculated based on a package with nominal body width and length dimensions.

Stencil Vitals



Solder Paste

TI recommends the use of paste when mounting MicroStar BGAs. The use of paste offers the following advantages:

- It acts as a flux to aid wetting of the solder ball to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.

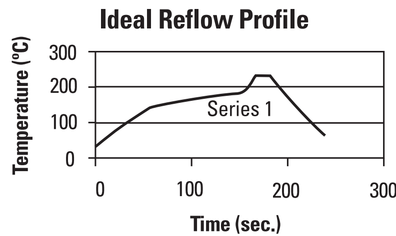
Paste selection is normally driven by overall system assembly requirements. In general, the "no clean" compositions are preferred due to the difficulty in cleaning under the mounted components.

IR Reflow Profile

Ideal (1st and 2nd) Reflow Profile

RT to 140°C: 60 - 90 sec.
140°C to 180°C: 60 - 120 sec.
Time above 183°C: 60 - 150 sec.
Peak Temp.: 220°C ±5°C
Time within 5°C Peak Temp: 10-20 sec.
Ramp down rate: 6°C/sec. Max.

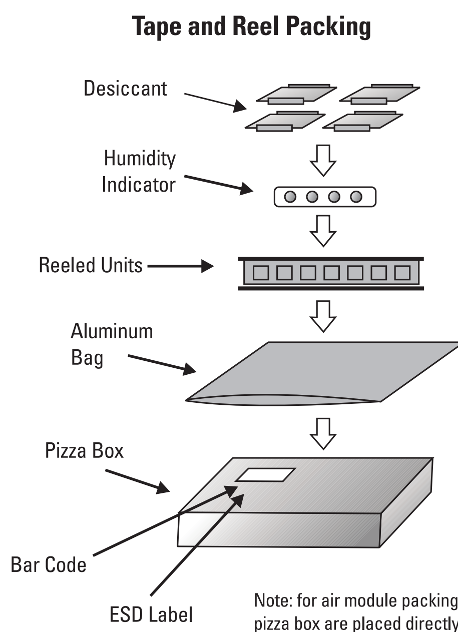
Ideal Reflow Profile



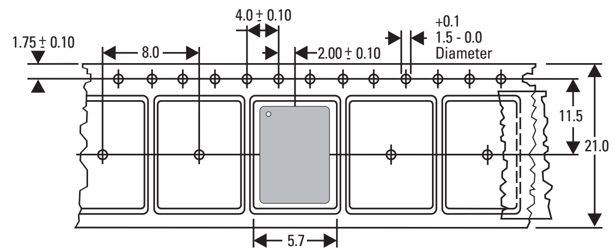
Note:
This is an ideal profile, and actual conditions obtained in any specific reflow oven will vary. This profile is based on convection or RF plus forced convection heating.

Packaging Tape and Reel

Tape and Reel Packing



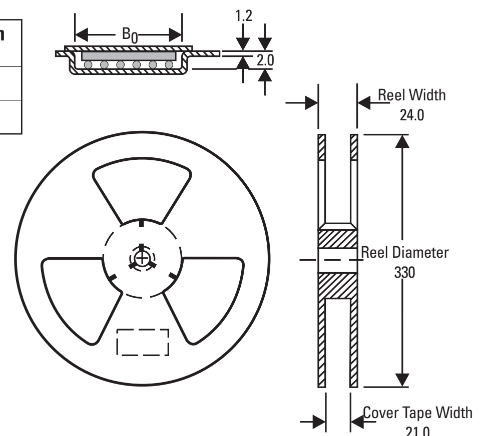
Note: for air module packing pizza box are placed directly.



Package	Pocket Length (B_0)
96GKE	13.7
114GKF	16.2

Quantity per reel = 1,000
Dimensions in millimeters

(Not to scale)



Sockets

Sockets and Socket Manufacturer (Ordering Information)

Yamaichi Socket numbers:	LFBGA-96	PN# IC280-096-144
	LFBGA-114	PN# IC280-114-145

Yamaichi Electronics USA, Inc.
2235 Zanker Road
San Jose, CA 95131
Phone: (408) 456-0797

Questions and Answers

Q. Do the solder balls come off during shipping?

A. No, this has never been observed. The balls are 100 percent inspected for co-planarity, diameter and other physical properties prior to packing for shipment. Because solder is used during the ball attachment process, uniformly high ball attachment strengths are developed. Also, the ball attachment strength is monitored frequently in the assembly process to prevent ball loss from vibration and other shipping forces.

Q. Is package repair possible? Are tools available?

A. Yes, some limited package repair is possible, and there are some semi-auto M/C tools available. However, TI does not guarantee the reliability of repaired packages.

Q. What are the leads that appear on the package edge for? Are they connected to the inner pattern?

A. Those leads are used for plating connections during the plating of Ni/Au on the copper trace during the fabrication of the substrate. Since they do have electrical connection with the inner pattern, they can be used for test probing and signal analysis. There is no reliability risk with them.

Q. What alignment accuracy is possible?

A. Alignment accuracy for the 0.8-mm pitch package is dependent upon board level pad tolerance, placement accuracy, and solder ball position tolerance. Nominal ball position tolerances are specified at ±80 microns. These packages are self-aligning during solder reflow, so final alignment accuracy may be better than placement accuracy.

Q. Can the solder joints be inspected after reflow?

A. Process yields of 5-ppm rejects are typically seen, so no final in-line inspection is required. Some customers are achieving satisfactory results during process set-up with lamographic X-ray techniques.

Q. How do the board assembly yields of MicroStar BGAs compare to QFPs?

A. Many customers are initially concerned about assembly yields. However, once they had MicroStar BGAs in production, most of them report improved process yields compared to QFPs. This is due to the elimination of bent and misoriented leads, the wider terminal pitch than with 0.5-mm pitch QFPs, and the ability of these packages to self-align during reflow. The collapsing solder balls also mean that the coplanarity is improved over leaded components.

Q. Are there specific recommendations for SMT processing?

A. Texas Instruments recommends alignment with the solder balls for the CSP package, although it is possible to use the package outline for alignment. Most customers have found they do not need to change their reflow profile.

Q. Can customers mount MicroStar BGA packages on the bottom side of the PCB board?

A. Yes, they can and the ideal 2nd reflow profile is the same as the 1st (IR profile is recommended in the bulletin). The root causes for solder ball off are:

• Excess amount of solder paste during customers board assembly. TI recommends minimizing the amount of solder paste on the bottom side by using a stencil thickness of 0.15 mm with 0.38-mm aperture opening.

• Moisture absorption also affects the solder ball off issue. Since the package is classified as moisture level 3, the 1st and 2nd reflow have to be completed within a week.

Q. Can the boards be repaired?

A. Yes, there are rework and repair tools and pro-files available. We strongly recommend that removed packages be discarded.

Q. Is TI developing a lead-free version of MicroStar BGAs?

A. Yes, Texas Instruments is working toward eliminating lead in the solder balls to comply with lead-free environmental policies. The lead-free solder is in final evaluation. Only the solder will change, not the package structure or the mechanical dimensions. The solder system under development is based on Sn-Ag metallurgy. Check with your local TI Field Sales representative for sample availability.

Q. What size land diameter for these packages should I design on my board?

A. Land size is the key to board-level reliability, and Texas Instruments strongly recommends following the design rules included in this bulletin.

Q. Where can the decoupling capacitors go for the LFBGA package?

A. The recommended capacitance value and number of capacitors for decoupling is a 0.1 mF capacitor for each VCC on the LFBGA package. The decoupling capacitors should be connected as close as possible to the GROUND and VCC planes.

Q. Any EMI concerns for traces under the package and how can customers design their board to minimize EMI?

A. EMI can be controlled by minimizing any complex current loops on the PCB trace. Some helpful hints include:

• Solid ground and power planes be used in the design. Partitioned ground and power planes must be avoided. These ground and power partitions may create complex current loops increasing radiation.

• Avoid right angles or "T" crosses on the trace. Right angles can cause impedance mismatch and increase trace capacitance causing signal degradation.

• Minimize power supply loops by keeping power and ground traces parallel and adjancent to each other. Significant package EMI can be reduced by using this method.

• Use decoupling capacitors as described in the previous question.

References

Recommended References:

1. *MicroStar BGA Packaging Reference Guide* — SSYZ015
2. *96 and 114 ball LFBGA Application Note* — IDT, Philips Semiconductor and Texas Instruments
3. *Board Level Reliability Evaluations of 40, 32 and 30 Mil Pitch Bal Grid Array Packages Over -40 to 125°C* — Puligandla Viswanadham, Steve Dunford and Ted Carper, Circuit Card Assemblies Center of Excellence Raytheon Systems Co.
4. *Comprehensive User's Guide for µBGA*Packages* — www.intel.com/design/flcomp/packdata/297846.htm
5. *Solder Paste Printing Guidelines for BGA and CSP Assemblies* — Donald C. Burr, published in SMT January 1999.
6. *Maintaining BGA Reliability During Rework* — Stuart Downes and Robert Farrell, published in SMT January 1999.
7. *BGA Rework Considerations* — Jennie S. Hwang, published in SMT November 1998.

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