Quad Flatpack No-Lead Logic Packages

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ABSTRACT

Texas Instruments Quad Flatpack No-lead (QFN) 14/16/20-terminal Pb-free plastic packages meet dimensions specified in JEDEC standard MO-220, allow for board miniaturization, and hold several advantages over traditional SOIC, SSOP, TSSOP, and TVSOP packages. The packages are physically smaller, have a smaller routing area, improved thermal performance, and improved electrical parasitics, while giving customers a pinout scheme that is consistent with the previously mentioned packages. Additionally, the absence of external leads eliminates bent-lead concerns and issues. These QFN packages have reliable solderability with either SnPb or Pb-free solder paste, and are packaged to industry-standard tape-and-reel specifications. Package marking is in accordance with TI standards.

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1 Introduction

As worldwide mobility increases, consumers wanting to "stay connected" in the digital world have demanded smaller and lighter products. Consumer-electronics manufacturers, for the most part, are striving to reduce product size to meet this demand. Smaller, thinner, and thermally enhanced packages help achieve product miniaturization. A performance analysis has shown that quad flatpack no-lead (QFN) packages have better thermal performance than µ*BGA Jr., and TSSOP packages for low pin counts. Other benefits of the QFN packages are low inductance and capacitance, small package volume, smaller board routing area, and no external leads compared to TSSOP like packages. Texas Instruments has chosen QFN as one of the vehicles that allows electronic-component manufacturers to achieve product miniaturization.

14-, 16-, and 20-pin QFN packages will be offered in many logic or linear product families, as defined in Section 1.1, *Product Offerings*. This package is ideal for space-constrained products such as cellular, DVD/CD players, MP3 players, VCRs, Digital STB, DSC, notebook computers, PC cards, and personal digital assistants (PDAs). These packages also are best suited for products with increased thermal and electrical requirements.

The QFN packages are depopulated, and dimensionally align with JEDEC standard MO-220,[1] The package construction allows the pinout to remain consistent with current SOIC, SSOP, TSSOP, and TVSOP packages. Package features, characteristics, and performance are defined in this application report.

1.1 Product Offerings

Table 1 shows the product families to be offered initially in 14-, 16-, and 20-pin QFN packages. Available functions are too numerous to list. Additionally, based on customer demand, the product-family list is expected to grow. Please check the TI website at www.ti.com for the latest list of product families and functions.

Table 1. Product Technology Families for 14-, 16-, and 20-Pin QFN Packages

Family	Description	Pins
ABT	Advanced BiCMOS Technology	14, 20
AHC/T	Advanced High-Speed CMOS	14, 16
ALVC	Advanced Low-Voltage CMOS Technology	14
CBT	Crossbar Technology	14, 16, 20
CBTLV	Low-Voltage Crossbar Technology	14, 16, 20
GTLP	Gunning-Transceiver Logic Plus	16
LV	Low-Voltage HCMOS Technology	14, 16, 20
LVC	Low-Voltage CMOS Technology	14, 16, 20
LVT	Low-Voltage BiCMOS Technology	14, 20

2 Industry Requirements

2.1 Industry Requirements

The consumer-electronics industry is focused on product miniaturization as a result of consumer demands for smaller and better-performing products. To attain smaller products, electronic manufacturers require smaller packages (area and height) to reduce board size and product volume and weight. Package volume and weight are extremely important because consumers desire electronic products that do not inhibit mobility. Product performance comes from three areas: increased functions, increased heat dissipation, and improved electrical parasitics. The number of functions can be increased because packages are smaller and more packages can be added to the board. This is more so if the product volume is not decreased and the existing board is maximized with packages. Heat dissipation is important because the package with the best thermal dissipation typically can run at faster speeds. Last, packages with better electrical parasitics generally have lower signal noise. This is important because high-end processors require logic devices for stable, clean, signal output. All of this becomes complicated by the fact that consumers do not want to pay more for new technology. Thus, manufacturers must develop processes that do not increase cost significantly. This is a challenge because smaller packages often need new, more-accurate equipment for processing. Texas Instruments has selected the QFN package to address these industry requirements and is helping define industry-standard design requirements for QFN.

3 Physical Description

3.1 Package Characteristics

Figure 1 shows a cross section of a generic QFN package.

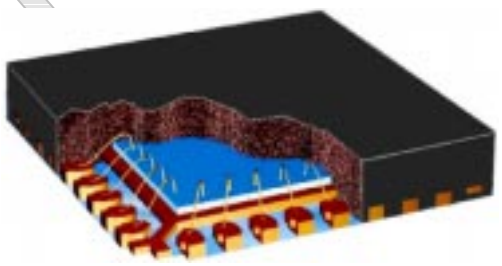


Figure 1. Cross Section of a Generic QFN Package

Table 2 summarizes the package attributes for the 14-, 16-, and 20-pin QFN packages.

Table 2. QFN Package Physical Attributes

Attribute	14QFN	16QFN	20QFN
Pin Count	14	16	20
Square/Rectangular	Square	Rectangular	Rectangular
Package Length (mm) nominal	3.5	4.0	4.5
Package Width (mm) nominal	3.5	3.5	3.5
Lead Finger Length (mm) nominal	0.4	0.4	0.4
Lead Finger Width (mm) nominal	0.23	0.23	0.23
Exposed Pad Length (mm) max.	2.15	2.65	3.15
Exposed Pad Width (mm) max.	2.15	2.15	2.15
Thickness (mm) nominal	0.90	0.90	0.90
Package Weight (g)	0.032	0.036	0.043
Lead Finish	Matte Tin	Matte Tin	Matte Tin
Shipping Media, Tape and Reel (units)	1000	1000	1000

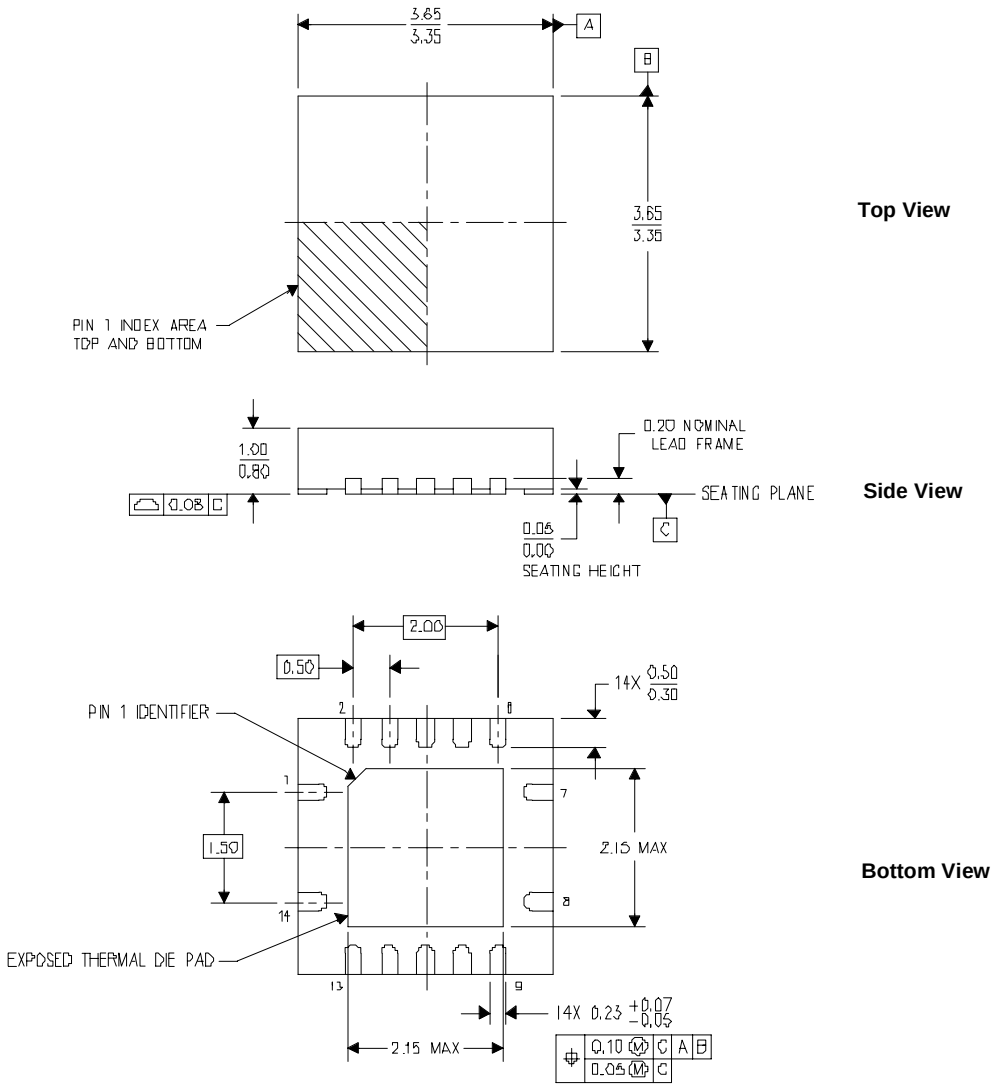


Figure 2. 14-Pin QFN Package Dimensions

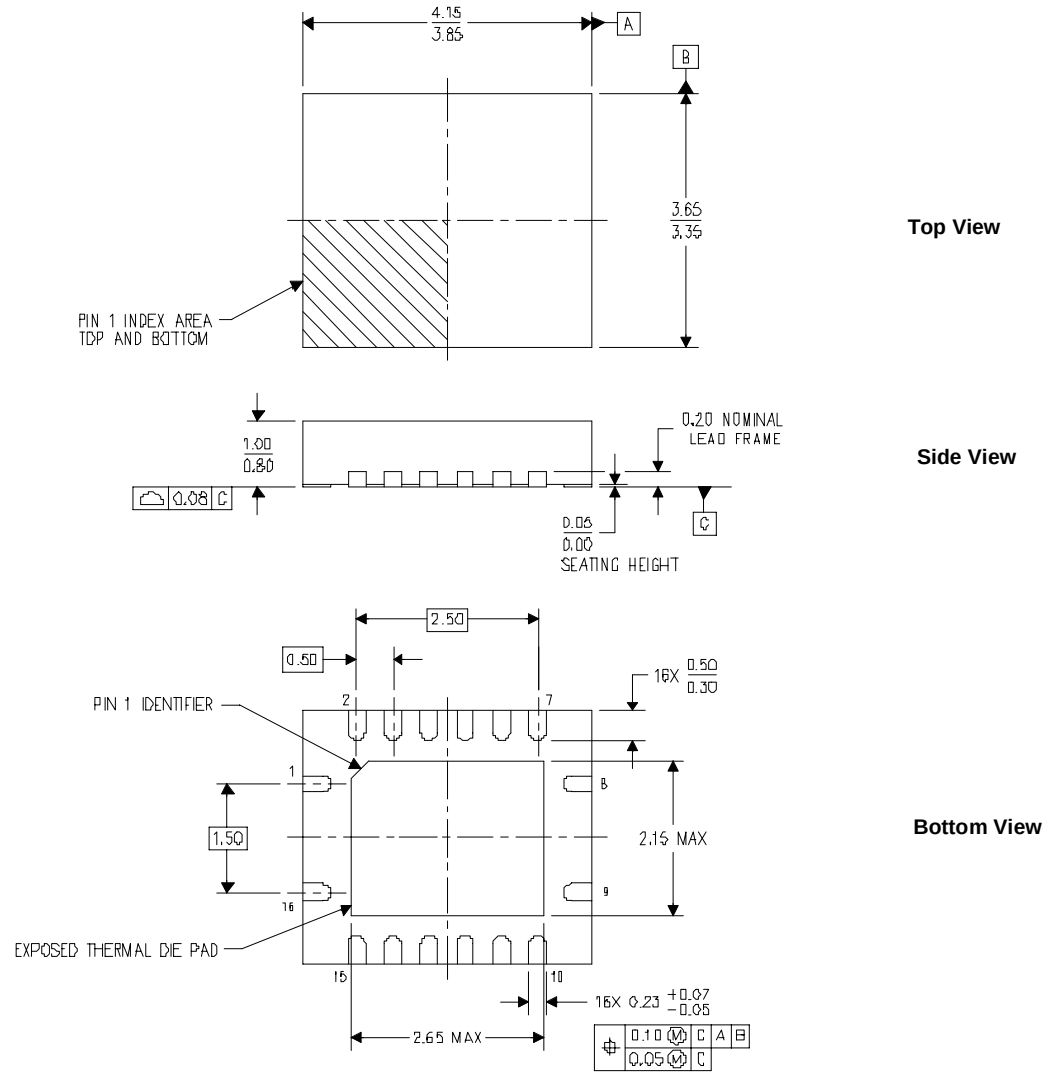


Figure 3. 16-Pin QFN Package Dimensions

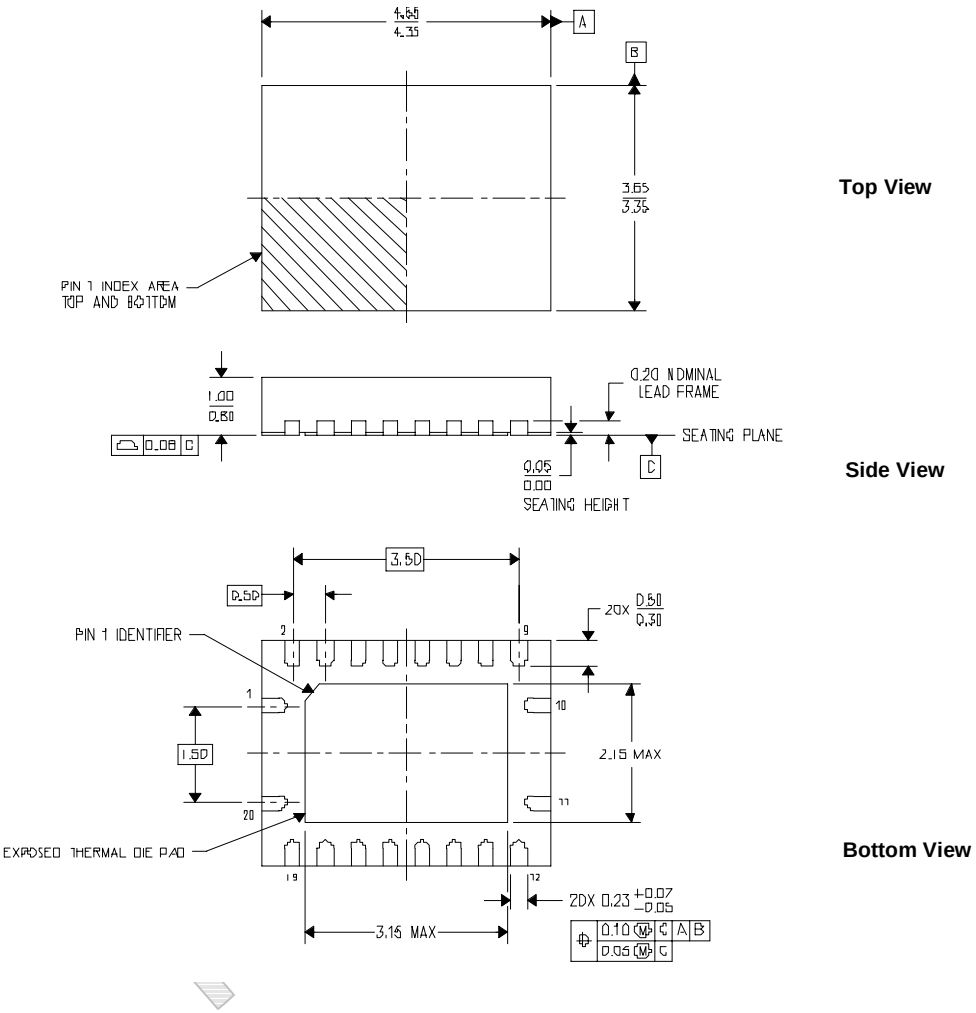
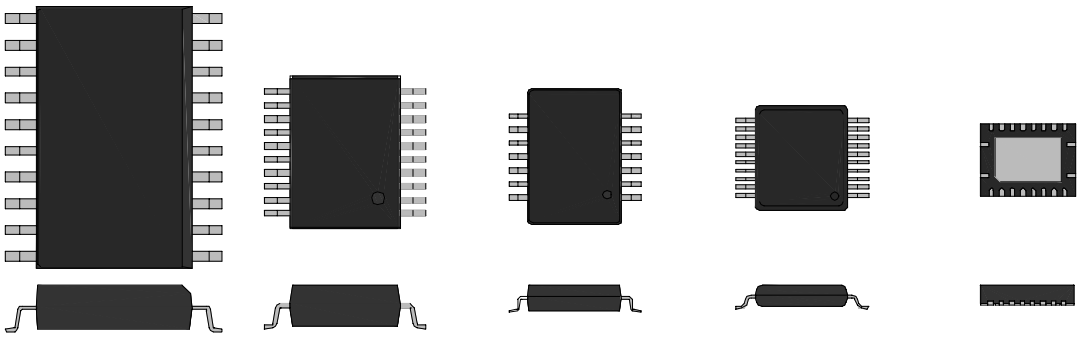


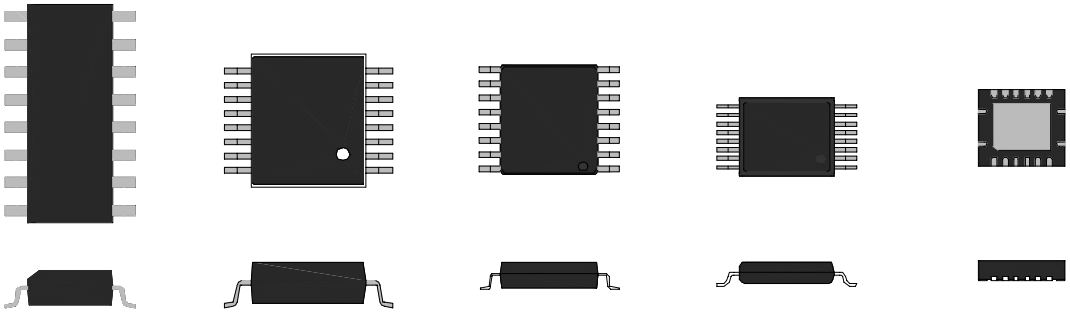
Figure 4. 20-Pin QFN Package Dimensions

Figures 5 through 7 compare the QFN package size, height, and weight to that of alternative package solutions.



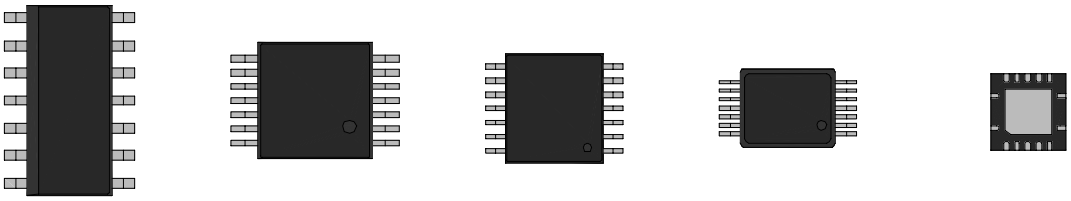
Attribute	SOIC-20 (DW)	SSOP-20 (DB)	TSSOP-20 (PW)	TVSOP-20 (DGV)	QFN-20 (RGY)
Length, mm	12.82 ± 0.13	7.20 ± 0.30	6.50 ± 0.10	5.00 ± 0.10	4.5 ± 0.15
Width, mm	10.40 ± 0.25	7.80 ± 0.40	6.40 ± 0.20	6.40 ± 0.20	3.50 ± 0.15
Height, Max. mm	2.65	2.00	1.20	1.20	1.00
Pitch, mm	0.50	0.50	0.50	0.40	0.50
Footprint, mm^2	133.33	56.16	41.60	32.00	15.75
Weight, g	0.495	0.151	0.075	0.055	0.043
Area Savings %	88.19	71.96	62.14	50.78	-

Figure 5. 20-Pin QFN Comparison to Alternative Package Solutions



Attribute	SOIC-16 (D)	SSOP-16 (DB)	TSSOP-16 (PW)	TVSOP-16 (DGV)	QFN-16 (RGY)
Length, mm	9.90 ± 0.10	6.20 ± 0.30	5.00 ± 0.10	3.60 ± 0.10	4.00 ± 0.15
Width, mm	6.00 ± 0.20	7.80 ± 0.40	6.40 ± 0.20	6.40 ± 0.20	3.50 ± 0.15
Height, Max. mm	1.75	2.00	1.20	1.20	1.00
Pitch, mm	0.50	0.50	0.50	0.40	0.50
Footprint, mm^2	59.40	48.36	32.00	23.04	14.00
Weight, g	0.150	0.140	0.062	0.040	0.036
Area savings, %	76.43	71.05	56.25	39.24	-

Figure 6. 16-Pin QFN Comparison to Alternative Package Solutions



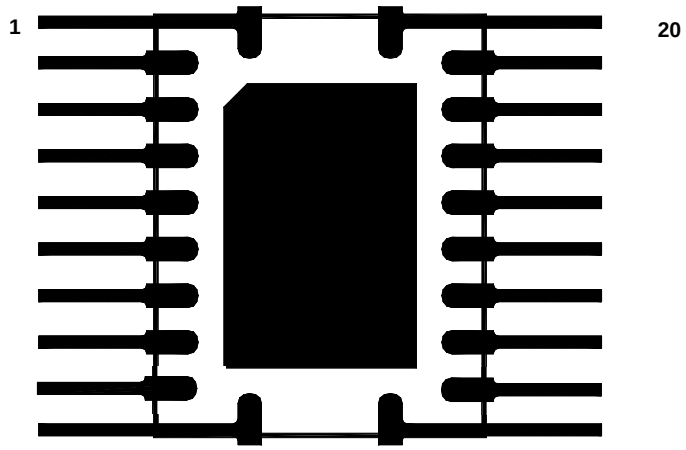
Attribute	SOIC-14 (D)	SSOP-14 (DB)	TSSOP-14 (PW)	TVSOP-14 (DGV)	QFN-14 (RGY)
Length, mm	8.65 ± 0.10	6.20 ± 0.30	5.00 ± 0.10	3.60 ± 0.10	3.50 ± 0.15
Width, mm	6.00 ± 0.20	7.80 ± 0.40	6.40 ± 0.20	6.40 ± 0.20	3.50 ± 0.15
Height, Max. mm	1.75	2.00	1.20	1.20	1.00
Pitch (mm)	0.50	0.50	0.50	0.40	0.50
Footprint (mm^2)	51.90	48.36	32.00	23.04	12.25
Weight, g	0.127	0.122	0.055	0.040	0.032
Area savings, %	76.40	74.67	61.72	46.83	-

Figure 7. 14-Pin QFN Comparison to Alternative Package Solutions

3.2 QFN Pinout

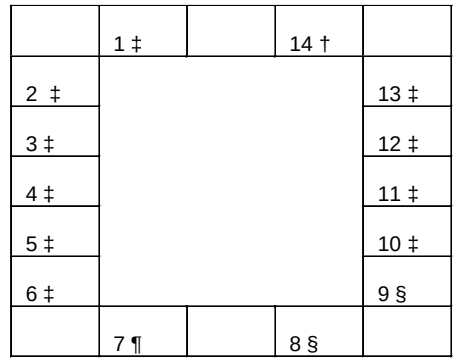
The standard pinout configurations for 14-, 16-, and 20-QFN packages resemble the conventional arrangement of 14-, 16-, and 20-dual in-line packages. Figures 8 through 9 show standard QFN pinouts for 14- and 20-QFN packages. These pinouts are accurate for most devices; however, some functions vary, especially in the 16-pin package. Please refer to the device data sheet to confirm specific pinouts. Note the flow-through design afforded by the package configuration.

	1 §		20 †	
2 ‡				19 §
3 ‡				18 ‡
4 ‡				17 ‡
5 ‡				16 ‡
6 ‡				15 ‡
7 ‡				14 ‡
8 ‡				13 ‡
9 ‡				12 ‡
	10 ¶		11 ‡	



† = Vcc
‡ = I/O and Signal
§ = Control
¶ = Ground
Note A: Schematic is not drawn to scale

Figure 8. 20 Pin QFN Package Standard Pinout



Note A: Schematic is not drawn to scale
† = Vcc
‡ = I/O and Signal
§ = Control
¶ = Ground

Figure 9. 14-Pin QFN Package Standard Pinout

3.3 Package Nomenclature

These packages are generically referred to in this application note as QFN. The Texas Instruments package designator for these 14, 16, and 20-pin QFN packages is RGY. This common designator refers to all these three packages with common width of 3.5mm. The designator is extended to RGYR to represent the parts packed in tape & reel as explained in section 5.

3.4 Power Dissipation

When thermal dissipation is crucial, the QFN package has an advantage over standard dual- and quad-leaded packages. The leadframe die pad is exposed at the bottom of the package and should be soldered to a properly designed thermal pad in the PWB. This provides a more direct heat-sink path from the die to the board, and the addition of thermal vias from the thermal pad to an internal ground plane will dramatically increase power dissipation. Soldering the exposed pad also significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests.

Unless otherwise stated, the following model data assumes that the package has the exposed pad soldered to the thermal pad on the PWB. The thermal effects of intentionally omitting solder from the exposed pad also is shown later in this section for informational purposes. The standards used for these models are available for downloading at http://www.jedec.org/download/default.cfm.[2,3,4] It is highly encouraged that customers familiarize themselves with these standards when comparing the power-dissipation performance of similar or alternative packaging, to ensure the comparison is made on equivalent terms.

It is important to understand that the following data is intended for comparison of the QFN package to alternative packages under similar conditions (the standards mentioned previously). System-level performance is heavily dependent upon board thickness, metal layers, component spacing (thermal coupling), airflow, and board orientation in the system. The model data provided can be further used to construct system-level thermal models to predict performance in any particular system, but does not reflect the package's performance in any system as listed, except in accordance with the standards under which it was modeled.

For the following data, values are given for each standard. All standards use the same land pad and thermal pad design, however they differ in internal board construction. Test cards complying with JESD 51-3 have no internal metal layers, and are, naturally, the worst case in performance. The shorthand reference for this board design is 1S0P; meaning one signal, zero planes. JESD 51-5 has two internal metal layers and thermal vias connecting the upper layer to the thermal pad. These vias are 0.30-mm diameter and are spaced 1.2 mm, center to center. The vias are allowed to populate only the region defined by the perimeter of the thermal pad, and cannot extend beyond the perimeter. This is referred to as 1S2P with vias. JESD 51-7 test cards have the same two metal layers as the JESD 51-5 test card, but no vias are allowed. This is referred to as 1S2P. The standards also allow for a second signal trace on the backside (2S2P or 2S0P), but the backside signal traces make little difference (< 2%) in most cases. These three standards give a wide range of conditions under which alternative packages can be compared.

Table 3. Modeled 20-Pin QFN Thermal-Impedance Values

20-Pin QFN Per JESD 51-5 (1S2P Direct Attach Method)			
Airflow, LFM	**Θ_{JA} (C/W)**	**Θ_{JC} (C/W)**	**Θ_{JB} (C/W)**
0	37.31	21.35	19.00
150	35.47		
250	34.66		
500	33.58		

20-Pin QFN Per JESD 51-7 (1S2P)			
Airflow, LFM	**Θ_{JA} (C/W)**	**Θ_{JC} (C/W)**	**Θ_{JB} (C/W)**
0	87.36	34.58	56.07
150	85.33		
250	84.68		
500	82.38		

20 Pin QFN Per JESD 51-3 (1S0P)		
Airflow, LFM	**Θ_{JA} (C/W)**	**Θ_{JC} (C/W)**
0	161.08	40.56
150	148.28	
250	144.40	
500	131.69	

NOTE: Θ_{JB} is neither applicable nor defined for JESD 51-3 test cards.

Table 4. Modeled 16-Pin QFN Thermal-Impedance Values

16-Pin QFN Per JESD 51-5 (1S2P Direct Attach Method)			
Airflow, LFM	**Θ_{JA} (C/W)**	**Θ_{JC} (C/W)**	**Θ_{JB} (C/W)**
0	38.67	22.82	18.93
150	36.84		
250	36.01		
500	34.90		

16-Pin QFN Per JESD 51-7 (1S2P)			
Airflow, LFM	**Θ_{JA} (C/W)**	**Θ_{JC} (C/W)**	**Θ_{JB} (C/W)**
0	89.04	36.99	55.34
150	87.03		
250	85.84		
500	84.08		

16-Pin QFN Per JESD 51-3 (1S0P)		
Airflow, LFM	**Θ_{JA} (C/W)**	**Θ_{JC} (C/W)**
0	166.11	44.11
150	153.03	
250	145.94	
500	136.05	

NOTE: Θ_{JB} is neither applicable nor defined for JESD 51-3 test cards.

Table 5. Modeled 14-Pin QFN Thermal-Impedance Values

14-Pin QFN Per JESD 51-5 (1S2P Direct-Attach Method)			
Airflow, LFM	**Θ_{JC} (C/W)**	**Θ_{JC} (C/W)**	**Θ_{JB} (C/W)**
0	47.29	27.70	25.30
150	45.36		
250	44.51		
500	43.34		

14-Pin QFN Per JESD 51-7 (1S2P)			
Airflow, LFM	**Θ_{JA} (C/W)**	**Θ_{JC} (C/W)**	**Θ_{JB} (C/W)**
0	114.27	47.60	80.01
150	112.36		
250	110.08		
500	108.60		

14-Pin QFN Per JESD 51-3 (1S0P)		
Airflow, LFM	**Θ_{JA} (C/W)**	**Θ_{JC} (C/W)**
0	200.37	55.32
150	185.86	
250	178.22	
500	167.46	

Note: Θ_{JB} is neither applicable nor defined for JESD 51-3 test cards.

Figures 10 through 18 show power dissipation of QFN packages on the JEDEC standard test cards.[2,3,4]. All power-dissipation values assume a junction temperature of 150°C and are modeled.

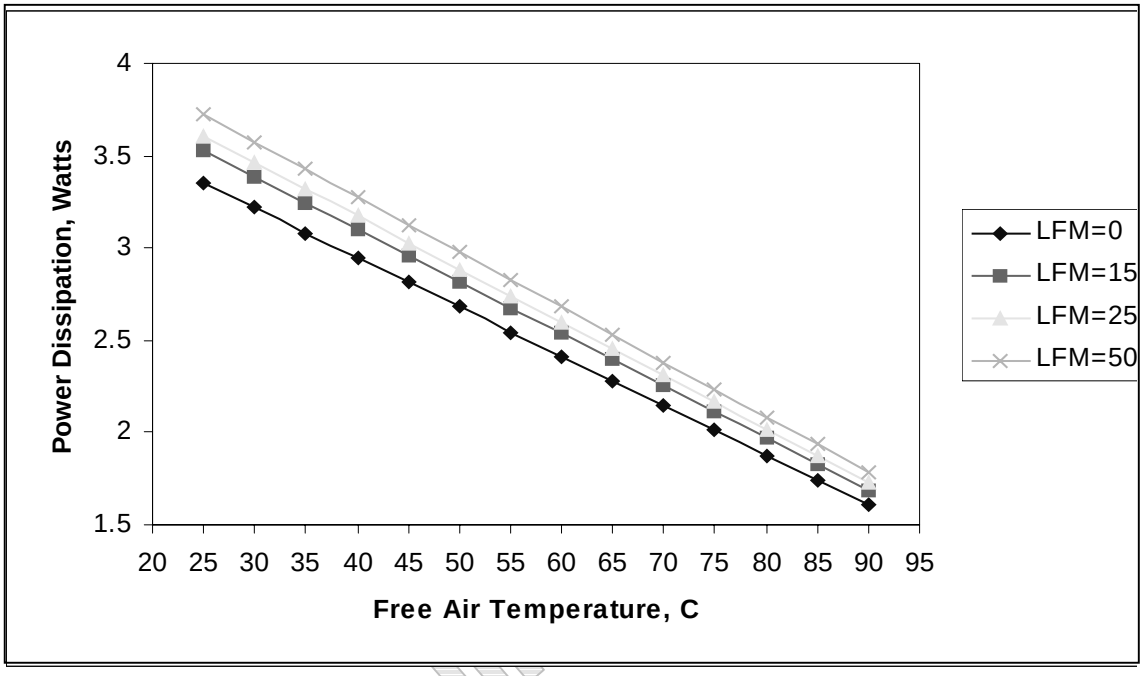


Figure 10. 20-Pin QFN Power Dissipation on JESD 51-5 (1S2P Direct Attach) Test Card

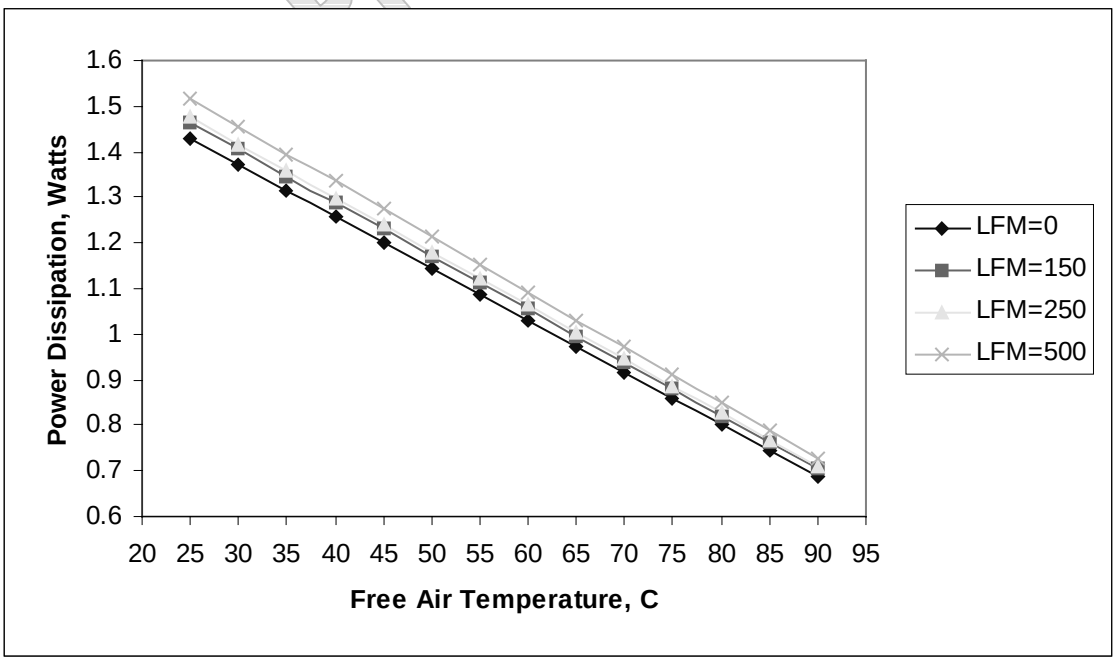


Figure 11. 20-Pin QFN Power Dissipation on JESD 51-7 (1S2P) Test Card

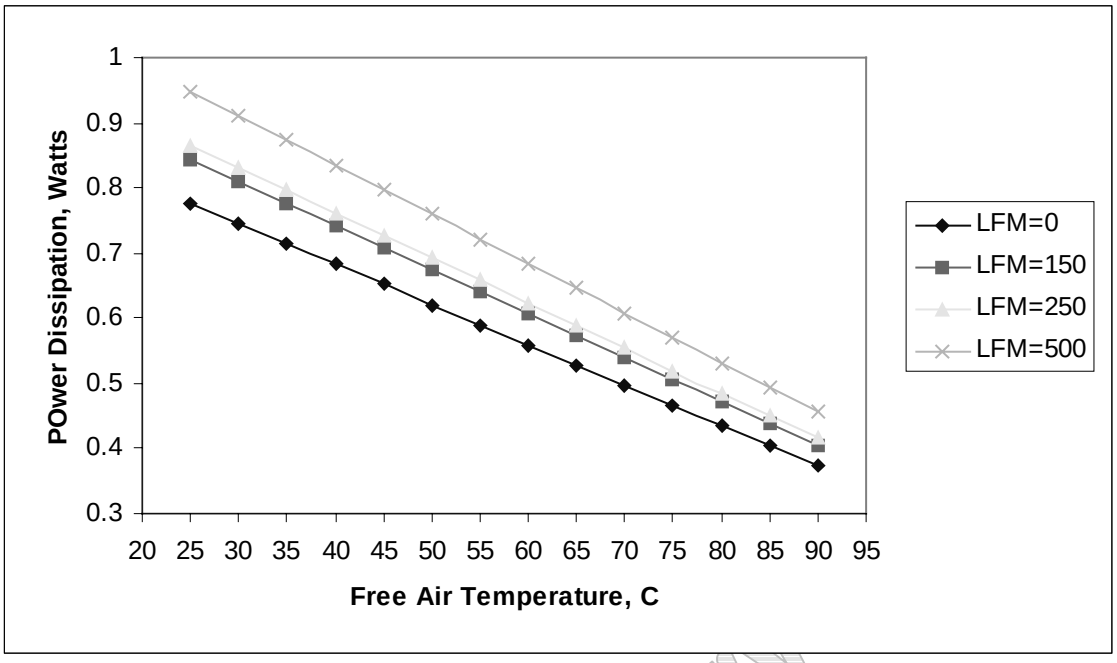


Figure 12. 20-Pin QFN Power Dissipation on JESD 51-3 (1S0P) Test Card

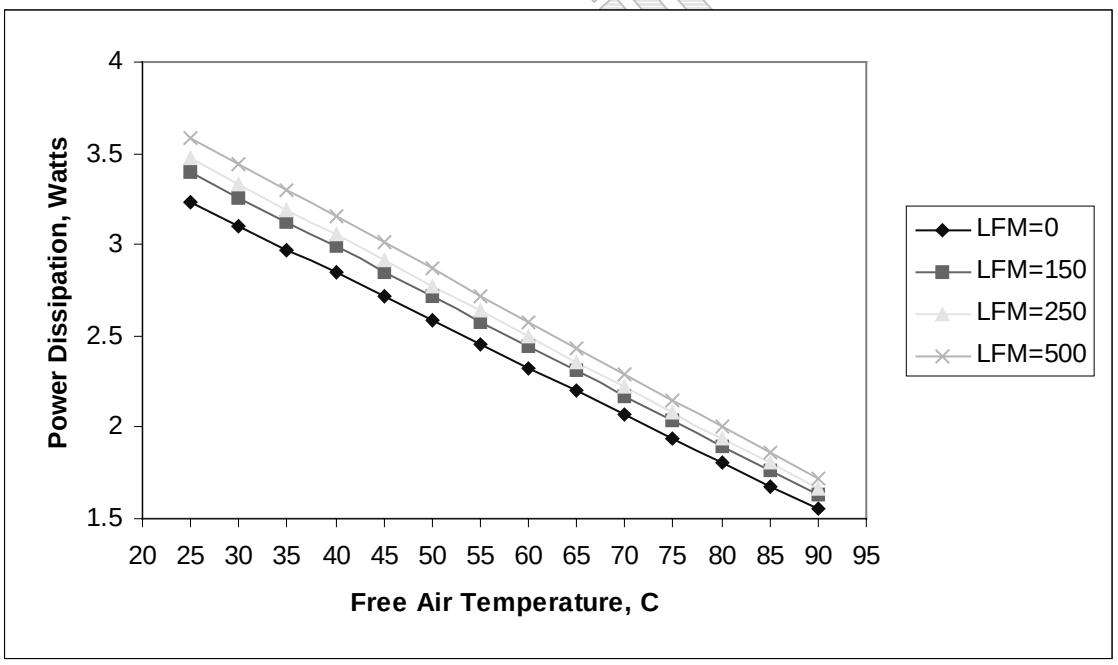


Figure 13. 16-Pin QFN Power Dissipation on JESD 51-5 (1S2P Direct Attach) Test Card

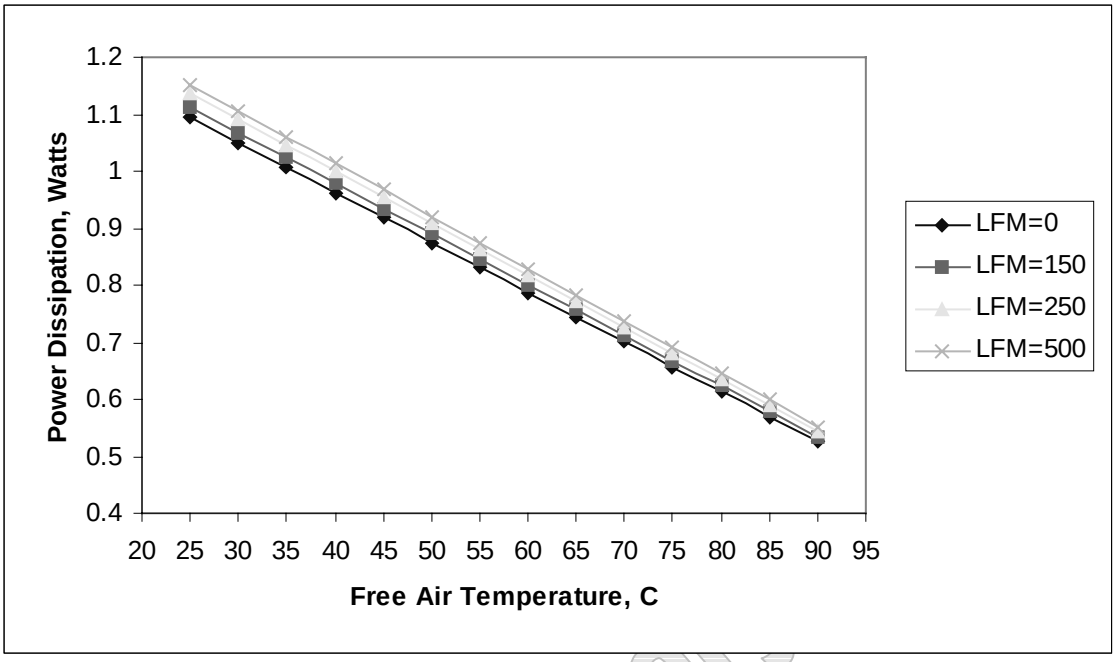


Figure 14. 16-Pin QFN Power Dissipation on JESD 51-7 (1S2P) Test Card

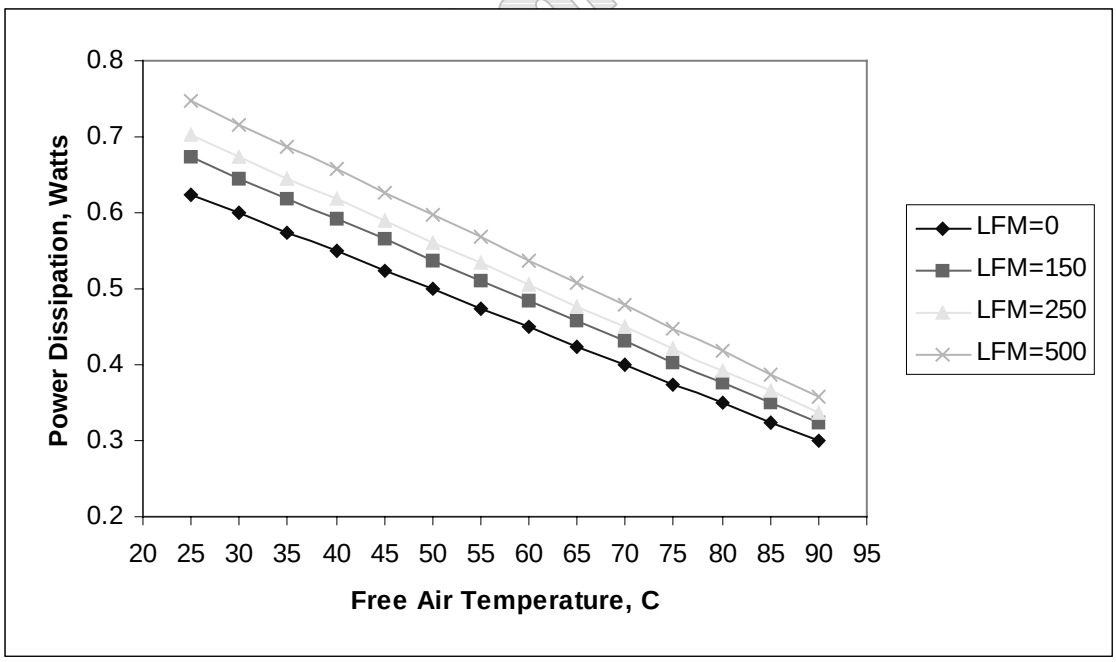


Figure 15. 16-Pin QFN Power Dissipation on JESD 51-3 (1S0P) Test Card

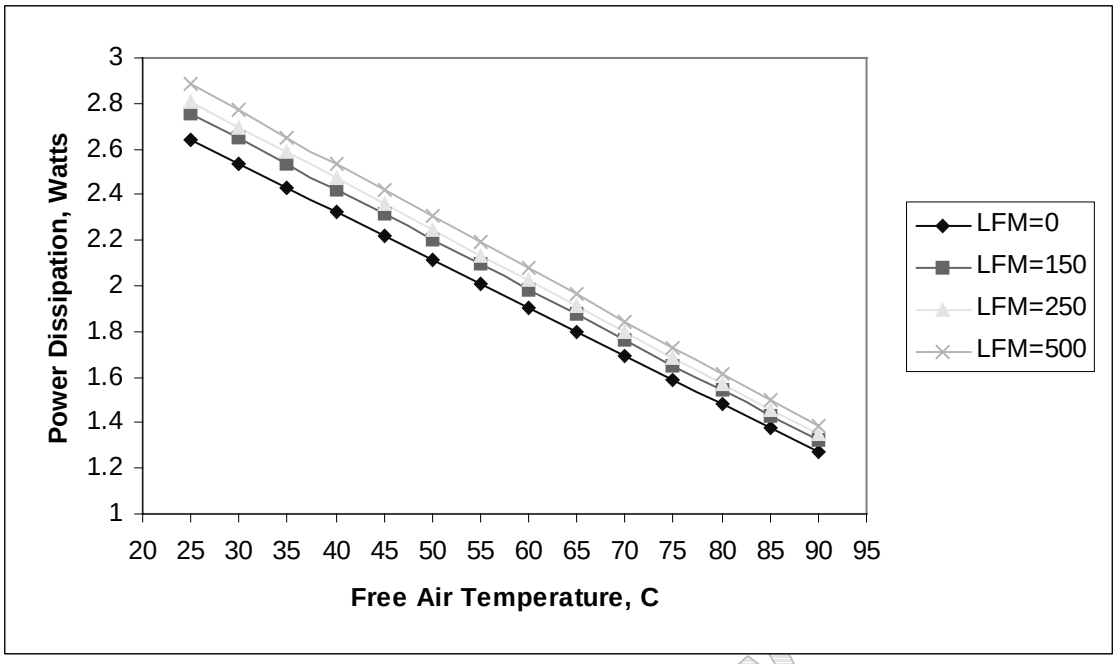


Figure 16. 14-Pin QFN Power Dissipation on JESD 51-5 (1S2P Direct Attach) Test Card

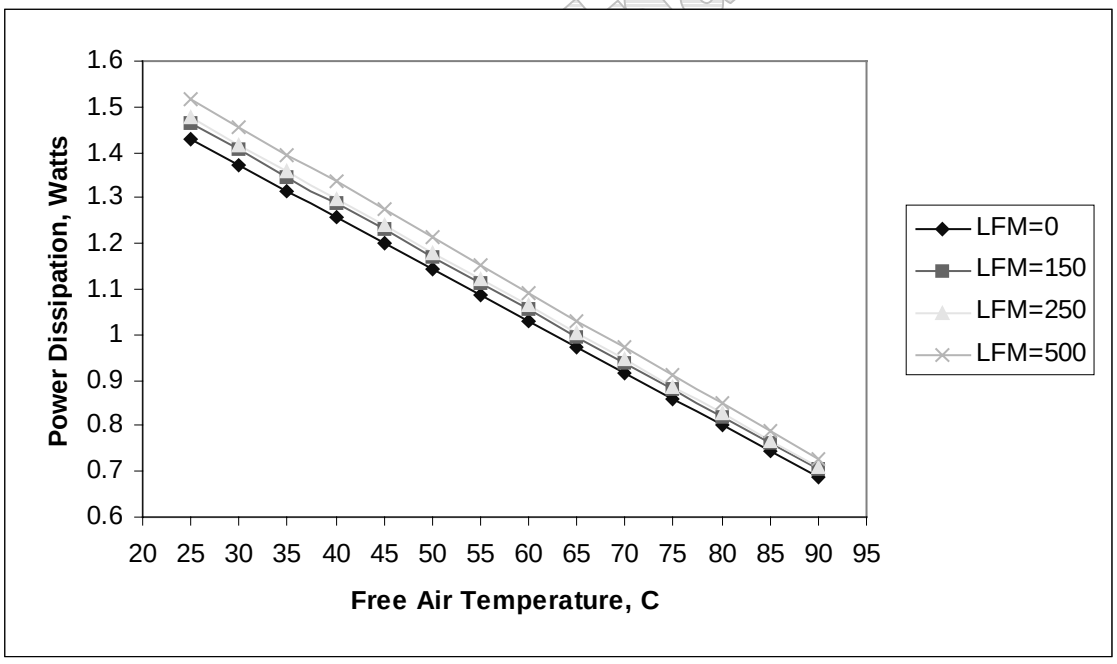


Figure 17. 14-Pin QFN Power Dissipation on JESD 51-7 (1S2P) Test Card

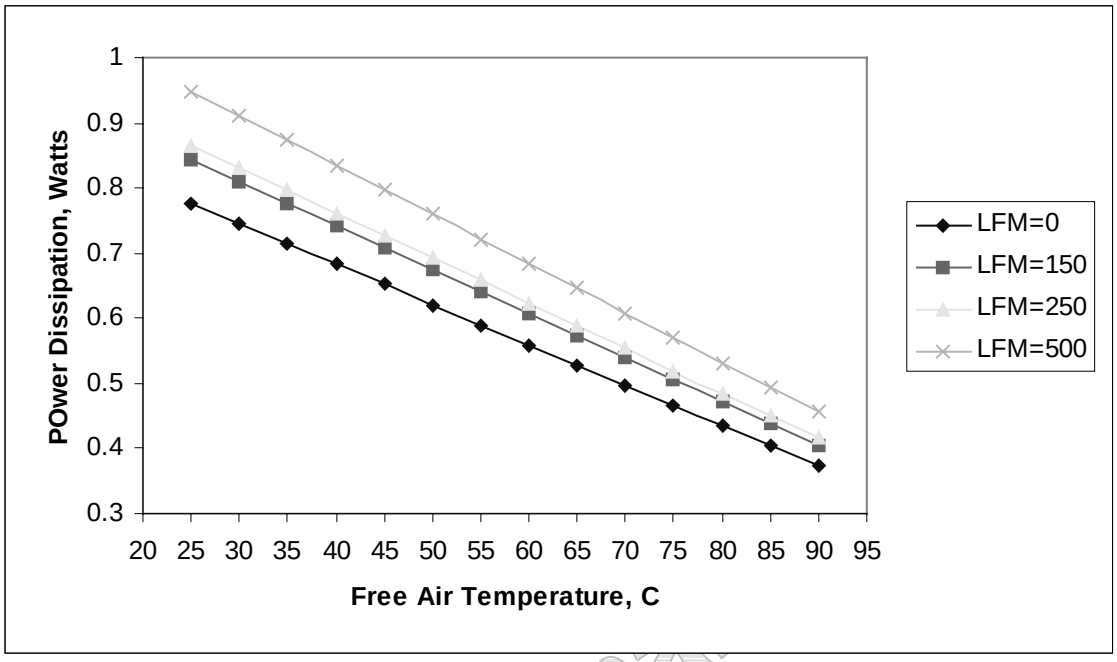


Figure 18. 14-Pin QFN Power Dissipation on JESD 51-3 (1S0P) Test Card

The largest single factor impacting power dissipation is board construction. For these JEDEC test cardsused to obtain results in Figures 10 through 18, the JESD 51-5 direct attach standard offers the best performance. Figures 19 through 22 show the effect of board construction on power dissipation and thermal impedance for the QFN packages.

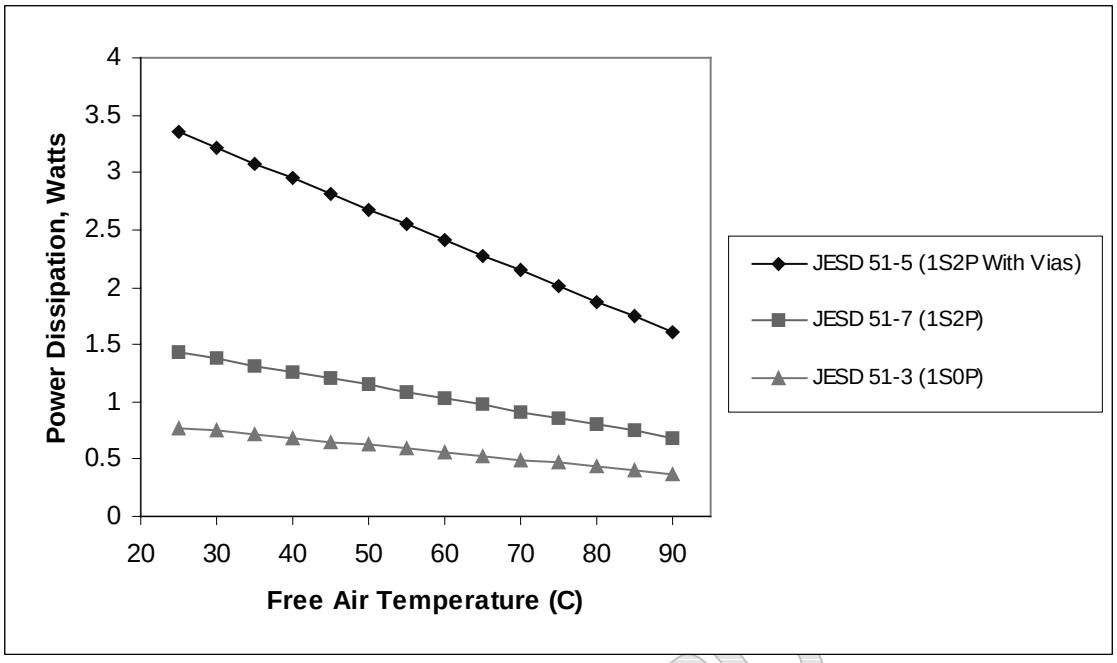


Figure 19. The Effect of Board Layers and Vias on 20-Pin QFN Power Dissipation (JEDEC Test Cards)

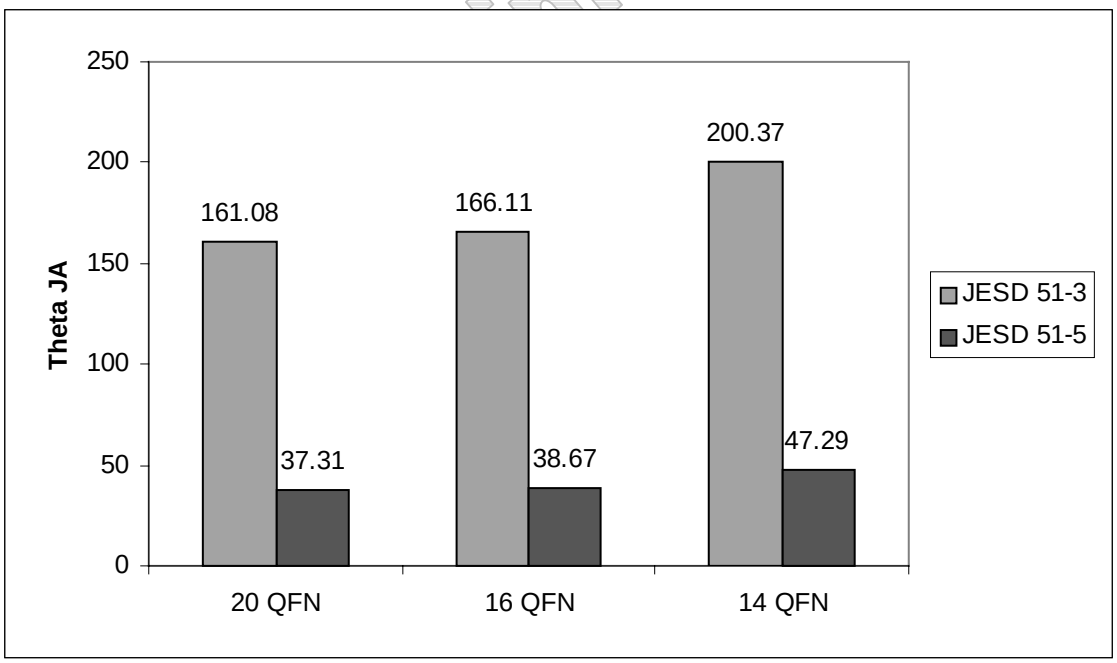


Figure 20. Effect of Board Layers and Vias on θ_{JA} (JESD 51-3 vs JESD 51-5)

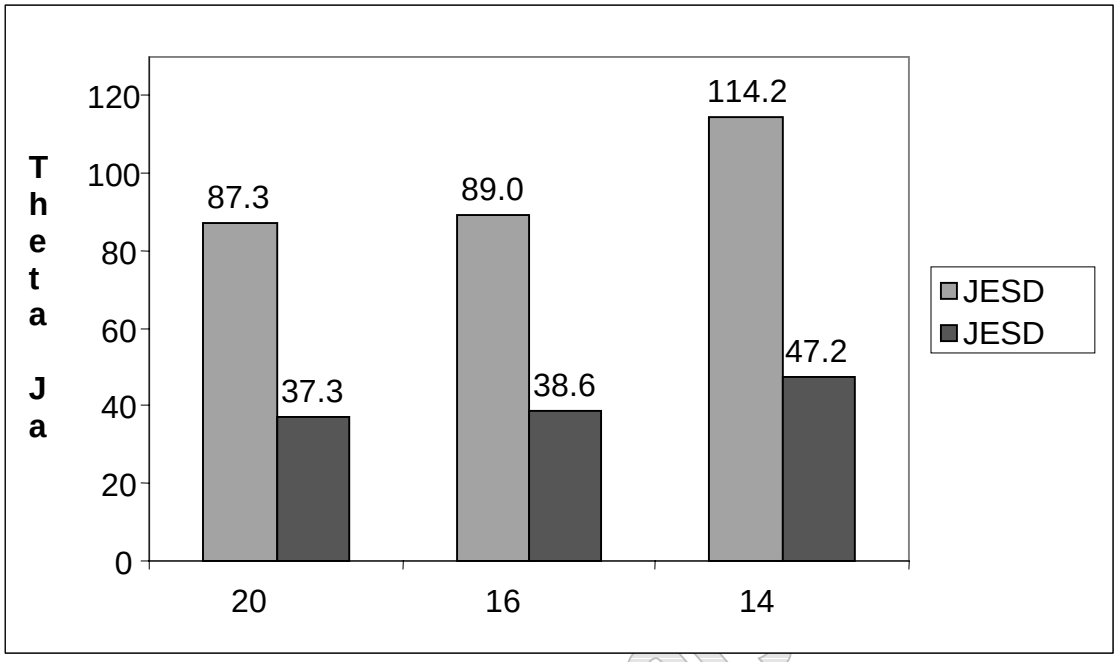


Figure 21. Effect of Board Layers and Vias on θ_{JA} (JESD 51-3 vs JESD 51-5)

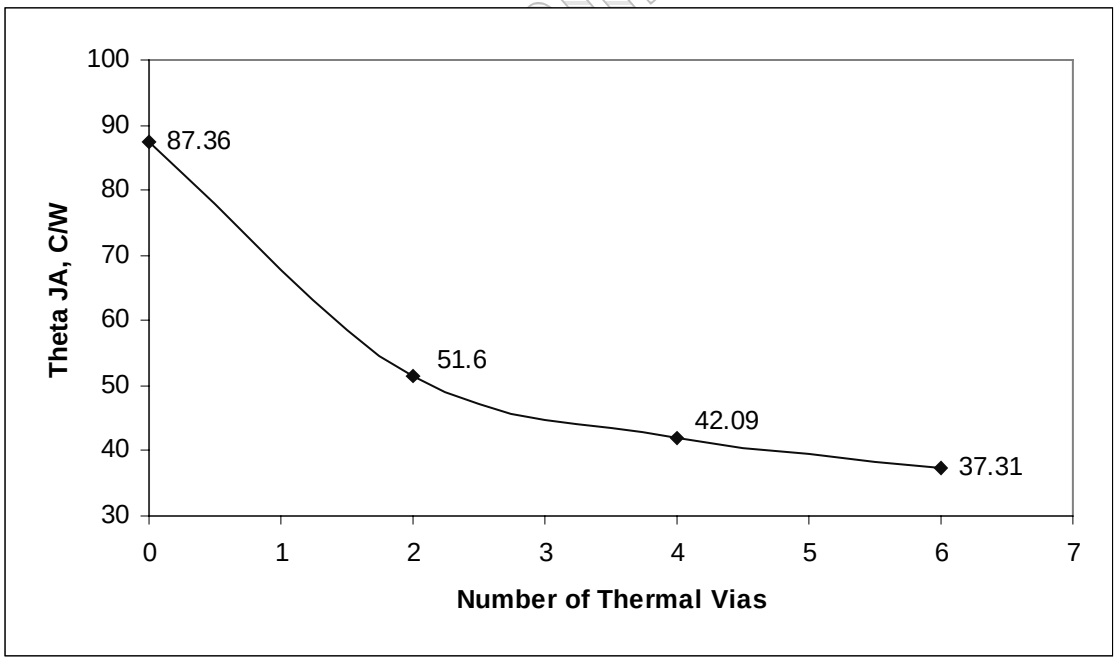


Figure 22. Modeled Theta θ_{JA} vs Number of Thermal Vias on JESD 51-5 Test Card (20-Pin QFN)

Figures 23 through 25 compare the junction-to-ambient thermal impedance of the QFN packages to popular packaging alternatives. These modeled values are on the applicable high-thermal -conductivity boards, per JESD 51-5 and JESD 51-7.

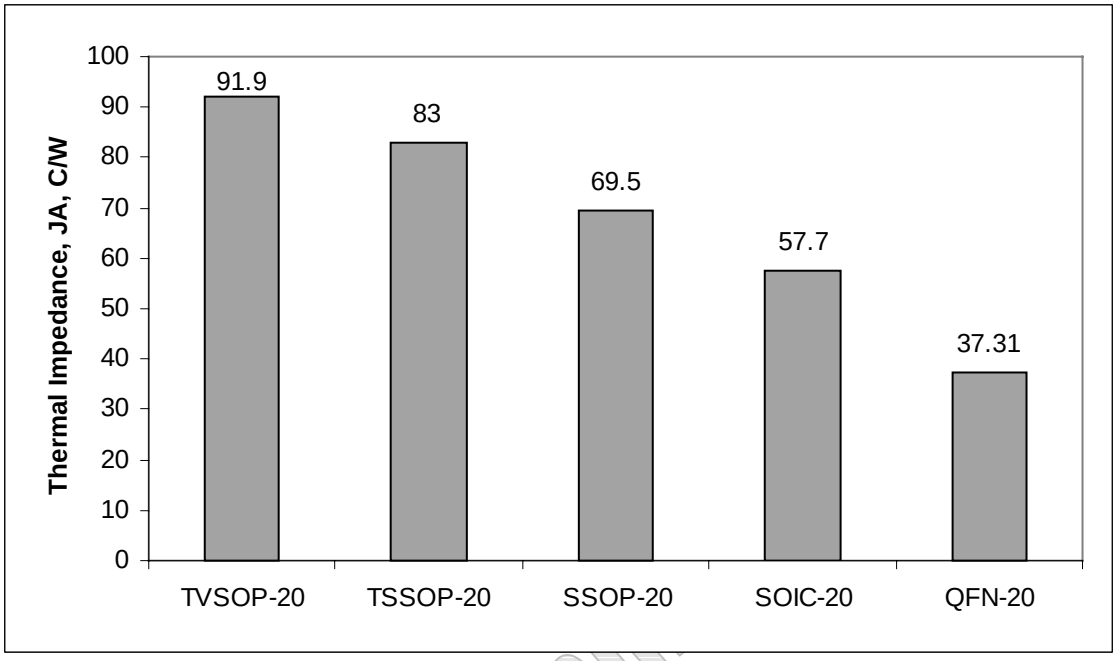


Figure 23. Modeled Thermal Impedance of 20-Pin QFN vs Alternative Packaging

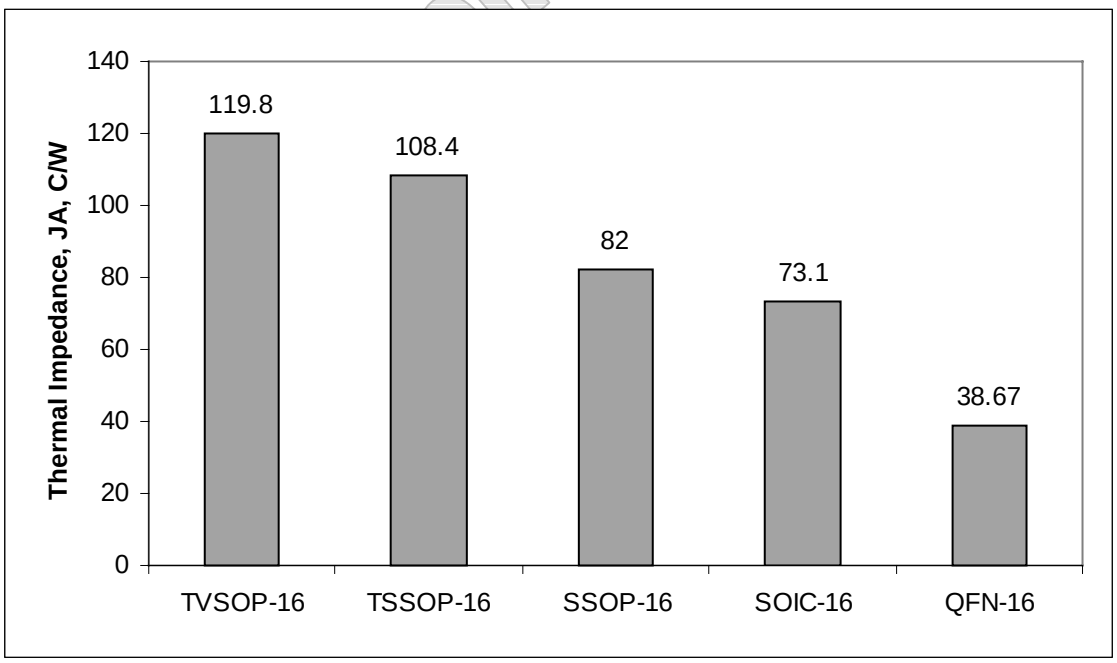


Figure 24. Modeled Thermal Impedance of 16-Pin QFN vs Alternative Packaging

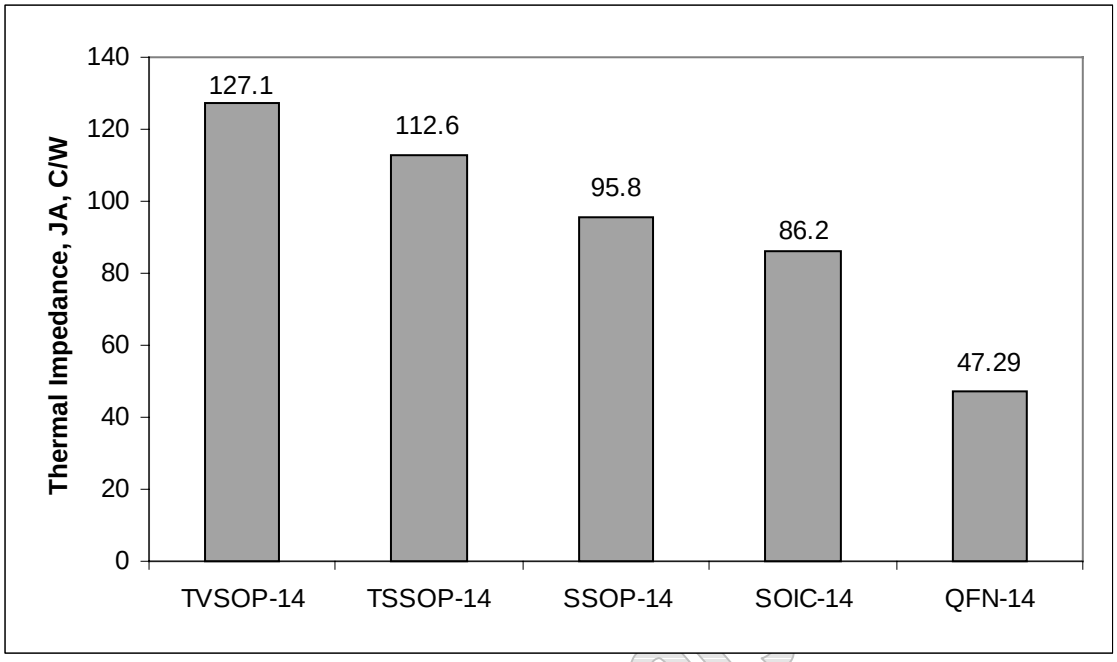


Figure 25. Modeled Thermal Impedance of 14-Pin QFN vs Alternative Packaging

3.5 Electrical

Inductance is directly related to the length of a wire and its proximity to the ground plane. Any wire naturally creates an inductor. The longer the wire, the greater is its inductance. Inductance occurs when current is induced into a wire, creating an electromagnetic field. The closer this induced electromagnetic field is to ground, the less effective it becomes. As the wire gets shorter and/or closer to the ground plane, its inductance decreases.

Capacitance is created when two plates (wires, lines, or layers) overlap and are separated by a given distance. This distance can be insulated by air, plastic, glass, or other materials. Capacitance can be calculated by:

$$C = (0.225 \epsilon_r A) / d \quad (1)$$

Where:

C = capacitance
ϵ_r = dielectric value of insulator
A = area that plates overlap
d = distance between plates

Area changes the most from package to package. The distances lead to lead and die pad to ground plane varies somewhat, while the dielectric varyof the insulators (ϵ_r) remains relatively constant.

The unique construction of QFN packages reduces both inductance and capacitance. The exposed die pad of the QFN package is at board level following assembly, which minimizes inductance, but slightly increases capacitance (smaller d in equation 1) when grounded. Even with this increase, the QFN package still is superior to other dual in-line packages when capacitance is considered. Tables 6 through 8 and Figures 26 through 28 compare modeled package parasitics of the QFN packages with other packaging options using the same die. Note that these QFN models take the exposed pad into account, and the fact that the pad is grounded to the board ground.

Table 6. Modeled 20-Pin QFN Package Parasitics Comparison

	SOIC-20 (DW)	SSOP-20 (DB)	TSSOP-20 (PW)	TVSOP-20 (DGV)	QFN-20 (RGY)
Avg. R, Ω	0.038	0.040	0.050	0.044	**0.043**
Avg. L, nH	5.012	3.495	2.802	2.561	**1.178**
Avg. C, pF	0.717	0.420	.0.317	0.342	**0.252**

Table 7. Modeled 16-Pin QFN Package Parasitics Comparison

	SOIC-16 (D)	SSOP-16 (DB)	TSSOP-16 (PW)	TVSOP-16 (DGV)	QFN-16 (RGY)
Avg. R, Ω	0.039	0.048	0.045	0.039	**0.030**
Avg. L, nH	3.453	3.536	2.593	2.543	**0.818**
Avg. C, pF	0.521	0.376	0.281	0.386	**0.236**

Table 8. Modeled 14-Pin QFN Package Parasitics Comparison

	SOIC-14 (D)	SSOP-14 (DB)	TSSOP-14 (PW)	TVSOP-14 (DGV)	QFN-14 (RGY)
Avg. R, Ω	0.031	0.044	0.032	0.035	**0.029**
Avg. L, nH	3.109	3.551	2.378	2.499	**0.791**
Avg. C, pF	0.473	0.402	0.314	0.361	**0.226**

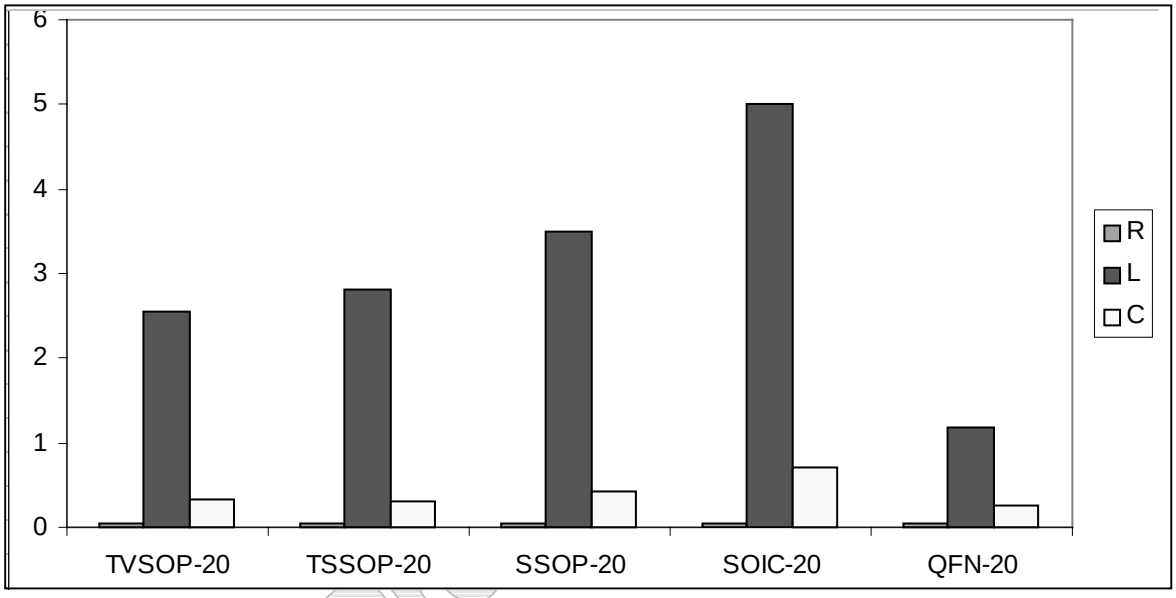


Figure 26. Modeled 20-Pin Package Parasitics Comparison

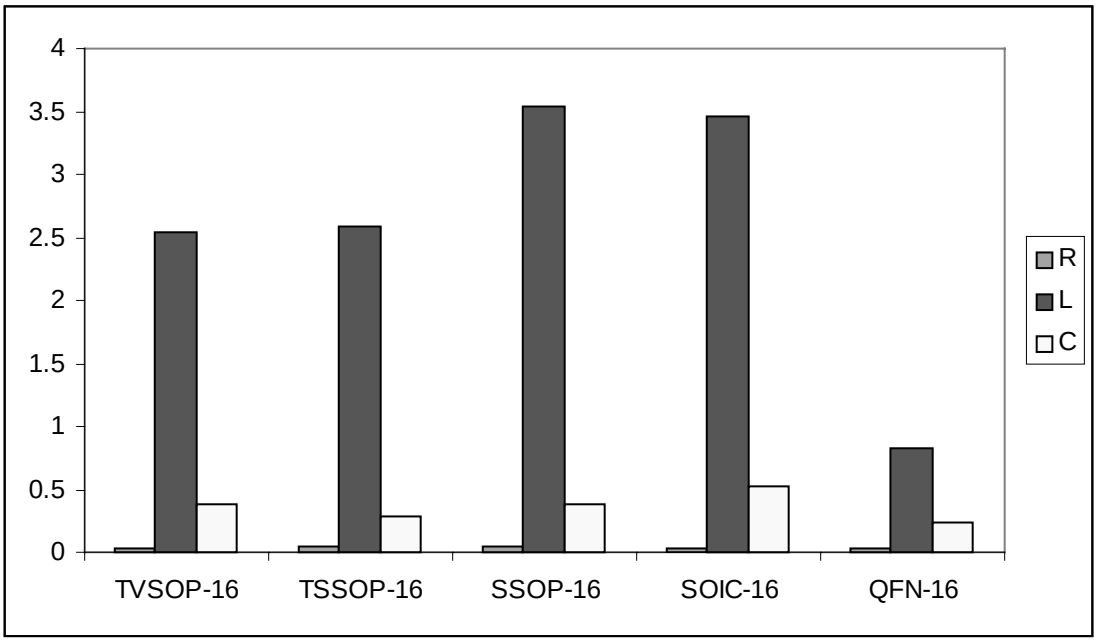


Figure 27. Modeled 16-Pin Package Parasitics Comparison

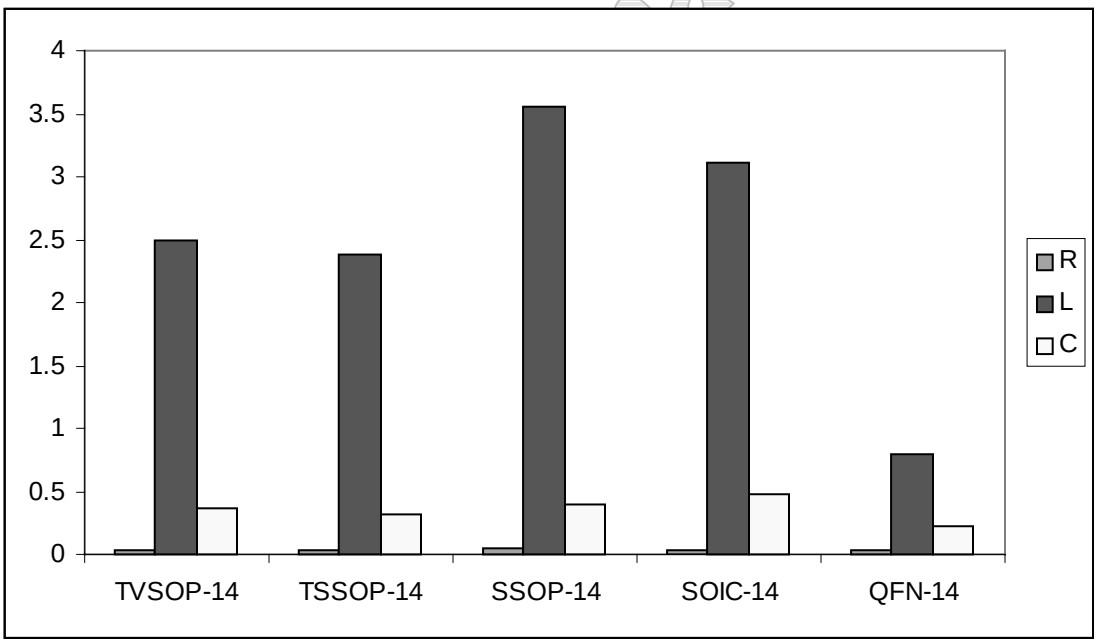


Figure 28. Modeled 14-Pin Package Parasitics Comparison

3.6 Board-Level Reliability

When soldered, the QFN exposed-pad design acts as a package anchor, significantly increasing the board-level reliability over that of an LCC or other leadless packages. The exposed pad must be soldered to provide the structural integrity expected by industry, as well as optimal thermal performance.

There is a significant amount of historical data on QFN board-level reliability available. Various sizes of QFN packages have shown good performance in temperature cycling, key push, vibration, drop, and three-point bending tests.

A 4 mm X 4 mm 16-pin QFN package passed 2000 thermal cycles when mounted to a 0.9-mm-thick FR-4 PCB with NiAu pad finish and SnPb eutectic solder paste. The temperature cycle was –40 to 100°C, with a 30-minute dwell and a 3-minute transition. The failure criterion was a resistance increase to 0.5 Ω, or more, for 200 ns or longer.

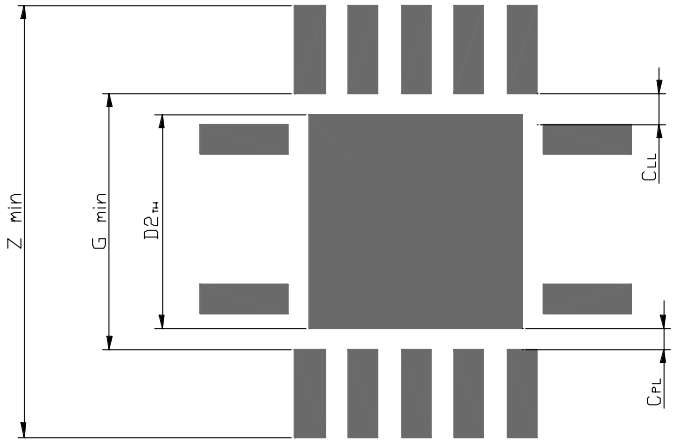
4 Board-Level Assembly

4.1 PCB Design Guidelines

One of the key efforts in implementing the QFN package is the design of the land pattern. The QFN has rectangular metal terminals exposed on the bottom peripheral surface of the package body. Electrical and mechanical connections between the component and the PCB are made by screen-printing solder paste on the PCB and reflowing the paste after placement. To ensure reliable solder joints, on properly designing the land pattern to the QFN terminal pattern is essential. IPC-SM-782 is used as the standard for the PCB land-pad designs.

There are two basic designs for PCB land pads for the QFN package: non-solder-mask-defined (NSMD) and the solder-mask-defined (SMD) styles. The industry has debated the merits of both styles of land pads, and, although we recommend the NSMD pad, both styles are acceptable for use with the QFN package. NSMD pads are recommended over SMD pads because of the tighter tolerance on copper etching than solder masking. NSDM, by definition, also provides a larger copper pad area and allows the solder to anchor to the edges of the copper pads, thus providing improved solder-joint reliability.

Figure 29 illustrates the critical dimensions of a generic QFN land pattern.



Symbol	Description
Zmax	Terminal Land Pad – Outside dimension.
Gmin	Terminal Land Pad – Inside dimension
X	Terminal Land Width
Y	Terminal Land Length
CLL†	Minimum distance between two perpendicular lands in any corner
CPL†	Minimum distance between die paddle and inside edge of terminal pad

CLL and CPL are Clearance Dimensions defined to prevent solder bridging.

Figure 29. Critical Dimensions of 14-Pin QFN Package Land Pad

4.2 PWB Land-Pattern Design

As a general rule, the PWB terminal pads should be designed 0.2 mm to 0.5 mm longer (away from package center) than the package terminal length for good solder filleting, and also should be extended 0.05 mm toward the centerline of the package (see Figure 30). The pad width should be the maximum width of the component terminal for lead pitches below 0.65 mm to minimize solder bridging. These pad designs are wide enough to allow for via-in-pad routing techniques to be employed on an economical basis. Single-layer routing or standard via outside the package outline also is feasible because of flow-through design.

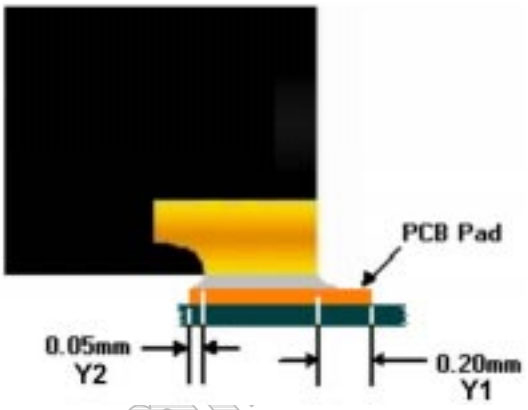


Figure 30. Cross Section of QFN Terminal-Land-Pad Geometry

Zmin should accommodate the maximum package length or width (D or E), the profile tolerances of the package body (aaa = 0.10 mm for these packages), plus the recommended extensions (Y1) for fillet on both ends of the package (0.2 mm x 2). In other words:

$$Zmin = D\ bsc + aaa + 2(Y1) = D + 0.15\ mm + 0.4\ mm \quad (2)$$

$$Zmin = E\ bsc + aaa + 2(Y1) = E + 0.15\ mm + 0.4\ mm \quad (3)$$

Gmin should be designed so that the worst case of maximum terminal length is accommodated. In this case, Gmin is calculated as follows:

$$Gmin = D\ bsc - 2(Lmax) - 2(Y2) = D - 2(0.50) - 2(0.05) \quad (4)$$

$$Gmin = E\ bsc - 2(Lmax) - 2(Y2) = E - 2(0.50) - 2(0.05) \quad (5)$$

The construction of the exposed pad QFN provides enhanced thermal and board-level reliability characteristics. In order to take full advantage of this feature the pad must be physically connected to the PCB substrate with solder.

The thermal pad (see $D2_{th}$ in Figure 29) should be greater than D2 (exposed pad width) of the package whenever possible. However, adequate clearance (Cpl > 0.15 mm) must be met to prevent solder bridging. If this clearance cannot be met, reduce the area $D2_{th}$.

In other words:

$D2_{th}$ >D2 only if $D2_{th}$ < Gmin - (2 x Cpl) (6)

$E2_{th}$ >E2 only if $E2_{th}$ < Gmin - (2 x Cpl) (7)

$D2_{th}$ max = Gmin – 2 (Cpl) = Gmin-2 (0.20) (8)

$E2_{th}$ max = Gmin – 2 (Cpl) = Gmin-2 (0.20) (9)

An example of this design is illustrated below for the 20 QFN. Refer to the package drawing (Figure 4) for package dimensions and to Figure 31 for the land-pad design. Figures 32-33 below use the same criteria and detail the land-pad design recommendations for 16- and 14-pin QFN packages. All dimensions are in millimeters.

Zmin = D *bsc* + aaa +2 (Y1) = 4.5 +0.15 + 2(0.2) = 5.05

Zmin = E *bsc* + aaa +2 (Y1) = 3.5 +0.15 + 2(0.2) = 4.05

Gmin = D *bsc* –2 (Lmax) = 4.5 – 2(0.50) -2(.05) = 3.4

Gmin = E *bsc* –2 (Lmax) = 3.5 – 2(0.50) -2(.05) = 2.4

$D2_{th}$ max = Gmin-2 (Cpl) = 3.4 – 2(0.20) = 3.0

$E2_{th}$ max = Gmin – 2 (Cpl) = 2.4-2(0.20) = 2.0

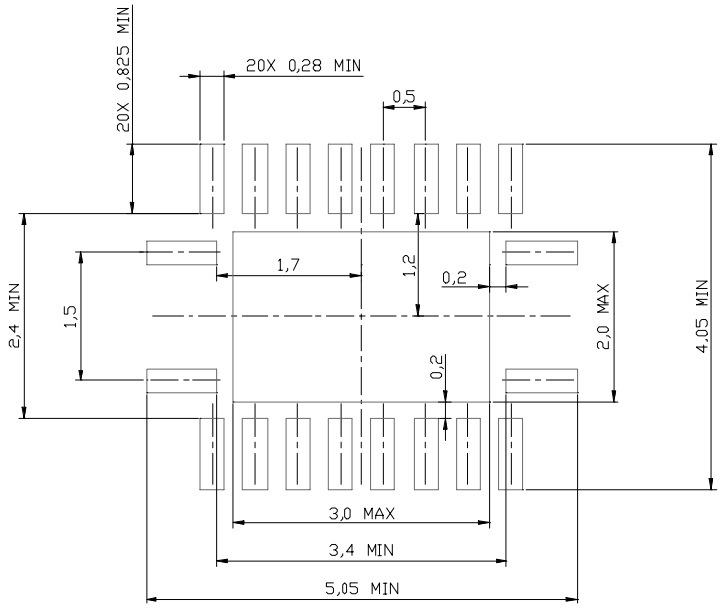


Figure 31. 20-Pin QFN Recommended PCB Land Pad Design

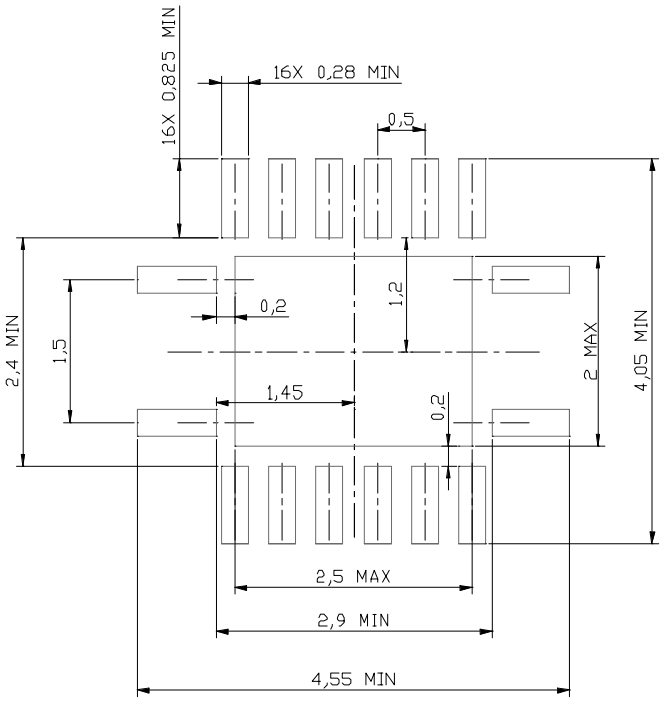


Figure 32. 16-Pin QFN Recommended PCB Land-Pad Design

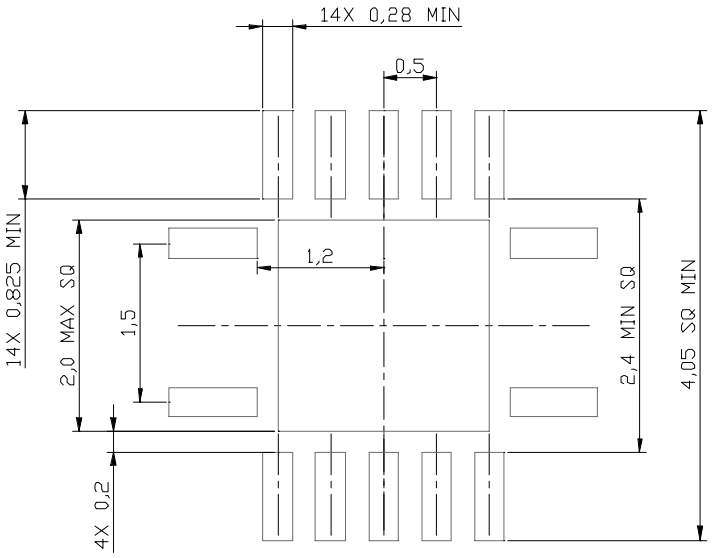


Figure 33. 14-Pin QFN Recommended PCB Land-Pad Design

4.3 Stencil Design

The size difference between the large exposed pad and small terminal leads of the QFN can present a challenge in producing an even solder-line thickness. Because of this, careful consideration must be given to stencil design. Stencil thickness, as well as the etched-pattern geometry, determines the volume of solder paste deposited onto the land pattern. Stencil alignment accuracy and consistent solder-volume transfer is critical for uniform results in the solder reflow process. Stencils usually are made of polymer or stainless steel, with stainless steel being more durable and providing less deformation in the squeegee step. Apertures should be trapezoidal in cross section to ensure uniform release of the solder paste and to reduce smearing. The solder-joint thickness for QFN terminal leads should be 50 µm to 75 µm. Stencil thickness is usually in the 100 µm to 150 µm (0.004 in. to 0.006 in.) range. If a step-down stencil design is not used, the SMT device(s) that prove to be the limiting factor on the PCB determine the actual thickness of the stencil.

A squeegee durometer of 95, or harder, should be used. The blade angle and speed must be optimized to ensure even paste transfer. Characterization of the stencil output is recommended before placing parts.

As a guide, a stencil thickness of 0.1016 mm to 0.125 mm (4mils to 5 mils) for these specific QFN packages is recommended. Figures 34 through 36 detail the stencil recommendations for the 14-, 16-, and 20-QFN packages. All designs below have area ratios > 0.66 and paste-transfer efficiencies of 73% for terminal pads and 100% for thermal pads at a stencil thickness of 0.127 mm (5 mils). At a stencil thickness of 0.1016 mm (4 mils), the area ratio is 0.86, terminal-pad paste-transfer efficiency is 89% and 100% for the thermal pad. The slotted-thermal-pad stencil design is recommended so that the QFN will not float during reflow and cause opens between the terminal leads and pads. This feature also allows adequate room for outgassing of paste during the reflow operation, thus minimizing voids.

A low-residue, no-clean Type 3 or 4 solder paste is recommended, for use with either the SnPb or SnAgCu paste.

Stencil design advice and parameters are provided courtesy of Cookson Electronics, Assembly Materials Group, at http://www.cooksongroup.co.uk/

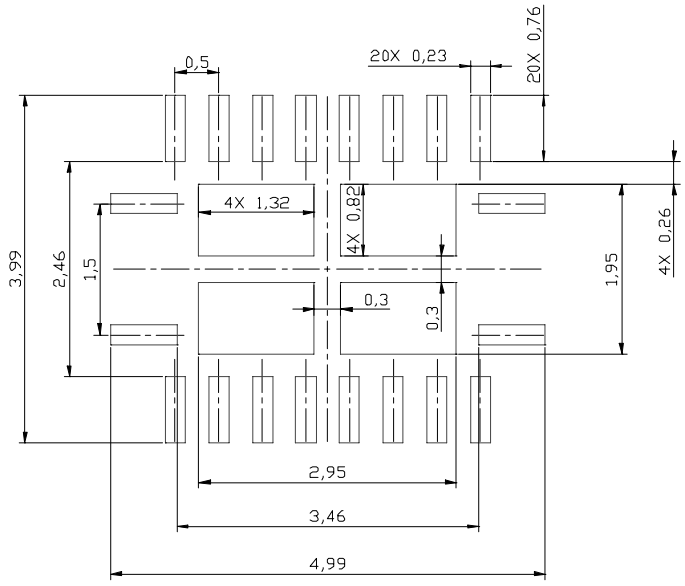


Figure 34. 20-Pin QFN Stencil Design Recommendation

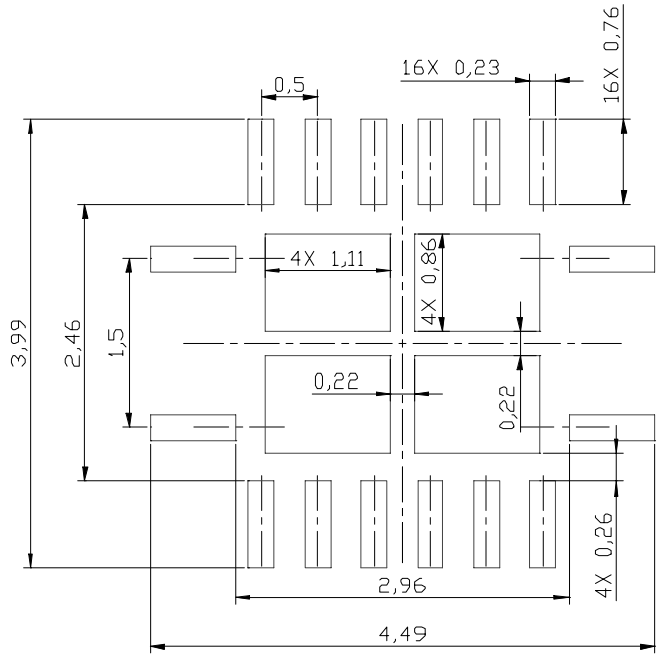


Figure 35. 16-Pin QFN Stencil Design Recommendation

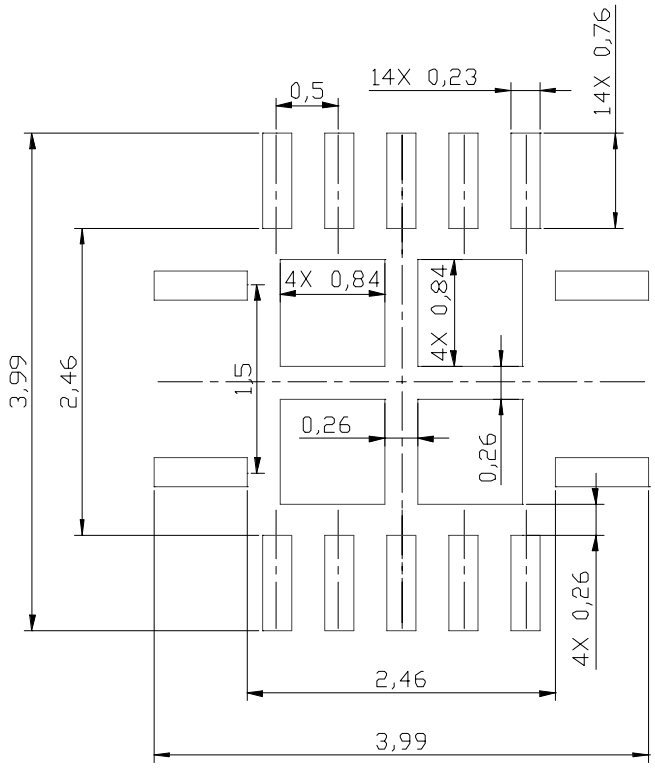


Figure 36. 14-Pin QFN Stencil Design Recommendation

4.4 Component Placement and Reflow

The accuracy of the pic-and-place equipment governs the package placement and rotational (theta) alignment. Slightly misaligned parts (less than 50 percent off the terminal pad center) will automatically self-align during reflow. Grossly misaligned packages (greater than 50 percent off terminal pad center) should be removed prior to reflow, as they may develop electrical shorts from solder bridges.

There are two popular methods for package alignment using machine vision:

- Package silhouette—the vision system locates the package outline
- Lead-frame recognition—Some vision systems can directly locate on the lead-frame pin-1 ID feature (chamfer in exposed pad).

Both methods are acceptable for MLP placement, but both have advantages and disadvantages. The pad-recognition-type alignment tends to be more accurate, but is also slower since more complex vision processing is required of the pick-and-place machine. The package silhouette method allows the pick-and-place system to run faster, but generally is less accurate.

Both methods are acceptable, and have been successfully demonstrated by major pick-and-place equipment vendors and contract assembly houses.

There are no special requirements when reflowing QFN packages. As with all components, it is important that reflow profiles be checked on all new board designs at different locations on the board because component temperatures may vary because of surrounding thermal sinks, location of the device on the board, and package densities.

It is recommended that the maximum reflow temperature, soak times, and ramp rates specified for a specific solder paste not be exceeded. Please consult your paste manufacturer for specifics regarding your particular paste because target temperatures and their associated times can vary widely, depending upon metallurgy and flux composition. In general, SnPb peak temperatures will be approximately 235°C and Pb free will be 250 to 260°C. The matte tin finish used for these QFN packages has proven interchangeability with either paste type.

A generic PB-free paste reflow profile with time/temperature targets is shown in Figure 37. Temperatures shown are pad temperatures.

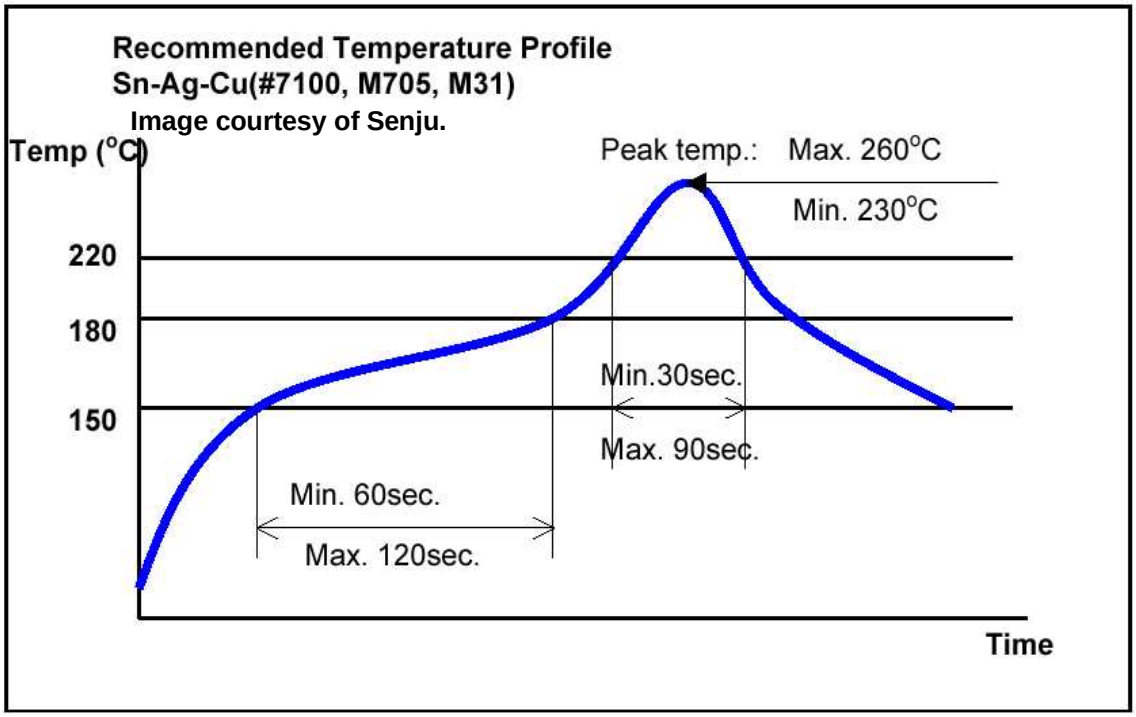


Figure 37. Pb-Free Paste Reflow Profile

4.5 Rework

QFN rework processes are an adaptation (and in some cases a simplification) of ball grid array package rework processes. The basic elements of this process are:

- Board preheat
- Reflow of component solder
- Vacuum removal of component
- Cleaning and preparation of PWB lands
- Screening of solder paste
- Placement and reflow of new component
- Inspection of solder joints

Several automated rework systems exist in the market and address the previous steps in a variety of ways. One system worth noting is by Air-Vac Engineering (http://www.air-vac-eng.com). The rework steps above (except inspection) can be accomplished with high precision on a single machine under either computer or manual control.

Another example of a well-established rework system is the Metcal APR-5000. This system contains the essential hardware and automated software features necessary for reworking QFN and other packages. This system takes up less than 6 ft^2 of manufacturing floor space. Closed-loop, computer-controlled time, temperature, and airflow parameters help ensure process control and repeatability. The system software manages the reflow, profile: preheat, soak, ramp, reflow and cooling. In addition, board temperature can be monitored using three integrated flying thermocouples, and real-time adjustment can be made to all parameters while the profile is running.

A variety of off-the-shelf vacuum collets and solder screens are available from Metcal. Please reference http://www.Metcal.com for open tools and for custom tooling requirements.

5 Tape and Reel

5.1 Material Specifications

TI offers tape-and-reel packing for 14-, 16-, 20-pin logic QFN packages in standard packing quantities (SPQ) of 1000 units/reel. The units are shipped in embossed carrier tape, sealed with heat-activated or pressure-sensitive cover tape on plastic reels. All of the tape-and-reel materials comply with EIA-481 B, and EIA-541. [5,6] The EIA specifications are shown in Table 9 and Figures 38 through 40. The carrier tape is made of conductive polystyrene and has a surface resistivity that falls within the static-dissipative range ($1x10^6$ to $1x10^{11}$ ohms/square). Heat-activated or pressure-sensitive, antistatic, clear polyester film is used for the cover tape. The dimensions of most interest to the end user are tape width (W), pocket pitch (P), and pocket size (Ao, Bo, Ko) as shown in Figure 38.

The units are placed in the carrier tape pocket, with pin 1 located as detailed in EIA-481B. The longest axis of the package is perpendicular to the tape sprocket holes, and pin 1 is closest to the round sprocket holes. Thus, for rectangular or square packages, pin 1 is located in quadrant 1 per (see Figure 40). The 3.5 x 4.5 mm 20-pin QFN is shown in Figure 41. All dimensions are in millimeters.

Table 9. Carrier Tape Dimensions in Millimeters

Package	Carrier-Tape Width (W)	Pocket Pitch (P)	Pocket Width (A_o)	Pocket Length (B_o)	Pocket Depth (K_o)	Device Quantity Per Reel (SPQ)
14-Pin QFN	12.0 ± 0.30	8.0 ± 0.10	3.80 ± 0.10	4.80 ± 0.10	1.20 ± 0.10	1000
16-Pin QFN	12.0 ± 0.30	8.0 ± 0.10	3.80 ± 0.10	4.30 ± 0.10	1.20 ± 0.10	1000
20-Pin QFN	12.0 ± 0.30	8.0 ± 0.10	3.80 ± 0.10	3.80 ± 0.10	1.20 ± 0.10	1000

D_o	D_1 Min	E_1	P_o	P_2	R Ref.	S_1 Min.	T Max.	T_1 o Max.
1.5+0.1 -0.0	1.5	1.75 ± 0.1	4.0 ± 0.	2.0 ±. 05	30	0.6	0.6	0.1

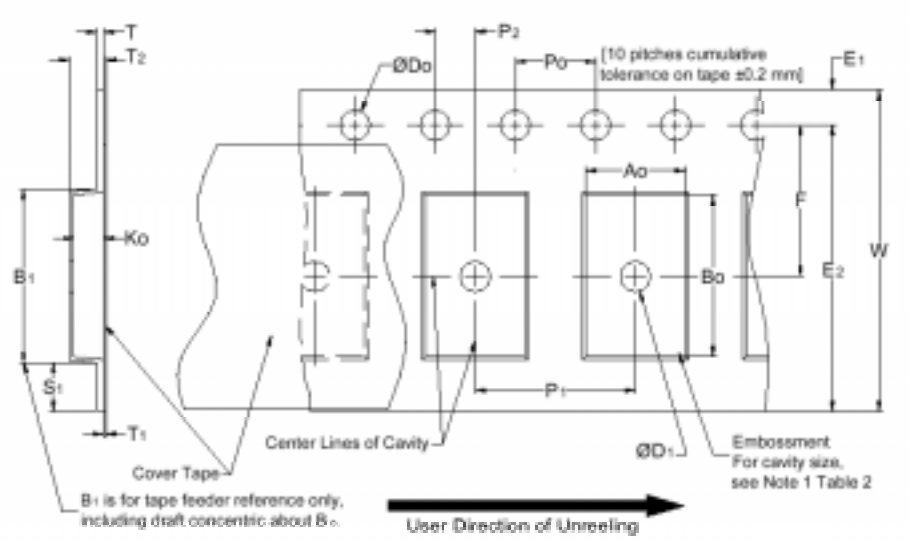
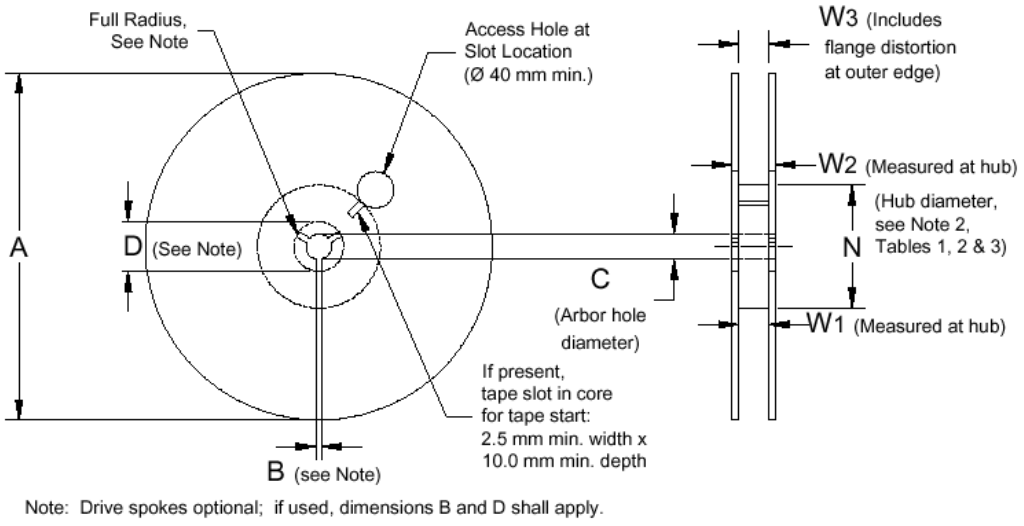


Figure 38. Carrier Tape Drawing



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Reel Diameter (A)	Reel Width (W1)	Hub Diameter Max (N)	Reel Thickness (W2)	Arbor Hole Diameter (C)	Quality/Reel 14/16/20
180 ± 0.60	12.4 + 2.0/-0.0	60 ± 0.50	13.65 ± 1.95	13.0 + .5/-.2	1000

Figure 39. Reel Drawing and Specifications

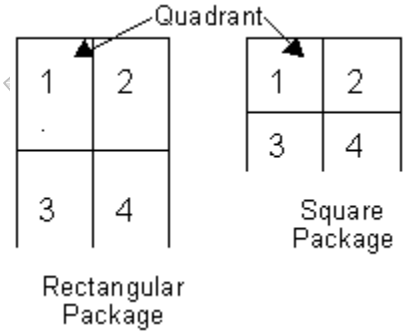


Figure 40. Carrier Tape Pin 1 Quadrant Location per EIA-481B

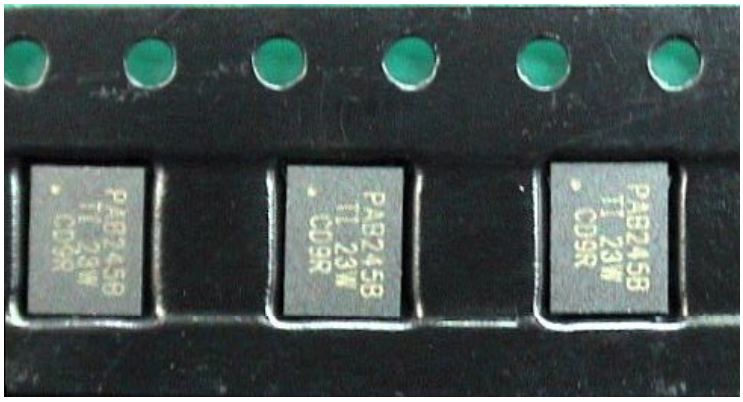


Figure 41. Pin-1 Orientation of QFN Packages

5.2 Labels

All reels have an ESD label or symbol on the hub or sprocket, and a barcode label placed on the same side of the reel and on the side opposite the carrier-tape round sprocket holes, as shown in Figure 42.

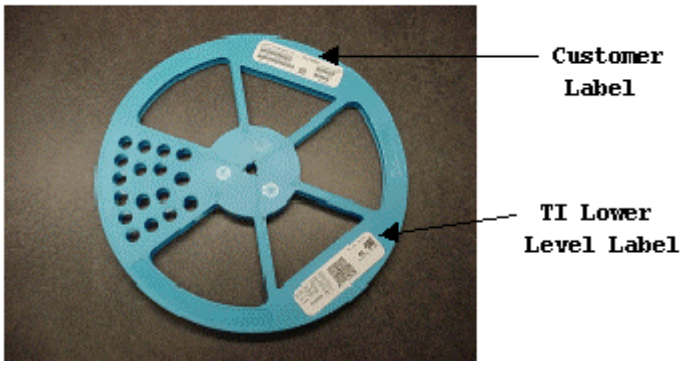


Figure 42. Reel Labeling

Intermediate container orientation and labeling specification for reels is shown as shown in Figures 43 through 45.

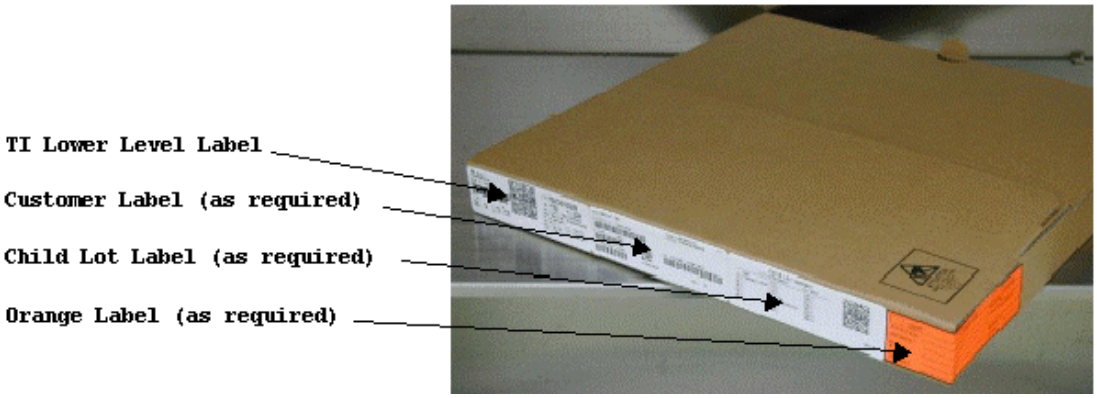


Figure 43. Regular Pizza-Box Label Placement

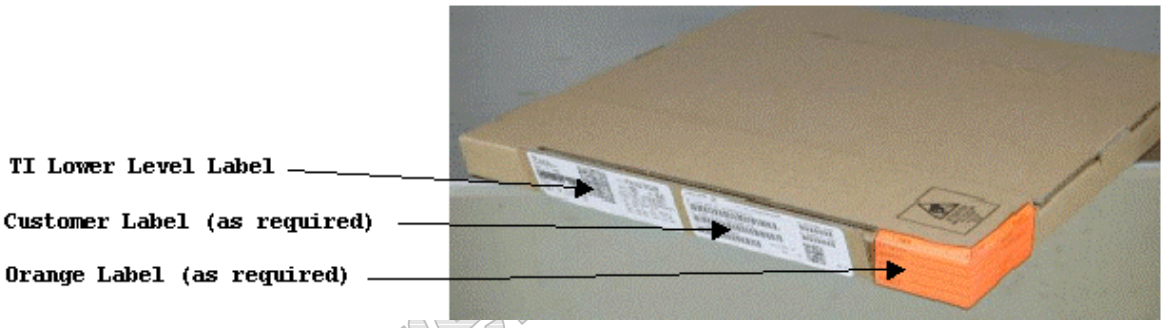


Figure 44. Label Placement On Pizza Box with Flap

Figure 45. Child-Lot Label Placement on Pizza-Box Label Flap

The moisture-caution circle can appear on any surface of the box, except areas that will be occupied by other labels, and the bottom of the box.

5.3 Dry Pack Requirements for Moisture Sensitive Material

Moisture sensitive material as classified by JEDEC standard J-STD-033 must be dry packed. Dry packing limits the exposure of the package to moisture so that it can be re-flowed without “popcorning”. Dry packing consists of desiccant material and a humidity indicator card (HIC) sealed with the populated reel inside a moisture barrier bag (MBB). A representative HIC and MBB are shown below in figures 48 and 49. Table 46 shows the dry pack requirements for MSL 1-2 packages.

Level	Dry Before Bag	MBB	Desiccant	MSID Label	Caution Label
1	Optional	Optional	Optional	Not Required	Not Required
2	Optional	Required	Required	Required	Required

Figure 46. Dry Pack Requirements for MSL 1-2 Packages

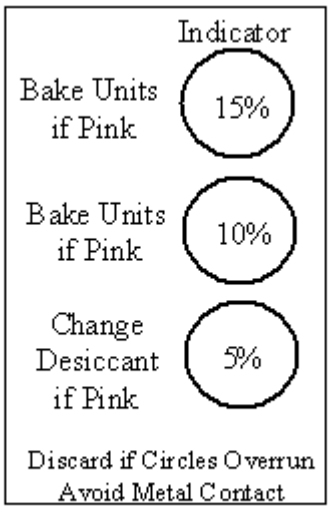


Figure 47. Humidity Indicator Card

Labels will be placed on moisture barrier bags as shown in Figure 48.

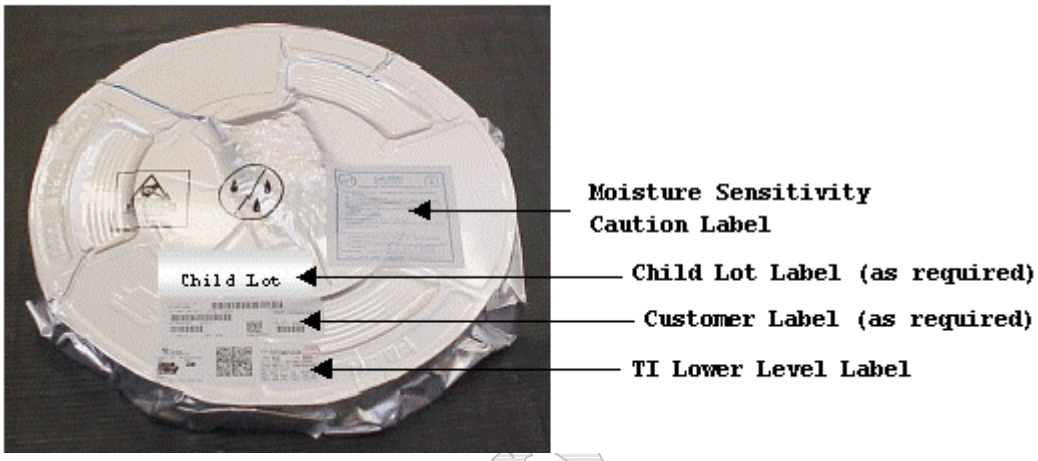


Figure 48. Label Placement on Tape and Reel Moisture Barrier Bag

The required dry pack labels are the "Moisture-Sensitive identification" (MSID) label and the "Caution" label as specified in QSS 007-004. The MSID label shall be affixed to the lowest level-shipping container that contains the MBB. The "Caution" label shall be affixed to the outside surface of the MBB.

The calculated shelf life for dry packed components shall be a minimum of 12 months from the MBB seal date, when stored in a non-condensing atmospheric environment of < 40ºC/90% RH.

Level	Floor Life (out of bag) at factory ambient of +30°C/60% RH or as stated
1	Unlimited at +30°C/85%RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Table 10. Floor Life Under Conditions Other Than 30ºC/60% RH

5.3.1 Symbols and Labels

The symbol shown in Figure 49 indicates that devices are moisture sensitive at level 2 or below and must appear on all moisture sensitive caution labels.

Figure 49. Moisture Sensitive Symbol

The label shown in Figure 50 shall be on the lowest level-shipping container to indicate that moisture-sensitive devices are in the container. This label is recommended to be a minimum of 20 millimeters in diameter.

Figure 50. MSID Label

The moisture sensitive caution label, shown in Figure 51, shall be used for levels 2, 2a, 3, 4, 5, and 5a as defined by J-STD-020. This label is required on the moisture barrier bag and shall provide the following information:

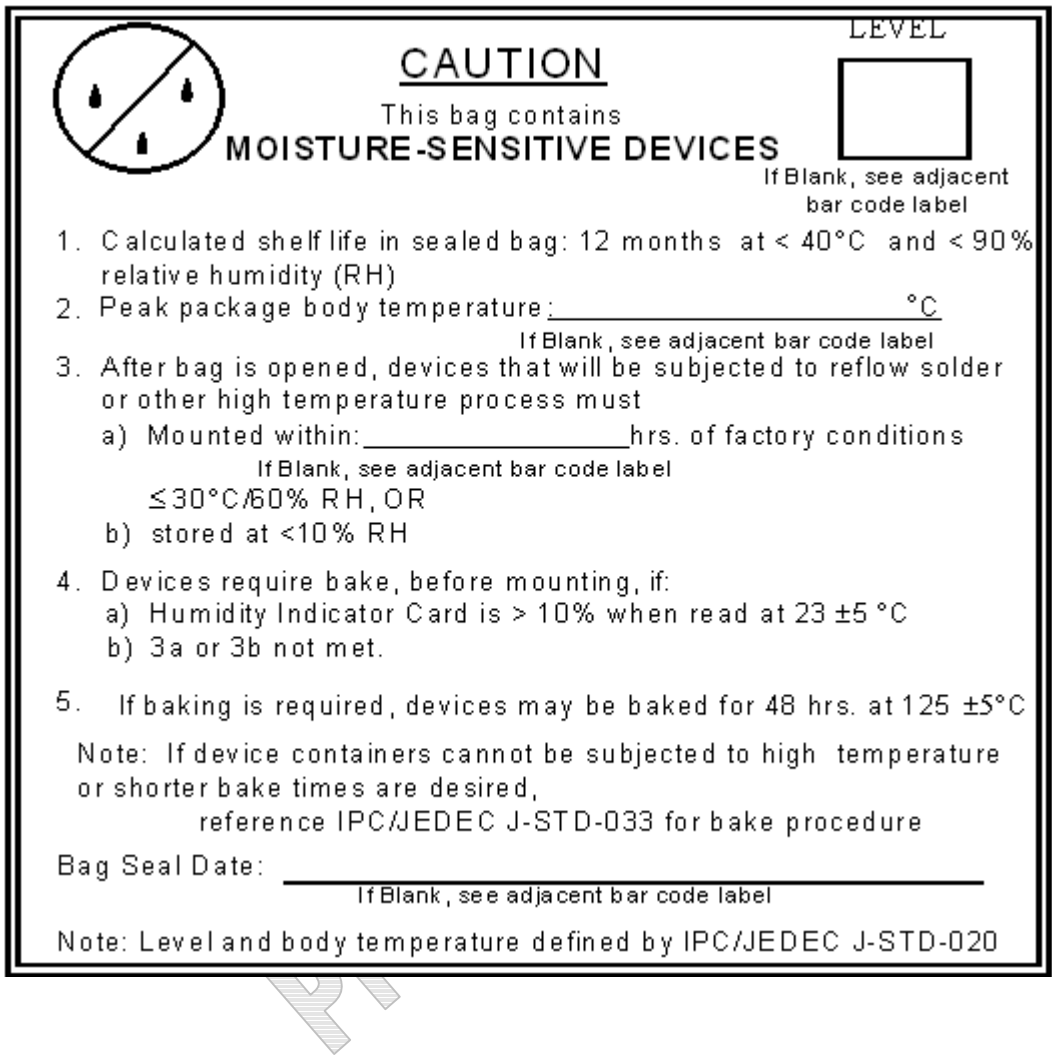


Figure 51. Moisture Sensitive Caution Label for Levels 2-5a

6 Symbolization

The top of the package will be laser marked with device name, corporate ID, date code, assembly-site code, assembly-lot trace code, and pin-1 location. Table 11 shows the symbolization guidelines for 14-pin, 16-pin, and 20-pin QFN packages.

Table 11. Device-Marking Guidelines

QFN Symbolization Guidelines					
Pins	**Package**	**Namerule and Format**	**Maximum Characters per Row**	**Maximum Rows**	**Symbol Format**
14	QFN	C2	7	3	AB245B TI YMS LLLL O
16	QFN	C2	6	3	
20	QFN	C2	6	3	

The symbol-format column in Table 11 has the following definitions:

AB245B = Short device name for SN74ABT245BRGYR
TI = Texas Instruments
Y = Year
M = Month
S = Site code
LLLL = Lot trace code
O = Pin-1 quadrant identifier (data sheet specifies exact Pin-1 location)

For specific marking on any particular device, please see the device data sheet at www.ti.com.

7 Test Sockets

Test sockets for the 14, 16, and 20-pin QFN devices can be obtained from:

Plastronics
2601 Texas Drive
Irving, Texas 75062
Phone: 972-258-2580
Fax: 972-258-6771

Socket part numbers:
20 Pin: 20QN50T14535
16 Pin: 16QN50T23030
14 Pin: 14QN50T23535

8 Features and Benefits

In summary, key features and corresponding advantages for logic products in the QFN package are:

- Superior package parasitics, as compared to traditional dual in-line packaging solutions. Inductance ranges from 54% to76% lower than alternative packages and capacitance ranges from 14% to 64% lower than other comparable packages.
- Superior thermal performance and board-level reliability compared to alternative package solutions. QFN junction-to-ambient thermal impedance ranges from 59-67% lower than TVSOP, 55% to 64% less than TSSOP, 46% to52% less than SSOP, and 35% to 47% less than SOIC. Mechanical integrity of mounted package is greatly enhanced by soldered exposed die pad.
- Conventional one-to-one pinout resembling dual-in-line packages. Keeps ground, V_{CC}, and signal pin numbers consistent with previous dual-in-line packages.
- Pb-free packages with backward-compatible solderability that can be soldered with either SnPb or Pb-free pastes.
- Significant area savings over traditional dual inline packages. QFN is 56% to 62% smaller than its equivalent-pin TSSOP counterpart.
- Provides flow-through layout like conventional dual-in-line packages.

9 Conclusion

Texas Instruments 14, 16, and 20-pin QFN package offerings are leadframe-based leadless packages, with improved thermal performance, electrical performance, and package volume over similar TSSOP, TVSOP, SSOP, and SOIC packages. Additionally, the QFN packages meet the industry's lead-free demands, have reliable solderability using either Pb or Pb-free solder pastes, and can be reworked and manufactured using conventional equipment. The packages allow for product miniaturization and comply with dimensional specifications of JEDEC standard MO-220.

10 Acknowledgments

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11 References

References 1 through 4 are available at:

http://www.jedec.org/download/default.cfm

1. JEDEC Standard MO-220, *Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (HP-VFQFP-N)*

2. JESD 51-5, *Extnesion of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

3. JESD 51-7*, High Effective Thermal conductivity Test Board for Leaded Surface Mount Packages*

4. JESD 51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

5. EIA-481 B, *Taping of Surface Mount Components for Automatic Placement*

6. EIA-541, *Packing Material Standards for ESD Sensitive Items*